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IBIS AMI Modeling of Retimer and Performance Analysis of Retimer based Active Serial Links

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Abstract

This paper presents a novel retimer modeling approach based on IBIS-AMI to capture the performance of a retimer that operates up to 15 Gbps. The retimer model consists of two back-to-back Rx-Tx AMI models. It captured characteristic of the continuous linear time equalizer (CTLE), the variable gain amplifier (VGA), the decision feedback equalizer (DFE), and the clock-data-recovery (CDR) unit. It also implemented the adaptation algorithms for the CTLE, DFE, and CDR by optimizing the eye metric through an eye-monitoring system. The digital signal that drives the Tx model is recovered by the simulator by sampling the Rx AMI_GetWave output waveform at one half UI after each clock tick returned by the Rx AMI_GetWave function. We demonstrate the interoperability between retimer and SerDes models and their loss compensation features in full link simulation. It is shown that the retimer CDR tracks low-frequency jitter and filters high-frequency jitter to improve the system jitter rejection ratio.

Author(s) Biography

Kian Haur (Alfred) Chong is a Senior System Engineer in the WEBENCH® System Development Team at Texas Instruments. His current works emphasize in the development of IBIS-AMI models and architectural of the in house Signal Integrity Simulation Engine. His previous role at TI has been high-speed system definition, system simulation and validation, and physical characterization of high-speed SerDes products from 2.5Gbps to 25+Gbps. He received his Ph.D. from University of Washington in 2006.

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Liang Liu is an application engineer in the Data Path Solution Team at Texas Instruments. He has been with TI since 2010 and focuses on supporting the high speed repeater, CDR and Serdes products. He works on the signal integrity simulation and application supports in the past 6 years. Prior to joining TI, he worked for Maxim and Nokia-Siemens Networks. He received his BSEE from Wuhan University in 2000.

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Fangyi Rao is a master engineer at Agilent Technologies. He received his Ph.D. degree in theoretical physics from Northwestern University. He joined Agilent EEsof in 2006 and works on Analog/RF and SI simulation technologies in ADS and RFDE. From 2003 to 2006 he was with Cadence Design Systems, where he developed the company's Harmonic Balance technology and perturbation analysis of nonlinear circuits. Prior to 2003 he worked in the areas of EM simulation, nonlinear device modeling, and medical imaging.

Introduction

As data rates go higher and higher, serial link designers are facing bandwidth limitation imposed by channel loss. While low-loss dielectric materials and sophisticated SerDes equalization techniques reduce and compensate signal attenuation, they increase the cost and complexity in board and SerDes IC designs. The mid-channel repeater device such as redriver and retimer, which is placed in the middle of the channel to restore and retransmit the signal, is a promising solution to mitigate the channel loss and is increasingly applied in high-speed interconnects. A redriver restores the signal with equalization and pre-emphasis. In addition, a retimer employs clock-data-recovery (CDR) to sample the equalized signal, recover the digital signal, and retransmit it to the downstream channel. With CDR and sampling circuits, a retimer can track and filter jitters in the incoming signal and fully compensate the upstream channel loss.

To analyze and optimize the performance of the entire serial link, behaviors of both active devices and passive channels need to be accurately modeled. IBIS-AMI is proven a powerful method to incorporate SerDes and channel models into a unified simulation environment that protects IC vendors' IP [1]. However, the presence of active nonlinear mid-channel repeaters poses a challenge to the AMI methodology, which is based on the assumption of linear and time-invariant (LTI) channels. An AMI modeling approach for redriver had been proposed in [2], where a redriver is modeled by two back-to-back AMI receiver (Rx) and transmitter (Tx) models, and the redriver Rx algorithmic model's output signal is the input to the redriver Tx algorithmic model. While this approach is a natural way to model redrivers, which are analog devices, it is inefficient when modeling retimer specific processes such as digital signal regeneration and retiming by the CDR.

In this paper an innovative approach for retimer modeling and simulation is presented. The approach directly utilizes clocks generated by the retimer CDR to sample the retimer Rx analog output signal and generate the digital stimulus that drives the retimer Tx. Functionalities of retimer models are described, and the performance of retimer jitter rejection is discussed. A 12Gbps link consists of a SerDes Tx, a retimer and a SerDes Rx, whose models are developed by different IC vendors, is simulated with the proposed method. Improvements of eye open, jitter and bit-error-rate (BER) over channels without retimer are demonstrated. Simulation results are correlated with silicon. The approach is shown to provide interoperability between SerDes, retimer and redriver models.

1. IBIS-AMI Modeling and Simulation Flow for Retimer

As illustrated in Figure 1, a retimer is modeled by two back-to-back AMI Rx and Tx models. Similar to redriver AMI models, the retimer Rx analog model represents the device input termination, and the Tx analog model the output impedance. Retimer Rx and Tx algorithmic models represent equalization, CDR and pre-emphasis. In particular, the Rx algorithmic model must implement the AMI_GetWave function, and the function must return clock times.

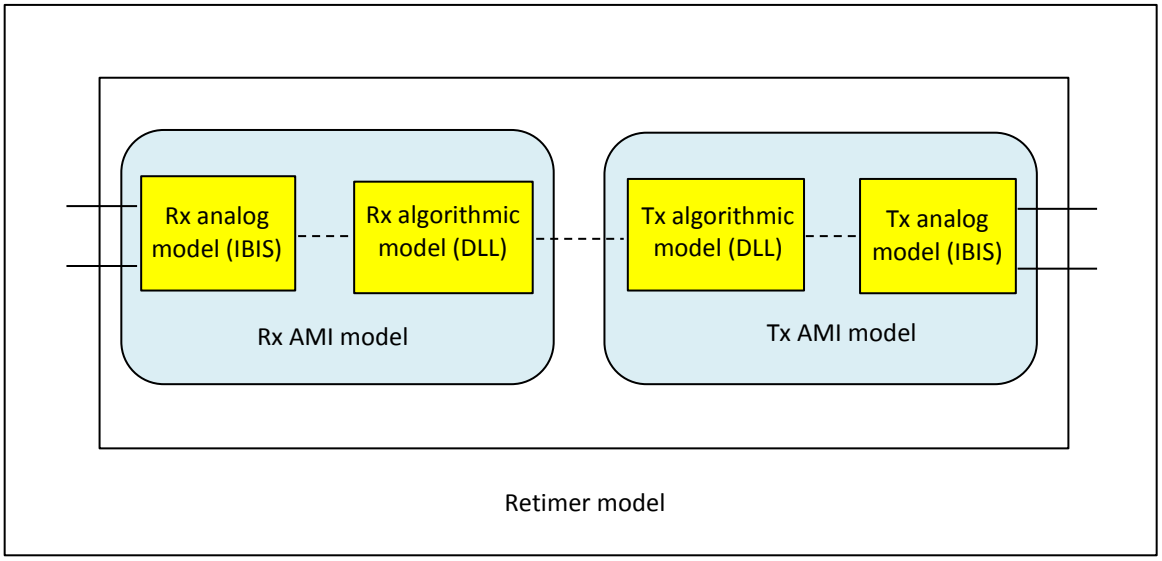

Figure 1. Retimer AMI model

The retimer simulation flow is shown in Figure 2. The SerDes Tx is connected to the retimer by the upstream channel, and the retimer is connected to the SerDes Rx by the downstream channel. The SerDes Tx analog model, the upstream physical channel and the retimer Rx analog model are assumed to the linear and time-invariant. They are represented by a combined impulse response, h_{AC1}. The retimer Tx analog model, the downstream physical channel and the SerDes Rx analog model are also assumed to be LTI. They are represented by another combined impulse response, h_{AC2}. During the simulation, SerDes Tx algorithmic model's output, v_{SerDes}^{out}, is convolved with h_{AC1} to produce the input signal, v_{Rx}^{in}, to retimer Rx's AMI_GetWave function. The function returns signal v_{Rx}^{out} and clock times. The simulator samples v_{Rx}^{out} at half unit interval (UI) after each clock time and generates the square waveform of the digital stimulus, v_{Tx}^{in}, which is passed into the retimer Tx algorithmic model. The retimer Tx model's output, v_{Tx}^{out}, is convolved with h_{AC2}. The resulting signal, v_{SerDes}^{in}, is the input to the SerDes Rx algorithmic model. Note that transitions in the digital stimulus take place at exactly the clock times generated by the CDR in retimer Rx's AMI_GetWave function. Therefore, upstream channel jitters tracked by the retimer CDR are passed down to the downstream channel. Jitters not tracked by the CDR are rejected.

Since retimers are modeled within the AMI framework, the proposed approach provides interoperability between SerDes and retimer models from different IC vendors without comprising their IP. Moreover, the method maintains the AMI simulation efficiency by treating upstream and downstream channels with convolutions. The approach can be applied to cascaded retimers. Channels with mixtures of retimer and redriver can also be simulated by the combination of this flow and the one described in [2] for redriver.

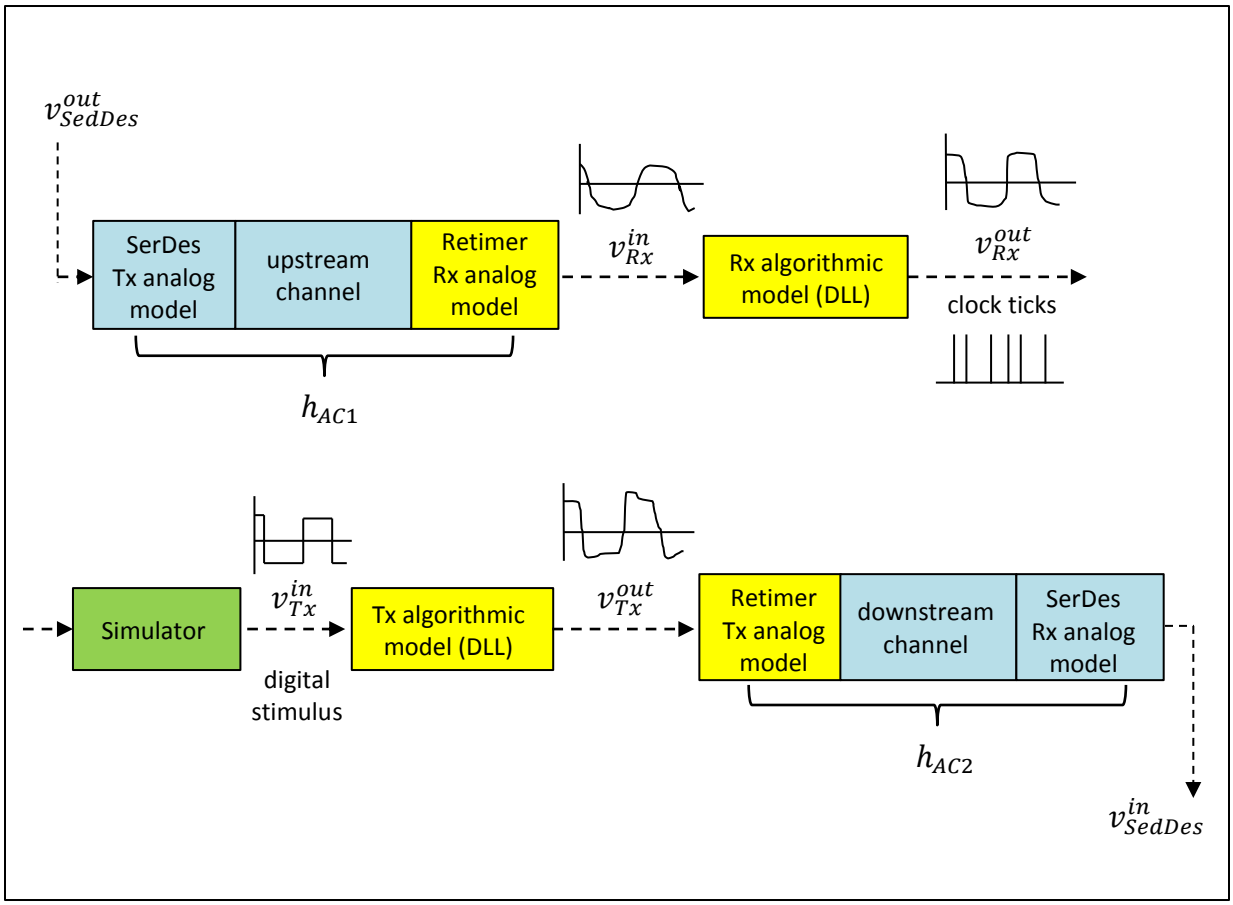

Figure 2. Retimer AMI simulation flow

2. Retimer and Retimer IBIS-AMI model

Retimer and redriver have the same function to serve as a mid-channel repeater to provide additional equalization capability for high-speed transceiver system that has insufficient strength to recover data from the high loss and high reflection transmission medium. Retimer differentiates from redriver by having a CDR, and the presence of CDR in the retimer enables the option of including advanced equalization component at ease such as FFE, and DFE. In this section, both redriver and retimer topologies will be presented and their differences will be briefly described. The detail IBIS-AMI modeling implementation of a retimer will be discussed and a method to use the retimer IBIS-AMI model to verify its jitter transfer capability is presented.

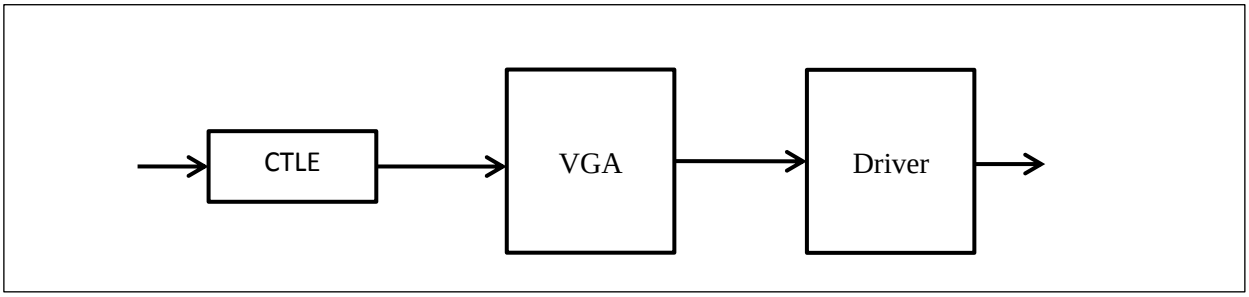

Figure 3. A common redriver's block diagram

Redriver has relatively simple architecture that generally consists of merely a continuous time linear equalizer (CTLE) to compensate the high-frequency signal loss, an optional variable gain amplifier (VGA) to amplify signal magnitude, and a driver to retransmit the data as depicted in Figure 3. An optional de-emphasis scheme may present in the driver to shift the energy from low frequency signal to high frequency signal. All non-linear impairments such as jitters besides the CTLE compensated deterministic jitter, reflection, and the slew-rate of the signal can propagate from the input to the output of the redriver. Hence, redriver performs optimally well as the mid-channel signal conditioner to compensate a system that needs additional linear compensation from the CTLE. Redriver topology and its modeling methodology had been presented in [2].

In contrast, retimer has more complex architecture than redriver. In addition to a CTLE that linearly compensate the high-frequency signal loss and an optional VGA that amplifies the signal, it also consists of a CDR block to recover the clock from the input data. The recovered clock then triggers a slicer to digitize the optimally equalized signal as depicted in Figure 4. Retimer may also include an optional feed-forward equalizer (FFE) and decision feedback equalizer (DFE) to compensate reflection and data dependent inter-symbol interference (ISI). A variation of the CDR feedback scheme have been observed in which the CDR is trained either by the output of the VGA (V_{vga}^{out}) or the output of DFE (V_{DFE}^{out}) to recover the clock from the

equalized data. One of the feedback schemes are usually carefully selected by the designer to enhance the CDR adaptation algorithm as depicted in Figure 5. On the output end, a retimer consists of a driver with optional clock-triggered de-emphasis to retransmit the retimed digital signal.

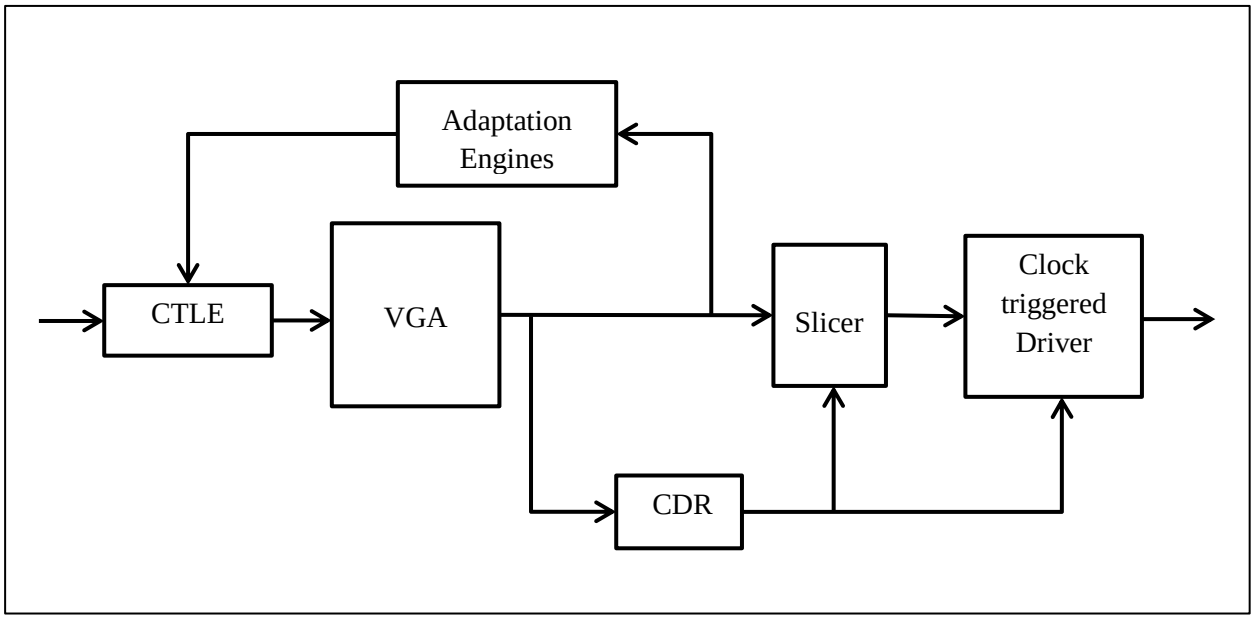

Figure 4. A Simple Retimer Topology

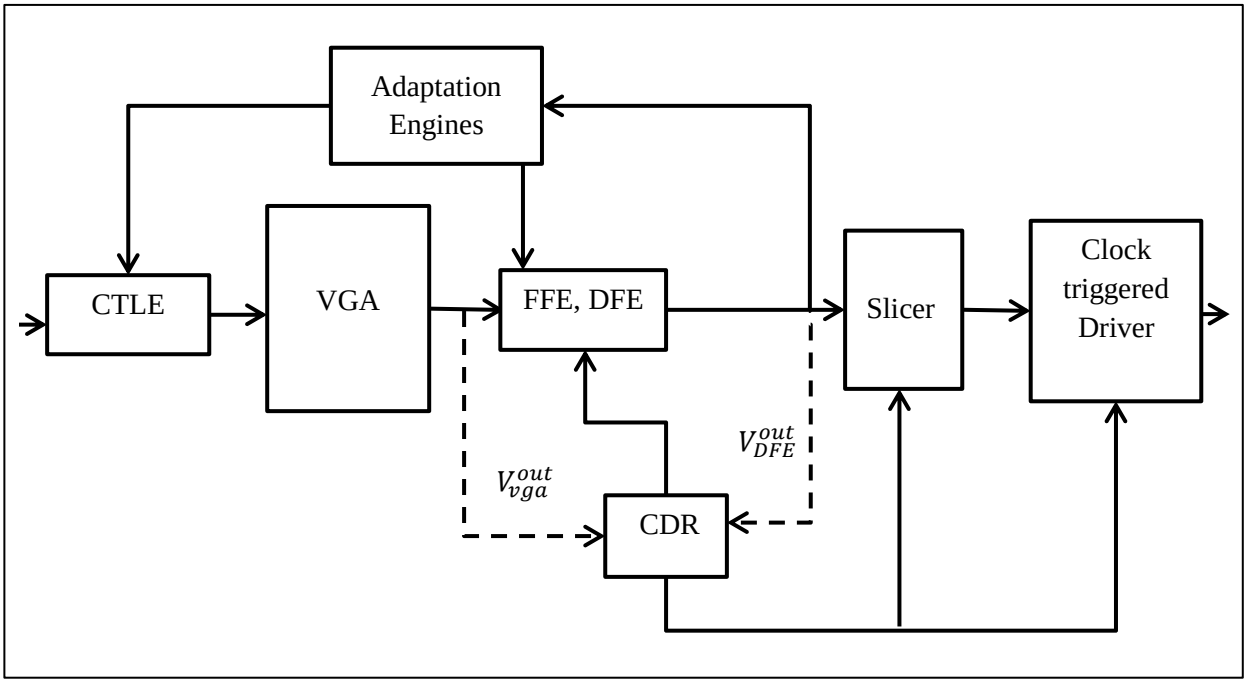

Figure 5. A Retimer with DFE and CDR trained by CTLE or VGA equalized signal

In general it is more costly in resources to design a retimer than a redriver due to the complexity of the CDR, the DFE, and their self-adaptation algorithms. Despite the additional effort and cost in designing the retimer, it is undeniable that the CDR's capability to reset jitter from the up-stream signal is an extremely attractive feature for a system that has noisy signal source as a result of the inherent VCO jitter of the reference clock. In addition, the DFE in the retimer can handle higher reflection and data-dependent ISI than a redriver by dynamically adjusting its compensation based on the history of data pattern to reduce the reflection caused by the up-stream signal path and uncompensated Inter-Symbol Interference.

IBIS-AMI standard only specifies one output pin and one clock pin for retimer's receiver. In a system in which a retimer has marginal performance, it is crucial for the system designer of the retimer to identify the underperforming component of the retimer. The underperformance component could be the insufficient equalization of CTLE and DFE, error propagation of DFE, false adaptation that causes over or under equalization. To provide the probing capability for each of the components, a multiplex is added to the receiver AMI model to mux the output from the CTLE, VGA, DFE, and Slicer to the receiver output pin as depicted in Figure 6. This enables the circuit designer to correlate the performance at the specific internal nodes and also provides system designer a way to identify the underperforming component of a failing system. On top of that, it allows simulating the retimer model as redriver by selecting the output of the VGA as the output of the redriver Rx model. It is particular beneficial in figuring out the additional performance gain of using a retimer over a redriver.

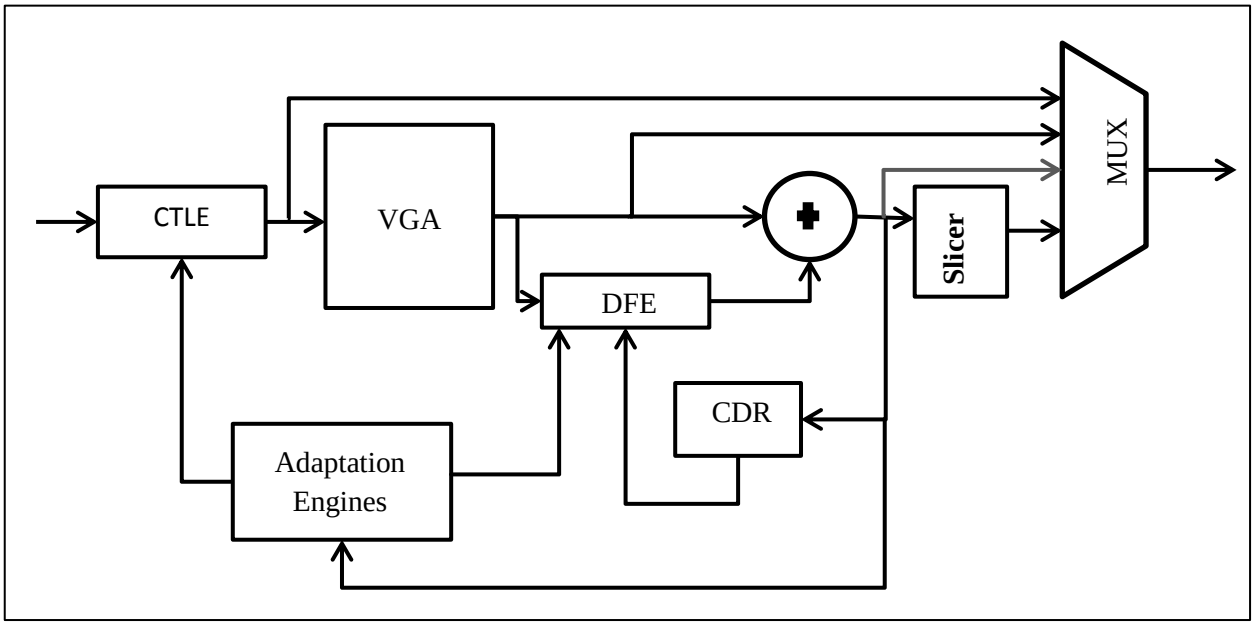

Figure 6. Block diagram of an IBIS-AMI retimer's receiver implementation with in-build probing capability

3. Method in Analyzing Retimer Jitter Transfer Characteristic by Using IBIS-AMI model

Jitter transfer function of a retimer behaves like a low pass filter as the retimer tracks the low frequency jitter and filters out high frequency jitter. When jitter presences in a high-speed serial IO system, the CDR tracks those jitters whose frequencies are lower than the loop bandwidth of the CDR and filters out the jitter whose frequency is higher than the CDR loop bandwidth. This causes the distribution of the recovered sampling clock following the distribution of low frequency jitter. The recovered clock is then used to re-time the input digital data to the transmitter, which inevitably propagates the jitter from the recovered sampling clock to the re-transmitted data. Hence, the output jitter of a retimer tracks the low frequency of the input jitter.

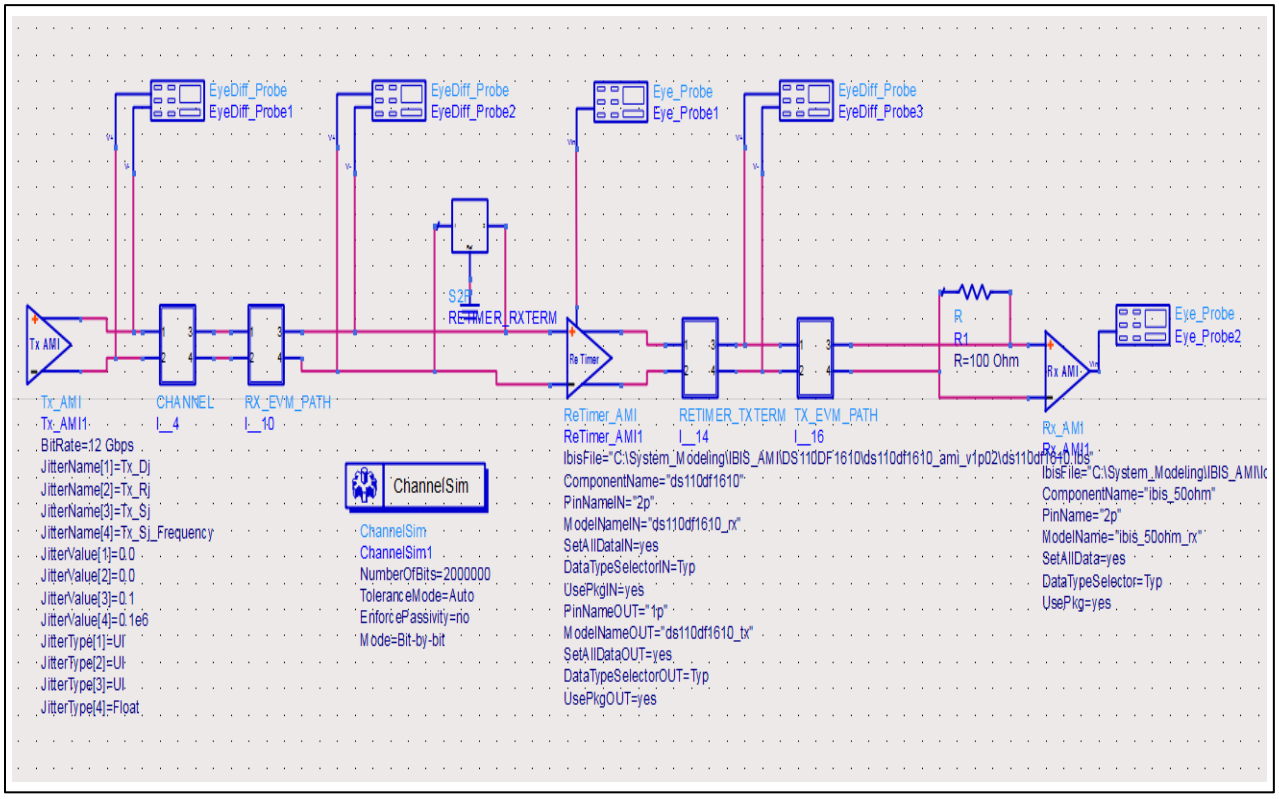

Figure 7. Simulation setup for jitter transfer analysis

Figure 7 depicts the setup of simulations that illustrate the retimer jitter transfer characteristic. An ideal IBIS-AMI transmitter model is used as the transmitter. The driver bandwidth of the signal generator and the characteristic of the 2-inch SMA differential cable are lumped into the CHANNEL block. PCB board traces, input and output package models of the retimer are represented by RX_EVM_PATH and TX_EVMPATH blocks respectively. Retimer input and output terminations are modeled by the RETIMER_RXTERM and RETIMER_TXTERM respectively.

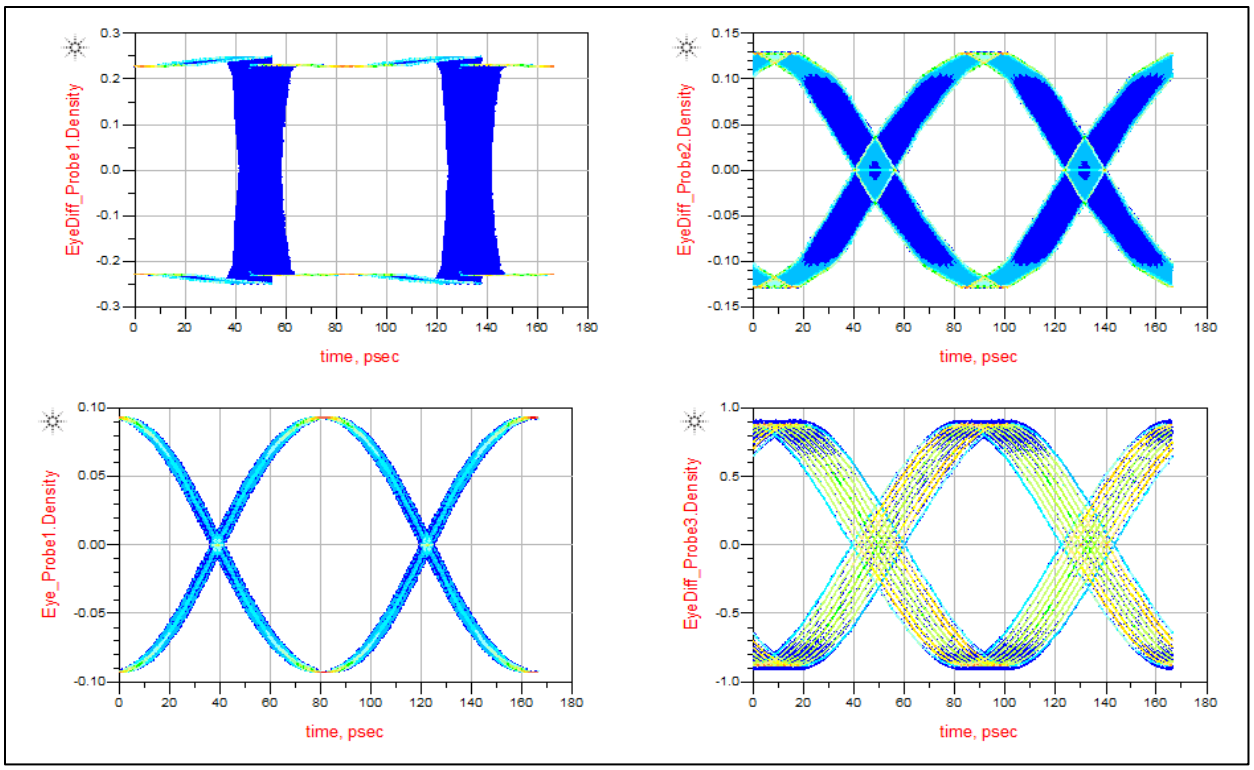

Figure 8. Simulation results with SJ magnitude = 0.1 UI and SJ frequency = 100kHz

To illustrate that the retimer tracks the low frequency jitter, sinusoidal jitter (SJ) is injected into the clock pattern from the transmitter by using the built-in SJ function from the IBIS-AMI standard compliant EDA tool. The magnitude of the SJ is set to 0.1 unit interval (UI) and the frequency is set to 100kHz. The top left eye-diagram of Figure 8 depicts the ideal clock signal from ideal transmitter with the additional SJ injected, and the top right eye-diagram of Figure 8 depicts the signal density and jitter distribution shaped by the signal path before feeding into the retimer. The bottom left eye-diagram of Figure 8 depicts the signal density and jitter distribution at the VGA of the retimer's receiver with minimum VGA gain applied. This equalized signal is further optimized by the DFE before it is digitized by the slicer that is triggered by the recovered clock from the CDR. Since the injected SJ frequency is lower than the CDR loop-bandwidth, the CDR tracks almost all the jitter components. Therefore, the jitter distribution is relatively small as seen by the retimer's receiver as the result of the CDR's capability to track the slow-frequency jitter by adjusting its phase interpolator to put the data slicer always close to the center of the eye as depicted in the eye-diagram. The bottom right eye-diagram of Figure 8 depicts the signal and jitter density at the output of the retimer transmitter, whose digitized input data is re-timed by using recovered clock from CDR. As the result of retimer CDR fully tracking the low frequency jitter, this output signal has similar jitter distribution as the SJ distribution at the retimer input (top-right eye in Figure 8) despite the signal edge has been shaped by the transmitter bandwidth, and jitter is passed by the retimer from the upstream channel to the downstream channel.

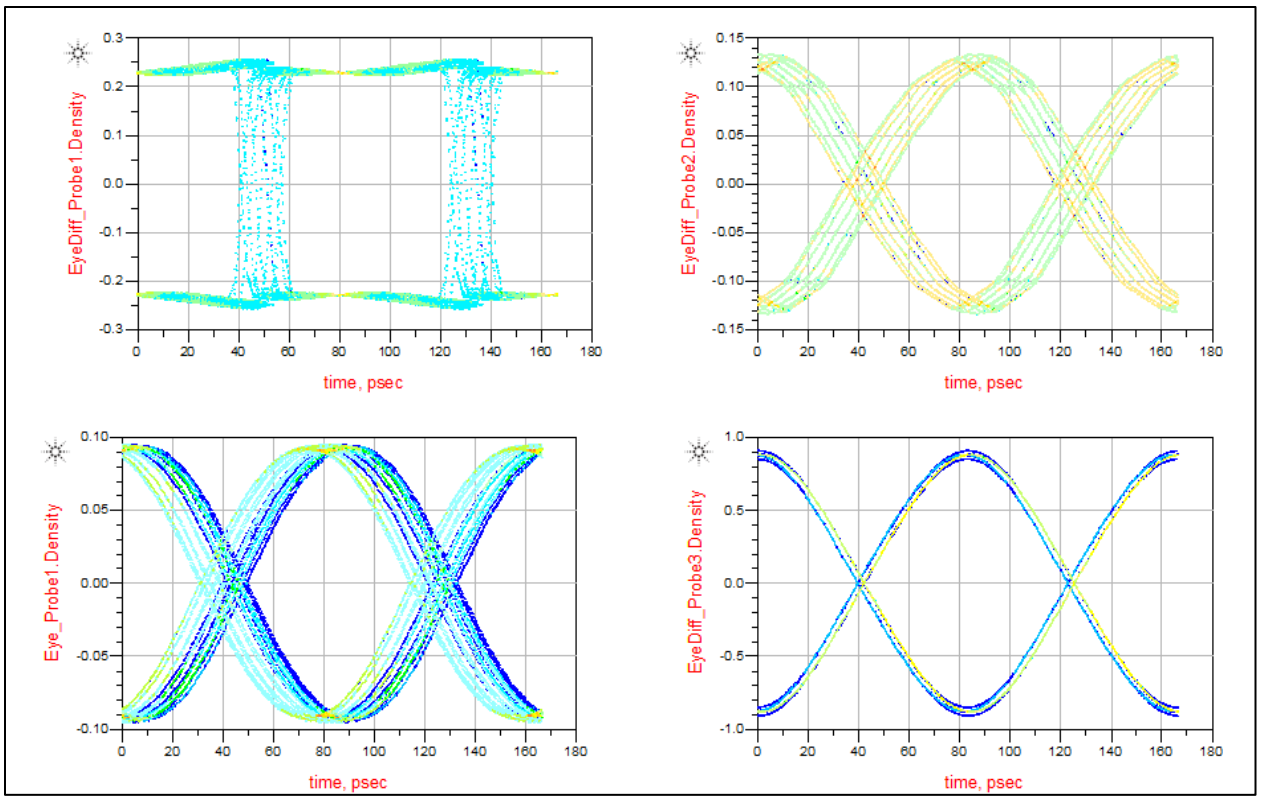

Figure 9. Simulation results with SJ magnitude = 0.1 UI and SJ frequency = 500 MHz

Figure 9 depicts the simulation results with SJ magnitude set to 0.1UI and SJ frequency set to 500MHz. Similarly, the top left and top right eye-diagram of Figure 9 shows the data density and the jitter distribution of the ideal transmitter output and the retimer input signals, respectively. The bottom left eye-diagram of Figure 9 depicts the signal density and jitter distribution at the VGA of the retimer's receiver with minimum VGA gain applied. Since the jitter frequency of the input signal is much higher than the CDR loop-bandwidth, the CDR does not have enough information to modulate its phase interpolator to track the high-frequency jitter. Instead, it keeps its phase interpolator to lock at the center of the peak to peak jitter range. Because of the almost stagnant CDR, the retimer's receiver observes all the jitter, as shown in Figure 9. On the other hand, due to the same fact that the phase interpolator locks at the center of the jitter range, the clock generated by the CDR has relatively small jitter compare to the jitter from the input signal. This recovered clock is then used to trigger the transmitter, whose output signal, depicted in the bottom right eye-diagram of Figure 9, consequently contains smaller jitter than the retimer's input (the top right eye of Figure 9). As a result, high frequency input jitter is filtered by the retimer and does not propagate to the downstream channel. The retimer jitter transfer function can be measured from the distribution of the retimer output jitter, which closely resembles jitter hunted by the CDR.

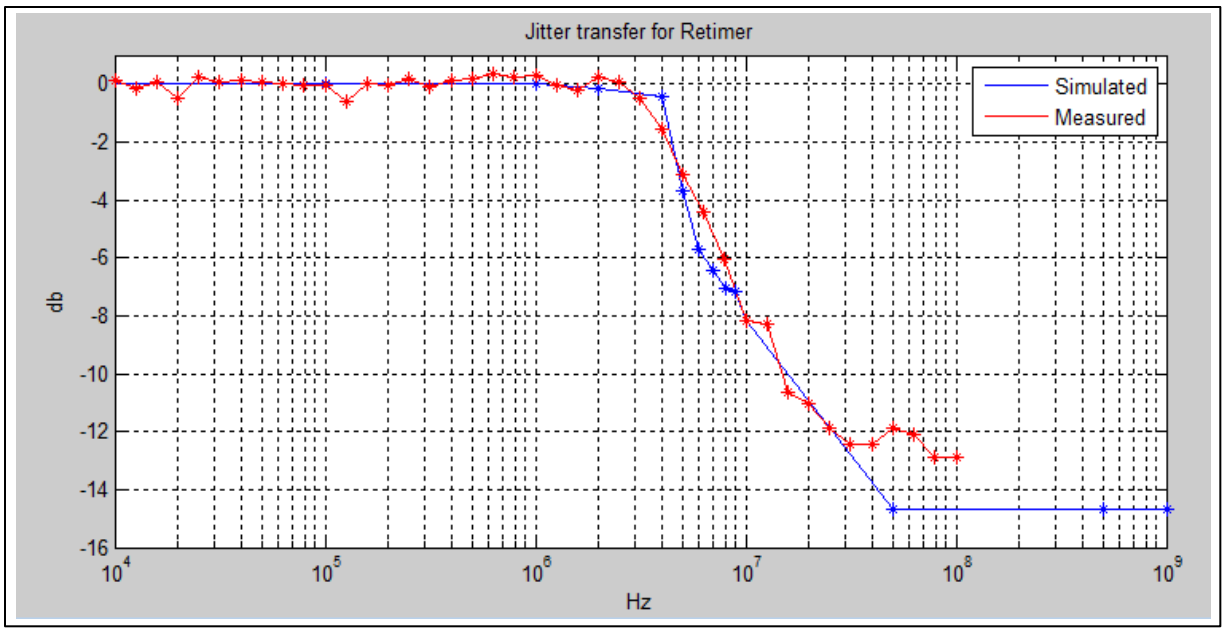

Figure 10. Jitter transfer for a retimer behaves like a low-pass filter

Figure 10 depicts jitter transfer curves obtained from simulations and lab measurements by sweeping the SJ frequency. The simulated jitter transfer curve using the retimer AMI model and the measured jitter transfer curve of the retimer device correlate well within 2db mismatch beyond 40Mhz. The mismatch could be resulted from underestimating the inherent jitter from the VCO in the model, and the relatively high instrument noise floor.

4. System Level Analysis of High-Speed Interface System with Retimer

In high speed serial links, SerDes ICs play crucial role, as they have to adapt to the given channel and recover the bits satisfactorily within the bit error rate limits as specified in the serial standards. They also have to support the standard specific equalization requirements. For example, PCIe 3.0 transmitter needs to have 11 different De-emphasis/pre-shoot presets. Usually transmitter chip is simpler, incorporates FFE (Feed forward equalizer) only, while the receiver employs a number of advanced adaptation loops to coordinate between VGA, CTLE and DFE apart from CDR. VGA is an all-pass filter boosting small input signals. CTLE provides additional gain at high frequency bands to mitigate the effects of low pass transmission media. A 10-tap DFE is used to cancel inter-symbol interference (ISI) and other channel impairments. Adaptation is performed using the Group delay or LMS algorithms. Typically IBIS AMI models of SerDes transmitter ICs support both time domain and statistical modes, while the receiver support only time-domain (bit-by-bit) mode, since it contain nonlinear elements – CDR and/or adaptive state machines which are not conducive to LTI modeling. For correlation with the actual link performance, IBIS AMI models shall include the effects of Process, Voltage and Temperature (PVT) corners on the equalization behavior. During link simulation setup, the seed values of equalizer taps, PVT corner selection and slew rate settings are exposed to the user. Correlation has been performed on the IBIS AMI models of SerDes chips with the lab measurements at all the equalizer tap settings. Lab data are de-embedded of the DUT interface board traces so that the output waveforms are closest to the chip package pins. In this paper, LSI SAS3 12Gbps SerDes is used as the transmitter and receiver of the serial link.

4.1 Performance limit of passive channel serial links

Channel loss and crosstalk have critical impacts on high speed serial link performance. The former is measured by the insertion loss at the fundamental or Nyquist frequency of data rate. The latter is characterized by the insertion to crosstalk ratio (ICR), which is the difference between insertion and crosstalk at the receiver, akin to signal to noise ratio. Traditional serial links employing passive channel, transmitter equalization and multi-tap DFE receiver are found to work when the channel's electrical characteristics satisfies twin conditions -- Insertion loss at the Nyquist is less than 30dB, and ICR is more than 15dB.The following link simulation setup verifies such limits. The test channel, illustrated in Fig. 11, has 29.5dB differential loss and 34dB of insertion to far-end crosstalk (FEXT) ratio. Near end crosstalk (NEXT) is not considered in the link simulation.

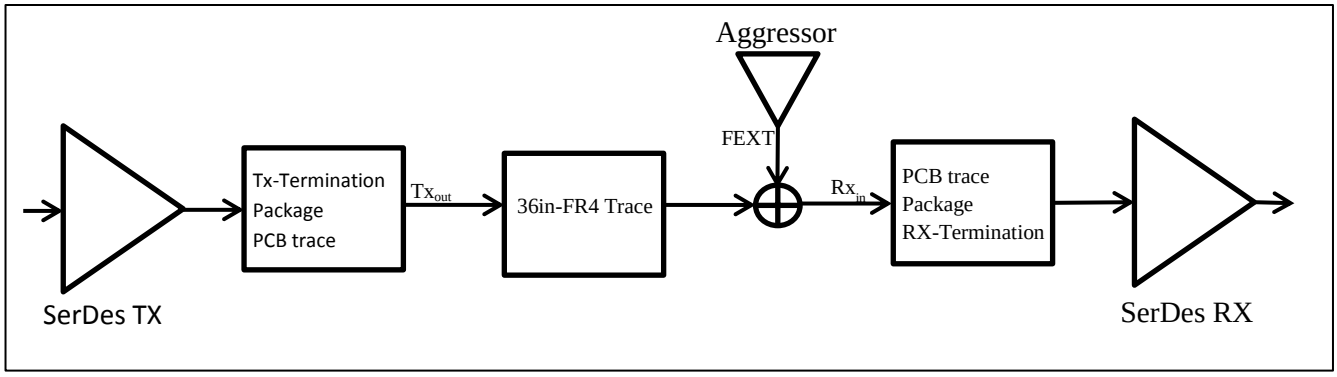

Figure 11. Simulation setup for 12Gbps link with passive channel. FEXT is present in the system.

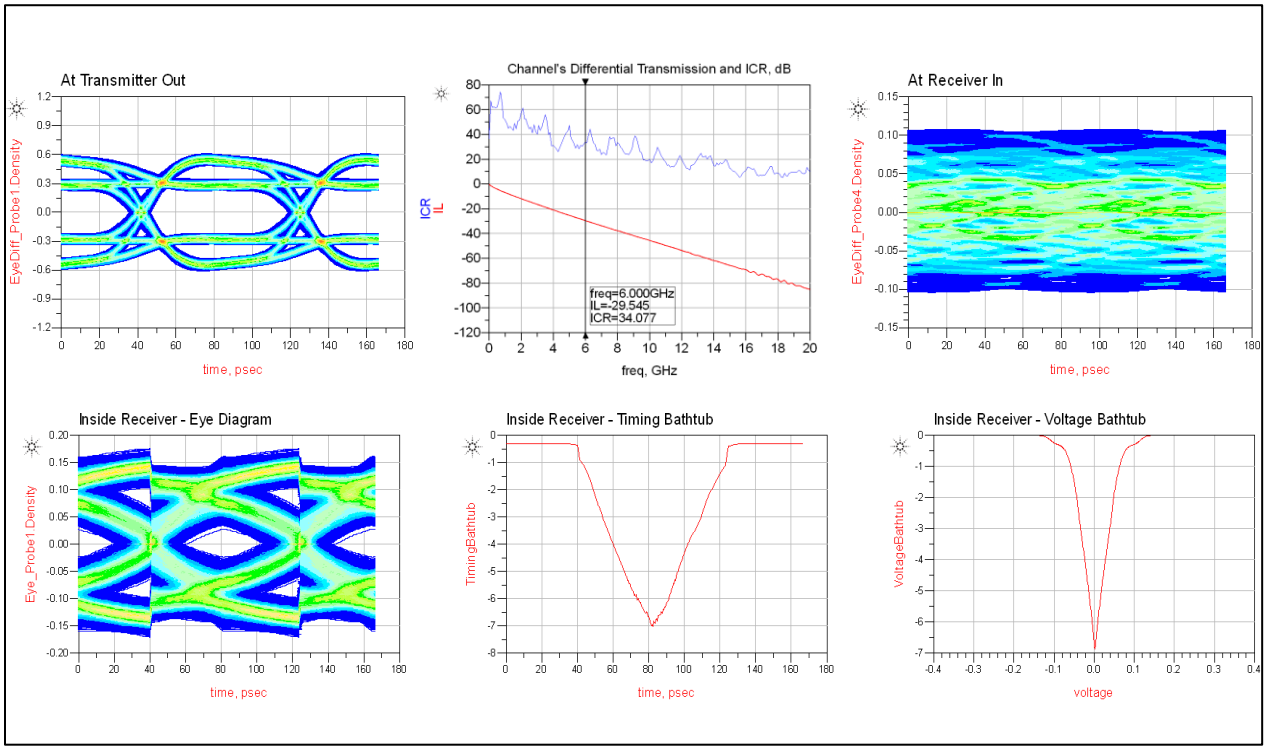

Figure 12. Simulation results of 12Gbps link with passive channel. FEXT is present in the system.

Simulated eye diagrams and bathtub curves of the test channel at 12Gbps are shown in Fig. 12. The bathtub curves indicate that the system can only work till BER 10^{-7}. To extend the BER performance to the required value of 10^{-12}, highly complex receiver with advanced equalization techniques such as Partial Response and Noise Predictive Maximum Likelihood (PRML/NPML) Equalization and Detection with Viterbi decoder [3] and forward error correction (FEC) coding is needed. Alternatively, retimer can be employed in the middle of a channel to not only meet but exceed the BER requirement, as shown in the following discussion.

4.2 Evaluation of Retimer based active Serial links

We evaluated retimer based 12Gbps active serial link, illustrated in Fig. 13, in the presence of crosstalk in a lossy channel with loss characteristics similar to that of a typical 10m MiniSAS HD cable. The channel is a SAS3.0 compliance board manufactured by LSI, and its characteristics are shown in Fig.14. In this case study, we used two of such channels with retimer in between.

Texas Instruments DS125DF1610 is a sixteen-channel multi-rate retimer with an input Continuous Time Linear Equalizer, Variable Gain Amplifier, Decision Feedback Equalizer, clock and data recovery, and an output driver with FIR filter equalization. The DS125DF1610 can enhance the reach and robustness of long, lossy, crosstalk impaired high speed serial links to achieve BER < 1×10^{-15}. Programmable transmit FIR filter offers control of the pre-cursor, main tap and post-cursor. The fully adaptive receive equalization (CTLE, VGA and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high speed serial data. A non-disruptive mission mode eye-monitor feature allows link monitoring internal to the receiver. The built-in PRBS generator and checker compliment the internal diagnostic features to complete standalone BERT measurements.

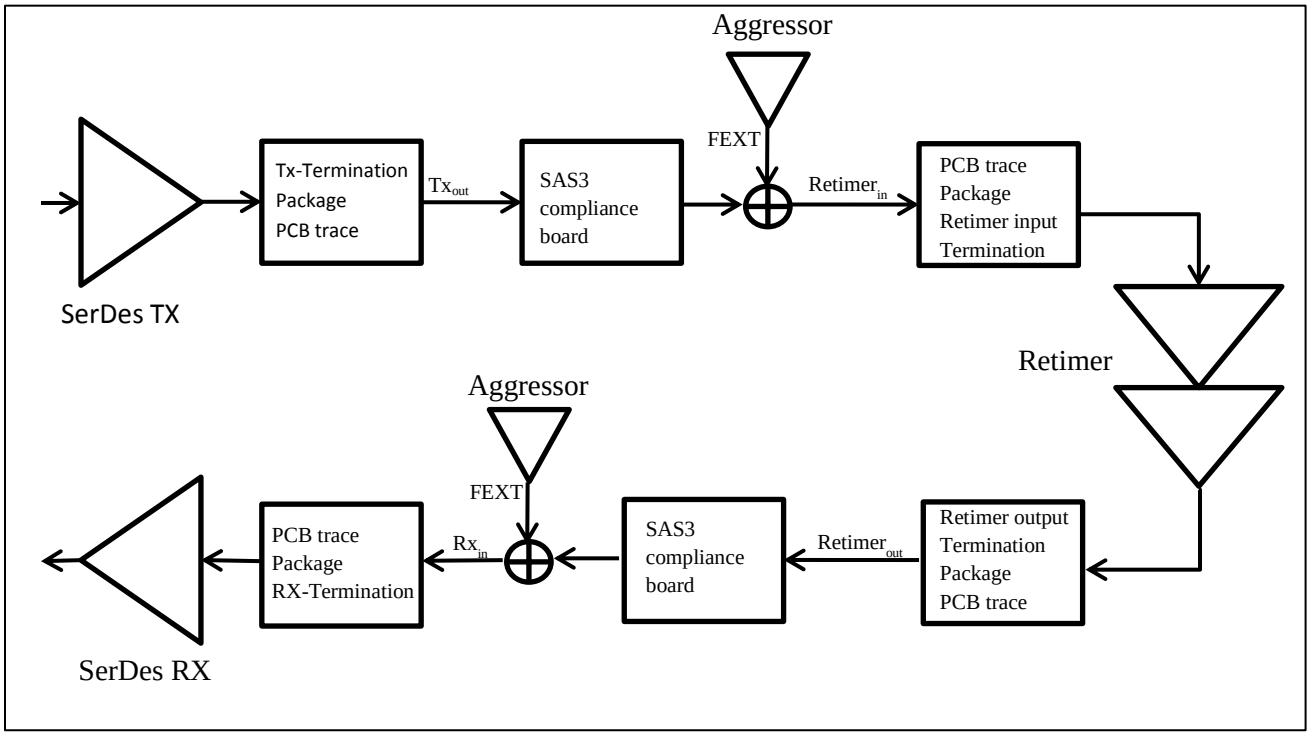

Figure 13. Simulation and Measurement Setup for 12Gbps link with retimer. FEXT is present in the system.

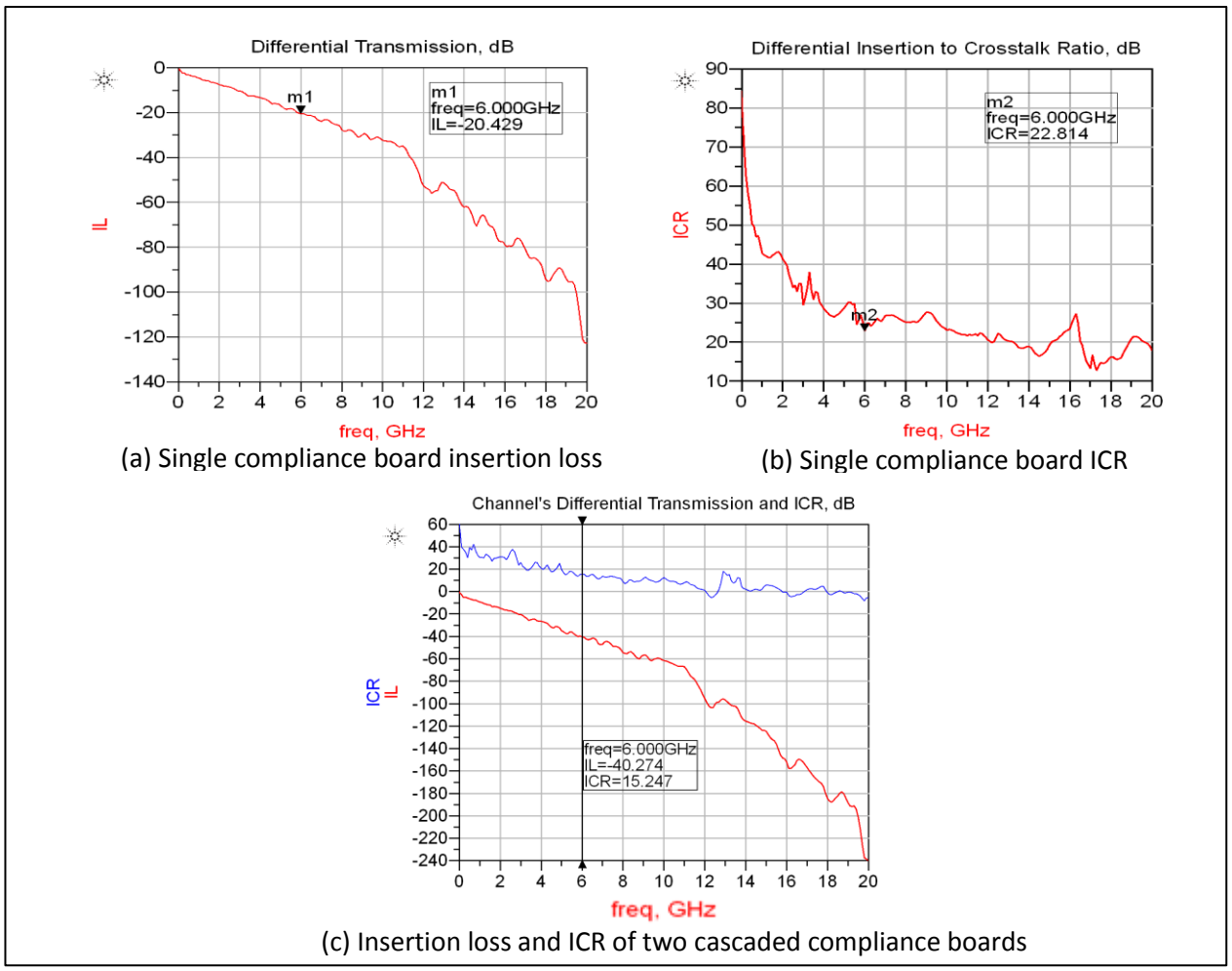

Figure 14. SAS compliance board – Insertion loss and ICR

Figure 13 depicts setup for the full link measurement that includes a SerDes transmitter and SerDes receiver and retimer. The up-stream link has total 20dB loss contributed by the 20 in FR4 trace, transmitter and retimer input packages, and the EVM board trace. The down-stream link has total 20dB loss contributed by the 20 in FR4 trace, retimer output and receiver packages, and the EVM board trace. For the crosstalk, only far-end crosstalk (FEXT) at the receiver is considered. The induced FEXT is asynchronous and at the same data rate as the SerDes i.e. 12Gbps. The FEXT is found to be -43dB at the Nyquist, leading to an ICR of 23dB. The differential insertion loss and the insertion-to-crosstalk ratio of a single compliance board are shown in Figure 14(a) and Figure 14(b), respectively. Figure 14(c) shows the combined response of the two cascaded compliance boards. We observe that with doubling the channel length, the total insertion loss scales proportionally from 20dB to 40dB, while the FEXT is reduced to -55dB, resulting in a total ICR of 15dB.

Simulated eye diagrams and bathtub curves are shown in Figure 15. The SerDes transmitter dispatches PRBS7 pattern at 12Gbps and its de-emphasis setting is swept to optimize the eye-height and eye-width of the output of the retimer. Figure 15(b) shows that the eye at the retimer input is completely close due to the loss and reflection from the upstream channel and interconnects. The input signal to the retimer further degraded by the front-end parasitic impairment before it is compensated by the CTLE, VGA, and DFE. The optimally compensated signal is then re-transmitted by the driver that is timed by the recovered clock. The output signal of the retimer is shown in Figure 15(c).

The optimally compensated signal is then attenuated by the down-stream signal path along the 20in FR4 trace. Due to the relatively high loss from this signal path, the eye is completely close again at the input of the receiver as depicted in Figure 15(d). The signal is restored by the receiver equalizations as demonstrated in Figure 15(e) by the receiver internal eye captured at the receiver slicer. From the receiver bathtub curves in Figure 15(f) and Figure 15(g), we can see that the active serial link under study with the total insertion loss of 40dB and ICR of 15dB works till BER of 10^{-16}, passing the SAS3 specification. In contrast, a passive link with 30dB insertion loss and ICR of 34dB only works till BER of 10^{-7}, as shown in the Figure 12. Figure 15 demonstrates that retimer increases system tolerances to channel loss and ICR by at least 10dB and 19dB, respectively. Note that in the actual scenario the results will improve further with the back channel adaption and link training turned on.

Figure 16 shows correlation between simualtion and measurement at various points in the link, including transimitter output, retimer input, retimer output and receiver input. Eye diagrams and BER contours inside the receiver are plotted in Figure 17, where the measured results are captured by the EyeScope functionality of LSI SerDes. Figure 17 shows that at 10^{-12} BER, the simulated eye height is 72mV, in good agreement with the measured value of 70mV. The eye width is 15ps in simulation and about 25ps in measurement. The two values are reasonably consistent to each other, and the discrepancy is possibly due to different extrapolation methods at extremely low BER employed by the simulator and the EyeScope. Results in Figure 16 and Figure 17 show that AMI models accurately represent the behaviors of the SerDes and retimer devices.

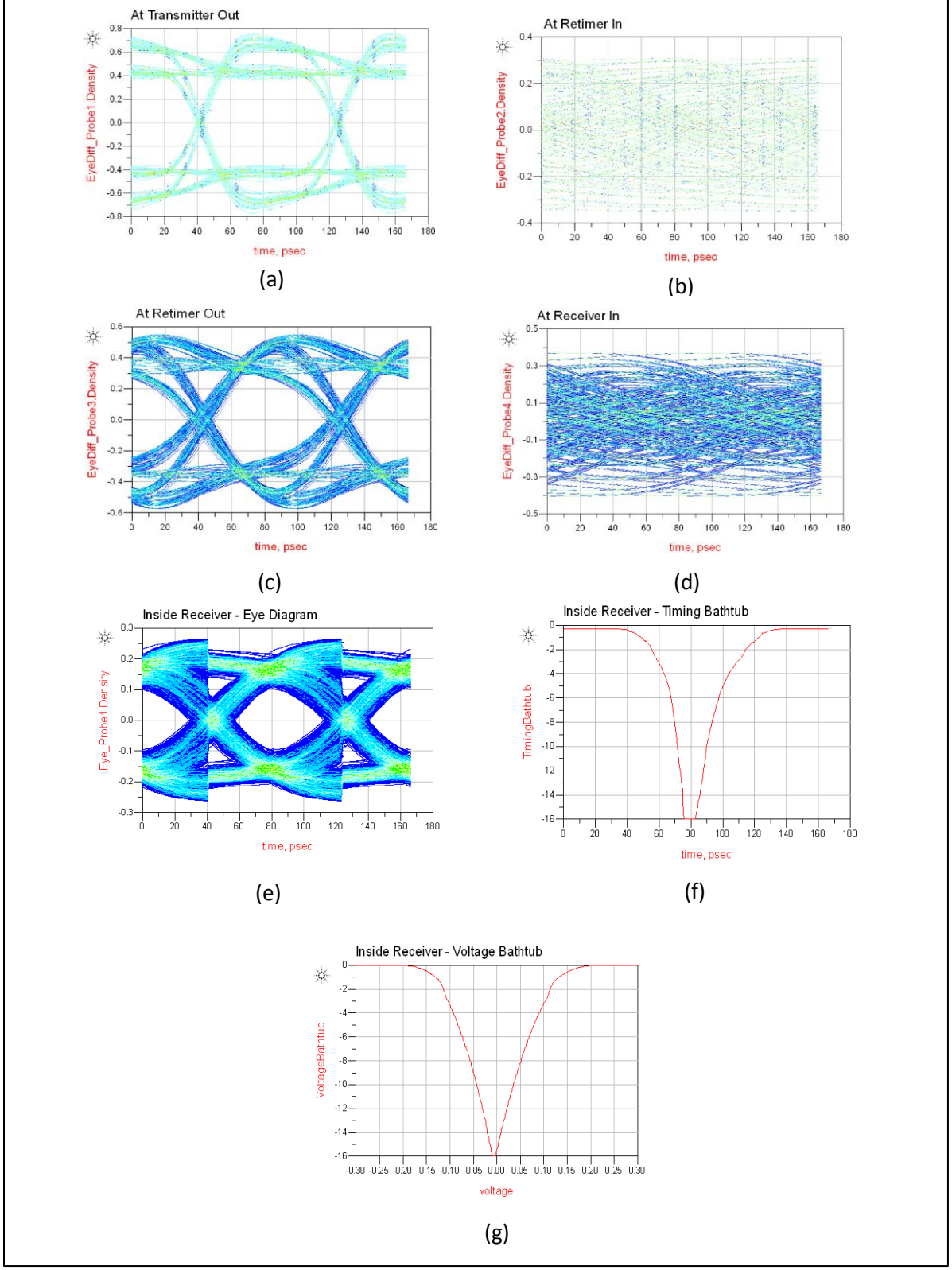

Figure 15. Simulation results of 12Gbps link with retimer. FEXT is present in the system.

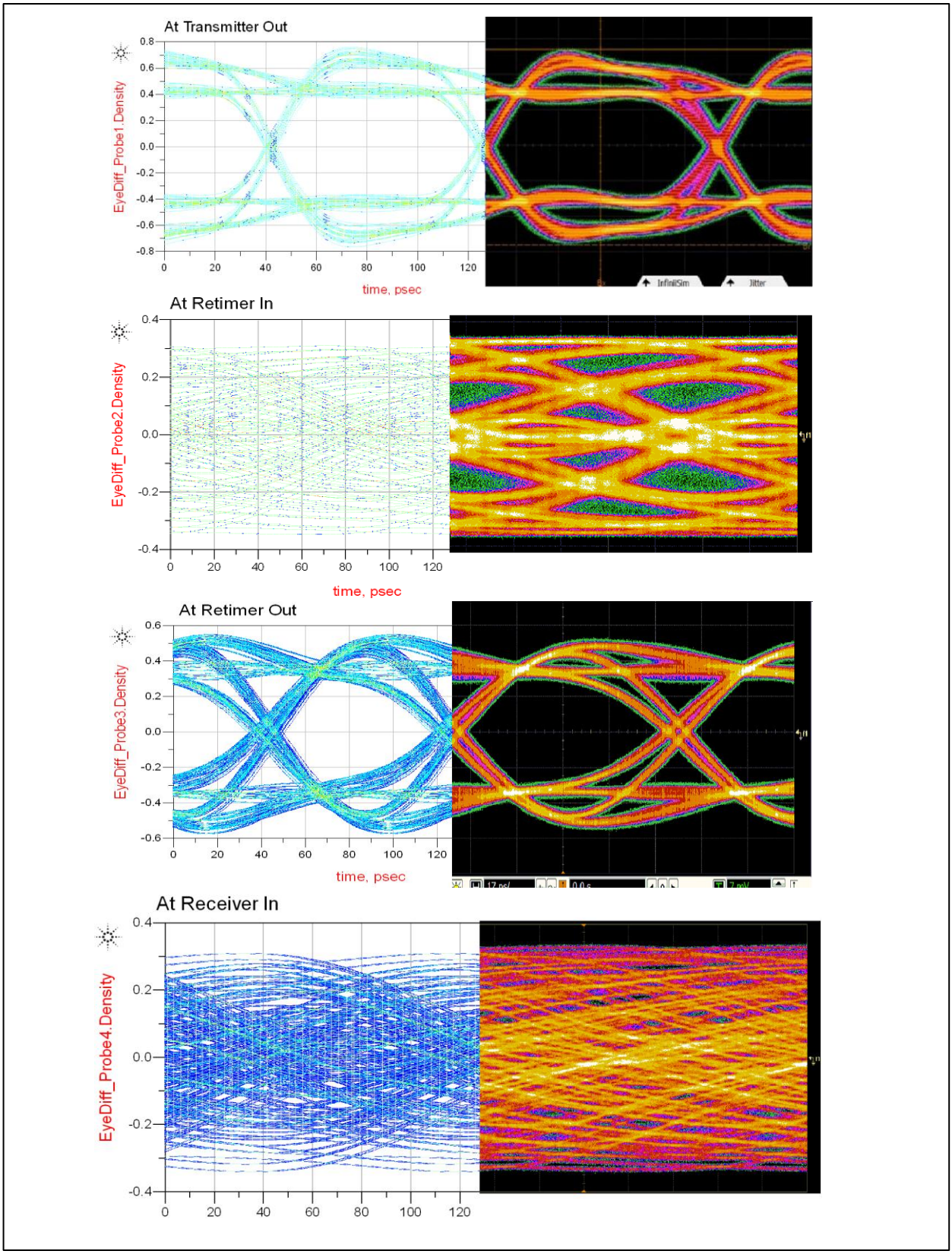

Figure 16. Correlation between simualtion and measurement at different points in the link

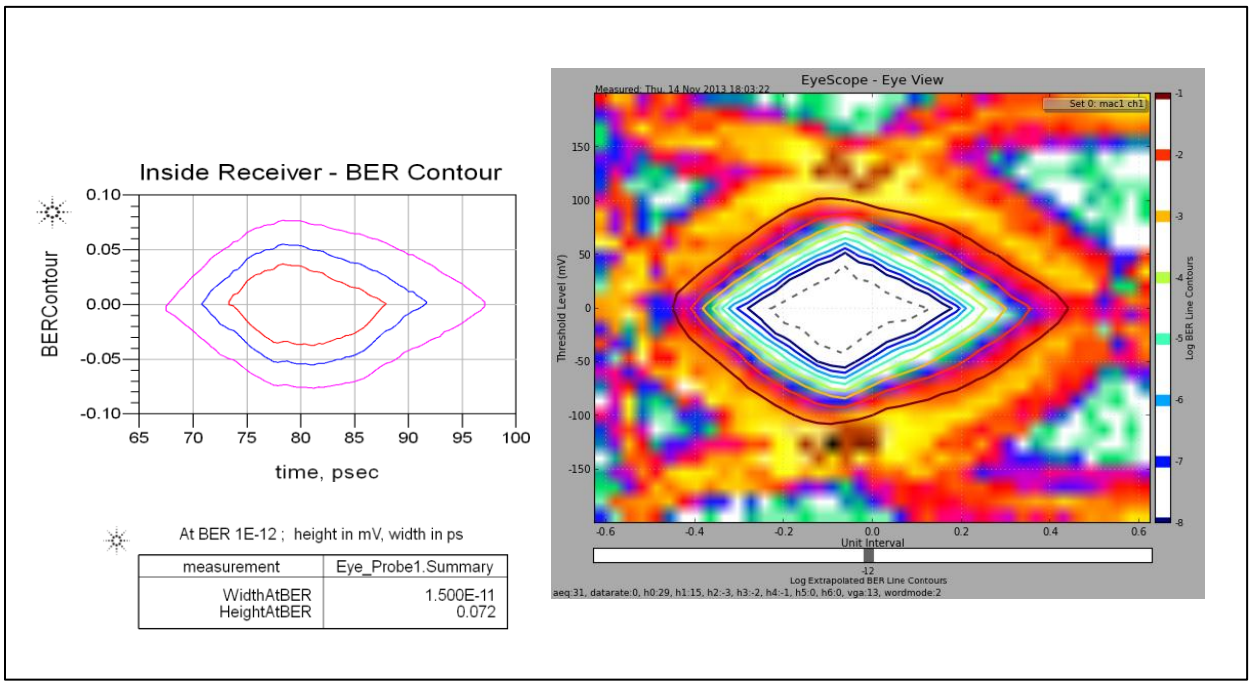

Figure 17. Simulation and measurement correlation results of 12Gbps link with retimer. The measured eye diagram and BER contours inside the receiver are captured by the EyeScope in the SerDes receiver. Simulated contours are at BER values of 10^{-12}, 10^{-9} and 10^{-6}. Simulated WidthAtBER and HeightAtBER are measured at BER=10^{-12} and in units of ps and volt, respectively. The inner-most contour in the measured eye is at BER=10^{-12}.

5. Conclusion

Active channel with retimer is a more cost and resource effective solution to overcome loss in high-speed links compared to other approaches that employ advanced equalization technique such as Forward-Error-Control (FEC) algorithm, high level Pulse Amplitude Modulation technique such as PAM-4 or PAM-8, and expensive low-loss dielectric material. In this paper, we described a methodology in developing IBIS-AMI models for retimers that directly utilizes the retimer CDR output. The method is compliant to the IBIS-AMI 5.2 Standard and offers interoperability between retimer and SerDes models, which enables end-to-end system simulations. We showed that the IBIS-AMI retimer model results correlate well to the silicon measurement results. A full link analysis demonstrated that retimer enhances system tolerances to both channel loss and crosstalk. In addition, retimer's capability to reset the jitter from the up-stream channel and thus reduce the jitter passed to the down-stream channel was found to improve performance of systems that suffer from high frequency jitter source. The modeling and simulation methodology discussed in this paper provides an efficient yet reliable way for system designer to evaluate and fine-tune the insertion-loss, return-loss, and cross-talk of the pre-manufactured transmission medium to ensure first pass success in high-speed active link designs.

References

1. IBIS Specification 5.2

2. Madbubul Bari, Ron Olisar, Hassan Rafat, Fangyi Rao, Sharon Wang, Ming Yan, "End to end Link Analysis and Optimization with Mid-channel redrivers AMI Models", DesignCon2013

3. Pervez Aziz, Cathy Liu, Adam Healey, "Partial Response and Noise Predictive Maximum Likelihood (PRML/NPML) Equalization and Detection for High Speed Serial Link Systems", DesignCon2013

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