# Selecting Best Device for Power Circuit Design Through Gate Charge Characterization

White Paper

Hisao Kakitani and Ryo Takeda – Agilent Technologies International, Japan Ltd.
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## Market and technology trends in power electronics

The improved performance of recent power devices is enabling higher frequency and more compact switching power supply designs. Emerging new devices such as super junction MOSFET or GaN FET are soon expected to replace the traditional devices such as silicon MOSFET or IGBT. Switching power supplies operating in higher frequency from a few hundred kHz to more than 1 MHz have been developed and are available using these innovative power devices.

High frequency operation reduces the cost of power circuits by shrinking the magnetic component size. This, in turn, results in smaller and lighter circuit designs. However, high frequency switching increases the power device loss. The main power loss in a switching power supply is the loss associated with the power semiconductor devices. Therefore, selecting the optimum low power devices is essential when designing power electronic circuits.

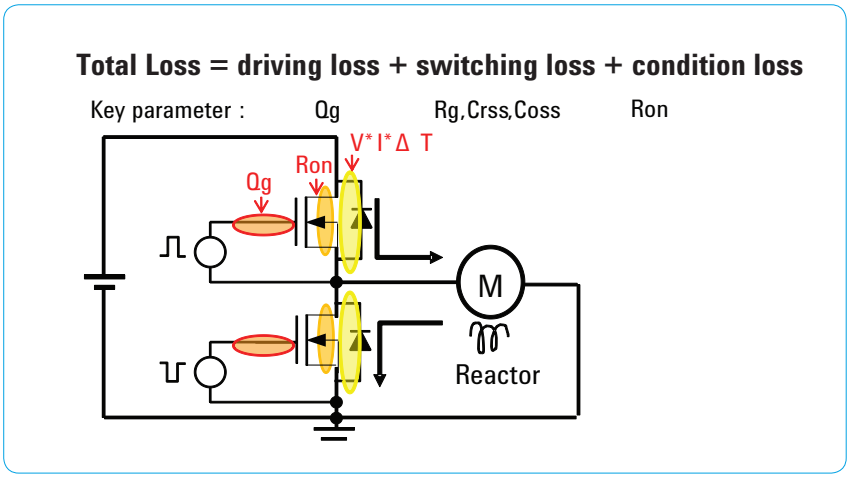


*Figure 1. Loss in Power Devices is the main factor of total circuit power loss*

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## Required evaluation for optimum power device selection

Selection of the correct power device for a power electronics circuit requires a detailed assessment of many parameters. Blocking voltage, leakage current and thermal characteristics are all important factors from reliability point of view. Saturation voltage, threshold voltage, trans-conductance and peak current are important from operation point of view. Minimizing power loss is essential to the overall design of an efficient power electronics circuit.

Power device losses can mainly be categorized into three elements; driving loss that is generated when driving the power device; switching loss that is generated when the device is turned on or off and conduction loss that is generated while the device is turned on (Figure 1). Conduction loss is dominant for switching frequencies below 10 kHz. Driving loss and switching loss become dominant as the switching frequency increases (Figure 2). Each type of power loss can be calculated via inherent device parameters.

Driving loss can be calculated from gate charge (Qg). Switching loss can be calculated from gate resistance (Rg) and device parasitic capacitances (or gate charge characteristics) while conduction loss can be calculated from on-resistance (Ron). It therefore follows that test equipment that can characterize these parameters is necessary for power loss evaluation. Device parasitic capacitances are broken down into input capacitance (Ciss), output capacitance (Coss) and reverse transfer capacitance (Crss).

Selection of a power device that has a good balance between on-resistance and device parasitic capacitances is the first step in the design of an efficient power electronics circuit. Gate charge is defined as a total amount of charge that is required to fully turn on a power device. It can also be seen as a parameter that represents the non-linear characteristics of device input capacitance, (Ciss = Cgs + Cgd). Both on-resistance and device parasitic capacitances are important in high switching frequency power devices with small FOM (Figure Of Merit), which is calculated as a product of Qg and Ron.

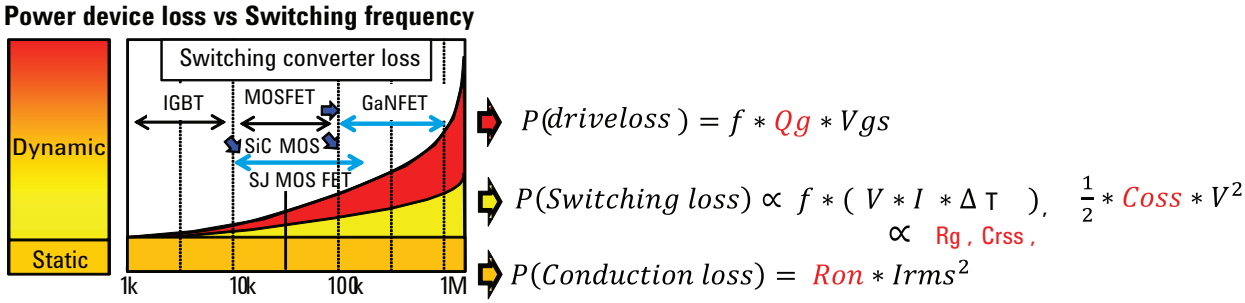


*Figure 2. Increasing driving loss and switching loss*

## What is Gate Charge?

Gate charge is the total amount of charge to turn on a power device. In other words it is the time integration of current flowing into gate terminal when the device transforms into the on-state. Driving loss is then calculated as product of gate charge, gate voltage, and frequency.

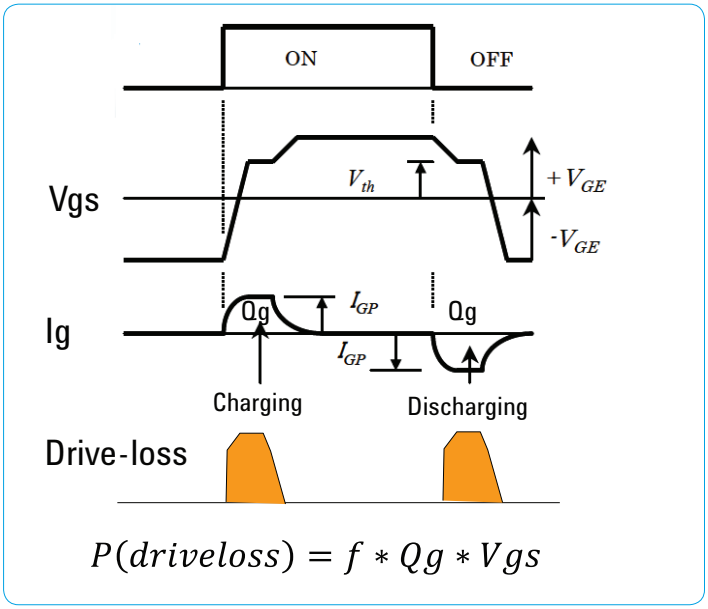


*Figure 3. Driving loss by gate charge*

As shown in Figure 4, gate charge characteristics are drawn as a continual curve that consists of three segments with different slopes.

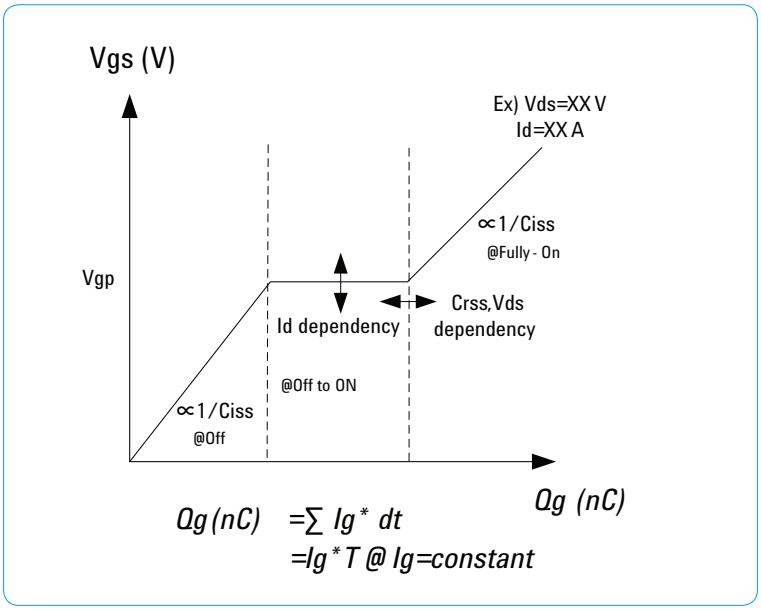


*Figure 4. Theoretical understanding of Qg curve*

## What is Gate Charge?

If gate current (Ig) is kept constant the gate charge is a product of Ig and time (t). Then, the Qg curve is obtained by making sampling measurement on gate voltage (Vgs). The first segment of the Qg curve represents Vgs rise where Ciss_off is being charged by Ig while the device is off. It is represented as Vgs = (1/Ciss_off)*Qg. Because Cgs is, in general, much bigger than Crss it can be approximated as Vgs = (1/Cgs)*Qg. The gate charge for this segment is called Qgs. When Vgs increases above threshold voltage (Vth) the drain (or collector) current starts to flow. Vgs in this segment is increased until the drain current reaches the rated current in the Id-Vgs characteristics. In the second segment with flat slope, where the device is changing state from on to fully-on, Vgs is not increased because all the Ig current flows into the Crss.

Figure 5 shows the capacitance characteristics of a transistor and Figure 5 (d) shows the voltage dependency of Crss. Changes in Crss can be classified into two distinct areas:

When Vds>Vgs Crss is increased according to the decrease of Vds. The amount of increased Qgd1 charge is:

$Qgd1=\int_{0}^{Vds-Vgs} Crss * dV$ Vds>Vgs, --- (1).

Qgd1 is called mirror charge.

In the Vgs> Vgd state Crss is significantly increased by channel forming under the Gate due to the device turn-on. The increase of Qgd2 charge is:

$Qgd2=\int_{Vds}^{Vgs} Ciss\_on * dV$ --- (2).

The value of Ciss_on is obtained from the Vgs – Ciss characteristics as shown in Figure 5(c). The charge in this segment is called Qgd. The size of Qgd depends on drain (or collector) voltage in off-state and the on-state of Crss.

$Qgd=Qgd1+Qgd2$ --- (3).

The Qgd value limits the device switching performance.

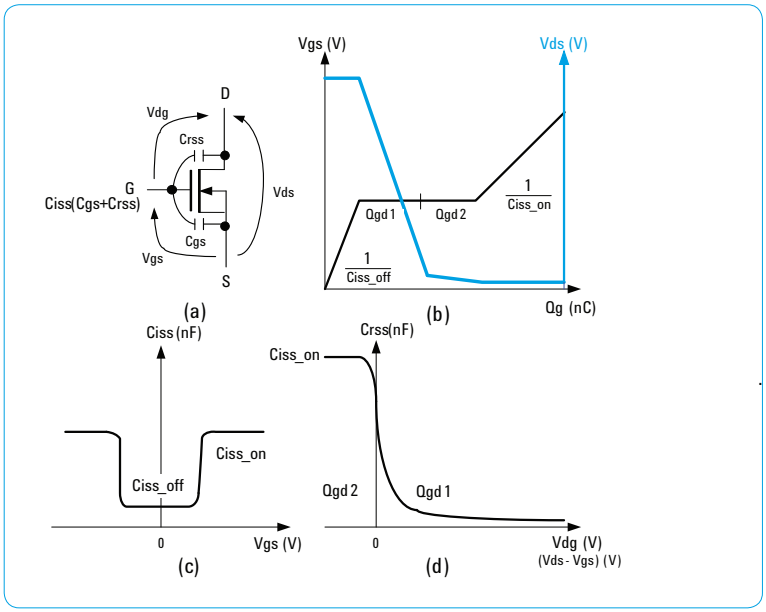


*Figure 5. Qg Characteristics by non linear Crss-Vdg Characteristics*

In the last segment the device is fully turned on and charging of Ciss_on is resumed. Vgs is represented as Vgs = (1/Ciss_on)*Qg.

## Design points for Driving Circuits

Circuit designers utilize gate charge characteristics to design gate drive circuits and to calculate driving loss. They set the gate driving voltage by considering device performance, dispersion, unexpected device turn-on and then read out total amount of charge from Qg curve. For example, let's assume that the Qg curve shown in Figure 6 is obtained with Vds=600 V and Id=100 A. If the gate is driven from 0 to 15 V the read out Qg is 500 nC. The driving loss is 0.15 W if the switching frequency is 20 kHz: [P(driving loss) = f * Qg * Vg = 20k * 500n * 15]. In addition, if you expect 100 ns rise time then at least 5 A [500 nC/100 ns] of drive current is required. Insufficient drive current delays switching speed resulting in increased switching loss. Maximizing drive current is an important parameter in drive circuit design.

It is generally recommended to drive the gate voltage of an IGBT from a negative value in order to avoid unexpected turn-on. The correct total Qg value is obtained from the sum of the Qg values in both the negative and positive voltage regions. For example in Figure 6 the gate voltage is swung from -15 V to +15 V and 400 nC has to be added to Qg resulting in a total drive loss of 0.27 W: [P(driving loss) = 20k * (400n + 500n) * 15].

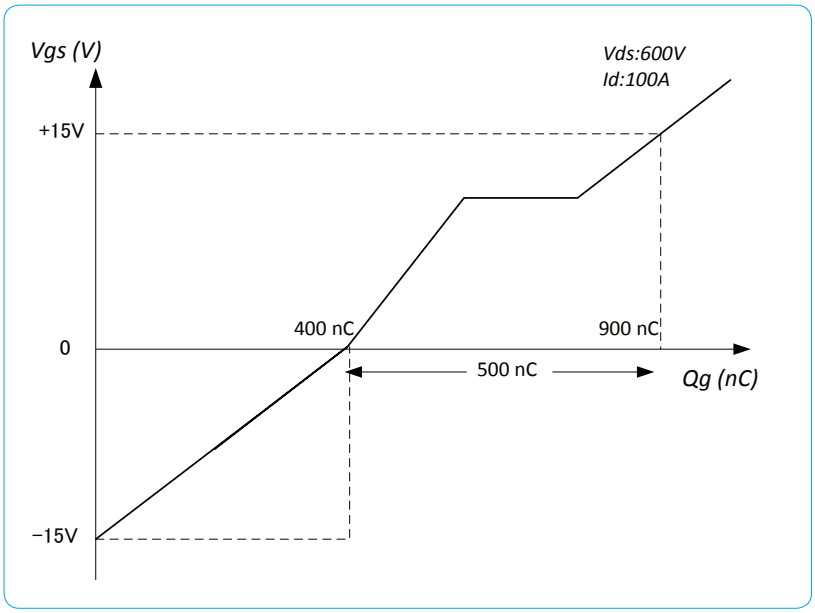


*Figure 6. Qg Characteristics from negative Vgs*

The Qg curve in combination with the device output voltage characteristics enable detailed analysis and optimization of a switching mode power device.

## Relationship between switching time and gate charge

A switching time calculation based upon a first order transient response of gate charge characteristics, gate series resistance (Rs) and input capacitance (Ciss) is often used. Rs is the sum of device gate resistance (Rg) and an external resistor attached to the gate.

Gate voltage Vgs, at a given time t, is represented using the gate drive voltage VGS, as follows:

Vgs(t)=VGS{1-e^(-t/(Ciss*Rs))) } ---- (4)

Therefore, t is given as:

t=(Ciss*Rs)*ln {VGS/(VGS-Vgs)} ---- (5)

Time constant is given as:

τ=(Ciss*Rs)  @ 63.2% of VGS --- (6)

Substituting Qg = Ciss * Vgs into equation (5) yields:

t=(Qg/Vgs)*Rs*ln {VGS/(VGS-Vgs)} ---- (7)

Utilizing (7) above the difference between t1 and t2 is as follows:

t2-t1=((Qg2-Qg1)/(Vg2-Vg1))*Rs*ln {(VGS-Vg1)/(VGS-Vg2)} ---- (8)

Td(on), Tr, Tf, and Td(off), as listed on a device datasheet, are calculated from (8) by substituting the corresponding data of; gate voltage, drain voltage and drain current versus Qg. The device manufacturer application note needs to be referenced for the definition of each switching time parameter.

- Turn On Delay time, Td(on): from 10% of VGS to 90% of VDS
  td(on)=((Qg2-Qg1)/(Vg2-Vg1))*Rs*ln {(VGS-Vg1)/(VGS-Vg2) ---- (9)
- Rise time, Tr: from 90% of VDS to 10% of VDS
  tr=((Qg3-Qg2)/(Vg3-Vg2))*Rs*ln {(VGS-Vg2)/(VGS-Vg3) ---- (10)
- Turn Off Delay time, Td(off): from 90% of VGS to 90% of VDS
  td(off)=((Qg6-Qg5)/(Vg6-Vg5))*Rs*ln {Vg6/Vg5 ---- (11)
- Fall time, Tf: from 10% of VD to 90% of VDS
  tf=((Qg7-Qg6)/(Vg7-Vg6))*Rs*ln {Vg7/Vg6}---- (12)

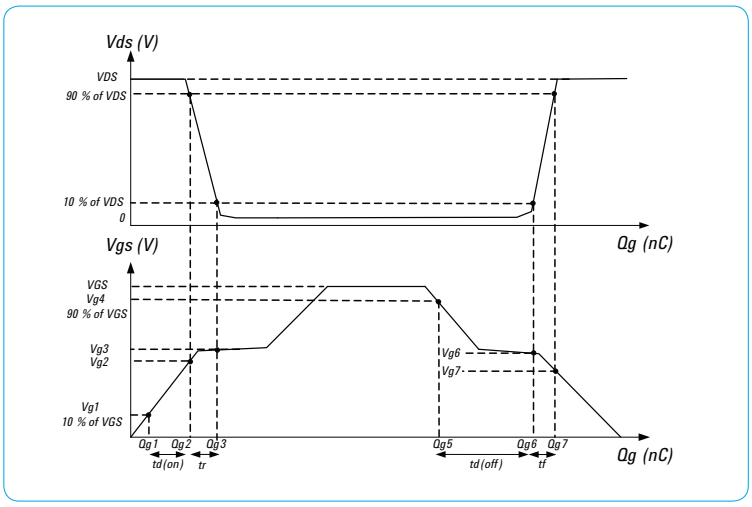


*Figure 7. Switching time calculation derived from Qg characteristics*

## Relationship between switching loss and gate charge

Switching charge (Qsw) is defined as the total charge in the period for which the drain voltage and the drain current are crossed. It is approximately equal to the mirror charge (Qgd1) of equation (1). In DC-DC converter design there is an established calculation of switching loss derived from Qsw.

The product of gate current (ig) and switching time (Tsw(on) or Tsw(off)) is Qsw which allows the following switching loss calculation for both device turn-on and turn-off. In the case of a purely resistive load, Id and Vds crosses at the midpoint. In the case of an inductive load, the phase of current and voltage is different and the loss factor changed. A pictorial representation is displayed in Figure 8.

Tsw(on)=Qsw/ig=Rs*Qsw/(VGS-Vgp) ---- (13)

Tsw(off)=Qsw/ig=Rs*Qsw/Vgp ---- (14)

Psw(inductive)=(½)*VDS*ID*(Tsw(on)+Tsw(off))*f ---- (15)

Psw(resistive)=(¼)*VDS*ID*(Tsw(on)+Tsw(off))*f ---- (16)

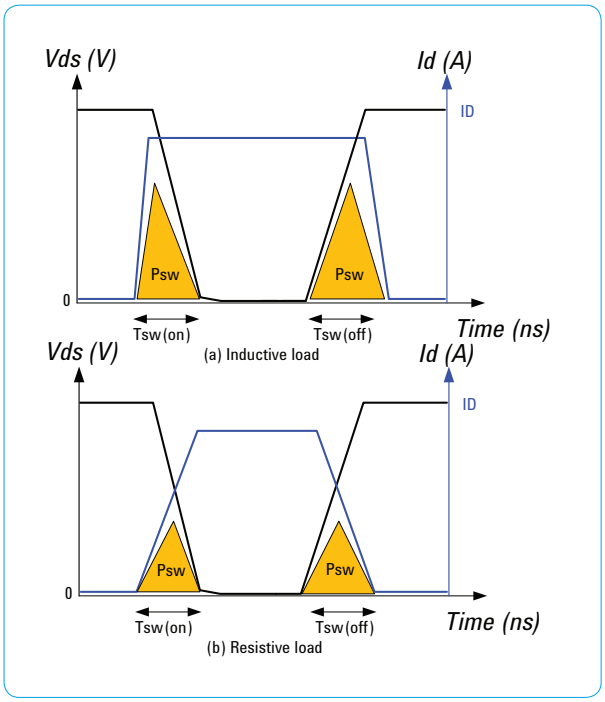


*Figure 8. Switching loss*

## Challenges to measure Gate Charge

A test circuit to measure a Qg curve is often shown on a device datasheet. Figure 9(a) shows a circuit with constant current source, Figure 9(b) shows one with resistive load while Figure 9(c) shows one with an inductive load. In the case of Figure 9(b) it is difficult to obtain the corner point between the first and second slope as the current has voltage dependency.

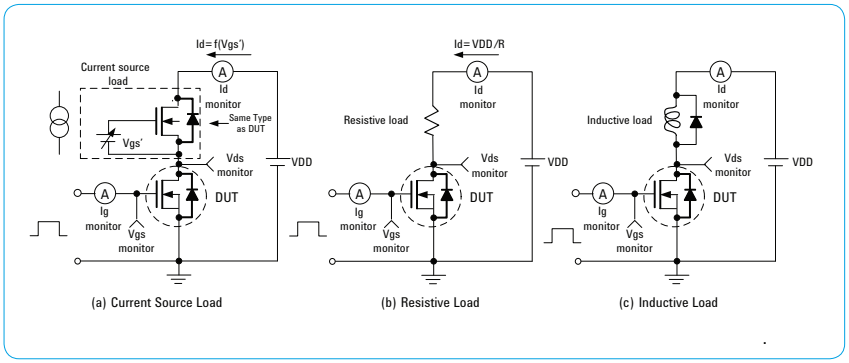


*Figure 9. Gate charge measurement circuits*

Although all three circuits appear simple it is difficult to design a Qg test environment for the following two reasons:

1. A stable power supply to provide accurate time dependent output voltage and current.

2. A gate drive circuit which can accurately measure time dependent current and voltage.

1. To measure Qg a stable high power supply is necessary. For example to supply 120 kW at 600 V it is necessary to supply 200 A current. Designing a stable power supply with this capability is difficult. Qg measurement observation requires only pulsed power to capture the switching transient response. Accordingly, current discharged from large capacitor is sufficient as a power supply. However, safe fabrication of such a system is difficult.

2. In order to evaluate Qg accurately a constant current source gate drive circuit is required. Qg is the product of constant current and the time. The Qg curve can be simply obtained by sampling Vgs over time. The slew rate of a gate drive voltage source should be well controlled otherwise device switching occurs too quickly and transient characteristics become difficult to measure.

Many device manufacturers own dynamic test systems dedicated to Qg measurement. However, it is difficult for circuit designers to access such a test system due to cost and size. Accordingly Agilent Technologies has developed a bench top instrument that can quickly and easily evaluate Qg in an office environment.

## A new and innovative Qg test technique

Agilent Technologies has developed a new method to derive complete Qg curves (Figure 10 Qg curve 3). This composite curve is fashioned from two different Qg curves. The first, (Qg curve 1) is measured with a high current low voltage test instrument while the second, (Qg curve 2) is measured with a high voltage low current test instrument.

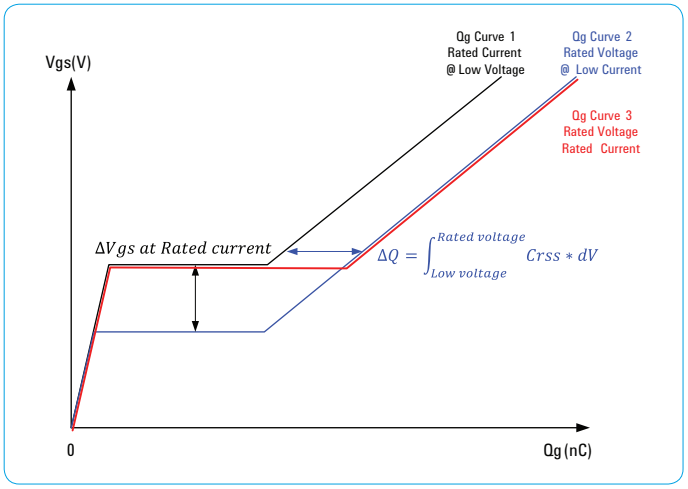


*Figure 10. New Qg measurement technique*

A high current low voltage instrument delivers the Qg curve during device turn-on while a high voltage low current instrument provides the Qg curve displaying the device Crss dependency. This technique eliminates the need for a huge power supply which is otherwise mandatory for high voltage and high current devices.

Agilent Technologies has developed a test system with a constant current source gate driver. This is used in combination with a high current but low voltage and high voltage but low current drain (collector) supply with simultaneous voltage and current sampling capability. This unique combination enables complete gate charge measurement, switching time and the resultant loss calculation.

Table 1 shows an example IGBT and super junction MOSFET characterization by measuring Ron/Qg/Rg/Crss characteristics. The super junction MOSFET has switching loss advantages over the IGBT for frequencies in excess of 20 kHz of switching frequency for measurements performed under similar conditions.

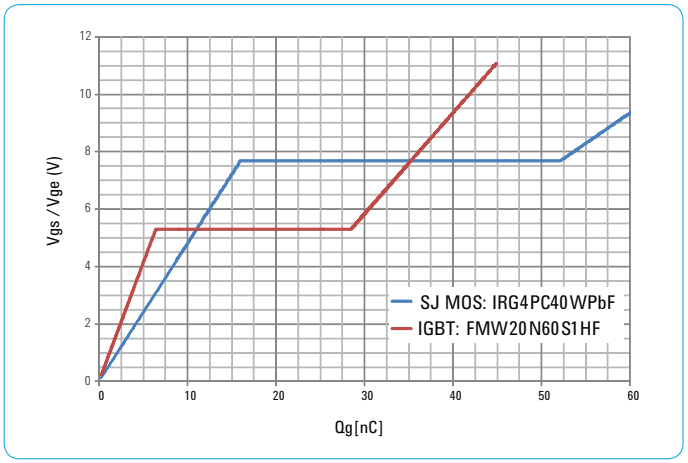


*Figure 11. Gate Charge Characteristics of IGBT and Super Junction MOS FET*

## A new and innovative Qg test technique

*Table1. Comparison table of IGBT/MOS's switching loss*

| Conditions | | |
|---|---|---|
| VDS | 480V | |
| ID | 20A | |
| Vgs | 0 to 10V | |
| Switching Frequency | 10kHz / 20kHz | |
| Ton Duty Cycle | 10% | |
| Gate Series Resistance | 27Ω | |
| Device Type | IGBT | Super Junction MOS FET |
| | IRG4PC40WPBF | FMW20N60S1HF |
| **Measured** | | |
| Qg | 63 nC | 42 nC |
| Qgd | 36 nC | 22 nC |
| Qsw (=Qgd1) | 12.2 nC | 10.0 nC |
| Rg | 0.7 Ω | 3.5 Ω |
| Vce_sat/ Rds_on @ 20A | 1.95 V | 183 mΩ |
| **Calculated** | | |
| Td(on) | 39 ns | 15 ns |
| Tr | 47 ns | 28 ns |
| Tf | 28 ns | 36 ns |
| Td(off) | 162 ns | 170 ns |
| P(driving loss) | 6.3 mW | 4.2 mW |
| P(Switching loss) @L load | 9.0 W /18.1 W | 5.8 W/11.5 W |
| P(conduction loss) | 3.9 W | 7.3 W |
| Total Power loss | 12.9 W /22.0 W | 13.1 W/18.8 W |

## Device evaluation by Agilent Technologies B1506A

The B1506A Power Device Analyzer for Circuit Design is an industry first bench top instrument that has Qg curve test capability up to 1500 A/3 kV. It can generate complete Qg curves from 1 nC to 100 µC using a new and innovative method using a sophisticated gate driver with sensitive current control in combination with high current/low voltage source/sampling and high voltage/low current source/sampling capabilities.

*Table 2. B1506A Qg curve measurement range.*

| Measure/control parameter | Range | Minimum resolution |
|---|---|---|
| Qg | 1 nC to 100 µC | 10 pC |
| Vdd | +/- 0 V to 3000 V | 100 µV |
| Id Limit | +/- 1 A to 1100 A | 2mA |
| Ig | +/- 1 nA to 1 A | 10 pA |
| Vg | +/- 30V | 40 µV |
| On Time | 50 µs – 950 µs | 2 µs |
| Driver Vg for Current load | +/- 30 V | 40 µV |

In addition to IV characteristics the B1506A can also measure device parasitic parameters: Rg, Ciss, Crss, Coss, Cgs, Cds. Accordingly, it can validate a power device from two different perspectives. Additionally, it also can calculate switching time (td, tr, tf), power losses (driving, switching and conduction) from Qg curves and other measured parameters. Finally, temperature dependency characteristics from -50°C to +250°C can be measured.

The Agilent Technologies B1506A can evaluate all necessary circuit design parameters over a wide range of operating conditions.

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