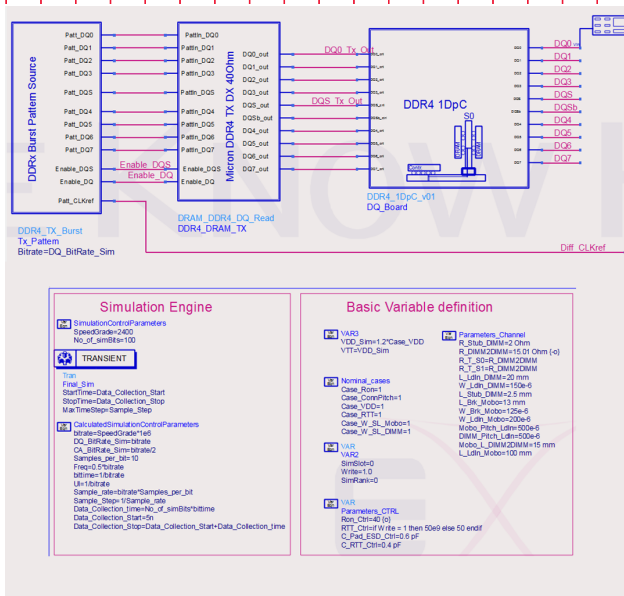


Keysight W2351EP DDR4 Compliance Test Bench

Data Sheet



Introduction

The W2351EP DDR4 Compliance Test Bench helps solve the problem of simulation-measurement correlation. In the past, the pre-manufacture design could be simulated and tested using compliance tools from an EDA vendor. And the post-manufacture prototype could be bench tested using compliance tools from test and measurement instrument vendors. However, because of subtle differences between the two vendors independent approaches to compliance, it was almost impossible to correlate the two. This opened the possibility of the pre-manufacture design passing and the post-manufacture prototype failing, necessitating a time-consuming and expensive design spin.

In contrast, the DDR4 Compliance Test Bench leverages the exact same industry-leading Compliance App used on Agilent Infiniium oscilloscopes. It mimics a real hardware test bench, and, using a scripting technology called "Waveform Bridge," emits the same waveforms that the Infiniium app receives when you are testing in your lab. Thus, the exact same tests - no ifs, ands, or buts - are applied to both the pre-manufacture simulated design and the actual post-manufacture prototype.

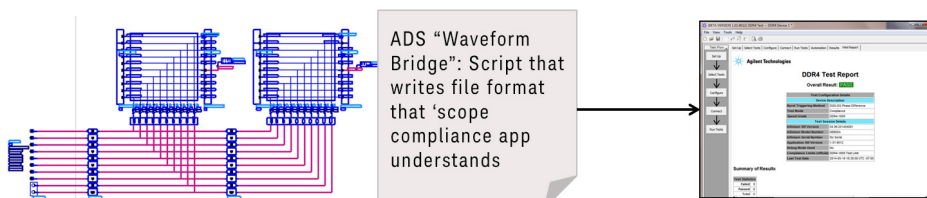
Benefits Across The Development Process

Run a sign-off compliance test on the simulated test bench waveforms before committing to fabrication. Run the exact same tests on the simulated testbench that will be run on the oscilloscope in the test lab when prototypes come back from fab.

- DDR controller designer at an IC company may swap out the simulated testbench's generic controller model with actual controller I/O model
- PCB/package/DIMM designer at an OEM or IC company may swap out parts of the simulated testbench's generic channel cascade with the post-layout EM-based model of actual package (or PCB or DIMM)
- DRAM I/O designer at an IC company may swap out the simulated testbench's generic DRAM model with actual DRAM I/O model



Design and simulate...



... then fabricate with confidence...

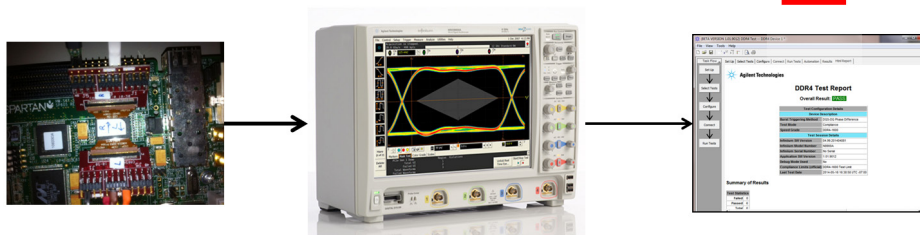


Figure 1. Engineers can apply the same set of compliance tests and receive the exact same compliance report on the simulated design as they will use on the fabricated prototype.

Simulated Test Bench

The simulated test bench is composed of subcircuits, namely a DDR controller, a channel, and a DDR memory chip. The circuit runs under the pre-requisite ADS Transient Simulator. The generic chip I/Os are represented by traditional IBIS models, but you can swap out one or both of these with either IBIS or netlist models that are more specific to your design. Likewise, any or all parts of the generic channel model cascade (consisting of the controller package, motherboard, DIMM connector, DIMM PCB, memory package) can be replaced with pre- or post-layout models. For example, an electromagnetic (EM) field solver can be used to create an S-parameter model of a byte lane on the post-layout motherboard.

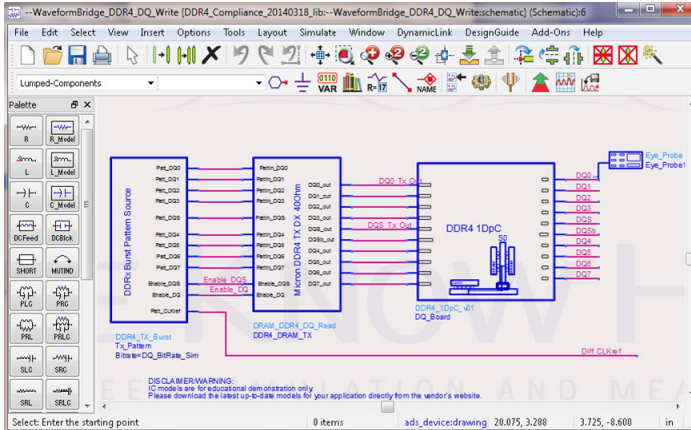
Waveform Bridge Script

Once the simulated testbench has been adopted to reflect your pre-manufacture design, the Transient simulation runs writing the appropriate waveforms to the dataset. The Waveform Bridge script is a post-processing step that takes waveforms in the data set and writes them to a file that the Infiniium Compliance Test Application can parse.

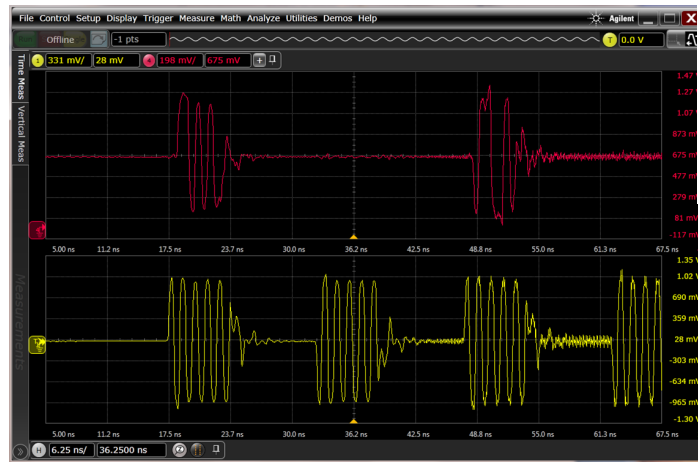
Use with N6462A DDR4 Compliance Test Application

The file that the Waveform Bridge writes can be read into the N6462A DDR4 Compliance Test Application for Infiniium 9000 and 90000 Series Oscilloscopes. This application can be run using stored (“offline”) data. In this way you can be assured that the tests you run on the pre-manufacture design simulation will be identical to the ones you will run when the prototype is subsequently manufactured.

Step 1. Set up simulation using W2351EP DDR4 Compliance Test Bench



Step 2. ADS simulation of DQS and DQ waveforms run in the Infiniium Offline Display



Step 3. Define set of compliance tests to run on simulated or “stored data”

List Of Tests Group			
-VSEH/VSEL for Strobes			
Test Group Signal Requirement:			
Signal Required	Compulsory/ Optional	Signal Loaded Status	Overall Signal Loaded Status:
DQS	Compulsory		
DQ	Compulsory		
CS	Optional		
-VSEH/VSEL for Clocks			
Test Group Signal Requirement:			
Signal Required	Compulsory/ Optional	Signal Loaded Status	Overall Signal Loaded Status:
CLK	Compulsory		
-VOH/VOL			
Test Group Signal Requirement:			
Signal Required	Compulsory/ Optional	Signal Loaded Status	Overall Signal Loaded Status:
DQS	Compulsory		
DQ	Compulsory		
CS	Optional		

Step 4. Generate the same report on your simulated data as you generate on your prototype

DDR4 Test Report

Overall Result: **PASS**

Test Configuration Details	
Device Description	
Burst Triggering Method	DQS-DQ Phase Difference
Test Mode	Compliance
Speed Grade	DDR4-1600
Test Session Details	
Infiniium SW Version	04.99.201404081
Infiniium Model Number	N8900A
Infiniium Serial Number	No Serial
Application SW Version	1.01.9012
Debug Mode Used	No
Compliance Limits (official)	DDR4-1600 Test Limit
Last Test Date	2014-05-16 16:38:58 UTC -07:00

Typical Configuration

Product
W2210 ADS Core+ Transient Convolution
W2351 ADS DDR4 Compliance Test Bench
N8900A-001 Infiniium Offline
N8900A-002 DSA Package (EZJIT Plus and SDA)
N6462A-1TP DDR4 Compliance Transportable License

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