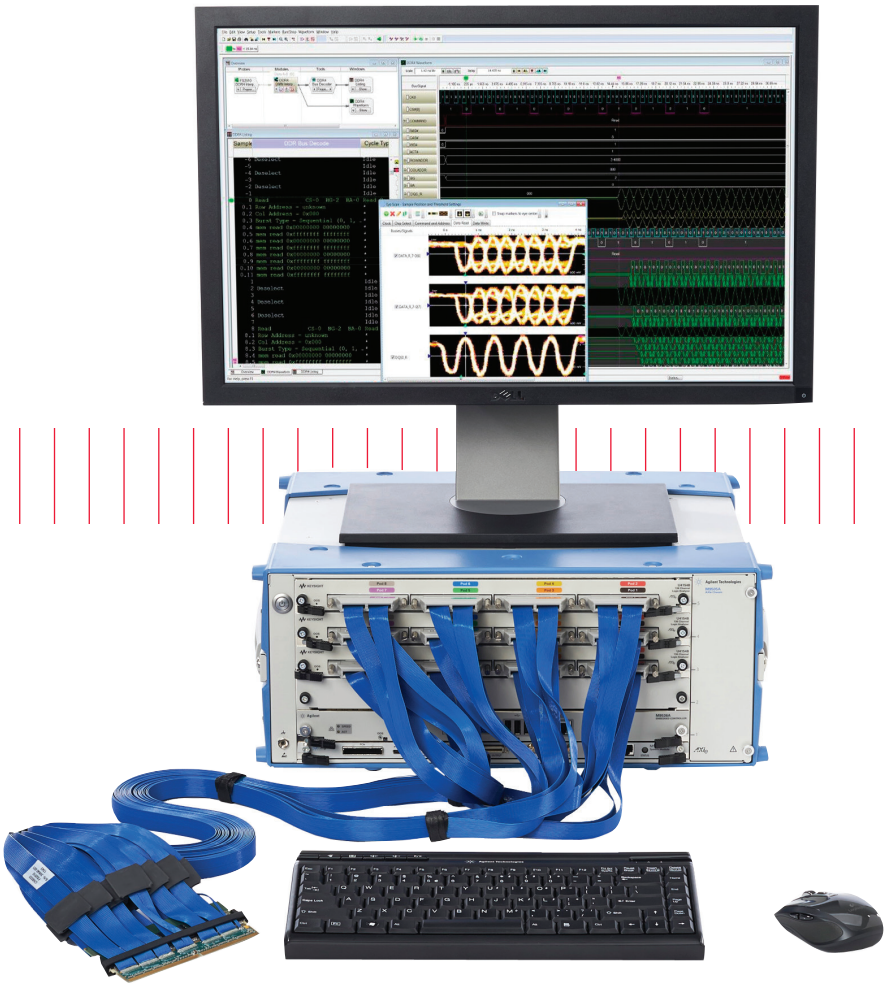
Keysight U4154B

4 Gb/s State Mode Logic Analyzer Module



Data Sheet

KEYSIGHT TECHNOLOGIES

Introduction

Product Description

The Keysight Technologies, Inc. U4154B logic analyzer system combines reliable data capture with powerful analysis and validation tools to enable you to quickly and confidently validate and debug high speed digital designs operating at speeds up to 4 Gb/s.

Figure 1A shows the small Read DQ eyes associated with a DDR4 system operating at 2400 Mb/s data rate. This screen shot is captured in signal trace mode with no back to back bursts so that the eyes for the entire burst of 8 are displayed. The U4154B logic analyzer uses its unique eye scan capability to auto-matically place the sampling point in both time and voltage within the eye on each individual channel for optimal sampling reliability.

Figure 1B shows the trigger setup to capture a burst of 8 Writes. The trigger sequencer operates up to 2.5 GHz, enabling accurate and precise triggering.

Figure 1C and Figure 1D show the state listing and waveform for this capture.

12.5 GHz Timing Zoom with 256 K sample memory gives you simultaneous state and high-resolution timing measurements covering a time span of 20 us, which corresponds to 43680 clock cycles at a 2133 MHz clock rate.

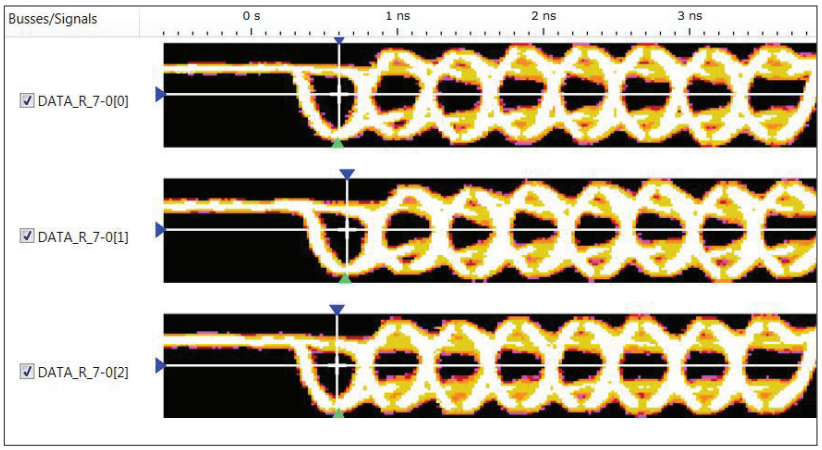


Figure 1A

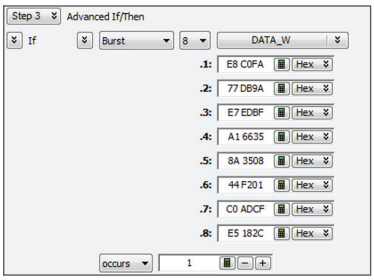


Figure 1B

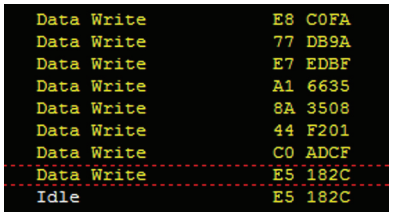


Figure 1C

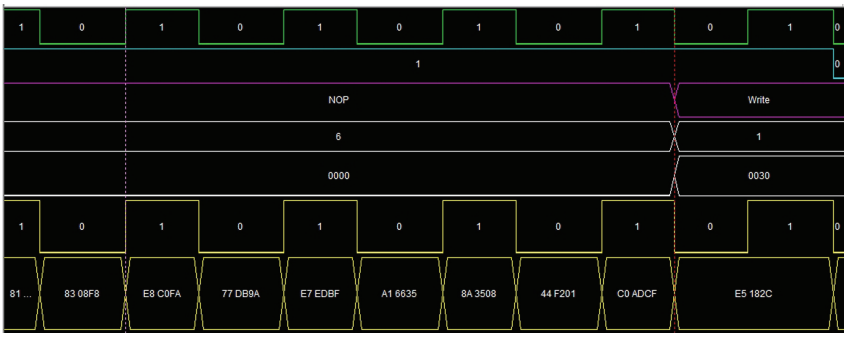


Figure 1D

Available memory depth up to 200 M samples allows you to debug very complex problems where the cause and symptoms may be separated by several seconds. The amount of memory can be upgraded after purchase; see “Upgrades” in ”Ordering Information.”

No need to sacrifice sampling resolution to view more system activity. In timing mode, if your system has bursts of activity followed by times with little activity, you can use transitional timing along with the logic analyzer’s deep memory to capture seconds to minutes of activity at 400 ps (2.5 GHz) sampling resolution. You also have the flexibility to increase the amount of time captured by excluding certain buses or signals from the transition detector, for example clock or strobe signals that add little useful information to the measurement. In State mode, use store qualification to save only states of interest into memory.

The dual-sample mode has two benefits: For DDR memory signals up to 2.5 Gb/s, it allows seperation of reads from writes, with automatic setup of the correct sampling positions for each. Dual sample mode also allows acquisition of state (synchronous) data at rates up to 4 Gb/s. When used in this mode, the data will appear in two labels. One label for rising edge and another for falling edge captures. The logic analyzer will be clocked with one edge of the system clock. Labels can be merged using the Keysight B4602A Signal Extractor tool. When operated in dual-sample mode on all pods, the channel count is 68 channels for one U4154B 136 channels for two U4154Bs, or 204 channels for three U4154B modules combined. Dual-sample mode can be selected on a per-pod-pair basis, so if you have only a subset of signals that require dual-sample mode, the channel count can be higher.

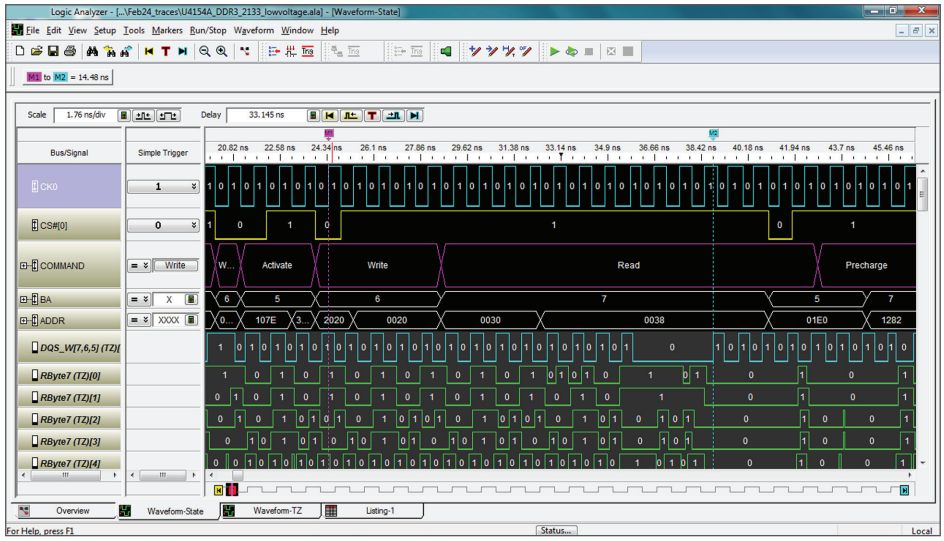


Figure 2. Timing Zoom precisely measures the time between the rising edge of the clock and the rising edge of DQS in a DDR system.

For DDR2/3/4 and LPDDR/2/3/4 memory solutions under 2.5 Gb/s data rates, dual sample mode is used to separate read and write data traffic. The B4621 DDR2/3/4 decoder or the B4623B LPDDR/2/3/4 decoder reassembles the data to align with the associated commands. (There’s no need for the B4602A tool for DDR and LPDDR solutions.)

For DDR4 and LPDDR4 memory solutions over 2.5Gb/s, double probing is required to capture Read and Write DQ signals and dual sample mode is used to capture rising and falling edge DQ samples. Using this technique, a maximum of 34 DDR4 or LPDDR4 DQ signals operating over 2.5 Gb/s can be captured per U4154B module. Address, command, and control signals for DDR or LPDDR memory do not require double probing above or below 2.5Gb/s data rates.

Support for bursty clock allows you to take measurements that include periods of inactivity on the clock, such as power management transitions when the clock is inactive.

In state mode, the U4154B allows one clock input into pod 1 of the clocking module.

- Single module pod 1 has clock any slot
- Double module set - pod 1 bottom module of set is clocking module
- Three card set - pod 1 of middle module is clocking module

There are five clock qualifiers available on the clocking module. The clock inputs to pods 2, 3, 4, and 5 can be used as “AND” or “OR” clock qualifiers. The “RESET” clock qualifier input on pod 7 is available as an “AND” input only when the other clock qualifiers are setup as “OR” inputs. The most common use mode for this clock qualifier is to capture “RESET” when the other clock qualifiers are looking for CKE.

DDR measurements made fast, easy, and powerful

The DDR setup assistant simplifies measurement setup and minimizes the time to make your first measurement. The DDR setup tool guides you through even the most complex DDR setup in minutes. DDR eye scan makes it easy to determine the optimum acquisition sample point without requiring an oscilloscope. Keysight qualified scans place the sample position at the center of the eye on every individual channel for maximum data capture reliability, including separate sampling positions for read and write data.

The DDR setup assistant includes a variety of powerful, time-saving trigger features optimized for DDR measurements. Burst trigger captures an entire data burst of 8 on DDR memory systems from one sequence level in the trigger menu. Intuitive trigger macros with diagrams provide visualization of triggering options and simplify the process of creating triggers.

The DDR setup assistant tool is available at no charge as part of the Keysight DDR/LPDDR memory support tools software package that can be downloaded from www.keysight.com/find/lpa-sw-download.

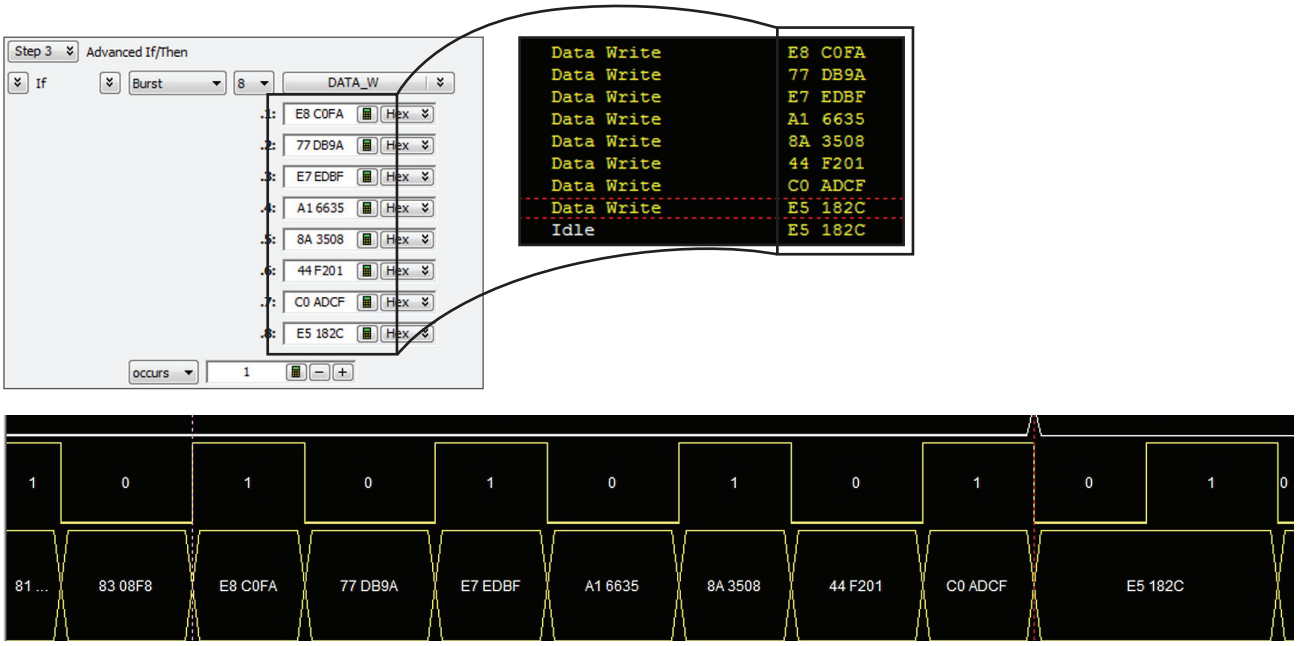


Figure 3. Burst recognizer trigger makes it easy to trigger on events in a burst read or write.

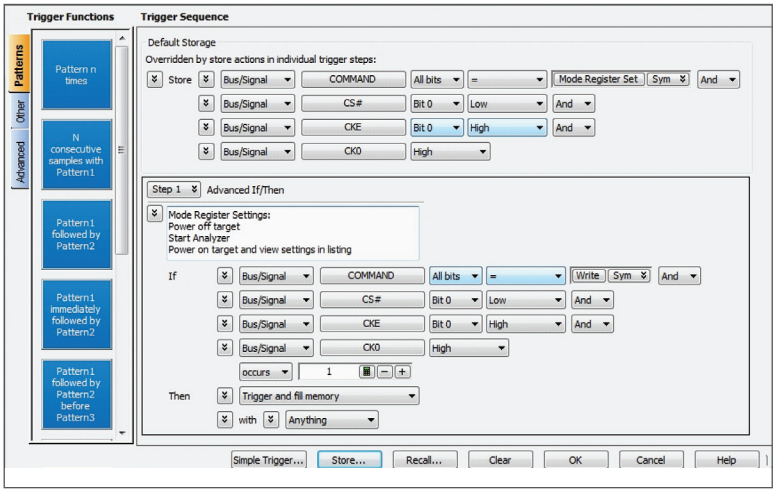


Figure 4. Mode register set trigger allows you to capture key events during initialization without wasting valuable memory.

Signal integrity insight made fast and easy

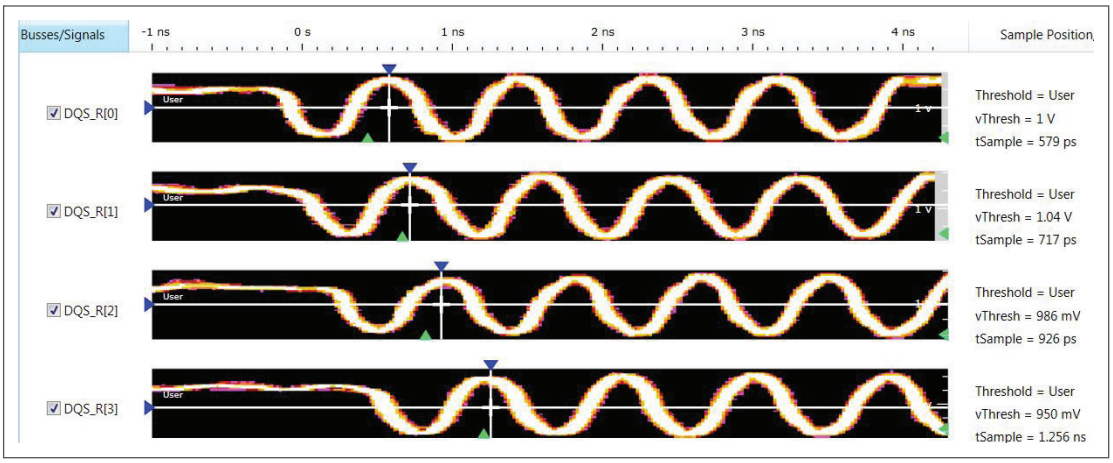


Figure 5. Burst qualified eye scan allows you to view the activity on the signals only when a burst taking place. Screen shot above shows DDR4 2400 Mb/s is Read DQS scanned in signal trace mode with no back to back bursts.

As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement in the design validation process. Eye scan lets you acquire signal integrity information on all the buses in your design, under a wide variety of operating conditions, in a matter of minutes. Identify problem signals quickly for further investigation with an oscilloscope. Results can be viewed for each individual signal or as a composite of multiple signals or buses. Support for up to 5 clock qualifiers, the ability to qualify scans of any signal from any combination of other signals, full triggering capabilities for scan qualification, and customizable viewing windows allows you to sample only when the qualifying signal is active and see specific system activity of interest. The eye scan technology in the U4154B provides insights that can't be achieved with any other test method.

DDR eye scan automatically groups signals so you can quickly spot byte lane related signal integrity problems. Scans can be qualified based on state trigger criteria, thus providing unique insight. For example, read and write scans can be separated for greater insight. Signal trace mode scan allows you to gather signal integrity information on two read or write cycles separated by only one cycle.

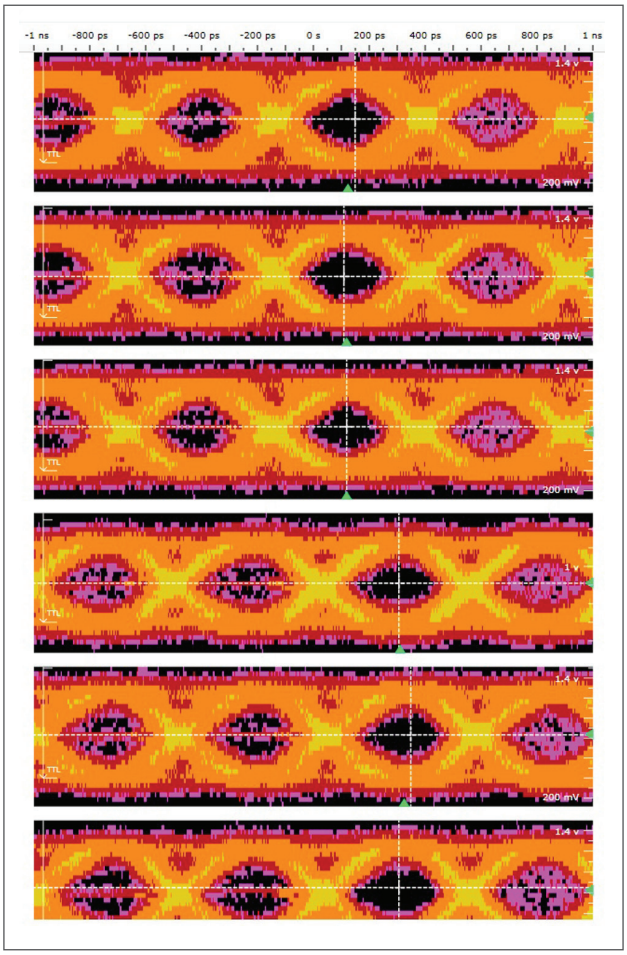


Figure 6. Eye scan clearly indicates the DDR3 byte lane shift caused by fly-by routing.

Harness your logic analyzer and scope for powerful insight

Combine the powerful triggering and protocol analysis of a logic analyzer with the signal integrity insight of a scope to solve tough design problems. Keysight ViewScope allows you to easily make time-correlated measurements between Keysight logic analyzers and oscilloscopes. The time-correlated logic analyzer and oscilloscope waveforms are integrated into a single logic analyzer waveform display for easy viewing and analysis. You can also trigger the oscilloscope from the logic analyzer (or vice versa), and automatically de-skew the two instruments.

ViewScope enables you to perform the following tasks more easily, quickly, and effectively:

- Validate signal integrity
- Track down problems caused by signal integrity
- Validate correct operation of A/D and D/A converters
- Validate correct logical and timing relationships between the analog and digital portions of a design

Operating modes

Operating mode	Conventional state (synchronous) Option -02G	Conventional state (synchronous) Option -01G (std)	Dual sample state Option -02G	Dual sample state Option -01G (std)	Conventional timing full channel	Conventional timing half channel	Transitional timing full channel	Transitional timing half channel	Timing Zoom
Acquisition rate	2.5 Gb/s	1.4 Gb/s	4 Gb/s	2.8 Gb/s	2.5 GHz	5 GHz	2.5 GHz	5 GHz	12.5 GHz
Number of channels in one U4154B	136	136	68	68	136	68	136	68	136
Number of channels in two U4154Bs combined	272	272	136	136	272	136	272	136	272
Number of channels in three U4154Bs combined	408	408	204	204	408	204	408	204	408
Memory depth (samples)									
Base memory	2 M	2 M	2 M	2 M	2 M	4 M	2 M	4 M	256 K
Opt 004	4 M	4 M	4 M	4 M	4 M	8 M	4 M	8 M	256 K
Opt 008	8 M	8 M	8 M	8 M	8 M	16 M	8 M	16 M	256 K
Opt 016	16 M	16 M	16 M	16 M	16 M	32 M	16 M	32 M	256 K
Opt 032	32 M	32 M	32 M	32 M	32 M	64 M	32 M	64 M	256 K
Opt 064	64 M	64 M	64 M	64 M	64 M	128 M	64 M	128 M	256 K
Opt 128	128 M	128 M	128 M	128 M	128 M	256 M	128 M	256 M	256 K
Opt 200	200 M	200 M	200 M	200 M	200 M	400 M	200 M	400 M	256 K

Contact Keysight Technologies for information on additional configurations.
Note: Memory can be upgraded after purchase. See “Upgrades” in “Ordering Information.”

When you need more channels or more functions

Multiframe allows you to combine 16 plus AXIe chassis.

Note: One PC host is recommended for each AXIe chassis.

Applications

- Functional and parametric validation of memory systems and other high-speed digital systems operating up to 4 Gb/s
- Debug of hardware and software in high-speed digital systems operating up to 4 Gb/s

Features

- State capture up to 4 Gb/s on 68 channels, 2.5 Gb/s on 136 channels per module
- Reliable data capture on eye openings as small as 100 ps by 100 mV
- 12.5 GHz Timing Zoom with 256 K sample memory
- Memory depth up to 200M samples
- Wide variety of probing solutions including BGA, interposer, mid-bus, and flying leads
- Up to 10,880 channels in a system using Multiframe

Customer values

- Confidence in state measurements with signal eye openings as small as 100 ps by 100 mV
- Rapidly view signal integrity information on all the buses in your design, under a wide variety of operating conditions, in a matter of minutes
- Quickly and easily set up complex DDR measurements

Hardware platform

Minimum hardware

Module

One or more U4154B 136-channel logic analyzer modules.

- Three U4154Bs can be combined for a maximum of 408 channels on a single time base and trigger sequencer.
- Three U4154B are required to capture all ADD/CMD/Data from a DDR4 DIMM interposer for data rates over 2.5 Gb/s.
- Two U4154Bs are required to capture all read and write data on a 64 data bit DDR2/3/4 interface for data rates up to 2.5 Gb/s.
- DDR2/3/4 solutions requiring 5 pods or less one U4154B module.
- LPDDR1/2/3/4 solutions operating up to 2.5 Gb/s, requiring 4 pods or less one U4154B module.
- LPDDR4 operating more than 2.5 Gb/s may require up to three merged U4154B modules depending on the number of data signals probed and the probing layout.

For DDR Memory systems operating above 2.5 Gb/s, double probing of the DQ signals provides capture of read and write traffic with dual sample mode used for the rising and falling edge samples. Users should expect to use four U4154B inputs for each DDR memory DQ captured at data rates more than 2.5 Gb/s.

Chassis and controller

Keysight M9502A 2-slot or M95905A 5-slot AXIe chassis. Refer to www.keysight.com/find/axie-chassis*

One M9536A AXIe Embedded Controller. Or:

One user-supplied PC equipped with PCIe link or capable of accepting a PCIe adapter. 64-bit OS ONLY. Windows Vista, Windows® Server 2008, Windows 7, Windows® Server 2008 R2, Windows 8, Windows® Server 2012, Windows 8.1, Windows® Server 2012 R2.

Version 6.0 or higher 64-bit application software for logic and protocol analyzers. Available for download from www.keysight.com/find/lpa-sw-download

For laptop PCs:

- One Keysight M9045B PCIe ExpressCard Adaptor
- One Keysight Y1200B PCIe cable: x1 to x8, 2.0m

For desktop PCs:

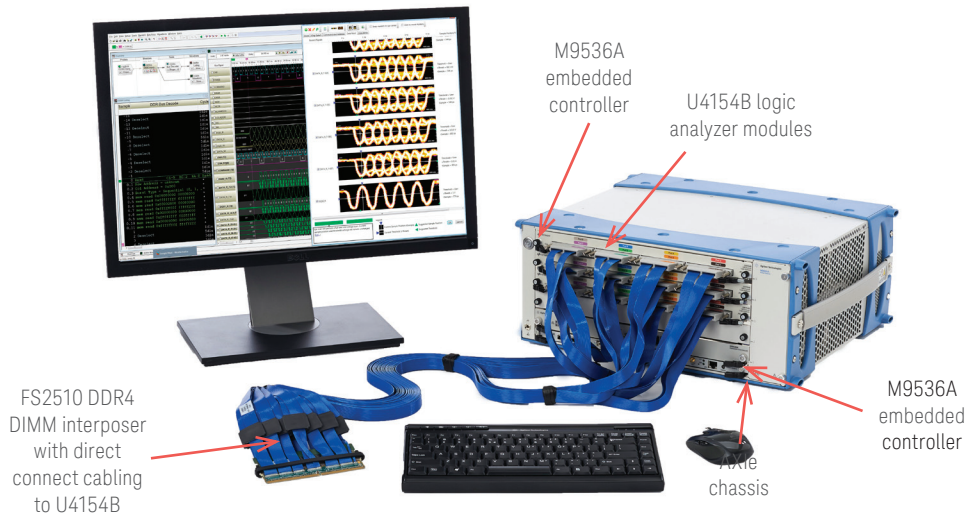
- One M9048A PCIe Desktop Adaptor

Interposers with direct connect cabling, as shown in the photo below with the DDR4 DIMM interposer, do not require additional U4201A cables.

Cables

Up to four U4201A logic analyzer cables may be required per U4154B module depending on probing method. See probing chart for details.

* 5-slot chassis is required for three merged modules or for two merged modules when used with M9536A embedded controller as the M9536A consumes the bottom slot in a chassis.



Probes as required to connect to the target system. (Probes in this chart require U4201A cables.)

Probe type	Model number	Channels	Maximum data rate	Supported signal types	Number of U4201A required per probe
Soft Touch Connectorless Pro Series	E5406A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock	1 for each E5406A
Soft Touch Connectorless Low Profile	E5402A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock	1 for each E5402A
Soft Touch Connectorless Classic	E5390A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock	1 for each E5390A
Soft Touch Connectorless Half-size	E5398A	17 (16 data, 1 clock)	4 Gb/s	Single-ended data, differential or single-ended clock	1 for every E5398A
Soft Touch Connectorless Pro Series	E5405A	17 (16 data, 1 clock)	4 Gb/s	Differential or single-ended data, differential or single-ended clock	1 for every 2 E5405A
Soft Touch Connectorless Classic	E5387A	17 (16 data, 1 clock)	4 Gb/s	Differential or single-ended data, differential or single-ended clock	1 for every 2 E5387A
Samtec connector	E5378A	34 (32 data, 2 clock)	1.5 Gb/s	Single-ended data, differential or single-ended clock	1 for each E5378A
Samtec connector	E5379A	17 (16 data, 1 clock)	1.5 Gb/s	Differential or single-ended data, differential or single-ended clock	1 for every 2 E5379A
Mictor connector	E5380A	34 (32 data, 2 clock)	600 Mb/s	Single-ended data, differential or single-ended clock	1 for each E5380A
General purpose flying leads	E5382B	17 (16 data, 1 clock)	1.5 Gb/s	Single-ended data, differential or single-ended clock	1 for every 2 E5382B
General purpose flying leads	E5381B	17 (16 data, 1 clock)	1.5 Gb/s	Differential or single-ended data, differential or single-ended clock	1 for every 2 E5381B

Recommended probes for DDR and LPDDR memory include BGA probes, interposers, and Soft Touch mid-bus probes. Interposers are available from FuturePlus Systems or through Keysight. Refer to "Ordering Information." Information on FuturePlus interposers http://www.futureplus.com/DDR3-Memory/keysight-la-support-overview.html.

For additional DDR/2/3/4 and LPDDR/2/3/4 probing options, contact your local Keysight representative www.keysight.com/find/contactus.

Optional Hardware

Multiframe extensions

Up to 16 AXIe chassis can be combined in a single Multiframe system.

One or more Y1223A Multiframe cables to connect multiple frames. Order one fewer Y1223A cables than the total number of frames/chassis to be combined.

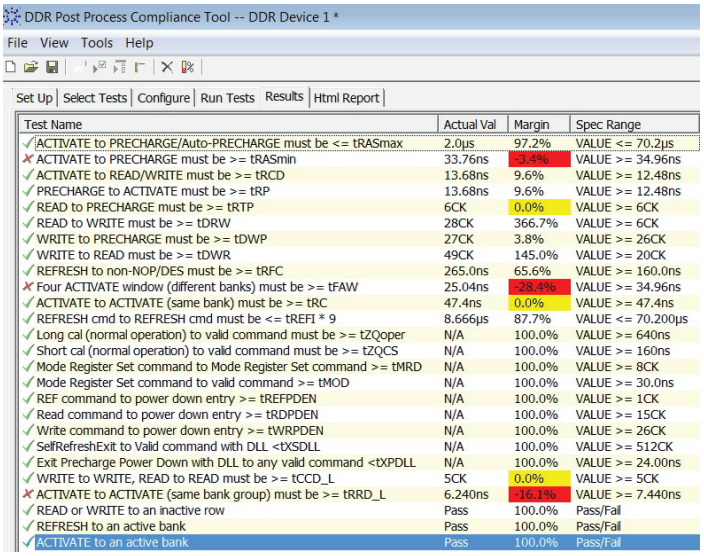


Figure 8. Figure 8. B4622B compliance toolset. Example of DDR4 compliance violations display.

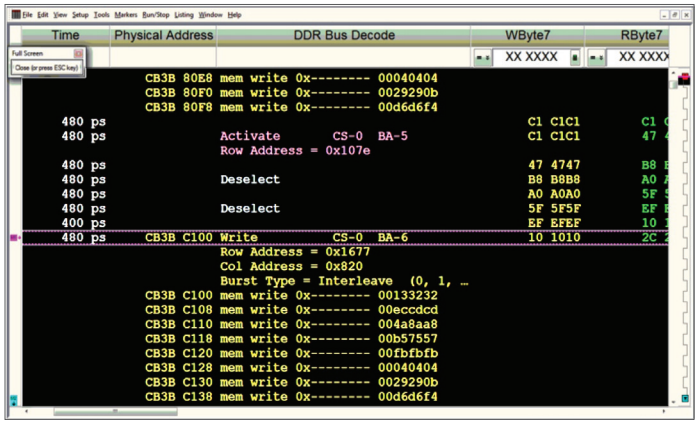


Figure 9. The B4621B protocol-decode software displays acquired signals as easily understood bus transactions.

Optional software

B4622B DDR2/3/4 or LPDDR/2/3/4 Protocol Compliance and Analysis Tool

Achieve greater protocol insight faster using the B4622B Protocol Compliance and Analysis toolset for DDR2, DDR3, DDR4, LPDDR, or LPDDR2/3/4. The B4622B provides four SW tools in one set covering automated Real-Time violation capture, protocol violations detection on captured traces, performance measurements, and physical address trigger setup for DDR2/3/4 or LPDDR/2/3/4. Create your own regression test suite for your DDR2/3/4 or LPDDR/2/3/4 or other digital system probed by your Keysight logic analyzer. Accelerate your regression test results by adding any valid logic analyzer trigger to customize your suite of automated Real-Time protocol or bus level timing violations.

Monitor your DDR2/3/4, LPDDR/2/3/4 or other digital system continuously for elusive, intermittent violations in protocol or bus level timing with your customizable Real-Time violation capture tool.

Bus decoders for DDR2/3/4 or LPDDR/2/3/4 validation

The B4621B bus decoder for DDR2, DDR3, or DDR4 and B4623B bus decoder for LPDDR, LPDDR2, LPDDR3 or LPDDR4 validation provide complete protocol decode of memory transactions using a Keysight logic analyzer as the analysis execution engine. The B4621B protocol-decode software translates acquired signals into easily understood bus transactions, with associated data bursts.

The B4623B bus decoder for LPDDR, LPDDR2, LPDDR3 or LPDDR4 validation provides complete protocol decode of memory transactions using a Keysight logic analyzer as the analysis execution engine. The B4623B protocol-decode software translates acquired signals into easily understood bus transactions with associated data bursts, at the full bus speed.

For additional analysis software, refer to www.keysight.com/find/logic-sw-apps

Technical Specifications and Characteristics

All specifications refer to the combination of a U4154B Logic Analyzer Module, U4201A logic analyzer probe cable, and any Keysight Soft Touch probe.

State (Synchronous) sampling mode	
Maximum state data rate Option 2.5 GHz state mode (spec)	2.5 Gb/s on 136 channels per U4154B, using either or both edges of clock (spec)
	4 Gb/s on 68 channels per U4154B, clocking on either edge of the clock (typ)
Maximum state data rate standard -01G 1.4 GHz state mode (spec)	1.4 Gb/s on 136 channels per U4154B, using either or both edges of clock (spec)
	2.8 Gb/s on 68 channels per U4154B, clocking on either edge of the clock (typ)
Maximum state clock frequency (typ)	2.5 GHz Option -02G
	1.4 GHz standard
Minimum state clock frequency[1] (typ)	12.5 MHz (single edge)
	6.25 MHz (both edges)
Sample position adjustment resolution (typ)	5 ps or 20 ps Option -02G
	20 ps standard
Sample position adjustment accuracy (typ)	± 150 ps
Minimum data valid window (typ)	100 ps Option -02G
	160 ps standard -01G
Minimum setup time (typ)	50 ps
Minimum hold time (typ)	50 ps
Minimum eye height (typ)	100 mV Option -02G
	160 mV standard
Sample position adjustment range (typ)	7 ns
Minimum state clock pulse width (typ)	200 ps
Number of clocks (nom)	1
Minimum time between active clock edges (typ)	400 ps
Maximum time between active clock edges 1 (typ)	80 ns
Number of clock qualifiers	4 (pods 2, 3, 4 and 5 on clocking module)
Clock qualifier setup time	150 ps
Clock qualifier hold time	150 ps
Number of “RESET” clock qualifiers	1 (pod 7 of clocking module)
“RESET” clock qualifier setup time	2 ns
“RESET” clock qualifier hold time	0 ps
Time tag resolution (typ)	80 ps
Maximum time count between stored states (typ)	66 days

1. Clock can pause for up to 66 days once every 8 or more edges.

Technical Specifications and Characteristics (continued)

Timing (Asynchronous) sampling mode		
	Half-channel mode	Full-channel Mode
Maximum sample rate (nom)	5 GHz	2.5 GHz
Minimum sample period (nom)	200 ps	400 ps
Pod usage (nom) 1 pod from each	1 pod from each odd/even pod pair, user selectable	All pods
Timing Zoom sampling rate (nom)	12.5 GHz	
Timing Zoom memory depth (nom)	256 K samples	
Maximum time between transitions (nom)	66 days	
Minimum data pulse width (typ)	1 sample period + 200 ps	
Time interval accuracy (typ)	± (1 sample period + 400 ps + 0.01% of time interval reading)	
Trigger characteristics		
Maximum trigger sequence speed (typ)	2500 MHz (400 ps) Option -02G	
	1400 MHz (714 ps) Option -01G	
Trigger resources (nom)	16 patterns evaluated as =, ! =, >, > =, <, < =	
	8 double-bounded ranges evaluated as in range, not in range	
	4 to 8 burst detectors	
	4 edge detectors in timing, 3 in transitional timing	
	1 occurrence counter persequence level	
	1 timer	
	3 flags	
	1 arm in	
Trigger resource Boolean conditions (nom)	Arbitrary Boolean combinations	
Trigger actions (nom)	Goto	
	Trigger and fill memory	
	Trigger and Goto	
	Trigger, send e-mail, and fill memory	
Store qualification actions (nom)	Default (global) and per sequence level	
	Store/don't store sample	
	Turn on/off default storing	
Timer actions	Start from reset	
	Stop and reset	
	Pause	
	Resume	
Flag actions	Set	
	Clear	
	Pulse set	
	Pulse clear	

Technical Specifications and Characteristics (continued)

Trigger characteristics (continued)	
Maximum trigger sequence levels (nom)	8
Trigger sequence level branching (nom)	Arbitrary 4-way if/then/else
Trigger position (nom)	Start, center, end, or user-defined
Maximum occurrence counter (nom)	999,999,999
Maximum pattern width (nom)	128 bits – single label
	408 bits – AND of multiple labels across three-card set
Maximum range width (nom)	64 bits
Timer range (nom)	100 ns to 27 hours (in timing modes)
	200 * state clock period to 27 hours (in state mode)
Timer resolution (nom)	5 ns
Timer accuracy (typ)	± (5 ns +0.01%) (in timing modes)
	± (8 * state clock period +2 ns +0.01%) (in state mode)
Timer reset latency (nom)	40 ns (in timing modes)
	80 * state clock period (in state mode)
General	
Number of channels (nom)	136 in one U4154B
	272 in two U4154Bs combined
	408 with three U4154B combined
Maximum channels on a single time base and trigger (nom)	408
Number of analyzers (nom)	1
Input signal amplitude V_{amptd} (typ)	⇒ 350 mV
Supported signal types	Single-ended and differential
Voltage threshold (typ)	–5 V to +5 V
Minimum threshold resolution (typ)	2 mV Option -02G
	20 mV standard
Threshold accuracy (typ)	± (30 mV + 1% of setting)
Threshold setting granularity	By channel

Technical Specifications and Characteristics (continued)

Environmental and physical

Operating environment	
Temperature (nom)	0 deg C to +40 °C
Humidity (nom)	0 to 80% relative humidity at 40 °C
Altitude	0 to 3000 m
Vibration	Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 0.2 g rms
Non-operating environment	
Temperature (nom)	–40 °C to +75 °C
Humidity (nom)	0 to 90% relative humidity at 65 °C
Altitude	0 to 15,300 m
Vibration (in shipping carton)	Random vibration 5 to 500 Hz
	10 minutes per axis
	Approximately 2.41 grms
	Swept sine resonant search
	5 to 500 Hz
	0.50 g (0-peak)
	5 minute resonant dwell at 4 resonances per axis
Weight	
Weight	2.34 kg

Definitions for Specifications

Specification (spec): Represents warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0 to 40 °C, unless otherwise stated, and after a 45 minute warm-up period. The specifications include measurement uncertainty. Data represented in this document are specifications unless otherwise noted.

Typical (typ): Represents characteristic performance, which 80% of the instruments manufactured will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 25 °C).

Nominal (nom): The expected mean or average performance, or an attribute whose performance is by design, such as the 50 Ω connector. This data is not warranted and is measured at room temperature (approximately 25 °C).

Measured (meas): An attribute measured during the design phase for purposes of communicating expected performance, such as amplitude drift vs. time. This data is not warranted and is measured at room temperature (approximately 25 °C).

Configuration

Recommended configuration for DDR2/3 or DDR4 < 2.5 Gb/s analysis		
Model	Quantity	Description
U4154B	2 [1]	Logic Analyzer, 136-channel , 12.5 GHz timing zoom, 2 Mb depth
Option 02G		2.5 GHz state, 2 Mb depth
M9502A or M9505A	1	AXIe 2 or 5 slot chassis. (To determine correct chassis, consider number of modules and if using embedded controller)
U4201A	8	Logic analyzer probe cable
M9536A*	1	AXIe Embedded Controller or M9045B or M9048A PCI Express adaptors
M9045B or M9048A	1	PCIe ExpressCard Adaptor for laptops; PCIe Desktop Adaptor
Y1200B or Y1202A	1	PCIe cable: x1 to x8, 2.0 m for use with M9045B; PCIe cable: x8, 2.0 m for use with M9048A [1]
Probes		As required, refer to ordering information

1. Only 1 U4154B module required for solutions requiring up to 5 pods for DDR2/3/4 or 4 pods for LPDDR/2/3/4. For DDR4 > 2.5 Gb/s used with a DDR4 DIMM interposer, three U4154B modules are required.

Note: M9536A controller, if used, must be installed in slot 1.

Related products	
Model	Description
U4301A	PCIe Analyzer
FS2510	FuturePlus DDR4 DIMM Interposer
FS2512	FuturePlus DDR4 SODIMM Interposer

Ordering

Model	Description
Option 02G	Increase max state speed to 2.5 Gb/s / 4 Gb/s
U4154B Option 02G	Base logic analyzer module 2 Mb, state speed 1.4 Gb/s / 2.8 Gb/s
Option 002	2 M sample memory depth (standard)
Option 004	4 M sample memory depth
Option 008	8 M sample memory depth
Option 016	16 M sample memory depth
Option 032	32 M sample memory depth
Option 064	64 M sample memory depth
Option 128	128 M sample memory depth
Option 200	200 M sample memory depth
M9502A	AXIe 2-slot chassis
M9505A	AXIe 5-slot chassis
U4201Ah	Logic Analyzer Cable For Use With E-Series Probes
Y1223A	Multiframe cable
M9536A	AXIe Embedded PC Controller
M9536A-M16	Memory upgrade from 8 GB RAM to 16 GB RAM
M9536A-W76	Windows 7 operating system (64 bit)
Probes	
W3631A	W3631A DDR3 x16 BGA Command and Data Probe for Logic Analyzer and Scope
W3633A	W3633A DDR3 x4/x8 BGA Command and Data Probe for Logic Analyzer and Scope
E5847A	46-ch Single-ended ZIF probe for DDR3 x4/x8 DRAM BGA probe connection to 90-pin logic analyzer cable
E5845A	46-ch Single-ended ZIF probe for DDR3 x16 DRAM BGA probe connection to 90-pin logic analyzer cable
E5406A	Pro Series Soft Touch Connectorless Probe - Single-ended, for 90-pin cable (34 channels)
E5405A	Pro Series Soft Touch Connectorless Probe - Differential, for 90-pin cable (17 channels)
E5402A	Low Profile, Pro Series Soft Touch Connectorless Probe - Single-ended, for 90-pin cable
E5390A	Soft Touch Connectorless Probe-Singleended, with 90-pin cable connectors
E5398A	Half-Size Soft Touch Connectorless Probe with 90-pin cable connectors
E5387A	Soft Touch Connectorless Probe-Differential, with 90-pin cable connectors
E5381B	Differential Flying Leads, 17 channels
E5382B	Single-ended Flying Leads, 17 channels
E5378A	Samtec Probe-Single-ended, with 90-pin cable connectors
E5379A	Samtec Probe-Differential, with 90-pin cable connectors
E5380A	Mictor Probe-Single-ended, with 90-pin cable connectors
FuturePlus FS2352B	DDR3 2133 DIMM interposer
FuturePlus FS2354	DDR3 1600 SODIMM interposer
FuturePlus FS2510	DDR4 2500 DIMM interposer (optional FS1070 conversion kit for FS2510 for data rates over 2.5 Gb/s)
FuturePlus FS2512	DDR4 1867 SODIMM interposer
W4633A	DDR4 x4/x8 BGA ADD/CMD/DATA interposer for U4154B logic analyzers
W2631B	DDR2 x16 BGA ADD/CMD/DATA probe for logic analyzers and scopes
W2633B	DDR2 x4/x8 BGA ADD/CMD/DATA probe for logic analyzers and scopes

Ordering (continued)

Model	Description
DDR analysis software	
B4621B	Bus Decoder for DDR2, DDR3, or DDR4 Validation
B4622B	DDR2/3/4 or LPDDR/2/3 Protocol Compliance Toolset
B4623B	Bus Decoder for LPDDR, LPDDR2, or LPDDR3 Validation
Other software	
B4601C	Serial-to-parallel analysis package
B4602A	Signal Extractor Tool
B4655A	FPGA dynamic probe for Xilinx
B4656A	FPGA dynamic probe for Altera
Upgrades	
U4154BU option 004	Upgrade memory to 4 M
U4154BU option 008	Upgrade memory to 8 M
U4154BU option 016	Upgrade memory to 16 M
U4154BU option 032	Upgrade memory to 32 M
U4154BU option 064	Upgrade memory to 64 M
U4154BU option 128	Upgrade memory to 128 M
U4154BU option 200	Upgrade memory to 200 M
U4154BU option 02G	Upgrade max state speed to 2.5 Gb/s / 4 Gb/s

Warranty and Calibration

Advantage services: calibration and warranty

Keysight Advantage Services is committed to your success throughout your equipment's lifetime.

Calibration	Description
Select Keysight calibration plan	
R1282A R-50C-011-3	3-year calibration assurance plan (return to Keysight): Priority calibration service covering all calibration costs for 3 years; 15% cheaper than buying stand-alone calibrations.
R1282A R-50C-011-5	5-year calibration assurance plan (return to Keysight): Priority calibration service covering all calibration costs for 5 years; 20% cheaper than buying stand-alone calibrations.
R1282A R-50C-021-3	ANSI Z540-1-1994 calibration – 3 years
R1282A R-50C-021-5	ANSI Z540-1-1994 calibration – 5 years
Warranty	**Description**
Select coverage	
R1280A Included	3-year warranty (return to Keysight), standard
R1280A R-51B-001-5Z	5-year warranty assurance plan (return to Keysight): Priority warranty service includes one-time coverage for an EOS/ESD failure.

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