Keysight Technologies

Precise Evaluation of Input, Output, and Reverse Transfer Capacitances of Power Devices

White Paper

KEYSIGHT TECHNOLOGIES

Increasing Importance of Capacitance Measurement

The switching frequency in power conversion circuits is increasing. This is primarily to reduce the size of passive components such as smoothing capacitors and reactors. Accurate characterization of device parameters affecting switching performance become more important as higher switching frequencies increase power circuit switching losses. Let's use the power MOSFET shown in Figure 1 as an example.

Gate resistance (Rg), input, output and reverse transfer capacitances (Ciss, Coss and Crss) are described in a device datasheet as typical parameters related to switching performance.

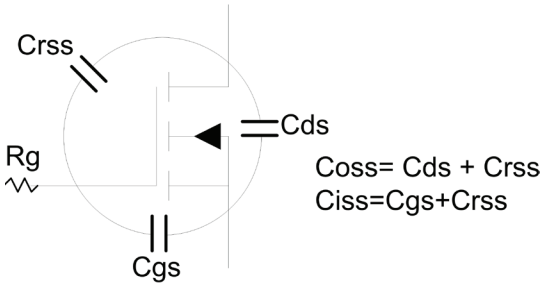

Figure 1. Three Capacitances of Power MOS FET

Rg and Crss dictate switching speed while Ciss determines driving condition. Power loss due to charging and discharging Coss is the primary component of switching loss in the case of a resonant converter. Crss and Coss have voltage dependency in the nano-farad range due to the power device's depletion region modulating with applied varying operational voltages.

These capacitances are conventionally measured by LCR meter. However, the maximum voltage of an integrated LCR voltage source is limited to around ±40 V. Therefore, most device data sheets do not include capacitance measurement data with more than ±40 V bias.

Circuit designers traditionally use curve fitting capacitance characteristics in their design work for voltages greater than 40 V. However, curve fitting is no longer viable due to complicated device structures based upon trench or super junction structures. In addition, complicated manufacturing processes induce additional variation in device performance. e.g. capacitance gap between high side FET and low side FET. Performance difference identification is key to device selection and failure analysis. Accordingly, for these reasons, device capacitance characterization from actual chip and module level measurements becomes essential.

Application notes provided by device manufacturers describe the power device capacitance measurement method. However, it is not a simple measurement. Many factors such as the determination of good peripheral circuit constants, measurement circuit compensation and appropriate measurement frequency have to be considered. This article discusses power device measurement methods and practical tips.

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Basic Device Capacitance Measurement

Capacitance measurement on a three terminal device such as IGBT or MOSFET requires AC guarding plus peripheral circuits and an external bias source. Basic measurement set ups for a power MOSFET are discussed in this chapter.

Coss measurement

Figure 2 shows the measurement circuit for output capacitance (Coss = Crss + Cds) of a MOSFET. High and low ports of the LCR meter are connected to the device after shorting the gate and the source terminals. The device impedance is calculated from applied voltage, Vm, and measured current, Im. Coss voltage dependency, (+/-40 V) is measured by the integrated LCR meter voltage source.

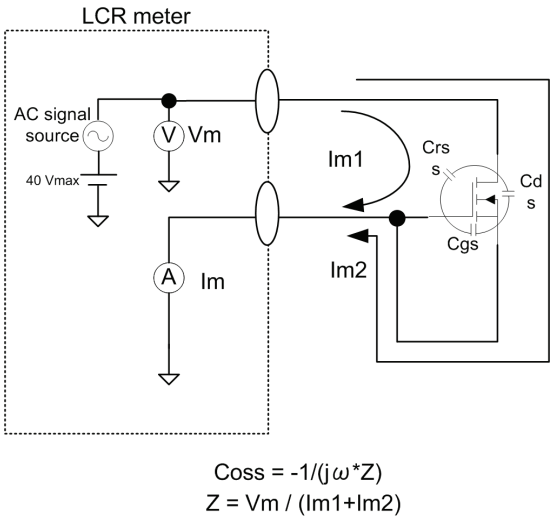


Figure 2. Coss measurement by LCR meter

Crss measurement

Figure 3 shows the measurement circuit for reverse transfer capacitance (Crss) of a MOSFET. High and low ports of the LCR meter are connected to gate and drain terminals. The AC guard terminal of the LCR meter is connected to the source terminal. The AC guard directs current flowing through Cds directly to LCR meter circuit common without going through the current meter.

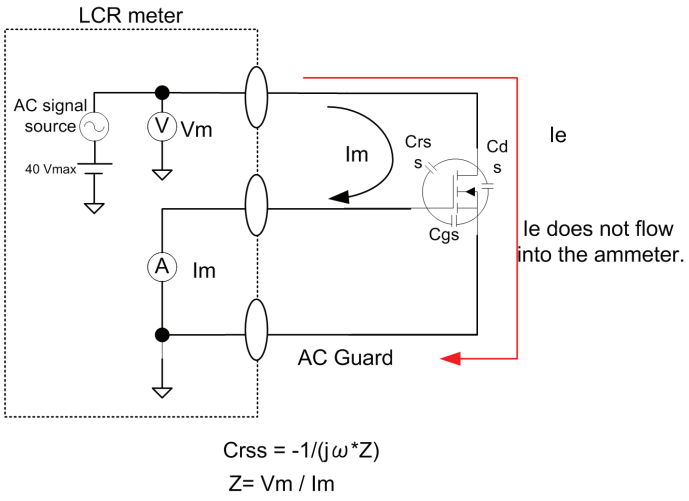
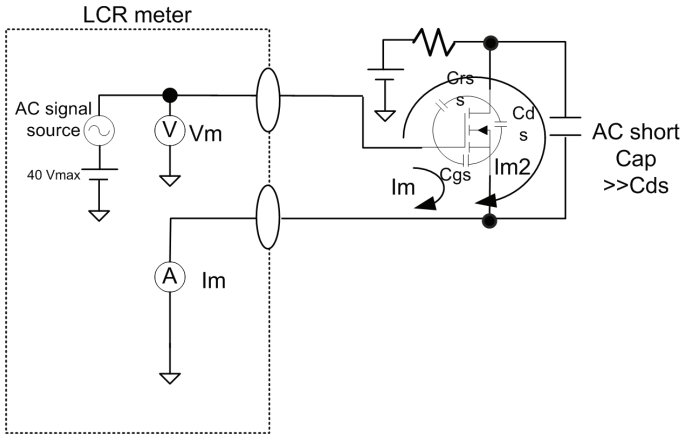


Figure 3. Crss measurement by LCR meter

Ciss measurement

Figure 4 shows the measurement circuit for input capacitance (Ciss) of a MOSFET. High and low ports of the LCR meter are connected to gate and source terminals. An external power supply is necessary to bias the drain terminal. A resistor or an inductor is necessary between the power supply and the drain in order to block the measurement AC signal flowing into the power supply. In addition, a large capacitor is necessary between drain and source terminals in order to short the AC measurement signal and to block the DC bias being applied to the drain terminal. The measurement signals flowing through Cgs and Crss are measured by the LCR current meter.



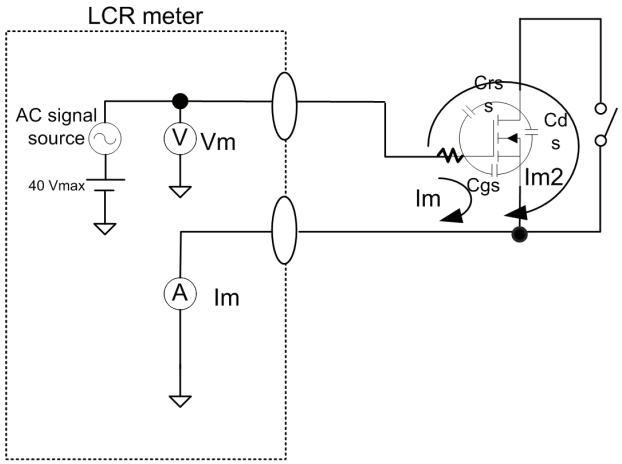
$Ciss = -1/(j\omega * Z)$

$Z = Vm / (Im1+Im2)$

Figure 4. Ciss measurement by LCR meter

Rg measurement

Figure 5 shows the measurement circuit for gate resistance (Rg) of a MOSFET. High and low ports of LCR meter are connected to gate and source terminals. Drain and source terminals can be shorted together. Occasionally, Rg is defined with the drain terminal open, as shown in Figure 5. The LCR meter is set to Rs-Cs mode and Rg is obtained from the measured input voltage (Vm) and output current (Im). The measurement frequency should be set to high in order to minimize the influence of Ciss. Gate voltage dependency of Ciss can be measured simultaneously with Rg by shorting drain and source terminals.



$Rg = Re(Z)$

$Z = Vm / (Im1+Im2)$

Figure 5. Rg/Ciss measurement by LCR meter

As discussed above the device connection and measurement circuitry wiring has to be changed for each different capacitance in three terminal device capacitance measurements.

Challenges in High Voltage Device Capacitance Measurement

High voltage bias tee

For capacitance measurements on high voltage power devices an external high voltage DC source is necessary due to the inadequacy of the integrated +/-40 V LCR power supply.

A resistor or an inductor is necessary at the output of the external DC source to avoid leakage of the measurement AC signal. In addition, a blocking capacitor is mandatory to superimpose the measurement AC signal on the voltage bias source. A large capacitor is ideal to minimize measurement AC signal attenuation at the DUT terminal. However, too large a capacitor slows down measurement speed. Typically the appropriate blocking capacitor size is around ten times larger than the largest DUT capacitance. The capacitor type should be thin film as it has less voltage dependency. Figures 6, 7 and 8 are capacitance measurement circuits for high voltage devices and correspond to Figures 2, 3 and 4, respectively. A significant issue to consider is the risk of destroying measurement equipment due to the sudden inrush of voltage or current from the blocking capacitor when the DUT catastrophically fails. A protection circuit should be configured using a voltage clamp diode, a surge absorber and a resistor, (not shown in any of the figures). It is recommended that the breakdown voltage of the DUT is measured in advance of capacitance measurements and that capacitance bias voltage be well below the device breakdown voltage. Additionally, the measurement circuit has to be fully enclosed for safety reasons as the stored energy in the blocking capacitor is potentially fatal. Figure 9 shows hazardous energy range described in IEC60950-1 and IEC61010-1.

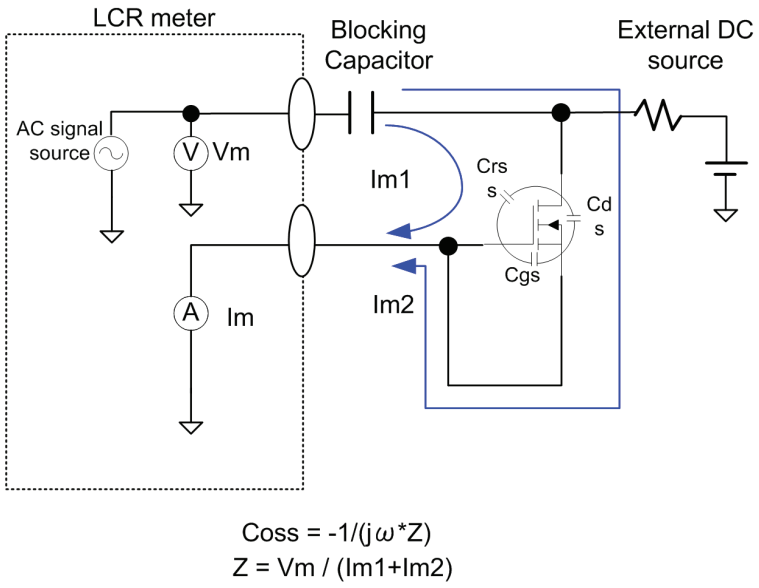


Figure 6. Coss measurement at High Voltage Bias

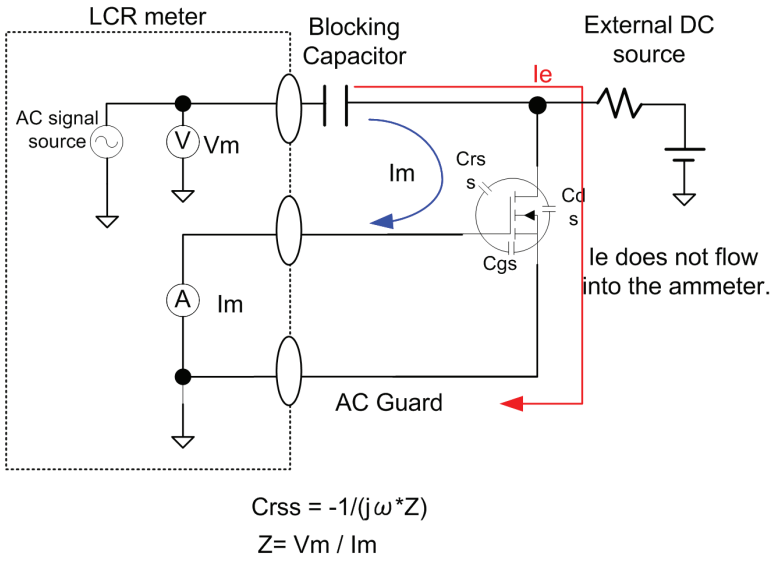


Figure 7. Crss measurement at High Voltage Bias

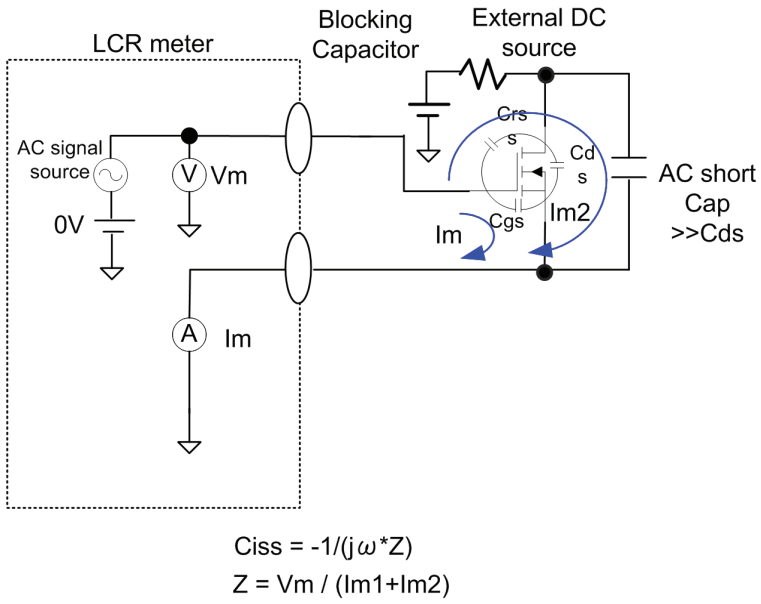


Figure 8. Ciss measurement at High Voltage Bias

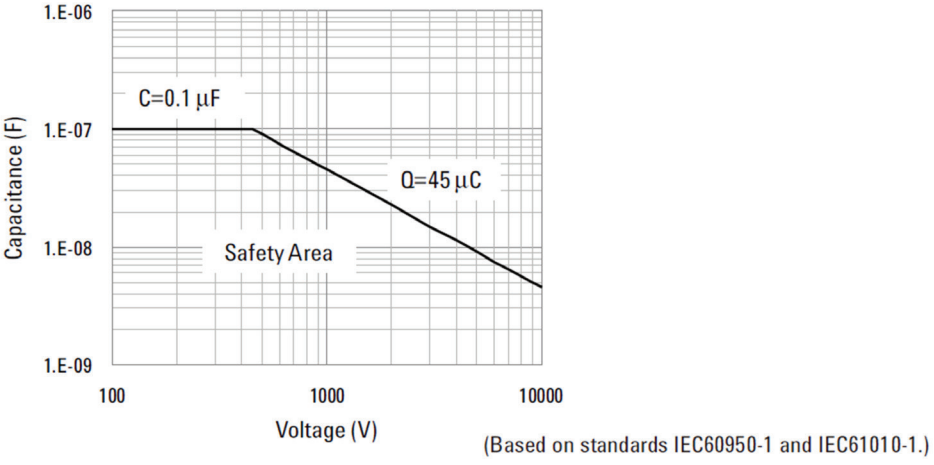


Figure 9. Capacitance Charge generally considered as safety

Normally on device

For depletion type devices, typically seen in GaN FET or SiC JFET, a negative voltage has to be applied to the gate terminal to turn off the device when making capacitance measurements. This measurement circuitry requires an additional blocking capacitor and an additional external DC source. Consequently it becomes complicated and troublesome to construct the test set up. Measurement circuitry examples are shown in Figures 10 and 11.

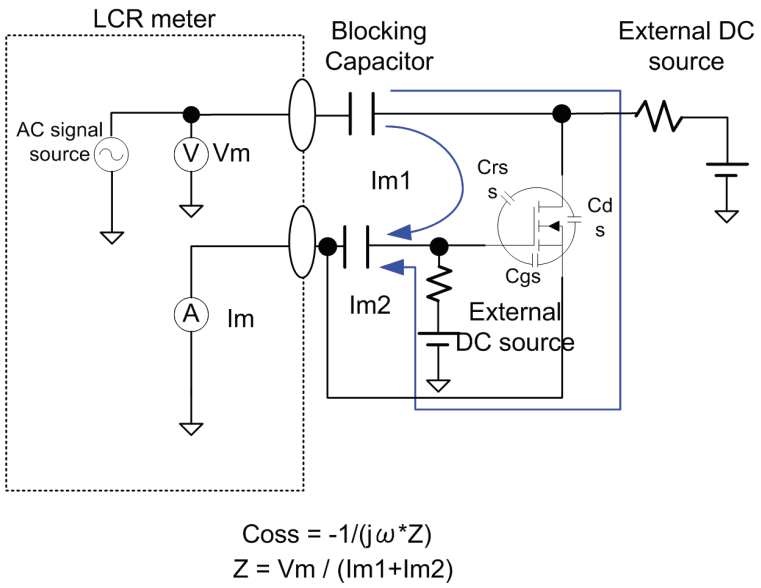


Figure 10. Coss measurement for normally on device at High Voltage Bias

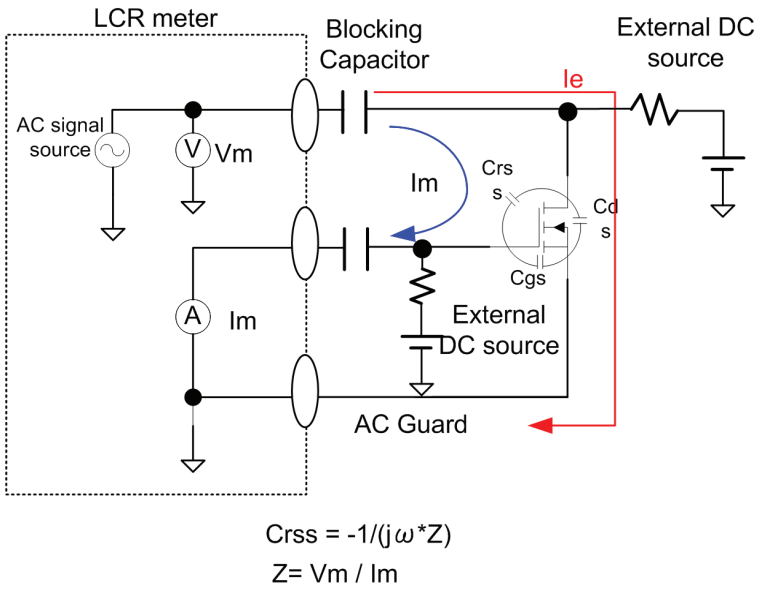


Figure 11. Crss measurement for normally on device at High Voltage Bias

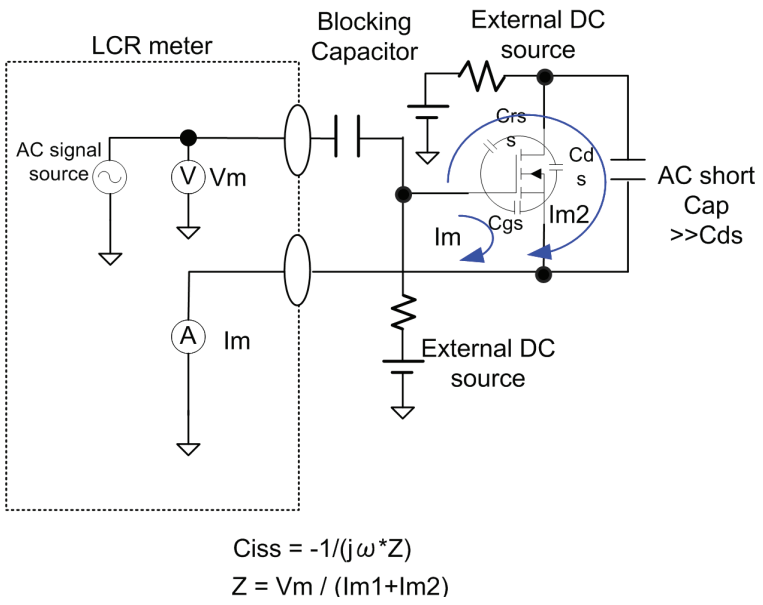


Figure 12. Ciss measurement for normally on device at High Voltage Bias

Power module

A power module, (e.g. 2-in-1 or 6-in-1) has multiple FETs inside. When measuring the capacitance of a FET in such a module the AC guard plays a key role in accurate measurements by nullifying the capacitance of other FETs. Figure 13 shows an example of AC guard connection when measuring Crss of high side FET 1 in the 6-in-1 module. Gate and source terminals of the other FETs are connected to the AC guard.

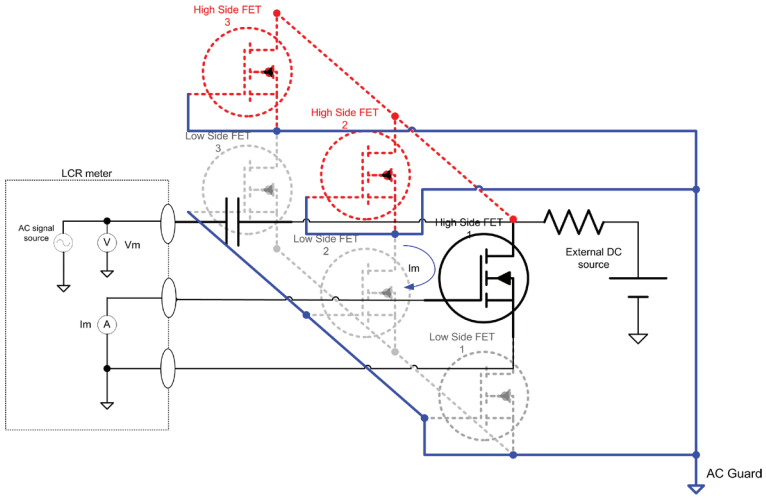


Figure 13. 6 in 1 Module, Crss measurement at High Voltage Bias

Compensation of test lead inductance

After constructing measurement circuitry utilizing the above techniques appropriate compensation should be performed.

The first is open compensation to cancel stray capacitance in the measurement path using the "open compensation" function within the LCR meter.

Secondly, short compensation should be performed in order to cancel out the residual inductance of the test leads. The "short compensation" function in an LCR meter is designed for a two terminal device and it needs to be extended for a three terminal device. Today it is rare practice to perform short compensation even although the influence of residual inductance is far from negligible. Figure 14 shows a circuit designed to compensate parasitic inductances in test circuitry. In this example the guard connection retains the residual parasitic inductance without correction. This, in turn, adds an additional potential error factor to power device capacitance measurements. If the capacitance of a power device is large the measurement error tends to be large when the measurement frequency is close to the resonant frequency. Resonant frequency is determined by the uncompensated residual inductance and device capacitance. E.g. the resonant frequency is 1.6 MHz for the combination of a 10 nF device capacitance and 1 m long test lead; (the equivalent residual inductance of a 1m wire connection lead is around 1 µH.) If the measurement frequency is set to 1 MHz, the error will be significant because it is close to the resonant frequency. For power device capacitance measurement at 1 MHz the residual inductance in the measurement circuitry has to be small. Alternatively, the measurement frequency has to be reduced (e.g. 100 kHz) in order to make an accurate measurement.

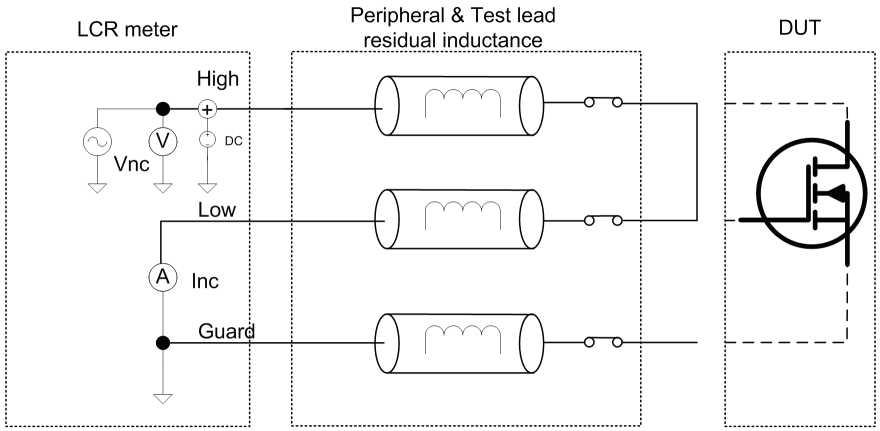


Figure 14. Short correction including Guard terminal is required for compensating residual inductance

When a large capacitance exists between the current meter and the AC guard, (e.g. Crss measurement) as shown in Figures 3, 7 and 11 phase compensation for the current meter feedback loop may be necessary. If an LCR meter shows an error status such as "bridge unbalanced" when making this measurement, (Crss) it usually means that phase compensation is required.

Practical use of C-V measurement data

In this chapter the influence of power device capacitances on switching circuit operation are discussed. Crss can be seen as a mirror capacitor in the switching circuit. Charging and discharging Crss determines the switching speed of the circuit. The curve integral of Crss vs. drain voltage is the cross switching charge (Qsw). Switching time can be calculated by dividing Qsw by gate drive current.

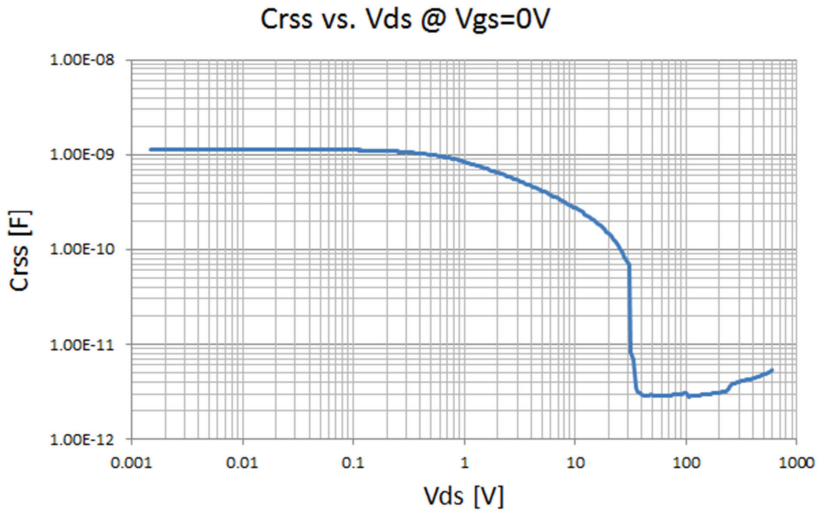


Figure 15. Crss residual dependency

$$Qsw = \int_0^{Vds-Vgs} Crss * dV\,ds \quad (1)$$

$$Tsw(on) = \frac{Qsw}{ig} \quad (2)$$

Power loss due to Coss is a component of switching loss. This loss is generated in any type of switching converter. In order to determine the loss it is necessary to calculate the total charge supplied to Coss during the switching period. Total charge is calculated by integrating Coss with respect to drain voltage from 0 V to device operating voltage. Dividing total charge by device operating voltage is called Equivalent Effective Output Capacitance of energy, (Coss_eff). The power loss caused by the effective output capacitance is calculated using the Coss_eff, device operation voltage and the switching frequency.

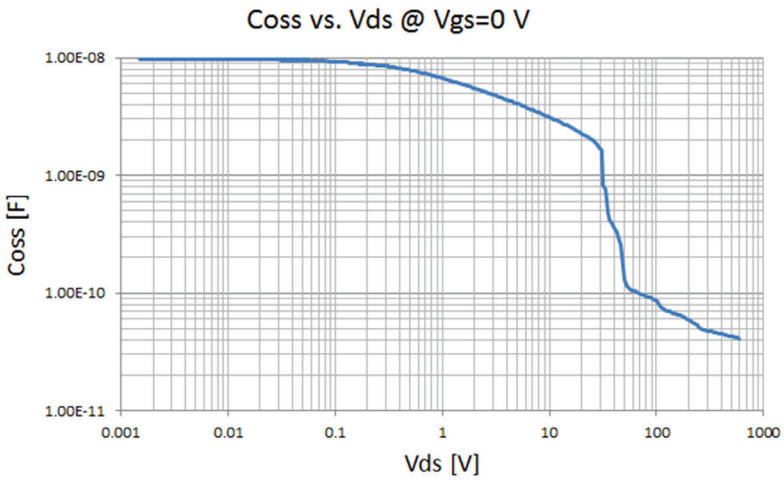


Figure 16. Coss voltage dependency

$$Coss\_eff = \frac{1}{Vds}\int_0^{Vds} Coss * dV\,ds \quad (3)$$

$$Powerloss\ by\ Coss_{eff} = \frac{1}{2} * Coss_{eff} * Vds^2 * freq. \quad (4)$$

Ciss is a key parameter for gate drive circuit design. Drain voltage dependence on Ciss at Vgs = 0 V is initiated by its component Crss. Measurement of the gate drive charge when the device is off is straightforward. However, measuring drive capacitance when the device is on or when sweeping gate voltage from negative to positive in order to avoid unexpected turn on due to Vgs dependency on Ciss is essential. Both can be evaluated using the measurement set up shown in Figure 5.

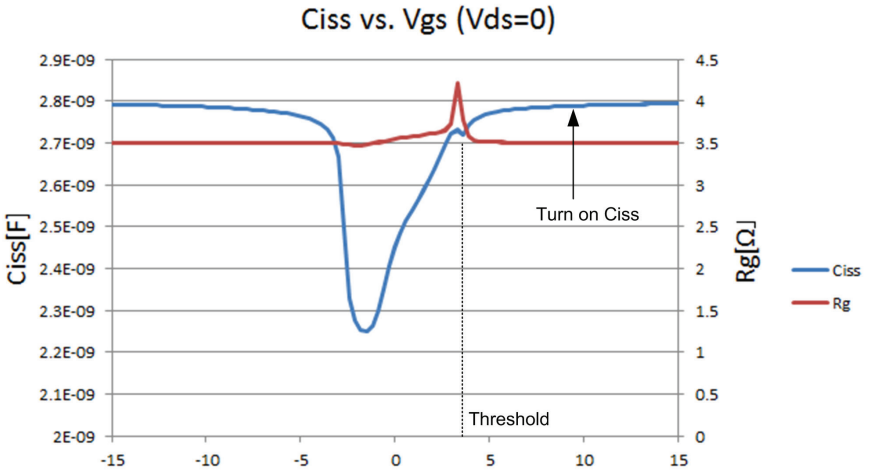


Figure 17. Ciss voltage dependency

Application of device capacitances within a circuit simulator

Accurate simulation and verification of switching operation is possible by applying device capacitance measurement results as a non-linear model within a circuit simulator, e.g. SPICE. Cgs, Crss and Cds are all necessary for the simulation. These parameters can be measured by connecting the AC guard to the free terminal on a three terminal transistor. Alternatively, Cgs and Cds can be calculated from the Ciss, Coss and Crss measurement result as Ciss = Cgs + Crss and Coss = Cds + Crss.

Crss characteristics deployed in a simulator should show Vdg dependency not Vds dependency. Vdg = Vds – Vgs. Fig 15 shows Crss characteristics in depletion mode (Vdg > 0, in depletion). However, for a complete simulation it is not sufficient as the Crss characteristics in enhancement mode (Vdg < 0 or Vds < Vgs) are missing. When Vdg < 0 the device is turned on and Crss rapidly increases. The approximate capacitance at turn on can be found in the Ciss – Vgs curve. The relevant non-linear Crss characteristics to apply should be derived from Figure 19.

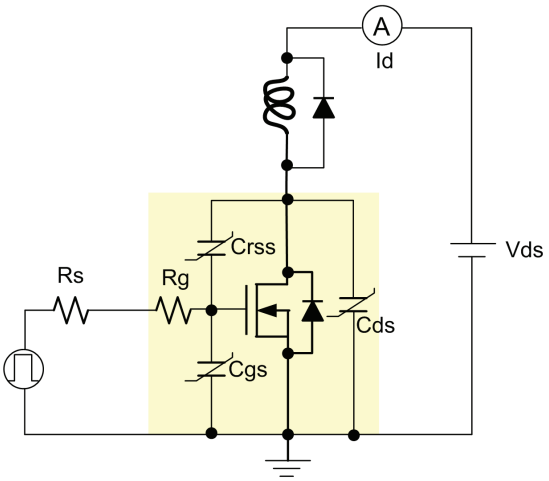


Figure 18. Apply device capacitance to Simmulator

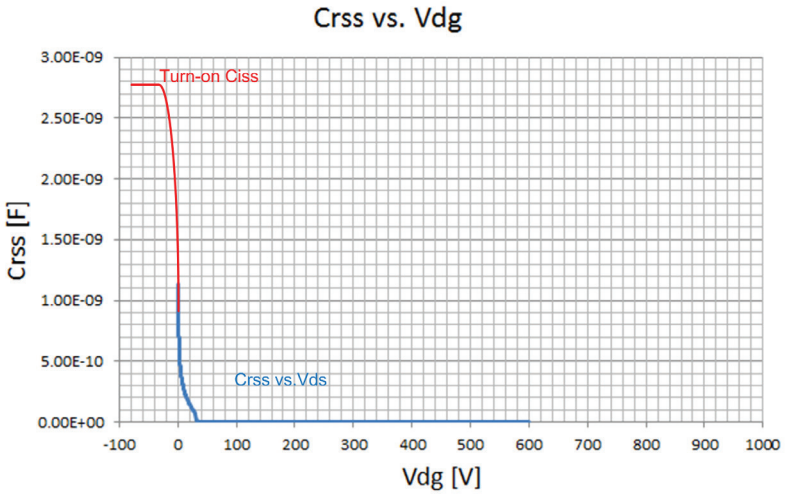


Figure 18. Crss Vdg dependency

Fully automated capacitance evaluation utilizing the Keysight B1507A switching characterization solution

Keysight Technologies has developed a power device capacitance analyzer which can automatically measure all power device junction capacitances and gate resistances without the need to reconfigure or re-cable the device under evaluation. This includes normally-on and normally-off devices with all the appropriate connections being made by a special selector for power device capacitance test. (Figure 20).

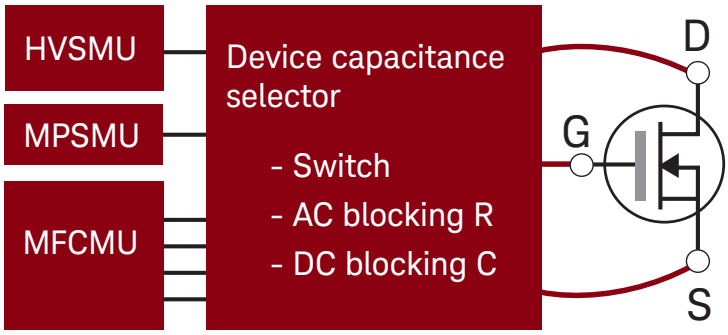
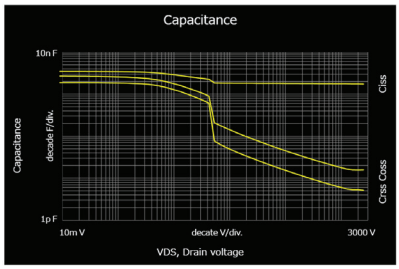


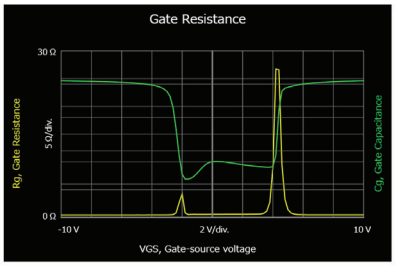
Figure 20. Keysight B1507A Hardware Block Diagram

Fully automating the solution eliminates connection and settings error. In addition it includes capacitance open, short and phase compensation for all three terminal devices. It is literally insert device, click measure and view results.

Figure 21 shows (a) Power MOS FET capacitance measurement to 3kV drain bias and (b) Power MOS FET gate resistance measurement. It allows device designers to develop and optimize high performance power devices. Additionally, it enables power circuit designers to select optimum power devices and eliminate substandard and counterfeit components.



(a) Up to 3 kV biased Ciss, Coss and Crss



(b) Rg (yellow) vs. gate voltage

Figure 21. Measurement examples

Precise power MOSFET capacitance measurement brings about further benefit to power circuit designers. Although switching loss dominates in switch mode power supply applications switching characteristics measurement is never a trivial task. There are many factors that make direct evaluation of switching characteristics far more difficult than static measurements. The main bottlenecks are: bandwidth of the current probe, ringing in the switching waveform due to parasitic inductance in the measurement path, creation of an appropriate gate driving circuit etc. On the other hand, since the measurement reproducibility of power MOSFET capacitance and gate resistance is high you can use these data to enhance the accuracy of switching circuit simulation. In addition enhanced models with drain voltage dependency on Crss, gate voltage dependency on Ciss and gate resistance can be introduced which will significantly increase the overall accuracy of the circuit simulator.

Figure 22 shows example simulation results which correlate well with the datasheet figures. Switching characteristics utilizing specific operating conditions can be simulated accurately with this method.

Finally the Keysight B1506A, another power device analyzer, can also be used for characterizing power device capacitances. It is a superset of B1507A having not only the same capacitance measurement capabilities but also wider IV, thermal, and gate charge measurement abilities.

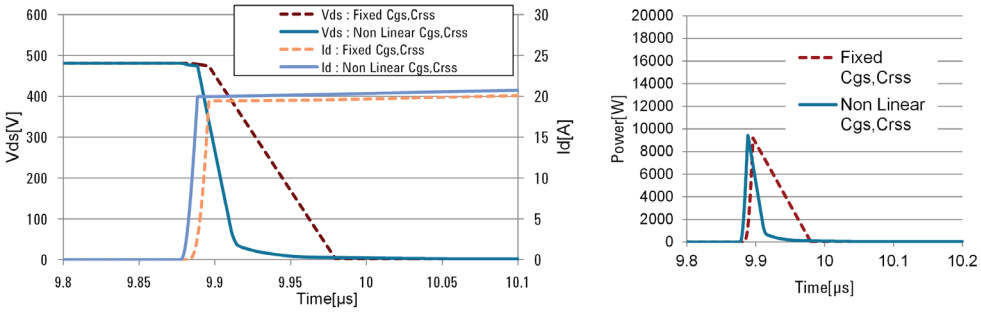


Figure 22. Simulated switching characteristics and power loss

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Published in USA, October 10, 2014
5992-0207EN
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