HP 8642A/B
SYNTHESIZED SIGNAL GENERATOR
(Including Options 001, 002 and 003)

Service Manual
Volume 2
SERIAL NUMBERS

This manual applies directly to modules with serial numbers prefixed:

2427A to 2816A and all *MAJOR* changes that apply to your instrument/modules.

rev.01NOV88

For additional important information about serial numbers, refer to "INSTRUMENTS COVERED BY THIS MANUAL" in Section 1.

Second Edition

EAST 24001 MISSION AVENUE, TAF C-34, SPOKANE, WASHINGTON, U.S.A. 99220

Service Manual HP Part 08642-90226

Other Documents Available:
Microfiche Operation and Calibration Manual HP Part 08642-90225
Operation and Calibration Manual HP Part 08642-90224
Microfiche Service Manual HP Part 08642-90227

Printed in U.S.A. : November 1988

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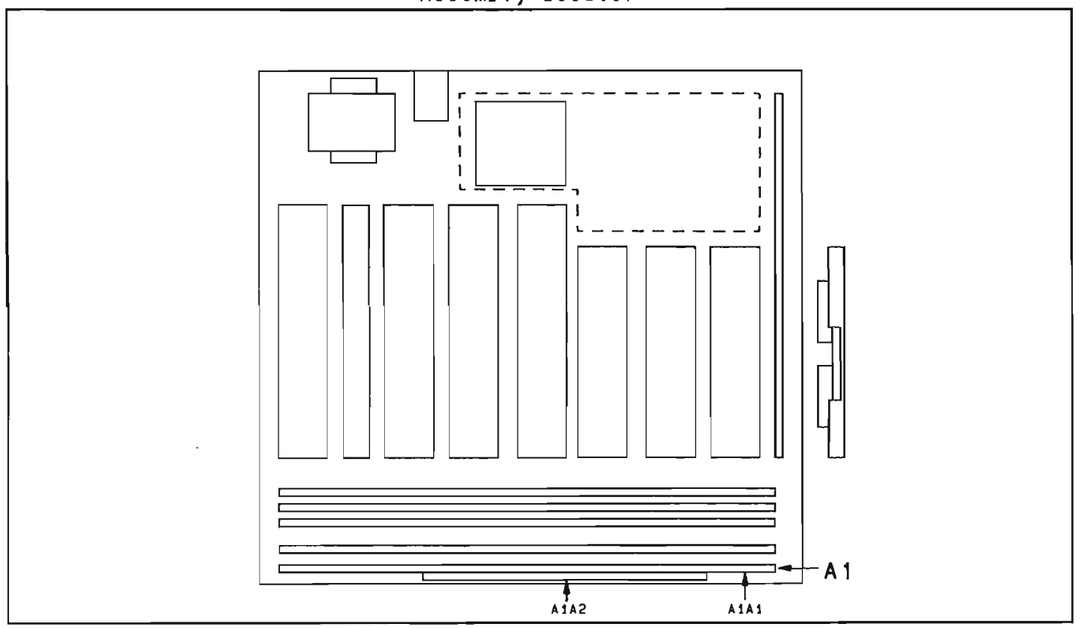
Assembly Locator



Simplified Block Diagram

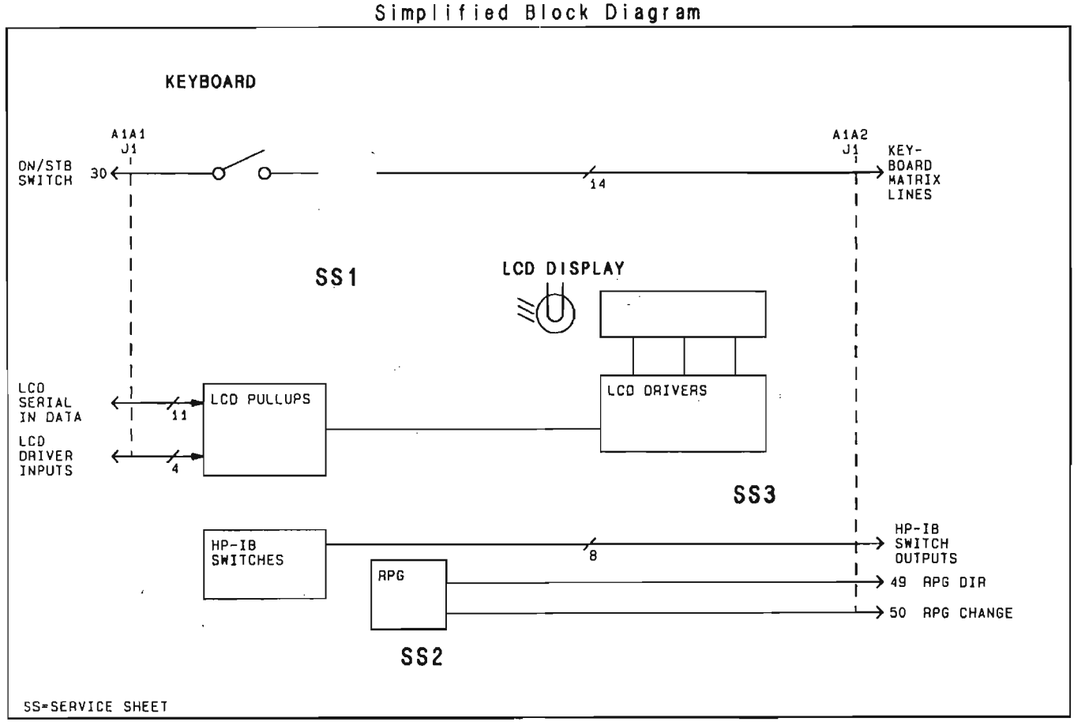
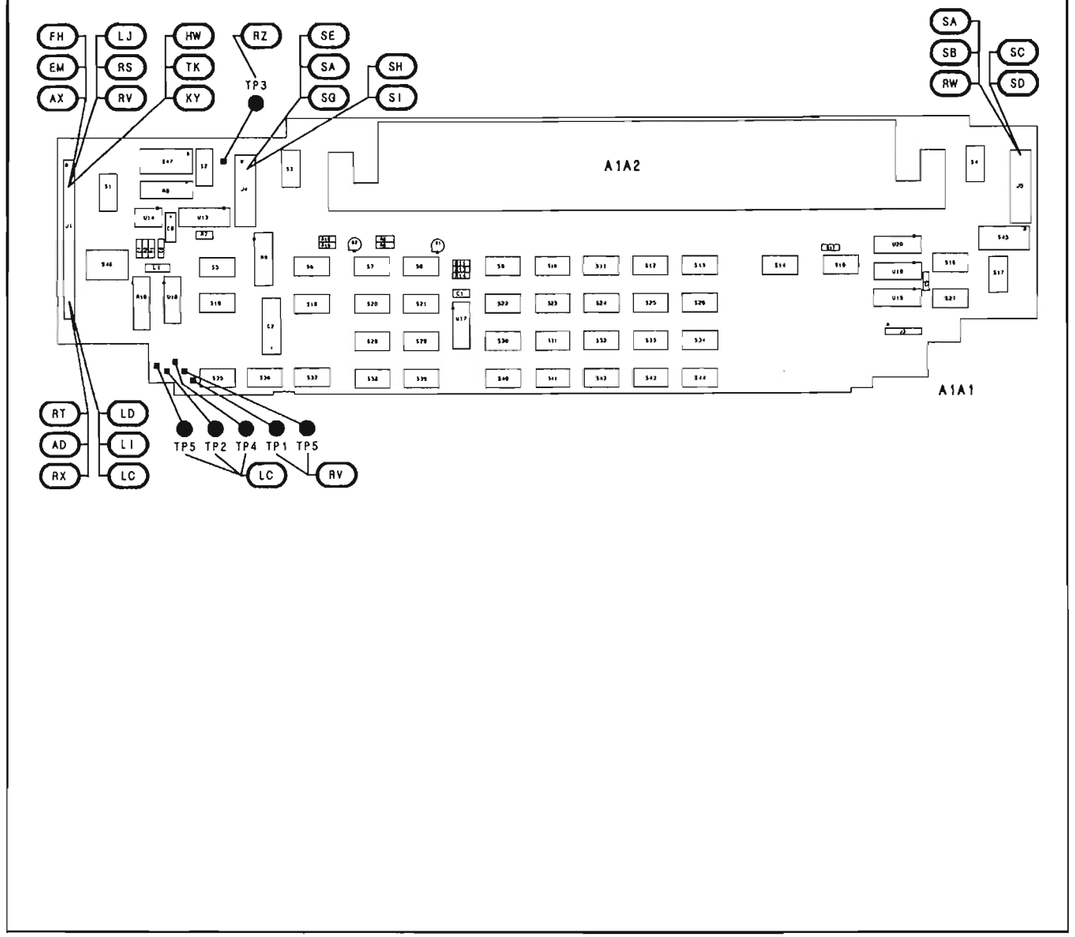
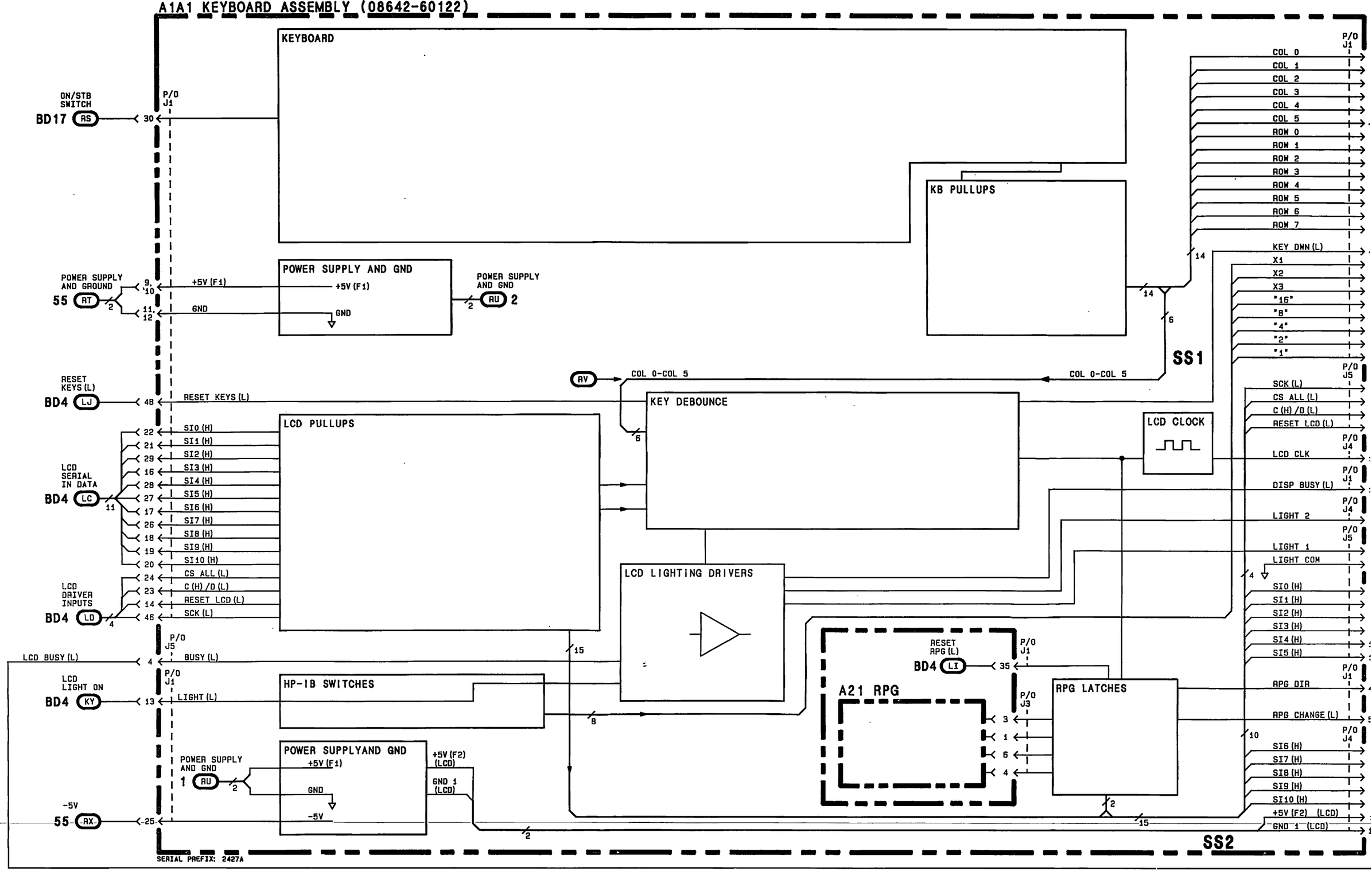


Figure 8E-100 BD2 General Information.

Module Test Point/Adjustment Locations



A1A1 KEYBOARD ASSEMBLY (08642-60122)



KB PULLUPS

COL 0-COL 5

SS1

P/O J1

COL 0
COL 1
COL 2
COL 3
COL 4
COL 5
ROW 0
ROW 1
ROW 2
ROW 3
ROW 4
ROW 5
ROW 6
ROW 7

KEYBOARD MATRIX LINES → AX BD4

KEY DWN (L) → IK BD4

X1
X2
X3
"16"
"8"
"4"
"2"
"1"

HP-IB SWITCH OUTPUTS → AD BD4

LCD CLOCK

P/O J5

SCK (L)
CS ALL (L)
C (H) /D (L)
RESET LCD (L)

SG SH SB SC RZ

P/O J4

LCD CLK

P/O J1

DISP BUSY (L) → FH BD4

P/O J4

LIGHT 2

LCD LIGHTING → SA

P/O J5

LIGHT 1
LIGHT COM

SI0 (H)
SI1 (H)
SI2 (H)
SI3 (H)
SI4 (H)
SI5 (H)

SI0-SI5 → SD

P/O J1

RPG DIR → EM BD4

RPG CHANGE (L) → HW BD3,4

P/O J4

SI6 (H)
SI7 (H)
SI8 (H)
SI9 (H)
SI10 (H)

SI6-SI10 → SE

+5V (F2) (LCD)
GND 1 (LCD)

SI → POWER SUPPLY AND GND

RESET RPG (L) BD4 LI

A21 RPG

P/O J3

RPG LATCHES

SS2

LCD BUSY (L)

A1A2 LCD DISPLAY ASSEMBLY (08642-60121)

P/O P2

LIGHT 2
LIGHT COM

LCD AND LIGHTS

SECTION A
SECTION C

P/O P1

LIGHT COM
LIGHT 1

P/O P2

SCK (L)
CS ALL (L)

P/O P1

C (H) /D (L)
RESET LCD (L)

P/O P2

LCD CLK

LCD DRIVERS

SECTION R (RIGHT) DRIVERS
SECTION C (CENT DRIVERS

P/O P1

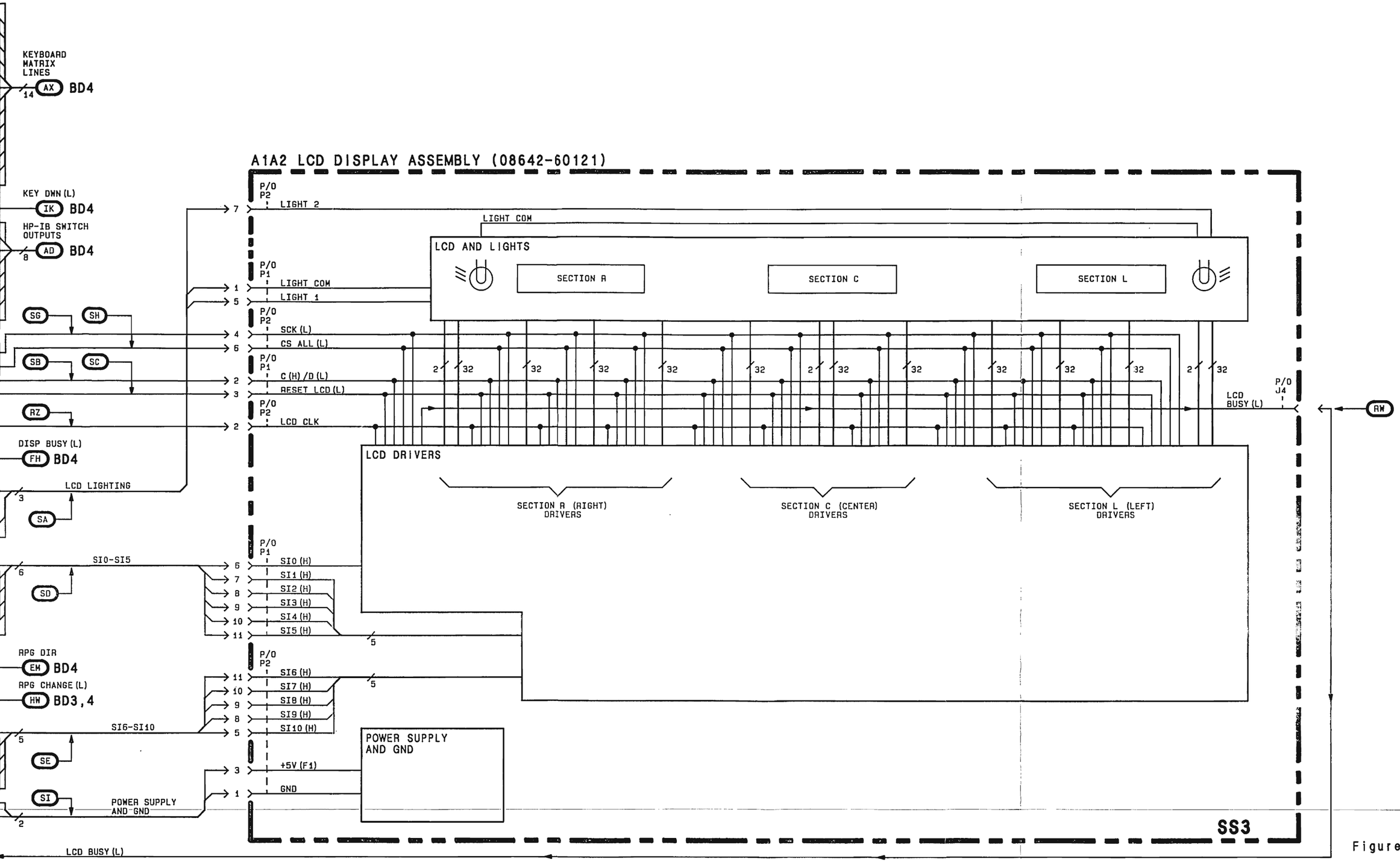
SI0 (H)
SI1 (H)
SI2 (H)
SI3 (H)
SI4 (H)
SI5 (H)

P/O P2

SI6 (H)
SI7 (H)
SI8 (H)
SI9 (H)
SI10 (H)

POWER SUPPLY AND GND

+5V (F1)
GND



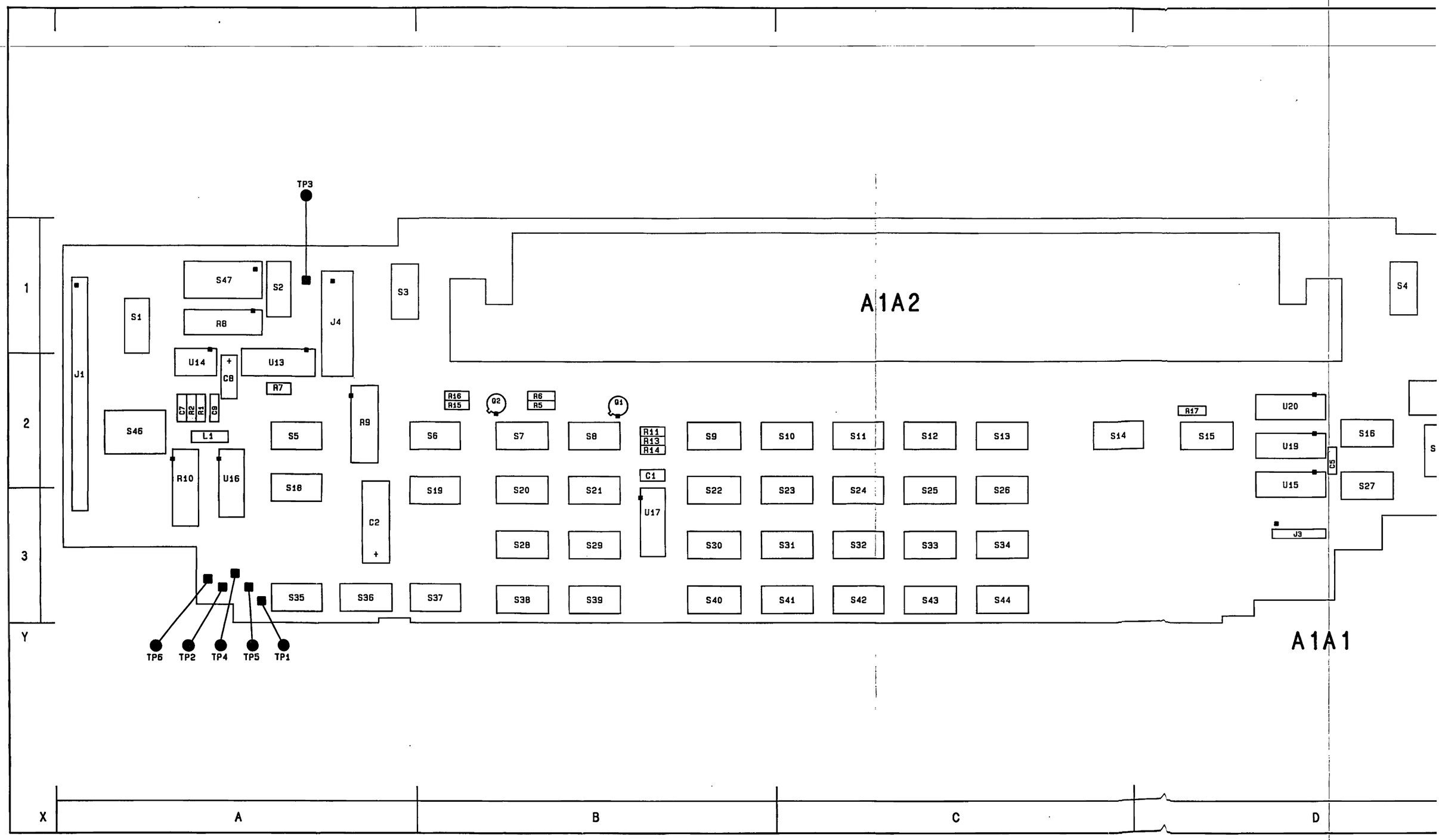
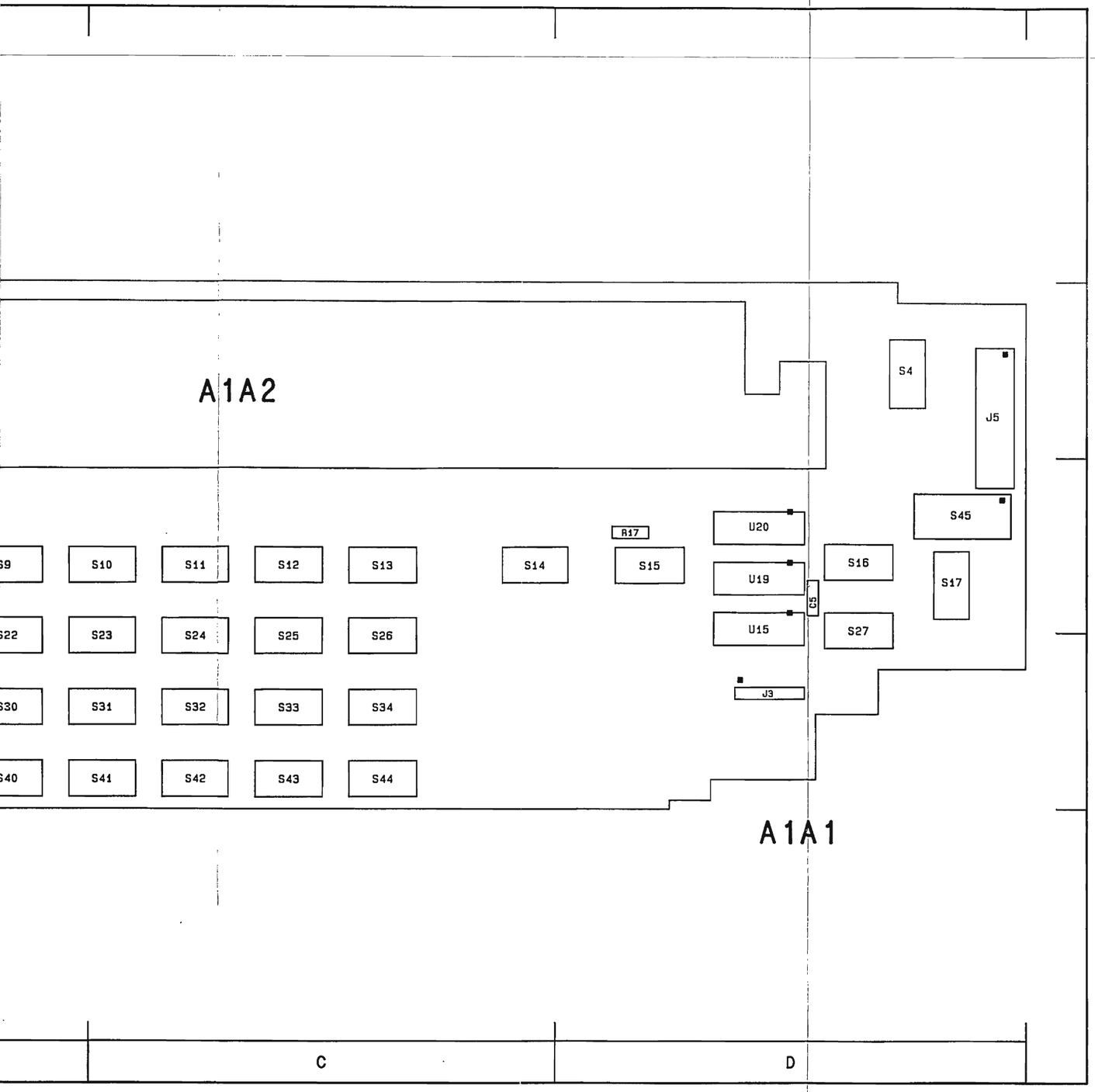
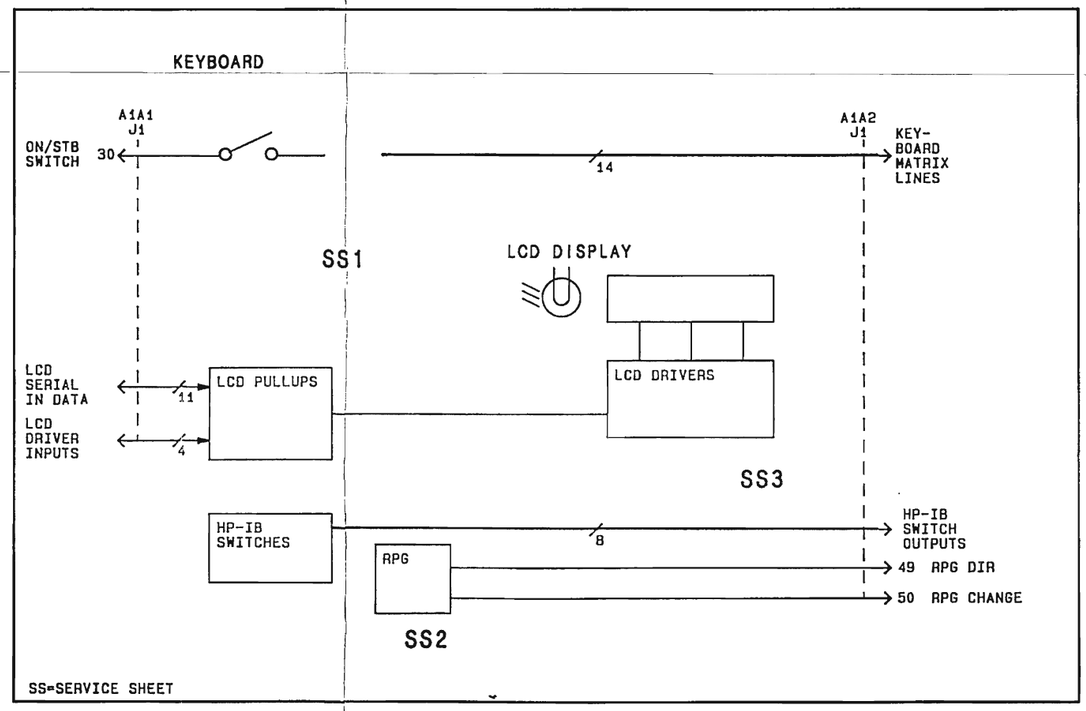


Figure 8E-102. SERVICE SHEET 1 INFORMATION

Component Locator



mponent Locator



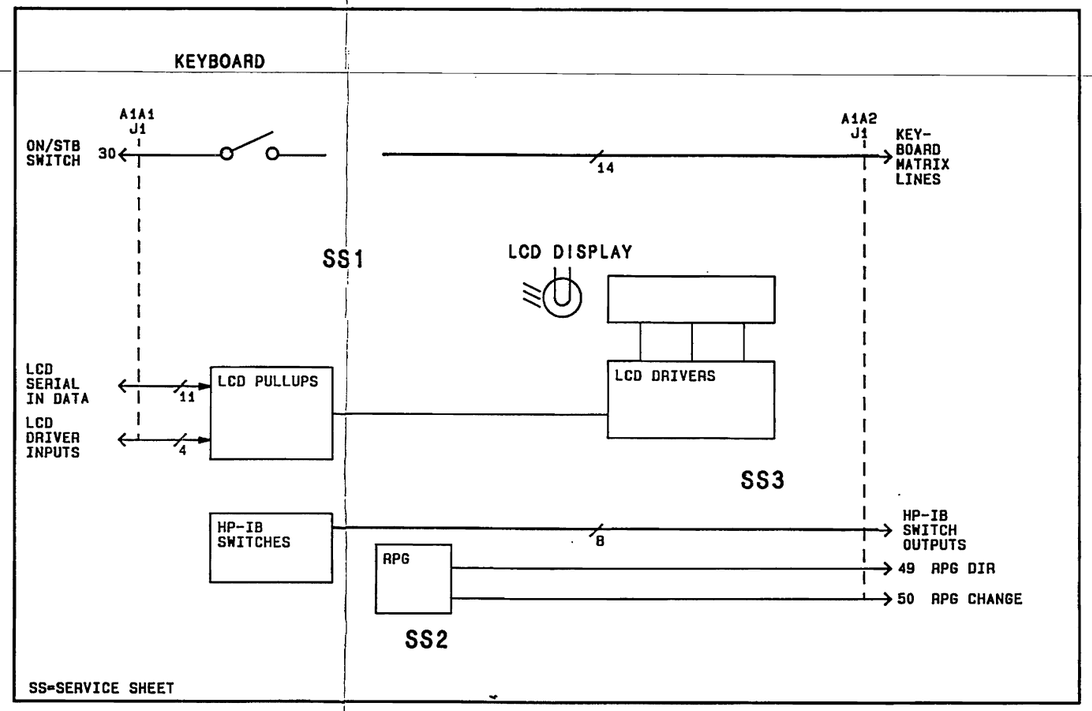
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
J1	A,2	S34	C,3														
		S35	A,3														
R10	A,2	S36	A,3														
		S37	B,3														
S1	A,1	S38	B,3														
S2	A,1	S39	B,3														
S3	A,1	S40	B,3														
S4	D,1	S41	C,3														
S5	A,2	S42	C,3														
S6	B,2	S43	C,3														
S7	B,2	S44	C,3														
S8	B,2	S46	A,2														
S9	B,2																
S10	C,2	TP1	A,3														
S11	C,2	TP5	A,3														
S12	C,2																
S13	C,2																
S14	C,2																
S15	D,2																
S16	D,2																
S17	D,2																
S18	A,2																
S19	B,3																
S20	B,3																
S21	B,3																
S22	B,3																
S23	C,3																
S24	C,3																
S25	C,3																
S26	C,3																
S27	D,2																
S28	B,3																
S29	B,3																
S30	B,3																
S31	C,3																
S32	C,3																
S33	C,3																

SEE REVERSE SIDE

A1 MODULE **BD2**



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
J1	A, 2	S34	C, 3														
		S35	A, 3														
R10	A, 2	S36	A, 3														
		S37	B, 3														
S1	A, 1	S38	B, 3														
S2	A, 1	S39	B, 3														
S3	A, 1	S40	B, 3														
S4	D, 1	S41	C, 3														
S5	A, 2	S42	C, 3														
S6	B, 2	S43	C, 3														
S7	B, 2	S44	C, 3														
S8	B, 2	S46	A, 2														
S9	B, 2																
S10	C, 2	TP1	A, 3														
S11	C, 2	TP5	A, 3														
S12	C, 2																
S13	C, 2																
S14	C, 2																
S15	D, 2																
S16	D, 2																
S17	D, 2																
S18	A, 2																
S19	B, 3																
S20	B, 3																
S21	B, 3																
S22	B, 3																
S23	C, 3																
S24	C, 3																
S25	C, 3																
S26	C, 3																
S27	D, 2																
S28	B, 3																
S29	B, 3																
S30	B, 3																
S31	C, 3																
S32	C, 3																
S33	C, 3																

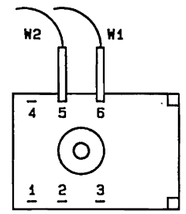
SEE REVERSE SIDE

A1 MODULE **BD2**

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
3. W1 and W2 are black wire jumpers.

A1A1
S46
CIRCUIT SIDE
TOP VIEW



Schematic General Information

P/O A1A1 KEYBOARD ASSEMBLY (08642-60122)

KEYBOARD

ON/STB SWITCH
53 RS
P/O A5 SS55
30
P/O A1A1 J1
W1 (NOTE 3)
W2 (NOTE 3)
S46

SWEEP

COL 0 / ROW 4
COL 0 / ROW 5
COL 0 / ROW 0
S18 STOP FREQ — COL 0 / ROW 7

ENTRY

S
COL 0 / OW 6
OL 2 / OW 1
S19 STOP AMPTD — COL 3 / ROW 1
S7 FREQ — COL 2 / ROW 2
S8 AMPTD — COL 2 / ROW 3
S9 —
S20 AM — COL 3 / ROW 2
S21 FM — COL 3 / ROW 3
S22 BACK SP
S28 MOD FREQ — COL 4 / ROW 2
S29 INCR SET — COL 4 / ROW 3
S30 SAVE

MODULATION SOURCE

S35 INT — COL 0 / ROW 3
S36 EXT AC — COL 0 / ROW 1
S37 EXT DC — COL 5 / ROW 1
S38 OFF ON — COL 5 / ROW 2
S39 SEQ — COL 5 / ROW 3
S40 RECALL

POWER SUPPLY AND GND

POWER SUPPLY AND GROUND
55 AT
2
P/O A5 SS55
9, 10
11, 12
P/O J1
+5V
GND
+5V (F1)
+5V (F1)
TP1
TP5
GND
POWER SUPPLY AND GND
AU 2

SERIAL PREFIX: 2427A

ENTRY

S8 AMP Y0 — COL 2 / ROW 3
S9 — — COL 2 / ROW 4
S10 7 — COL 2 / ROW 5
S11 8 — COL 2 / ROW 6
S12 9 — COL 2 / ROW 7
S13 GHz dBm — COL 2 / ROW 0

DATA

KNOB

S14 ◁ — COL 1 / ROW 0
S15 ▷ — COL 1 / ROW 7

S21 F — COL 3 / ROW 3
S22 BACK SP — COL 3 / ROW 4
S23 4 — COL 3 / ROW 5
S24 5 — COL 3 / ROW 6
S25 6 — COL 3 / ROW 7
S26 MHz V — COL 3 / ROW 0

S29 INCR SET — COL 4 / ROW 3
S30 SAVE — COL 4 / ROW 4
S31 1 — COL 4 / ROW 5
S32 2 — COL 4 / ROW 6
S33 3 — COL 4 / ROW 7
S34 kHz mV — COL 4 / ROW 0

S39 SEQ — COL 5 / ROW 3
S40 RECALL — COL 5 / ROW 4
S41 0 — COL 5 / ROW 5
S42 . — COL 5 / ROW 6
S43 rad % — COL 5 / ROW 7
S44 Hz µV — COL 5 / ROW 0

C1, A7

KB PULLUPS

ROW 7
ROW 6
ROW 5
ROW 4
ROW 3
ROW 2
ROW 1
ROW 0

COL 0
COL 1
COL 2
COL 3
COL 4
COL 5

ATTENTION
Static Sensitive
Devices

DATA

KNOB

STEP

C1, A7
2

COL 2 · ROW 5

S11 · 8 · COL 2 · ROW 6

S12 · 9 · COL 2 · ROW 7

S13 · GHz dBm · COL 2 · ROW 0

S14 · COL 1 · ROW 0

S15 · COL 1 · ROW 7

S16 · COL 1 · ROW 6

S4 · MSSG · COL 1 · ROW 3

S17 · RF OFF/ON · COL 1 · ROW 4

COL 3 · ROW 5

S24 · 5 · COL 3 · ROW 6

S25 · 6 · COL 3 · ROW 7

S26 · MHz V · COL 3 · ROW 0

S27 · COL 1 · ROW 5

COL 4 · ROW 5

S32 · 2 · COL 4 · ROW 6

S33 · 3 · COL 4 · ROW 7

S34 · kHz mV · COL 4 · ROW 0

COL 5 · ROW 5

S42 · . · COL 5 · ROW 6

S43 · rad % · COL 5 · ROW 7

S44 · Hz µV · COL 5 · ROW 0

KB PULLUPS

P/O A10 10k

4 15 2 10 9 7

16 +5V (F1)

ROW 7 · 3
ROW 6 · 13
ROW 5 · 12
ROW 4 · 11
ROW 3 · 6
ROW 2 · 1
ROW 1 · 8
ROW 0 · 14

COL 0 · COL 1 · COL 2 · COL 3 · COL 4 · COL 5

COL 0–COL 5 → AV 2 (6)

P/O J1

COL 0 → 41
COL 1 → 31
COL 2 → 34
COL 3 → 42
COL 4 → 43
COL 5 → 44

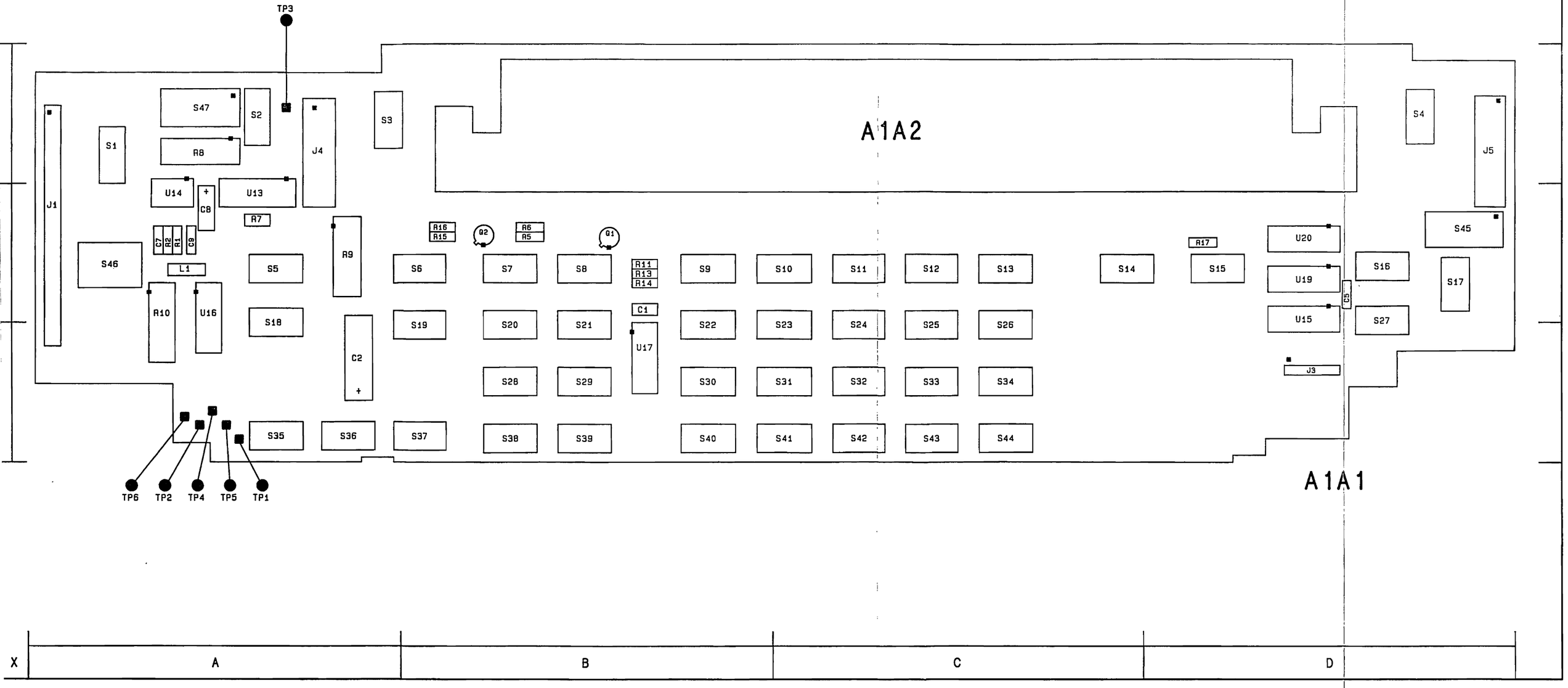
ROW 0 → 33
ROW 1 → 45
ROW 2 → 32
ROW 3 → 39
ROW 4 → 40
ROW 5 → 37
ROW 6 → 38
ROW 7 → 36

P/O A5 DIST. BD. SS55

KEYBOARD MATRIX LINES → AX 9 (14)

ATTENTION
Static Sensitive
Devices

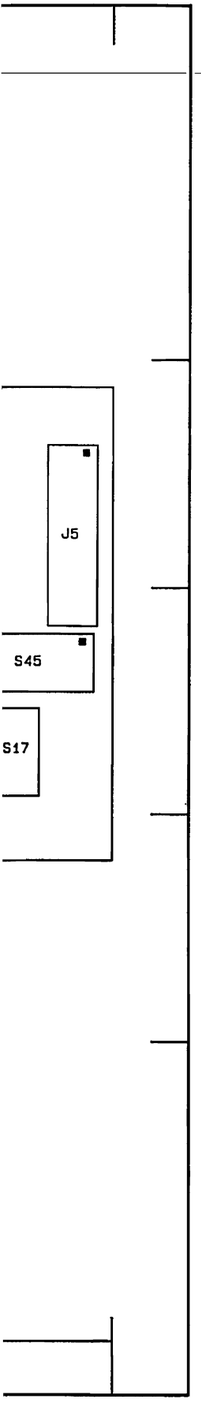
SS1
Figure 8E-103
8E-103

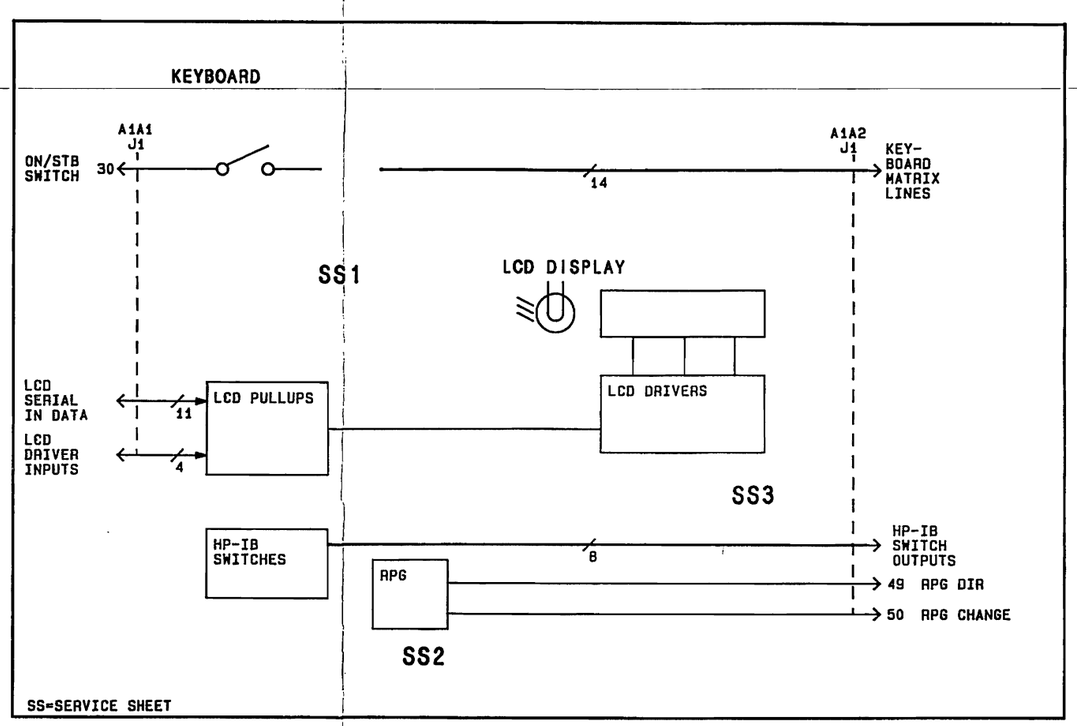


X | A | B | C | D

ure 8E-104. SERVICE SHEET 2 INFORMATION

Component Locator





Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	B, 2	TP2	A, 3														
C2	A, 3	TP3	A, 1														
C5	D, 2	TP4	A, 3														
C7	A, 2	TP6	A, 3														
C8	A, 2																
C9	A, 2	U13	A, 2														
		U14	A, 2														
J1	A, 2	U15	D, 2														
J3	D, 3	U16	A, 2														
J4	A, 1	U17	B, 3														
J5	D, 1	U19	D, 2														
		U20	D, 2														
L1	A, 2																
Q1	B, 2																
Q2	B, 2																
R1	A, 2																
R2	A, 2																
R5	B, 2																
R6	B, 2																
R7	A, 2																
R8	A, 1																
R9	A, 2																
R10	A, 2																
R11	B, 2																
R13	B, 2																
R14	B, 2																
R15	B, 2																
R16	B, 2																
R17	D, 2																
S45	D, 2																
S47	A, 1																

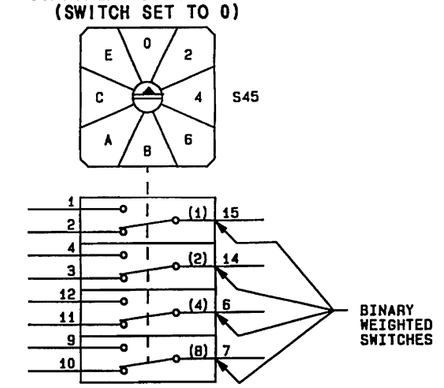
P/O A1A1 KEYBOARD ASSEMBLY **SS1**

SEE REVERSE SIDE

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
3. S45 has mechanically selectable switches. You select switches by changing the position of the arrow on the end of S45. The arrow points to a hexadecimal coded number. This number, when converted to binary code, will indicate binary weighted switch positions. See S45 diagram below.

A1A1
S45
COMPONENT SIDE END VIEW
(SWITCH SET TO 0)



P/O A1A1 KEYBOARD ASSEMBLY (08642-60122)

RESET KEYS (L) 11 LJ 48

LCD SERIAL IN DATA 11 LC 11

LCD DRIVER INPUTS 11 LD 4

LCD BUSY (L) 3 RW 4

P/O A5 DISTRIBUTION BOARD SS55

22 SI0 (H)
21 SI1 (H)
29 SI2 (H)
16 SI3 (H)
28 SI4 (H)
27 SI5 (H)
17 SI6 (H)
26 SI7 (H)
18 SI8 (H)
19 SI9 (H)
20 SI10 (H)
24 CSALL (L)
23 C (H) /D (L)
14 RESET LCD (L)
46 SCK (L)

P/O J1 RESET KEYS (L)

P/O J5 BUSY (L)

LCD PULLUPS

+5V (F1) 16 — P/O R9 10k — 7 10 4 12 3 2 13 1 14 15 11 5 6 9

+5V (F1) 16 — P/O R10 10k — 5

TP4 TP2 TP6

SI0 (H) SI1 (H) SI2 (H) SI3 (H) SI4 (H) SI5 (H) SI6 (H) SI7 (H) SI8 (H) SI9 (H) SI10 (H) CSALL (L) C (H) /D (L) RESET LCD (L) SCK (L)

HP-IB SWITCHES

+5V (F1) 16 — R8 10k — 9 8 7 6 5 4 3 2 1 10 11 12 13 14 15 8

+5V (F1) 16 — P/O R9 10k

LCD LIGHT ON 11 KY 13

P/O A5 SS55

P/O J1 LIGHT (L)

HP-IB SWITCH S47

8 7 6 5 4 3 2 1 — 9 10 11 12 13 14 15 16

X1 X2 X3 "16" "8" "4" "2" "1" — 8

POWER SUPPLY AND GND

POWER SUPPLY AND GND 1 AU 2

+5V (F1) — L1 82 µ — +5V (F2) — +5V (F2) (LCD) — GND 1 (LCD)

C2 100 µ

GND

-5V 55 AX 25 — -5V

15

SERIAL PREFIX: 2427A

KEY DEBOUNCE

KEY DOWN DETECT

COL 0-COL 5 1 AV 6

U16 +5V (F1) 14

COL 0 3
COL 1 1
COL 2 2
COL 3 4
COL 4 5
COL 5 6

8

4

3 P/O S45 (NOTE 3) 14

7

U15A +5V (F1) 14 — 1 2 3 — 7

U15B 4 5 6

U15D 13 12 11

U15C 10 9 8

LCD LIGHTING DRIVERS

CMOS TO TTL TRANSLATION

U17B 3 4 5 6

R11 100k +5V (F1)

U17C 12 13 11 — 10 NC

U17A +5V (F1) 14 — C1 0.1µ — 1 8 2 — 9 — 7

R14 14.7k

R13 10k +5V (F1)

Q1

R16 1k

Q2

R15 1k -5V

R6 1780

R5 1780

1.8 Ω

KEY DEBOUNCE

KEY DOWN DETECT

COL 0-COL 5

U16

+5V (F1)

COL 0
COL 1
COL 2
COL 3
COL 4
COL 5

P/O S45 (NOTE 3)

U15A

U15B

U15C

U15D

U13

RX/CX

CX

R7 31.6k

C8 1µ

U19

C5 0.1µ

NC

P/O S45 (NOTE 3)

LCD CLOCK

U14

R1 1330

R2 4320

C7 1000p

C9 0.1µ

Vcc

TP3

X1
X2
X3
"16"
"8"
"4"
"2"
"1"

LCD LIGHTING DRIVERS

CMOS TO TTL TRANSLATION

U17A

U17B

U17C

R11 100k

C1 0.1µ

R13 10k

R14 14.7k

R16 1k

R15 1k

Q1

Q2

-5V

R6 1780

R5 1780

1.8K

RESET RPG (L)

A1A1

P/O J1

A21 RPG

ROTARY SHUTTER

THE KNOB

P/O J3

RPG LATCHES

R17 13.6k

U20

SI2.H

SCK.L

P/O S45 (NOTE 3)

SI2.H, SCK.L

ATTENTION
Static Sensitive
Devices

+5V (F1)
U13
16
1
2
3
&
R
RX/CX
CX
13
NC
4
NC
15
14
9
10
11
5
NC
12
7
6
8
R7
31.6k
C8
1µ
P/O
S45
(NOTE 3)
+5V (F1)
U19
14
C5
0.1µ
1D
C1
R
S
2
3
1
4
5
6
12
11
13
10
9
NC
8
NC
7

LCD CLOCK
+5V (F2)
R1
1330
R2
4320
+5V (F2)
C7
1000p
C9
0.1µ
U14
2
6
7
8
Vcc
TP3
4
R
G
3
5
NC
1

KEY DWN (L)
P/O
J1
47
X1
X2
X3
"16"
"8"
"4"
"2"
"1"
1
2
3
4
5
6
7
8
8
P/O A5 SS55
KEY DWN (L)
IK
9
HP-IB
SWITCH
OUTPUTS
AD
9

LCD CLK
P/O
J4
10
LCD CLK
RZ
3

DISP BUSY (L)
P/O
J1
15
DISP
BUSY (L)
FH
9

LIGHT 1
LIGHT COM
P/O
J5
5
1
LCD
LIGHTING
SA
3

LIGHT 2
P/O
J4
5

RPG DIR
P/O
J1
49
RPG DIR
EM
9

RPG CHANGE (L)
P/O
J1
50
RPG CHANGE (L)
HW
9,4

C (H) /D (L)
P/O
J5
2
C (H) /D (L)
SB
3

RESET LCD (L)
3
RESET LCD (L
SC
3

SI0 (H)
SI1 (H)
SI2 (H)
SI3 (H)
SI4 (H)
SI5 (H)
6
7
8
9
10
11
SI0-SI5
SD
3

SI6 (H)
SI7 (H)
SI8 (H)
SI9 (H)
SI10 (H)
P/O
J4
1
2
3
4
7
SI6-SI10
SE
3

SCK (L)
8
SCK (L)
SG
3

CSALL (L)
6
CS ALL (L)
SH
3

GND 1 (LCD)
+5V (F2) (LCD)
P/O
J1
11
9
POWER SUPPLY
AND GROUND
SI
3

RESET
RPG (L)
11
LI
A1A1
P/O
J1
35

RPG

ROTARY
SHUTTER
THE
KNOB
+5V
+5V
+5V
3
1
6
4
P/O
J3
+5V (F1)
SI2.H
12
P/O
S45
(NOTE 3)
SCK.L
9
P/O
S45
(NOTE 3)
11
6
10
7
R17
19.6k
+5V (F1)
U20
14
2
3
1
4
12
11
13
10
1D
C1
R
S
5
6
NC
9
NC
8
7
2
SI2.H, SCK.L
15

RPG LATCHES

ATTENTION
Static Sensitive
Devices

SS2
Figure 8E-105
8E-105

A1A2 LCD DISPLAY ASSEMBLY (08642-60121)

LCD LIGHTING
2 SA 3
P/O P2 LITE 2
P/O P1 LITE COM
LITE 1

LCD AND LIGHTS

DS2

SECTION R (RIGHT)
PINS 2-64, 291-353, (PINS 1 AND 354 ARE COMMON BACKPLANE)

SCK (L) 2 SG
CS ALL (L) 2 SH
C (H) /D (L) 2 SB
RESET LCD (L) 2 SC
LCD CLK 2 RZ

LCD DRIVERS

COMMON BACK PLANE

U1 LCD CONTROLLER/ DRIVER 7225
+5V (F2) 3, 7, 33
SCK, CS, C, D, RESET, CL1, CL2, BUSY, SYNC, COM 0, COM 1, COM 2, COM 3
TP1
SI [DATA IN]
NC 14
4, 5, 6

U2, U3, U4, U5 (same)

SI0-SI5 2 SD 6
SI6-SI10 2 SE 5
SI0.H, SI1.H, SI2.H, SI3.H, SI4.H, SI5.H, SI6.H, SI7.H, SI8.H, SI9.H, SI10.H

POWER SUPPLY AND GROUND
2 SI 2
+5V (F1)
+5V (F2)
C1 0.1µ
GND

SERIAL PREFIX: 2427A

DS1

KPLANE)

SECTION C (CENTER)
PINS 65-113, 242-290, (PINS 89 AND 266 ARE COMMON BACKPLANE)

SECTION L (LEFT)
PINS 114-176, 179-241, (PINS 177 AND 178 ARE COMMON BACKPLANE

COMMON BACK PLANE

TP2

C2
0.1µ

+5V (F2)

U4 U5 U6 U7 U8 U9 U10 U11

3, 7, 33

NC

4, 5, 6

ATTENTION
Static Sensitive
Devices

DS1

SECTION C (CENTER)
3, 242-290, (PINS 89 AND 266 ARE COMMON BACKPLANE)

SECTION L (LEFT)
PINS 114-176, 179-241, (PINS 177 AND 178 ARE COMMON BACKPLANE)

DS3

P/O P1

LCD BUSY (L) AM 2

COMMON BACK PLANE

+5V (F2)

C2 0.1µ

U6 U7 U8 U9 U10 U11

3, 7, 33

NC

TP2

TP3

4, 5, 6

ATTENTION
Static Sensitive
Devices

U7 U8 U9 U10 U11

SS3
Figure 8E-107
8E-107

A3 Module

Troubleshooting and Adjustments Contents

Troubleshooting

Adjustments

Troubleshooting

A3 TROUBLESHOOTING INFORMATION

Before Proceeding With Module Troubleshooting

- You should have confidence that A3 is the faulty module from Module Level Diagnostics (MLD) results.

Overall Equipment List

Counter ..... HP 5328A
Digital Voltmeter (DVM) ..... HP 3456A

Essentials of A3 Module Operation

The A3 module consists of one assembly and contains the instrument Microprocessor, Memory, HP-IB, Calabration Data, and associated circuits. Refer to the Simplified Block Diagram on 8F-100 for the following discussion of A3.

The Module controls all aspects of instrument operation. The ROM contains both normal instrument operate on routines, service diagnostic routines and special functions. The EEPROMs contain required module calibration data for proper instrument operation. The RAM is used by the microprocessor to store and recall data for instrument operation including 51 complete instrument setups. The RAM is battery backed up and will retain data while the instrument is disconnected from the power line. The microprocessor and HP-IB Interface control the transfer of data to and from the instrument over the Bus.

COMPONENT REPLACEMENT PROCEDURES

The instrument's printed circuit boards are manufactured using a Hot Air Leveled (HAL) process. The printed circuit board traces, pads and plated-through holes (PTH) are copper and very fragile. While the process has several advantages over conventional processes, the printed circuit boards are more susceptible to broken traces, lifted pads and damage to the plated-through holes. Therefore, additional care must be taken when replaceing components on HAL printed circuit boards.

Listed below are soldering considerations that apply to all printed circuit boards:

The temperature of the soldering iron tip and time the tip is in contact with the printed circuit board.

The size and shape of the soldering iron tip.

The pressure of the soldering iron tip on the pad.

The operator's skill.

When replaceing components on HAL printed circuit boards the following steps should be taken:

Use a temperature controlled soldering iron set at a temperature of 600° F (315° C).

Cut out the body of the component to be removed. (Leave leads as long as possible for easier removal.)

Apply heat to the lead only. Adding solder as required, slide the tip down to the pad and remove solder with solder sucker.

CAUTION

Tip pressure on the pad is most critical and is totally operator dependent. Excessive tip pressure will damage or destroy the board. Do not use desoldering braid or solder wicking techniques on Hot Air Leveled boards.

The melting point of solder in the plated thorough hole (PTH) is reached in 2.5 seconds at a tip temperature of 600° to 750° F (315° to 400° C). The recommended time for heat to be applied is **3 seconds.** Keep the solder sucker clean and do not let the tip of the solder sucker hit the pad when removing solder. Breaking the lead loose can damage the PTH. If the lead is attached to the PTH after the solder has been removed, reheat the lead to remove it.

When soldering or desoldering multilead components, do not consecutively apply heat to adjacent leads. Instead, distribute heat by skipping leads or crossing to opposite side of device.

STATIC SENSITIVE DEVICES

This instrument has been assembled in and Electrical Static Discharge (ESD) protected environment. Use proper ESD precautions when handling boards or removing and replacing components.

CHECK 1: POWER SUPPLY, CLOCK AND RESET CHECKS

Essentials of A3 Module Control Operation

Refer to BD3 Figure 8F-101. Located on SS4 you will find the 5 MHz Oscillator. The 5 MHz Oscillator is the instrument 5 MHz clock to the Microprocessor, Priority Interrupt Encoding, and divided-by-2 for the HP-IB 2.5 MHz clock. The Microprocessor Enable (E) output (500 KHz) is the 5 MHz clock divided by 10 to enable the Timer.

Located on SS6 you will find the Reset Status Detector and Controller Reset and Power Up Protection Circuits. The Address Error Detector determines if the logic is in an illegal state. When an unused address is on the bus and the bus is strobed, there is a possibility the Microprocessor could "run away" or halt operation. The Low Voltage Detector determines if the +5 Vdc supply is below a set threshold. When either condition is detected the Microprocessor and the instrument are reset by the controller Reset and Power Up Protection Circuits. Connecting the Runaway Reset to TTL High prevents the Address Error Detector from reseting the Microprocessor.

Description of Check 1

The power supply +5 Volts to the A3 Module and the clocks are checked.

Required Equipment:

Counter ..... HP 5343A
Digital Voltmeter (DVM) ..... HP 3456A

Test the A3 Power Supply; Clocks; and Reset Circuit

1. Setup:

   Set the HP 8642A/B POWER switch to **Standby**.

   Remove the top cover.

   Use the Module locator diagram on the inside of the top cover to locate the A3 module.

   Raise the black and white extractors to their upright position.

   Pull the A3 module up and out of the instrument.

   Install the DCU Extender board (08642-60137) in the slot that the A3 module came out of.

   Connect the A3 module to the DCU Extender board.

   Set the HP 8642A/B POWER switch to **On**.

2. Measure Voltage Levels and Frequencies:

   Use the Digital Voltmeter to verify test points on 1, 2, 6, and 7 on the A3 module as shown in Table 8F-1.

   Use the Counter to verify test points 3, 4, and 5 on the A3 module as shown in Table 8F-1.

Table 8F-1.

Test Points				Measurement
No.	Component	Pin No.	Signal	
1	C44	+	+5V	≈ 5 Vdc
2	C44	-	GND	≈ 0 Vdc
3	U12	15	Clock	5 MHz
4	U12	19	E Clock	500 kHz
5	U10	3	Clock÷2	2.5 MHz
6	U14	6	LV Det	TTL High
7	J4	16	Reset	≈ 5Vdc

CHECK 2: MICROPROCESSOR, TIMER, ROM, RAM, EEPROM

Essentials of SS7 Operation

Refer to BD3 Figure 8F-101. Located on SS7 you will find the ROM and RAM Memory.

- Check 1 must pass.
- Microprocessor and Address Decoders on SS5 must be all right.

Description of Check 2

The Microprocessor Timer and RAM are checked by firmware routines, and the ROM and EEPROMS check sums are checked. The special Service Mode is entered and then the test initialized.

Test the Microprocessor

1. Preset the HP 8642 by pressing the Instr Preset (green key).
2. After the Preset Routine is completed, a frequency of 100 MHz and an amplitude of −140 dBm are displayed.
3. Enter [SHIFT], [SPCLS], OFF. ENTER NUMBER .PO is displayed.
4. Enter [3], ENTERING SERVICE MODE. I25 is displayed.
5. Enter [3] [9] [Hz] to initiate the Microprocessor test.
6. DIAG DONE HIT MSSG .V1 is displayed. Use [MSSG] to scroll through messages. TEST 9 OF A03 PASSED .U27 or TEST 9 OF A03 FAILED .U28 is displayed.

NOTE

U27 and U28 are error numbers for the A3 Module not U numbers for IC's.

Test the ROM

7. Repeat steps 1 through 4 above.
8. Enter [3] [1] [Hz] to initiate the ROM test.
9. DIAG DONE HIT MSSG .V1 is displayed. Use [MSSG] to scroll through messages.

   A complete list of messages is shown in Table 8F-3, ROM Messages.

   DIAG DONE, ERROR CODE A03 FAILED .U _____ is displayed. .U _____ is the Error Code or Message Code.

Table 8F-2. *ROM Test Messages*

Message Code	Meaning
.U2	ROM U23 Bad Check Sum
.U3	ROM U24 Bad Check Sum
.U4	ROM U25 Bad Check Sum
.U5	ROM U26 Bad Check Sum
.U6	ROM U27 Bad Check Sum
.U7	ROM U28 Bad Check Sum
.U8	ROM U32 Bad Check Sum
.U9	ROM U33 Bad Check Sum
.U10	ROM Check Sum Passed Test
.U11	ROM Check Sum Failed Test

NOTE

The RAM test is a non-destructive test. The contents of the RAM stack are not destroyed.

Test the RAM

10. Repeat steps 1 through 4 of the Microprocessor Test.
11. Enter [3] [2] [Hz] to initiate the RAM test.
12. DIAG. DONE HIT MSSG .V1 is displayed. Use [MSSG] to scroll through messages.

    ERROR CODE A03 FAILED .U _____ is displayed. U _____ is the ERROR CODE or MESSAGE CODE.

    A complete list of messages is shown in Table 8F-3, RAM Test Messages.

Table 8F-3. *RAM Test Messages*

Message Code	Meaning
.U12	RAM U34 Failed
.U13	RAM U35 Failed
.U14	RAM U36 Failed
.U15	RAM U37 Failed
.U16	RAM Test Passed
.U17	RAM Test Failed

Test the Timer

13. Repeat steps 1 through 4 of the Microprocessor Test.
14. Enter [3] [5] [Hz] to initiate Timer Test.
15. DIAG DONE HIT MSSG .V1 is displayed. Use [MSSG] to scroll through messages.

    TEST 5 of A03 Passed .U24

    TEST 5 of A03 Failed .U25

NOTE

The timer is checked using firmware timing loops.

Test the EEPROMS

16. Repeat steps 1 through 4 of the Microprocessor Test.
17. Enter [3] [4] [Hz] to initiate EEPROM test.
18. DIAG. DONE HIT MSSG .V1 is displayed. Use [MSSG] to scroll through messages.

    ERROR CODE A03 FAILED .U _____ is displayed. .U _____ is the Error Code or Message Code.

    A complete list of Messages is shown in Table 8F-4.

NOTE

Calibration Data is stored as 16 bit words. Low 8 bits (D0-D7) in U20 and upper 8 Bits (D8-D16) in U21. There is an EEPROM Cal Data Check sum for each module or section of module calibrated for the upper 8 bits (U21) and for the lower 8 bits (U20).

Table 8F-4. *EEPROM Test Codes*

Code	Meaning
U505	EEPROM Check Sum Tests Passed
U506	EEPROM Check Sum Test or Tests Failed
	U21 Check Sum Error, Cal Data
U510	Instrument Data, Model, Serial Number, Options
U511	A11, Ref Loop Module, Cal Data
U512	A12, Sum Loop Module, Cal Data
U513	A6, FM Loop Module, Cal Data
U514	A13, Output Module, Cal Data
U515	P/O A19, Doubler Section, Cal Data
U516	A16 (8642A), P/O (8642B) Attenuator, Cal Data
U517	P/O A19, Reverse Power 8642B, Cal Data
U518	A14, Heterdyne Module, Cal Data
U519	A2, Modulation Module, Cal Data
	U20 Check Sum Error, Cal Data
U520	Instrument Data, Model, Serial Number, Options
U521	A11, Ref Loop Module, Cal Data
U522	A12, Sum Loop Module, Cal Data
U523	A6, FM Loop Module, Cal Data
U524	A13, Output Module, Cal Data
U525	P/O A19, Doubler Section, Cal Data
U526	A16 (8642A), P/O (8642B) Attenuator, Cal Data
U527	P/O A19, Reverse Power 8642B, Cal Data
U528	A14, Heterdyne Module, Cal Data
U529	A2, Modulation Module, Cal Data
	U20 and U21 Check sum Error, Cal Data
U530	Instrument Data, Model, Serial Number, Options
U531	A11, Ref Loop Module, Cal Data
U532	A12, Sum Loop Module, Cal Data
U533	A6, FM Loop Module, Cal Data
U534	A13, Output Module, Cal Data
U535	P/O A19, Doubler Section, Cal Data
U536	A16 (8642A), P/O (8642B) Attenuator, Cal Data
U537	P/O A19, Reverse Power 8642B, Cal Data
U538	A14, Heterdyne Module, Cal Data
U539	A2, Modulation Module, Cal Data

Adjustments

DESCRIPTION OF A3 ADJUSTMENT

Overall Equipment List

Digital Voltmeter ..... HP 3456A

To adjust the threshold voltage of the Low Voltage Detector A3U514.

ADJUSTMENT 1: LOW VOLTAGE DETECTOR

- Service Sheet 6

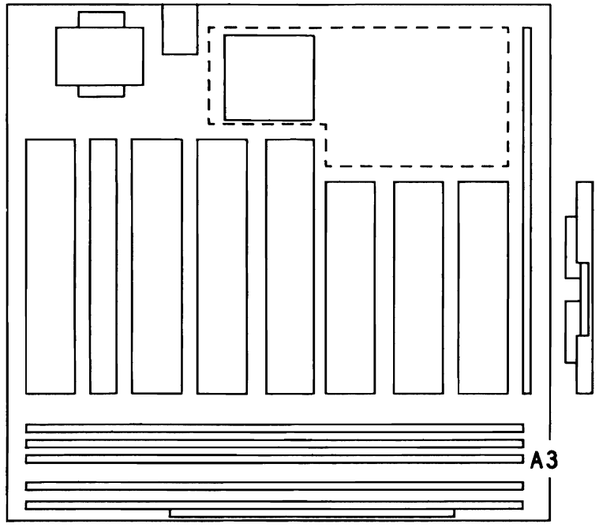
Required Equipment

Digital Voltmeter ..... HP 3456A

Procedure

1. Set the voltmeter to measure +2.4 Vdc. Connect its input to A3TP1 (Low Voltage threshold Test Point).
2. Adjust A3R49 (Low Voltage Adjustment) for between +2.3 +2.4 Vdc measured at A3TP1.

Assembly Locator



Simplified Block Diagram

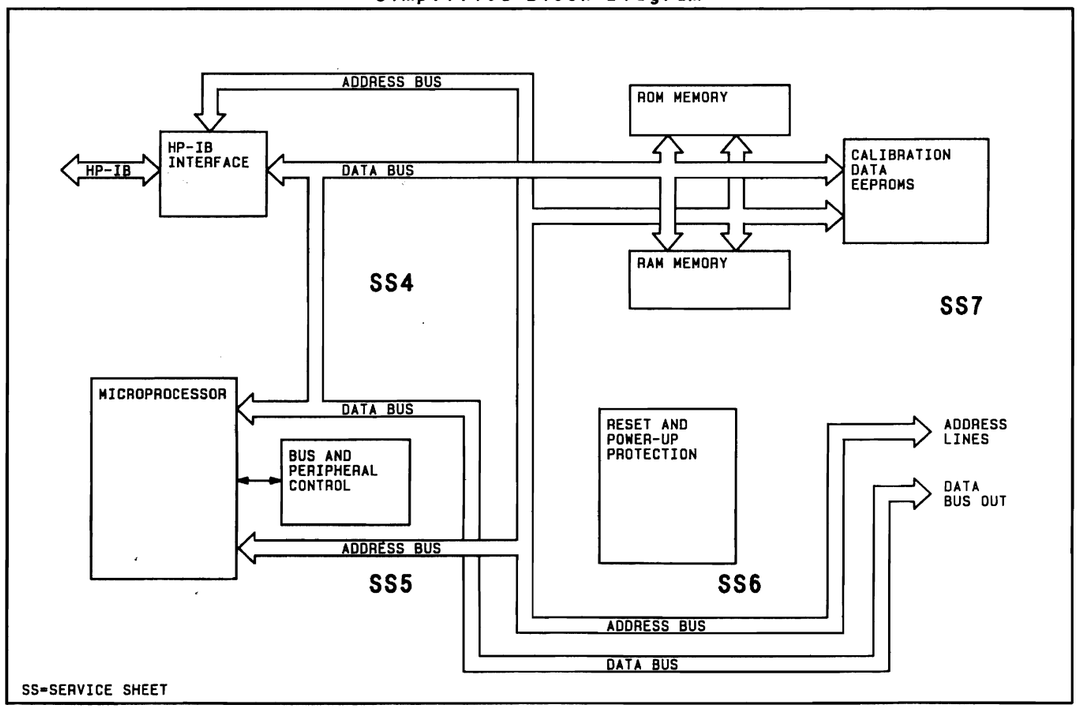
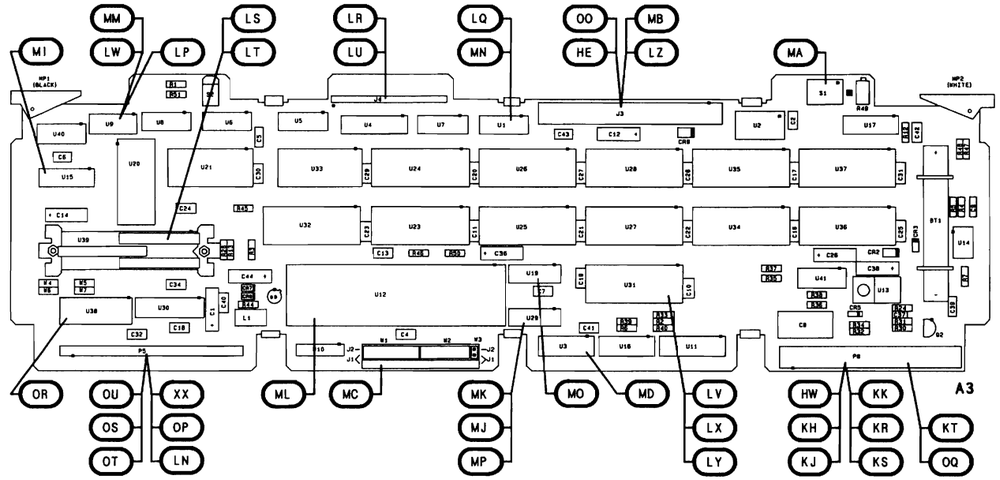


Figure 8F-100 BD3 General Information.

Module Test Point/Adjustment Locations



RS 232 INT SERIVCE CONNECT 46
SERVICE CONNECT 42
APG CHANGE(L)
BD2
BD4 HW 22
LB INT
BD4 KH 24
HP-IB SC
BD4 OR 24
INTERFACE MANAGEMENT
SS12 OS 2
INTERFACE MANAGEMENT/HANDSHAKE
SS12 OT 6
REAR PANEL HP-IB
HP-IB DATA
SS12 OU 8
SERVICE CONNECT 25
POWER SUPPLY AND GND
57 TG 2
SIGNAL COMMON
12 TL 19
+5V UNREG
BD17 OQ 8
P/O J3
P/O P8
P/O P5
P/O J3
P/O P5
ATN 4
EOI 6
SRQ 2
REN 16
IFC 14
DAV 8
NDAC 12
NRFD 10
DIO1 42
DIO2 40
DIO3 38
DIO4 36
DIO5 34
DIO6 32
DIO7 30
DIO8 28
+5V 47-50
GND 5, 9, 13, 17, 21, 26, 27, 29, 31, 33, 35, 39, 41, 43-46
HP-IB INTERFACE
HP-IB
POWER SUPPLY AND GND
POWER SUPPLY AND GND 2 LN 5,6
HP-IB ADDRESS A1-A3
UWR
OUTPUT ENABLE
HP-IB SEL
INTERRUPT PRIORITY ENCODING
X/Y
TTL HIGH 2
PROCESSOR INTERRUPT 3
TTL HIGH 1
D8-D15 (DATA BUS)
D8-D15
5 MHz CLOCK
CONTROLLER RESET
5 MHz OSCILLATOR
UWR
VAL MEM
TIMER SEL
TIMER ENABLE
TIMER
A6-A8 TIMER ADDRESS
LY
LQ
LP
LS
MC
MA
MB
A6-A8 (TIMER ADDRESS)
DATA BUS D8-D15
HP-IB ADDRESS A1-A3
SS4
LT
MO
ML
LW
LU
MD
LR
LV
LX
CLK
4
CLK
4
2
6
D0-D15
D0-D15
DATA BUS DISCONNECT
MICROPROCESSOR
3
PROCESSOR INTERRUPT
CONTROLLER RESET
LWR R/W DAWR, UWR
LATCH LWR LATCH UWR
AS
UDS
LDS
BUS AND PERIPHERAL CONTROL
UWR
CONTROLLER RESET
EEPROM OUTPUT ENABLE
EOE
OE
OUTPUT ENABLE
ADDRESS STROBE
ADDRESS BUS A1-A23
A19
3
D8-D15
DATA BUS
ADDRESS BUS A8-A15
TTL HIGH 1
TTL HIGH 2
ADDRESS DECODER
MEMORY SELECT
HB-IB SEL
TIMER SEL
ROM1 SEL
ROM2 SEL
ROM3 SEL
ROM4 SEL
RAM1 SEL
RAM2 SEL
A/D SEL
D/A SEL
LATCH SEL
CAL BD SEL
UNUSED ADDRESS DET
A16-18
A13-15
DATA BUS D0-D15
4 LN 2 POWER SUPPLY AND GND +5V(F1), GND

SERIAL PREFIX: 2427A

PRIORITY ENCODING
X/Y
TTL HIGH 2
PROCESSOR INTERRUPT
3
TTL HIGH 1
D8-D15
R
DATA BUS D8-D15
HP-IB ADDRESS A1-A3
SS4
LY
LS
MC
MA
A6-A8 (TIMER ADDRESS)
MB
LP
6
DATA BUS DISCONNECT
D0-D15
EEPROM OUTPUT ENABLE
OUTPUT ENABLE
OM
UT
LE
EOE
OE
DATA BUS
D8-D15
ADDRESS BUS A8-A15
TTL HIGH 1
TTL HIGH 2
ADDRESS DECODER
A16-18
A13-15
MEMORY SELECT
HB-IB SEL
TIMER SEL
MB
LT
MO
ML
LW
LZ
2
P/O P5
LUWR
LLWR
25
20
LUWR, LLWR
KX
BD4
P/O J4
CLK
AS
UDS
LDS
LUWR
LLWR
2
4
17
18
15
14
P/O SERVICE TEST POINTS
ROM1 SEL
ROM2 SEL
ROM3 SEL
ROM4 SEL
RAM1 SEL
RAM2 SEL
9
10
11
12
8
7
DAWR
P/O P8
10
KK
BD4
R/W
32
KS
BD4
ADDRESS DECODE
A/D SEL
D/A SEL
LATCH SEL
29
28
30
3
KT
BD4
P/O J3
18
RS 232 SELECT SERVICE CONNECT
CAL BD SEL
UNUSED ADDRESS DET
MP
MC
MK
MM
MI
MJ
LR
SS5
ROM MEMORY
ROM1 SEL
ROM2 SEL
ROM3 SEL
ROM4 SEL
D0-D15 (DATA BUS)
D0-D15 (DATA BUS)
D8-D15 (DATA BUS)
A1-A15 (MEMORY ADDRESS BUS)
MEMORY SELECT
A1-A15 (MEMORY ADDRESS BUS)
A1-A11
7
OUTPUT ENABLE
RAM1 SEL
RAM2 SEL
EEPROM SEL
CALIBRATION DATA EEPROMS
RAM MEMORY
CONTROLLER RESET
EEPROM OUTPUT ENABLE
+5V UNREG
GROUND
6
PZ
POWER SUPPLY AND GND
LWR, UWR
LWR, UWR
BATTERY SENSE
EEPROM WE
SS7
MN
2
RESET STATUS DETECTION
PROC STATUS
3
ERROR DET
ADDRESS STROBE
BUS GRANT
UNUSED ADDRESS DET
ERROR DET A20-A22
RUNAWAY RESET DISCONNECT
TTL HIGH 2
CONTROLLER RESET AND POWER UP PROTECTION
4
LN
POWER SUPPLY AND GND
+5V (F1), GND
GROUND
PZ
7
CONTROLLER RESET
SS6
ADDRESS BUS A1-A11
ADDRESS BUS A1-A11, A19, A20
DATA BUS D0-D15
DATA BUS D0-D15
DATA BUS D0-D15
CONTROLLER RESET
CAL BD SEL
CAL BD SEL

ROM MEMORY

ROM1 SEL
ROM2 SEL
ROM3 SEL
ROM4 SEL

D0-D15 (DATA BUS)
D0-D15 (DATA BUS)
D8-D15 (DATA BUS)
A1-A15 (MEMORY ADDRESS BUS)
A1-A15 (MEMORY ADDRESS BUS)
A1-A11
MEMORY SELECT
OUTPUT ENABLE

CALIBRATION DATA EEPROMS
EEPROM SEL
EEPROM OUTPUT ENABLE
EEPROM WE

RAM1 SEL
RAM2 SEL
RAM MEMORY
CONTROLLER RESET
LWR, UWR
LWR, UWR
BATTERY SENSE

POWER SUPPLY AND GND
+5V UNREG
GROUND
6 (PZ)

SS7

(LZ)
(MN)

RESET STATUS DETECTION

RUNAWAY RESET DISCONNECT

CONTROLLER RESET AND POWER UP PROTECTION

TTL HIGH 2

PROC STATUS 3
ERROR DET
ADDRESS STROBE
BUS GRANT
UNUSED
ADDRESS DET

ERROR DET A20-A22

4 (LN)
POWER SUPPLY AND GND
+5V(F1), GND
GROUND (PZ) 7

CONTROLLER RESET

SS6

ADDRESS BUS A1-A11
ADDRESS BUS A1-A11, A19, A20
DATA BUS D0-D15
DATA BUS D0-D15
CONTROLLER RESET
CAL BD SEL
CAL BD SEL

(MP) (MC) (MK) (MM) (MI) (MJ) (LR)

P/O P5
25
20
LUWR, LLWR (KX) BD4

P/O J4
2
4
17
18
15
14
9
10
11
12
8
7
P/O SERVICE TEST POINTS

P/O P8
10 DAWR (KK) BD4
32 R/W (KS) BD4
29
28
30
3
ADDRESS DECODE (KT) BD4

P/O J3
18 RS 232 SELECT SERVICE CONNECT

BEEPER
P/O J3
24 BEEPER (QQ) SS13

A1 26
A2 27
A3 28
A4 29
A5 30
A6 31
A7 32
A8 33
A9 34
A10 35
A11 36

UWR 22
LWR 19
CAL BD SEL 39
EQE 23
CAL BD ADDRESS AND CONTROL 15 (RS) SS13

D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
D7 8
D8 9
D9 10
D10 11
D11 12
D12 13
D13 14
D14 15
D15 16
CAL BOARD DATA 16 (HE) SS13

TO CAL BOARD (A20)

P/O P8
2 BATTERY SENSE (KL) BD4
1 EEPROM WE (KI) BD4

A1 20
A2 19
A3 18
A4 17
A5 16
A6 15
A7 14
ADDRESS LINES 7 (KR) BD4

OE 26 OUTPUT ENABLE (KJ) BD4

D0 49
D1 48
D2 47
D3 46
D4 45
D5 44
D6 43
D7 42
D8 41
D9 40
D10 39
D11 38
D12 37
D13 36
D14 35
D15 34
DATA BUS OUT 16 (KU) BD4

P/O J4
A19 5
A20 6
+5V(F1) 3
GND 1
P/O SERVICE TEST POINTS

P/O P5
SRQ COM 1
ATN COM 3
DAV COM 7
NRDF COM 11
NDAC COM 15
IFC COM 18
OUTER SHIELD 22, 23
HP-IB COMMON GND 7 (OP) BD4

BD3
Figure 8F-101
8F-101

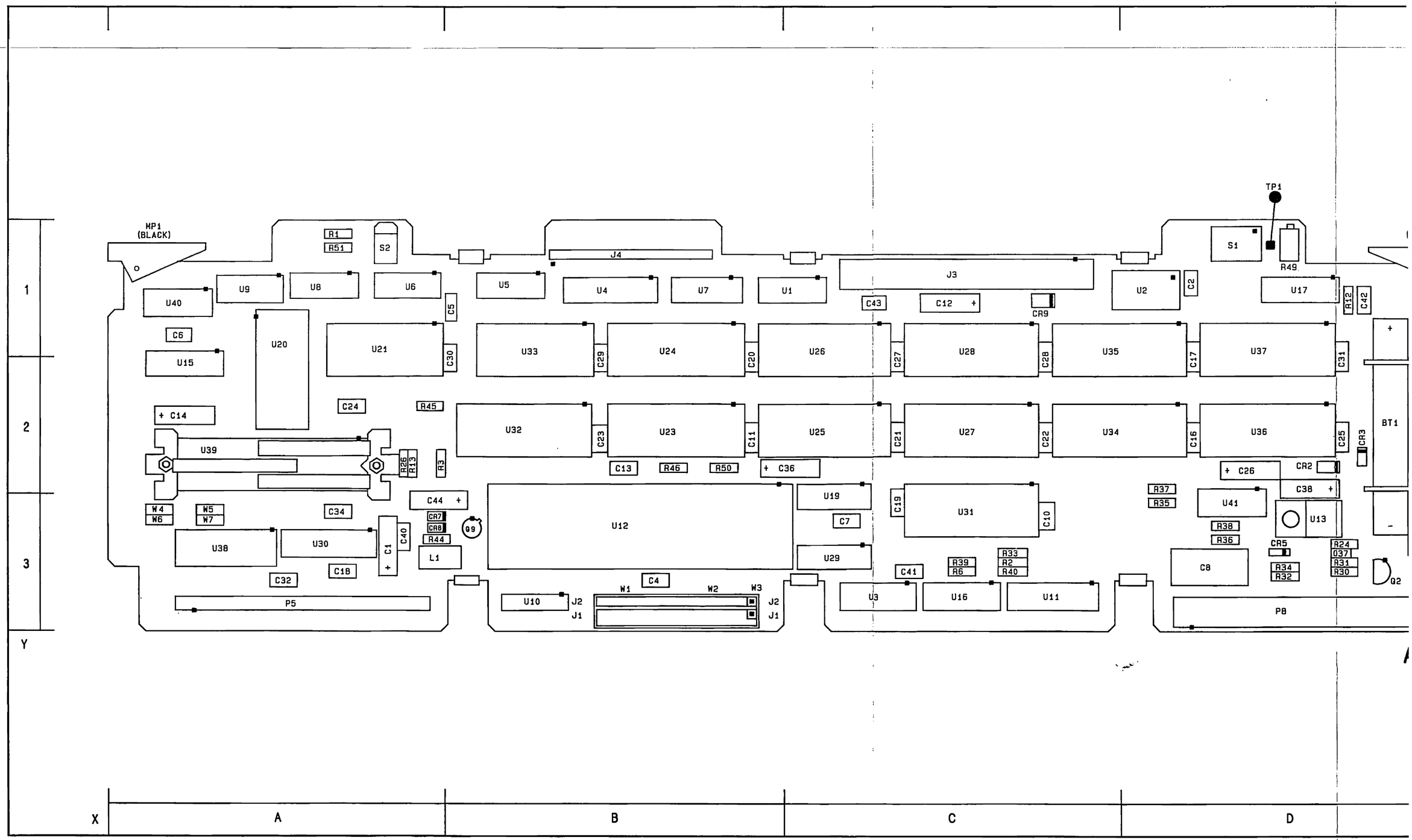
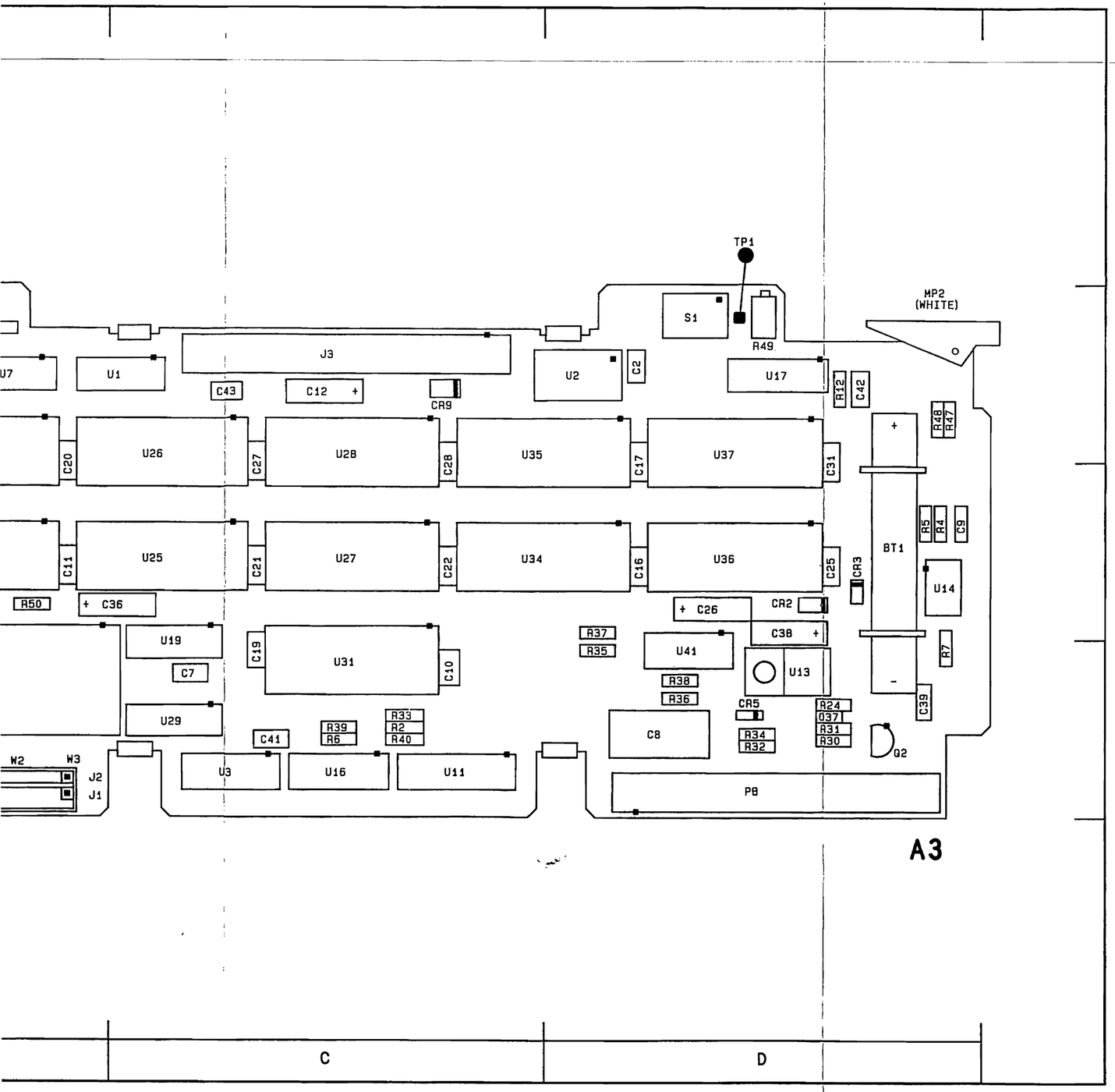
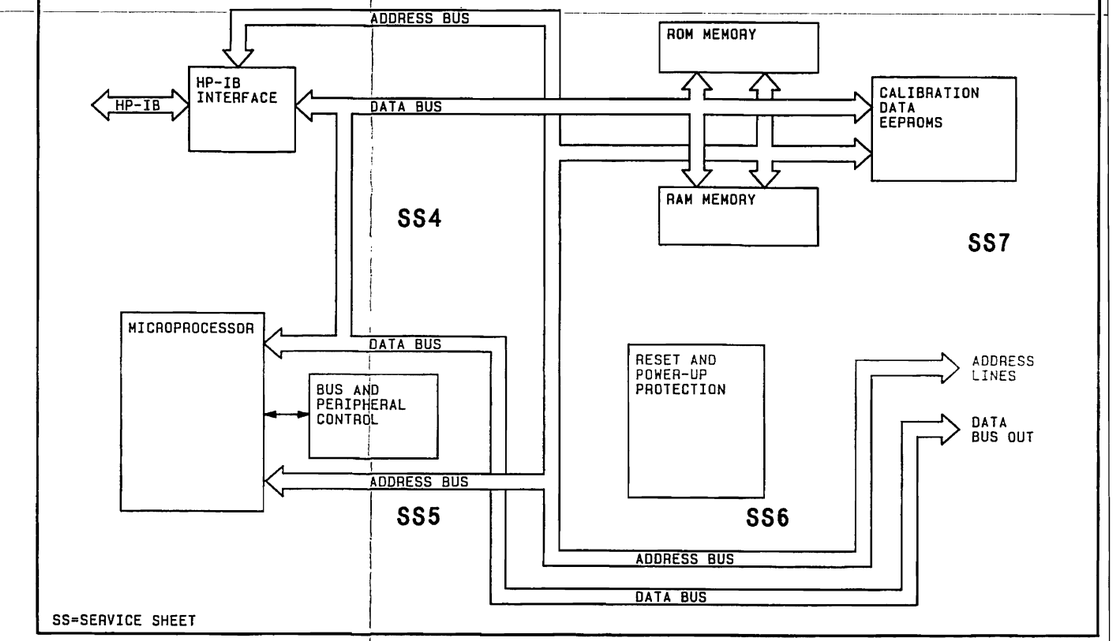


Figure 8F-102. SERVICE SHEET 4 INFORMATION

Component Locator



Component Locator



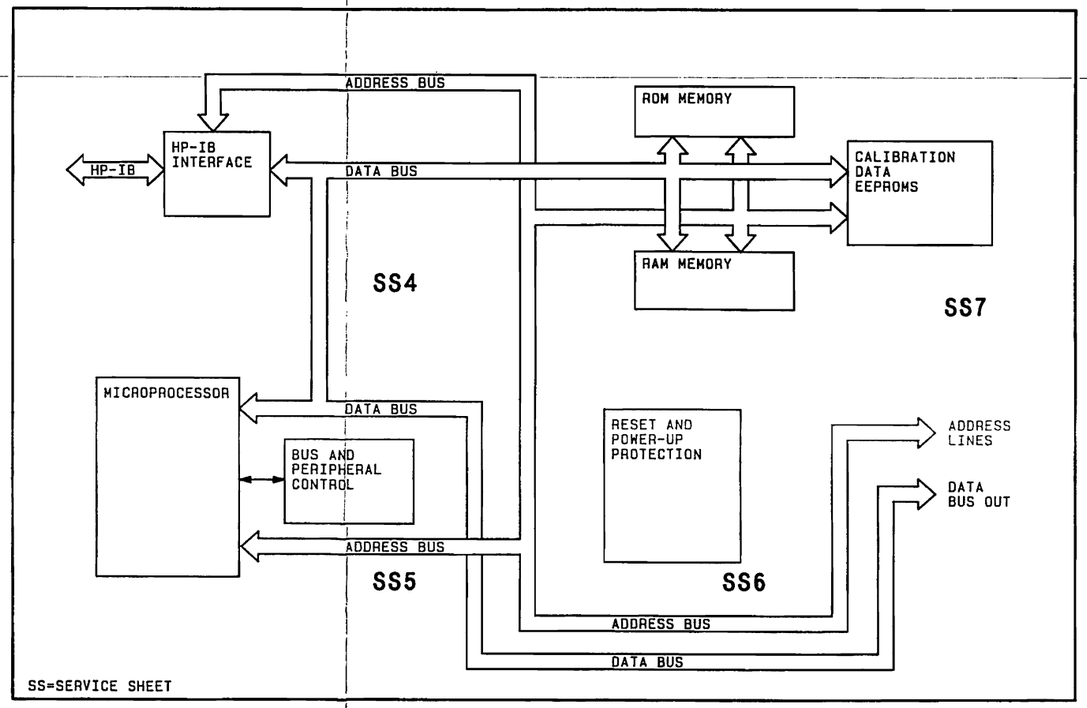
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	A, 3	U2	D, 1														
C2	D, 1	U3	C, 3														
C6	A, 1	U4	B, 1														
C10	C, 3	U6	A, 1														
C12	C, 1	U7	B, 1														
C14	A, 2	U9	A, 1														
C18	A, 3	U10	B, 3														
C19	C, 3	U11	C, 3														
C32	A, 3	U16	C, 3														
C34	A, 3	U30	A, 3														
C36	B, 2	U31	C, 3														
C40	A, 3	U38	A, 3														
C41	C, 3	U39	A, 2														
C42	D, 1																
C43	C, 1	W4	A, 3														
C44	A, 3	W5	A, 3														
		W6	A, 3														
J3	C, 1	W7	A, 3														
L1	A, 3																
MP1	A, 1																
MP2	D, 1																
P5	A, 3																
P8	D, 3																
R2	C, 3																
R6	C, 3																
R12	D, 1																
R13	A, 2																
R26	A, 2																
R39	C, 3																
R40	C, 3																
S1	D, 1																

A3 MODULE **BD3**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	A, 3	U2	D, 1														
C2	D, 1	U3	C, 3														
C6	A, 1	U4	B, 1														
C10	C, 3	U6	A, 1														
C12	C, 1	U7	B, 1														
C14	A, 2	U9	A, 1														
C18	A, 3	U10	B, 3														
C19	C, 3	U11	C, 3														
C32	A, 3	U16	C, 3														
C34	A, 3	U30	A, 3														
C36	B, 2	U31	C, 3														
C40	A, 3	U38	A, 3														
C41	C, 3	U39	A, 2														
C42	D, 1																
C43	C, 1	W4	A, 3														
C44	A, 3	W5	A, 3														
		W6	A, 3														
J3	C, 1	W7	A, 3														
L1	A, 3																
MP1	A, 1																
MP2	D, 1																
P5	A, 3																
P8	D, 3																
R2	C, 3																
R6	C, 3																
R12	D, 1																
R13	A, 2																
R26	A, 2																
R39	C, 3																
R40	C, 3																
S1	D, 1																

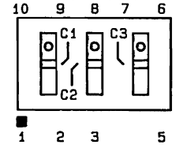
SEE REVERSE SIDE

A3 MODULE **BD3**

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
3. W4-W7 are 0 ohm resistors.
4. All capacitors shown in Power Supply and Gnd are connected between +5V and ground planes. They are layed out in strategic locations to reduce undesired signal effects.

A3
S1
COMPONENT SIDE
TOP VIEW



CHANGES

2526A and above

On the schematic:

- In **5 MHz OSCILLATOR**, change the power supply to U2 pin 4 from +5V(F1) to +5V(F3).

2613A and above

On the Component Locator:

- R52 - Add R52 between U4 and U33.

In Component Coordinates:

- R52 - Add R52 B,1.

On the schematic:

- R52 - In **5 MHz OSCILLATOR**, add R52 immediately off the output of U4 pin 14, in the series path before the first node.
- In the upper left portion of the schematic change the A3 part number to 08642-60224.

P/O A3 MICROPROCESSOR/MEMORY MODULE (08642-60124)

RS 232 INT
SERVICE CONNECT
RPG CHANGE (L)
2,9 HW
LB INT
9 KH
HP-IB SC
11 OA
INTERFACE MANAGEMENT
12 OS
INTERFACE MANAGEMENT/ HANDSHAKE
12 OT
HP-IB DATA
12 OU
SIGNAL COMMON
12 TL
POWER SUPPLY AND GROUND
57 TG
P/O A5 SS58
P/O A5 SS57 (08642-60126) INTERFACE ASSY
P/O A5 DISTRIBUTION
P/O A5 SS57
P/O J3
P/O P8
P/O P5
SERVICE CONNECT
UNR
5 LQ
OUTPUT ENABLE
5,7 LP
CONTROLLER A
5,6,7 LR
POWER SUPPLY AND GND
LN 5,6

HP-IB INTERFACE

INTERFACE BUS TRANSCEIVER

U38
+5V (F1)
C32 0.1µ
EN1/G4
EN2/G5
EN3
EN6
ATN
EOI
SRQ
REN
IFC
DAV
NDAC
NRFD
W7 (NOTE 3)
W6 (NOTE 3)
W5 (NOTE 3)
W4 (NOTE 3)

PARALLEL POLL DETECT

U7B
+5V (F1)

HP-IB DATA BUS TRANSCEIVER

U30
+5V (F1)
C18 0.1µ
M1 [3S]
M2 [OC]
EN3 [XMT]
EN4 [RCV]
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8

U39
+5V (F1)
C34 0.1µ
GENERAL PURPOSE INTERFACE ADAPTER 9914A
CONT
REN
IFC
NDAC
NRFD
DAV
EOI
ATN
SRQ
TRIG
TE
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
HP-IB INTERFACE
INSTRUMENT INTERFACE
WE
DBIN
RS0
RS1
RS2
CE
CLK
INT
RESET
ACCRQ
ACCGR
D0
D1
D2
D3
D4
D5
D6
D7
A1
A2
A3
2.5 MHz
LEVEL 2 INT
NC
R26 5110 +5V

LEVEL TRANSLAT
U9A

POWER SUPPLY AND GND

P/O P5
+5V
GND
L1 5µ
(NOTE 4)
+5V (F1)
C40 0.1µ
C1 22µ
C6 0.1µ
C10 4.7µ
C14 4.7µ
C41 0.1µ
C42 0.1µ
C43 0.1µ
C12 4.7µ
C26 4.7µ
C36 4.7µ
C44 4.7µ

5 MHz OSCILLATOR

EXT CLK SWITCH
5MHz OSCILLATOR
+5V (F1)
U4E
P/O S1
U2
NC
C2 0.1µ
U10
CT=0
CTRDIV16
7, 12, 13

SERIAL PREFIX: 2427A

UWR 5 LQ

OUTPUT ENABLE 5,7 LP

HP-IB ADDRESS 5 LS 3

HP-IB SEL 5 LT

INTERRUPT PRIORITY ENCODING

LEVEL TRANSLATE U9A

U39

GENERAL PURPOSE INTERFACE ADAPTER 9914A

HP-IB INTERFACE

INSTRUMENT INTERFACE

CONT, REN, IFC, NDAC, NRFD, DAV, EOI, ATN, SRQ, TRIG, TE, DIO1–DIO8

WE, DBIN, RS0, RS1, RS2, CE, CLK, INT, RESET, ACCRQ, ACCGR, D0–D7

+5V (F1) C34 0.1µ

A1 A2 A3

2.5 MHz

LEVEL 2 INT

NC R26 5110 +5V (F1)

+5V (F1) R13 10k

LB INT U4B

RPG CHANGE (L) U6D

+5V (F1) R12 10K P/O S1

SA SWITCH

+5V (F1) R40 10k R5 1k

TTL HIGH 1 MA 5

PARALLEL POLL DETECT

U7B

HP-IB DATA BUS TRANSCEIVER

U30

M1 [3S] M2 [OC] EN3 [XMT] EN4 [RCV]

3 (1▽/2▽)

+5V (F1) C18 0.1µ

DIO1–DIO8

TIMER

5 MHz CLOCK LU 5

+5V (F1) C19 0.1µ R2 10k

U31

PROGRAMABLE TIMER 6840

IRQ, W/R, CS0, CS1, ENABLE, RS0, RS1, RS2, RESET, CLOCK 1, GATE 1, CLOCK 2, GATE 2, CLOCK 3, GATE 3, D0–D7, O1–O3

VAL MEM 5 LV

TIMER SEL 5 LW

TIMER ENABLE 5 LX

TIMER ADDRESS 5 LY

U9F

CONTROLLER RESET 5,6,7 LA

5 MHz OSCILLATOR

DIVIDE BY 2

U10 CTRDIV16

EXT CLK SWITCH

5MHz OSCILLATOR

U4E

U2

P/O S1

7, 12, 13 NC 8, 9, 10, 11 NC

C2 0.1µ

+5V (F1) C12 4.7µ C26 4.7µ C36 4.7µ C44 4.7µ

GND

POWER SUPPLY AND GND LN 5,6

ADDRESS
HP-IB SEL
5 LT
INTERRUPT PRIORITY ENCODING
LB INT
U4B
RPG CHANGE (L)
U6D
+5V (F1)
R13 10k
R40 10k
R6 1k
U11
U16
HPR1/BIN
LEVEL 1
LEVEL 2
LEVEL 3
LEVEL 4
LEVEL 5
LEVEL 6
LEVEL 7
R12 10K
P/O S1
SA SWITCH
R39 4640
U3
IPL0
IPL1
IPL2
NC
TTL HIGH 2
MC 5,6
PROCESSOR INTERRUPT
MD 5
P/O J3
BEEPER
OO 13
TTL HIGH 1
MA 5
DATA BUS
5,7 MB
D0-D15
5 MHz CLOCK
LU 5
TIMER
U31
PROGRAMABLE TIMER 6840
C19 0.1µ
R2 10k
UWR
VAL MEM
5 LV
TIMER SEL
5 LW
TIMER ENABLE
5 LX
TIMER ADDRESS
5 LY
U9F
IRQ
W/R
CS0
CS1
ENABLE
RS0
RS1
RS2
RESET
CLOCK 1
GATE 1
CLOCK 2
GATE 2
CLOCK 3
GATE 3
ATTENTION
Static Sensitive
Devices
P/O P8
P/O A5 SS58
CAL BOARD DATA
HE 13
DATA BUS OUT
KU 8

SS4
Figure 8F-103
8F-103

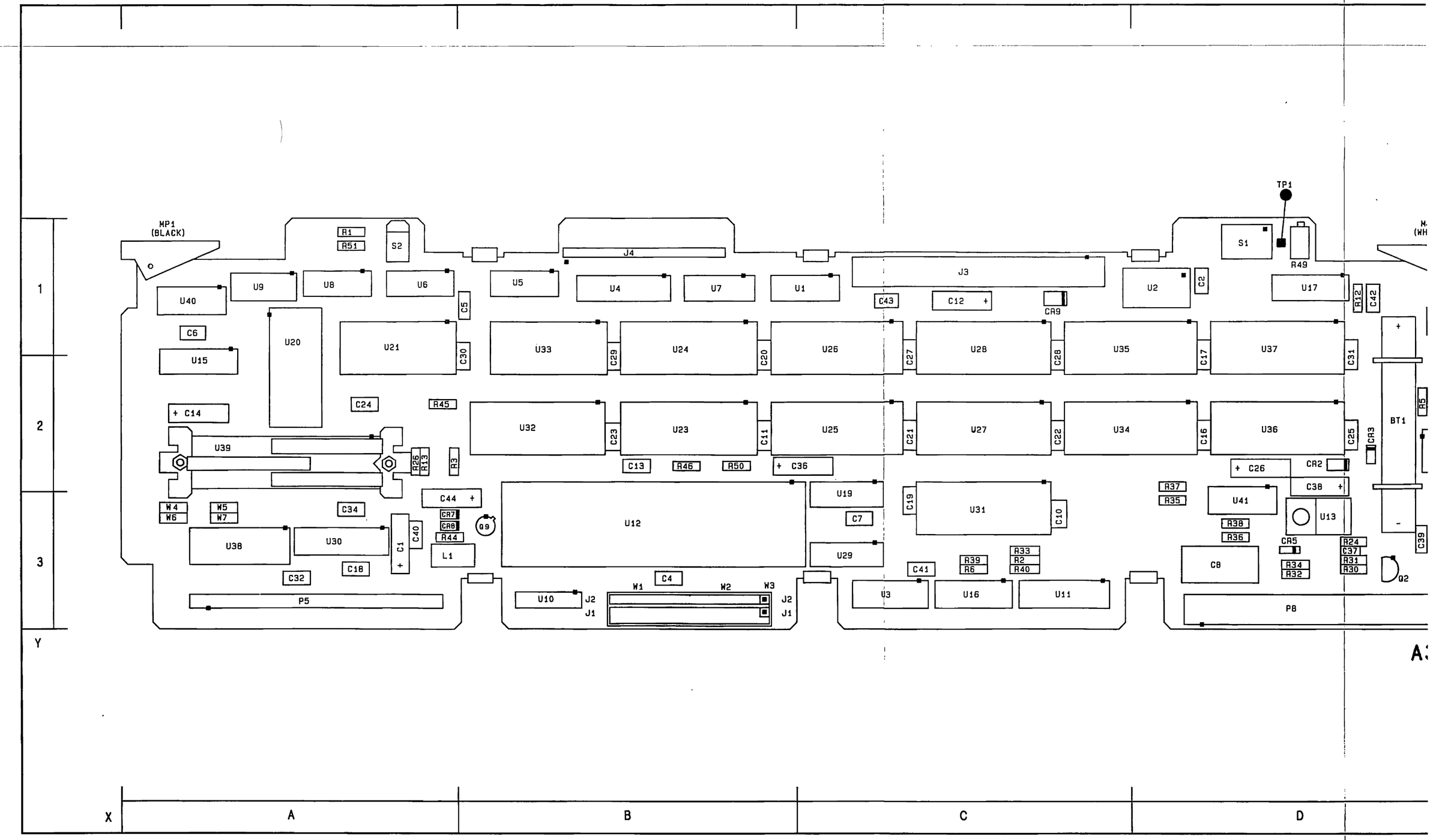
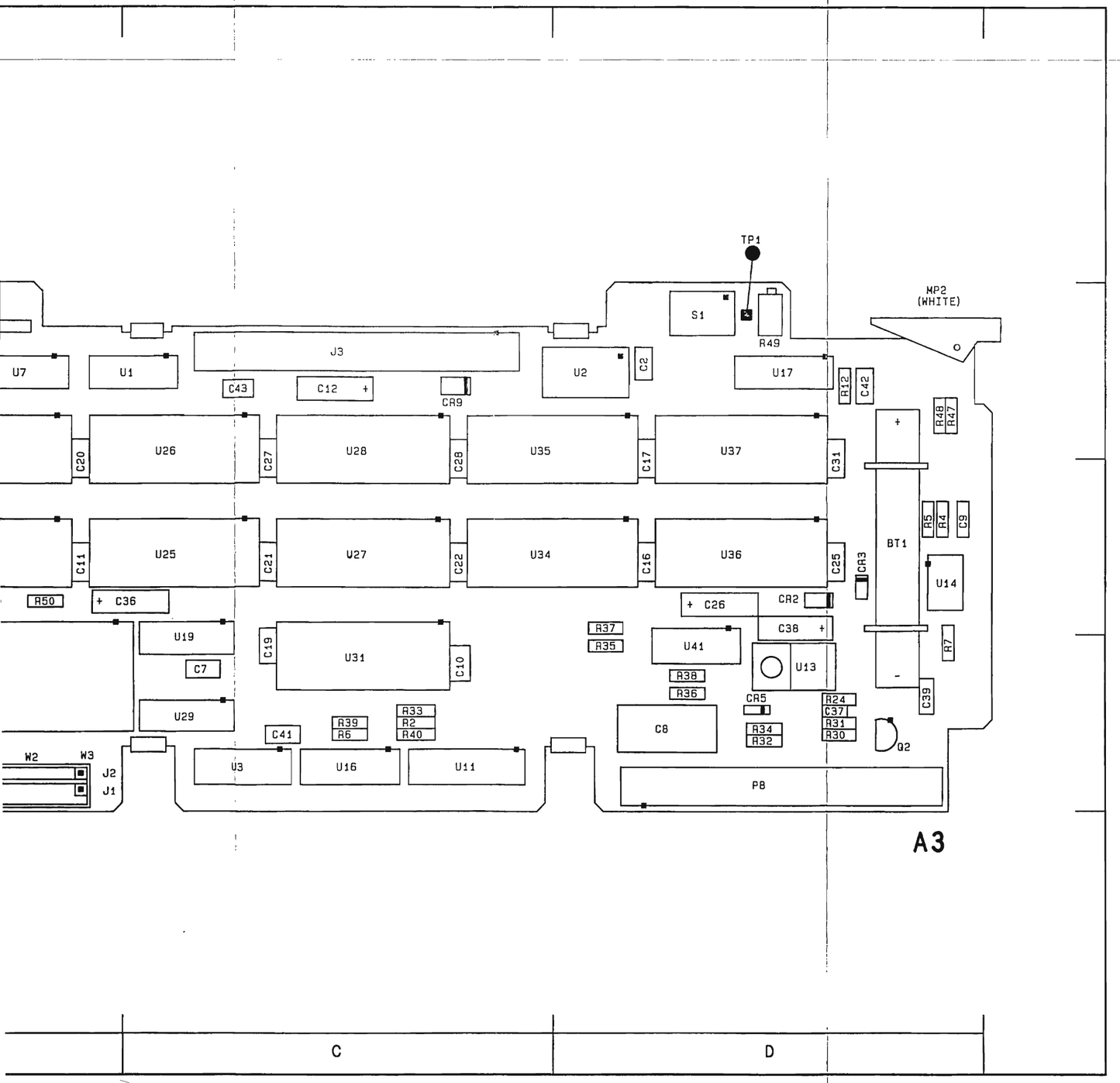
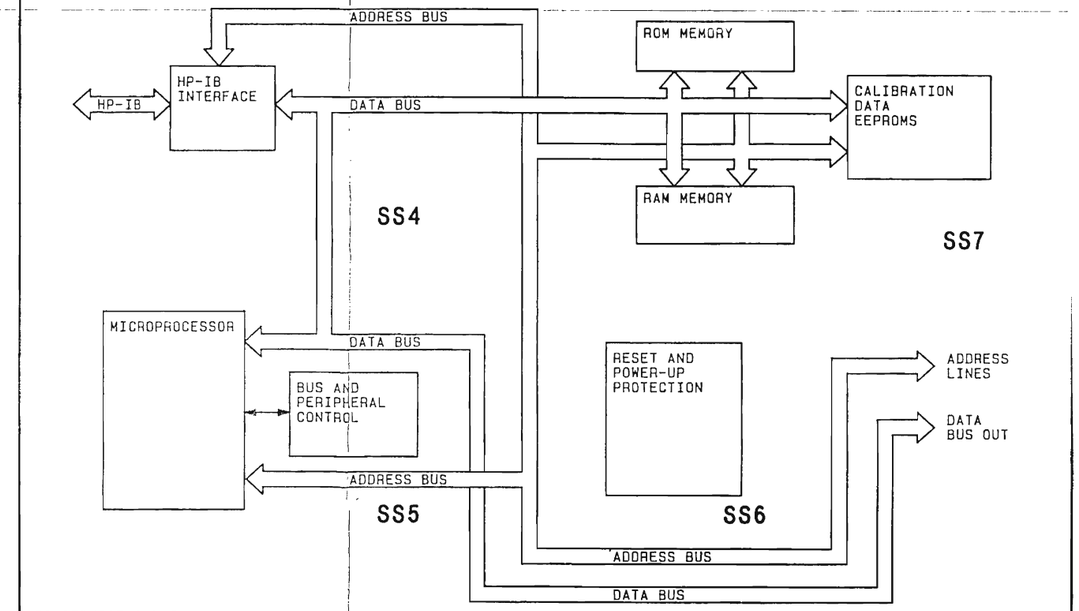


Figure 8F-104. SERVICE SHEET 5 INFORMATION

Component Locator



Component Locator



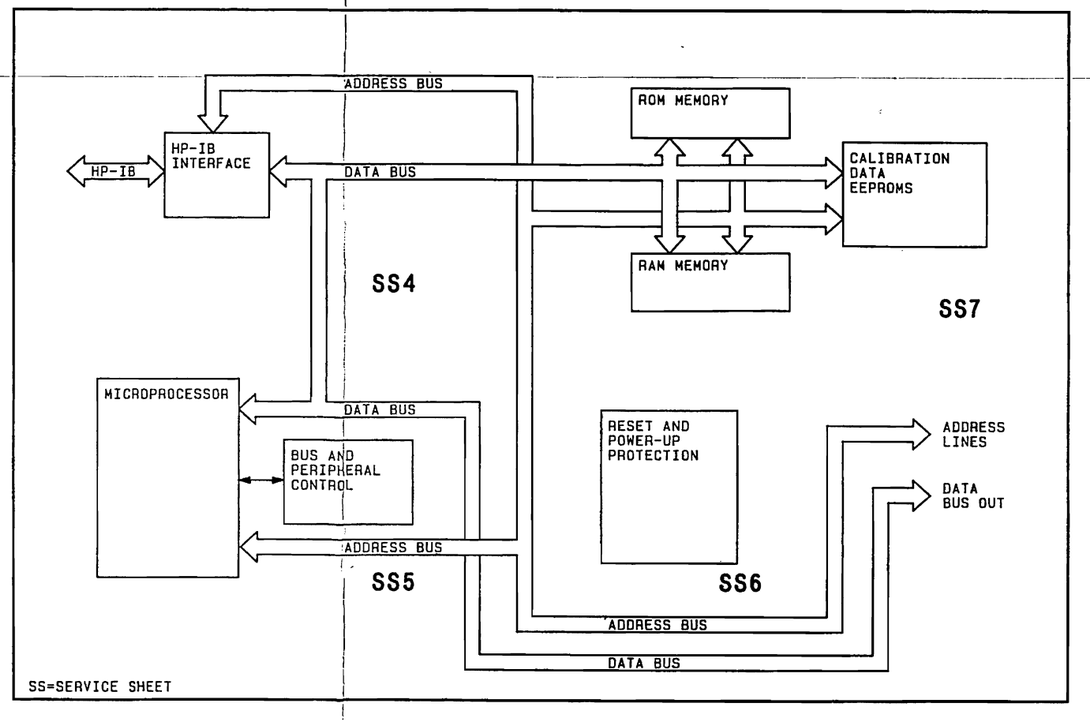
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C4	B, 3	U1	B, 1												
C5	B, 1	U4	B, 1												
C7	C, 3	U5	B, 1												
C13	B, 2	U6	A, 1												
		U7	B, 1												
CR7	A, 3	U8	A, 1												
CR8	A, 3	U9	A, 1												
		U12	B, 3												
J1	B, 3	U17	D, 1												
J2	B, 3	U19	C, 3												
J3	C, 1														
J4	B, 1	W1	B, 3												
		W2	B, 3												
MP1	A, 1														
MP2	D, 1														
P5	A, 3														
P8	D, 3														
Q9	B, 3														
R1	A, 1														
R3	A, 2														
R44	A, 3														
R45	A, 2														
R46	B, 2														
R50	B, 2														

P/O A3 PROCESSOR/ MEMORY MODULE **SS4**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C4	B, 3	U1	B, 1												
C5	B, 1	U4	B, 1												
C7	C, 3	U5	B, 1												
C13	B, 2	U6	A, 1												
		U7	B, 1												
CR7	A, 3	U8	A, 1												
CR8	A, 3	U9	A, 1												
		U12	B, 3												
J1	B, 3	U17	D, 1												
J2	B, 3	U19	C, 3												
J3	C, 1														
J4	B, 1	W1	B, 3												
		W2	B, 3												
MP1	A, 1														
MP2	D, 1														
P5	A, 3														
P8	D, 3														
Q9	B, 3														
R1	A, 1														
R3	A, 2														
R44	A, 3														
R45	A, 2														
R46	B, 2														
R50	B, 2														

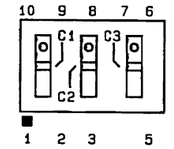
P/O A3 PROCESSOR/ MEMORY MODULE SS4

SEE REVERSE SIDE

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
3. W2 and W3 are 8 contact blue post jumpers. They connect one row of J2 to the single row of J1 for normal operation. To disconnect data bus, move jumpers over to connect one row of J2 to its other row. This other row is grounded.

A3
S1
COMPONENT SIDE
TOP VIEW



CHANGES

All Serial Prefixes

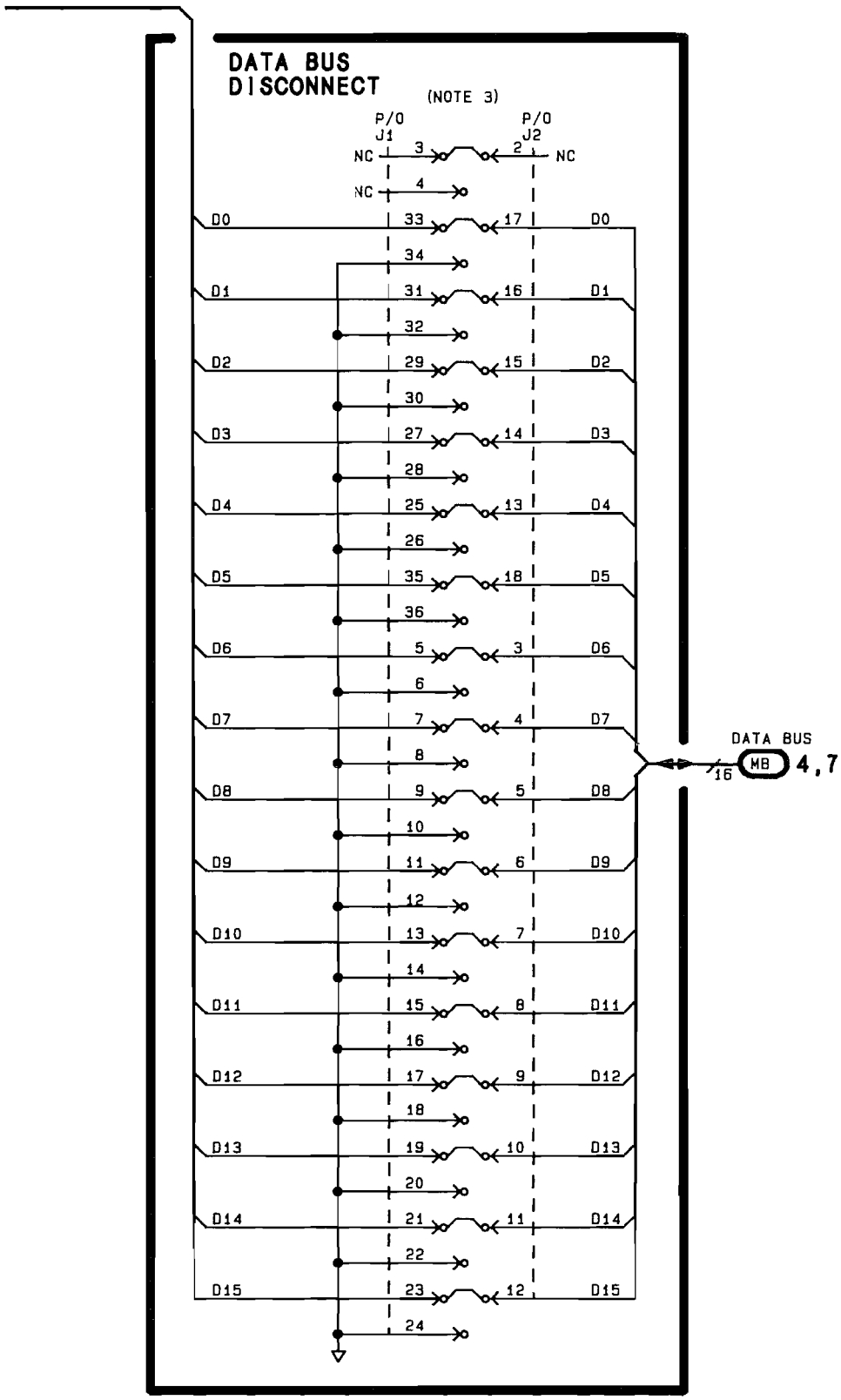
In Schematic General Information (Notes):

- J1, J2 - In Note 3, change J1 to J2 and J2 to J1.

2613A and above

On the schematic:

- In the upper left portion of the schematic change the A3 part number to 08642-60224.



CHANGES TO FIGURE 8F-105 (All serial prefixes)

MICROPROCESSOR

5 MHz CLOCK 4 LU

VAL MEM 4 LV

TIMER ENABLE 4 LX

PROCESSOR INTERRUPT 4 MD

CONTROLLER RESET 4,6,7 LR

POWER SUPPLY AND GND 4 LN

C13 0.1µ

C4 0.1µ

U12 MIRCOPROCESSOR 68000

+5V (F1)

R46 10k

R50 10K

IPL0 IPL1 IPL2

FC0 FC1 FC2

CLK E VMA BR BG BGACK IPL 0 IPL 1 IPL 2 RESET HALT BERR

D0–D15

R/W LDS UDS AS VPA DTACK

A1–A23

16, 53

BUS AND PERIPHERAL CONTROL

WRITE ENABLE

U1B U7A U1A

LWA UWA DAWA

OUTPUT ENABLE LOGIC

U6A U6B U4A U4C U9C U4D U9B U6C

C5 0.1µ

OUTPUT ENABLE

DATA ACKNOWLEDGE

R3 1k

U5

U8

R1 1k

LATCH UWA LATCH LWA NC

PROC STATUS MI 6

BUS GRANT MJ 6

ADDRESS ERROR DET MK 6

A19 A20-23 A1-A20

MEMORY ADDRESS BUS ML 7

A1-A15 A1-A11, A13-A15

HP-IB ADDRESS LS 4

A1-A3 A6-A8

POWER SUPPLY AND GND

+5V (F1)

SERIAL PREFIX: 2427A

RAL CONTROL

ENABLE

LWR

U1B

UWR

CLK

A/W

LWR

DAWR

UWR

U1A

+5V (F1)

U8

LATCH UWR

LATCH LWR

R1
1k

OUTPUT ENABLE
LOGIC

U6A

U6B

U6C

U4C

U4D

U9C

C5
0.1µ

OUTPUT ENABLE

DATA ACKNOWLEDGE

R3
1k

U5

ATTENTION
Static Sensitive
Devices

EEPROM
OUTPUT ENABLE

CR7

CR8

R44
2150

Q9

R45
196

EEPROM
OUTPUT
ENABLE
LZ 7

OUTPUT
ENABLE
LP 4

EOE

OE

ADDRESS
STROBE
MM 6

ADDRESS
ERROR DET
MK 6

A20-23

A1-A20

MEMORY
ADDRESS
BUS
ML 7
A1-A15

HP-IB ADDRESS
LS 4
A1-A3

TIMER ADDRESS
LY 4
A6-A8

A1-A11, A13-A15

DATA BUS
DISCONNECT
(NOTE 3)

P/O J1

P/O J2

NC

D0

D1

D2

D3

D4

D5

D6

D7

D8

D9

D10

D11

D12

D13

D14

D15

DATA BUS
MB 4,7

TTL HIGH 2
4,6 MC

TTL HIGH 1
4 MA

ADDRESS
DECODER

ADDRESS DECODER

U19

U17

BIN/OCT

C7
0.1µ

A16

A17

A18

A13

A14

A15

&

EN

15 ROM1 SEL
14 ROM2 SEL
13 ROM3 SEL
12 ROM4 SEL
11 RAM1 SEL
10 RAM2 SEL
9 EEROM SEL
7 I/O SEL

15 HP-IB SEL
14 RS 232 INT
13 TIMER SEL
12 A/D SEL
11 D/A SEL
10 LATCH SEL
9 CAL BD SEL

A16-A18

A13-A15

ATTENTION
Static Sensitive
Devices

DATA BUS
DISCONNECT
(NOTE 3)

P/O J1 — P/O J2

NC 3 — 2 NC
NC 4
D0 35 — 18 D0
36
D1 33 — 17 D1
34
D2 31 — 16 D2
32
D3 29 — 15 D3
30
D4 27 — 14 D4
28
D5 25 — 13 D5
26
D6 23 — 12 D6
24
D7 21 — 11 D7
22
D8 19 — 10 D8
20
D9 17 — 9 D9
18
D10 15 — 8 D10
16
D11 13 — 7 D11
14
D12 11 — 6 D12
12
D13 9 — 5 D13
10
D14 7 — 4 D14
8
D15 5 — 3 D15
6

DATA BUS (MB) 4,7 — 16

ENABLE

+5V (F1)
R44 2150
Q9
R45 196
EEPROM OUTPUT ENABLE (LZ) 7

UT LE 4
EOE
OE
2

TTL HIGH 2 4,6 (MC)
TTL HIGH 1 4 (MA)

ADDRESS DECODER

ADDRESS DECODER
+5V (F1)
C7 0.1µ
U19 16 BIN/OCT
A16 1
A17 2
A18 3
6
4
5
& EN
8
0 15 ROM1 SEL
1 14 ROM2 SEL
2 13 ROM3 SEL
3 12 ROM4 SEL
4 11 RAM1 SEL
5 10 RAM2 SEL
6 9 EEROM SEL
7 7 I/O SEL

+5V (F1)
U17 16 BIN/OCT
A13 1
A14 2
A15 3
6
4
5
& EN
8
0 15 HP-IB SEL
1 14 RS 232 INT
2 13 TIMER SEL
3 12 A/D SEL
4 11 D/A SEL
5 10 LATCH SEL
6 9 CAL BD SEL
7 7

U9E
11 — 10

LWR, UWR (MN) 7

MEMORY SELECT (MO) 7
ROM1 SEL
ROM2 SEL
ROM3 SEL
ROM4 SEL
RAM1 SEL
RAM2 SEL

HP-IB SEL (LT) 4
TIMER SEL (LW) 4
UNUSED ADDRESS DET (MP) 6

A16-A18 3 3 A13-A15

ADDRESS 4

P/O P5
LATCH UWR 25
LATCH LWR 20
6
LUWR, LLWR (KX) 11

P/O J4
CLK 2
AS 4
UDS 17
LDS 18
LATCH UWR 15
LATCH LWR 14
A19 5
A20 6
OE 13
1

ROM1 SEL 9
ROM2 SEL 10
ROM3 SEL 11
ROM4 SEL 12
RAM1 SEL 8
RAM2 SEL 7

P/O SERVICE TEST POINTS

P/O P8
DAWR 10
R/W 32
A/D SEL 29
D/A SEL 28
LATCH SEL 30
A1 20
A2 19
A3 18
A4 17
A5 16
A6 15
A7 14
OE 26

P/O J3
RS-232 SEL 18
UWR 22
LWR 19
CAL BD SEL 39
EOE 23
A1 26
A2 27
A3 28
A4 29
A5 30
A6 31
A7 32
A8 33
A9 34
A10 35
A11 36

RS 232 SELECT SERVICE CONNECT

P/O A5 SS57

P/O A5 DISTRIBUTION ASSY SS56
DAWR (KK) 10
R/W (KS) 8
ADDRESS DECODE (KT) 8
ADDRESS LINES (KR) 8
OUTPUT ENABLE (KJ) 9

CAL BD ADDRESS AND CONTROL (RS) 13

16 13 13

SS5
Figure 8F-105
8F-105

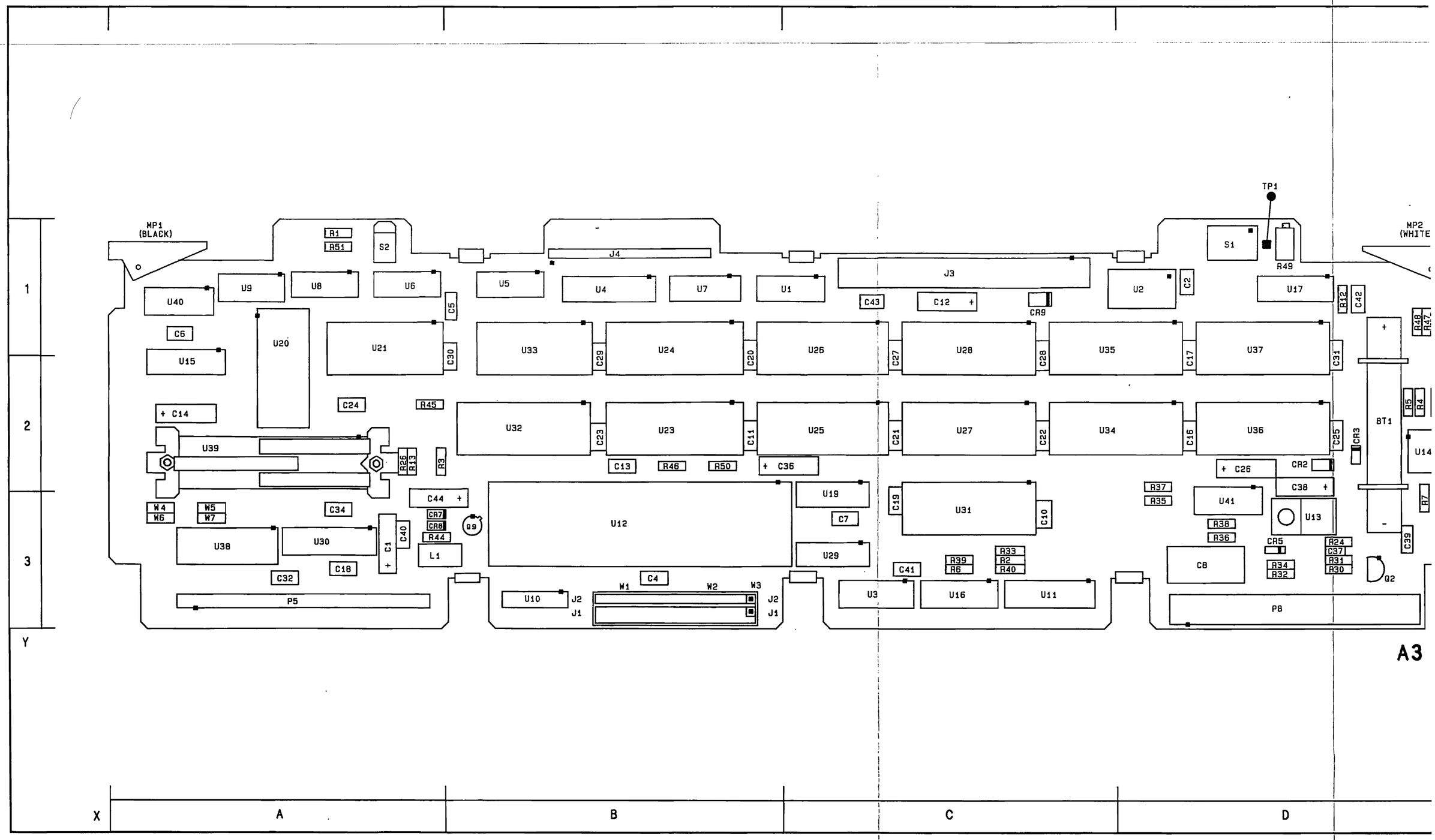
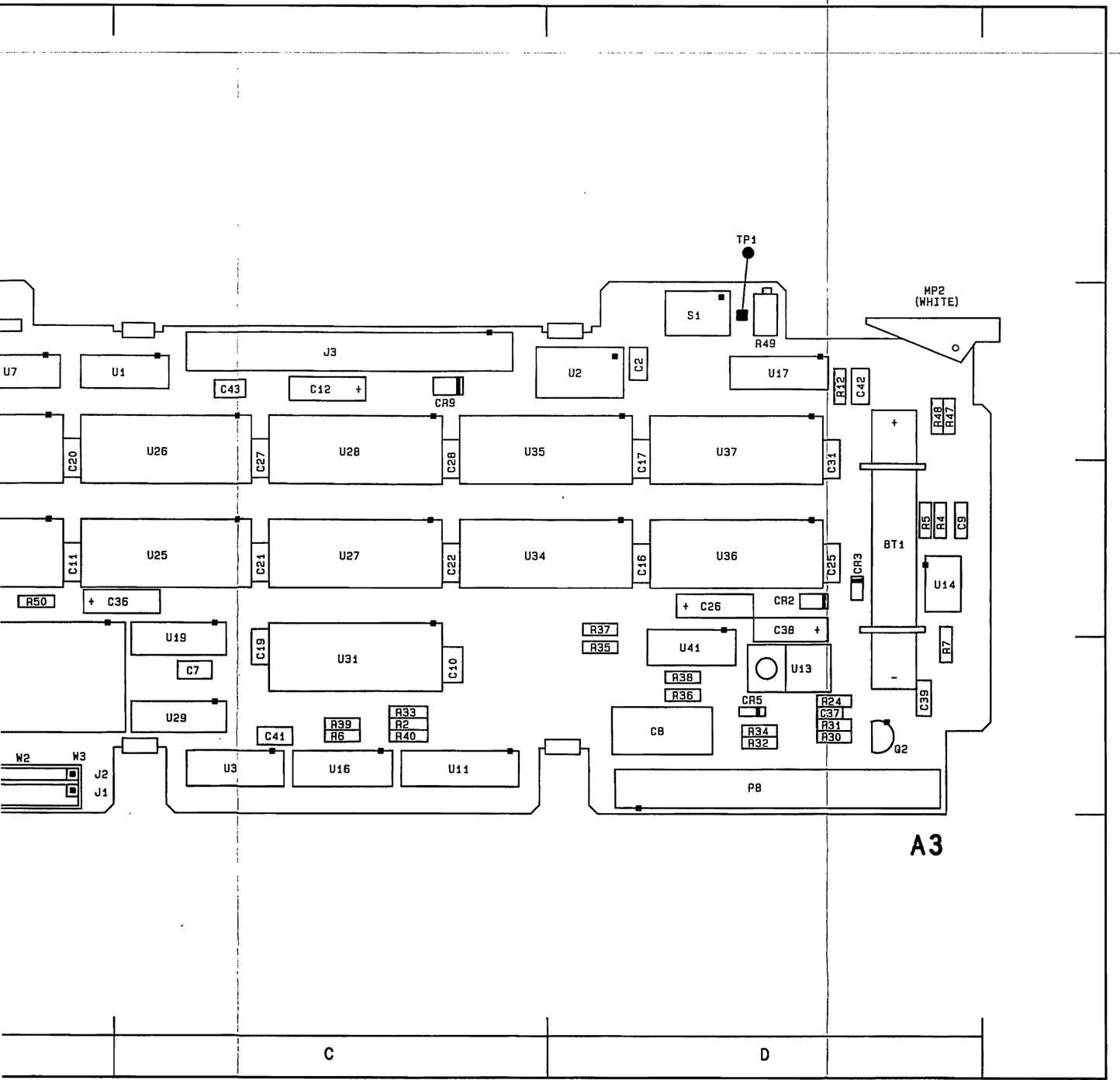
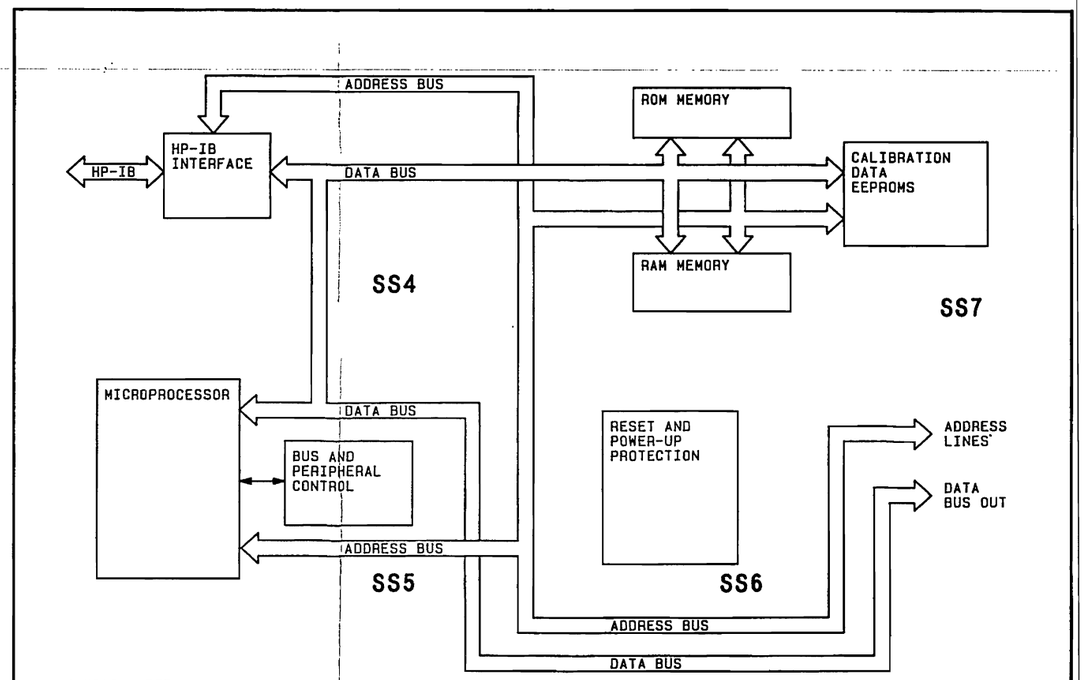


Figure 8F-106. SERVICE SHEET 6 INFORMATION

Component Locator



Component Locator



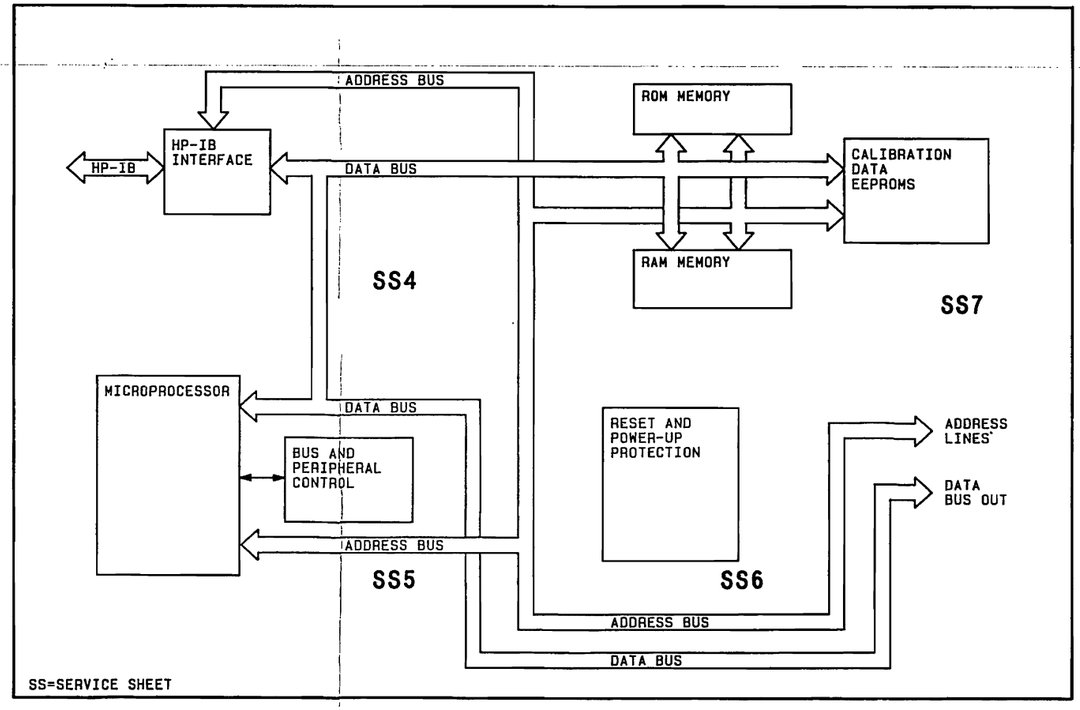
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C8	D, 3	U4	B, 1												
C9	D, 2	U7	B, 1												
		U9	A, 1												
CR5	D, 3	U14	D, 2												
		U15	A, 2												
J1	B, 3	U29	C, 3												
J3	C, 1	U40	A, 1												
		U41	D, 3												
MP1	A, 1														
MP2	D, 1	W3	B, 3												
Q2	D, 3														
R4	D, 2														
R5	D, 2														
R7	D, 3														
R30	D, 3														
R31	D, 3														
R32	D, 3														
R33	C, 3														
R34	D, 3														
R35	D, 3														
R36	D, 3														
R37	D, 2														
R38	D, 3														
R47	D, 1														
R48	D, 1														
R49	D, 1														
TP1	D, 1														

P/O A3 PROCESSOR/ MEMORY MODULE **SS5**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C8	D, 3	U4	B, 1														
C9	D, 2	U7	B, 1														
		U9	A, 1														
CR5	D, 3	U14	D, 2														
		U15	A, 2														
J1	B, 3	U29	C, 3														
J3	C, 1	U40	A, 1														
		U41	D, 3														
MP1	A, 1																
MP2	D, 1	W3	B, 3														
Q2	D, 3																
R4	D, 2																
R5	D, 2																
R7	D, 3																
R30	D, 3																
R31	D, 3																
R32	D, 3																
R33	C, 3																
R34	D, 3																
R35	D, 3																
R36	D, 3																
R37	D, 2																
R38	D, 3																
R47	D, 1																
R48	D, 1																
R49	D, 1																
TP1	D, 1																

P/O A3 PROCESSOR/
MEMORY MODULE

SS5

SEE REVERSE SIDE

Notes:

1. Each module in the HP 8642 has a nine digit module indentification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
3. W3 is a single contact blue post connector. It connects J1 pin 1 to J2 pin 1 in normal operation. To disconnect runaway reset, move W3 over to connect J1 pin 1 to J1 pin 2. J1 pin 2 is a TTL High.

CHANGES

2613A and above

On the schematic:

- In the upper left portion of the schematic change the A3 part number to 08642-60224.

P/O J3

RESET STATUS DETECTION

ADDRESS ERROR DETECTOR

U15 +5V(F1) 16 X/Y

PROC STATUS 5 MI 3
FC0 1
FC1 2
FC2 6
G 4 5
EN 8

0 15 NC
1 14
2 13
3 12
4 11
5 10
6 9
7 7
NC

U40D 13 12 11
U40C 9 10 8
U4F 18 19 17
U7C +5V(F1) 14 9 10 8 7
RUNAWAY RESET

U9D 9 8
U7D 12 13 11

ADDRESS STROBE 5 MM

U29 +5V(F1) 16 X/Y

BUS GRANT 5 MJ
BG 1
A20 2
A21 3
G 6
EN 4
A22 4
A23 5
8

0 15 NC
1 14
2 13
3 12
4 11
5 10
6 9
7 7
NC

ERROR DET 5 MK A20-A22 4
UNUSED ADDRESS DET 5 MP

LOW VOLTAGE DETECTOR

NC
R49 2k 3 CW 2 1
LOW VOLTAGE ADJ.
TP1
+5V(F1)
C9 0.1μ
R48 10k
U14 7 1 2 NC 5
8
R47 1k
6
4 3
+5V(F1)
R4 16.2k
R7 750k
R5 16.2k

RUNAWAY RESET DISCONNECT

P/O J2 1
W3 (NOTE 3)
P/O J1 1 2
TTL HIGH 2 4,5 MC

CONTROLLER RESET

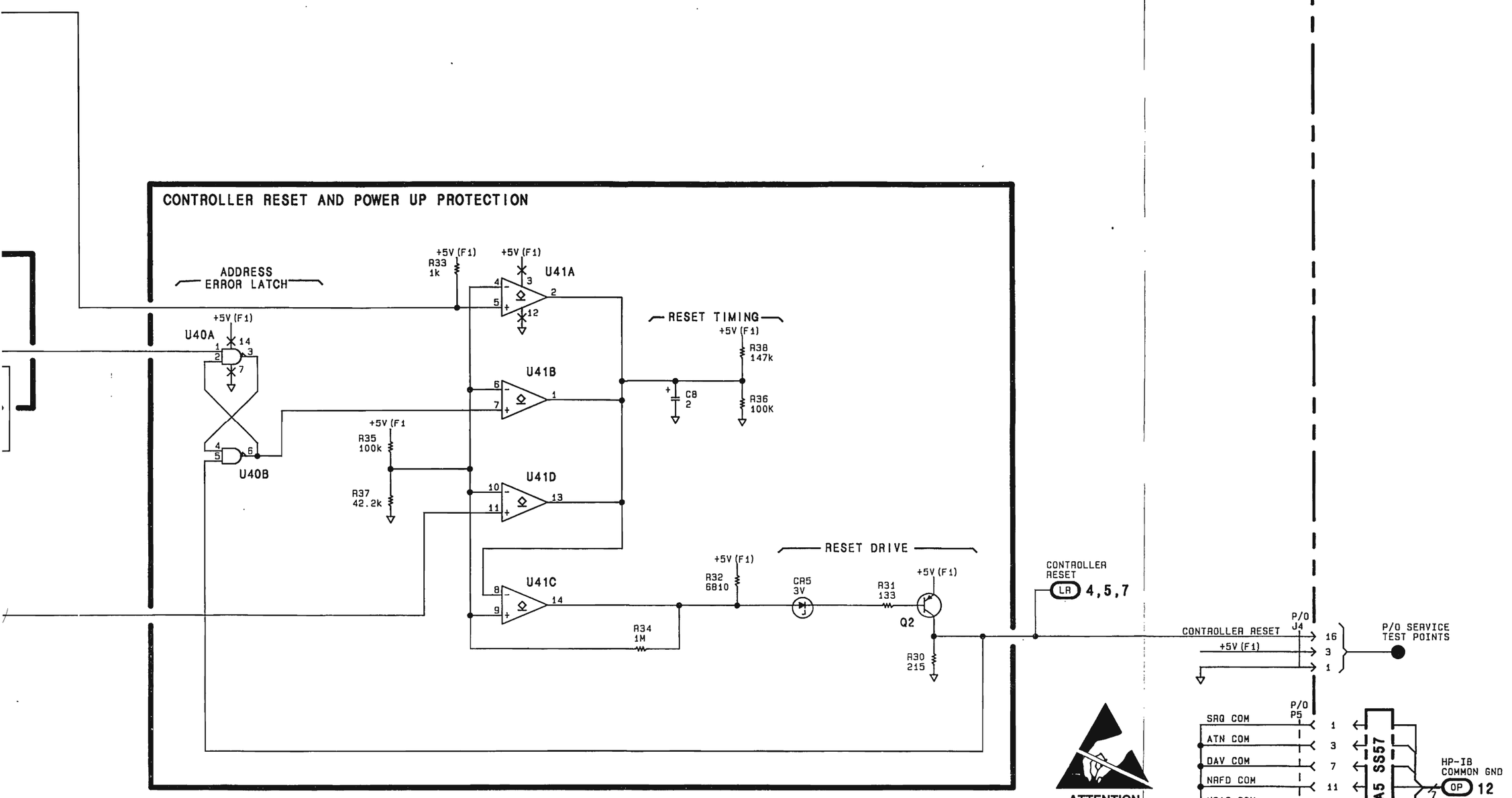
ADDRESS ERROR LATCH

+5V(F1)
U40A 1 2 14 3 7
U40B 4 5 6

POWER SUPPLY AND GND

POWER SUPPLY AND GND 4 LN 2
+5V(F1) +5V(F1)
GND
GROUND PZ 7

SERIAL PREFIX: 2427A



SS6
Figure 8F-107
8F-107

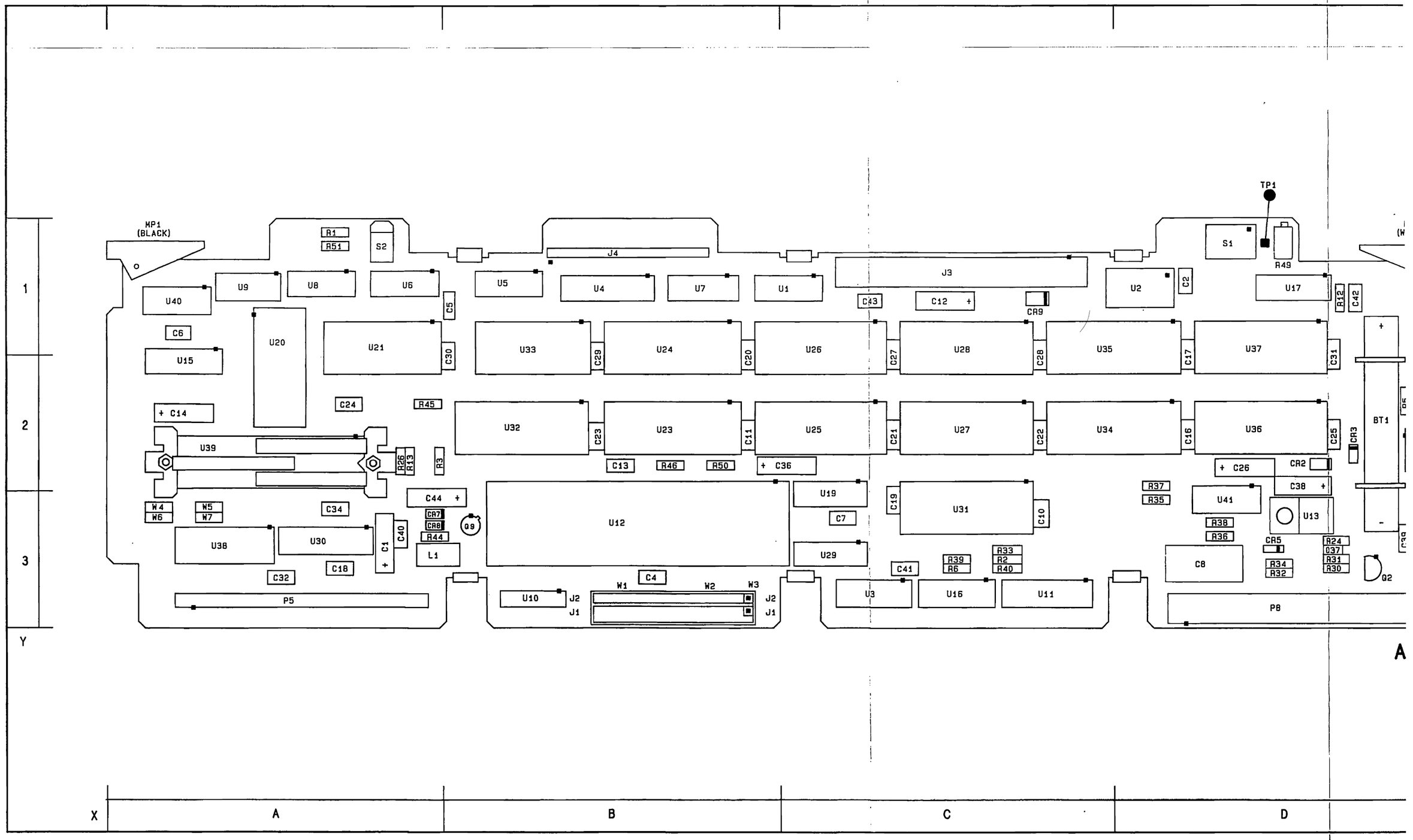
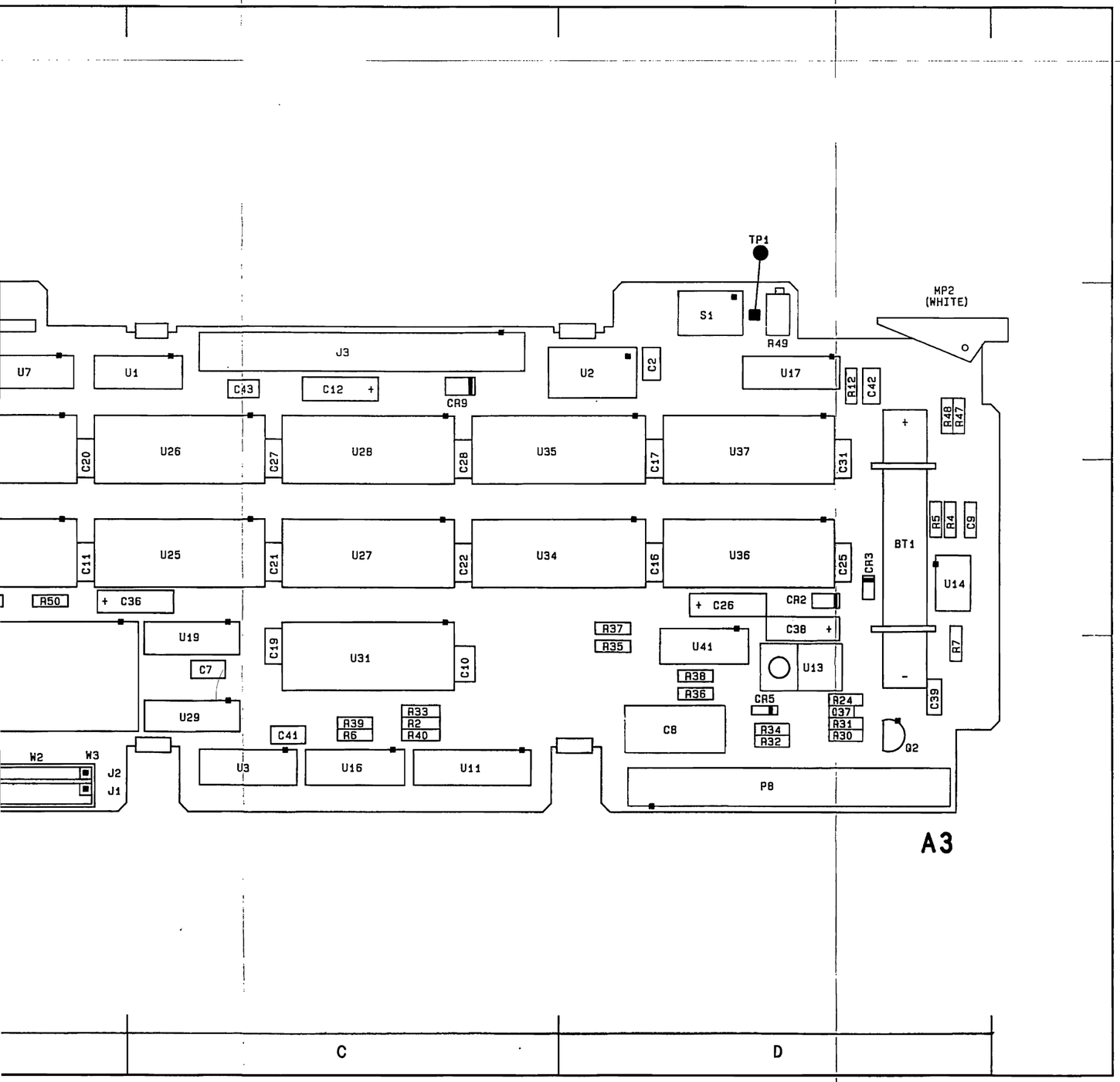
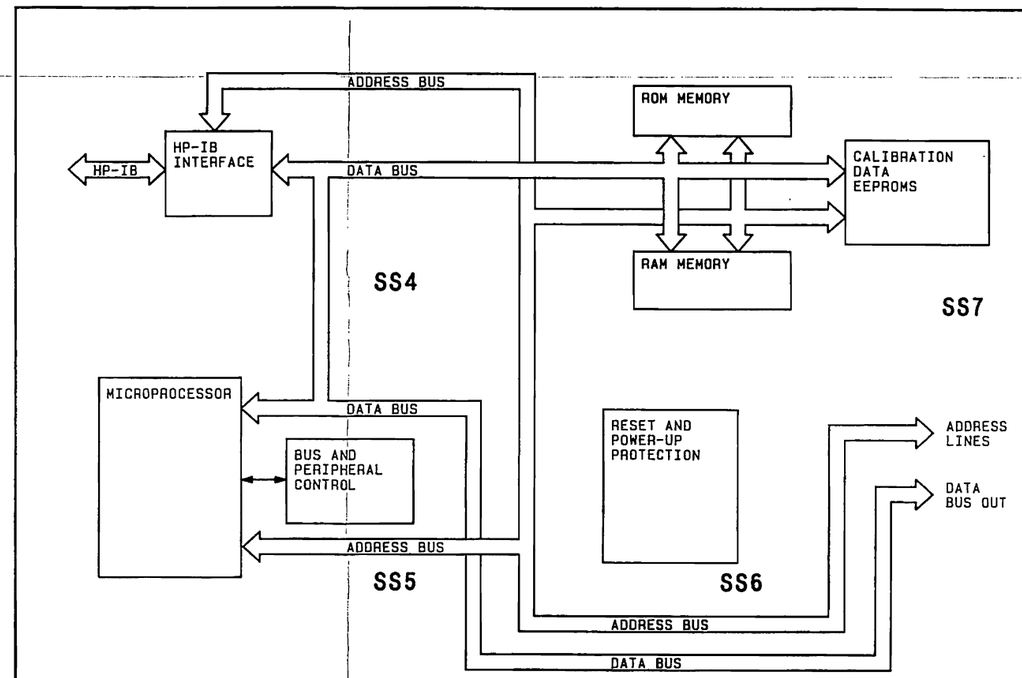


Figure 8F-108. SERVICE SHEET 7 INFORMATION

Component Locator



Component Locator



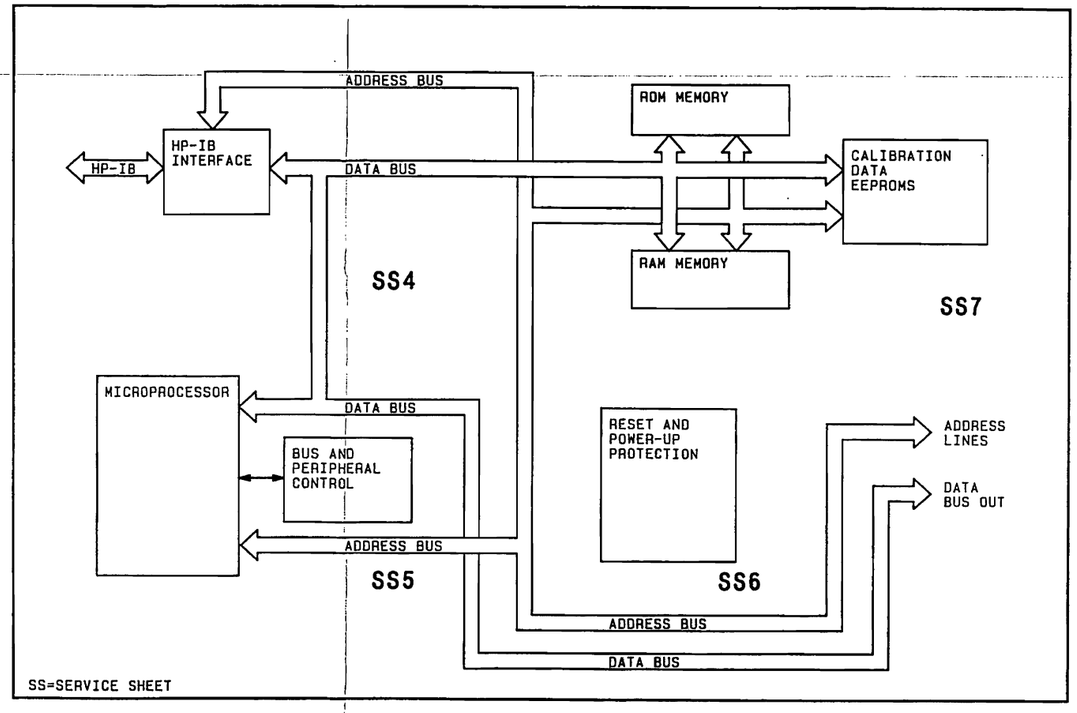
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
BT1	D, 2	U1	B, 1												
		U13	D, 3												
C11	B, 2	U20	A, 1												
C16	D, 2	U21	A, 1												
C17	D, 1	U23	B, 2												
C20	B, 1	U24	B, 1												
C21	C, 2	U25	C, 2												
C22	C, 2	U26	C, 1												
C23	B, 2	U27	C, 2												
C24	A, 2	U28	C, 1												
C25	D, 2	U32	B, 2												
C26	D, 2	U33	B, 1												
C27	C, 1	U34	C, 2												
C28	C, 1	U35	C, 1												
C29	B, 1	U36	D, 2												
C30	B, 1	U37	D, 1												
C31	D, 1														
C37	D, 3														
C38	D, 2														
C39	D, 3														
CR2	D, 2														
CR3	D, 2														
CR9	C, 1														
MP1	A, 1														
MP2	D, 1														
R24	D, 3														
R51	A, 1														
S1	D, 1														
S2	A, 1														

P/O A3 PROCESSOR/ MEMORY MODULE **SS6**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
BT1	D, 2	U1	B, 1												
		U13	D, 3												
C11	B, 2	U20	A, 1												
C16	D, 2	U21	A, 1												
C17	D, 1	U23	B, 2												
C20	B, 1	U24	B, 1												
C21	C, 2	U25	C, 2												
C22	C, 2	U26	C, 1												
C23	B, 2	U27	C, 2												
C24	A, 2	U28	C, 1												
C25	D, 2	U32	B, 2												
C26	D, 2	U33	B, 1												
C27	C, 1	U34	C, 2												
C28	C, 1	U35	C, 1												
C29	B, 1	U36	D, 2												
C30	B, 1	U37	D, 1												
C31	D, 1														
C37	D, 3														
C38	D, 2														
C39	D, 3														
CR2	D, 2														
CR3	D, 2														
CR9	C, 1														
MP1	A, 1														
MP2	D, 1														
R24	D, 3														
R51	A, 1														
S1	D, 1														
S2	A, 1														

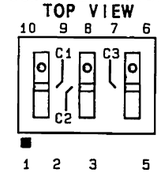
P/O A3 PROCESSOR/ MEMORY MODULE **SS6**

SEE REVERSE SIDE

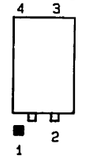
Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

A3 S1 COMPONENT SIDE TOP VIEW



A3 S2 COMPONENT SIDE TOP VIEW



CHANGES

All serial prefixes

On the schematic:

- U23-28, U32, U33 - In **ROM MEMORY**, change pin 28 to +5V(F1).
- U20, U21 - In **CALIBRATION DATA EPROMS** change pin 24 to +5V(F1).

2526A and above

On the schematic:

- In **POWER SUPPLY AND GND**, add a power supply line from the anode of CR3, and label it +5V(F3).

2613A and above

On the schematic:

- In the upper left portion of the schematic change the A3 part number to 08642-60224.

P/O A3 MICROPROCESSOR/MEMORY MODULE (08642-60124)

P/O A5 DISTRIBUTION ASSY (08642-60126) SS58

SERIAL PREFIX: 2427A

ROM MEMORY

U23 EPROM 32k X 8 — +5V (F2) — C11 0.1µ
U24 EPROM 32k X 8 — +5V (F2) — C20 0.1µ
U25 EPROM 32k X 8 — +5V (F2) — C21 0.1µ
U26 EPROM 32k X 8 — +5V (F2) — C27 0.1µ

+5V (F2) — CR9

ROM1 SEL — ROM1 SEL — ROM2 SEL — ROM2 SEL — ROM3 SEL

DATA BUS 4,5 MB
MEMORY ADDRESS BUS 5 ML
MEMORY SELECT 5 MO
OUTPUT ENABLE 4,5 LP

RAM MEMORY

U34 RAM 8192 X 8 — +5V (F2) — C16 0.1µ
U35 RAM 8192 X 8 — +5V (F2) — C17 0.1µ

RAM1 SEL — RAM1 SEL — RAM2 SEL

CONTROLLER RESET 4,5,6 LR
LWR, UWR 5 MN

POWER SUPPLY AND GND

+5V UNREG 53 OQ
P/O P8 +5V UNREG
VOLTAGE REGULATOR U13 — C39 0.1µ — C38 10µ — CR3 — CR2 — +5V (F2) — C37 0.01µ
GROUND 6 PZ

BATTERY AND DISCONNECT SWITCH
BT1 3.6V
R24 348
P/O S1

U25 EPROM 32k X 8 — +5V (F2) — C21 0.1µ
U26 EPROM 32k X 8 — +5V (F2) — C27 0.1µ
U27 EPROM 32k X 8 — +5V (F2) — C22 0.1µ
U28 EPROM 32k X 8 — +5V (F2) — C28 0.1µ
U32 EPROM 32k X 8 — +5V (F2) — C23 0.1µ
U33 EPROM 32k X 8 — +5V (F2)

ROM2 SEL
ROM3 SEL
ROM3 SEL
ROM4 SEL
ROM4 SEL
ROM3
D8-D15
A1-A11
EEPROM SEL

U34 RAM 8192 X 8 — +5V (F2) — C16 0.1µ
U35 RAM 8192 X 8 — +5V (F2) — C17 0.1µ
U36 RAM 8192 X 8 — +5V (F2) — C25 0.1µ
U37 RAM 8192 X 8 — +5V (F2) — C31 0.1µ

RAM1 SEL
RAM1 SEL
RAM2 SEL
RAM2 SEL

CALIBRATION DATA EEPROMS

U20 EEPROM 204

D0-D7

EEPROM OUTPUT ENABLE
5 LZ

WRITE DISABLE
+5V (F2)
A51 1k
S2
U1D
U1C
EEPROM WE
LWR
UWR
BATTERY SENSE

U27 EPROM 32k X 8 — +5V (F2) — C22 0.1µ — A 0/32767 — ROM3 SEL — [VPP]

U28 EPROM 32k X 8 — +5V (F2) — C28 0.1µ — A 0/32767 — ROM4 SEL — [VPP]

U32 EPROM 32k X 8 — +5V (F2) — C23 0.1µ — A 0/32767 — ROM4 SEL — [VPP]

U33 EPROM 32k X 8 — +5V (F2) — C29 0.1µ — A 0/32767 — [VPP]

D0-D7

D8-D15

A1-A11

EEPROM SEL

RAM2 SEL

UWR

LWR

CALIBRATION DATA EEPROMS

U36 RAM 8192 X 8 — +5V (F2) — C25 0.1µ — A 0/8191 — [WRITE] [READ] C1

U37 RAM 8192 X 8 — +5V (F2) — C31 0.1µ — A 0/8191 — [WRITE] [READ] C1

U20 EEPROM 2048 X 8 — +5V (F2) — C24 0.1µ — A 0/2047 — G1 — C2 (READ) — EN (BYTE WRITE)

U21 EEPROM 2048 X 8 — +5V (F2) — C30 0.1µ — A 0/2047 — G1 — C2 (READ) — EN (BYTE WRITE)

EEPROM OUTPUT ENABLE — 5 LZ

WRITE DISABLE — +5V (F2) — R51 1k — S2 — EEPROM WE — U1D — U1C — UWR

BATTERY SENSE

ATTENTION
Static Sensitive Devices

P/O A5 DIST. ASSY SS58

BATTERY SENSE — P/O P8 — 2 — BATT SENSE — KL — 10

EEPROM WE — 1 — EEPROM WE — KI — 9

SS7
Figure 8F-109
8F-109

A4 Module

Troubleshooting and Adjustment Contents

Troubleshooting

NOTE

Input latches, SS9, are checked when troubleshooting the keyboard Module A1.

Output latches, SS11, are checked when troubleshooting modules the data is sent to. Diagnostics will determine what module failed. The latched data for the failed module is checked as part of the module checks.

When the data to each module is checked, the data bits are set to TTL high or low from the front panel.

Check 3 gives you the equation to determine the data to set each bit. Some data bits are not latched TTL high or low but are pulsed.

Adjustments

Troubleshooting

A4 TROUBLESHOOTING INFORMATION

Before Proceeding with Module Troubleshooting

- You should have confidence that A4 is the faulty module from Module Level Diagnostics (MLD) results. (Refer to Instrument Level Troubleshooting, HP 8642 Service Manual.)
- Open the HP 8642 Service Manual to Figure 8G-100. There are 3 diagrams of the A4 Latch Module. One is the Simplified Block Diagram.
- Open the foldout on page 8G-101 (BD4). There, you will see a more detailed Block Diagram of the Latch Module. This Troubleshooting Block Diagram is meant to be used during all checks.
- The objective of Troubleshooting checks is to isolate the malfunction to an area of circuitry represented on one Service Sheet. The checks are intended to be done in the order they are numbered.

Overall Equipment List

Digital Voltmeter (DVM) ..... HP 3456A
Logic Probe HP545A

Essentials of A4 Module Operation

NOTE

The A3 Processor/Memory Module must be operating to control and pass data to and from the A4 Module.

The A4 Latch module consists of Transceivers, I/O Decoders, and I/O Latches to send data to the Microprocessor and to receive data from the Microprocessor for the modules. The Voltmeter, X-Axis Sweep and Out-of-Lock Detect are also part of the module.

The Bus Transceiver and I/O Decoder are shown on Service Sheet 8. The Bus Transceiver sends and receives 16 bits of data to and from the Microprocessor. The I/O Decode decodes addresses A1 through A7 to select one of six Input Latches (Service Sheet 9), one of twelve Output Latches (Service Sheet 11), X-Axis Sweep DAC,(Service Sheet 11), or Voltmeter DAC (Service Sheet 10).

The Input Latches receive keyboard, HP-IB and Interrupt data for the Microprocessor. The Microprocessor controls the latching and sending of the data over the Data Bus. The Output Latches receive data from the Microprocessor. Data received controls the instrument modules.

CHECK 1: POWER SUPPLIES (SS8)

Essentials of SS8 Circuit Operation

Refer to BD4 Figure 8G-101. Located on SS8 you will find the Bus Transceivers, I/O Decode and Power Supply. The Transceivers and I/O Decode are checked in Check 2. Check 1 checks that the Power Supply Voltage to the A4 Module are correct.

Required Equipment:

Digital Voltmeter (DVM) HP3456A

Test the A4 Module Power Supplies

1. Setup:

   Set the HP 8642A/B POWER switch to standby.

   Remove the top cover.

   Use the module locator diagram on the inside of the top cover to locate the A4 module.

   The Power Supply Voltages are measured at the Service Connector J1 located at the upper right hand corner of the module.

   Set the HP 8642A/B POWER switch to ON.

2. Measure Voltage Level:

   Check the Power Supply Voltages to the A4 Module as shown in Table 8G-1.

Table 8G-1.

J1 Pin	Vdc
1	+15
2	−15
4	+5

CHECK 2: X-AXIS SWEEP, VOLTMETER, TRANSCEIVERS AND OUTPUT LATCH U7

Essentials Of Check 2 Operation

Refer to BD4 Figure 8G-101. Located on SS8 you will find the Transceivers and I/O Decode. The Transceiver receives data for the Voltmeter select Latch U7 (SS11), the X-Axis Sweep DAC (SS11) and the Voltmeter DAC (SS10). The I/O Decode selects the Latch or DAC to receive the data.

Description of Check 2

A firmware routine sends data from the A3 Module to set the voltage output of the X-Axis Sweep at nine different points and measures the voltage using the Internal Voltmeter. The Voltmeter Inputs of +10V Ref, Ground and Battery are also checked.

Procedure

1. Setup:

   Preset the 8642. [INSTR PRESET] [SHIFT]

   Hold shift key until 100,000000 MHz −140.0 DM appears, to override the 20 second reset test.

   Enter [SHIFT] [SPCL], OFF. ENTER NUMBER .PO is displayed.

   Enter [3], ENTERING SERVICE MODE. I25 is displayed.

   Enter [3] [1] [0] [Hz] to initiate the test.

   DIAG DONE HIT MSSG .V1 is displayed. Use [MSSG] to scroll through messages.

   ERROR CODE A04 FAILED .L_is displayed. L_is the Error or Message Code.

   A complete list of Messages is shown in Table 8G-2, A4 Module Messages.

Table 8G-2. *A4 Module Messages*

Message Code	Meaning
L7	+10V Ref not between 9.8 and 10.2 Volts
L8	Gnd not between −0.2 and 0.2 Volts
L10	X-Axis voltages not between −0.4 and 0.4 Volts
L11	X-Axis voltages not between 1.6 and 2.4 Volts
L12	X-Axis voltages not between 2.6 and 3.4 Volts
L13	X-Axis voltages not between 3.6 and 4.4 Volts
L14	X-Axis voltages not between 4.6 and 5.4 Volts
L15	X-Axis voltages not between 4.6 and 5.4 Volts
L16	X-Axis voltages not between 5.6 and 6.4 Volts
L17	X-Axis voltages not between 6.6 and 7.4 Volts
L18	X-Axis voltages not between 7.5 and 8.3 Volts
L19	X-Axis voltages not between 8.5 and 9.3 Volts
L20	X-Axis voltages not between 9.4 and 10.3 Volts
L21	Battery Voltage < 1.0 Volts or > 4.5 Volts
L22	Battery Voltage ≥ 1.0 Volts and ≤ 3.5 Volts
L23	Test 1 of A04 PASSED
L24	Test 1 of A04 FAILED

CHECK 3: CHECK EACH LATCH BIT

Essentials of Check 3 Operation

Refer to BD4 Figure 8G-101. Located on SS11 you will find the Output Latches. The A3 Processor/Memory Module must be operating to control and pass data to to and from the A4 Module. The A1 keyboard/LCD Display Module must be all right and the A4 Module Input Latches (SS9). The A4 Module Transceivers and I/O Decode (SS8) must send data to the latches and select the latch to receive the data.

Description of Check 3

Data is entered from the Front Panel to select the latch and to set a latch bit high or low.

Determine Data To Send

1. Equation:

   (Bit Number) + (Latch Number) * 8 = data

   Bit Number = 0 through 7 for data bits D0 through D7, and for data bits D_8 through D_{15}. (D_8 = 0, D_{15} = 7).

   Latch Number = 1 through 12 for Latch enable L_1 through L_{12}, for L_{21} the Latch Number is 9.

   Example: Data bit is D8, Bit Numbers = 0 latch enable is L8 (U19), Latch Number = 8 (0) + (8)(8) = 64

Check High State

[SHIFT] [SPCL] [3] [6] [0] [1] [6] [4] [Hz]

Latch U19, Pin 2 is set high.

[6] [0] [1] sets the latch bit high.

Check Low State

[SHIFT] [SPCL] [3] [6] [0] [2] [6] [4] [Hz]

Latch U19, Pin 2 is set low.

[6] [0] [2] sets the latch bit low.

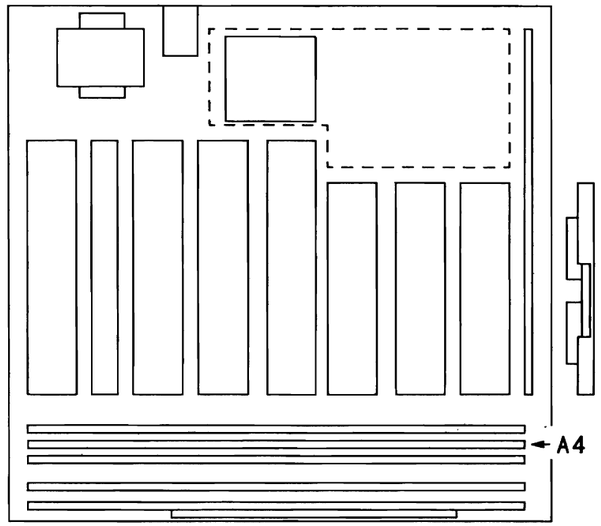
NOTE

Latches U9 and U11, Display Bits, outputs can not be set High or Low. They pulse each time a key is pressed.

When latch U18 output at pin 9 is set low (K8 RESET KEYS) the keyboard is disabled. Instrument must be cycled OFF and ON to clear. Latch U11 outputs will turn on all displays all segments. Instrument must be Preset to clear.

Latch U13, a loop unlocked will prevent a bit from being latched. Output bit will pulse.

Assembly Locator



Simplified Block Diagram

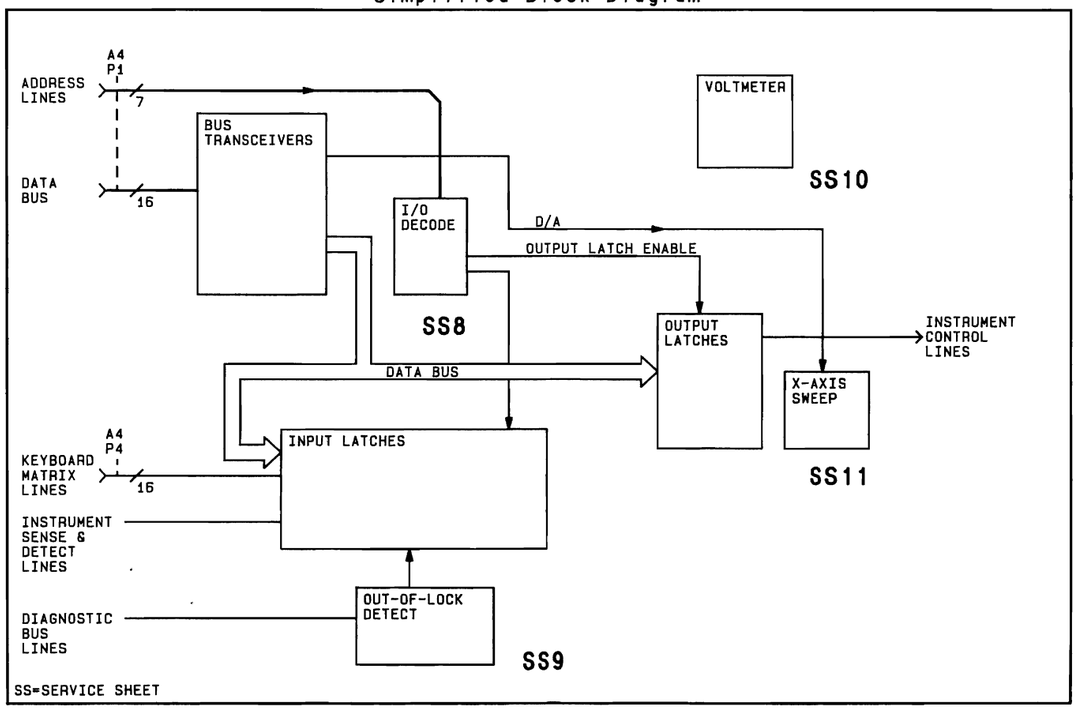
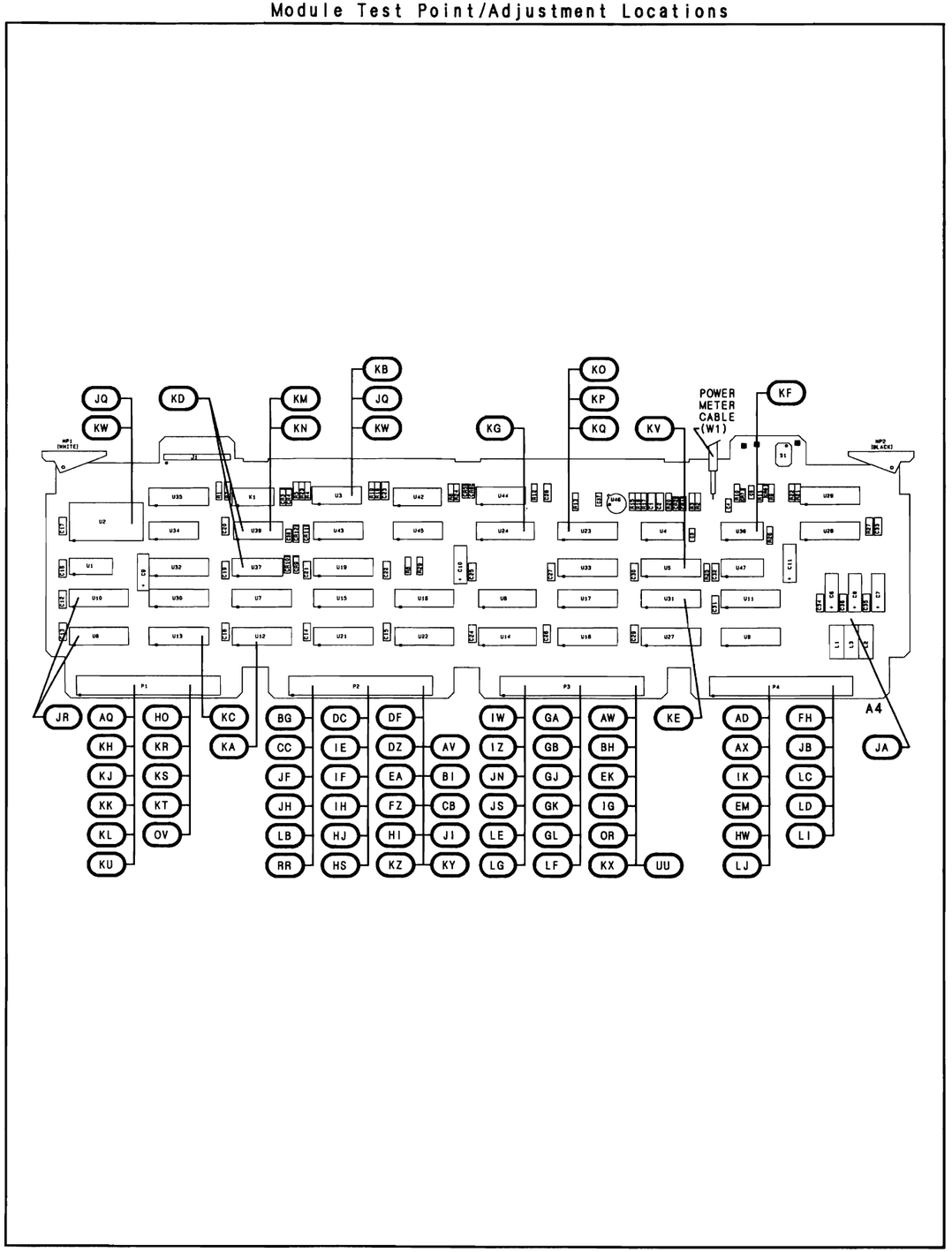


Figure 8G-100 BD4 General Information.

Module Test Point/Adjustment Locations



A4 LATCH MODULE (08642-60125)

BUS TRANSCEIVERS

I/O DECODE

INPUT LATCHES

POWER SUPPLY AND GND

ADDRESS LINES BD3 KR → P/O P1 31–37 A1–A7 (7)

R/W BD3 KS → P/O P1 19 R/W

ADDRESS DECODE BD3 KT (3) → P/O P1 21–23 LATCHES (L), A/D (L), D/A (L)

DATA BUS OUT BD3 KU (16) → P/O P1 2–17 D0–D15

POWER SUPPLY BD17 JB (3) → P/O P4 49, 47, 48, 50 +15V, +5V, -15V

GROUND 60 TS → P/O P3 11-13, 19-21, 25, 27, 29-31, 34-36, 38, 41, 47 GND

OUTPUT EN BD3 KJ → P/O P1 25

HP-IB SWITCH OUTPUTS BD2 AD (8) → P/O P4 1, 3, 14, 22, 6, 5, 4, 2 "1", "4", X2, X1, X3, "16", "8", "2"

KEYBOARD MATRIX LINES BD2 AX (16) → P/O P4 37–44, 29–34 ROW 0–7, COL 0–5

RPG DIR BD2 EM → P/O P4 28 RPG DIR

DISP BUSY (L) BD2 FH → P/O P4 24 DISP BUSY (L)

SERIAL PREFIX: 2427A

ATN LEVEL/BAND LOCK BD17 GL (2) → P/O P3 42, 46 ATN BAND LOCK, ATN LEVEL LOCK

MOD HI BD6 GB → P/O P3 43 MOD HI

COUNTER OUTPUT BD8 KJ → P/O P3 45 COUNTER OUTPUT

OVEN SENSE BD17 IZ → P/O P3 44 OVEN SENSE

FN LOW SWEEP LIMIT BD10 UU → P/O P3 37 FN LSL

ATN REV PWR INT BD17 IW → P/O P3 39 RPP INT

MOD HI LO INT BD6 GA → P/O P3 40 MOD HI LO INT

RPG CHANGE (L) BD2 HW → P/O P4 26 RPG CHANGE (L)

KEY DWN (L) BD2 IK → P/O P4 45 KEY DWN (L)

EEPROM WE BD3 KI → P/O P1 50 EEPROM WE

POWER SUPPLY AND GND 8 JA → +15V (F1), +5V (F1), -15V (F1)

MODULATION DIAG. BUS BD6 FZ → P/O P2 13 MOD

FM LOOP DIAG. BUS BD8 IE → P/O P2 7 FM OOL

REF LOOP DIAG. BUS BD11 DF → P/O P2 10 REF OOL

SUM LOOP DIAG. BUS BD12 EA → P/O P2 6 SUM OOL

DOUBLER DIAG. BUS BD16 JF → P/O P2 8 DBLR

OUTPUT SEC. DIAG. BUS BD14 HJ → P/O P2 12 OS OOL

HET REF DIAG. BUS BD15 HS → P/O P2 11 HET OOL

SAWR LOOP DIAG. BUS BD9 BH → P/O P3 32 SAWR OOL

TIMEBASE DIAG. BUS BD7 AW → P/O P3 28 TB OOL

IF REF DIAG. BUS BD10 JN → P/O P2 7 FN OOL

OUT-OF-LOCK DETECT

INTERRUPT DETECT

CNT INT DIS

OOL MASK

TTL HIGH

OOL RESET (L)

LB INT → P/O P1 27 KH

LLWR, LHWR → P/O SERVICE CONNECTION → BD3 KX (2)

VM → 7, 9, 4, 8

SS9

DAWR BD3 KK → P/O P1 41

SAWR SENSE 1, 2 BD9 BG (2) → P/O P2 2, 9 S1, S2

EXT REF SENSE BD7 AV → P/O P2 4

BATT SENSE BD3 KL → P/O P1 49 W1

VM MUX 0-3

VOLTMETER INPUTS

TO VM

X AXIS SENSE

POWER SUPPLY AND GND → +15V (F1), +5V (F1), -15V (F1)

POWER SUPPLY AND GND 8 JA (4)

P/O J1 SA QUAL 6, +15V (F1), +5V (F1), -15V (F1), GND

P/O SERVICE CONNECTIONS

POWER SUPPLY AND GND 9, 10, 11 JA (4)

A/D, D/A, OUTPUT LATCH EN, TTL HIGH

INPUT LATCH EN (6)

VM TEST BIT

VM DAT

KA, KB, KC, KD, KE, KF, KP, KQ

JA, JB, JR

SS8

Scans by ArtekMedia => 2009

DAWR
BD3 KK → 41 P/O P1

SAWR SENSE 1,2
BD9 BG → 2 → 2, 9 → 9 P/O P2 S1, S2

EXT REF SENSE
BD7 AV → 4

BATT SENSE
BD3 KL → 49 P/O P1 W1

P/O J1 6
P/O SERVICE CONNECTIONS

VM MUX 0-3
TO VM
X AXIS SENSE

VOLTMETER INPUTS

INTERNAL VOLTMETER

POWER SUPPLY AND GND
8 JA → 4
+15V (F1)
+5V (F1)
-15V (F1)

SUPPLY
ND
9, 10, 11

KB KQ

SS10

KN KM
VM MUX 0-3
X AXIS SENSE

KV
D/A

KO
A/D
7

T LATCH EN
IGH

KD KW

KP
VM DATA

KE
VM TEST BIT

VM TEST BIT

KA KC KF KG
DAWR 2
DATA BUS
HET APP DIS
CNT INT DIS
OOL MASK
OOL RESET

OUTPUT LATCHES

X-AXIS

OUT-OF-LOCK DETECT
VM 7
4
9
8
INTERRUPT DETECT
CNT INT DIS
OOL MASK
TTL-HIGH
OOL RESET (L)
3

P/O SERVICE CONNECTIONS
4
LLWR, LHWR
BD3 KX → 2 → 48 P/O P3 LATCH UWR
→ 49 LATCH LWR

P/O P1 27 LB INT KH BD3

8 JA → 4
POWER SUPPLY AND GND
+15V (F1)
+5V (F1)
-15V (F1)

P/O P2
5 → LCD LIGHT ON KY BD2
1 → DOUBLER MUX JI BD16
HET MUX A → 3
HET MUX B → P/O P1 45
HET MUX SELECT LINES HO BD15
44 → TIME BASE DISABLE AQ BD7

P/O P2
SAWR A → 40
SAWR B → 42
SAWR OSC SELECT LINES BI BD9
DIV 2 → 37
DIVIDER CTRL LINE DIV 2 RR BD13
P/O P3
DIV 0 → 2
DIV 1 → 3
DIVIDER CTRL LINES DIV 0, 1 EK BD4
HET BD → 1
HET BAND JS BD15

P/O P2
OS CLK → 41
OS DATA → 43
OUTPUT SEC. CTRL LINES HI BD14
REF CLK → 45
REF DATA → 50
REF LOOP CTRL LINES DC BD11
SUM CLK → 49
SUM DATA → 48
SUM LOOP CTRL LINES DZ BD12
FM CLK → 46
FM DATA → 44
FM CTRL LINES IF BD8

MOD D0
MOD D1
MOD D2
MOD D3
MOD D4
MOD D5
MOD D6
MOD D7

SS9

INTERNAL VOLTMETER

SS10

VM MUX 0-3
X AXIS SENSE
D/A
VM TEST BIT
DAWR 2
DATA BUS
HET APP DIS
CNT INT DIS
OOL MASK
OOL RESET
LATCH UWR
LATCH LWR
OUTPUT LATCHES
KN KM KV KO KW

X-AXIS SWEEP
VM MUX 0-3
X-AXIS SENSE
D/A

SS11

P/O P2
DBL CLOCK 18
DBL DATA 19
FN H EXT CLK 14
FN H INV 15
FN C0 20
FN C1 21
FN C2 17
FN C3 16
FN OSC CON 38
ATN 0 24
ATN 1 25
ATN 2 27
ATN 3 36
ATN 4 34
ATN 5 28
ATN 6 26
HET SW CONTROL 23

DOUBLER CONTROL LINES JH BD16
FRACTIONAL N CONTROL LINES CB BD10
OSCILLATOR CONTROL ENABLE CC BD10
ATTENUATOR DRIVER CONTROL KZ BD17
HET SW CONTROL LB BD17

P/O J1
LLWR 6
LHWR 5
S.A. FLAG 7
J1-10 10
J1-11 11
J1-12 12
P/O SERVICE CONNECTORS

P/O P1
X-AXIS 43
Z-AXIS 39
Z AXIS, X AXIS OV BDX

P/O P4
C(H)/D(L) 16
SCK (L) 18
CSALL (L) 20
RESET LCD (L) 21
SI8 (H) 7
SI9 (H) 9
SI10 (H) 13
SI0 (H) 8
SI1 (H) 10
SI2 (H) 11
SI3 (H) 12
SI4 (H) 15
SI5 (H) 17
SI6 (H) 19
SI7 (H) 23
LCD DRIVER INPUTS LD BD2
LCD SERIAL IN DATA LC BD2

P/O P2
DATA OUT CLK 39
COUNTER CLOCK IH BD8
COUNTER CONTROL LINES IG BD8

P/O P3
COUNTED SIGNAL SEL 4
DATA OUT STROBE 5
COUNT PERIOD SEL 6
APP RESET 8
ATN LEVEL TRIG 16
ATN BAND TRIG 24
MOD CLK 26
HP-IB SC 50
APP RESET LE BD17
ATN LEVEL TRIG LF BD17
ATN BAND TRIG LG BD17
MODULATION CLK GJ BD6
HP-IB SC OR BD3

P/O P4
KB RESET RPG (L) 25
KB RESET KEYS (L) 46
KB RESET RPG (L) LI BD2
RESET KEYS (L LJ BD2

P/O P3
MOD D0 9
MOD D1 15
MOD D2 17
MOD D3 23
MOD D4 22
MOD D5 18
MOD D6 14
MOD D7 10
MODULATION ADDRESS/ DATA LINES GK BD6

P/O P2
OS CLK 41
OS DATA 43
REF CLK 45
REF DATA 50
SUM CLK 49
SUM DATA 48
FM CLK 46
FM DATA 44
OUTPUT SEC. CTRL LINES HI BD14
REF LOOP CTRL LINES DC BD11
SUM LOOP CTRL LINES DZ BD12
FM CTRL LINES IF BD8

P/O P2
SAWR A 40
SAWR B 42
DIV 2 37
SAWR OSC SELECT LINES BI BD9
DIVIDER CTRL LINE DIV 2 RA BD13

P/O P3
DIV 0 2
DIV 1 3
DIVIDER CTRL LINES DIV 0, 1 EK BD4

P/O P2
HET BD 1
HET BAND JS BD15

P/O P2
5 LCD LIGHT ON KY BD2
1 DOUBLER MUX JI BD16

P/O P1
HET MUX A 3
HET MUX B 45
HET MUX SELECT LINES HO BD15

P/O P2
44 TIME BASE DISABLE AQ BD7

8 JA

POWER SUPPLY AND GND
+15V (F1)
+5V (F1)
-15V (F1)

BD4

Figure 8G-101
8G-101

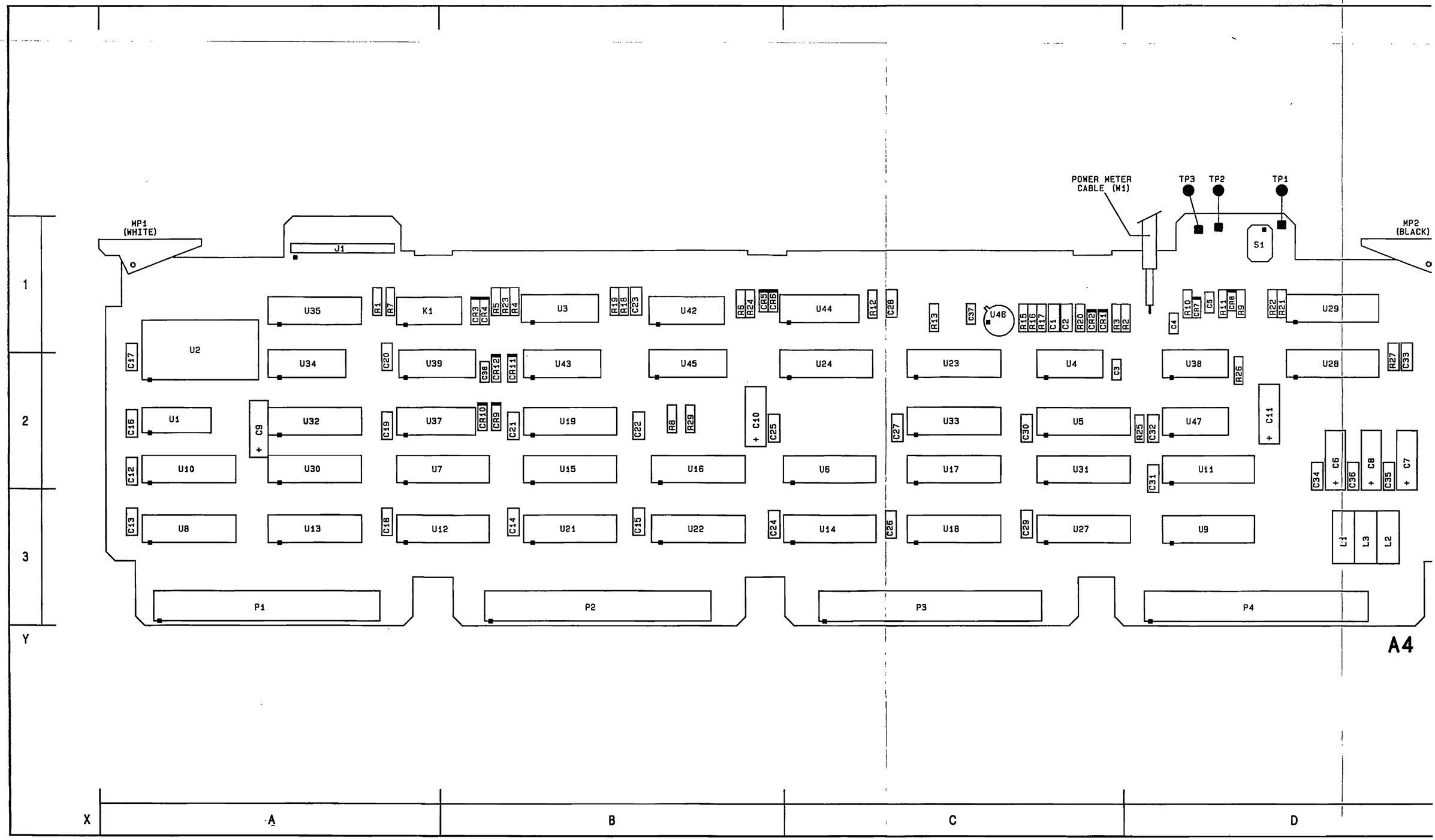
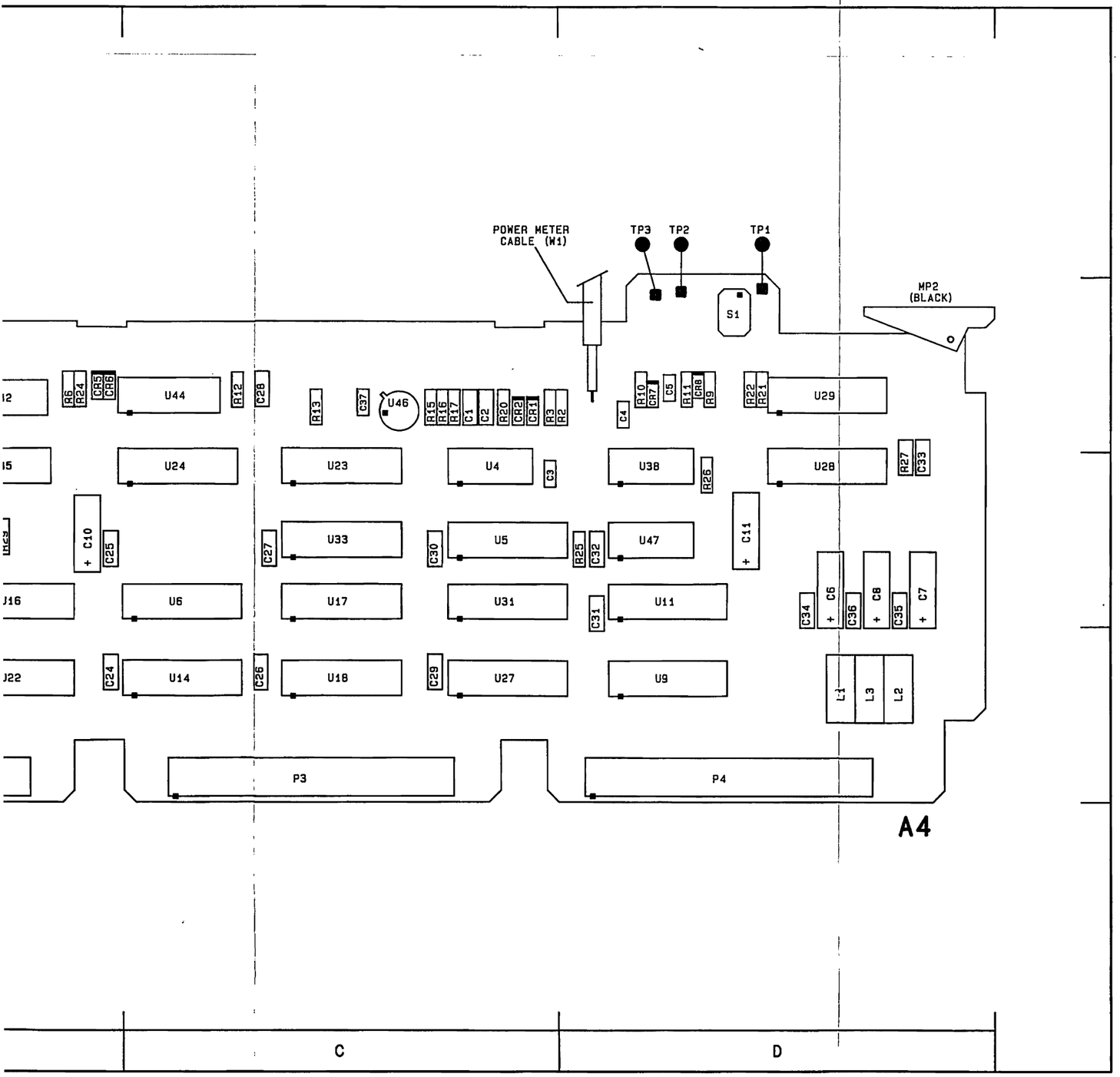
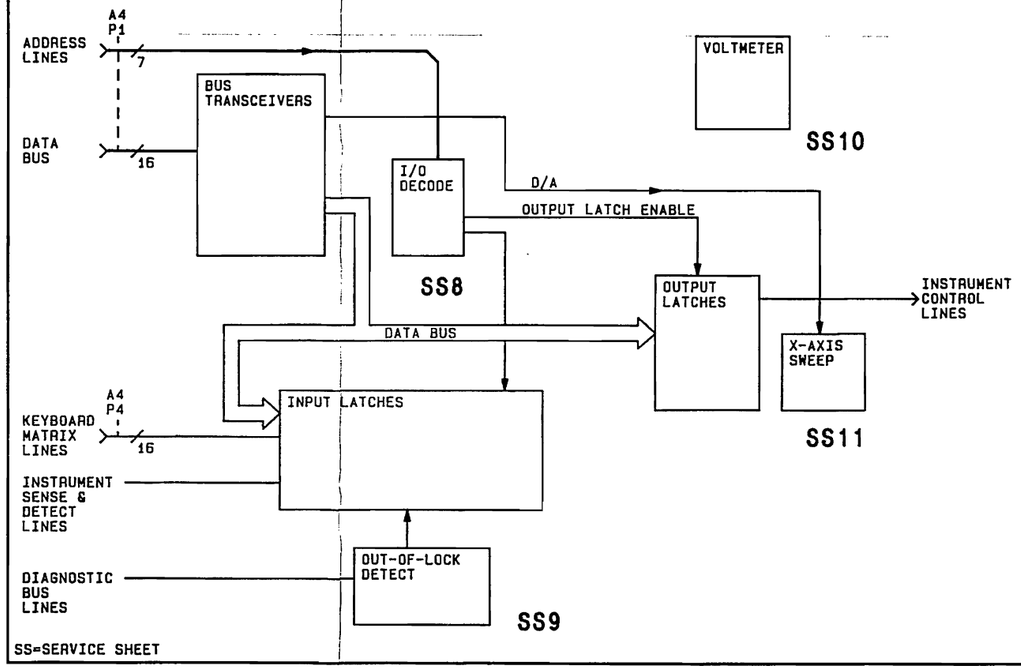


Figure 8G-102. SERVICE SHEET 8 INFORMATION

Component Locator



Component Locator



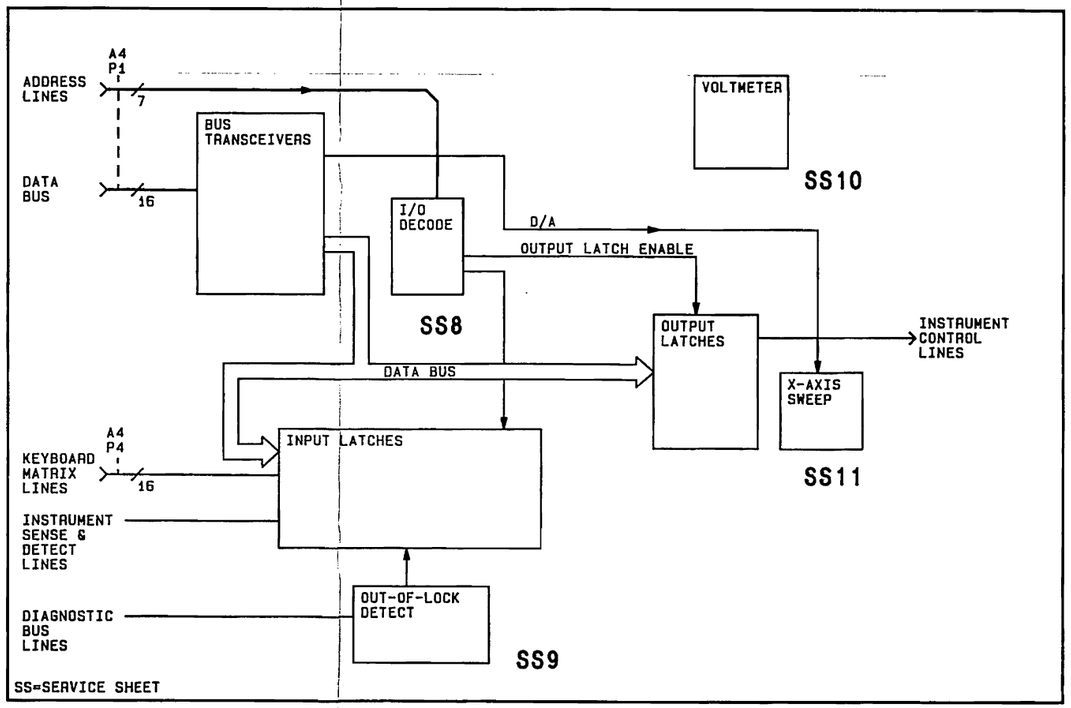
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C6	D, 2														
C7	D, 2														
C8	D, 2														
C9	A, 2														
C10	B, 2														
C11	D, 2														
C12	A, 2														
C13	A, 3														
C34	D, 2														
C35	D, 2														
C36	D, 2														
J1	A, 1														
L1	D, 3														
L2	D, 3														
L3	D, 3														
MP1	A, 1														
MP2	D, 1														
P1	A, 3														
P4	D, 3														
R8	B, 2														
U1	A, 2														
U2	A, 1														
U3	B, 1														
U8	A, 3														
U10	A, 2														

SEE REVERSE SIDE

A4 MODULE **BD4**



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C6	D, 2														
C7	D, 2														
C8	D, 2														
C9	A, 2														
C10	B, 2														
C11	D, 2														
C12	A, 2														
C13	A, 3														
C34	D, 2														
C35	D, 2														
C36	D, 2														
J1	A, 1														
L1	D, 3														
L2	D, 3														
L3	D, 3														
MP1	A, 1														
MP2	D, 1														
P1	A, 3														
P4	D, 3														
RB	B, 2														
U1	A, 2														
U2	A, 1														
U3	B, 1														
U8	A, 3														
U10	A, 2														

A4 MODULE **BD4**

SEE REVERSE SIDE

Notes:

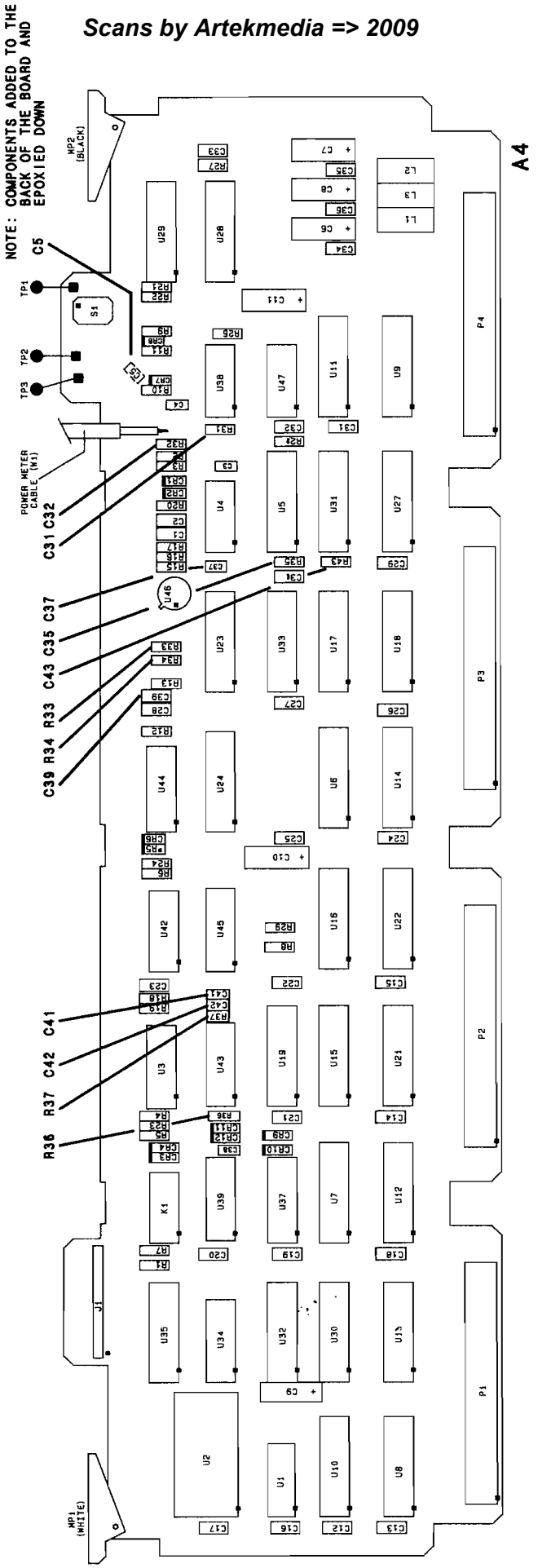
1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

CHANGES

All Serial Prefixes

On the schematic:

- C8 - In **POWER SUPPLY AND GND**, move the polarity symbol (+) to the ground side of C8.
- J1 - On the right side of **I/O DECODE**, change J1 pin 6 to pin 8 (SA QUAL).



CHANGES TO FIGURE 8G-102 (2636A AND ABOVE)

P/O A4 LATCH MODULE (08642-60125)

P/O A5 DISTRIBUTION ASSEMBLY (08642-60126) SS63

ADDRESS LINES 5 KR
R/W 5 KS
ADDRESS DECODE 5 KT
DATA BUS OUT 4 KU

P/O P1: 31 A1, 32 A2, 33 A3, 34 A4, 35 A5, 36 A6, 37 A7

19 R/W
21 LATCH SEL
22 A/D SEL
23 D/A SEL

BUS TRANSCEIVERS

LATCHES
D/A
A/D
U1B

2 D0, 3 D1, 4 D2, 5 D3, 6 D4, 7 D5, 8 D6, 9 D7
10 D8, 11 D9, 12 D10, 13 D11, 14 D12, 15 D13, 16 D14, 17 D15

U8, U10: G3, 3 EN1, 3 EN2, ▷1▽, ▽2◁, ✳10
+5V (F1), ✳20
C13 0.1µ
C12 0.1µ

D/A KV 11
A/D KQ 10
D0-D9 / 10 VM DATA KP 10
16 DATA BUS JR 9,11

POWER SUPPLY AND GND

POWER SUPPLY 59 JB / 3
GROUND 60 TS

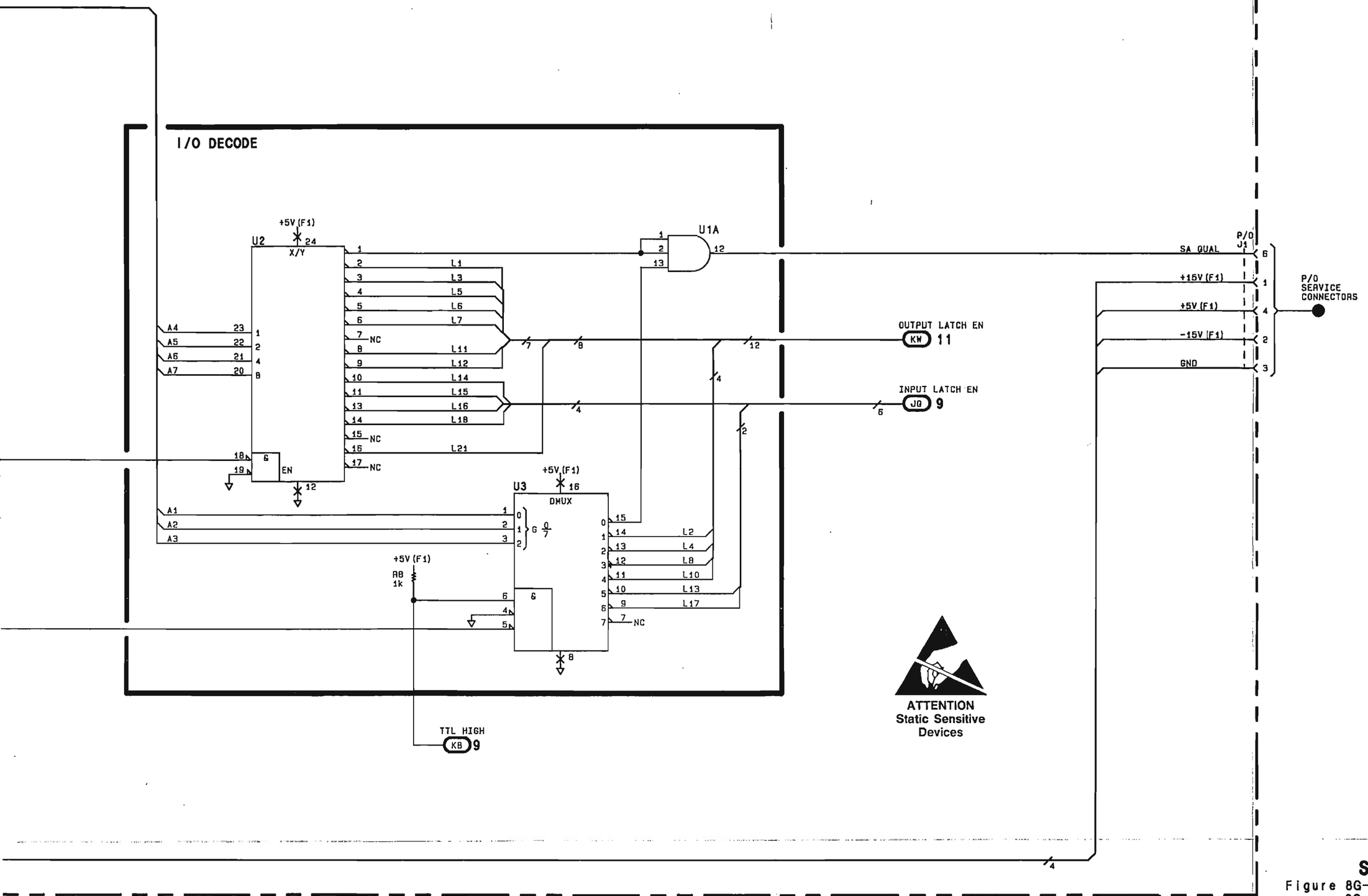
P/O P4: 49 +15V, 47, 48 +5V, 50 -15V
P/O P3: 11-13, 19-24, 25, 27, 29-31, 34-36, 38, 41, 47 GND

L2 5µ, C35 0.1µ, C7 15µ → +15V (F1)
L1 5µ, C34 0.1µ, C6 22µ, C9 4.7µ, C10 4.7µ, C11 4.7µ → +5V (F1)
L3 5µ, C36 0.1µ, C8 15µ → -15V (F1)
GND

+5V (F1), -15V (F1), GND → POWER SUPPLY AND GND JA 9,10,11

A4 A5 A6 A7 A1 A2 A3

SERIAL PREFIX: 2427A



SS8
Figure 8G-103
8G-103

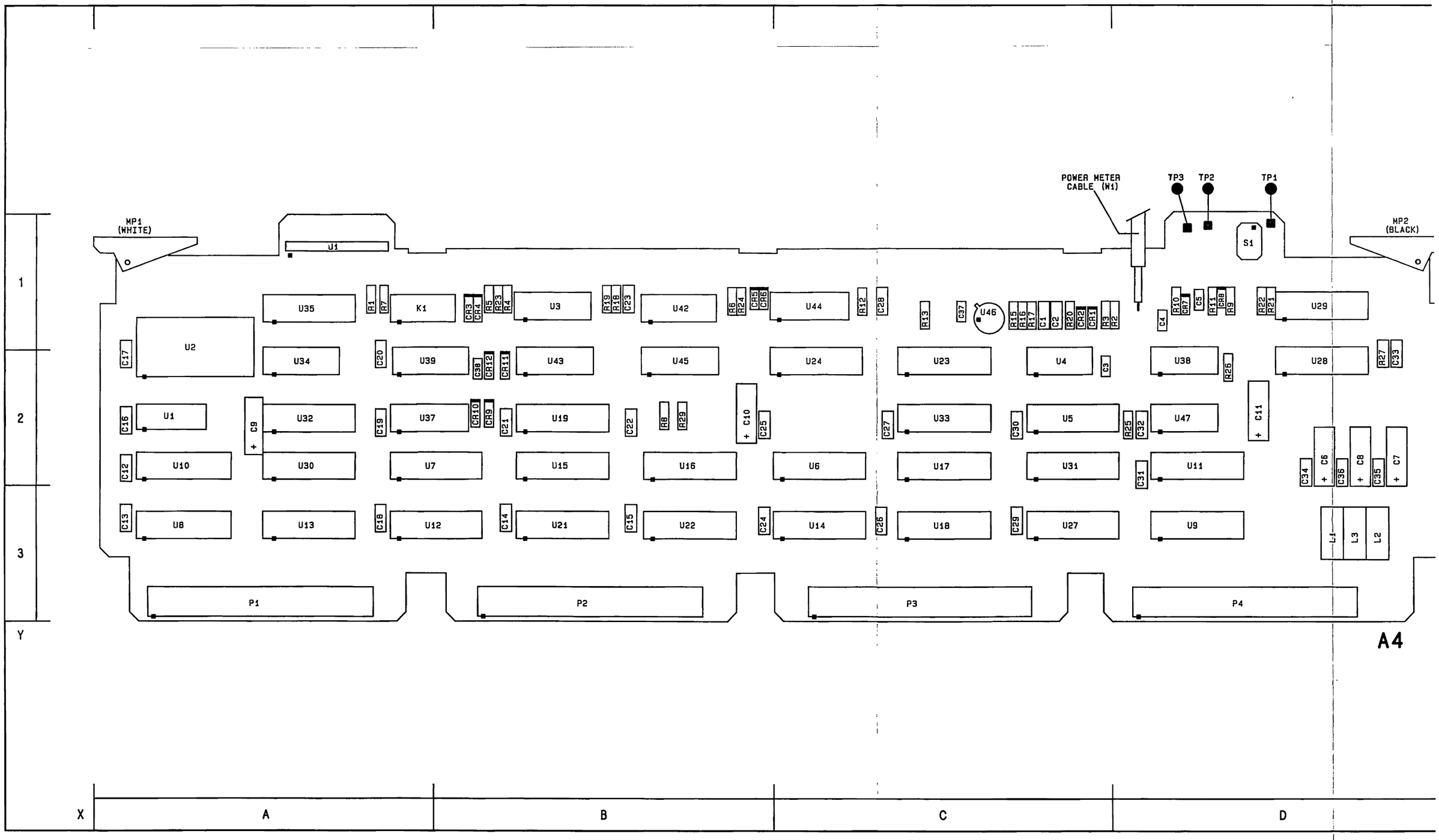
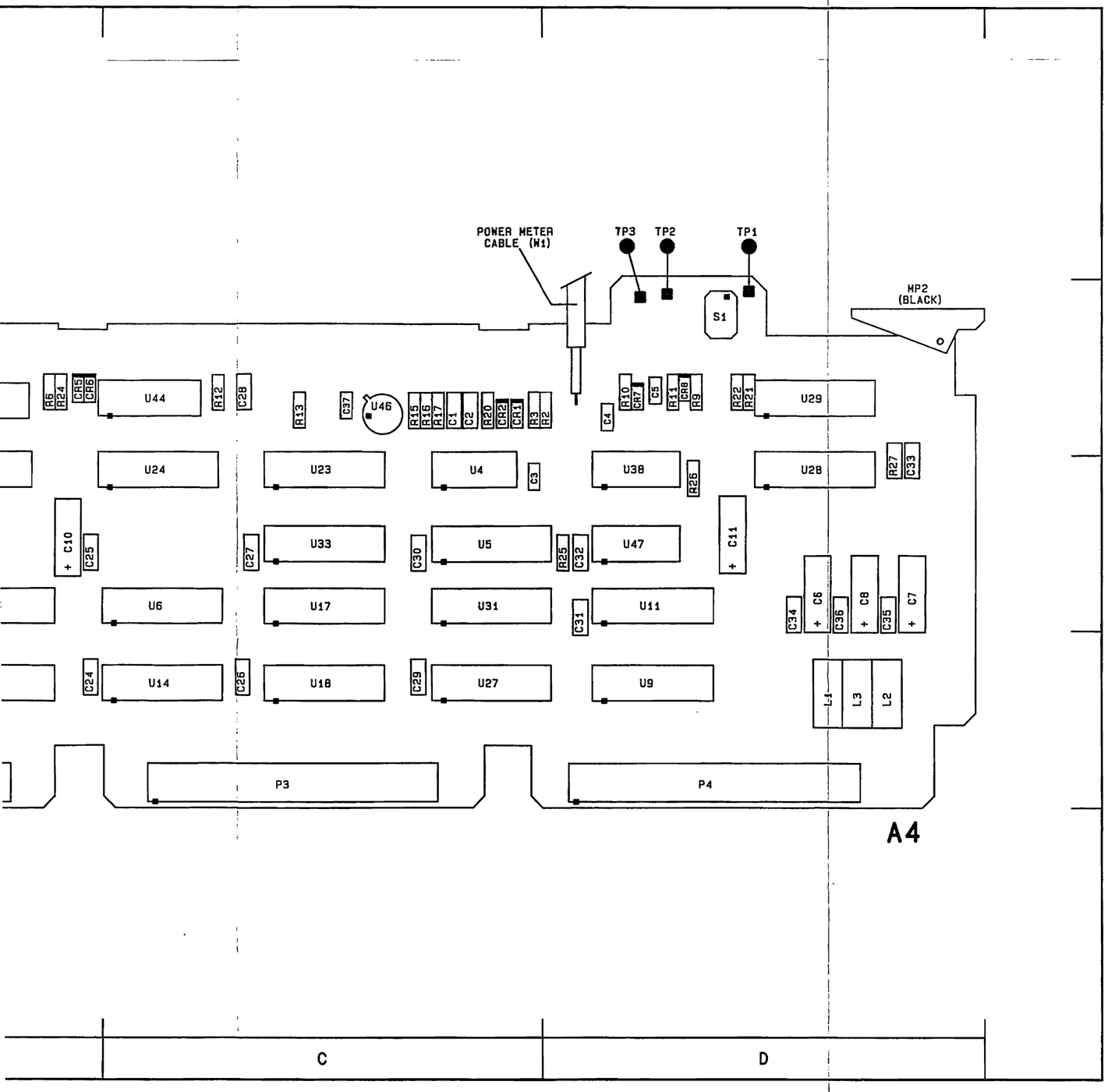
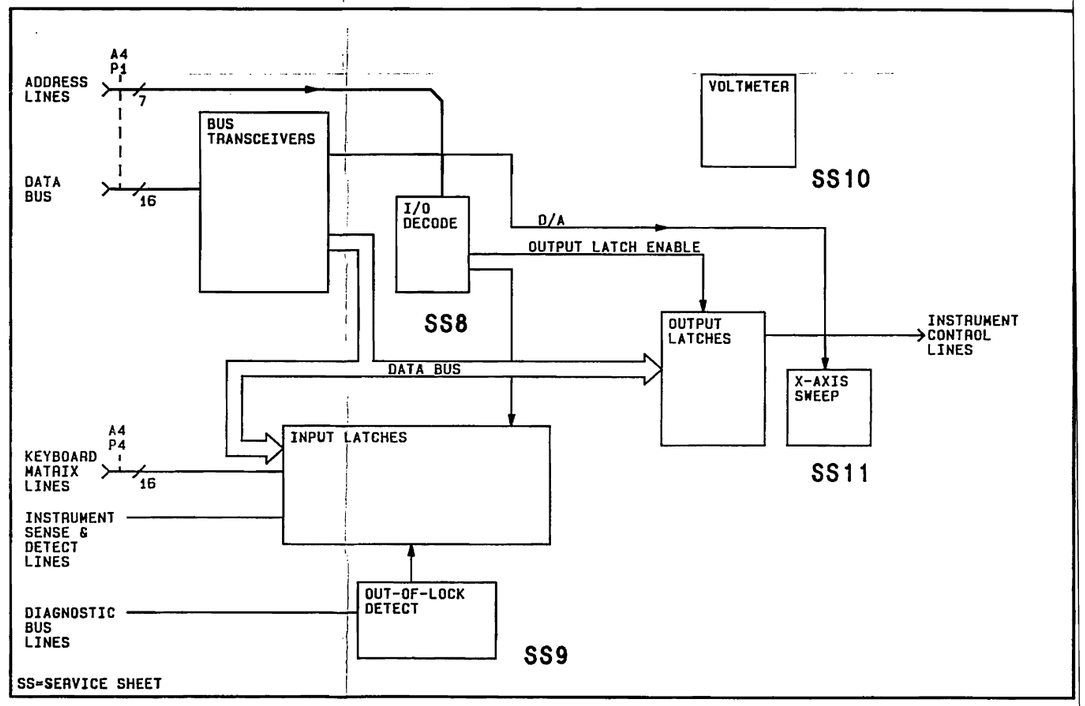


Figure 8G-104. SERVICE SHEET 9 INFORMATION

Component Locator



omponent Locator



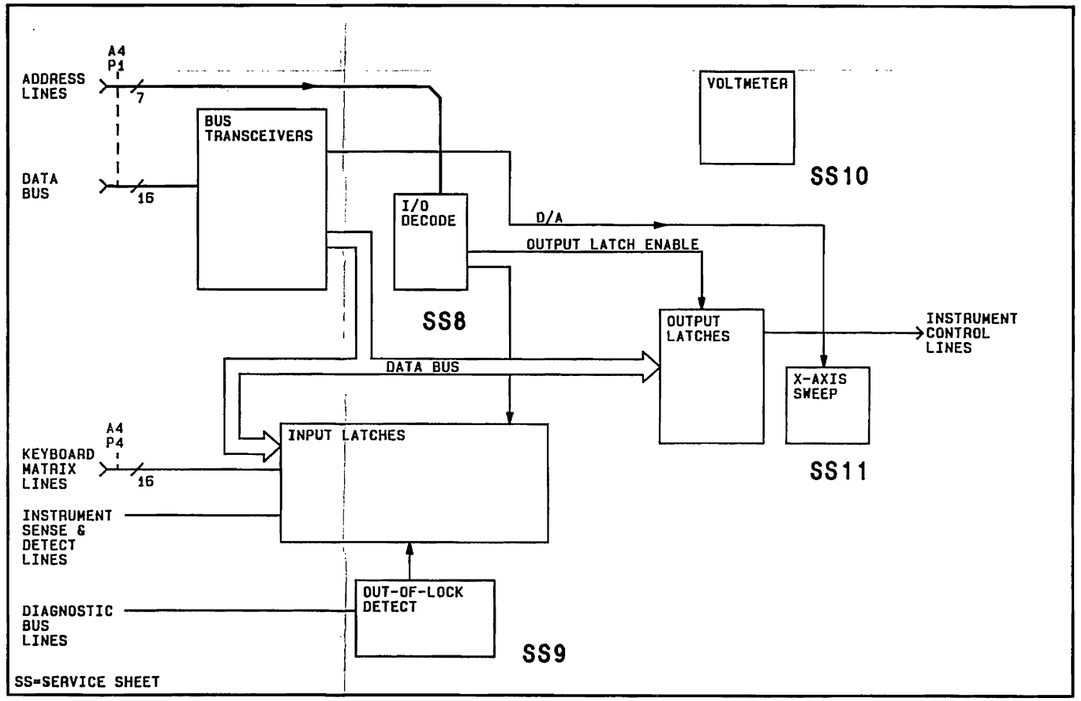
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
J1	A, 1	U45	B, 2												
		U47	D, 2												
MP1	A, 1														
MP2	D, 1														
P1	A, 3														
P2	B, 3														
P3	C, 3														
P4	D, 3														
R7	A, 1														
R12	C, 1														
R18	B, 1														
R19	B, 1														
R21	D, 1														
R22	D, 1														
R25	D, 2														
R26	D, 2														
R27	D, 2														
S1	D, 1														
U1	A, 2														
U24	C, 2														
U27	C, 3														
U28	D, 2														
U29	D, 1														
U30	A, 2														
U31	C, 2														
U32	A, 2														
U33	C, 2														
U34	A, 2														
U35	A, 1														
U38	D, 2														
U42	B, 1														
U43	B, 2														
U44	C, 1														

P/O A4 LATCH MODULE **SS8**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

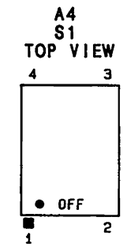
COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
J1	A, 1	U45	B, 2														
		U47	D, 2														
MP1	A, 1																
MP2	D, 1																
P1	A, 3																
P2	B, 3																
P3	C, 3																
P4	D, 3																
R7	A, 1																
R12	C, 1																
R18	B, 1																
R19	B, 1																
R21	D, 1																
R22	D, 1																
R25	D, 2																
R26	D, 2																
R27	D, 2																
S1	D, 1																
U1	A, 2																
U24	C, 2																
U27	C, 3																
U28	D, 2																
U29	D, 1																
U30	A, 2																
U31	C, 2																
U32	A, 2																
U33	C, 2																
U34	A, 2																
U35	A, 1																
U38	D, 2																
U42	B, 1																
U43	B, 2																
U44	C, 1																

P/O A4 LATCH MODULE **SS8**

SEE REVERSE SIDE

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.



Schematic General Information

CHANGES

All Serial Prefixes

On the schematic:

- J1 - At the right side of the schematic, change J1 pin 4 to pin 7.

2521A and above

On the Component Locator:

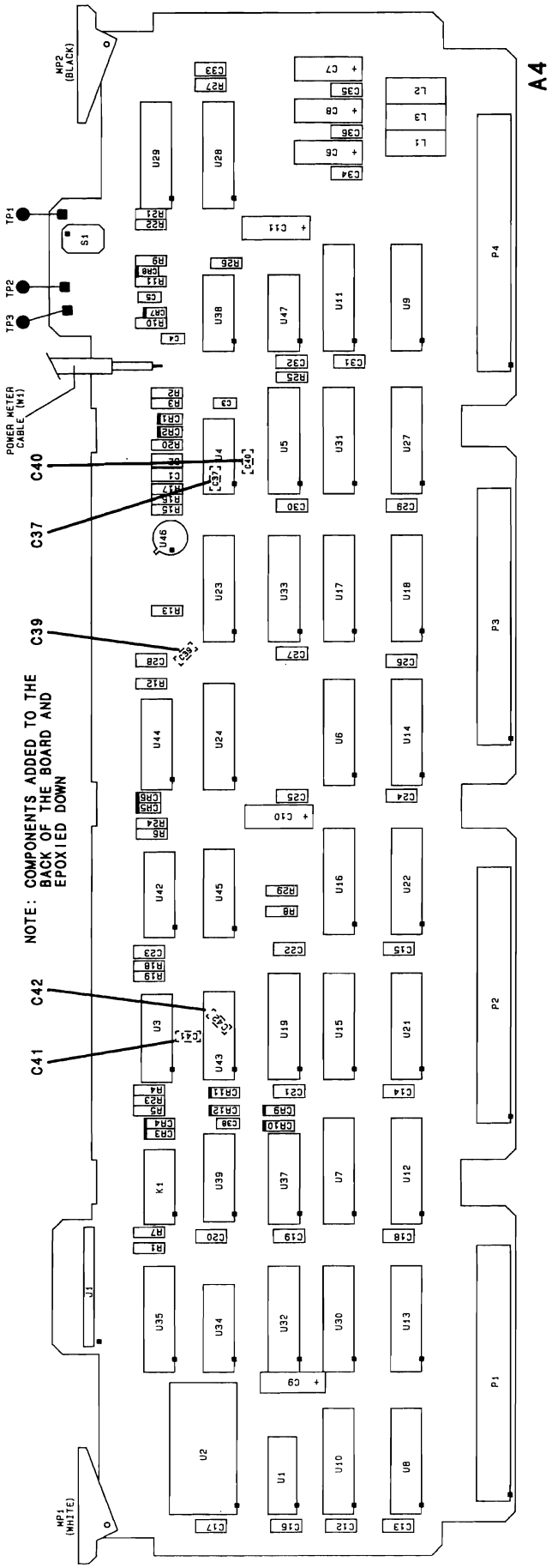
- C41, C42 - Note location of added components shown on page 8G-104.2

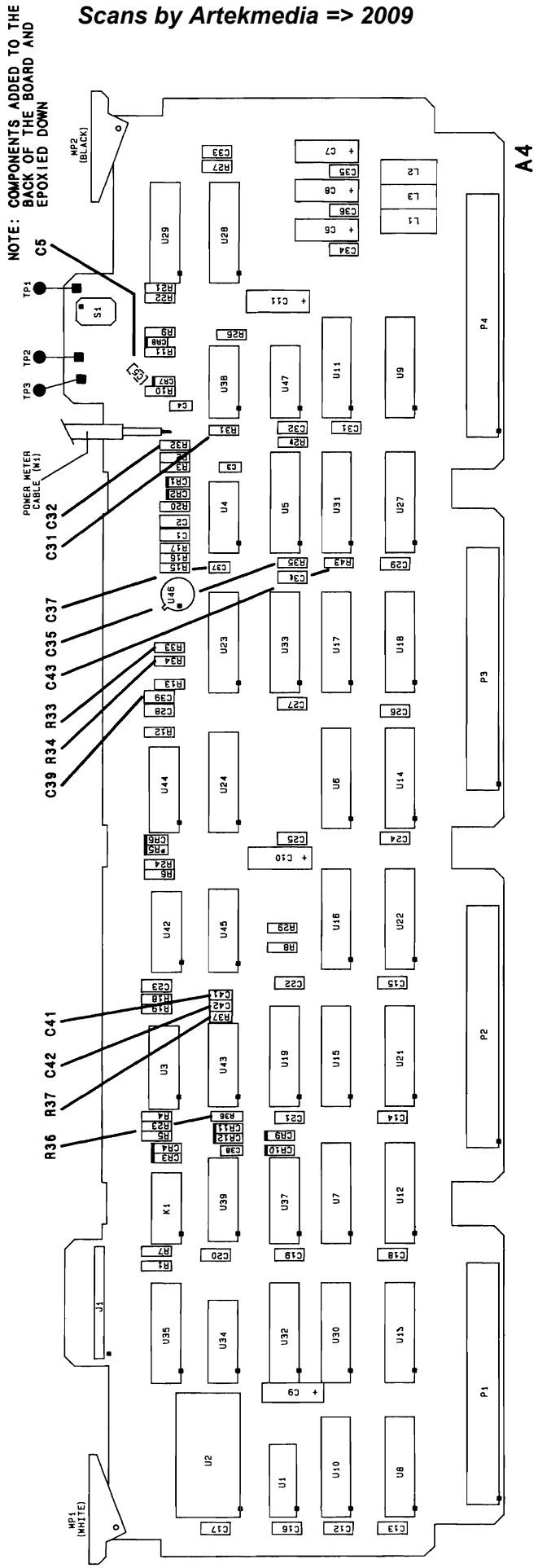
In Component Coordinates:

- C41, C42 - Add (C41 B,1), and (C42 B,2).

On the schematic:

- In the upper left portion of the schematic, change the A4 part number to 08642-60225.
- C41, C42 - In **OUT-OF-LOCK DETECT**, add a capacitor from U43A pin 13, to ground. Designate it C41, and give it a value of 0.1u (Farads). Add a capacitor from U43A pin 5, to ground. Designate it C42, and give it a value of 0.1u (Farads).





P/O A4 LATCH MODULE (08642-60125)

INPUT LATCH EN 8 JQ

DATA BUS 8,11 JR

OUTPUT ENABLE 5 KJ → P/O A5 SS63 → P/O P1 25

INPUT LATCHES

U32C U27 U24A U28 U32D U29

+5V (F1)

R27 1k

HP-IB SWITCH OUTPUTS 2 AD (8)

P/O P4: "1" 1, "4" 3, X2 14, X1 22, X3 6, "16" 5, "8" 4, "2" 2

P/O A5 SS59

KEYBOARD MATRIX LINES 1 AX (14)

ROW 0 37, ROW 1 38, ROW 2 39, ROW 3 40, ROW 4 41, ROW 5 42, ROW 6 43, ROW 7 44

COL 0 29, COL 1 30, COL 2 31, COL 3 32, COL 4 33, COL 5 34

RPG DIR 2 EM → 28 RPG DIR

DISP BUSY (L) 2 FH → 24 DISP BUSY

ATN LEVEL/ BAND LOCK 54 GL (2) → P/O P3 42 ATN BAND LOCK, 46 ATN LEVEL LOCK

MOD HI 16 GB → 43 MOD HI

COUNTER OUTPUT 24 IL → 45 COUNTER OUTPUT

FN LOW SWEEP LIMIT 29 UU → 37 FN LSL

ATN REV POWER INT 54 IW → 39 APP INT

MOD HI/LO INT 16 GA → 40 MOD HI LO INT

OVEN SENSE 53 IZ → 44 OVEN SENSE

P/O A5 SS60

RPG CHANGE (L) 2,4 HW → P/O A5 SS59 → P/O P4 26 RPG CHANGE (L)

KEY DOWN (L) 2 IK → P/O A5 SS59 → 45 KEY DWN (L)

EEPROM WE 7 KI → P/O A5 SS63 → P/O P1 50 EEPROM WE

S1 R22 4640 R21 4640 +5V (F1)

NORM/DIAG.

SA SELECT

U24C U1C U47F U24B

POWER SUPPLY AND GND

8, 10, 11 JA (4)

+15V (F1) +5V (F1) -15V (F1) GND

SERIAL PREFIX: 2427A

CNT DATA BACK

U47A U47B NC

OUT-OF-LOCK DETECT

TO VM KD 10

±15V TO TTL LEVEL TRANSLATORS

R18 100k

U43A U43C U42A U42B U42C U42D U43D

MOD LO

FM OOL REF OOL SUM OOL DBLR OS OOL HET OOL SAWR OOL TB OOL FN OOL

R12 1k

U44

FM SUM DBL OS REF

R19 42.2k

OOL RESET (L) 11 KA A4

MODULATION DIAGNOSTIC BUS 16 FZ → P/O P2 13 MOD

FM LOOP DIAGNOSTIC BUS 23 IE → 7 FM

REFERENCE LOOP DIAGNOSTIC BUS 33 DF → 10 REF

SUM LOOP DIAGNOSTIC BUS 39 EA → 6 SUM

DOUBLER DIAGNOSTIC BUS 49 JF → 8 DBLR

OUTPUT SECTION DIAGNOSTIC BUS 44 HJ → 12 OS

HET REF DIAGNOSTIC BUS 45 HS → 11 HET

SAWR LOOP DIAGNOSTIC BUS 25 BH → 32 P/O P3 SAWR OOL

TIMEBASE DIAGNOSTIC BUS 21 AW → 28 TB OOL

IF REFERENCE DIAGNOSTIC BUS 30 JN → 7 FN OOL

P/O A5 SS61

P/O A5 SS60

16
L13
L14
8 D8-D15
P/O J1
P/O SERVICE CONNECTORS
READ EN

+5V (F1)
U30C
U31
MOD HI
MOD LO
DISP BUSY
KB CW
ATTN LEVEL LOCK
ATN BAND LOCK
D2
D3
D5
D7
D0
D6
D1
D4

U30D
U33
EEPROM WE
FN LSL
HI/LO INT
RPG INT
KEY DWN
RPP INT
R25 1k
D6
D5
D4
D1
D0
D2
D3
D7

U24F
U35
FN
TB
SAW
FM
OS
DBL
SUM
REF
R7 1k
D8
D11
D13
D12
D9
D10
D14
D15

6
2 KEY DWN, HI/LO INT
M TEST BIT
KE
HET, RPP DIS
11 K6
2
HET DIS
RPP INT DIS
U24D
U24E
A0
A1
HET
8
4

9
9
8
B7
B6
B5
B4
B3
B2
B1
B0
U30A
U30B
U30E
U30F
U32A
U32B
U32E
U32F
FN
SAW
OS
SUM
REF
DBL
FM
TB
FN OOL
SAW OOL
OS OOL
SUM OOL
REF OOL
DBL OOL
FM OOL
TB OOL

OOL
ETECT
ATCHES
4
+5V (F1)
U45
SAW
TB
FN
HET

INTERRUPT DETECT
+5V (F1)
R26 1k
U38
CNT INT DIS
11 KF
NC
CNT RDY INT

ATTENTION
Static Sensitive
Devices

12
+5V (F1)
U34
A0
A1
FN OOL
SAW OOL
OS OOL
SUM OOL
REF OOL
DBL OOL
FM OOL
TB OOL
MOD HI LO INT
RPG CHANGE (L)
CNT RDY INT
P/O P1
27
LB INT
KH 4
P/O A5 SS63

OOL MASK
11 KC
A4

SS9
Figure 8G-105
8G-105

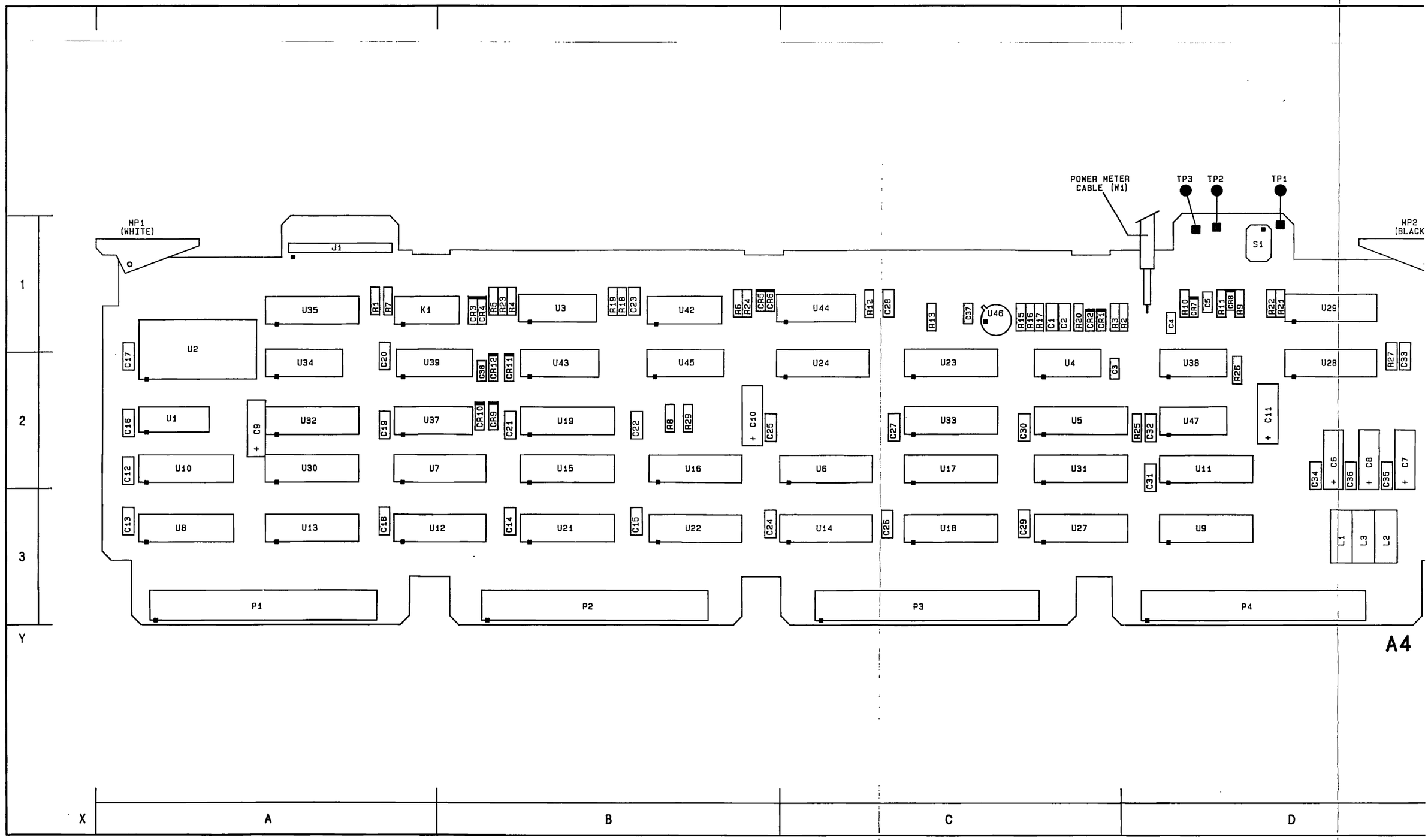
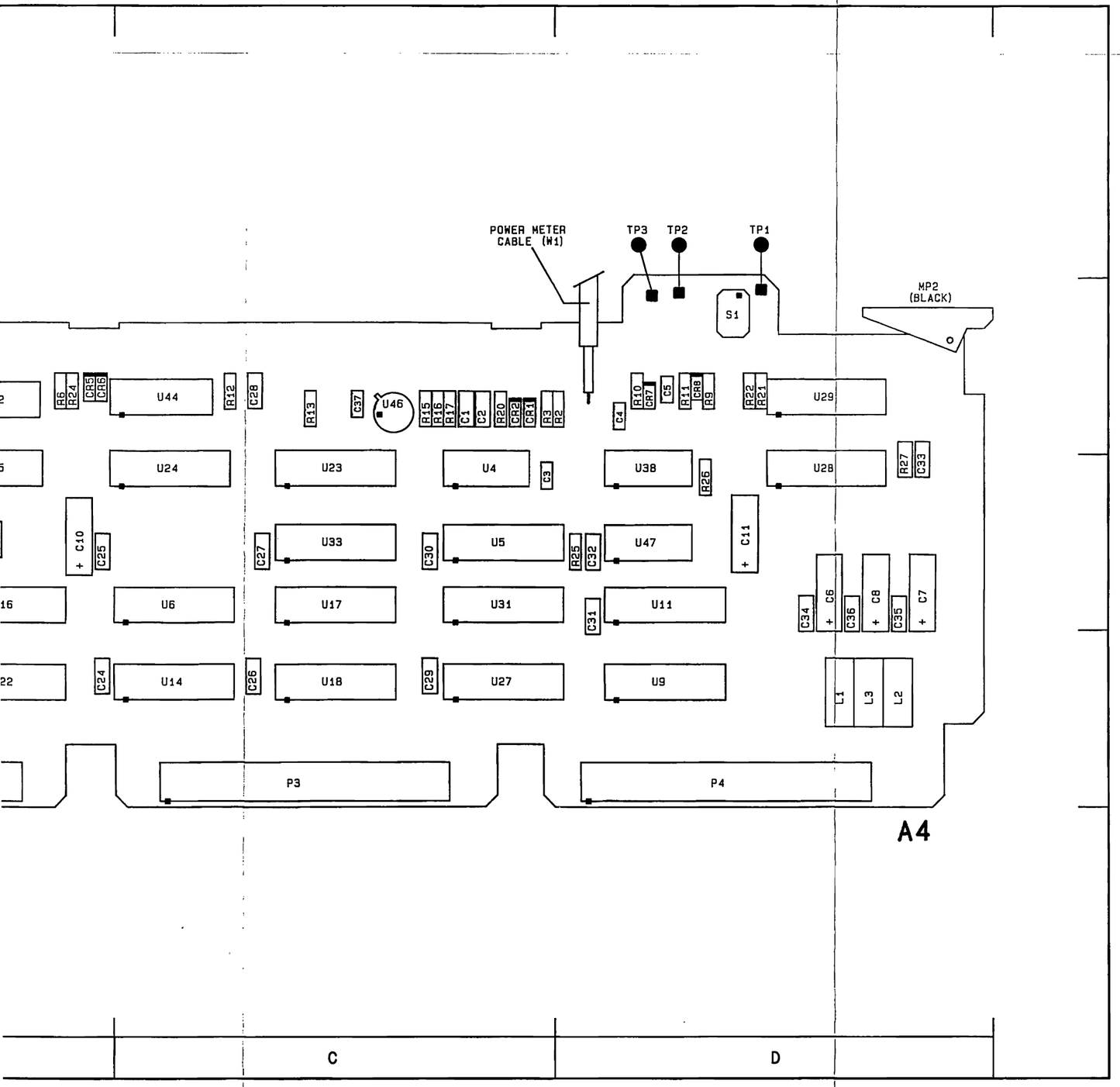


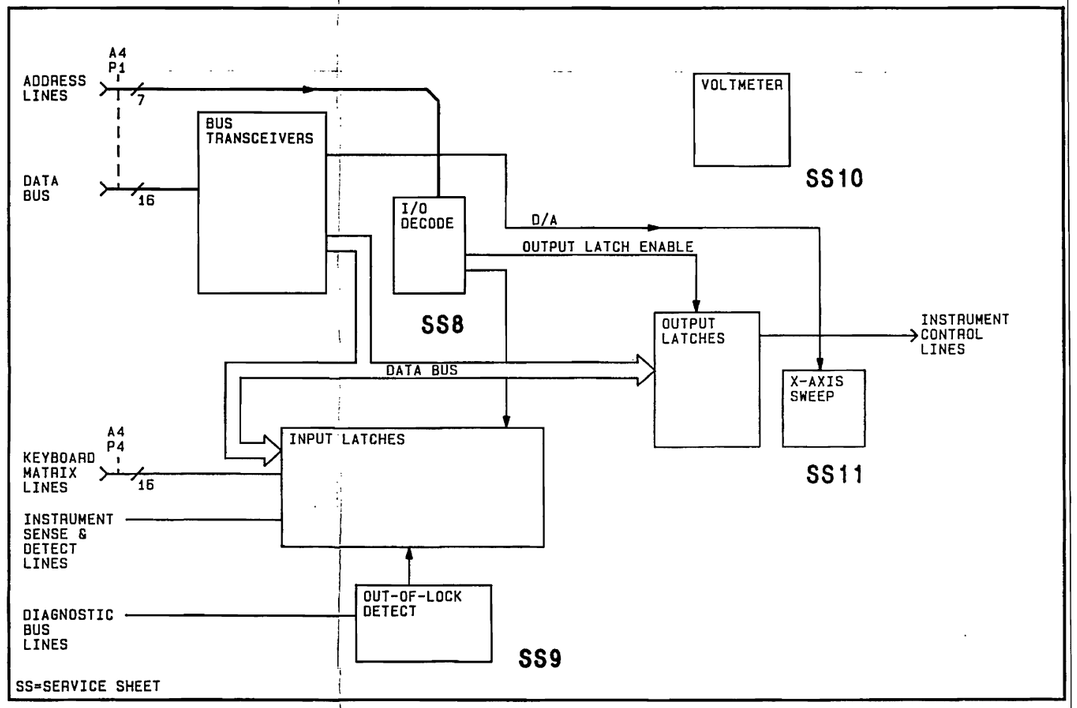
Figure 8G-106. SERVICE SHEET 10 INFORMATION

Component Locator



A4

Component Locator



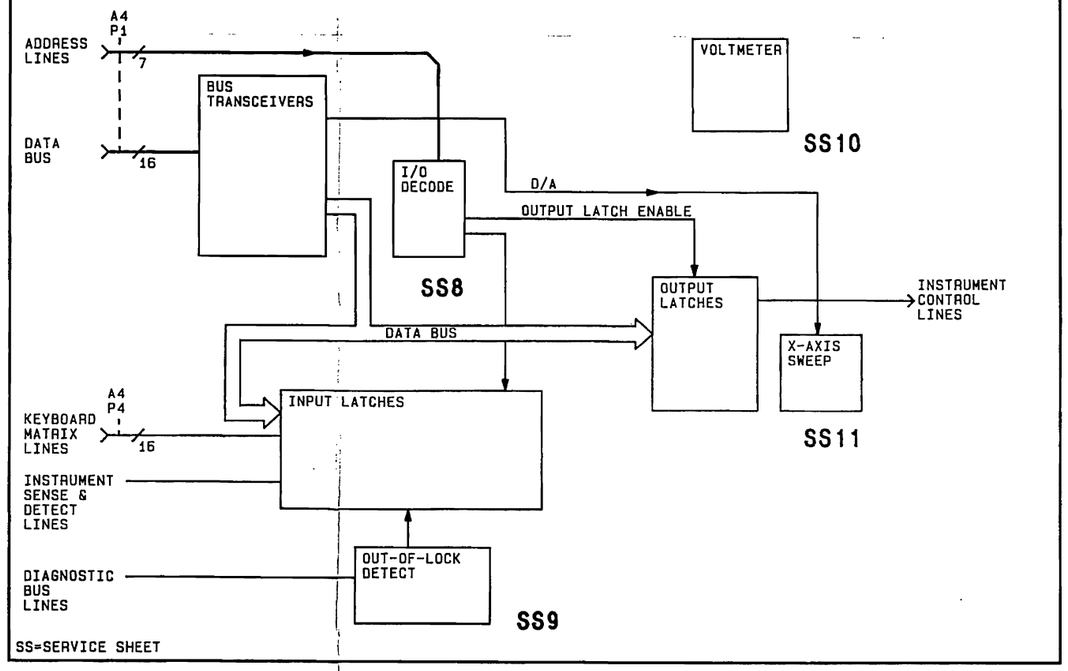
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	C, 1	TP1	D, 1												
C2	C, 1	TP2	D, 1												
C4	D, 1	TP3	D, 1												
C5	D, 1														
C37	C, 1	U4	C, 2												
C38	B, 2	U23	C, 2												
		U37	A, 2												
CR5	B, 1	U39	A, 2												
CR6	B, 1	U46	C, 1												
CR7	D, 1	U47	D, 2												
CR8	D, 1														
CR9	B, 2	W1	D, 1												
CR10	B, 2														
CR11	B, 2														
CR12	B, 2														
J1	A, 1														
K1	A, 1														
MP1	A, 1														
MP2	D, 1														
P1	A, 3														
P2	B, 3														
R6	B, 1														
R9	D, 1														
R10	D, 1														
R11	D, 1														
R13	C, 1														
R15	C, 1														
R16	C, 1														
R17	C, 1														
R24	B, 1														
R29	B, 2														

SEE REVERSE SIDE

P/O A4 LATCH MODULE **SS9**



Reference Block Diagram

Component Coordinates

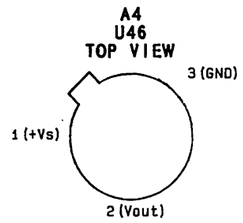
COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	C, 1	TP1	D, 1												
C2	C, 1	TP2	D, 1												
C4	D, 1	TP3	D, 1												
C5	D, 1														
C37	C, 1	U4	C, 2												
C38	B, 2	U23	C, 2												
		U37	A, 2												
CR5	B, 1	U39	A, 2												
CR6	B, 1	U46	C, 1												
CR7	D, 1	U47	D, 2												
CR8	D, 1														
CR9	B, 2	W1	D, 1												
CR10	B, 2														
CR11	B, 2														
CR12	B, 2														
J1	A, 1														
K1	A, 1														
MP1	A, 1														
MP2	D, 1														
P1	A, 3														
P2	B, 3														
R6	B, 1														
R9	D, 1														
R10	D, 1														
R11	D, 1														
R13	C, 1														
R15	C, 1														
R16	C, 1														
R17	C, 1														
R24	B, 1														
R29	B, 2														

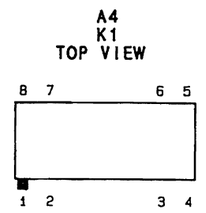
SEE REVERSE SIDE

P/O A4 LATCH MODULE **SS9**

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.





Schematic General Information

CHANGES

All Serial Prefixes

On the schematic:

- TP2, TP3 - In **INTERNAL VOLTMETER**, switch the reference designators for TP2 and TP3.

2521A and above

On the Component Locator:

- C37, C39, C40 - Note location of added components, shown on page 8G-106.2

In Component Coordinates:

- C37, C39, C40 - Change coordinates of C37 to C,2. Add (C39 C,1) and (C40 C,2).
- C37, C39, C40 - In **INTERNAL VOLTMETER**, add a capacitor from U23 pin 20, to ground. Designate it C39, and assign it a value of 0.1u (Farads). Change the value of C37 to 470p (Farads). Add a capacitor from U4A pin 4 to ground. Designate it C40, and assign it a value of 0.1u (Farads).

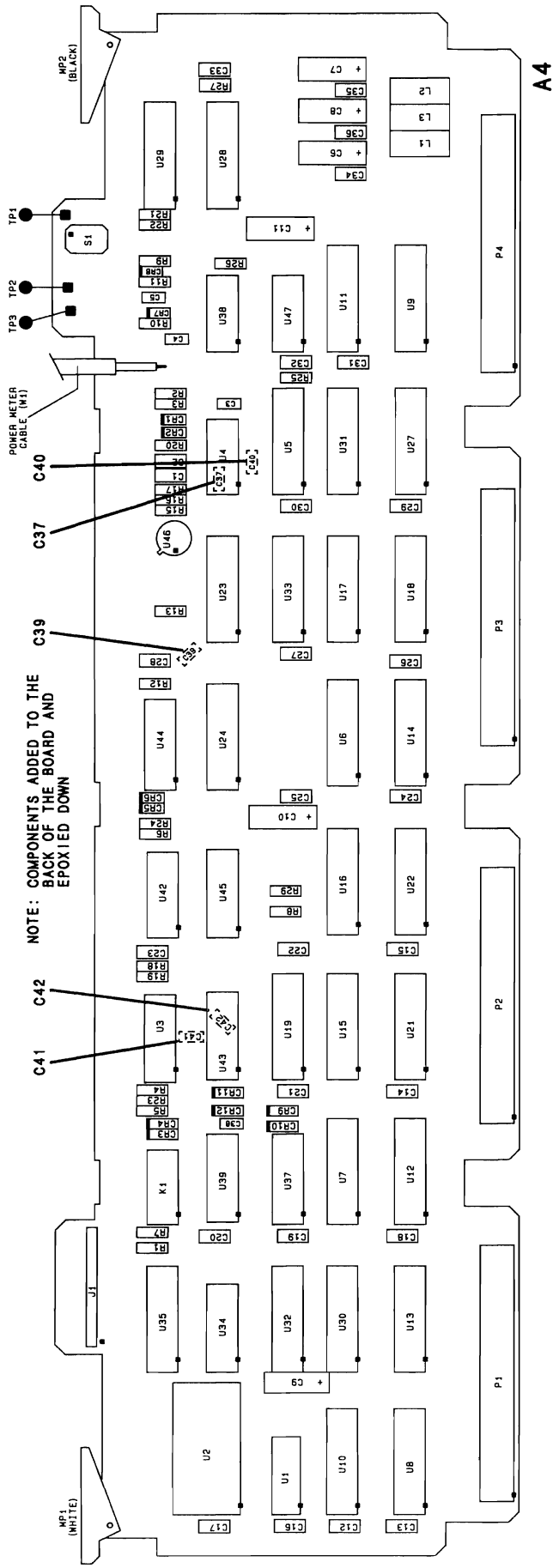
2636A and above

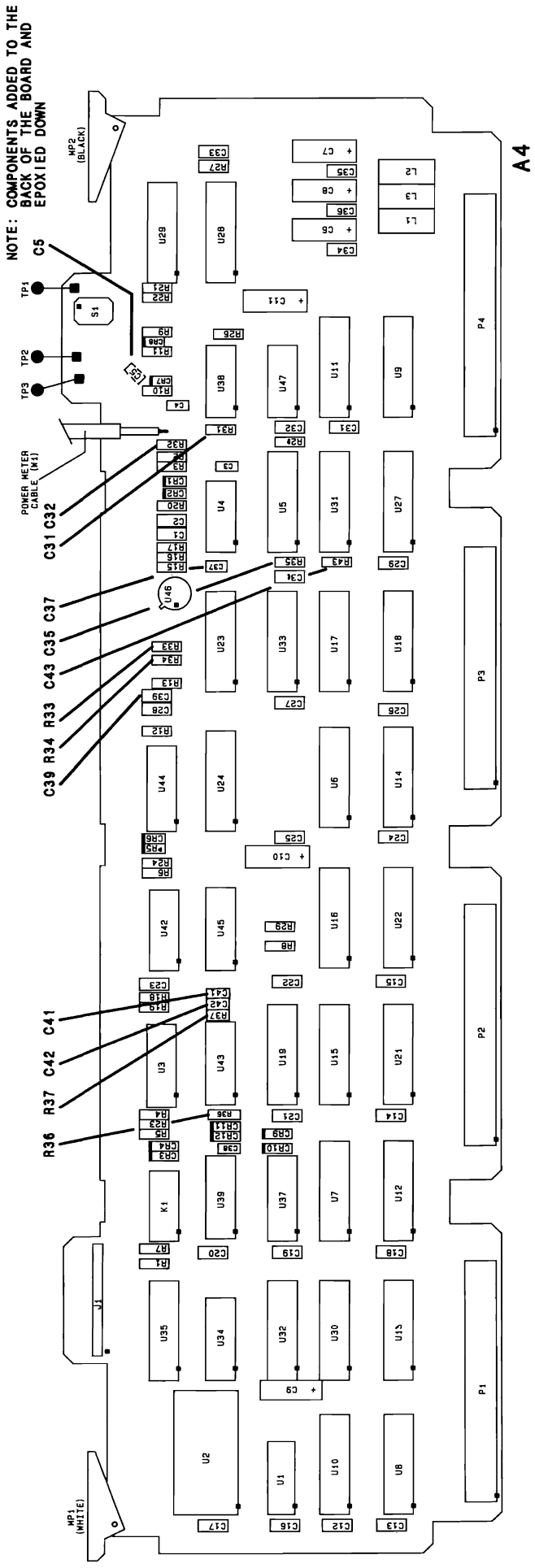
On the schematic:

- In the upper left portion of the schematic, change the A4 part number to 08642-60225.
- C40 - In **INTERNAL VOLTMETER**, delete C40. (C40 was added on serial break 2521A.)
- R30 - In **INTERNAL VOLTMETER**, add R30, 51.1K, in series with the +15V (F1) supply between the node of C39 and the +15V supply.
- R31 - In **INTERNAL VOLTMETER**, add R31, 10 ohms, between the node of C1 and the +15V supply.
- R32 - In **INTERNAL VOLTMETER**, add R32, 10 ohm's between the node of C2 and the -15V (F1) supply.
- R33 - In **INTERNAL VOLTMETER**, add R33, 287 ohm's, on the connection between U43D pin 6 and the node going to R15.
- R34 - In **INTERNAL VOLTMETER**, add R34, 51.1K, from U43D pin 8 and connect it below R33.

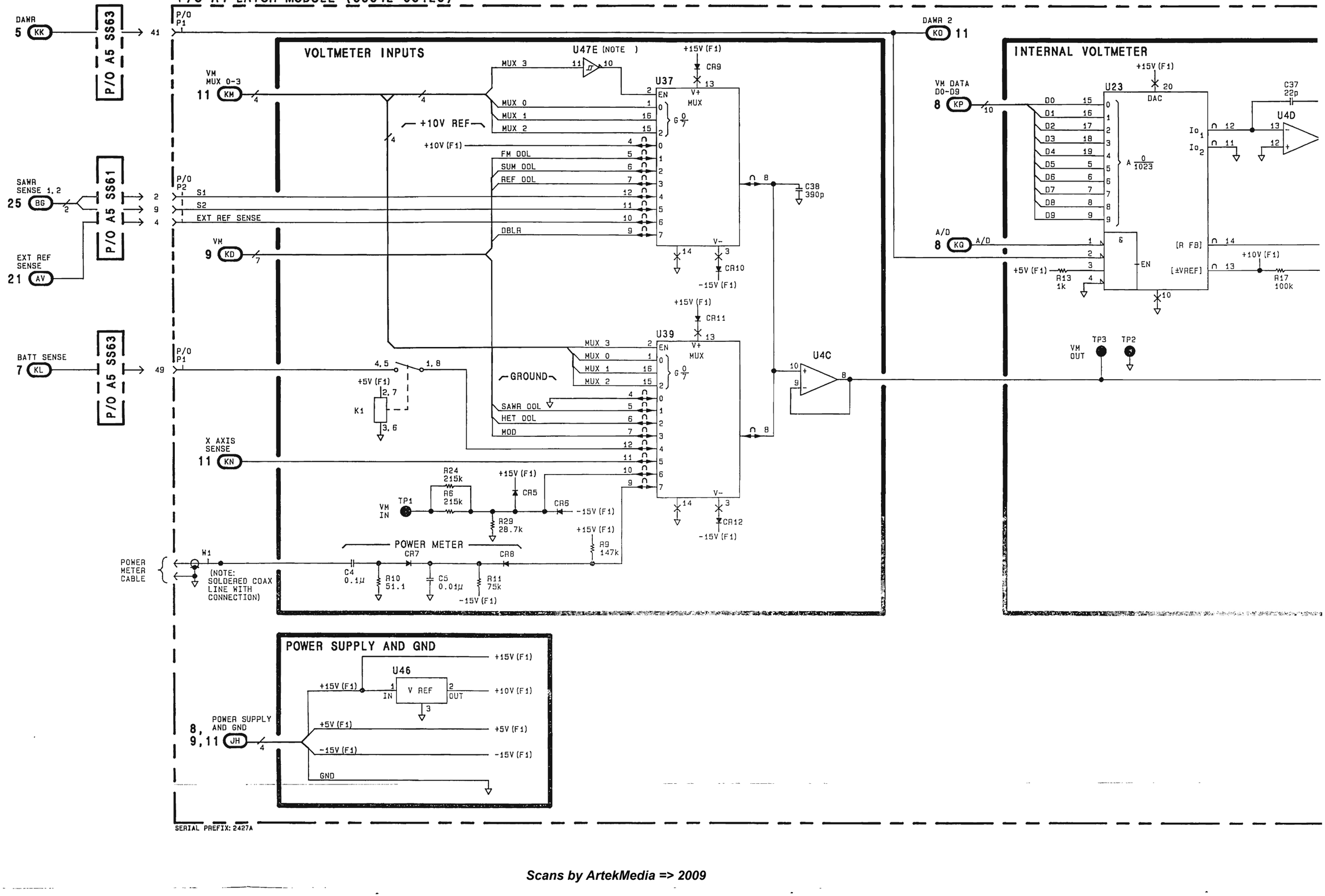
On the Component Locator:

- Replace the Component Locator with the revised Component Locator on page 8G-106.2.

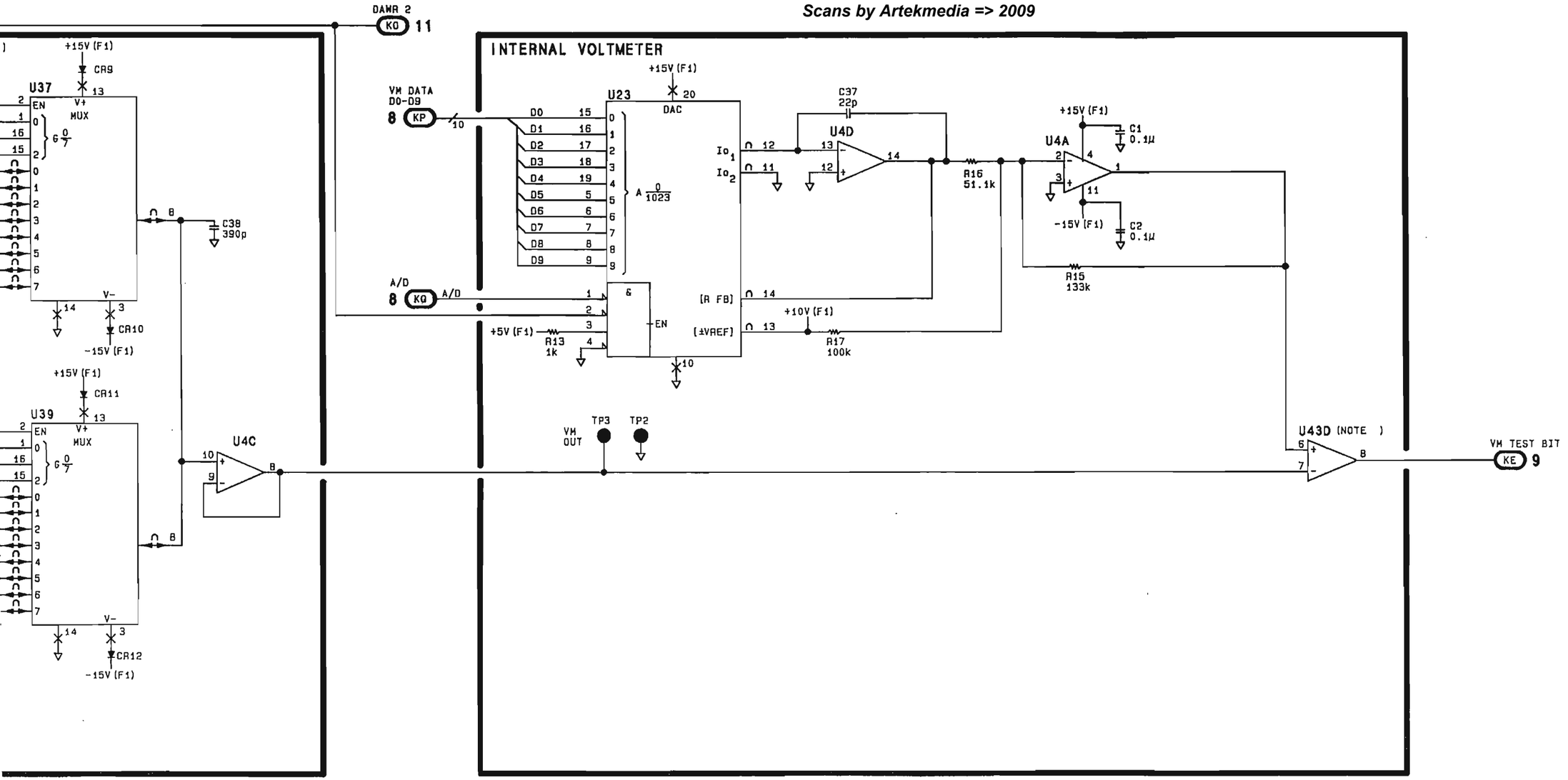




P/O A4 LATCH MODULE (08642-60125)



SERIAL PREFIX: 2427A



ATTENTION
Static Sensitive
Devices

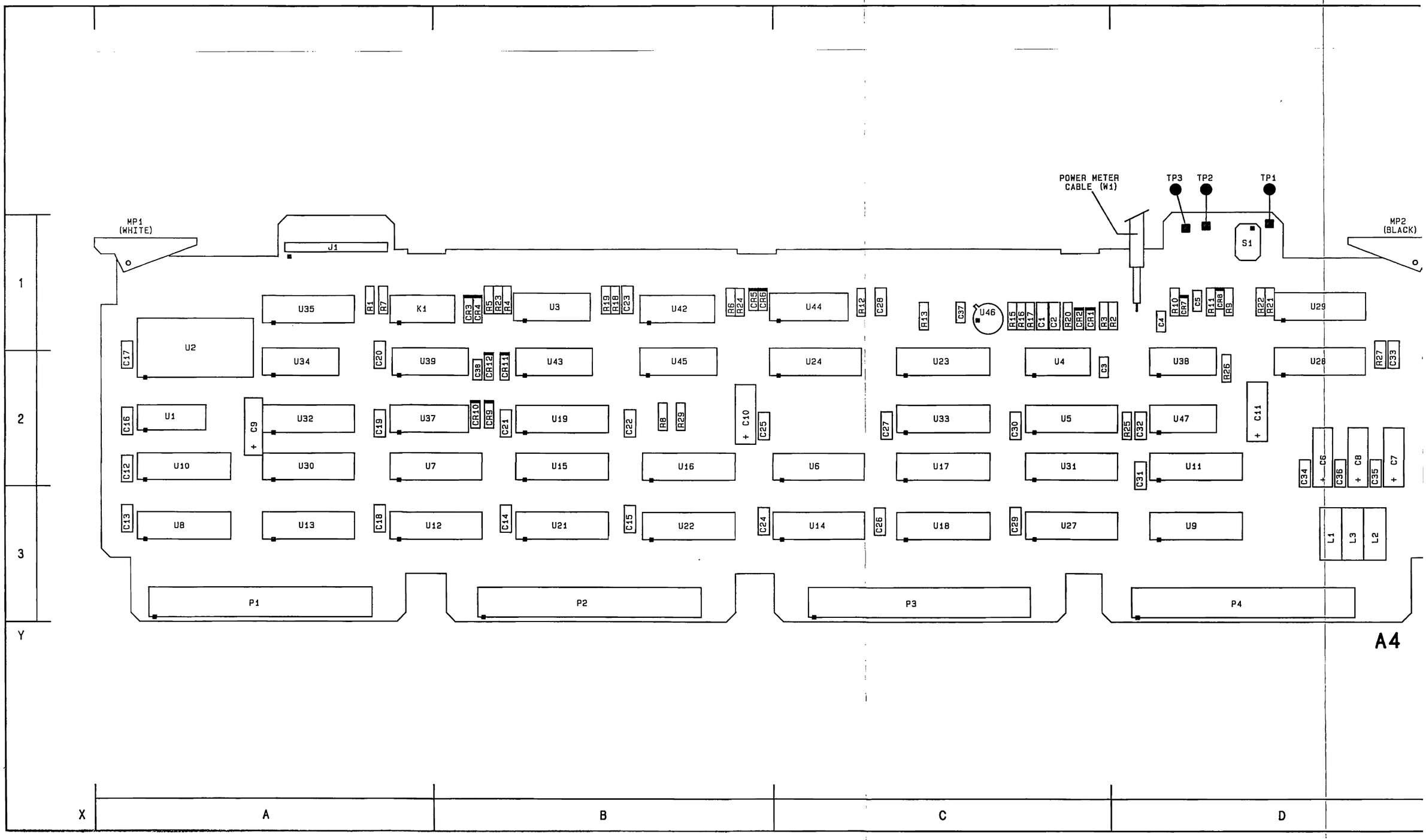
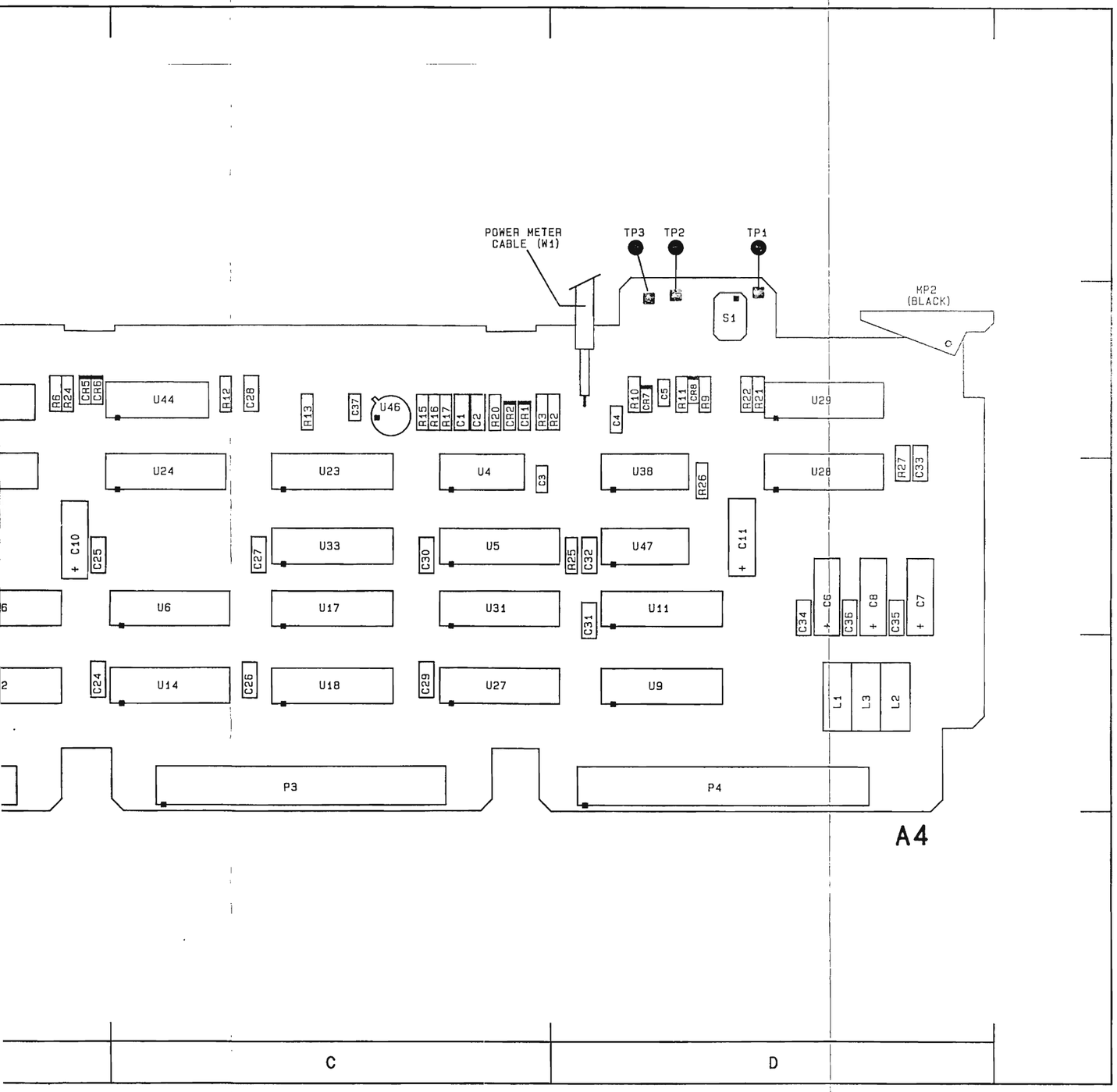


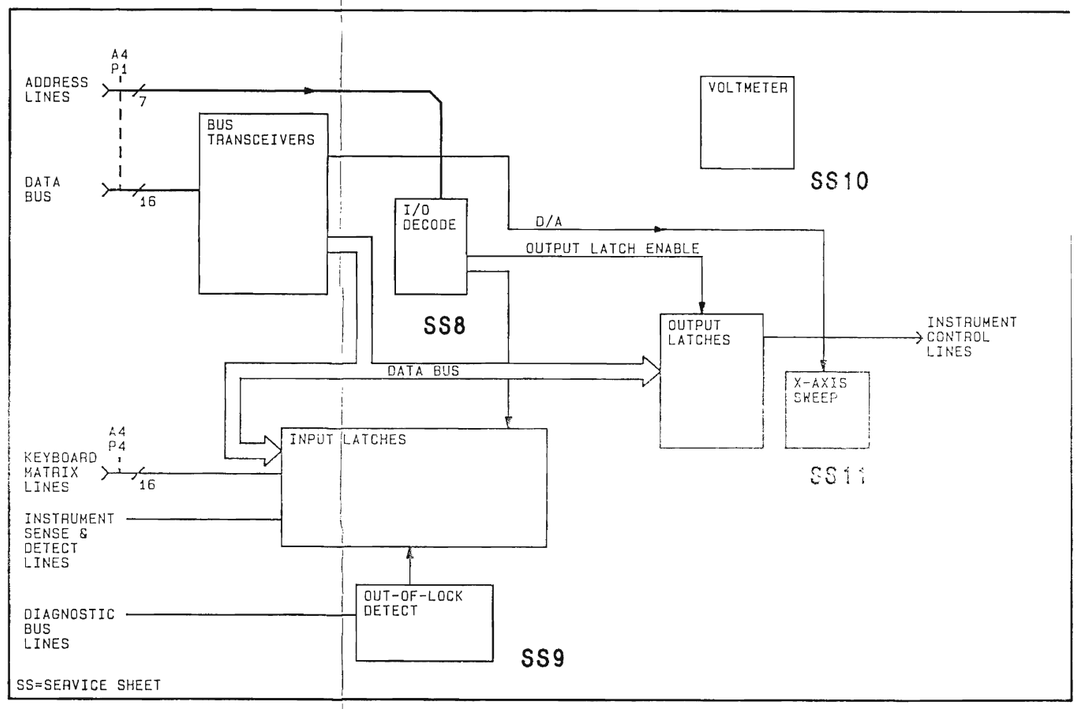
Figure 8G-108. SERVICE SHEET 11 INFORMATION

Component Locator



A4

Component Locator



Reference Block Diagram

Component Coordinates

COMP	X,Y
C3	C, 2
C14	B, 3
C15	B, 3
C16	A, 2
C17	A, 2
C18	A, 3
C19	A, 2
C20	A, 2
C21	B, 2
C22	B, 2
C23	B, 1
C24	B, 3
C25	B, 2
C26	C, 3
C27	C, 2
C28	C, 1
C29	C, 3
C30	C, 2
C31	D, 2
C32	D, 2
C33	D, 2
CR1	C, 1
CR2	C, 1
CR3	B, 1
CR4	B, 1
J1	A, 1
MP1	A, 1
MP2	D, 1
P1	A, 3
P2	B, 3
P3	C, 3
P4	D, 3

COMP	X,Y
R1	A, 1
R2	D, 1
R3	C, 1
R4	B, 1
R5	B, 1
R20	C, 1
R23	B, 1
U4	C, 2
U5	C, 2
U6	C, 2
U7	A, 2
U9	D, 3
U11	D, 2
U12	B, 3
U13	A, 3
U14	C, 3
U15	B, 2
U16	B, 2
U17	C, 2
U18	C, 3
U19	B, 2
U21	B, 3
U22	B, 3

COMP	X,Y

COMP	X,Y

COMP	X,Y

COMP	X,Y

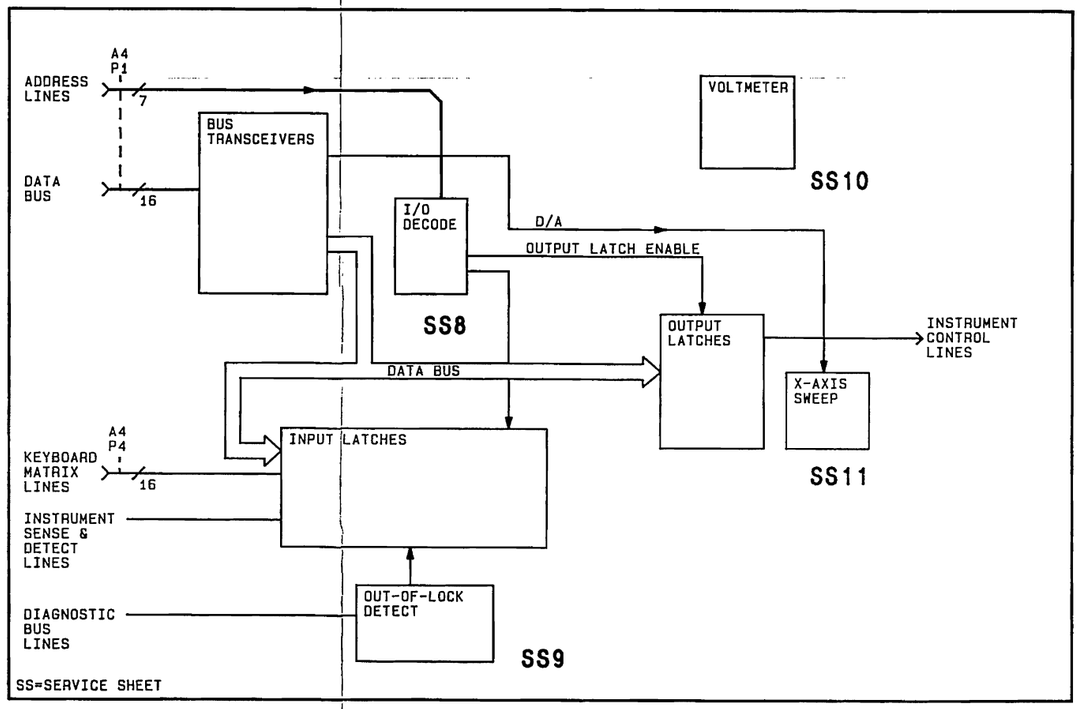
COMP	X,Y

COMP	X,Y

COMP	X,Y

P/O A4 LATCH MODULE **SS10**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C3	C, 2	R1	A, 1												
C14	B, 3	R2	D, 1												
C15	B, 3	R3	C, 1												
C16	A, 2	R4	B, 1												
C17	A, 2	R5	B, 1												
C18	A, 3	R20	C, 1												
C19	A, 2	R23	B, 1												
C20	A, 2														
C21	B, 2	U4	C, 2												
C22	B, 2	U5	C, 2												
C23	B, 1	U6	C, 2												
C24	B, 3	U7	A, 2												
C25	B, 2	U9	D, 3												
C26	C, 3	U11	D, 2												
C27	C, 2	U12	B, 3												
C28	C, 1	U13	A, 3												
C29	C, 3	U14	C, 3												
C30	C, 2	U15	B, 2												
C31	D, 2	U16	B, 2												
C32	D, 2	U17	C, 2												
C33	D, 2	U18	C, 3												
		U19	B, 2												
CR1	C, 1	U21	B, 3												
CR2	C, 1	U22	B, 3												
CR3	B, 1														
CR4	B, 1														
J1	A, 1														
MP1	A, 1														
MP2	D, 1														
P1	A, 3														
P2	B, 3														
P3	C, 3														
P4	D, 3														

P/O A4 LATCH MODULE **SS10**

SEE REVERSE SIDE

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
3. All capacitors shown in Power Supply and Gnd are connected between +5V and ground planes. They are layed out in strategic locations to reduce undesired signal effects.

CHANGES

All Serial Prefixes

On the schematic:

- J1 - On the right side of the schematic, change J1 pin 7 to pin 9 (S.A. FLAG).

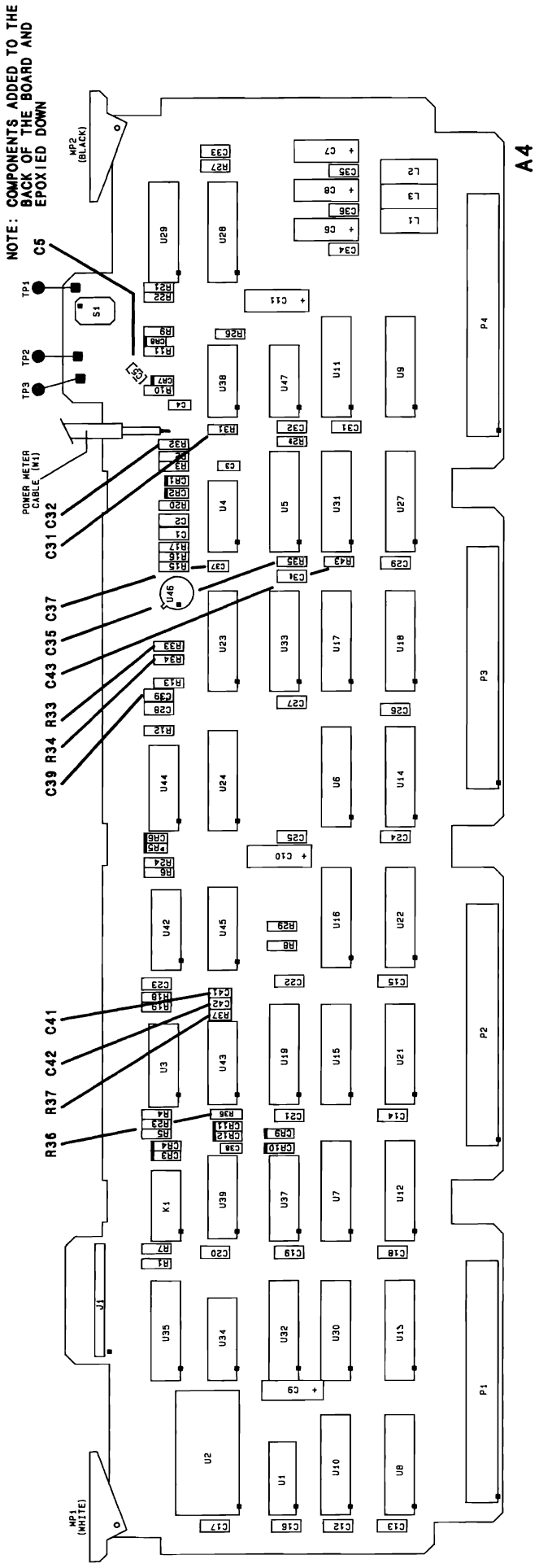
2636A and above

On the schematic:

- In the upper left portion of the schematic, change the A4 part number to 08642-60225.
- C43,R35 - In **X-AXIS SWEEP** add C43 0.1u (Farads) from U5 pin 20 to ground. Add R35 in series between the +15V (F1) supply and the node of C43.

On the Component Locator:

- Replace the Component Locator with the revised Component Locator on page 8G-108.2.



P/O A4 LATCH MODULE (08642-60125)

P/O A5 DIST. ASSY. SS57

LUWR, LLWR 5 KX

DAWR 2 10 KO

OOL MASK 8 KC 9

P/O P3 LATCH UWR 48

LATCH LWR 49

OUTPUT LATCHES

U13 20 — +5V (F1)

D11	3	2	B0
D8	4	5	B7
D10	7	6	B2
D9	8	9	B5
D12	13	12	B1
D13	14	15	B6
D14	17	16	B4
D15	18	19	B3

U15 20 — +5V (F1)

D13	3	2	A
D12	4	5	D
D10	7	6	E
D9	8	9	F
D14	13	12	
D8	14	15	B
D11	17	16	C
D15	18	19	

S.A. FLAG

U21A 20 — +5V (F1) — C14 0.1µ

A	2	18	FN HEC
C	4	16	FN C3
	6	14	DBL CLK
B	8	12	FN C0

FN OSC CON

U21B 19

F	11	9	FN C1
	13	7	DBL DATA
E	15	5	FN C2
D	17	3	FN H INV

U19 20 — +5V (F1)

D8	3	2	ATN 0
D14	4	5	ATN 6
D13	7	6	ATN 5
D12	8	9	ATN 4
D11	13	12	ATN 3
D10	14	15	ATN 2
D9	17	16	ATN 1
D15	18	19	HET SW DRIVER CONTROL

S.A. FLAG LHWR

DATA BUS 8 JR

OUTPUT LATCH EN 8 KW

U12 20 — +5V (F1)

D6	3	2	OSCILLATOR DISABLE
D1	4	5	HET MUX A
D0	7	6	DOUBLER MUX
D4	8	9	LCD LIGHT ON (L)
D3	13	12	HET MUX B
D5	14	15	OOL RESET
D2	17	16	APP INT
D7	18	19	HET DIS

U14 20 — +5V (F1)

D0	3	2	
D7	4	5	SAWR B
D2	7	6	HET BD
D4	8	9	DIV 0
D3	13	12	DIV 1
D5	14	15	DIV 2
D6	17	16	SAWR A
D1	18	19	

U16 0 — +5V (F1)

D0	3	2	A
D1	4	5	B
D2	7	6	C
D3	8	9	D
D4	13	12	
D5	14	15	
D6	17	16	
D7	18	19	

U22A 20 — +5V (F1) — C15 0.1µ

A	2	18	OS CLK
B	4	16	OS DATA
C	6	14	REF CLK
D	8	12	REF DATA

U22B 19

	11	9	SUM CLK
	13	7	SUM DATA
	15	5	FM CLK
	17	3	FM DATA

U17 20 — +5V (F1)

D0	3	2	MOD D0
D1	4	5	MOD D1
D2	7	6	MOD D2
D3	8	9	MOD D3
D4	13	12	MOD D4
D5	14	15	MOD D5
D6	17	16	MOD D6
D7	18	19	MOD D7

OOL RESET (L) KA 9

HET APP DISABLE KG 9

LCD LIGHT ON (L) — P/O P2 5 — P/O A5 SS61 — LCD LIGHT ON KY 2

MUX SEL 2 — 1 — DOUBLER MUX JI 50

HET MUX B — 3 — HET MUX B TZ 45

P/O P1 — HET MUX A — 45 — P/O A5 SS63 — HET MUX A HO 45

TIMEBASE DISABLE — 44 — TIMEBASE DISABLE AQ 21

SAWR A — P/O P2 40 — P/O A5 SS62 — SAWR OSCILLATOR SELECT BI 26

SAWR B — 42

DIV 2 — 37 — DIVIDER CONTROL LINE DIV 2 AR 41

DIV 0 — P/O P3 2 — P/O A5 SS60 — DIVIDER CONTROL LINES DIV 0, 1 EK 41

DIV 1 — 3

HET BD — 1 — HET BAND JS 45

OS CLK — P/O P2 41 — P/O A5 SS62

OS DATA — 43

REF CLK — 45

REF DATA — 50

SUM CLK — 49

SUM DATA — 48

FM CLK — 46

FM DATA — 44

POWER SUPPLY AND GND

POWER SUPPLY AND GND 8, 9, 10 JA

+15V (F1)

+5V (F1)

-15V (F1)

C16-33 0.1µ (NOTE 3)

SERIAL PREFIX: 2427A

U21A EN 1 20 +5V (F1) C14 0.1µ
2 18 FN HEC
4 16 FN C3
6 14 DBL CLK
8 12 FN CO
10
FN OSC CON
U21B EN 19
11 9 FN C1
13 7 DBL DATA
15 5 FN C2
17 3 FN H INV

U19 G1 1 20 +5V (F1) 1C2 11
D8 3 2D 2 ATN 0
D14 4 5 ATN 6
D13 7 6 ATN 5
D12 8 9 ATN 4
D11 13 12 ATN 3
D10 14 15 ATN 2
D9 17 16 ATN 1
D15 18 19 HET SW DRIVER CONTROL
10

S.A. FLAG
LHWR
U11 G1 1 20 +5V (F1) 1C2 11
D8 3 2D 2 DISP 8
D11 4 5 NC
D13 7 6 DISP 13
D15 8 9 DISP 15
D10 13 12 DISP 10
D14 14 15 DISP 14
D12 17 16 DISP 12
D19 18 19 DISP 9
10

U6 G1 1 20 +5V (F1) 1C2 11
D7 3 2D 2 NC
D0 4 5 DATA OUT CLK
D3 7 6 COUNTED SIGNAL SEL
D1 8 9 DATA OUT STROBE
D2 13 12 COUNT PERIOD SEL
D6 14 15 J1-12
D5 17 16 J1-11
D4 18 19 J1-10
10

D/A
8 KV

X-AXIS SWEEP

U5 DAC 20 +15V (F1)
D0 15 D1 16 D2 17 D3 18 D4 19 D5 5 D6 6 D7 7 D8 8 D9 9
A 0/1023
Io1 12
Io2 11
G 1 EN 2
+5V (F1) R20 1k 3
[R FB] 14
[±VREF] 13
10
R3 1k
-15V (F1)
R2 2150
C3 22p
U4B (NO
6
5

U22A EN 1 20 +5V (F1) C15 0.1µ
U22B EN 19
A 2 B 4 C 6 D 8
18 OS CLK
16 OS DATA
14 REF CLK
12 REF DATA
9 SUM CLK
7 SUM DATA
5 FM CLK
3 FM DATA
10

U16 G1 1 0 +5V (F1) 1C2 11
0 3 2D 2 A
1 4 5 B
2 7 6 C
3 8 9 D
4 13 12
5 14 15
6 17 16
7 18 19
10

U17 G1 1 20 +5V (F1) 1C2 11
D0 3 2D 2 MOD D0
D1 4 5 MOD D1
D2 7 6 MOD D2
D3 8 9 MOD D3
D4 13 12 MOD D4
D5 14 15 MOD D5
D6 17 16 MOD D6
D7 18 19 MOD D7
10

U18 G1 1 20 +5V (F1) 1C2 11
D4 3 2D 2 MOD CLK
D6 4 5 ATN LEV TRIG
D2 7 6 HP-IB SC
D0 8 9 KB RESET KEYS
D5 13 12
D1 14 15 KB RESET RPG
D7 17 16 ATTN RPP RESET
D3 18 19 ATTN BD TRIG
10

U9 G1 1 20 +5V (F1) 1C2 11
D0 3 2D 2 DISP 16
D3 4 5 DISP 19
D4 7 6 DISP 20
D6 8 9 DISP 22
D7 13 12 DISP 23
D5 14 15 DISP 21
D2 17 16 DISP 18
D1 18 19 DISP 17
10

U7 G1 1 20 +5V (F1) 1C2 11
D4 3 2D 2 NC
D5 4 5 NC
D6 7 6 NC
D7 8 9
D0 13 12 MUX 0
D1 14 15 MUX 1
D3 17 16 MUX 3
D2 18 19 MUX 2
10

ATTENTION
Static Sensitive
Devices

+5V (F1) CR4 R4 1k
CR3
R5 2150
R23 2150
Z-AXIS

VM
MUX 0-3
4 KM 10

P/O P2 P/O A5 SS62
WR A 40 WR B 42 / 2 37
SAWR OSCILLATOR SELECT BI 26
DIVIDER CONTROL LINE DIV 2 RR 41
P/O P3 P/O A5 SS60
/ 0 2 / 1 3
DIVIDER CONTROL LINES DIV 0, 1 EK 41
T BD 1
HET BAND JS 45

P/O P2 P/O A5 SS62
OS CLK 41
OS DATA 43
REF CLK 45
REF DATA 50
SUM CLK 49
SUM DATA 48
FM CLK 46
FM DATA 44
OUTPUT SECTION CONTROL LINES HI 44
REF LOOP CONTROL LINES DC 33
SUM LOOP CONTROL LINES DZ 39
FM CONTROL LINES IF 24

P/O P3 P/O A5 SS60
MOD D0 9
MOD D1 15
MOD D2 17
MOD D3 23
MOD D4 22
MOD D5 18
MOD D6 14
MOD D7 10
MODULATION ADDRESS/ DATA LINES GK 18

CNT INT DIS KF 9

Scans by ArtekMedia => 2009

X-AXIS SWEEP

U6 U18 U9 U7 U5 U4B (NOTE)

DISP 8 NC DISP 13 DISP 15 DISP 10 DISP 14 DISP 12 DISP 9

MOD CLK ATN LEV TRIG HP-IB SC KB RESET KEYS KB RESET RPG ATTN RPP RESET ATTN BD TRIG

DISP 16 DISP 19 DISP 20 DISP 22 DISP 23 DISP 21 DISP 18 DISP 17

NC NC NC MUX 0 MUX 1 MUX 3 MUX 2

DATA OUT CLK COUNTED SIGNAL SEL DATA OUT STROBE COUNT PERIOD SEL J1-12 J1-11 J1-10

D/A 8 KV

VM MUX 0-3 KM 10

CNT INT DIS KF 9

MODULATION ADDRESS/ DATA LINES GK 18

X-AXIS SENSE KN 10

DOUBLER CONTROL LINES JH 51

FRACTIONAL N CONTROL LINES CB 29

OSCILLATOR CONTROL ENABLE CC 29

ATTENUATOR DRIVER CONTROL KZ 54

HET SW DRIVER CONTROL LB 54

P/O SERVICE CONNECTORS

Z AXIS, X AXIS OV 12

LCD DRIVER INPUTS LD 2

LCD SERIAL IN DATA LC 2

COUNTER CLOCK IH 24

COUNTER CONTROL LINES IG 24

RPP RESET LE 54

ATN LEVEL TRIG LF 54

ATN BAND TRIG LG 54

MODULATION CLK GJ 18

HP-IB SC OR 4

RESET RPG (L) LI 2

RESET KEYS (L) LJ 2

SS11

Figure 8G-109
8G-109

CHANGES

All Serial Prefixes

On the component locator:

- J3-J6 - Change the connector reference designators as follows:

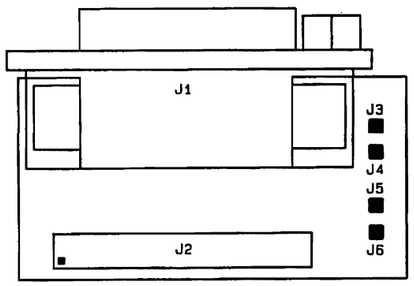
  J3 to J5
  J4 to J6
  J5 to J4
  J6 to J3

- Write "A15" at the bottom right below the diagram

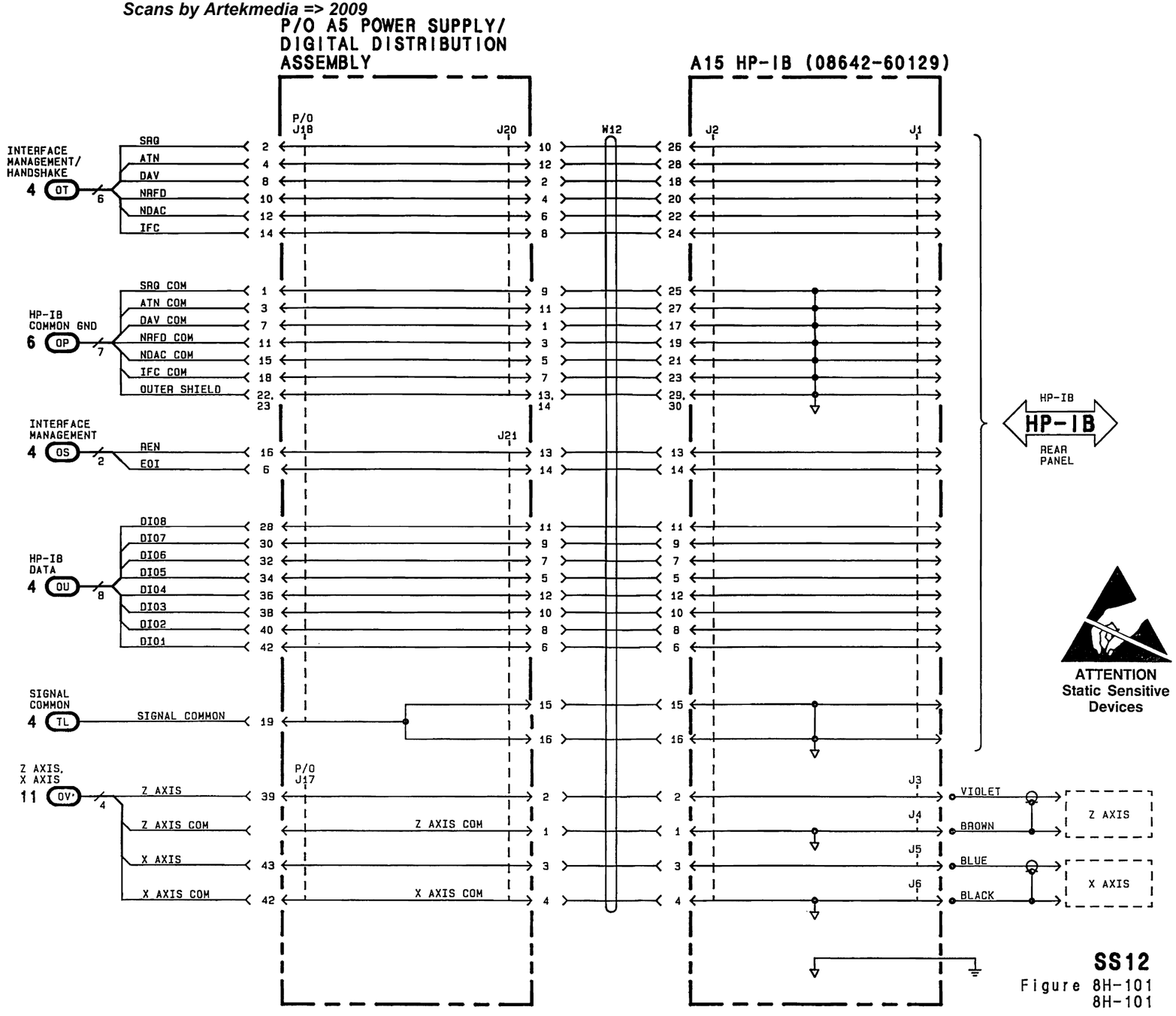
2816A and above

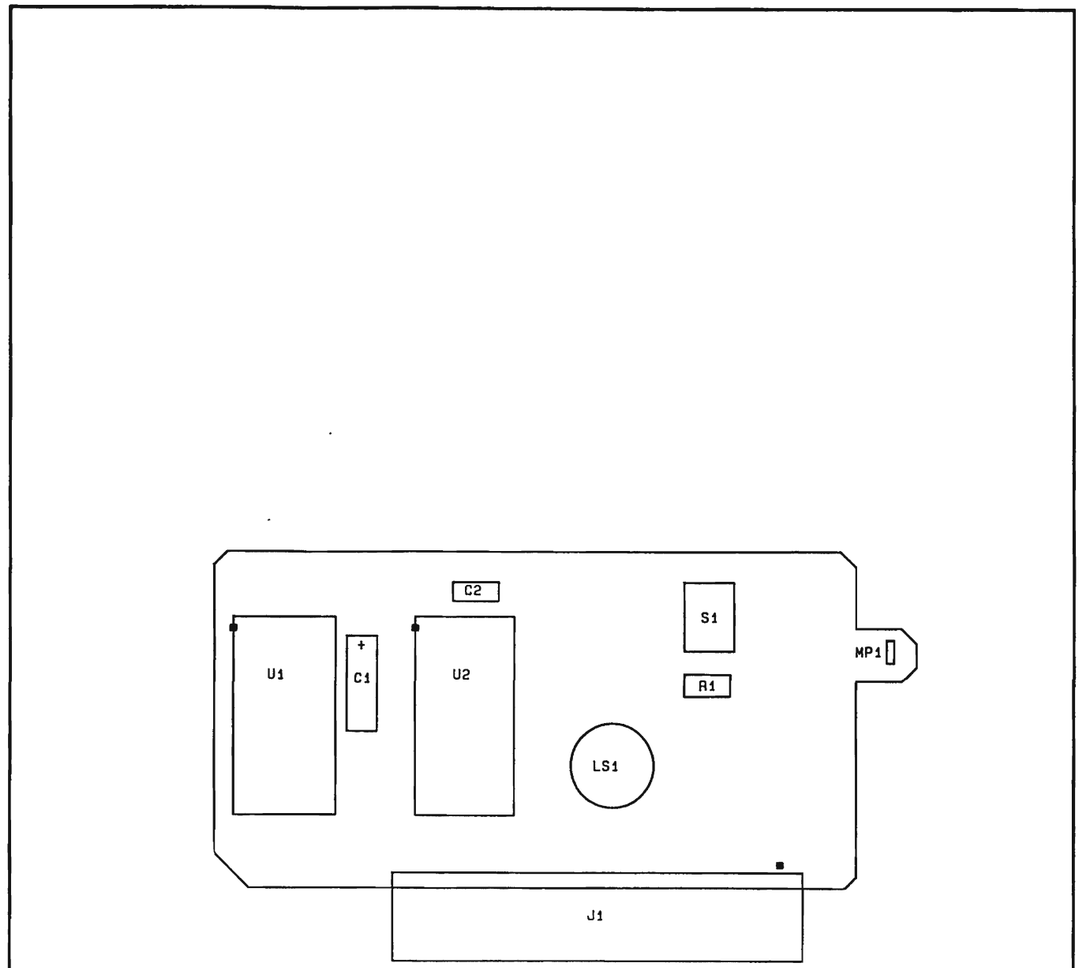
On the schematic:

- In the upper left hand portion of the schematic change the assembly part number to 08642-60229.



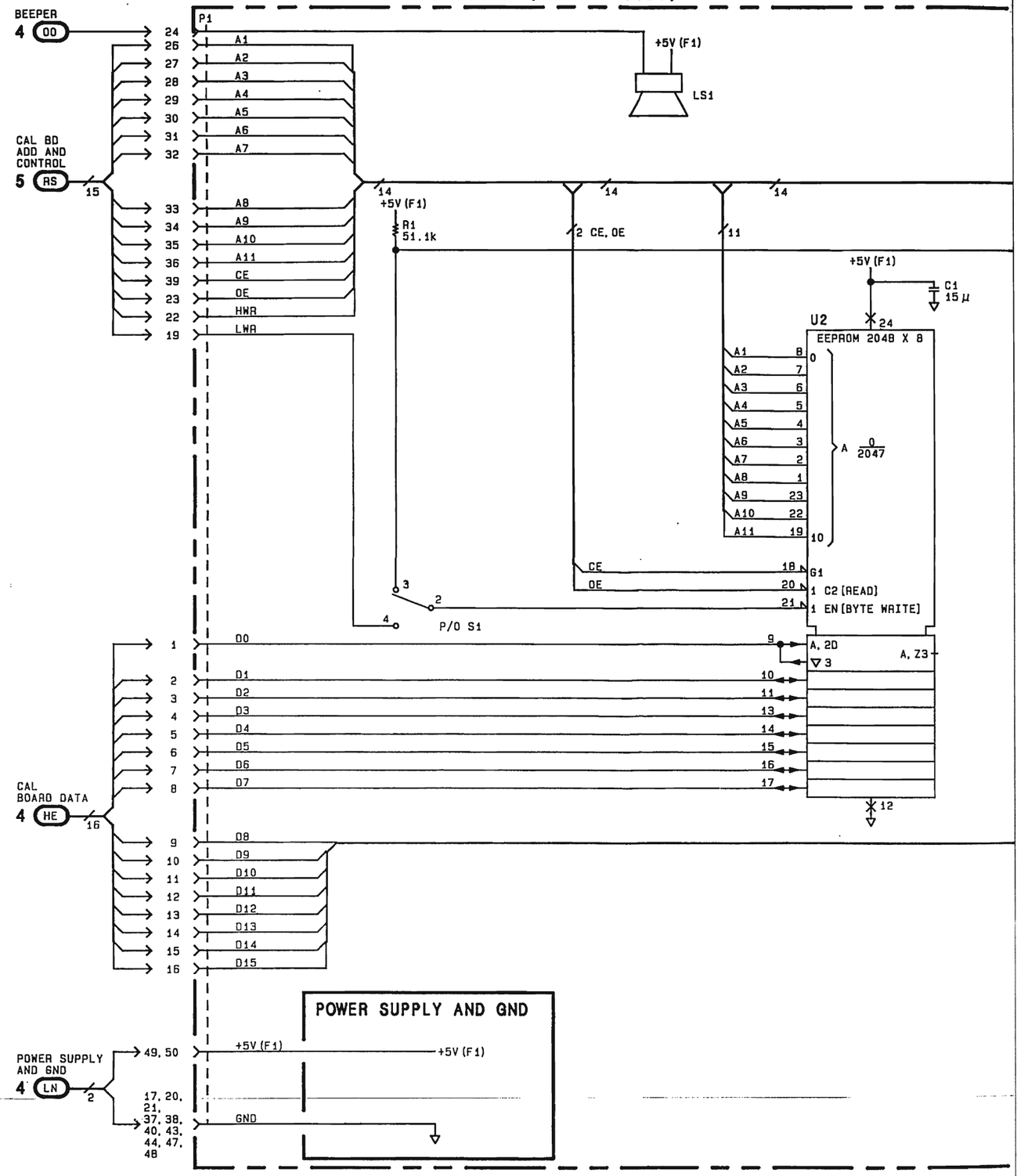
Component Locator



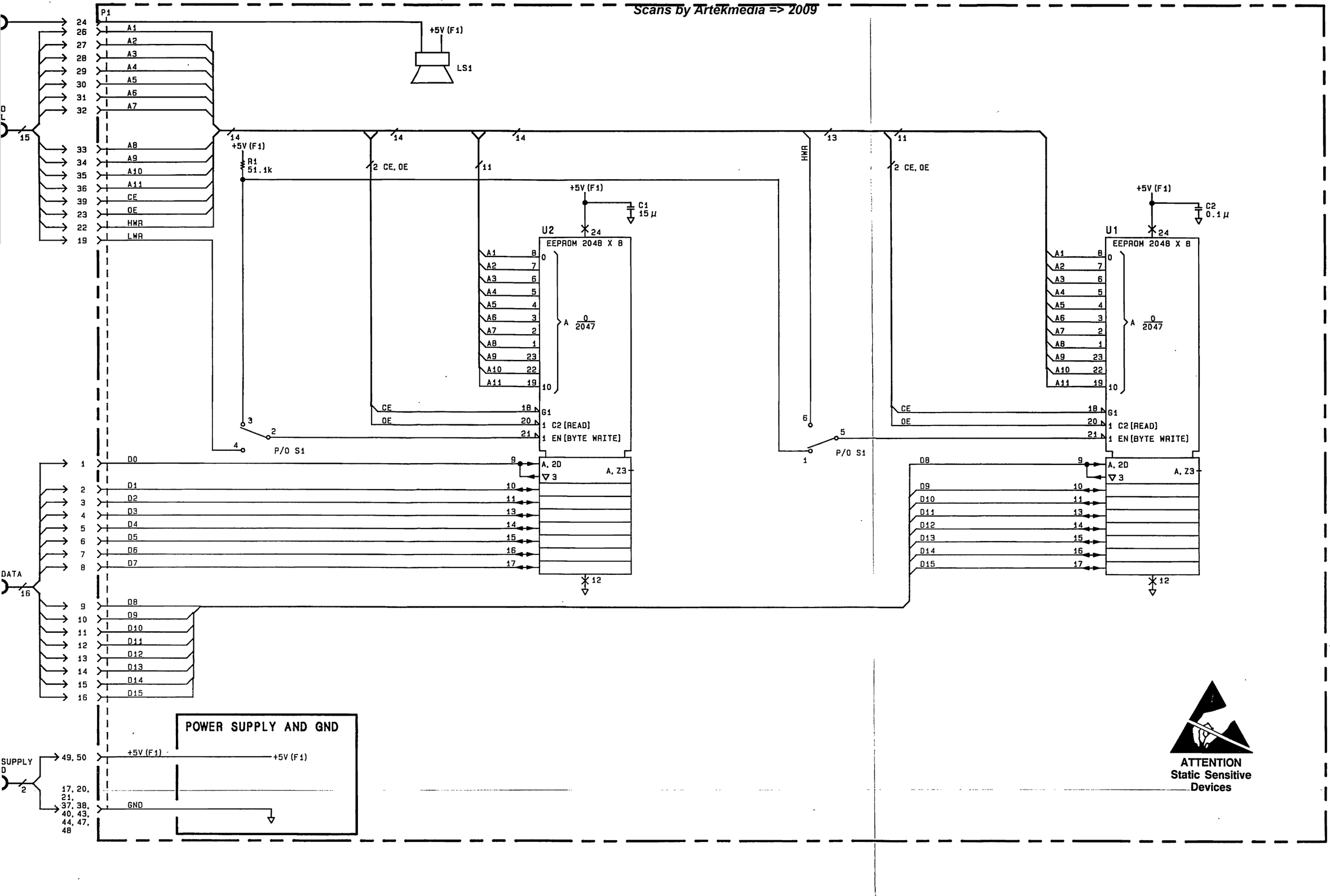


Component Locator

A20 CALIBRATION DATA MODULE (08642-60133)



A20 CALIBRATION DATA MODULE (08642-60133)



ATTENTION
Static Sensitive
Devices

A2 Module

Troubleshooting and Adjustments Contents

Troubleshooting

Adjustments

Troubleshooting

A2 TROUBLESHOOTING INFORMATION

Before Proceeding With Module Troubleshooting

- You should have confidence that A2 is the faulty module from Module Level Diagnostics (MLD) results. (Refer to Instrument Level Troubleshooting, HP 8642 Service Manual).
- Open the HP 8642 manual to the foldout on page 8J-100. There are three diagrams of A2 (the Modulation Module). One diagram is titled Simplified Block Diagram. It is a block diagram intended to be used to understand the basic operation of A2. A Test Point/Adjustment Location diagram is also provided. This diagram is to be used during troubleshooting Checks for BD5 when Test Point bullets ((XX)) are given, usually in tables.

There is another Simplified Block Diagram and Test Point/Adjustment Location diagram opposite BD6 (page 8J-102).

- Look at the foldouts on BD5 (page 8J-101), and BD6 (page 8J-103). There, you will see more detailed Block Diagrams of the Modulation Module.
- The objective of Troubleshooting Checks is to isolate the malfunction to an area of circuitry represented on one Service Sheet. The Checks are intended to be done in the order they are numbered.
- Once the malfunction is isolated, refer to the Component Level Repair Directory. There, you will find tables that contain information useful for locating faulty components.
- Specification failures (for example, phase noise, spurs, etc.) might not be found by Troubleshooting Checks. Manual Adjustments and Auto Adjust Procedures can be done, and the HP 8642 then re-tested to see if the specific failure condition still exists. At this point, if repair is necessary, Module Performance Checks may be helpful to pinpoint a failure condition in the module.

Overall Equipment List

Oscilloscope	HP1980B
Digital Voltmeter (DVM)	HP3456A
HP 8642 Bench Service Kit	HP 11802A
Audio Analyzer	HP 8903A
Pulse/Function Generator	HP 8116A
Logic Probe (Part of signature multimeter)	5005B

Essentials of A2 Module Operation

The A2 Modulation Module has two basic purposes:

1. To generate low distortion audio signals for the HP 8642's internal modulation source and modulation output.
2. To pass external audio signals form the HP 8642's external modulation inputs to the AM and FM modulators.

Refer to Figure 8J-100, Simplified Block diagram, for the following discussion. This Block Diagram shows the **OSCILLATOR** and **FM** circuitry. The **OSCILLATOR** (SS14 & 15) is composed of two basic parts; the oscillator, and an ALC Loop for accurate oscillator output level control. The **FM** circuity (SS17) contains an **INTERNAL/EXTERNAL SWITCH, LEVEL ADJUST,** and **FM RANGE SELECT** attenuator. For further detail on these circuits read the SS14, SS15, and SS17 Essentials of Circuit Operations.

Refer to Figure 8J-102, Simplified Block Diagram for the following discussion. This shows the **MODULATION CONTROL LATCHES** (SS18), the **AM/ PULSE** circuits (SS16), and the A2 Module **DIAGNOSTICS** (SS16). The control latches hae a **DATA LATCH SELECT** which address the appropriate data latch, and the individual control latches, which control the rest of the A2 circuitry. The **AM/PULSE** circuits consist of **INTERNAL/EXTERNAL** input switching, **SELECT**, which routes the **AM** audio signal to either the **A13** module for carrier frequencies below 1057.5 MHz, or to the A19 module (HP 8642B only) for carrier frequencies and status information to the HP 8642's internal voltmeter and controller. For further detail on these circuits refer to the SS16 and SS18 Essentials of Circuit Operations.

CHECK 1: A2 CONTROL CIRCUITRY (SS18)

Essentials of SS18 Circuit Operation

To get control data (73 bits total) onto the A2 Modulation Module, an 8-bit wide data receiver is used. Data enters the A2 Module on the DO-D7 lines (J1-1 thru 8) and the clock line on J11. To get data into an individual latch, an 8-bit address is put on the data lines while the Modulation CLK (GJ) is held low. When this line goes high, the address is latched into U31. A proper address in U31 causes one of the outputs of either U31 or U32 to go low, which in turn enables one of the data latches (U42, 41, 46, 22, 7, 8, 16, 24, or 23). Then, actual data is put on the 8-bit data bus, and when the clock line goes low, the data is clocked into the enabled data latch. Three control lines, CNT INT (EY), and OSC DC (OY) are affected directly by clocking in an address only, and are cleared when a new address is clocked in. From the data latches, control lines go to where they are needed on the Mod board.

Description of Check 1

This is a check of the A2 control circuitry. You will set control bits to their high and low states, using the HP 8642 Service Mode as instructed in tables. You will also "pulse" outputs using the Service Mode and verify them with a Logic Probe. If a test fails, refer to the Component Level Repair Directory.

Required Equipment:

Logic Probe (Part of signature multimeter) ..... HP 5005B
Digital Voltmeter (DVM) HP3456A

Test the Power Supply (from SS14)

1. Setup:

   Switch the HP 8642 to Standby.

   Swing the HP 8642 front panel open to access A2. (Refer to the Disassembly Procedures if you are unfamiliar with this procedure).

   Switch the HP 8642 on.

2. Measure Voltage Levels:

   Check the **POWER SUPPLY AND GND** line voltages at the points given in Table 8J-1. (Locations can be found on the Component Locator on page 8J-104.)

Table 8J-1. A2 Power Supply Lines

Component	Nominal Voltage
C 119	≈ +15V
C 127	≈ +15V
C 121	≈ −15V
C 123	≈ +5V
C 125	≈ −5V
Cathode CR1	≈ +15V
TP 30	GND

Test Logic States on the Control Lines

3. Measure Voltages:

   Key in [SHIFT] [SPCL] [3] to enter Service Mode.

   Key in each service function listed in Tables 8J-2, 8J-3, 8J-4, 8J-5, 8J-6, 8J-7, 8J-8 and 8J-9 and use the Logic Probe or DVM to measure the TTL level at the points listed. (TTL "1" = 2.0 Vdc to 5.1 Vdc, TTL "0" = 0 Vdc to 0.8 Vdc.)

Table 8J–2. *FM Dac Bits (SS17)*

Service Function	Data Bit no. / A2U11 (GH) Pin no.	9 / 4	8 / 5	7 / 6	6 / 7	5 / 8	4 / 9	3 / 10	2 / 11	1 / 12	0 / 13
6 1 2 3 4 1 HZ		0	1	0	1	0	1	0	1	0	1
6 1 2 6 8 2 HZ		1	0	1	0	1	0	1	0	1	0

Table 8J–3. *AM DAC Bits (SS16)*

Service Function	Data Bit no. / A2U5 (FR) Pin no.	11 / 4	10 / 5	9 / 6	8 / 7	7 / 8	6 / 9	5 / 10	4 / 11	3 / 12	2 / 13	1 / 14	0 / 15
6 1 2 5 4 6 1 HZ		0	1	0	1	0	1	0	1	0	1	0	1
6 1 2 6 8 2 6 HZ		1	0	1	0	1	0	1	0	1	0	1	0

Table 8J–4. *Mod Out Dac Bits (SS14)*

Service Function	Data Bit no. / A2U47 (EW) Pin no.	9 / 4	8 / 5	7 / 6	6 / 7	5 / 8	4 / 9	3 / 10	2 / 11	1 / 12	0 / 13
6 1 2 8 5 3 3 HZ		0	1	0	1	0	1	0	1	0	1
6 1 2 8 8 7 4 HZ		1	0	1	0	1	0	1	0	1	0

Table 8J–5. *Oscillator Dac Bits (SS14)*

Service Function	Data Bit no. / A2U43 (ES) Pin no.	9 / 4	8 / 5	7 / 6	6 / 7	5 / 8	4 / 9	3 / 10	2 / 11	1 / 12	0 / 13
6 1 2 1 2 6 2 9 HZ		0	1	0	1	0	1	0	1	0	1
6 1 2 1 2 9 7 0 HZ		1	0	1	0	1	0	1	0	1	0

Table 8J–6. *Oscillator FET Bits (SS14)*

Service Function	Oscillator FET Bit no. A2U45 (ER) Pin no.	0 1	1 9	2 8	3 16
6 1 2 1 7 7 4 9 HZ		1	0	1	0
6 1 2 1 9 1 1 4 HZ		0	1	0	1

Table 8J–7. *AM/FM Control Bits (SS18)*

Service Function	A2 IC–Pin	AM LNA Gain (FN) U1–9	EXT AM (FO) U8–9	INT AM (FO) U8–6	INT FM (GN) U16–12	EXT FM (GN) U16–15	EXT FM W/PRE (GF) U16–19	FM INV HI (GE) U16–16
6 1 2 1 7 7 4 9 HZ		1	0	1	0	1	0	1
6 1 2 1 9 1 1 4 HZ		0	1	0	1	0	1	0

Table 8J–8. *Mux, HI/LO, and Self Test Bits (SS18)*

Service Function	A2 IC–Pin	MUX SEL S0 (FU) U22–15	MUX SEL S1 (FU) U52–16	MUX SEL S2 (FU) U22–9	Self Test (FJ) U8–5	HI/LO RESET (FW) U39–2,3	HI/LO AM/FM (FP) U14–9
6 1 2 2 0 5 0 1 HZ		0	1	0	1	0	1
6 1 2 2 0 5 2 2 HZ		1	0	1	0	1	0

Table 8J–9. *Int/Ext Count and Osc DC Bits (SS18)*

Service Function	A2 IC–Pin	OSC DC (OY) U32–15	CNT EXT (EY) U32–10	CNT INT (EY) U32–9
6 1 2 2 8 6 7 2 HZ		1	1	0
6 1 2 2 8 6 7 3 HZ		1	0	1
6 1 2 2 8 6 7 4 HZ		0	1	1

Test the Control Lines While Pulsed

4. Key in [SHIFT] [SPCL] [3] to enter Service Mode.
5. In Tables 8J-10 and 8J-11, place the Logic Probe on the I.C. and pin number specified, then key in the service function for that pin number. The Logic Probe should indicate that a positive pulse occurred.

Table 8J-10. *AM/FM, AC/DC Control Bits (SS18)*

Service Function*	Line Label	Test Point	Result
[6][1][2][2][4][6][4][0][HZ]	FM AC [GD]	A2U16 pin 9	Pulse
[6][1][2][2][4][7][0][4][HZ]	FM DC [GD]	A2U16 pin 6	Pulse
[6][1][2][2][4][8][3][2][HZ]	AM AC [FK]	A2U41 pin 6	Pulse
[6][1][2][2][5][0][8][8][HZ]	AM DC [FK]	A2U41 pin 2	Pulse
[6][1][2][2][5][6][0][0][HZ]	DBL AM [FS]	A2U16 pin 5	Pulse
[6][1][2][2][6][6][2][4][HZ]	NOR AM [FS]	A2U16 pin 2	Pulse

* These bits are automatically pulsed high.

Table 8J-11. *Attenuator Control Bits (SS18)*

Service Function *	Line Label	Test Point	Result
[6][1][2][2][4][5][7][7][HZ]	36 dB IN [GG]	A2U23 pin 12	Pulse
[6][1][2][2][4][5][7][8][HZ]	36 dB OUT [GG]	A2U23 pin 6	Pulse
[6][1][2][2][4][5][8][0][HZ]	18 dB IN [GG]	A2U23 pin 2	Pulse
[6][1][2][2][4][5][8][4][HZ]	18 dB OUT [GG]	A2U23 pin 5	Pulse
[6][1][2][2][4][5][9][2][HZ]	9 dB IN [GG]	A2U23 pin 9	Pulse
[6][1][2][2][4][6][0][8][HZ]	9 dB OUT [GG]	A2U23 pin 15	Pulse

* These bits are automatically pulsed high.

CHECK 2: A2 MODULATION OSCILLATOR AND ALC LOOP (SS14 AND SS15)

Essentials of SS14 and SS15 Circuit Operation

SS14 shows the **Oscillator, Output Amplifier, Zero Crossing Detector** and **Int/Ext Count Select** circuitry.

The **OSCILLATOR** is a state variable oscillator design; that is, it is formed by combining various functions (amplification, inversion, summation, and integration). It is made up of three circuit blocks; **INTEGRATOR 1 (U44), INTEGRATOR 2 (U34),** and **UNITY GAIN INVERTING AMPLIFIER (U34),** and **unity gain inverting amplifiers (U49).** Each Integrator causes 270° phase shift (90° plus an inversion) and the inverting amplifier provides an additional 180° phase shift. This results in 720° total phase shift around the loop which results in positive feedback, a necessary condition for oscillation. Coarse frequency tuning is accomplished by switching integrator capacitor values (five ranges switched by U45 and U35). Frequency fine tuning is performed using DAC's U43 and U35, which act as variable resistors with 1023 steps in resistance settings. The Oscillator output is from **INTEGRATOR 1 (TP1).** Oscillator amplitude is controlled by the ALC circuitry (SS15) which provides an ALC signal at the input to the **UNITY GAIN INVERTING AMPLIFIER (U49).** The ALC signal has variable amplitude and is either 0° or 180° out of phase with the oscillator signal at the input to the inverting amplifier. The two signals are summed in the inverting amplifier with the resulting amplitude out controlling the oscillator amplitude. The ALC loop holds the oscillator output amplitude at 3.9 Vp.

The output from the **OSCILLATOR** goes to the **OUTPUT AMPLIFIER (U48).** The output Amplifiers gain is controlled by DAC U47 in 1023 steps. This output drives both the Modulation Output (HP 8642 Front panel) and the AM/FM modulation circuits. R19 defines the 600Ω output impedance for the Modulation output.

The **ZERO CROSSING DETECTOR** provides two control pulses to the ALC circuits. **SAMPLED VALUE TRANSFER** (FA) and **PEAK DETECTOR** (FB) . Both pulses are approximately 2 us TTL low pulses.

The **INT/EXT COUNT SELECT** circuit switches between the internal source or an external source for modulation frequency counting.

SS15 shows the **PEAK DETECTOR, SAMPLED VALUE TRANSFER, ERROR VOLTAGE AMPLIFIER, ALL INTEGRATOR, and ALC LOOP MULTIPLIER circuits of the ALC Loop.**

The Peak Detector U36A-U36B combination acts as a peak-hold circuit. R52 and C41 improve "MOD OUT", "INT AM" and "INT FM" flatness at 100 kHz by rolling off the input to the peak detector making the ALC loop output slightly more power to offset the loop's roll off.

When the osc output voltage rises above zero, U36A's output voltage rises to one diode drop above the oscillator voltage such that the output of buffer U36B directly follows the rising osc voltage. When the oscillator passes its positive peak, however, U36A's output voltage drops to one diode drop below the oscillator's output voltage, back-biasing CR6, forward-biasing CR5, and holding U36B's output at the peak osc voltage. At this point Sampled Value Transfer switches U37 A,B and C and **ALC INTEGRATOR SWITCH U37C** close for about 2 uS, transferring the peak sample to hold capacitor C40. On the negative osc output peaks, U37D momentarily closes, discharging peak detecting cap C42 and resetting the peak detector's output to zero.

ERROR VOLTAGE AMPLIFIER U38A acts as an error voltage amp by subtracting a fixed reference from the sampled peak voltage. When the voltage across C40 is 6.9V, the output U38A is OV. This error voltage is then integrated by ALC integrator U38A in order to remove static level errors by forcing the steady-state error voltage to be zero. For example, if the oscillators amplitude is too low, the voltage across C40 will be below 6.9V, causing the output of the error voltage amp, U38A, to be negative. This error voltage is then inverted and integrated by **ALC INTEGRATOR** U38B, which then applies a positive-going control voltage to the noninverting input of the **ALC MULTIPLIER**, U53-4. This will increase the positive feedback in the OSC LOOP, causing oscillation amplitude to grow until the sampled peak voltage on C40 becomes a 6.9V. At this point, the error amp output voltage becomes zero, and the output of the **ALC INTEGRATOR** ends up holding whatever constant control voltage is necessary to maintain oscillator amplitude.

U53 and U54 form the feedback control analog portion of the **ALC LOOP**. The ALC feedback, **(ALC LOOP MULTIPLIER** (ET) **)** which comes from the output of op-amp U54, is essentially the product of the voltage at U53-9 (the OSC LOOP output) and the difference in the voltages between U53-4 and U53-8 (the ALC LOOP output control voltage).

The **OSCILLATOR's** frequency is set by a successive approximation routine using the instruments controller and the counter on the A6 FM/Timebase/counter module. The controller sets the range switches on the Integrators for the proper range, then successively counts the oscillators frequency and changes the DAC settings on the Integrator DAC's until the frequency is within +/− 1% of the desired frequency.

Description of Check 2

This check tests the Modulation Oscillator shown on BD5 and SS14, and the ALC loop shown on BD5 and SS15.

First, you will use the Audio Analyzer to simulate the ALC Loop Multiplier signal, and verify correct operation of the Oscillator bands.

The Zero Crossing Detector and Int/Ext Count Select (also on SS14) are tested next.

The ALC loop on SS15 is then verified for correct operation.

Finally, you will use the Audio Analyzer and DVM to further test the Oscillator for the correct frequency resolution, level accuracy, output distortion, and DC offsets.

If a test fails during Check 2, refer to the Component Level Repair Directory.

Required Equipment:

Audio Analyzer	HP 8903B
Digital Voltmeter(DVM)	HP 3456A
Oscilloscope	HP 1980B

Test the Oscillator Operation

1. Setup:

   Switch the HP 8642 to Standby.

   Disable the ALC loop by desoldering A2 R13 at the lead nearest A2 U54.

   Connect the Audio Analyzer output to the desoldered lead of A2 R13 (ET) .

   Connect the Audio Analyzer Input to A2 TP1.

   Switch the HP 8642 on.

   Key in: [SHIFT] [SPCL] [3], [6] [1] [2] [1] [3] [3] [1] [1] [Hz] to set the oscillator DAC's to their highest setting.

2. Measure Frequency and Voltage Levels:

   Key in [SHIFT] [SPCL] [3] to enter Service Mode. Then key in each Service Function in Table 8J-12, set the Audio Analyzer output to the frequency and amplitude indicated.

   Then Measure the output signal at A2 TP1 with the Audio Analyzer for each Service Function in Table 8J-12. You should measure a peak signal of 0.5V or greater at a frequency within the limits given.

Table 8J–12. *Oscillator Bands*

Band	Service Function	Audio Analyzer Output	Freq Limit
1	6 1 2 1 8 2 4 0 HZ	79 Hz @ 250 mV	71.5 to 87.5 Hz
2	6 1 2 1 8 1 1 2 HZ	434 Hz @ 250 mV	399 to 484 Hz
3	6 1 2 1 7 8 5 6 HZ	2.87 kHz @ 250 mV	2.58 to 3.16 kHz
4	6 1 2 1 7 3 4 4 HZ	18.53 kHz @ 250 mV	16.7 to 20.4 kHz
5	6 1 2 1 8 3 6 8 HZ	100.0 kHz @ 250 mV	98 to 118 kHz

Test the Zero Crossing Detector

3. Setup:

   Ensure Setup has not changed from Step 2.

   The HP 8642 display should still be displaying 1984 from Step 2. If not Key in: SHIFT SPCL 3, 6 1 2 1 1 3 3 1 1 Hz, 6 1 2 1 8 3 6 8 Hz.

   Connect Channel 1 of the Oscilloscope to A2 TP2 (EX) .

   Connect Channel 2 to A2 TP6.

   Switch the HP 8642 on.

4. Verify Waveforms:

   The signal at TP 6 should be a TTL signal that is in phase with the signal at TP 2.

   Move the Channel 2 probe to TP 7. The signal at TP 7 should be a TTL signal that is 180 ° out of phase with the signal at TP 2.

Test the Int/Ext Count Select Lines

5. Setup:

   The Set on has not changed from Step 4.

   Connect Channel 1 of the Oscilloscope to A2 TP5.

   Connect Channel 2 of the Oscilloscope to A2 TP6.

   Key in: 6 1 3 1 Hz.

6. Verify Waveform:

   The signal at A2 TP5 should be the same as the signal at A2 TP6.

   Key in: 6 1 3 0 Hz to select External Count.

NOTE

There should be no signal connected to the HP 8642's AM/PULSE input (front or rear panel).

There should be no signal present at A2 TP5.

Using a jumper, connect A2 TP6 to A2 TP 19 (Ext Count) (EZ) .

The signal at A2 TP5 should be the same as the signal at A2 TP6.

Key in: [6] [1] [3] [0] [Hz].

Test the ALC Loop Feedback (SS15)

7. Setup:

Ensure that A2 R13 is desoldered at the lead nearest U54, and that the Audio Analyzer is connected to A2 R13.

Key in: [SHIFT] [SPCL] [3], [6] [1] [2] [1] [7] [8] [5] [6] [Hz] to select Band 3.

Key in: [6] [1] [2] [1] [3] [3] [1] [1] [Hz] to set the HP 8642 frequency to the high end of Band 3.

Change the Audio Analyzer's frequency to 2.87 kHz and 250 mV.

Connect Channel 1 of the Oscilloscope to A2 TP1 (Osc Detect) (EV) .

Adjust the Audio Analyzer's frequency setting for the maximum signal at A2 TP1 ≈7V peak.

Adjust the Audio Analyzer's amplitude to obtain 8V peak at A2 TP1.

Connect A2 TP12 (ALC Loop Multiplier) (ET) to Channel 2 of the Oscilloscope.

8. Measure Voltage Levels:

The signal at A2 TP12 should be ≈7V peak and 180° out of phase with the signal at A2 TP1. The signal at A2 TP11 should be ≈ −14 Vdc.

Adjust the Audio Analyzer's amplitude to obtain 6V peak at A2 TP1.

The signal at A2 TP12 should be ≈6V peak and in phase with the signal at A2 TP1.

The signal at A2 TP11 should be ≈14V DC.

NOTE

The DC voltage at A2 TP11 determines the amplitude and phase of the signal at A2 TP12. A negative DC voltage produces a signal at A2 TP12 that is 180 ° out of phase with the signal at A2 TP1. A positive DC voltage produces a signal at A2 TP12 that is in phase with the signal at A2 TP1.

The further the DC voltage is from 0V, the greater the amplitude of the signal at A2 TP12.

Test the Oscillators Frequency Resolution

9. Setup:

Switch the HP 8642 to Standby.

Reconnect A2 R13 to the A2 board.

Connect A2 TP1 (Int Osc) to the HP 8903's high input.

Switch the HP 8642 on.

10. Measure Frequencies and Voltage Levels:

    Key in: [SHIFT] [SPCL] [3], [6] [1] [2] [1] [7] [3] [4] [4] [Hz] to select Band 4.

    Key in: [6] [1] [2] [1] [3] [3] [1] [1] [Hz] to set the HP 8642 frequency to the top of Band 4.

    The frequency should be 16.7 kHz to 20.4 kHz.

11. Adjust Frequency:

    Adjust A2 R8 and/or A2 R27 so that the oscillators frequency is 19.998 kHz to 20.002 kHz.

    For each Binary no. in Table 8J-13, key in the Encoded Data no. and verify that the output frequency is within the limits given, and that the output level is between 4.8 Vac to 4.9 Vac.

Table 8J-13. *MOD OSC Freq Resolution*

Encoded Data no.	Binary no.	Lower Limit	Upper Limit
612 13311 Hz	1023	19990 Hz	20010 Hz
612 12800 Hz	512	9990 Hz	10010 Hz
612 12544 Hz	256	4990 Hz	5010 Hz
612 12416 Hz	128	2490 Hz	2510 Hz
612 12352 Hz	64	1240 Hz	1260 Hz
612 12320 Hz	32	615 Hz	635 Hz
612 12304 Hz	16	302 Hz	323 Hz
612 12296 Hz	8	146 Hz	166 Hz
612 12292 Hz	4	68.1 Hz	88.1 Hz
612 12290 Hz	2	29.1 Hz	49.1 Hz
612 12289 Hz	1	9.53 Hz	29.5 Hz

12. Readjust Frequency (R27 and R8):

    Refer to the A2 adjustments at the end of this procedure. Do only the A2R27 and R28 manual adjustments.

Test the Modulation Output DAC (SS14)

13. Setup:

    Connect the MOD OUT port (front or rear panel) to the DVM. Set the DVM to measure Vac.

    Key in: [SHIFT] [SPCL] [3] [6] [1] [2] [1] [7] [8] [5] [6] [Hz] to set the Modulation Oscillator to Band 3.

    Key in: [6] [1] [2] [1] [3] [3] [1] [1] [Hz] to set the Modulation Oscillator DAC to 1023.

    Key in: [6] [1] [2] [9] [2] [1] [5] [Hz] to set the Modulation Output to its maximum amplitude. (Binary 1023 on Output Amplifier DAC).

14. Measure Voltage Levels:

    The MOD OUT signal level should be 4.6 to 5.2 Vac.

    Record the DVM measurement in the block labeled [R ____] in the Result column in Table 8J-14.

15. Generate Table 8J-14:

Using the formulas provided, generate Table 8J-14's upper and lower voltage limits.

$V = R \div 2046$ V _____

$A = R \div 1.998$ A _____

16. Measure Voltages:

For each binary number in Table 8J-14, key in the service function number and verify that the voltage is within the limits calculated in the previous step.

Table 8J-14. *Modulation Output Level DAC Operation*

Service Function	Binary no.	Lower Limit	Result	Upper Limit
6 1 2 9 2 1 5 HZ	1023	4.6 Vac	R_____	5.2 Vac
6 1 2 8 7 0 4 HZ	512	A − V	B_____	A + V
6 1 2 8 4 4 8 HZ	256	(A ÷ 2) − V	C_____	(A ÷ 2) + V
6 1 2 8 3 2 0 HZ	128	(A ÷ 4) − V	D_____	(A ÷ 4) + V
6 1 2 8 2 5 6 HZ	64	(A ÷ 8) − V	E_____	(A ÷ 8) + V
6 1 2 8 2 2 4 HZ	32	(A ÷ 16) − V	F_____	(A ÷ 16) + V
6 1 2 8 2 0 8 HZ	16	(A ÷ 32) − V	G_____	(A ÷ 32) + V
6 1 2 8 2 0 0 HZ	8	(A ÷ 64) − V	H_____	(A ÷ 64) + V
6 1 2 8 1 9 6 HZ	4	(A ÷ 128) − V	I_____	(A ÷ 128) + V
6 1 2 8 1 9 4 HZ	2	(A ÷ 256) − V	J_____	(A ÷ 256) + V
6 1 2 8 1 9 3 HZ	1	(A ÷ 512) − V	K_____	(A ÷ 512) + V
6 1 2 8 1 9 2 HZ	0	− .003 Vac	L _____	+ .003 Vac

Test the Modulation Level Accuracy

17. Setup:

Connect the HP 8642 MOD OUT to the DVM.

Select Vac on the DVM.

Key in: INST PRESET SHIFT MOD OUT ON to turn on the Modulation Oscillator and set the amplitude level to 1V peak.

18. Measure Voltages:

Set the HP 8642 Modulation Oscillator to each frequency given in Table 8J-15 and verify that the output level is between 1.363 and 1.475 Vac.

Table 8J-15. *Level Accuracy*

Modulation Frequency
20 Hz
63.1 Hz
63.2 Hz
398 Hz
399 Hz
1 kHz
2.51 kHz
2.52 kHz
15.8 kHz
15.9 kHz
100 kHz

Test the Modulation Output Distortion

19. Setup:

    Connect the HP 8642 MOD OUT to the Audio Analyzer "High" input.

    Set the Audio Analyzer to measure distortion.

20. Measure Distortion Levels:

    Set the HP 8642 Mod Oscillator to each frequency in Table 8J-16 at a level of 510 mV peak, and verify that the distortion is less than the levels given in Table 8J-16.

Table 8J-16. *Output Distortion*

MOD Frequency	Distortion Level
20 Hz	< 0.02 %
63.1 Hz	< 0.02 %
63.2 Hz	< 0.02 %
398 Hz	< 0.02 %
399 Hz	< 0.02 %
1 kHz	< 0.02 %
2.51 kHz	< 0.02 %
2.52 kHz	< 0.02 %
15.8 kHz	< 0.02 %
15.9 kHz	< 0.15 %
100 kHz	< 0.15 %

Test for MOD OUT DC Voltage Offset

21. Setup:

    Key in: [INST PRESET]

    Connect the MOD OUT to the DVM.

    Select Vdc on the DVM.

    Key in: [SHIFT] [MOD OUT] [ON] to turn on the Modulation Oscillator and set the amplitude level to 1V peak.

22. Measure Voltages:

    Set the HP 8642 Modulation Oscillator to each frequency given in Table 8J-17 and verify that the DC offset level is between −15 mV and +15 mV (dc).

Table 8J-17. *Modulation Frequencies*

MOD Frequency
2.51 kHz
2.52 kHz
15.8 kHz
15.9 kHz
100 kHz

Test the Modulation Oscillator Frequency Accuracy

23. Setup:

    Connect the HP 8642 MOD OUT to the Audio Analyzer "High" input.

24. Measure Frequencies:

    Select each modulation frequency in Table 8J-18 at a level of 1V peak, and verify that the frequency accuracy is within the specified limits.

Table 8J-18.

MOD Frequency	Lower Limit	Result	Upper Limit
20 Hz	19.6 Hz	_____	20.4 Hz
63.1 Hz	61.8 Hz	_____	64.4 Hz
63.2 Hz	61.9 Hz	_____	64.5 Hz
398 Hz	390 Hz	_____	406 Hz
399 Hz	391 Hz	_____	407 Hz
1000 Hz	980 Hz	_____	1020 Hz
2510 Hz	2459.8 Hz	_____	2560.2 Hz
2512 Hz	2461.8 Hz	_____	2562.2 Hz
15800 Hz	15484 Hz	_____	16116 Hz
15900 Hz	15582 Hz	_____	16218 Hz
100000 Hz	98000 Hz	_____	102000 Hz

CHECK 3: A2 FM CIRCUITRY (SS17)

Essentials of SS17 Circuit Operation

Service Sheet 17 shows all of the FM audio circuitry which contains the **FM INPUT AC/DC COUPLER, FM LOW NOISE AMPLIFIER, FM ± UNITY GAIN AMP, INTERNAL FM SWITCH, EXTERNAL FM SWITCH, FM SUMMING AMPLIFIER, FM LEVEL ADJUST,** and the **FM RANGE SELECT.**

External FM and PHASE MOD inputs enter the Modulation module at A2J5. Relay K3 selects either AC or DC input coupling, and R112 defines a 600Ω input impedance. R113, CR12, and CR13 provide input protection to ± 5V whether the instrument is on or off. FM Low Noise Amp U17 amplifies the nominally 1.0 Vp input to 6.9 Vp for both FM and PHASE MOD. R116. R117, VR8, and VR9 limit the output swing of U17 so as not to overload the analog switches that follow in the signal path.

The low noise amp's output feeds into the ± Unity Gain inverting amplifier, U19, which is either switched into or out of the signal path by U18. This allows the user control over the polarity of the freq or phase modulation. Since a negative audio input to the A6 FM module produces an increasing RF output frequency, the default condition is to leave this inverting amp out so that the Mod Section is overall inverting in order to make an increasing front panel audio input cause a positive RF freq shift.

The external audio then feeds into the FM sum amp, U21, through FET switch U9. The internal oscillator, at a fixed 6.9 Vp, also feeds into the sum amp through FET switch U20. For FM with preemphasis, FET switch U10 feeds the external audio through a hardware preemphasis circuit composed of C101, R133, R134, and R135, which places a zero at 212.2 Hz and a pole at about 30 kHz. Internal FM with preemphasis is done by setting the modulation level in software since the mod rate is known. For this reason, int and ext FM with preemphasis cannot be done simultaneously.

The combined Int and Ext audio then goes to a multiplying DAC amp composed of U11 and U12, which has 10 bits of resolution (1024 gain steps between a gain of 0 and −1) and provides for fine adjustment of FM or PHASE MOD deviation. The output of the DAC amp then drives a floating FM Output Drive of U25 and U26, which in turn drives an attenuator composed of K4, 5, and 6 that provides coarse (approximately 9 dB step size) adjustment of the modulation level. The attenuator's output resistance is about 50Ω for noise reasons. Also, the outputs of the FM Output Drive and the attenuator are referenced to the A6 FM Module ground in order to minimize the effects of ground loops between the FM Module and the Modulation module.

Description of Check 3

This check tests the A2 FM circuitry by using the HP 8642 Service Mode. External test equipment is used to measure key circuit points while the circuitry is set up in a pre-determined state.

If a test fails during Check 3, refer to the Component Level Repair Directory.

Required Equipment:

Audio Analyzer ..... HP 8903B
Oscilloscope HP1980B
Digital Voltmeter (DVM) HP3456A

Test the FM AC/DC Input Coupler and Low Noise Amplifier

1. Setup:

   Switch the HP 8642 to standby.

   Connect A2 TP29 (FQ) , FM LNA to the DVM.

   Set the DVM to measure Vdc.

   Switch the HP 8642 on.

2. Measure Voltage Levels:

   Key in [SHIFT] [SPCL] [3] to enter Service Mode.

   Key in each Service Function in Table 8J-19 while verifying that the voltage measured at A2 TP29 is within the limits given.

Table 8J-19. *FM LNA Output*

Service Function	Description	TP 29 Voltage (FQ)
[6] [1] [2] [2] [4] [6] [4] [0] [HZ]	ACFM/Self Test Off	−10 mV to +10 mVdc
[6] [1] [2] [2] [0] [4] [8] [0] [HZ] *	ACFM/Self Test On	8.5 to 9.5 Vdc
[6] [1] [2] [2] [4] [7] [0] [4] [HZ]	DCFM/Self Test On	−10 mV to +10 mVdc
[6] [1] [2] [2] [0] [4] [8] [4] [HZ]	DCFM/Self Test Off	−10 mV to +10 mVdc

* Enabling the self test bit applies a 1 Vdc signal to the FM ac input.

3. Connect an External Source:

   Key in: [INST PRESET].

   Set the Audio Analyzer to 1.4V (1 Vp) and 600Ω output impedance.

   Connect the Audio Analyzer output to the FM/PM Input on the front or rear panel of the HP 8642.

   Set the DVM to measure Vac.

4. Measure Voltages:

   Key in [SHIFT] [SPCL] [3] to enter Service Mode.

   Key in each Service Function in Table 8J-20 while verifying that measured voltages at A2 TP29 are within the limits given.

Table 8J-20.

Service Function	Description	TP 29 Voltage (FQ)
[6] [1] [2] [2] [4] [6] [4] [0] [HZ]	ACFM	4.78 to 4.98 Vac
[6] [1] [2] [2] [4] [7] [0] [4] [HZ]	DCFM	4.78 to 4.98 Vac

Disconnect the DVM from A2 TP29.

Test the FM ± Unity Gain Amp

5. Setup:

   Connect A2 TP25 to the Oscilloscope Channel 2 input.

   Connect A2 TP29 (FQ) to the Oscilloscope Channel 1 input.

   Set the Audio Analyzer to 2 kHz and 1V peak, 600Ω output impedance.

   Connect the Audio Analyzer to the FM/PM Input on the front or rear panel of the HP 8642.

   Key in: [INST PRESET]

6. Verify Waveforms:

   Key in each Function in Table 8J-21 while verifying that the waveform at A2 TP25 is the correct amplitude and the correct phase relationship with A2 TP29.

Table 8J-21.

Function	Waveform at TP 25
[FM] [ON] [EXT AC]	≈5.5 Vpk 180 Out-of-Phase with TP 29
[SHIFT] [SPCL] [1] [1] [5]	≈5.5 Vpk In-of-Phase with TP 29

7. Remove the Oscilloscope from A2 TP25 and A2 TP29.

Test the Int/Ext FM Switches

8. Setup:

   Key in: [INST PRESET]

   Set the Audio Analyzer to set to 2 kHz and 1.4V (1.0 Vpk). Connect the Audio Analyzer to the FM/PM Input on the front or rear panel of the HP 8642.

   Connect A2 TP25 to the Audio Analyzers "High" input.

   Set the Audio Analyzer to measure Vac.

9. Measure Voltages:

   Key in each Function in Table 8J-22 while verifying with the Audio Analyzer that the signal frequency and level at A2 TP25 is within the limits given.

Table 8J-22.

Function	Signal at TP 25
[FM] [ON] [INT]	≈1 kHz @ 3.68 to 3.99 Vac
[EXT] [AC]	≈2 kHz @ 3.68 to 3.99 Vac
[SHIFT] [SPCL] [1] [1] [5]	≈2 kHz @ 3.68 to 3.99 Vac
[SHIFT] [SPCL] [6]	≈2 kHz @ 1.025 to 1.125 Vac

Test the FM Level Adjust DAC

10. Setup:

    Key in: [INST PRESET]

    Key in: [FM] [ON] [INT] to select Internal FM.

    Connect the DVM to A2 TP26.

    Set the DVM to measure VAC.

11. Measure Voltages:

    Key in [SHIFT] [SPCL] [3] to enter Service Mode.

    For each Function in Table 8J-23, verify that the measured and calculated values are within the limits given.

NOTE

For the first Service Function/DAC Setting, verify that the voltage measurement V1 is between the upper and lower limits given. For the rest of the settings, calculate the upper and lower limits by multiplying V1 times the factors given in the table.

Table 8J-23. *A2's FM Level DAC Voltages*

Service Function	DAC Setting	Lower Limit	Voltage At TP26	Upper Limit
[6][1][2][1][0][2][3][HZ]	1023	3.68 Vac	V 1 _____ Vac	3.99 Vac
[6][1][2][5][1][2][HZ]	512	V1 × .5	V 2 _____ Vac	V1 × .501
[6][1][2][2][5][6][HZ]	256	V1 × .2498	V 3 _____ Vac	V1 × .2507
[6][1][2][1][2][8][HZ]	128	V1 × .1246	V 4 _____ Vac	V1 × .1256
[6][1][2][6][4][HZ]	64	V1 × .06207	V 5 _____ Vac	V1 × .06305
[6][1][2][3][2][HZ]	32	V1 × .03079	V 6 _____ Vac	V1 × .03177
[6][1][2][1][6][HZ]	16	V1 × .01515	V 7 _____ Vac	V1 × .01613
[6][1][2][8][HZ]	8	V1 × .007331	V 8 _____ Vac	V1 × .008309
[6][1][2][4][HZ]	4	V1 × .003421	V 9 _____ Vac	V1 × .004399
[6][1][2][2][HZ]	2	V1 × .001466	V 10 _____ Vac	V1 × .002444
[6][1][2][1][HZ]	1	V1 × .0004888	V 11 _____ Vac	V1 × .001466
[6][1][2][0][HZ]	0	−.004 Vac	V 12 _____ Vac	.004 Vac

12. Remove the DVM from A2 TP26

Test the FM Range Select

13. Setup:

    Key in [INST PRESET].

    Remove W20 (GI) from A6A1 J4 and connect W20 to the DVM.

    Key in: [FM] [ON] [INT] to select Internal FM.

    Key in: [SHIFT] [SPCL] [3] [6] [1] [2] [1] [0] [2] [3] [Hz] to set the FM Level Adjust for maximum output.

14. Measure Voltages:

    Key in [SHIFT] [SPCL] [3] to enter Service Mode.

    Key in each Service Function in Table 8J-24 while verifying that the signal level to the DVM is within the limits given.

NOTE

For the first Function no./Attenuation setting, verify that the voltage measurement (V1) is between the upper and lower limits given. For the rest of the settings, calculate the upper and lower limits by multiplying V1 times the factors given in the table.

Table 8J-24. *FM Out Attenuator Operation*

Service Function	Attenuation	Attenuators In	Lower Voltage	Vac At W20	Upper Voltage
[6] [1] [2] [2] [6] [9] [8] [6] [HZ]	0 dB	0 dB	3.68 Vac	V1 _____	3.99 Vac
[6] [1] [2] [2] [6] [9] [7] [0] [HZ]	8.92 dB*	9 dB	V1 × .3544	V2 _____	V1 × .3618
[6] [1] [2] [2] [6] [9] [8] [2] [HZ]	18.43 dB*	18 dB	V1 × .1173	V3 _____	V1 × .1224
[6] [1] [2] [2] [6] [9] [6] [6] [HZ]	27.26 dB*	9 dB, 18 dB	V1 × .04201	V 4 _____	V1 × .04473
[6] [1] [2] [2] [6] [9] [8] [5] [HZ]	36 dB	36 dB	V1 × .01521	V 5 _____	V1 × .01652
[6] [1] [2] [2] [6] [9] [6] [9] [HZ]	44.89 dB	9 dB, 36 dB	V1 × .005408	V 6 _____	V1 × .005997
[6] [1] [2] [2] [6] [9] [8] [1] [HZ]	54.41 dB	18 dB, 36 dB	V1 × .001788	V7 _____	V1 × .002026
[6] [1] [2] [2] [6] [9] [6] [5] [HZ]	63.25 dB	9 dB, 18 dB, 36 dB	V1 × .0006396	V8 _____	V1 × .0007398

* These are the actual Attenuator values.

Test for FM DC Offset

15. Setup:

    Set the DVM to measure Vdc.

    Ensure that the DVM is connected to W20.

    Key in: [INST PRESET].

16. Measure Voltage Levels:

    Select each Function from Table 8J-25 and verify that the voltages are within the limits given.

Table 8J-25.

Function	Lower Limit	Voltage on W20	Upper Limit
FM On, EXT AC	−0.15	A _____	0.15 Vdc
FM Off	−0.15	B _____	0.15 Vdc
Subtract B From A	−0.002	A−B _____	0.002 Vdc

Restore Module

17. Switch the HP 8642 to Standby.
18. Reconnect W20 to A6A1 J4.

CHECK 4: A2 AM CIRCUITRY (SS16)

Essentials of SS16 Circuit Operation

Service Sheet 16 shows the AM modulation circuitry, the **AM/FM HI/LO DETECTOR**, and the **GENERAL DIAGNOSTICS INTERFACE** circuitry of the A2 modulation module.

External AM and PULSE MOD inputs enter the A2 Modulation Module at J2. Relay K1 selects either AC or DC input coupling, and R71 defines a 600Ω input impedance. R70 and CR9-10 provide input protection to +/−5V whether the instrument is on or off. Low noise amp U13 amplifies the nominally 1.0 Vp audio input to 6.9 Vp for AM or 1 Vp for PULSE MOD, selectable by analog switch U1. U13's supply resistors, R72-73, and zener diodes VR6-7 limit the output swing of U13 to avoid exceeding the maximum allowable input voltage of the analog switches that follow.

The audio signal then goes into the **AM Summing Amplifier**, U3, through analog switch U2. The internal oscillator, at a fixed 6.9 Vp, can also be summed in at this pont through U4.

The combined int and ext audio then drives the analog input of the **AM LEVEL ADJUST**, a multiplying DAC amplifier, composed of U5 and U6, which has a gain directly proportional to the binary digital input to the DAC (U5). This gain can be varied from approximately 0 to −1 with 12 bits (4096 steps) of resolution. The DAC amp determines the instrument's actual AM sensitivity, given that the instrument controller knows the AM sensitivity of the rest of the instrument. Relay K2 switches the output to either the instrument's normal or doubled (8642B only) output section, where the actual AM or PULSE modulation takes place. Since a positive audio voltage applied to either output section produces an increasing RF carrier amplitude, the Mod Section must be overall noninverting in order to maintain that relationship at the instrument RF output.

The purpose of the **HI/LO DETECTOR** is to monitor the positive peaks of the AC component of either the **EXT AM** input or the **EXT FM/PHASE MOD** input to see if those audio peaks are within +/− 2% of 1.0 Vp, too high, or too low.

Analog switch U14 selects the output of either the **AM low noise amp,** U13, or the FM low-noise amp, U17 (SS17), as the input to the HI/LO detector. The low-noise amps amplify the nominally 1.0 Vp inputs to 6.9 Vp, which gives about a 6.9:1 improvement to the signal-to-noise (and DC offsets) ratio in the HI/LO detector, which helps reduce measurement errors. C81 and R108 AC couple the detector's input to 20 Hz. U30 is a buffer required to drive the inverting inputs of the HI and LO comparators, U29C and U29D, respectively, which have significant input bias currents. A resistive ladder R102-105, driven from a + 15V reference voltage drives the noninverting inputs of the HI and LO comparators with 6.9V plus and minus 2% respectively.

When the front panel's monitored audio input is too low, both HI/LO comparator's outputs TP18 and TP19 respectively, are in a static high state. When the input level is too high, both comparators' outputs toggle at the external mod rate; and when the input is a nominal 1.0 Vp, only the LO comparator's output is statically high. U28A and B are two one-shots designed to stretch the HI/LO comparators' outputs into statically high and low states. The one-shots' pulse widths were chosen to be about 200 mS in order to guarantee operation below 10 Hz while not making the HI/LO detector's response time excessively long.

In order to interface with the instrument controller, the HI/LO detector must generate an interrupt whenever the status of either the HI or LO line changes. To generate this the R inputs of four S-R latches, U39 1 thru 4 are driven by one-shots U28A and B while a (FW) reset line from the control data receiver drives the S inputs of the latches. While this HI/LO reset line is held low, all four latch outputs are forced high regardless of the status of the HI and LO lines, keeping the MOD HI/LO int (GB) output high (at U40-4). When the HI/LO reset line returns high, however, the outputs of one of the HI latches and one of the LO latches go low while the other two latches outputs remain high, maintaining the Mod HI/LO INT (GB) output at a high level. Now, when the status of either the HI or the LO line (or both) changes states, one (or both) of the remaining high latches goes low, causing the CHANGE line to go low and telling the instrument controller to read the HI/LO detector's status, MOD HI (GB) .

The **GENERAL DIAGNOSTICS INTERFACE** acts as a single pole eight throw FET switch which can connect any one of eight test points in the Mod Section to the internal voltmeter, on the A4 Latch Board. The MUX normally monitors the HI/LO detector's LO line, but can also check several points in the internal oscillator's OSC LOOP and ALC LOOP as well as the Mod Section's audio amplifiers.

Description of Check 4

This check tests the A2 AM circuitry by using the HP 8642 Service Mode. External test equipment is used to measure key circuit points while the circuitry is set up in a pre-determined state.

If a test fails during Check 4, refer to the Component Level Repair Directory.

Required Equipment:

Oscilloscope HP1980B
Digital Voltmeter (DVM) ..... HP 3456A
Audio Analyzer ..... HP 8903B

Test the AM AC/DC Coupler

1. Setup:

   Key in: [INST PRESET]

   Connect the DVM to A2 TP13

2. Measure Voltages:

   Enter [SHIFT] [SPCL] [3] to enter Service Mode.

   Key in each Service Function from Table 8J-26 while verifying that the DC level at A2 TP13 is within limits.

Table 8J-26. *AM Input*

Service Function	Description	Results @ TP 13
[6] [1] [2] [2] [9] [6] [5] [HZ]	AC AM/Self Test Off	−.015 to .015 Vdc
[6] [1] [2] [2] [0] [4] [8] [0] [HZ]	AC AM/Self Test On	.6 to 1.5 Vdc
[6] [1] [2] [2] [7] [2] [2] [1] [HZ]	DC AM/Self Test On	−.015 to .015 Vdc
[6] [1] [2] [2] [0] [4] [8] [4] [HZ]	DC AM/Self Test Off	−.015 to .015 Vdc

Test the AM LNA Gain

3. Setup:

   Connect the Audio Analyzer output to the HP 8642 AM/PULSE input (J1 on the front panel).

   Set the Audio Analyzer for 1 KHz and 1.4 (1.0 Vpk), 600Ω output impedance.

   Connect the DVM to A2 TP14.

   Set the DVM to measure Vac.

4. Measure Voltages:

   Key in [SHIFT] [SPCL] [3] to enter Service Mode.

   Key in each Service Function from Table 8J-27 while verifying correct ac voltage levels.

Table 8J-27. *LNA Gain*

Service Function	Description	DVM Measurements at TP 14
[6] [1] [2] [2] [6] [9] [6] [5] [HZ]	AC AM LNA Gain ≈ 6.9	4.6 to 5.1 Vac
[6] [1] [2] [1] [8] [7] [0] [9] [HZ]	AC AM LNA Gain ≈ 1	.68 to .74 Vac

Test the Internal/External AM Switches

5. Setup:

   Key in: [INST PRESET].

   Key in: [AM] [ON] [MOD FREQ] [2] [kHZ] to set the Internal Modulation Oscillator to 2 kHz.

   Connect A2 TP15 to the Audio Analyzer "High" input.

   Set the Audio Analyzer to measure ac level.

   Ensure that the Audio Analyzer output is still connected to HP 8642 AM/PULSE input, and is set for 1 kHz and 1.4V.

6. Measure Frequencies and Amplitudes:

   Key in [SHIFT] [SPCL] [3] to enter Service Mode.

   Key in each Service Function from Table 8J-28 while verifying correct frequency and amplitude levels at A2 TP15 with the Audio Analyzer.

Table 8J-28. *AM Switches*

Service Function	Description	TP15 Results	
		FREQ	Amplitude
[6] [1] [2] [1] [7] [8] [7] [2] [HZ]	Internal AM	≈ 2 KHz	3.68 to 3.99 Vac
[6] [1] [2] [1] [7] [8] [8] [8] [HZ]	External AM	≈ 1 KHz	3.68 to 3.99 Vac
[6] [1] [2] [1] [7] [8] [5] [6] [HZ]	No AM Selected	N/A	0 to .5 Vac

Test the AM Level Adjust DAC

7. Setup:

   Key in: [INST PRESET].

   Key in: [AM] [ON] [INT] to select Internal AM.

   Connect the DVM to A2 TP16.

   Set the DVM to measure VAC.

   Ensure that the Audio Analyzer is still connected to the HP 8642 AM/Pulse input, and is set for 1 kHz at 1.4V.

8. Measure Voltages:

   Key in [SHIFT] [SPCL] [3] to enter Service Mode.

   Key in each Service Function from Table 8J-29 while verifying correct output levels at A2 TP16.

NOTE

For the first Service Function /DAC setting, verify that the voltage measurement V1 is between the upper and lower limits given. For the rest of the settings, calculate the upper and lower limits by multiplying V1 times the factors given in the table.

Table 8J-29. *A2 AM Level DAC Voltages*

Service Function	DAC Setting	Lower Limit	Voltage At TP16	Upper Limit
[6][1][2][8][1][9][1][HZ]	4095	3.68 Vac	V1 _____ Vac	3.99 Vac
[6][1][2][6][1][4][4][HZ]	2048	V1 × .5	V2 _____ Vac	V1 × .501
[6][1][2][5][1][2][0][HZ]	1024	V1 × .2498	V3 _____ Vac	V1 × .2507
[6][1][2][4][6][0][8][HZ]	512	V1 × .1246	V4 _____ Vac	V1 × .1256
[6][1][2][4][3][5][2][HZ]	256	V1 × .06215	V5 _____ Vac	V1 × .06290
[6][1][2][4][2][2][4][HZ]	128	V1 × .03100	V6 _____ Vac	V1 × .03152
[6][1][2][4][1][6][0][HZ]	64	V1 × .01535	V7 _____ Vac	V1 × .01590
[6][1][2][4][1][2][8][HZ]	32	V1 × .007680	V8 _____ Vac	V1 × .007950
[6][1][2][4][1][1][2][HZ]	16	V1 × .003770	V9 _____ Vac	V1 × .004045
[6][1][2][4][1][0][4][HZ]	8	V1 × .001820	V10 _____ Vac	V1 × .002090
[6][1][2][4][1][0][0][HZ]	4	V1 × .0008547	V11 _____ Vac	V1 × .001109
[6][1][2][4][0][9][8][HZ]	2	V1 × .0003663	V12 _____ Vac	V1 × .0006105
[6][1][2][4][0][9][7][HZ]	1	V1 × .0001221	V13 _____ Vac	V1 × .0003663
[6][1][2][4][0][9][6][HZ]	0	−.001 Vac	V14 _____ Vac	.001 Vac

Test the Normal/Doubled Outputs

9. Setup:

   Switch the HP 8642 to Standby.

   Disconnect W33 (the AM Out Doubled line) at A2 J4 (FX) .

   Disconnect W22 (the AM Out Normal line) at A2 J3.

   Connect external cables to A2 J3 and J4 (to be connected to the DVM).

   Switch the HP 8642 on.

   Key in: [AM] [ON] [INT] to select Internal AM.

   Key in: [SHIFT] [SPCL] [3] [6] [1] [2] [8] [1] [9] [1] [Hz] to set the AM level DAC to 4095.

10. Measure Voltages:

    Key in [SHIFT] [SPCL] [3] to enter Service Mode

    Key in each Service Function in Table 8J-30 while verifying the output levels at A2J3 and A2J4 with the DVM connected to the external cables.

Table 8J-30. *Normal/Doubled Outputs*

Service Function	Description	Results	
		A2 J3	A2 J4
61226965 Hz	AM Out Normal (FY)	3.68 to 3.99 Vac	0 to 0.025 Vac
61225941 Hz	AM Out Doubled (FY)	0 tp 0.025 Vac	3.68 to 3.99 Vac

   Switch the HP 8642 to Standby.

   Reconnect W33 to A2J4.

   Reconnect W22 to A2J3.

Test the HI/LO Detector

11. Setup:

    Switch the HP 8642 on.

    Set the Audio Analyzer output to 1 kHz and 1.27V (0.9 Vpk), 600Ω output impedance.

    Connect the Audio Analyzer output to the AM/PULSE input (J1 on the front panel).

    Key in: [AM] [ON] [EXT AC] to select External AC AM.

12. Measure Voltages:

    For each Audio Analyzer setting in Table 8J-31, use the Oscilloscope to verify correct TTL levels at the Test Points given.

NOTE

A "0" in the following table represents a TTL low signal (0.0 to +0.8 Vdc).
A "1" represents a TTL high (2.3 to +5.0 Vdc).

Table 8J–31.

8903 Setting	TP21 (MOD LO)	TP20 MOD HI	TP19 EXT CNT	Front Panel Mod HI/LO
1 kHz @ 1.27V (0.9 Vpk)	1	1	1	LO
1 kHz @ 1.4V (1 Vpk)	0	1	1 kHz TTL	None
1 kHz @ 1.55 (1.1 Vpk)	0	0	1 kHz TTL	HI

Test the General Diagnostics Interface

13. Setup:

    Key in: [INST PRESET].

    Key in: [AM] [ON] [EXT AC] to select External AC AM.

    Key in: [SHIFT] [SPCL] [3] [6] [1] [2] [8] [1] [9] [1] [Hz] to set the AM level DAC to 4095.

    Set the Audio Analyzer to 1 kHz, 1.27V (0.9 Vpk), and 600Ω output impedance.

    Connect the Oscilloscope to the Mod Diag Bus line at A2 TP22 (FZ) .

    Connect the Audio Analyzer Output to the AM/PULSE Input (J1 on the HP 8642 front panel).

14. Verify Signals:

    Key in: [SHIFT] [SPCL] [325] [Hz] to enable internal Voltmeter measurements.

    Key in each Function from Table 8J-32, while verifying correct signals at A2 TP22.

NOTE

Only three lines are checked at this point. If the multiplexer in the General Diagnostics Interface is suspected bad, see the Component Level Repair Directory (SS16) to test of the rest of the lines.

Table 8J–32. *General Diagnostics Interface*

Function	MUX Line	Signal At TP22
[5] [0] [HZ]	Lo DET Sense Point	+5 Vdc
[5] [3] [HZ]	AM Output Sense Point	1 KHz ≈ 5 Vpk
[5] [6] [HZ]	AM/FM LNA Sense Point	1 KHz ≈ 6 Vpk

Restore Module

15. Disconnect the Audio Analyzer from the AM/PULSE input.
16. Disconnect all test equipment from the A2 module.
17. Reconnect all HP 8642 internal cabling.

COMPONENT LEVEL REPAIR DIRECTORY

The following tables contain information to aid in component level repairs. These tables are designed to be used after the module troubleshooting procedures have verified a failure in circuitry represented on one of the module service sheet schematics. In general the tables supply one of the following types of information:

* Special function codes relevant to the module.

* Transistor emitter, base and collector voltages.

* Frequency and power levels at different circuit points.

* Module control line and power supply interconnections in the module and instrument.

SERVICE SHEET 15

Table 8J–33. SS15 DC Voltages

Location	Voltage
TP 8	−.1 to .1 Vdc
TP 10	.1 to −.1 Vdc
TP 11	−15 TO +15 Vdc
TP 12	−.1 to .1 Vdc
U 38 Pin 2	6.4 to 7.2 Vdc

Table 8J–34. SS15 OSC Ranges

Oscillator FREQ Range	OSC FET Bits A B C D	Settling Time	Nominal Range
10.0 to 63.1 Hz	0 1 1 1	51 mS	7.5 – 87.4 Hz
63.2 to 398 Hz	1 0 1 1	9.1 mS	399 – 484 Hz
399 to 2.51 kHz	1 1 0 1	15 mS	2.58 – 3.16 kHz
2.52 to 15.8 kHz	1 1 1 0	220 μS	16.7 – 20.4 kHz
15.9 kHz to 100 kHz	1 1 1 1	220 μS	105 – 129 kHz

SERVICE SHEET 16

Table 8J–35. SS16 Voltages

Input		Output	
Location	Voltage	Location	Voltage
U3 Pin 2	−.1 to .1 Vdc	TP 15	−.1 to .1 Vdc
U6 Pin 2	−.1 to .1 Vdc	TP 16	−.1 to .1 Vdc
U13 Pin 3	−.1 to .1 Vdc	TP 14	−.1 to .1 Vdc
U30 Pin 3	−.1 to .1 Vdc	TP 17	−.1 to .1 Vdc
U29 Pin 12	6.97 to 7.10 Vdc		
U29 Pin 14	6.69 to 6.83 Vdc		

Table 8J–36. SS16 HI/LO Detector Lines

MOD HI	MOD LO	Indication
0	0	Signal > 1 Vpk
1	0	Signal = 1 Vpk
1	1	Signal < 1 Vpk

*Table 8J–37. SS16 Stage Gains**

Stage	Input	Output	Gain
AM Low Noise AMP (7)	1 Vpk	6.9 Vpk	6.9
AM Low Noise AMP (1)	1 Vpk	1 Vpk	1
AM Summing AMP	6.9 Vpk	5.4 Vpk	.7853

* Input and Output voltages are given under normal operating conditions.

Table 8J–38. *SS16 Diagnostic Select Lines*

Enter Service Mode	Select Code	MOD Board Select Lines *
	6 1 2 2 0 4 8 5 HZ	0 MOD LO Detector Sense Point
	6 1 2 2 0 5 1 7 HZ	FM Out Sense Point
SHIFT	6 1 2 2 0 5 0 1 HZ	MOD Out Sense Point
SPCL	6 1 2 2 0 5 3 3 HZ	AM Out Sense Point
3	6 1 2 2 0 4 9 3 HZ	ALC Error Voltage Sense Point
	6 1 2 2 0 5 2 5 HZ	Internal/External count Select Sense Point
	6 1 2 2 0 5 0 9 HZ	Audio OSC 2nd Intg. Sense Point
	6 1 2 2 0 5 4 1 HZ	AM/FM LNA Output Sense Point

* Measure lines at A2 TP22 (SS16).

SERVICE SHEET 17

Table 8J–39. *SS17 Voltages*

Input		Output	
Location	**Voltage**	**Location**	**Voltage**
U12 Pin 3	−.1 to .1 Vdc	TP 26	−.1 to .1 Vdc
U17 Pin 3	−.1 to .1 Vdc	TP 29	−.1 to .1 Vdc
U19 Pin 2	−.1 to .1 Vdc	TP 24	−.1 to .1 Vdc
U21 Pin 2	−.1 to .1 Vdc	TP 25	−.1 to .1 Vdc
U25 Pin 3	−.1 to .1 Vdc		
		TP 27	−.1 to .1 Vdc

Table 8J–40. *SS17 Stage Gains**

Stage	Input	Output	Gain
FM Low Noise Amp	1 Vpk	6.9 Vpk	6.9
FM ± Unity Gain Amp	6.9 Vpk	6.9 Vpk	1
FM Summing Amp	6.9 Vpk	5.4 Vpk	.7853
FM Output Drive	0 to 5.5 Vpk	0 to 5.5 Vpk	1

* Input and Output voltages are given under normal operating conditions.

SERVICE SHEET 18

Table 8J–41. *SS18 DAC Special Functions*

Enter Service Mode	Function	Description
	6 1 1 0 DATA HZ	Displays the current AM DAC SETTING 0-4095
	6 1 1 1 DATA HZ	Displays the current AM DAC setting 0-1095
	6 1 1 2 DATA HZ	Displays the current MOD out DAC setting 0-1023
	6 1 1 3 DATA HZ	Displays the current OSC FREQ DAC setting 1-1023
	6 1 1 4 DATA HZ	Displays the FET switch control settings see table 30
	6 1 1 5 DATA HZ	Displays the HI/LO and diagnostic settings see table 31
	6 1 1 6 DATA HZ	Displays the relay settings (attenuators etc. see table 32
SHIFT	6 1 2 0 DATA HZ	Input Data to the FM DAC. Data = 0 to 1023
SPCL	6 1 2 1 DATA HZ	Input Data to the AM DAC. Data = (0 to 4095) +4096
3	6 1 2 2 DATA HZ	Input Data to the MOD out DAC.Data = (0 to 1023)+8192
	6 1 2 3 DATA HZ	Input Data to the OSC FREQ DAC. Data = (0 to 1023)+16384
	6 1 2 4 DATA HZ	Input data to the FET switches. Data + 16384 see table 30
	6 1 2 5 DATA HZ	Inputs data to the HI/LO Diagnostics. Data + 20480 see table 31
	6 1 2 6 DATA HZ	Inputs data to the relay controls. Data + 24576 see table 32
	6 1 2 2 2 8 6 7 HZ	Sets MOD board for internal audio count mode.
	6 1 2 2 8 6 7 3 HZ	Sets mod board for external audio count mode.
	6 1 2 2 8 6 7 4 HZ	Sets mod board for the oscillator DC function.

1 Display Service Functions return the decimal number set in the specified Data i.e. 6110 Hz may return 0-1023, depending on the amount of fm deviation set.

2 The DATA required is explained in the "Description" column. i.e. 6120 1023 Hz sets the FM DAC to 1023.

Table 8J–42. *SS18 FET Switch Settings*

Decimal Value	Bit	Bit Set	Ref Designation
2048	11	Not Used (MSB)	
1024	10	OSC FET Bit 3	U41 pin 15
512	9	OSC FET Bit 2	U41 pin 16
256	8	OSC FET Bit 1	U41 pin 5
128	7	OSC FET Bit 0	U41 pin 19
64	6	AM LNA Gain (1 = AV of 7, 0 = AV of 1)	U22 pin 5
32	5	EXT AM	U8 pin 9
16	4	INT AM	U8 pin 6
	3	INT FM	U16 pin 12
4	2	EXT FM	U16 pin 15
2	1	EXT FM W/PRE	U16 pin 19
1	0	FM INV/HI (LSB)	U16 pin 16

SHIFT SPCL 3 6 1 1 4 Hz Displays the current value of the FET switch settings. The display is a decimal number between 0 and 4095, which is the sum of the Decimal Values for each Bit Set. The decimal number must be converted to binary to determine which bits are set. SHIFT SPCL 3 6 1 2 4 DATA Hz sets the Bits specified by the DATA. The data is 1 decimal number which is the sum of all Decimal Values for each bit desired to be set, plus 16384, i.e. to set OSC FET Bit 1, key in SHIFT SPCL 3 6 1 2 4 16640 Hz. Data = (Sum of Decimal Values) + 16384.

Table 8J–43. *SS18 HI/LO & Diagnostic Bits*

Decimal Value	Bit. no.	Bit Set	Ref. Designator
32	5 (MSB)	MUX 0	U22 Pin 15
16	4	MUX 1	U22 Pin 12
8	3	MUX 2	U22 Pin 9
4	2	Self Test	U22 Pin 6
2	1	HI/LO Reset	U8 Pin 2
1	0 (LSB)	HI/LO AM/FM	U8 Pin 5

SHIFT SPCL 3 6 1 1 5 Hz Displays the current value of the HI/LO & Diagnostic Bits settings. The display is a decimal number between 0 and 4095, which is the sum of the Decimal Values, for each Bit Set. The decimal number must be converted to binary to determine which bits are set. SHIFT SPCL 3 6 1 2 5 DATA Hz sets the Bits specified by the DATA. The data is 1 decimal number which is the sum of all Decimal Values for each bit desired to be set, plus 16384, i.e. to set OSC FET Bit 1, key in SHIFT SPCL 3 6 1 2 5 20496 Hz. Data = (Sum of Decimal Values) + 20480.

Table 8J-44. *SS18 Relay Bits*

Decimal Value	Bit. no.	Bit Set	Ref. Designator
2048	11 (MSB)	Normal AM	U16 Pin 2
1024	10	Doubled AM	U16 Pin 5
512	9	AM DC	U41 Pin 2
256	8	AM AC	U41 Pin 6
128	7	FM DC	U16 Pin 6
64	6	FM AC	U16 Pin 9
32	5	9dB out	U23 Pin 15
16	4	9dB In	U23 Pin 9
8	3	18dB Out	U23 Pin 5
4	2	18dB In	U23 Pin 2
2	1*	36dB Out	U23 Pin 6
1	0 (LSB)	36dB In	U23 Pin 12

* 1 is the active state bits must be set in pairs.

[SHIFT] [SPCL] [3] [6] [1] [1] [6] [Hz] Displays the current value of the Relay Bits settings. The display is a decimal number between 0 and 4095, which is the sum of the Decimal Values, for each Bit Set. The decimal number must be converted to binary to determine which bits are set. [SHIFT] [SPCL] [3] [6] [1] [2] [6] [DATA] [Hz] sets the Bits specified by the [DATA]. The data is a decimal number which is the sum of all Decimal Values for each bit desired to be set, plus 24576, i.e. to set Normal AM, key in [SHIFT] [SPCL] [3] [6] [1] [2] [6] [26624] [Hz]. Data = (Sum of Decimal Values) + 24576.

GENERAL

Table 8J-45. *Power Supply Lines Interconnections*

Supply	A17	A5 In	A5 Out	A2 MOD
+15 Vdc	J2 9-18	J12 9-18	J11 / 19 and 20	J1 / 19 and 20
+5 Vdc	J2 35-50	J12 35-50	J11 / 16	J1 / 16
−5 Vdc	J2 23-26	J12 23-26	J11 / 18	J1 / 18
−15 Vdc	J2 19-22	J12 19-22	J11 / 15	J11 / 15
6ND		GND	J11 / 19 and 14	J1 / 9 and 14
+15V Sense		J12 / 7	J11 / 17	J1 / 17

Table 8J–46. *Setting Control Lines*

Key SEQ	Function	Select Function		Select Line	
		Key SEQ	Function	Key SEQ	Line Label
				4 8 HZ	MOD Data Bit 0
				4 9 HZ	MOD Data Bit 1
				5 0 HZ	MOD Data Bit 2
SHIFT	Enables	6 0 0	Reads Line State	5 1 HZ	MOD Data Bit 3
SPCL	Service	6 0 1	Sets Line To 1	5 2 HZ	MOD Data Bit 4
3	Mode	6 0 2	Sets Line To 0	5 3 HZ	MOD Data Bit 5
		6 1 5	Continuous Toggle	5 4 HZ	MOD Data Bit 6
				5 5 HZ	MOD Data Bit 7
				6 0 HZ	MOD Clock
				1 1 6 HZ	HI/LO INT.
				1 2 2 HZ	MOD HI
				1 2 3 HZ	MOD LO(Diag Buss)

Table 8J–47. *Control Line Interconnections*

Line Label	A2 Input	A5 Output	A5 Input	A4 Output	A4 Latch
DB 0	J1 / 1	J11 / 1	J15 / 9	J3 / 9	U17 / 2
DB 1	J1 / 2	J11 / 2	J15 / 15	J3 / 15	U17 / 5
DB 2	J1 / 3	J11 / 3	J15 / 17	J3 / 17	U17 / 6
DB 3	J1 / 4	J11 / 4	J15 / 23	J3 / 23	U17 / 9
DB 4	J1 / 5	J11 / 5	J15 / 22	J3 / 22	U17 / 12
DB 5	J1 / 6	J11 / 6	J15 / 18	J3 / 18	U17 / 15
DB 6	J1 / 7	J11 / 7	J15 / 14	J3 / 14	U17 / 16
DB 7	J1 / 8	J11 / 8	J15 / 10	J3 / 10	U17 / 19
MOD CLK	J1 / 11	J11 / 11	J15 / 26	J3 / 26	U18 / 2
HI/LO INT	J1 / 12	J11 / 12	J15 / 40	P3 / 40	U33 / 7
MOD HI	J1 / 10	J11 / 10	J15 / 43	P3 / 43	U31 / 3
DIAG BUS	J1 / 13	J11 / 13	J16 / 13	P2 / 13	U31 / 4

Adjustments

DESCRIPTION OF A2 ADJUSTMENTS

Overall Equipment List

Digital Voltmeter HP3456A
Audio Analyzer ..... HP 8903B
HPIB Printer ..... HP 2225A

NOTE

Each adjustment procedure assumes the HP 8642 internal cabling is connected normally and all circuitry is functioning properly.

The Adjustment Procedure for the A2 corrects for major tolerance errors in the modulation oscillator that would cause the HP 8642's mod frequency tuning algorithm to fail. The adjustment involves setting two variable resistors to their extreme limits and making a frequency and level measurement. Based on these measurements the correct settings are computed then the adjustment is made.

ADJUSTMENT 1: A2 MODULE

Procedure

1. Setup:

   Key in: [INST PRESET] and wait for the Preset Routine to finish.

   Key in: [SHIFT] [MOD OUT] [ON] .

   Set the Mod Oscillator DAC to 1023 by keying in the following:
   [SHIFT] [SPCL] [3] [6] [1] [2] [1] [3] [3] [1] [1] [Hz]

   Turn A2 R8 maximum CW and A2 R27 maximum CCW, (SS14).

   Connect the DVM to TP1. Set it to measure AC volts.

   Connect the Audio Analyzer input to TP2.

2. Adjustment:

   Measure and record the AC voltage ($v1$) (using the DVM) at TP1 .

   Move the DVM input to TP2.

   Measure and record the AC voltage ($v2$) (using the DVM) and the frequency ($f2$) (using the Audio Analyzer) at TP2.

   $$v1 = \_\_\_\_\_ \text{Volts}$$

   $$v2 = \_\_\_\_\_ \text{Volts}$$

   $$f2 = \_\_\_\_\_ \text{Hz}$$

   Compute the Frequency Adjustment limits ($f8$) of A2 R8 by:

   $$f8\textbf{Min} = \left(\sqrt{\frac{v2 \times f2 \times 2872}{v1}}\right) - 1 = \_\_\_\_\_ \text{Hz}$$

   $$f8\textbf{Max} = f8Min + 2 = \_\_\_\_\_ \text{Hz}$$

   Adjust A2 R8 for a frequency between $f8$**Max** and $f8$**Min** at TP2.

   Adjust A2 R27 for a frequency of 2847 to 2897 Hz at A2 TP2.

3. If you were sent to this procedure from Check 2 step 12, return to Check 2 step 13.

A2 AUTO-ADJUSTMENTS

NOTE

Read Section 5 before proceeding with this Auto-Adjust Routine.

Required Equipment:

DVM HP3456A
HP-IB Printer HP2225A

1. Initialize Auto Adjust Routine:

   Connect the Required Equipment to the HP 8642 via HP-IB. Ensure all equipment is turned on and that the printer address is set to 01.

   Key in: [INST PRESET]

   Key in: [SHIFT] [SPCL] [3] [8] [8] [Hz] [8] [0] [Hz].

   Key in: [9] [Hz] when **"ENTER ROUTINE NUMBER .G8000"** appears.

   Key in the the Day, Month, Year and Module Cal ID Number when prompted by the HP 8642 display. (See Section 5 for details.)

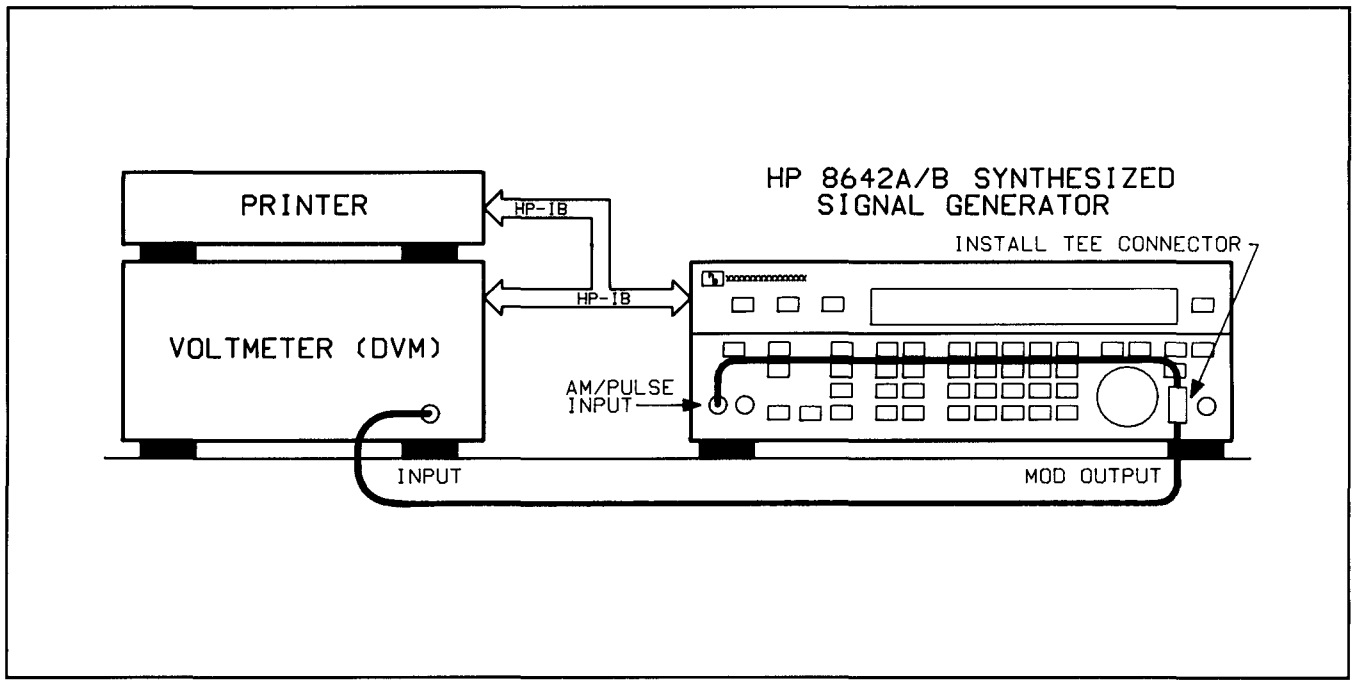


Figure 8J–1. *Set-Up 1*

2. When **"WAITING FOR SET-UP 1 .V24"** appears:

   Connect a BNC Tee connector to the MOD OUTPUT port on the HP 8642.

   Connect a BNC cable from the TEE connector to the DVM Measurement Input.

   Connect a BNC cable from the TEE connector to the AM/PULSE input port on the HP 8642.

   Set the DVM to measure Volts AC.

   Key in: [Hz] to continue. (Run time $\leq$ 1 minute)

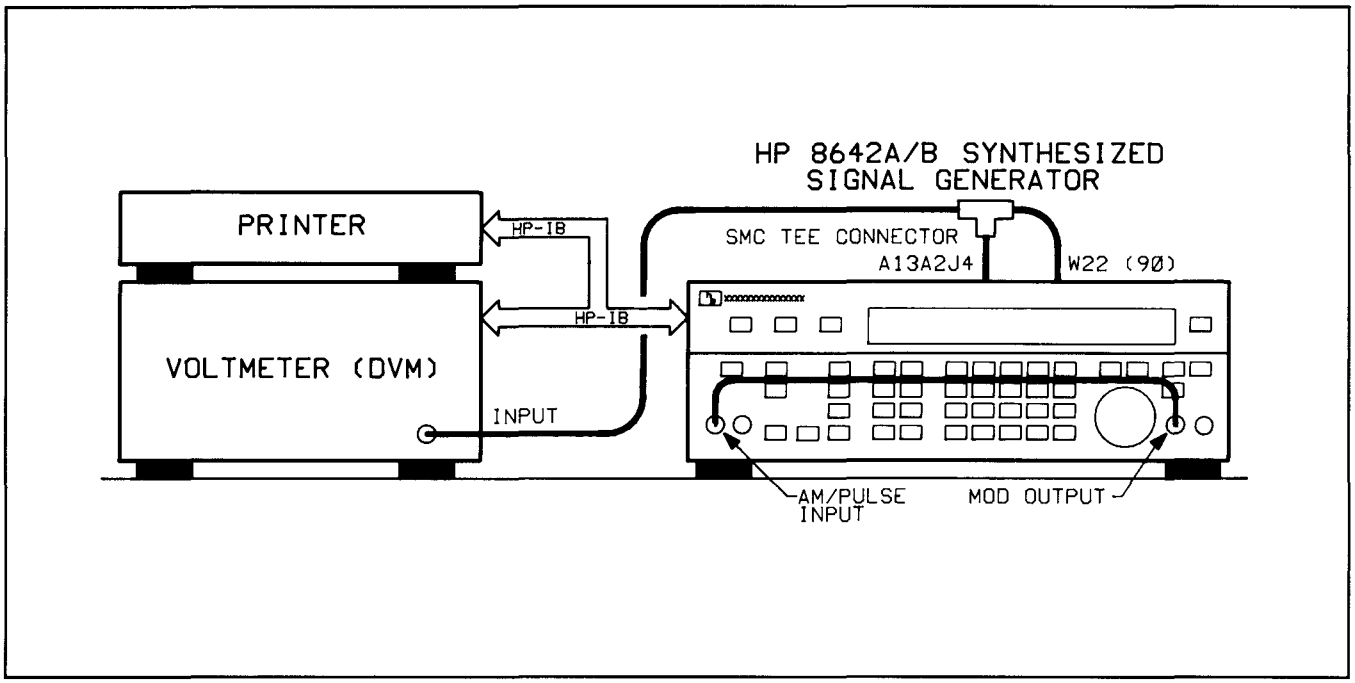


Figure 8J–2. *Set-Up 2*

3. When **"WAITING FOR SET-UP 2 .V25"** appears:

   Disconnect the BNC TEE connector from the MOD OUTPUT port and connect a cable from the AM/PULSE input port to the MOD OUTPUT port.

   Disconnect cable W22 from the A13 Module at A13A2 J4 (90).

   Connect an SMC TEE connector to the A13 Module at A13A2 J4.

   Connect the DVM cable with adapter to the TEE connector.

   Connect cable W22 (90) to the Tee connector.

   Set the DVM to measure Volts AC.

   Key in: [Hz] to continue. (Run time $\leq$ 1 minute)

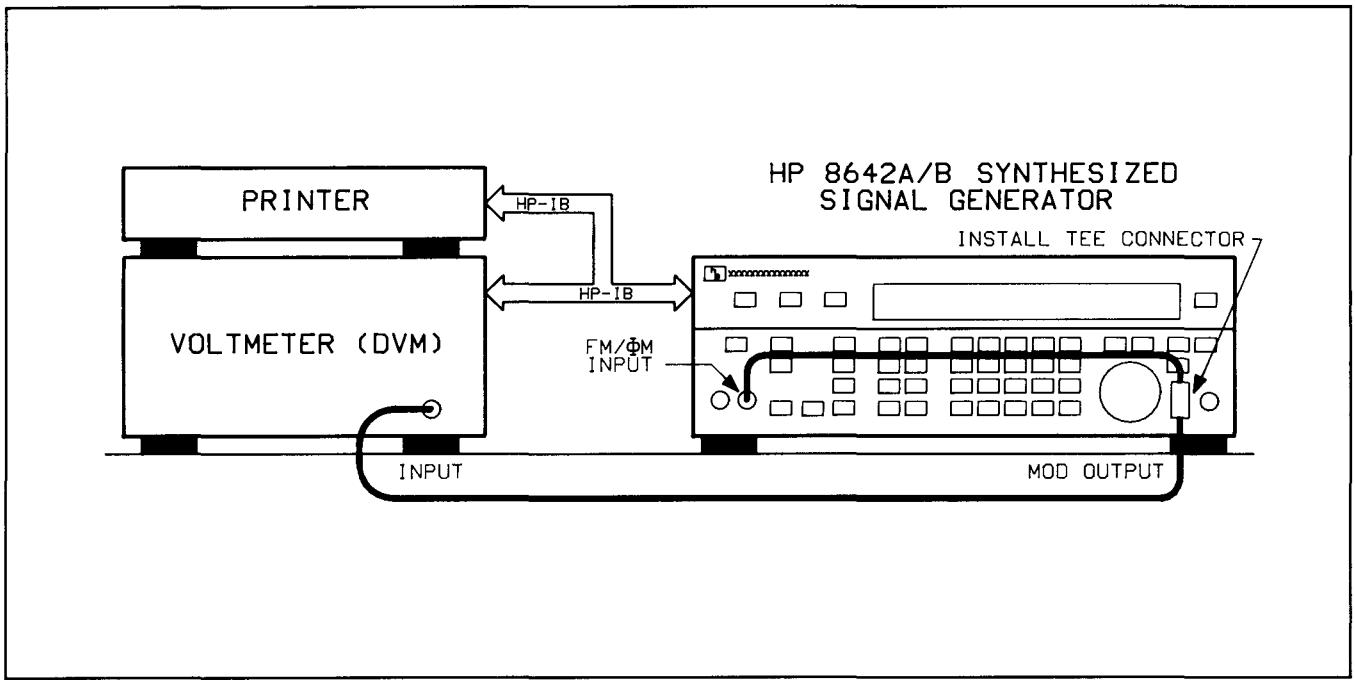


Figure 8J-3. *Set-Up 3*

4. When**"WAITING FOR SET-UP 3 .V26"** appears:

   Disconnect the DVM cable and W22 from the TEE connector and remove the TEE connector from A13A2 J4.

   Reconnect W22 to A13A2 J4.

   Connect a BNC TEE connector to the MOD OUTPUT port.

   Connect a BNC cable from the FM/ΦM to the TEE connector as shown.

   Connect a BNC cable from the DVM input to the TEE connector.

   Set the DVM to measure Volts AC.

   Key in: [Hz] to continue. (Run time ≤ 1 minute)

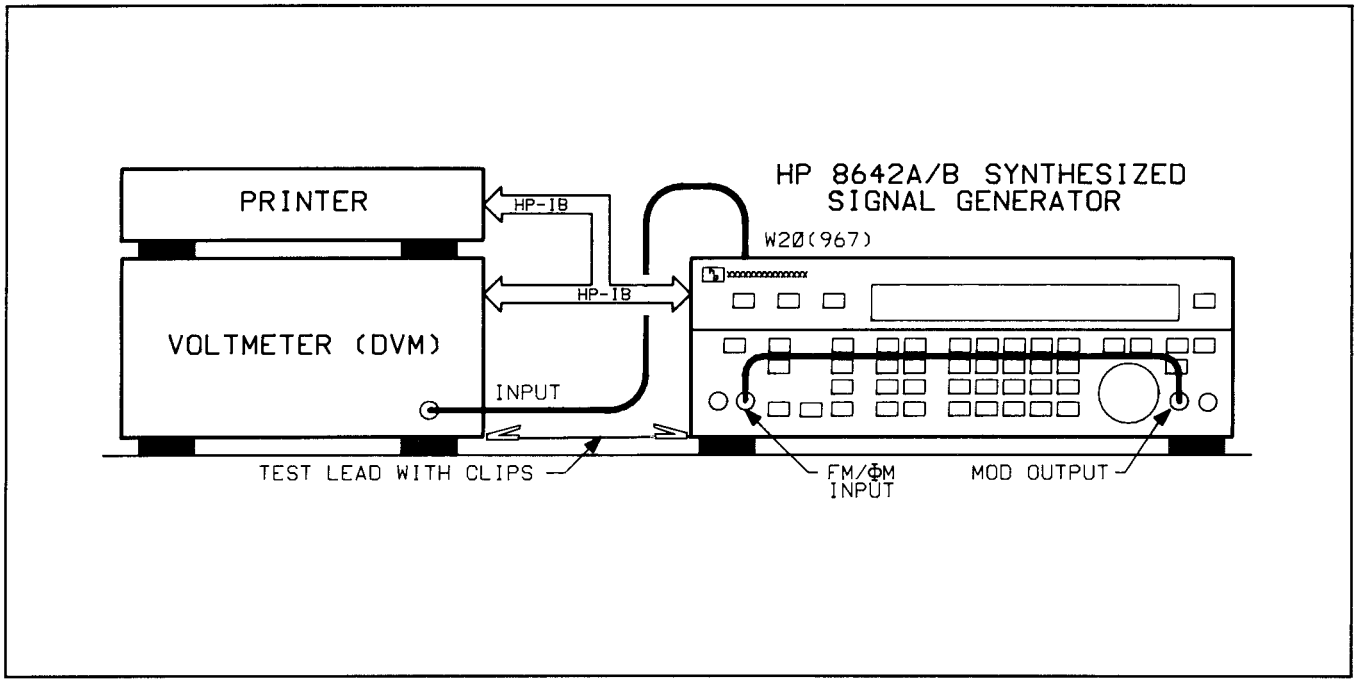


Figure 8J–4. *Set-Up 4*

5. When **"WAITING FOR SET-UP 4 .V27"** appears:

   Disconnect the BNC TEE from the MOD OUTPUT port and connect a cable from the FM/ΦM input port to the MOD OUTPUT port.

   Disconnect cable W20 from the A6 Module at A6A1 J4 (967).

   Connect cable W20 to the DVM cable.

   Set the DVM to measure Volts AC.

   Connect a test lead from the DVM chassis to the HP 8642 chassis.

   Key in: [Hz] to continue. (Run time ≤ 1 minute)

6. When **"UNPROTECT CAL. MEMORY .G8005"** appears:

   Switch A3 S2 toward the rear of the instrument to unprotect the EEPROM's.

   Press [Hz] to Continue.

7. When **"PROTECT CAL. MEMORY .G8006"** appears:

   Switch A3 S2 toward the front of the instrument to protect the EEPROM's.

   Press [Hz] to Continue.

8. When **"RECONNECT ALL CABLES .V29"** appears:

   Disconnect all test cables from the instrument.

   Reconnect any instrument cables which are still disconnected.

   Press [Hz] to Continue.

9. Run the instrument level diagnostics to verify operation:

   Key in: [SHIFT] [SPCL] [3] [3] [0] [Hz].

   When **"WAITING FOR SETUP 1 .Z24"** appears, connect the MOD OUT to the AM/PULSE INPUT and FM/ΦM INPUT.

   Press [Hz] to Continue.

10. When **"DIAG DONE .V1"** appears:

    Press the MSSG key to view the message buffer. If **"NO MESSAGES .00"** is contained in the message buffer, the HP 8642 is functioning properly.

11. Up Load Cal Data:

    Now that the functionality of the HP 8642 has been verified, used the following procedure to up load the new cal data.

    Switch the HP 8642 to standby.

    Remove the A20 Cal Module. (See Disassembly Procedures).

    Plug the A20 Module on to A3 J3.

    Switch the HP 8642 on.

    Switch A20 S1 to the CHANGE position.

    Key in: [SHIFT] [SPCL] [3] [7] [2] [9] [Hz].

    When **"TRANSFER VERIFIED .U613"** appears on the display, move A20 S1 up to its PROTECTED position.

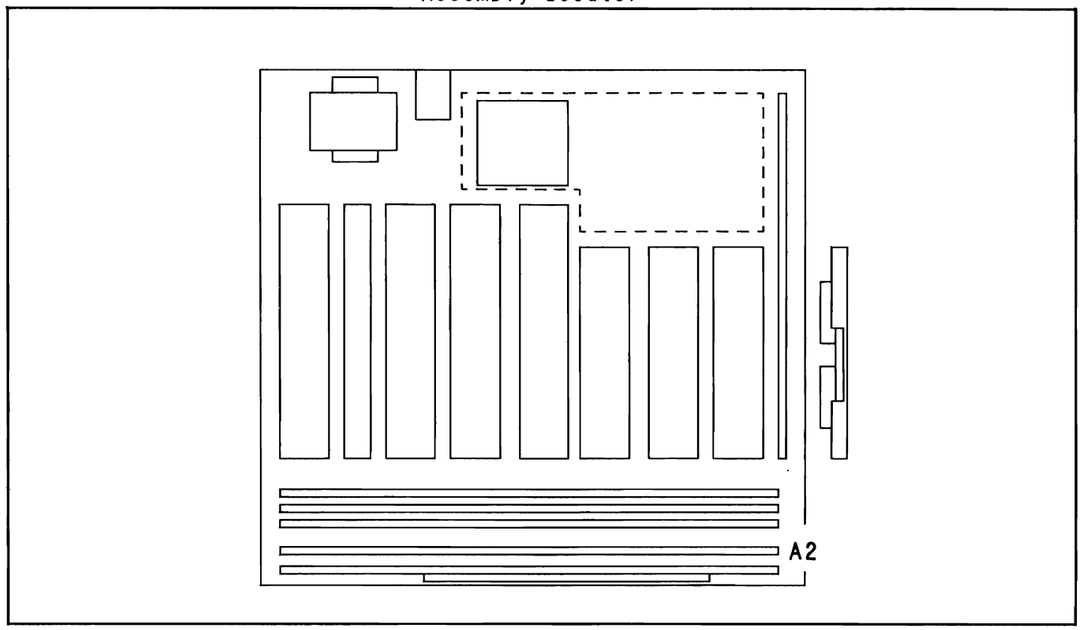
    Key in: [Hz] to end the routine.

    Switch the HP 8642 to Standby.

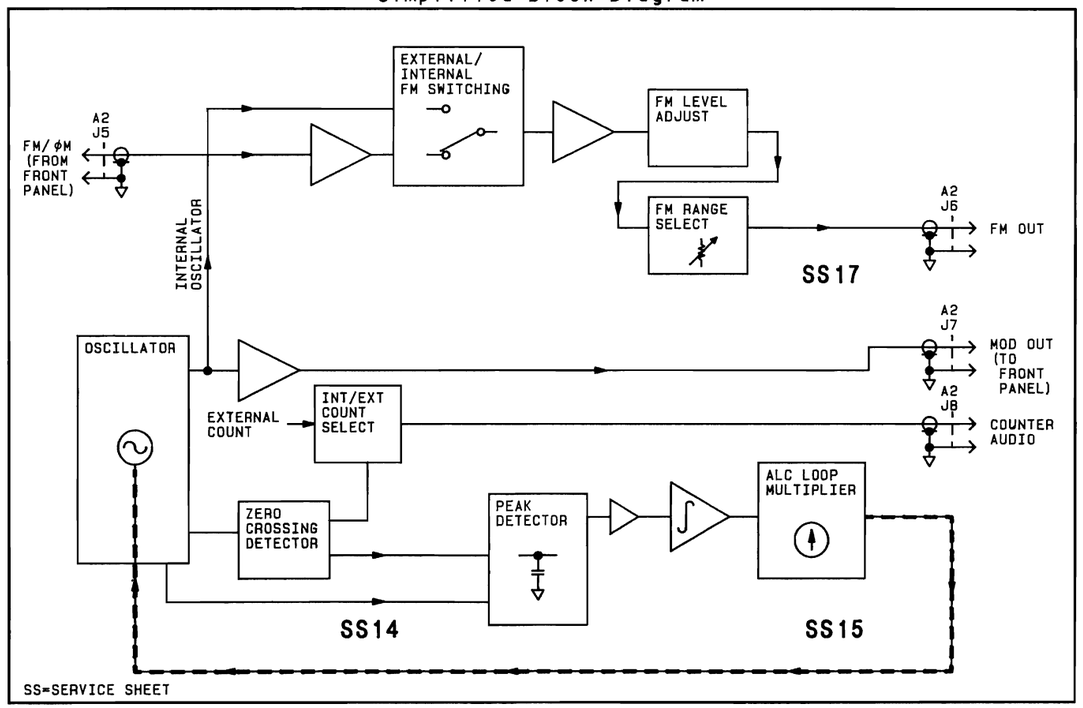
    Reconnect the A20 module to the rear panel (See Disassembly Procedures).

    Re-install the top cover.

Assembly Locator



Simplified Block Diagram



Module Test Point/Adjustment Locations

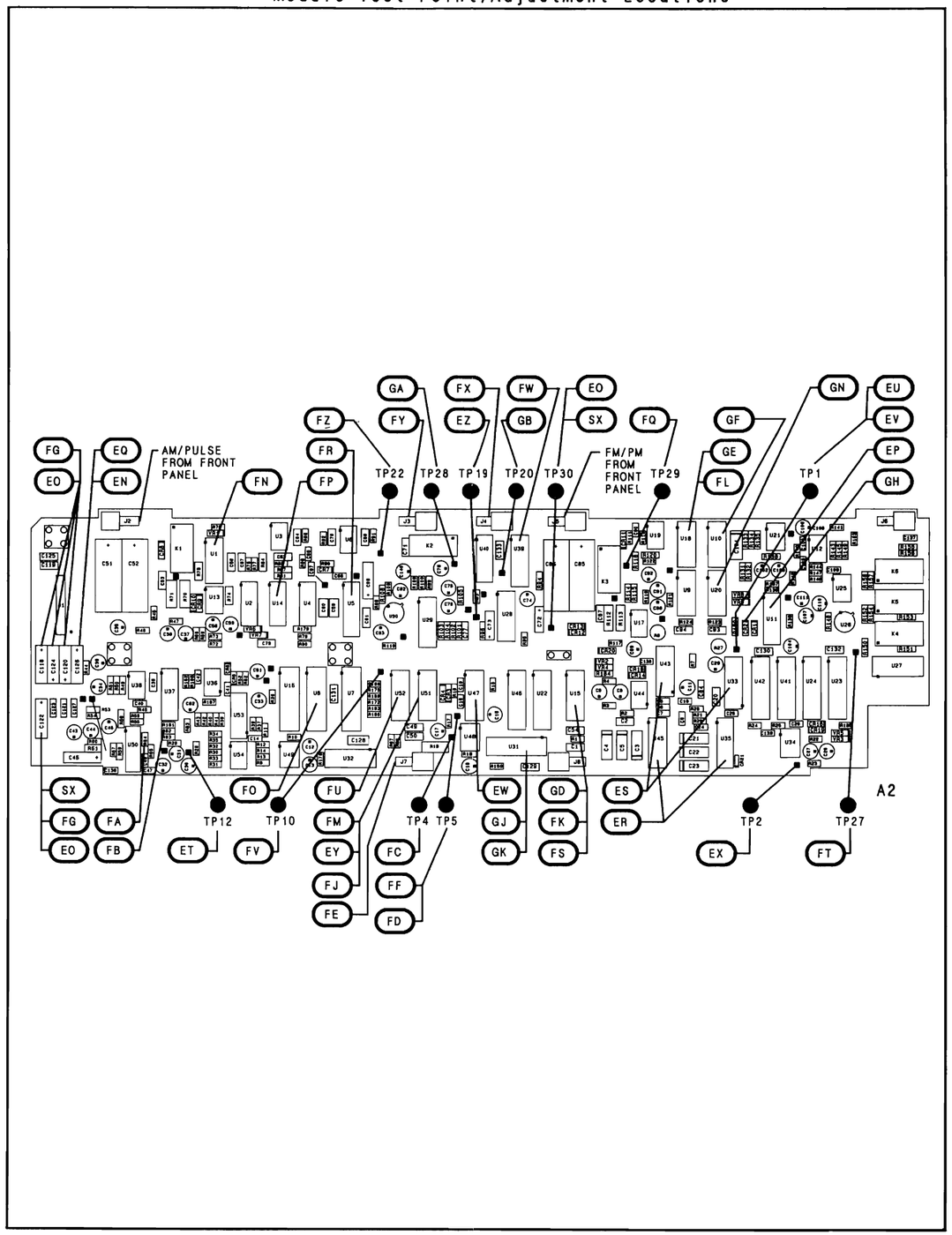


Figure 8J-100 BD5 General Information.

CHANGES

2514A and above

On the block diagram:

- In the upper left portion of the block diagram, change the A2 part number to 08642-60223.

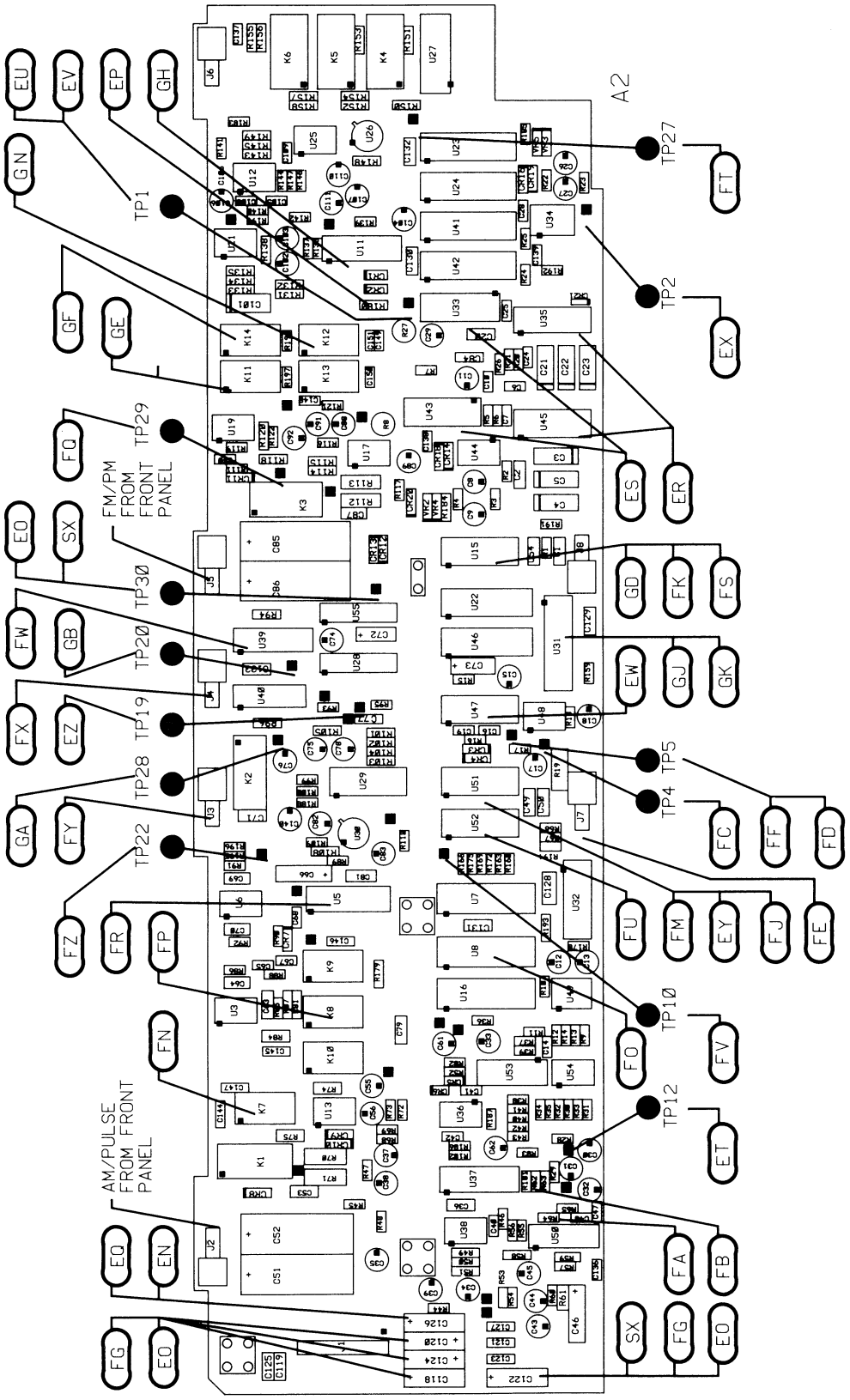
2714A and above

In General Information:

- Replace the *Module Test Point/Adjustment Locations* on page 8J-100 with the new *Module Test Point/Adjustment Locations* on page 8J-100.2.

On the block diagram:

- In the upper left portion of the block diagram, change the A2 part number to 08642-60323.



BD 5
8J-100.2

Module Test Point/Adjustment Locations (2714A and above).

OPTION 002

FM/ϕM (FROM REAR PANEL) J9 W201 98

FM/ϕM (FROM FRONT PANEL) J2 W19 98 J5

EU

OSCILLATOR

OSC FET BITS BD6 EA 4

OSC DAC BITS BD6 ES 10

+15V (REF)

OUTPUT AMPLIFIER

MOD OUT DAC BD6 EW 10

MUX 2 FC BD6

MOD OUT

EQ

CNT INT/EXT BD6 EY 2

EXT CNT BD6 EZ

INT/EXT COUNT SELECT

MUX 5 FD BD6

COUNTER AUDIO

ZERO CROSSING DETECTOR

MUX 6 EX BD6

SAMPLED VALUE TRANSFER

PEAK DETECTOR

FA

FB

POWER SUPPLY AND GND

+15V PROTECTED EP BD6

OSC DC BD6 OY

BIAS BD6 OZ

+15V (REF) EQ BD6

POWER SUPPLY AND GND SX BD6

POWER SUPPLY AND GND FG BD6

+15V SENSE POINT REF BD17 EN 17

POWER SUPPLY AND GROUND BD17 EQ 5 19, 20, 16, 15, 18, 14, 9

P/O J1 +15V +15V +5V -15V -5V GND

POWER SUPPLY AND GND 5

+15V PROTECTED

OSC DETECT

ALC LOOP MUTIPLIER

SS14

EV

EP

FG

ET

SERIAL PREFIX: 2427A

EU

FM INV HI
BD6 GE

AF
BD6 FL

INT/EXT FM
BD6 GN 2

INTERNAL
FM SWITCH

FM
SELF TEST
BD6 FM

FM AC/DC
BD6 GD 2

FM INPUT AC
DC COUPLER

FM LOW
NOISE
AMPLIFIER

FM ± UNITY
GAIN AMP

EXTERNAL FM
SWITCH

FM LNA
FQ BD6

EXT FM W/PRE
BD6 GF

ATT RELAY CON
BD6 GG

+15V
PROTECTED

POWER SUPPLY
AND GND
+15V, +5V
-15V, -5V, GND

MOD OUT DAC
BD6 EW 10

OUTPUT AMPLIFIER

MUX 2
FC BD6

MOD OUT

EQ

CNT
INT/EXT
BD6 EY 2

EXT CNT
BD6 EZ

INT/EXT COUNT
SELECT

MUX 5
FD BD6

COUNTER
AUDIO

ZERO
CROSSING
DETECTOR

MUX 6
EX BD6

SAMPLED
VALUE
TRANSFER

PEAK
DETECTOR

FA

FB

OSC
DETECT

SS14

5

EV

EP

FG

ET

SAMPLED VALUE
TRANSFER

SAMPLED
VALUE
TRANSFER

+15V (REF)

OSC DETECT

PEAK DETECTOR

PEAK DETECTOR

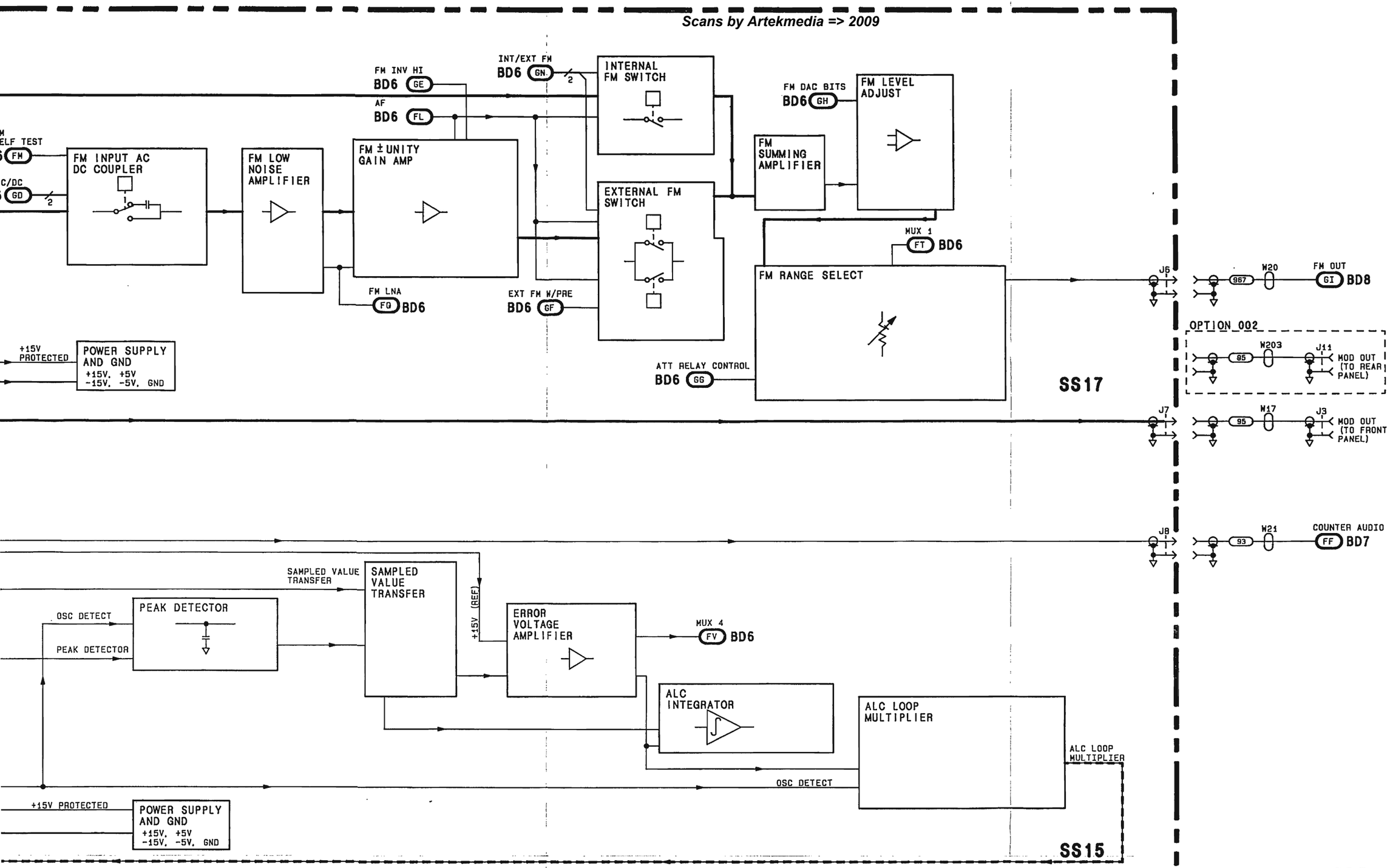
ERROR
VOLTAGE
AMPLIFIER

MUX 4
FV

ALC
INTEGRATO

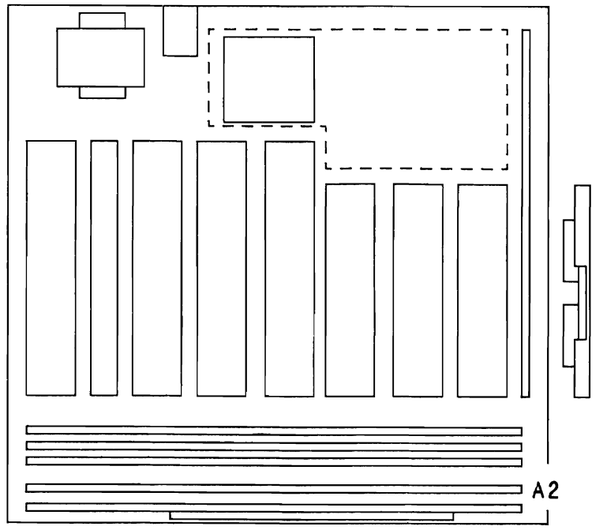
+15V PROTECTED

POWER SUPPLY
AND GND
+15V, +5V
-15V, -5V, GND

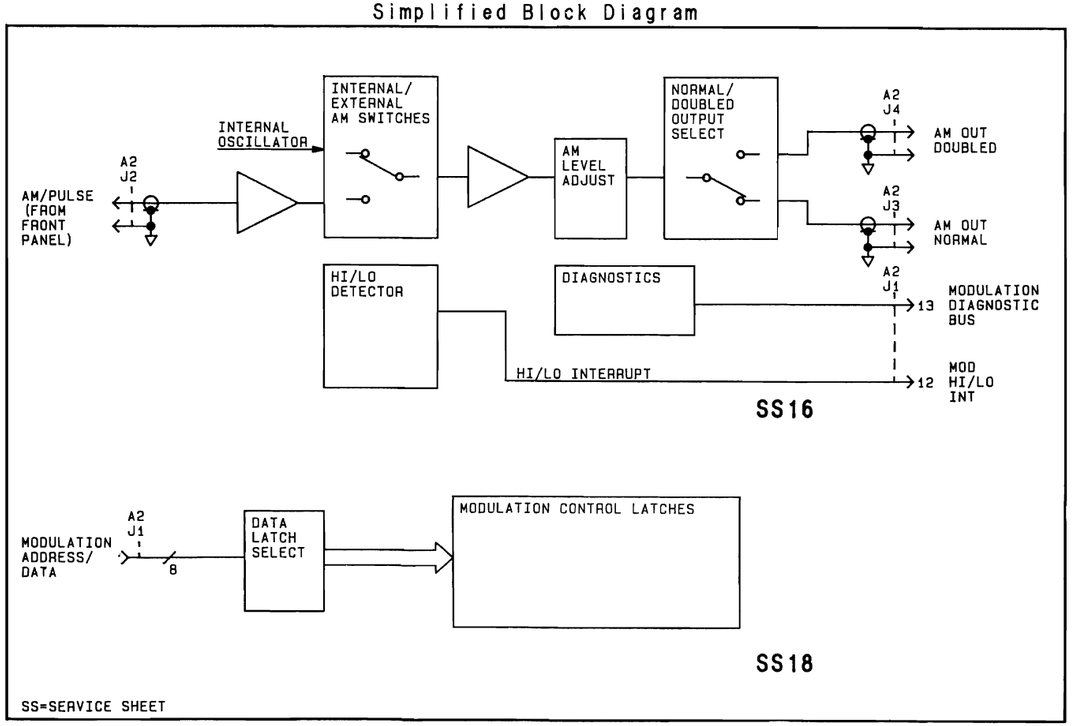


BD5
Figure 8J-101
8J-101

Assembly Locator



Simplified Block Diagram



Module Test Point/Adjustment Locations

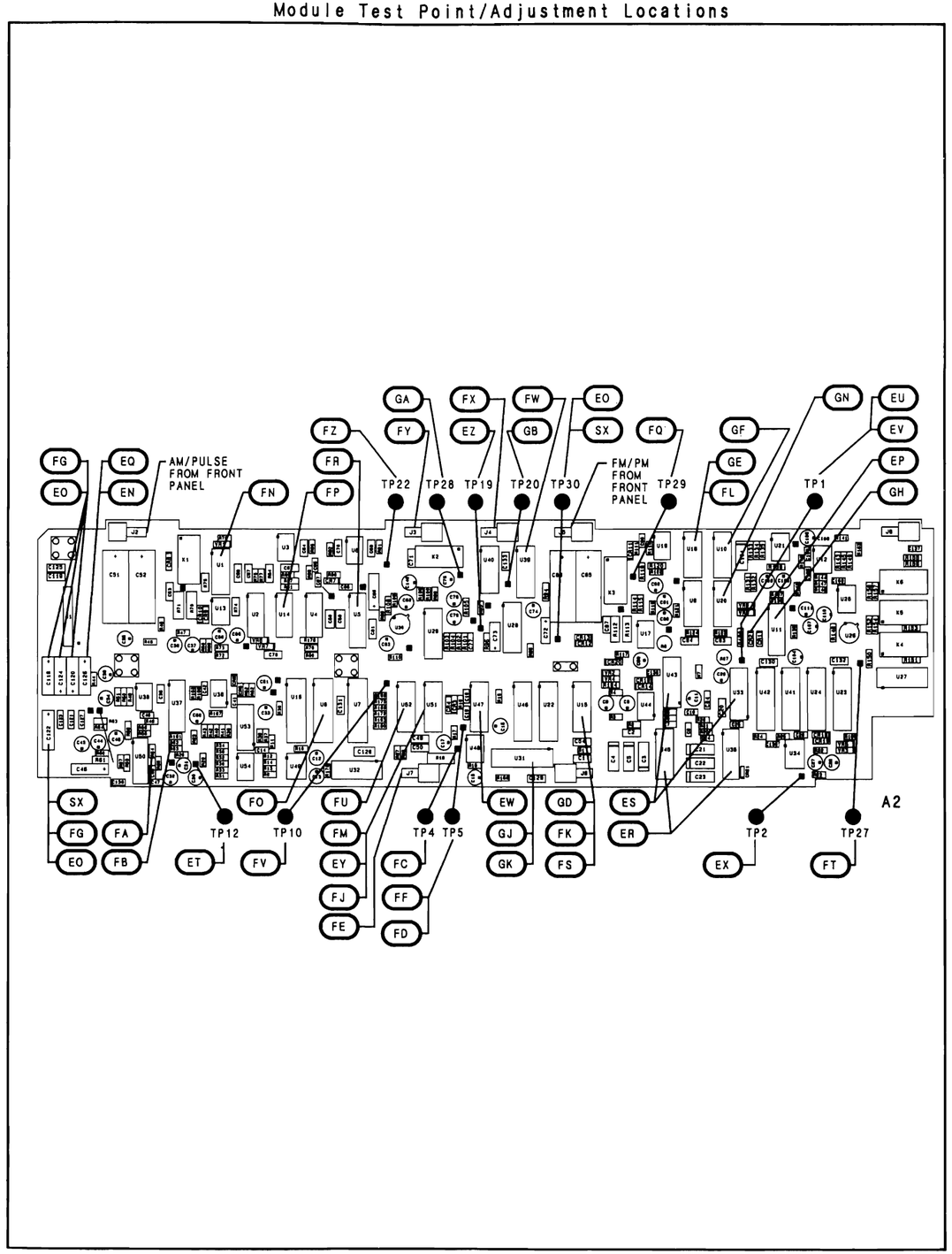


Figure 8J-102 BD6 General Information.

A2 MODULE BD5

SEE REVERSE SIDE

CHANGES

2514A and above

On the block diagram:

- In the upper left portion of the block diagram, change the A2 part number to 08642-60223.

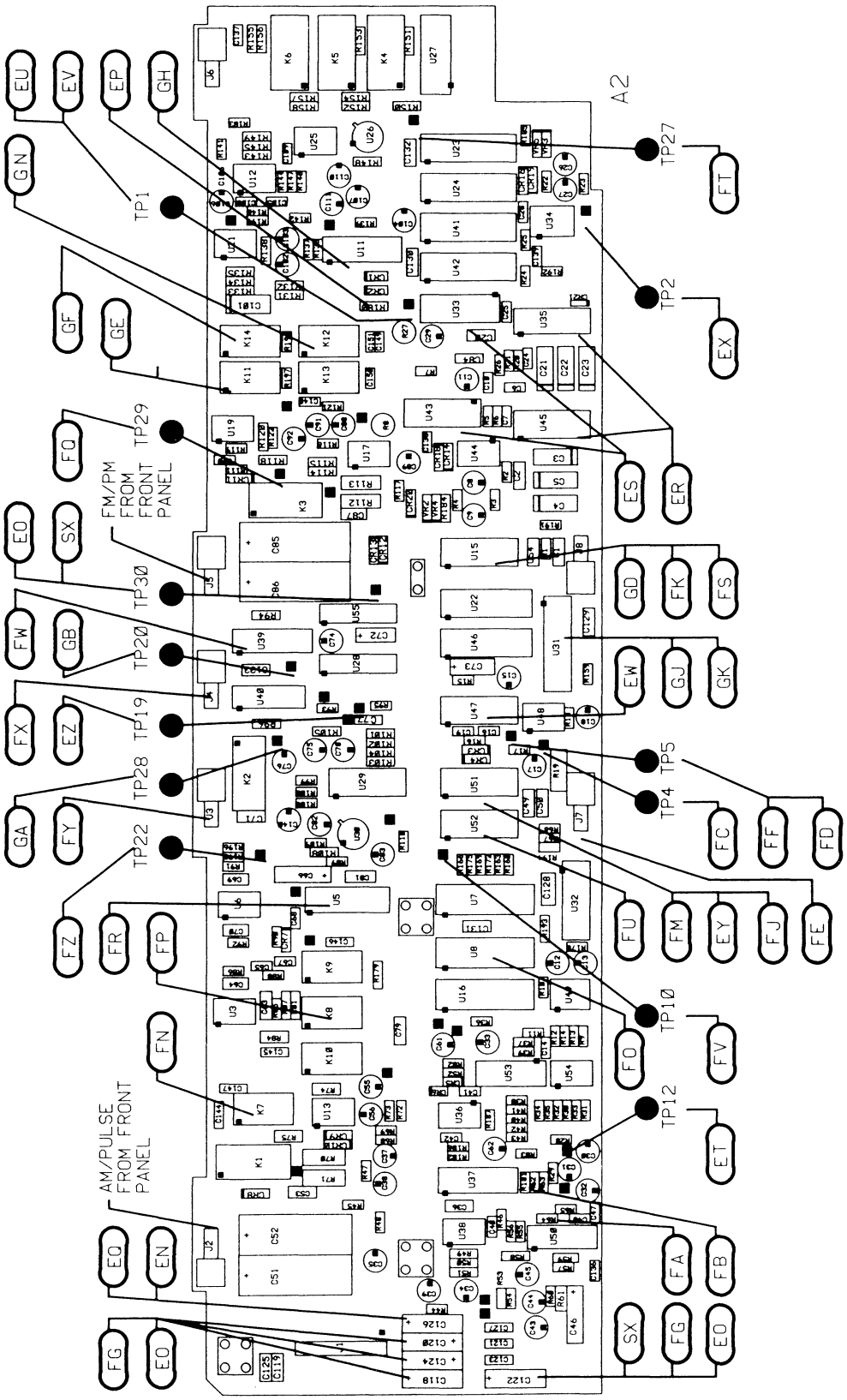
2714A and above

In General Information:

- Replace the *Module Test Point/Adjustment Locations* with the new *Module Test Point/Adjustment Locations* on page 8J-102.2.

On the block diagram:

- In the upper left portion of the block diagram, change the A2 part number to 08642-60323.



BD 6
8J-102.2

Module Test Point/Adjustment Locations (2714A and above).

P/O A2 MODULATION MODULE (08642-60123)

OPTION 002

AM/ PULSE (FROM REAR PANEL) J6 W202 945

AM/ PULSE (FROM FRONT PANEL) J1 W18 945 J2

SELF TEST SWITCH CONTROL

AM/FM SELF TEST

FM SELF TEST FM BD5

BIAS OZ BD5

AM AC/DC 2

AM INPUT AC/DC COUPLER

AM LOW NOISE AMPLIFIER

INT/AM 1

INT OSC BD5 EU

INTERNAL AM SWITCH

EXT AM

EXTERNAL AM SWITCH

AM DAC BITS 10

AM LEVEL ADJUST

AM SUMMING AMPLIFIER

+15V (REF) BD5 EQ

HI/LO AM/FM SELECT

HI/LO DETECTOR

+15V PROTECTED BD5 EP

POWER SUPPLY AND GND BD5 FQ

POWER SUPPLY AND GND +15V +5V -15V -5V GND

POWER SUPPLY AND GND 2 SX BD5

FET SWITCH REFERENCE

AF FL BD5

FM LNA BD5 FQ

EXT CNT EZ BD5

FJ FK FN FO FP FW FR

MODULATION CLK BD4 GJ

P/O J1 11

DATA LATCH SELECT

MODULATION ADDRESS/DATA BD4 GK 8

4 MOD D3
2 MOD D1
5 MOD D4
3 MOD D2
6 MOD D5
7 MOD D6
8 MOD D7
1 MOD D0

OSC DC OY BD5

CNT INT/EXT 2 EY BD5

MODULATION CONTROL LATCHES

10 ES BD5

4 ER BD5

POWER SUPPLY AND GND 16 SX 2

POWER SUPPLY AND GND +5V GND

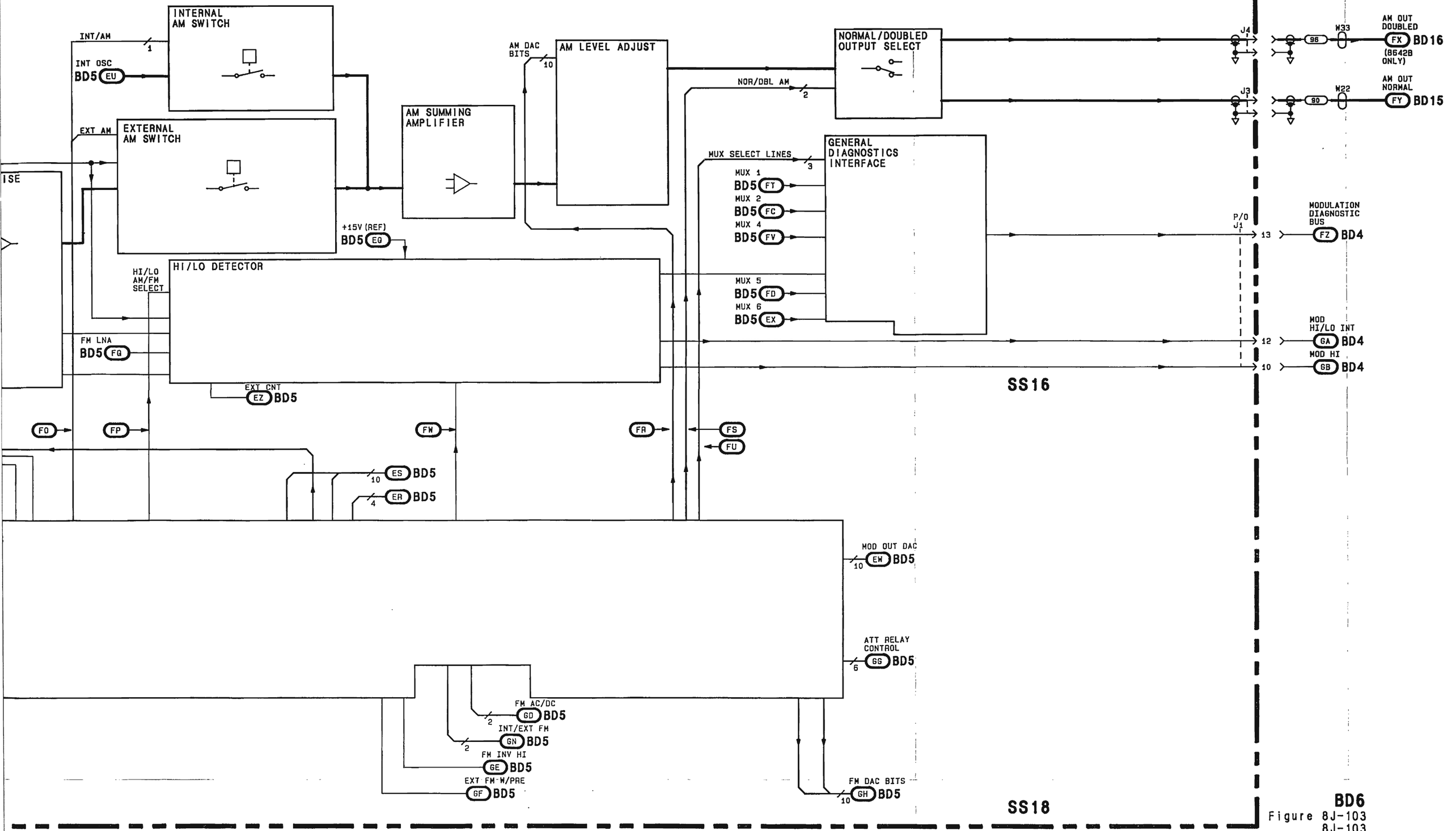
FM AC/DC 2 GD BD5

INT/EXT FM 2 GN BD5

FM INV HI GE BD5

EXT FM W/PRE GF BD5

SERIAL PREFIX: 2427A



BD6

Figure 8J-103
8J-103

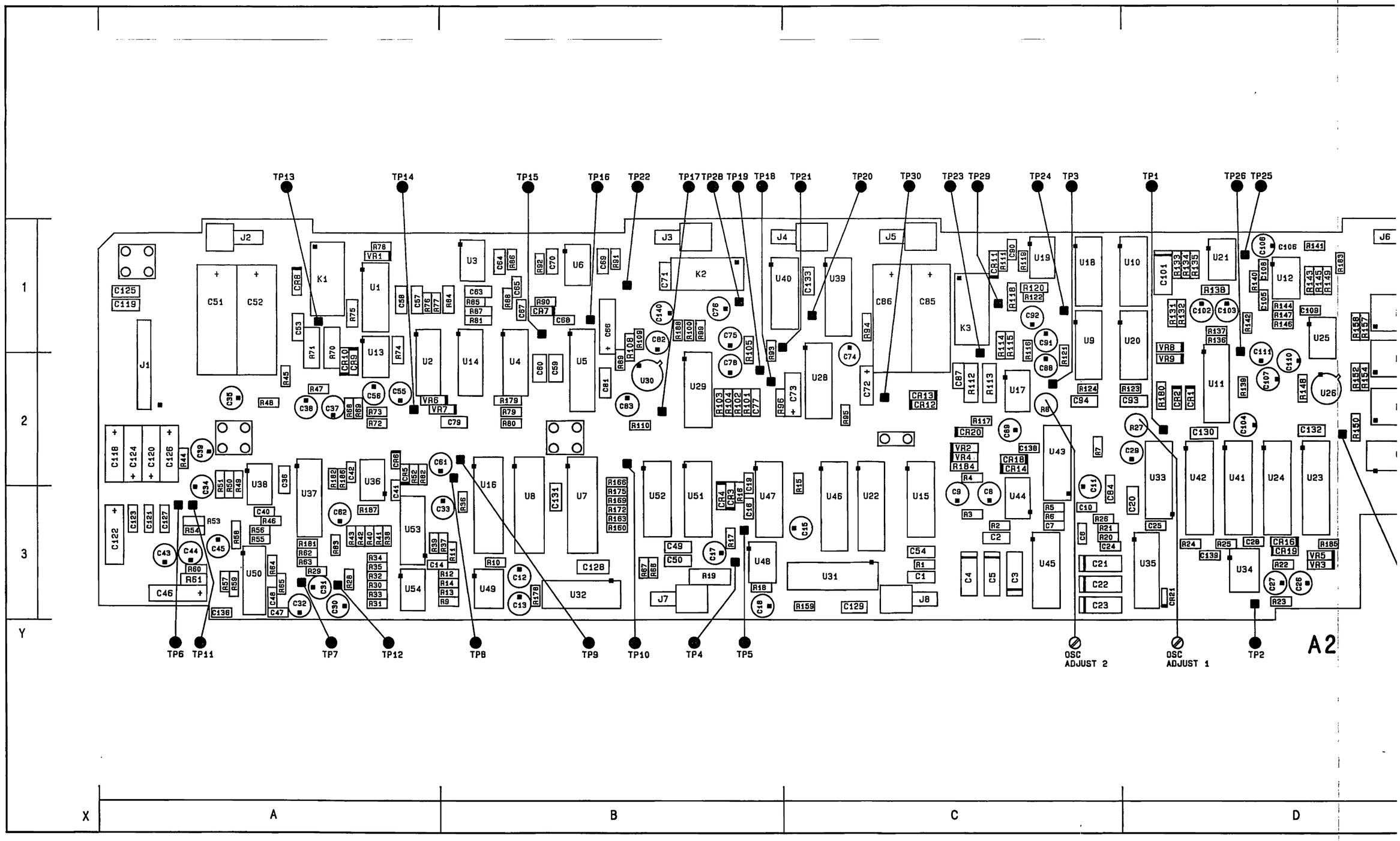
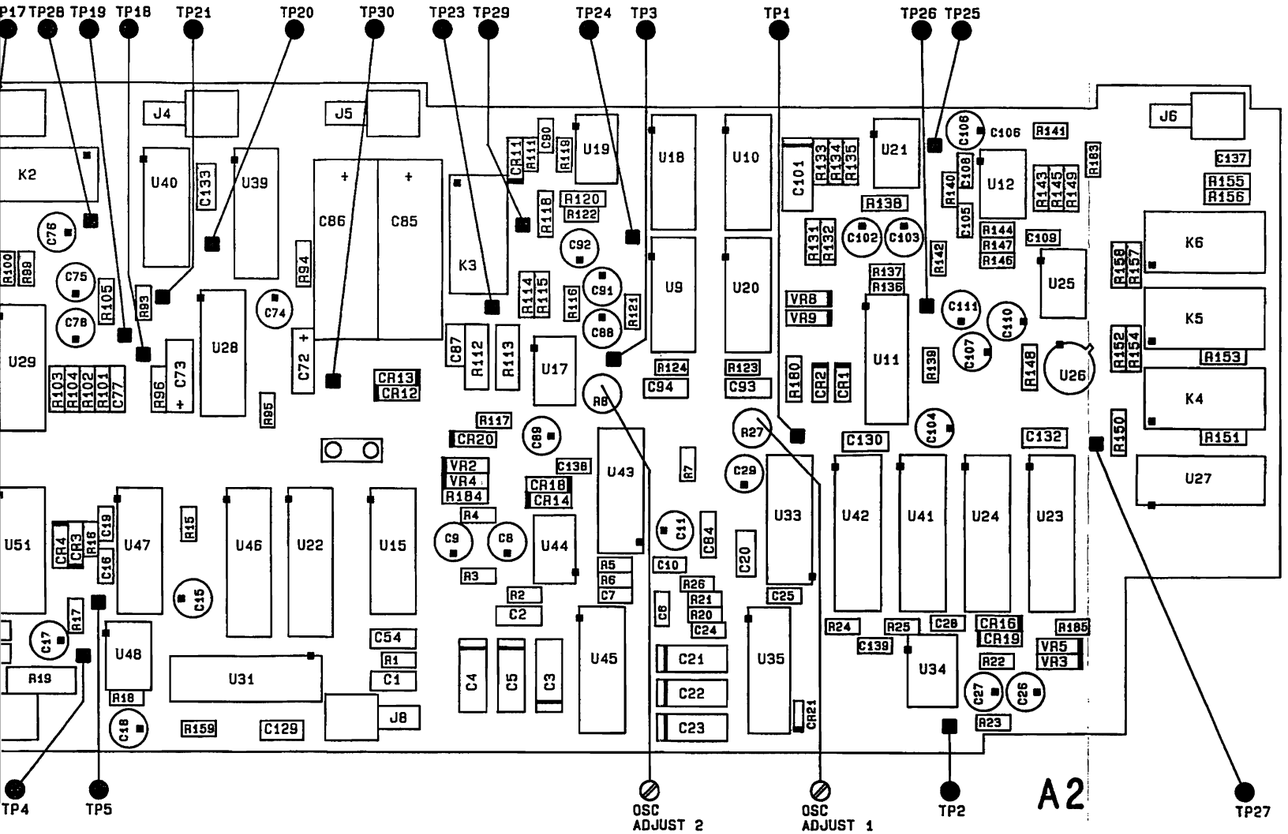


Figure 8J-104. SERVICE SHEET 14 INFORMATION

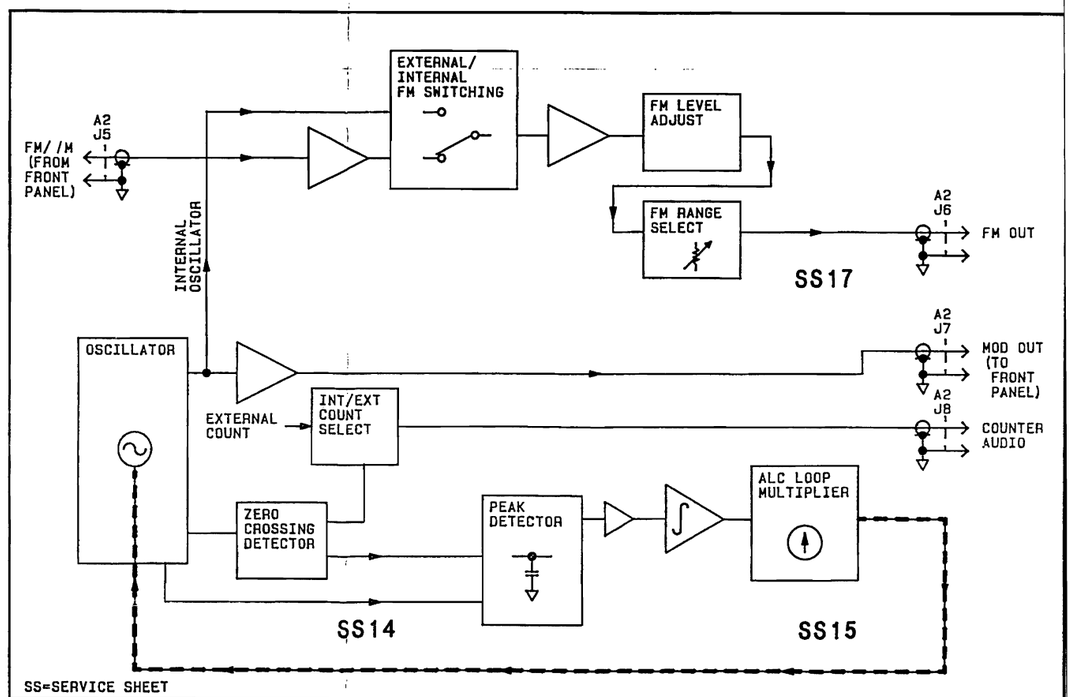
Component Locator



C

D

Component Locator



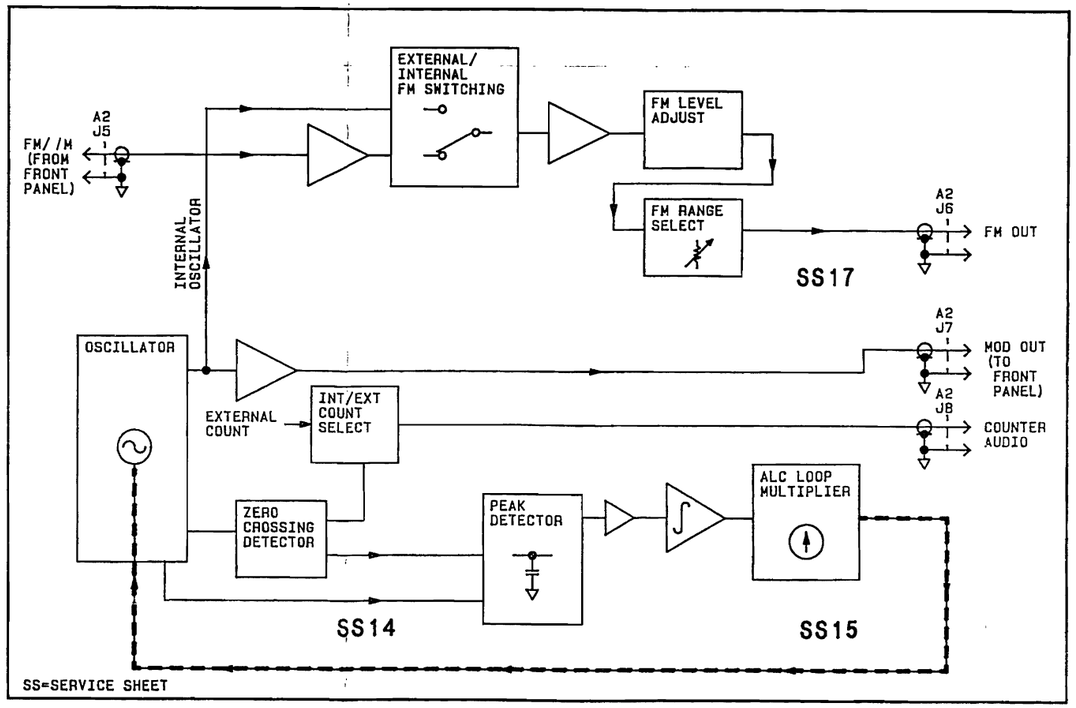
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	C, 3	C119	A, 1	R10	B, 3	TP1	D, 2								
C2	C, 3	C120	A, 2	R11	B, 3	TP2	D, 3								
C3	C, 3	C121	A, 3	R12	B, 3	TP3	C, 2								
C4	C, 3	C122	A, 3	R13	B, 3	TP4	B, 3								
C5	C, 3	C123	A, 3	R14	B, 3	TP5	B, 3								
C6	C, 3	C124	A, 2	R15	C, 3	TP6	A, 3								
C7	C, 3	C125	A, 1	R16	B, 3	TP7	A, 3								
C8	C, 3	C126	A, 2	R17	B, 3	TP30	C, 2								
C9	C, 3	C127	A, 3	R18	B, 3										
C10	C, 3	C136	A, 3	R19	B, 3	U33	D, 2								
C11	C, 2	C138	C, 2	R20	C, 3	U34	D, 3								
C12	B, 3	C138	D, 3	R21	C, 3	U35	D, 3								
C13	B, 3			R22	D, 3	U43	C, 2								
C14	A, 3	CR1	D, 2	R23	D, 3	U44	C, 3								
C15	C, 3	CR2	D, 2	R24	D, 3	U45	C, 3								
C16	B, 3	CR3	B, 3	R25	D, 3	U47	B, 3								
C17	B, 3	CR4	B, 3	R26	C, 3	U48	B, 3								
C18	B, 3	CR14	C, 2	R27	D, 2	U49	B, 3								
C19	B, 3	CR16	D, 3	R53	A, 3	U50	A, 3								
C20	D, 3	CR18	C, 2	R55	A, 3	U51	B, 3								
C21	C, 3	CR19	D, 3	R56	A, 3										
C22	C, 3	CR20	C, 2	R57	A, 3	VR2	C, 2								
C23	C, 3	CR21	D, 3	R58	A, 3	VR3	D, 3								
C24	C, 3			R59	A, 3	VR4	C, 2								
C25	D, 3	J1	A, 2	R60	A, 3	VR5	D, 3								
C26	D, 3	J7	B, 3	R61	A, 3										
C27	D, 3	J8	C, 3	R62	A, 3										
C28	D, 3			R63	A, 3										
C29	D, 2	R1	C, 3	R64	A, 3										
C43	A, 3	R2	C, 3	R65	A, 3										
C44	A, 3	R3	C, 3	R159	C, 3										
C45	A, 3	R4	C, 2	R184	C, 2										
C46	A, 3	R5	C, 3	R185	D, 3										
C47	A, 3	R6	C, 3												
C48	A, 3	R7	C, 2												
C84	C, 3	R8	C, 2												
C118	A, 2	R9	B, 3												

SEE REVERSE SIDE

P/O A2 MODULE **BD6**



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	C, 3	C119	A, 1	R10	B, 3	TP1	D, 2								
C2	C, 3	C120	A, 2	R11	B, 3	TP2	D, 3								
C3	C, 3	C121	A, 3	R12	B, 3	TP3	C, 2								
C4	C, 3	C122	A, 3	R13	B, 3	TP4	B, 3								
C5	C, 3	C123	A, 3	R14	B, 3	TP5	B, 3								
C6	C, 3	C124	A, 2	R15	C, 3	TP6	A, 3								
C7	C, 3	C125	A, 1	R16	B, 3	TP7	A, 3								
C8	C, 3	C126	A, 2	R17	B, 3	TP30	C, 2								
C9	C, 3	C127	A, 3	R18	B, 3										
C10	C, 3	C136	A, 3	R19	B, 3	U33	D, 2								
C11	C, 2	C138	C, 2	R20	C, 3	U34	D, 3								
C12	B, 3	C138	D, 3	R21	C, 3	U35	D, 3								
C13	B, 3			R22	D, 3	U43	C, 2								
C14	A, 3	CR1	D, 2	R23	D, 3	U44	C, 3								
C15	C, 3	CR2	D, 2	R24	D, 3	U45	C, 3								
C16	B, 3	CR3	B, 3	R25	D, 3	U47	B, 3								
C17	B, 3	CR4	B, 3	R26	C, 3	U48	B, 3								
C18	B, 3	CR14	C, 2	R27	D, 2	U49	B, 3								
C19	B, 3	CR16	D, 3	R53	A, 3	U50	A, 3								
C20	D, 3	CR18	C, 2	R55	A, 3	U51	B, 3								
C21	C, 3	CR19	D, 3	R56	A, 3										
C22	C, 3	CR20	C, 2	R57	A, 3	VR2	C, 2								
C23	C, 3	CR21	D, 3	R58	A, 3	VR3	D, 3								
C24	C, 3			R59	A, 3	VR4	C, 2								
C25	D, 3	J1	A, 2	R60	A, 3	VR5	D, 3								
C26	D, 3	J7	B, 3	R61	A, 3										
C27	D, 3	J8	C, 3	R62	A, 3										
C28	D, 3			R63	A, 3										
C29	D, 2	R1	C, 3	R64	A, 3										
C43	A, 3	R2	C, 3	R65	A, 3										
C44	A, 3	R3	C, 3	R159	C, 3										
C45	A, 3	R4	C, 2	R184	C, 2										
C46	A, 3	R5	C, 3	R185	D, 3										
C47	A, 3	R6	C, 3												
C48	A, 3	R7	C, 2												
C84	C, 3	R8	C, 2												
C118	A, 2	R9	B, 3												

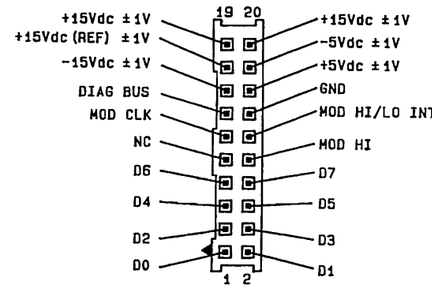
SEE REVERSE SIDE

P/O A2 MODULE BD6

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

A2J1
CABLE PLUG



CHANGES

All Serial Prefixes

On the Component Coordinates Table

- Change the second "C138" listed to "C139".

On the schematic:

- R184, 185 - In **OSCILLATOR**, change the value of R184 and R185 to 1.78K.

2514A and above

On the Component Locator:

- C141 - In grid location B,3 add C141 to the area between U16 and R11.
- C142 - In grid location B,3 add C142 to the area between R10 and R11.
- R189 - In grid location C,2 add R189 to the area between U43 and R7.

In Component Coordinates:

- C141, C142, R189,- Add components and grid coordinates shown above.

On the schematic:

- C141, C142, R189, - Replace appropriate portion of the schematic with the partial on page 8J-104.3.
- In the upper left portion of the schematic, change the A2 part number to 08642-60223.

CHANGES

2714A and above

On the Component Locator:

- SS14 - Replace *Figure 8J-104 Component Locator* with the new *Figure 8J-104 Component Locator* on page 8J-104.4.

On the Component Coordinates:

- R191, R192, R193, R194 - Add R191 C,3, R192 D,3, R193 B,3, R194, B,3.

In Schematic General Information:

- Add note 3; *TP6 is a test pad, not the post type.*

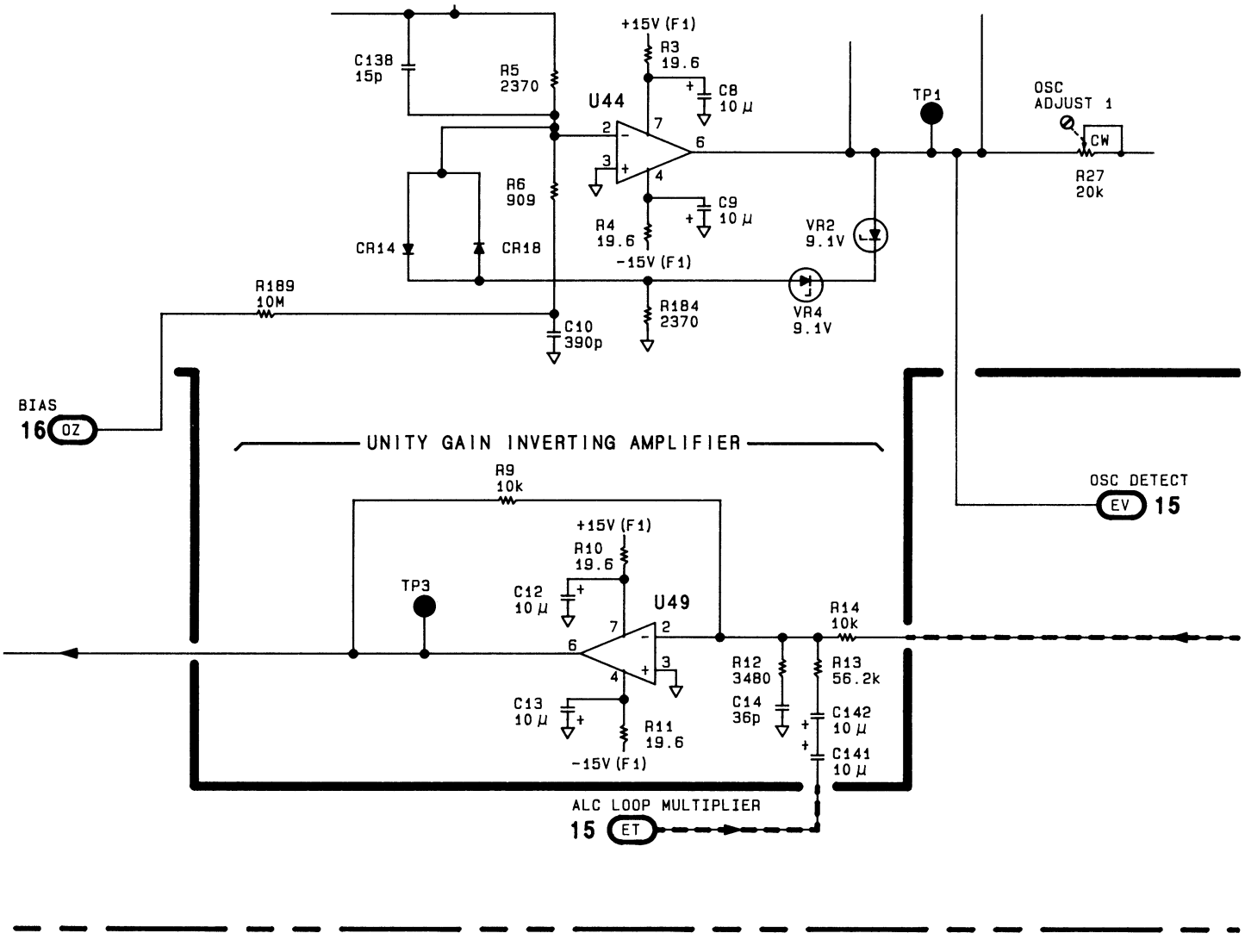
On the schematic:

- In the upper left portion of the schematic, change the A2 part number to 08642-60323.
- R5, R6, C10, R191,R192,R193 - In **OSCILLATOR**, under INTEGRATOR 1, change the value of R5 to 1.78k, R6 to 348k, C10 to 470pf and add R191 5.11K between pin 3 of U44 and ground. Under INTEGRATOR 2, change the value of R24 to 1.78k, R25 to 348k, C28 to 470pf and add R192 5.11K between pin 3 of U34 and ground. Under UNITY GAIN INVERTING AMPLIFIER, add R193 5.11K between pin 3 of U49 and ground.
- R194 - In **OUTPUT AMPLIFIER**, add R194 5.11K between pin 3 of U48 and ground.
- TP6 - In **ZERO CROSSING DETECTOR**, next to TP6 add "note 3".

2727A and above

On the schematic:

- R191,R192,R193 - In **OSCILLATOR**, under INTEGRATOR 1, change R191 to ZERO ohm. Under INTEGRATOR 2, change R192 to ZERO ohm. Under UNITY GAIN INVERTING AMPLIFIER, change R193 to ZERO ohm.
- R194 - In **OUTPUT AMPLIFIER**, change R194 to ZERO ohm.


+15V (F1)
R3
19.6
C8
10 µ
C138
15p
R5
2370
U44
TP1
OSC
ADJUST 1
CW
R27
20k
R6
909
C9
10 µ
R4
19.6
VR2
9.1V
CR14
CR18
-15V (F1)
R189
10M
R184
2370
VR4
9.1V
C10
390p
BIAS
16 OZ
UNITY GAIN INVERTING AMPLIFIER
R9
10k
OSC DETECT
EV 15
+15V (F1)
R10
19.6
TP3
C12
10 µ
U49
R14
10k
R12
3480
R13
56.2k
C14
36p
C142
10 µ
C141
10 µ
C13
10 µ
R11
19.6
-15V (F1)
ALC LOOP MULTIPLIER
15 ET

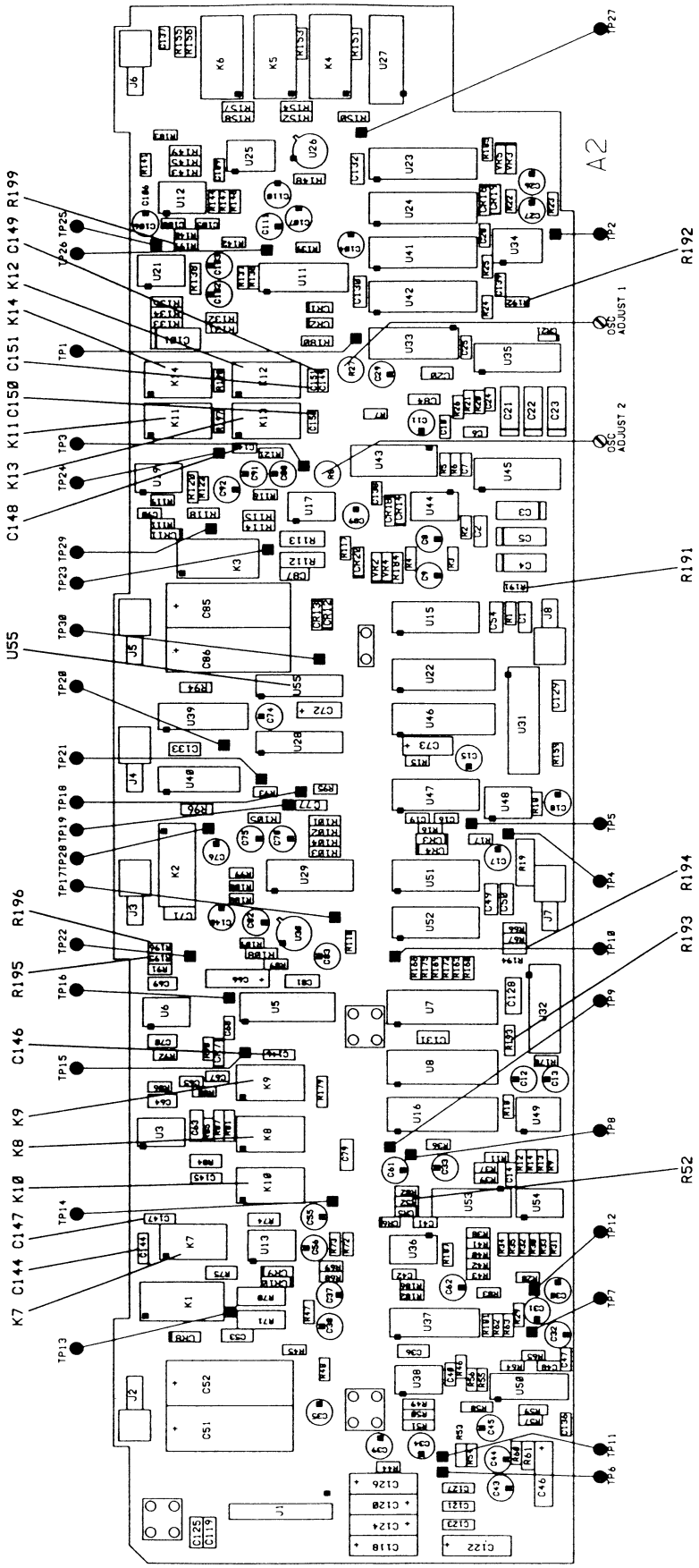


Figure 8J-104 Component Locations (2714A and above)

P/O A2 MODULATION MODULE (08642-60123)

OSC FET BITS 18 ER 4

OSC DAC BITS 18 ES 10

OSCILLATOR

INTEGRATOR 1

U45A
U45B
U45C
U45D
OSC FB0
OSC FB1
OSC FB2
OSC FB3
+15V PTCTD
R1 19.6
C1 0.1µ
C6 360p
C2 0.1µ
R2 19.6
-15V (F1)
C4 0.018µ
C5 2700p
C3 0.1µ
C7 68p

U43 [D/A CONV.] (CMOS)
OSC DB0 13
OSC DB1 12
OSC DB2 11
OSC DB3 10
OSC DB4 9
OSC DB5 8
OSC DB6 7
OSC DB7 6
OSC DB8 5
OSC DB9 4
A 0/1023
[Io1]
[Io2]
[V REF±] 15
[R FB] NC 16
R7 19.6
C11 10µ
R8 20k CW
OSC ADJUST 2
CR20
C138 15p
R5 2370
R6 909
CR14
CR18
C10 390p
U44
R3 19.6
C8 10µ
R4 19.6
C9 10µ
R184 2370
VR2 9.1V
VR4 9.1V
TP1
OSC ADJUST 1
R27 20k CW

U33 [D/A C (CMO
OSC DB0 13
OSC DB1 12
OSC DB2 11
OSC DB3 10
OSC DB4 9
OSC DB5 8
OSC DB6 7
OSC DB7 6
OSC DB8 5
OSC DB9 4
A 0/1023
[V REF±] 15
[R FB] NC 16
+15V F 1

UNITY GAIN INVERTING AMPLIFIER

R9 10k
+15V (F1)
R10 19.6
TP3
C12 10µ
U49
R14 10k
R12 3480
C14 36p
R13 56.2k
C13 10µ
R11 19.6
-15V (F1)

OSC DETECT EV 15

ALC LOOP MULTIPLIER 15 ET

POWER SUPPLY AND GND

+15V PROTECTED
+15V (F1)
CR1
CR2
+5V (F1)
+15V PROTECTED EP 15, 16, 17

+15V SENSE POINT REF 56 EN
P/O J1
17 +15V
C126 6.8µ
C127 0.1µ
+15V (REF)
+15V (REF) EQ 15, 16
19, 20 +15V
C118 6.8µ
C119 0.1µ
+15V (F1)
+15V (F1)
POWER SUPPLIES AND GROUND 56 EO 6
16 +5V
C122 33µ
C123 0.1µ
+5V (F1)
+5V (F1)
15 -15V
C120 6.8µ
C121 0.1µ
-15V (F1)
-15V (F1)
18 -5V
C124 33µ
C125 0.1µ
-5V (F1)
-5V (F1)
14 GND
GND
TP30
POWER SUPPLY AND GND FG 18
2 +5V (F1), GND
POWER SUPPLY AND GND FG 15, 16, 17
5

SERIAL PREFIX: 2427A

INT OSC
EU 16,17

MOD OUT DAC
18 EW

OUTPUT AMPLIFIER

U47 [D/A CONV.] (CMOS)
DAC 0 13
DAC 1 12
DAC 2 11
DAC 3 10
DAC 4 9
DAC 5 8
DAC 6 7
DAC 7 6
DAC 8 5
DAC 9 4
A 0/1023
[Io1] 1
[Io2] 2
15 [V REF±]
16 [R FB]
3
+15V PTCTD
C15 10µ
R15 19.6
+15V (F1)
R17 19.6
C17 10µ
U48
R16 2370
C16 56p
R18 19.6
C18 10µ
-15V (F1)
TP4
C19 10p
R19 600
+15V (F1)
CR3
CR4
-15 (F1)

INTEGRATOR 2

+15V PTCTD
R20 19.6
C84 0.1µ
NC
U35A
OSC FB0 1
X1 1 2
1 3
C24 360p
4 5
C20 0.1µ
R21 19.6
-15V (F1)
U35B
OSC FB2 8
X2 7 2
2 6
C22 0.018µ
U35C
OSC FB1 9
X3 10 3
3 11
C23 2700p
U35D
OSC FB3 16
X4 15 4
4 14
C21 0.1µ
C25 68p

+15V PTCTD
R26 19.6
C29 10µ
U33 [D/A CONV.] (CMOS)
OSC DB0 13
OSC DB1 12
OSC DB2 11
OSC DB3 10
OSC DB4 9
OSC DB5 8
OSC DB6 7
OSC DB7 6
OSC DB8 5
OSC DB9 4
A 0/1023
[Io1] 1
[Io2] 2
15 [V REF±]
NC 16 [R FB]
3
OSC ADJUST 1
CW
R27 20k
TP1
CR21
C139 15p
R24 2370
+15V (F1)
R22 19.6
C26 10µ
U34
R25 909
C28 390p
R23 19.6
C27 10µ
-15V (F1)
CR16
CR19
R185 2370
VR3 9.1V
VR5 9.1V
TP2
MUX 6
EX 16

OSC DETECT
EV 15

R14 10k
R13 56.2k

ZERO CROSSING DETECTOR

C136 10p
TP6
R59 316k
R58 316k
+5V (F1)
R55 19.6
+15V (F1)
R56 1k
R54 19.6
C44 10µ
U50
C45 10µ
COMP
13 G1
8 G2
3
4
1 11
2 9
6 10 2,5,7,12
NC
C43 10µ
R53 19.6
-15V (F1)
R60 34.8k
C46 3.3µ
R61 261k
R57 10k
TP7

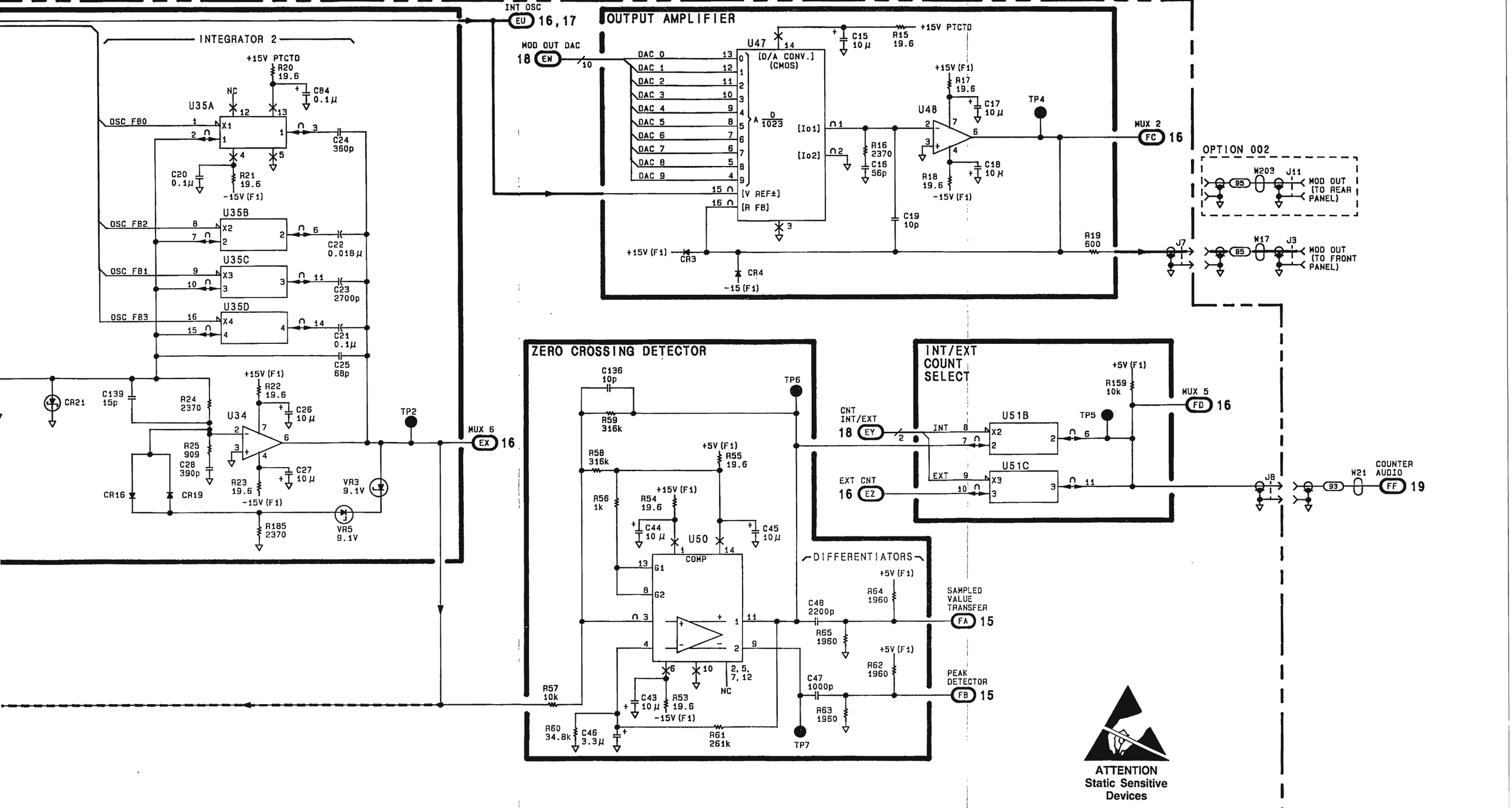
DIFFERENTIATORS

+5V (F1)
R64 1960
C48 2200p
R65 1960
SAMPLED VALUE TRANSFER
FA 15
+5V (F1)
R62 1960
C47 1000p
R63 1960
PEAK DETECTOR
FB 15

INT/EXT COUNT SELECT

+5V (F
R159 10k
CNT INT/EXT
18 EY
INT 8
U51B
X2 7 2
2 6
TP5
EXT CNT
16 EZ
EXT 9
U51C
X3 10 3
3 11

ATTENTI
Static Sen
Device



SS14
Figure 8J-105
8J-105

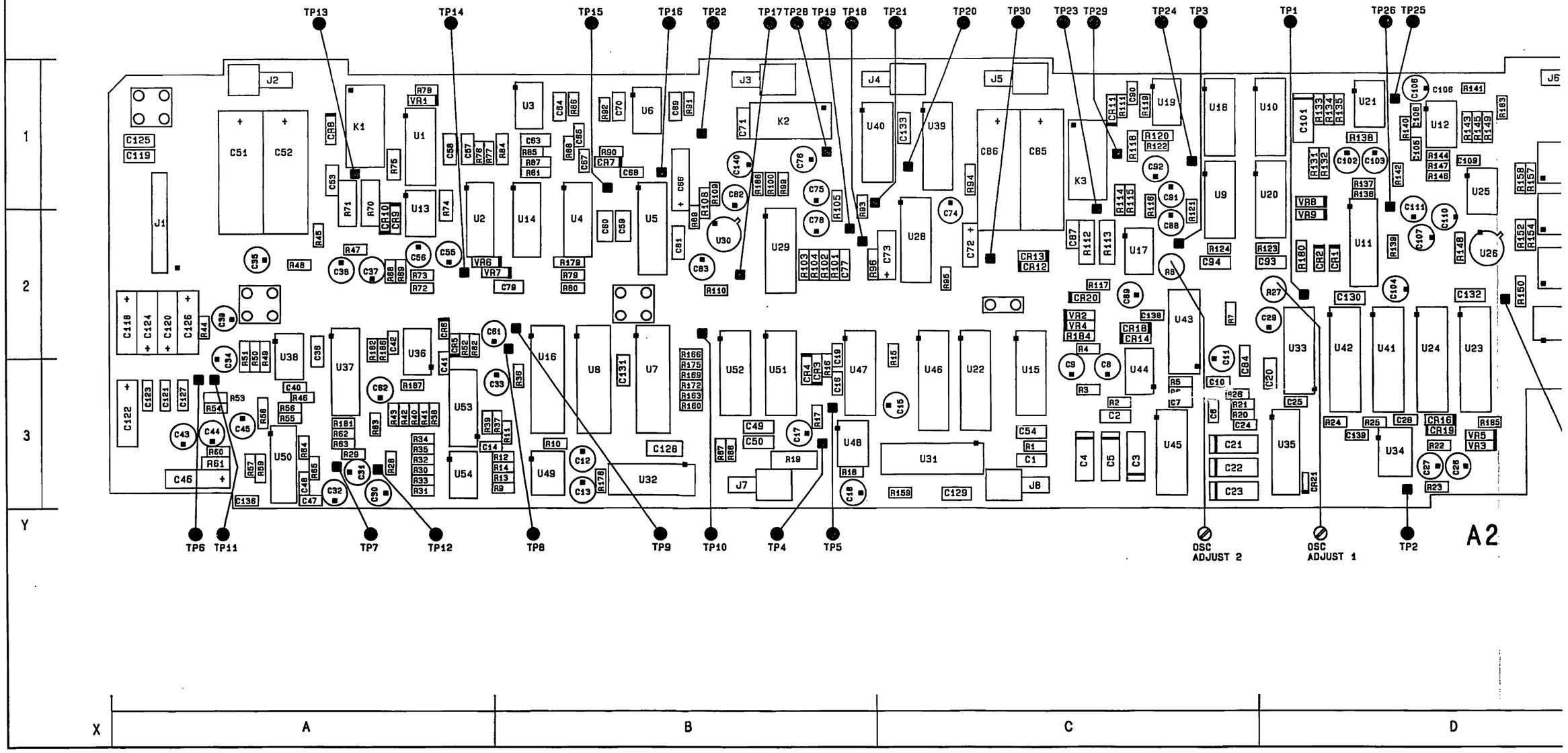
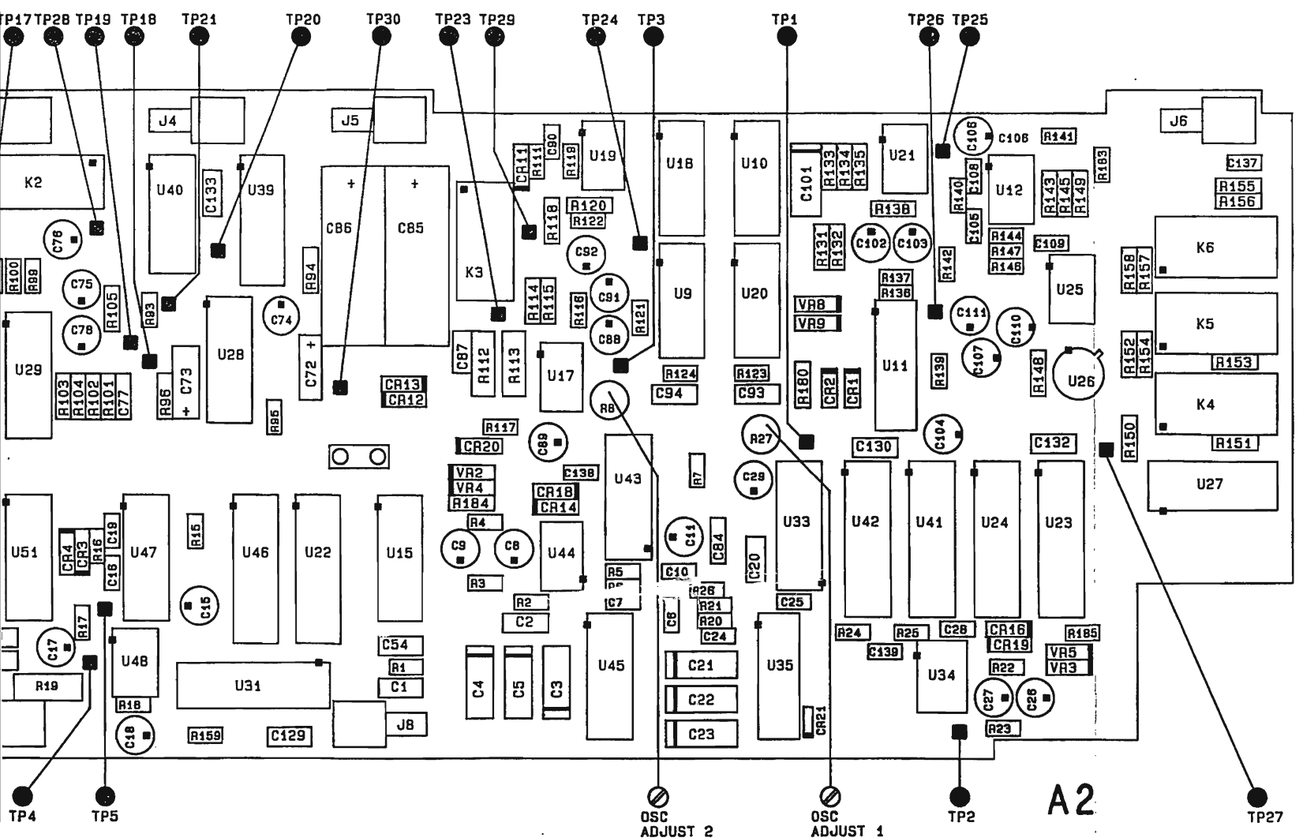


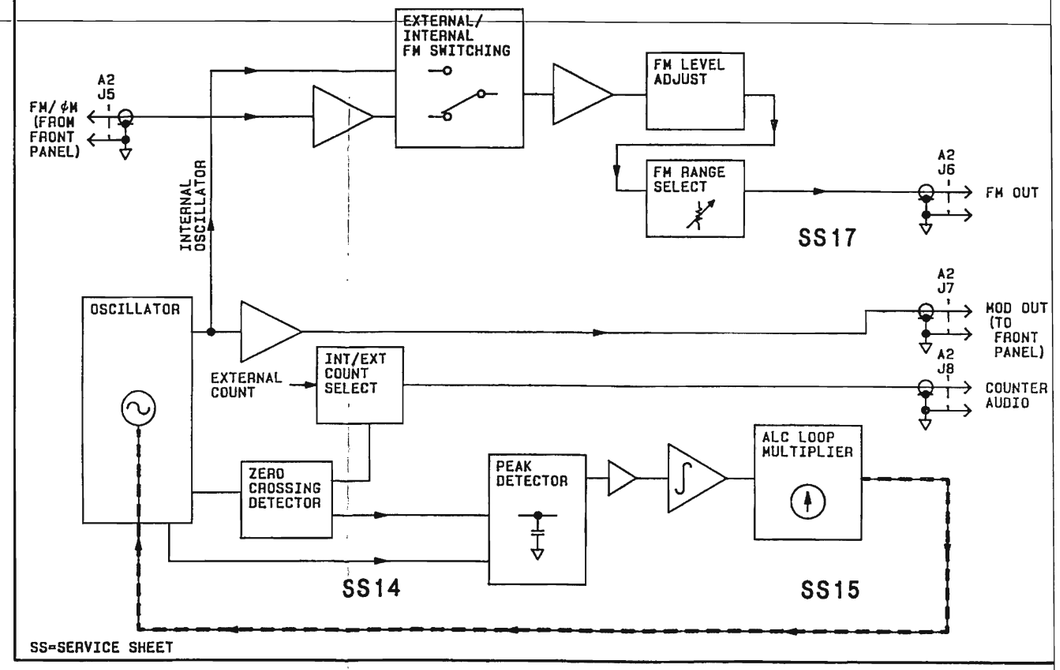
Figure 8J-106. SERVICE SHEET 15 INFORMATION

Component Locator



C D

Component Locator



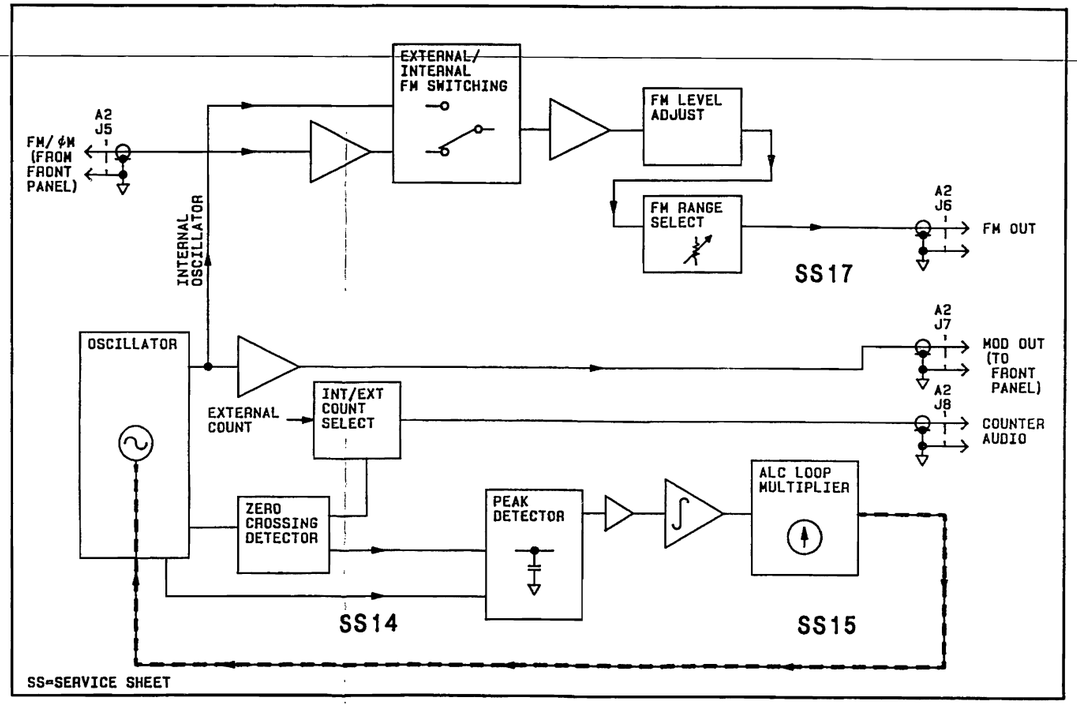
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C30	A, 3	R46	A, 3												
C31	A, 3	R47	A, 2												
C32	A, 3	R48	A, 2												
C33	B, 3	R49	A, 2												
C34	A, 3	R50	A, 2												
C35	A, 2	R50	A, 2												
C36	A, 2	R51	A, 2												
C37	A, 2	R52	A, 2												
C38	A, 2	R66	B, 3												
C39	A, 2	R67	B, 3												
C40	A, 3	R68	A, 2												
C41	A, 3	R69	A, 2												
C42	A, 2	R70	A, 1												
C61	A, 2	R71	A, 1												
C62	A, 3	R72	A, 2												
		R73	A, 2												
CR5	A, 2	R74	A, 1												
CR6	A, 2	R75	A, 1												
		R76	A, 1												
R28	A, 3	R82	A, 2												
R29	A, 3	R83	A, 3												
R30	A, 3	R181	A, 3												
R31	A, 3	R182	A, 2												
R32	A, 3	R186	A, 2												
R33	A, 3	R187	A, 3												
R34	A, 3														
R35	A, 3	TP8	B, 2												
R36	B, 3	TP9	B, 2												
R37	B, 3	TP10	B, 2												
R38	A, 3	TP11	A, 3												
R39	A, 3	TP12	A, 3												
R40	A, 3														
R41	A, 3	U36	A, 2												
R42	A, 3	U37	A, 3												
R43	A, 3	U38	A, 2												
R44	A, 2	U53	A, 3												
R45	A, 2	U54	A, 3												

P/O A2 MODULATION MODULE **SS14**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C30	A, 3	R46	A, 3												
C31	A, 3	R47	A, 2												
C32	A, 3	R48	A, 2												
C33	B, 3	R49	A, 2												
C34	A, 3	R50	A, 2												
C35	A, 2	R50	A, 2												
C36	A, 2	R51	A, 2												
C37	A, 2	R52	A, 2												
C38	A, 2	R66	B, 3												
C39	A, 2	R67	B, 3												
C40	A, 3	R68	A, 2												
C41	A, 3	R69	A, 2												
C42	A, 2	R70	A, 1												
C61	A, 2	R71	A, 1												
C62	A, 3	R72	A, 2												
		R73	A, 2												
CR5	A, 2	R74	A, 1												
CR6	A, 2	R75	A, 1												
		R76	A, 1												
R28	A, 3	R82	A, 2												
R29	A, 3	R83	A, 3												
R30	A, 3	R181	A, 3												
R31	A, 3	R182	A, 2												
R32	A, 3	R186	A, 2												
R33	A, 3	R187	A, 3												
R34	A, 3														
R35	A, 3	TP8	B, 2												
R36	B, 3	TP9	B, 2												
R37	B, 3	TP10	B, 2												
R38	A, 3	TP11	A, 3												
R39	A, 3	TP12	A, 3												
R40	A, 3														
R41	A, 3	U36	A, 2												
R42	A, 3	U37	A, 3												
R43	A, 3	U38	A, 2												
R44	A, 2	U53	A, 3												
R45	A, 2	U54	A, 3												

P/O A2 MODULATION MODULE **SS14**

SEE REVERSE SIDE

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

CHANGES

2514A and above

On the Component Locator:

- C143 - In grid location A,2 add C143 immediately above U37.
- R190 - In grid location A,2 add R190 immediately above U36.

In Component Coordinates:

- C143, R190 - Add components and grid coordinates shown above.

On the schematic:

- C143, R190 - In **PEAK DETECTOR**, add a resistor in series with U36 pin 3. Designate it R190, and assign a value of 3160 ohms. Between R190 and U36 pin 3, add a capacitor to ground. Designate it C143, and assign a value of 100p Farads.
- In the upper left portion of the schematic, change the A2 part number to 08642-60223.

2714A and above

On the Component Locator:

- Use *Figure 8J-106 Component Locations* with *Figure 8J-106 Component Locations* on page 8J-106.2.

In Schematic General Information:

- Add note 3; *TP9 is a test pad not the post type.*

On the Component Coordinates:

- Delete R66-76.

On the schematic:

- In the upper left portion of the schematic, change the A2 part number to 08642-60323.
- TP9 - In **PEAK DETECTOR**, next to TP9 add "note" 3.

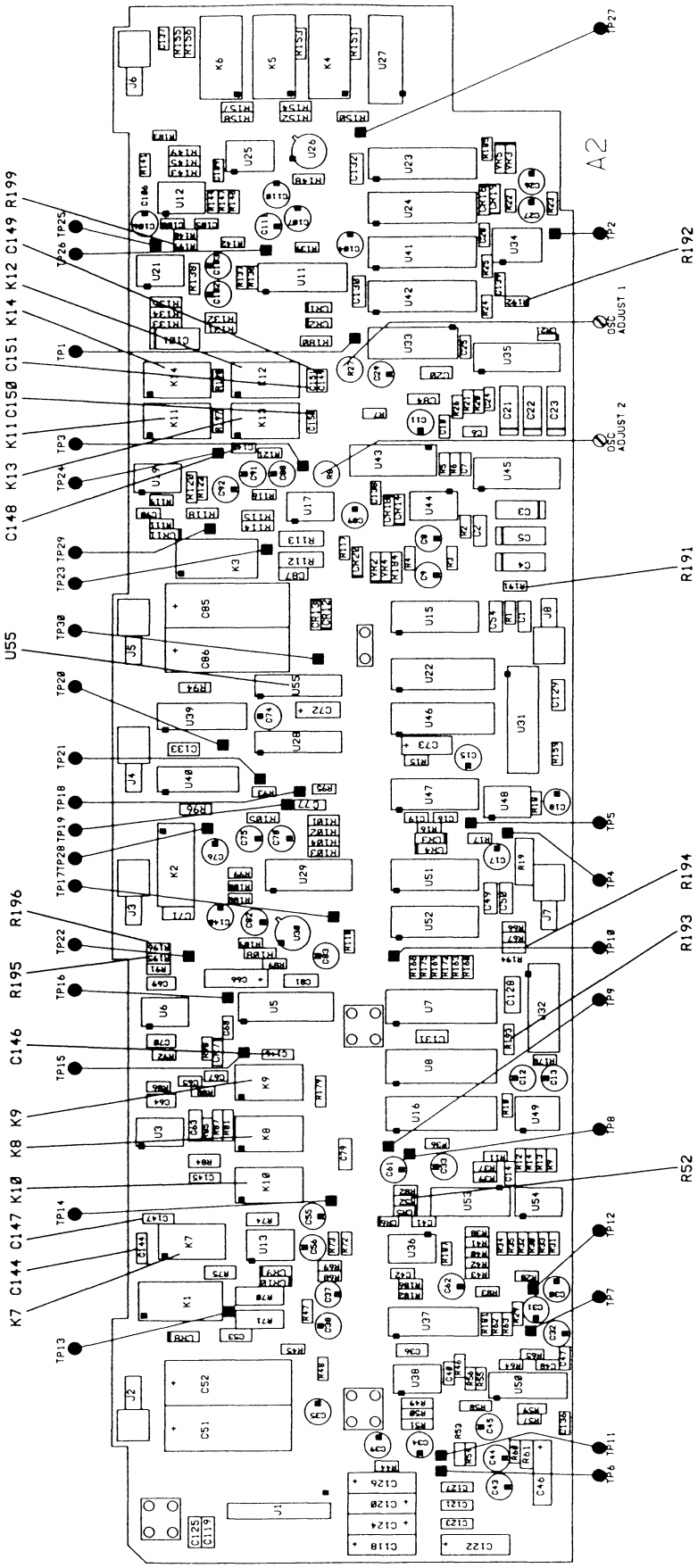
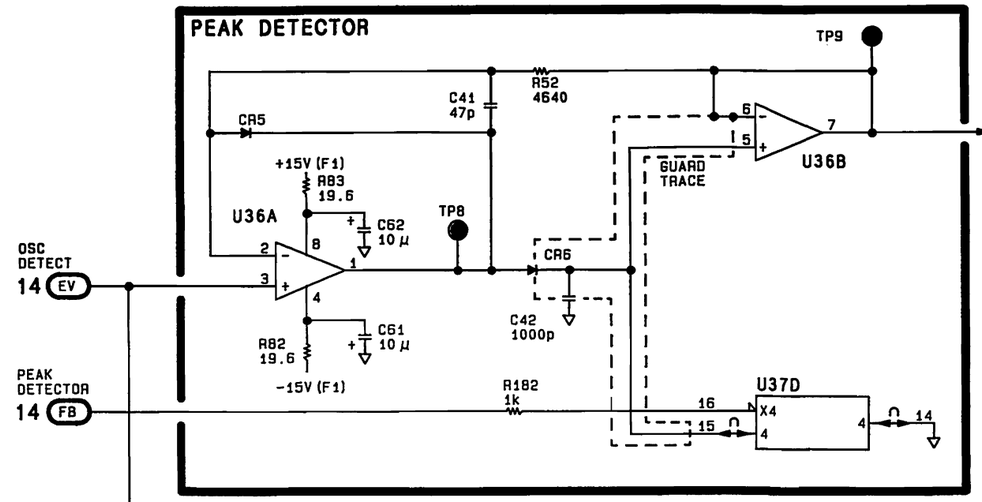
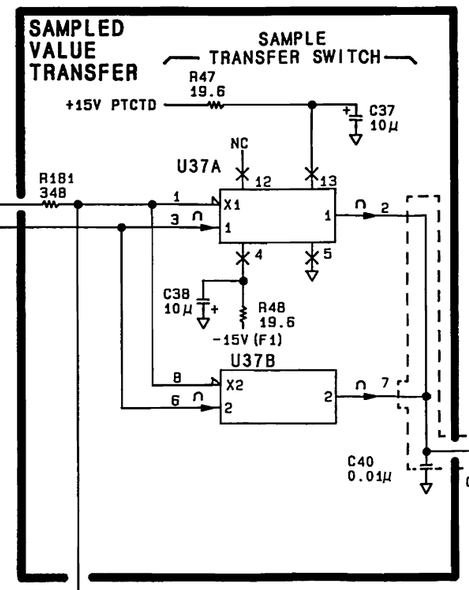
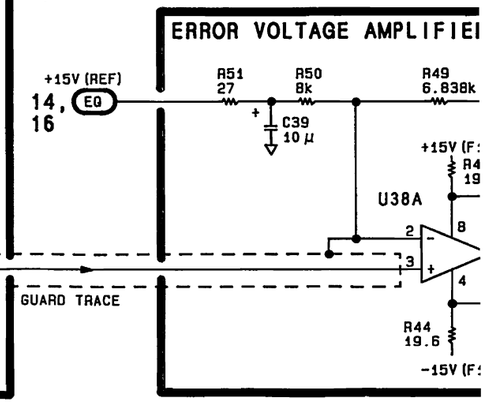


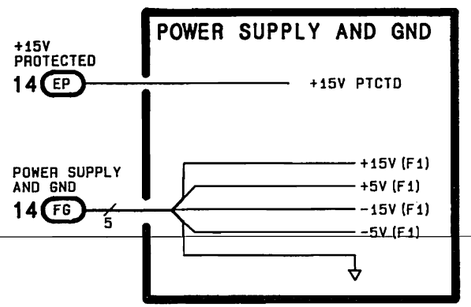
Figure 8J-106 Component Locations (2714A and above)

P/O A2 MODULATION MODULE (08642-60123)

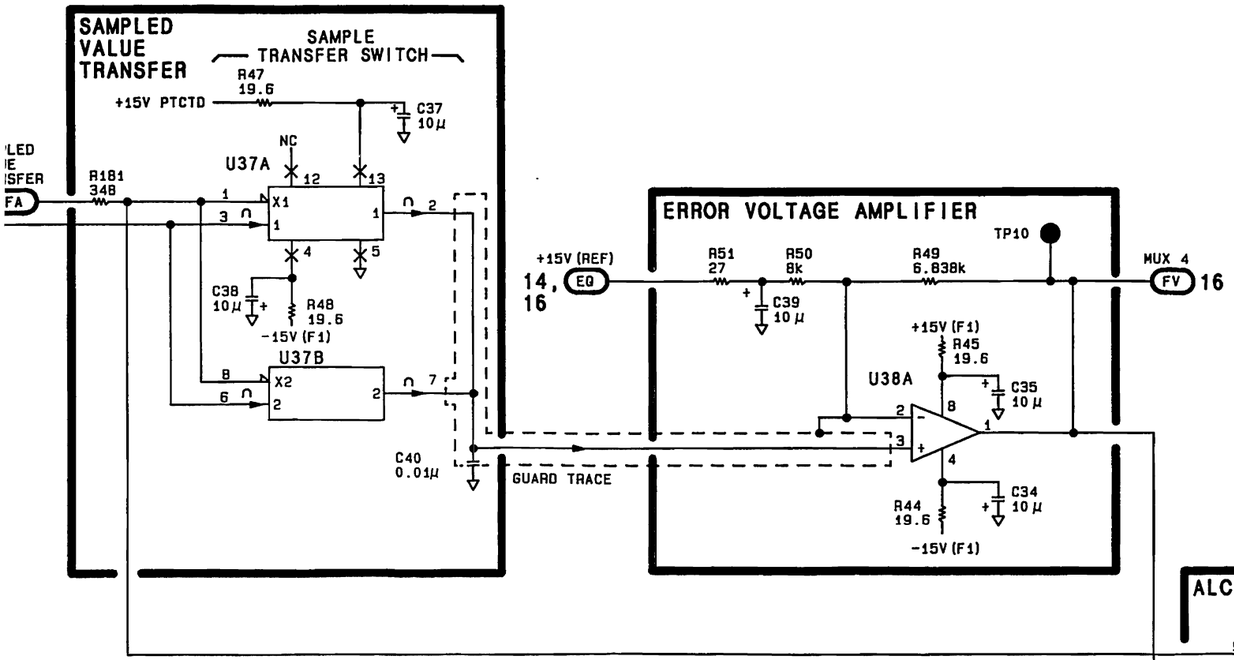


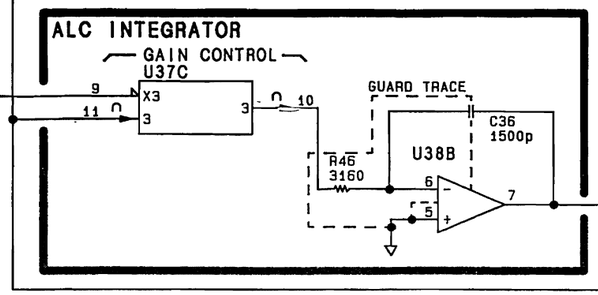


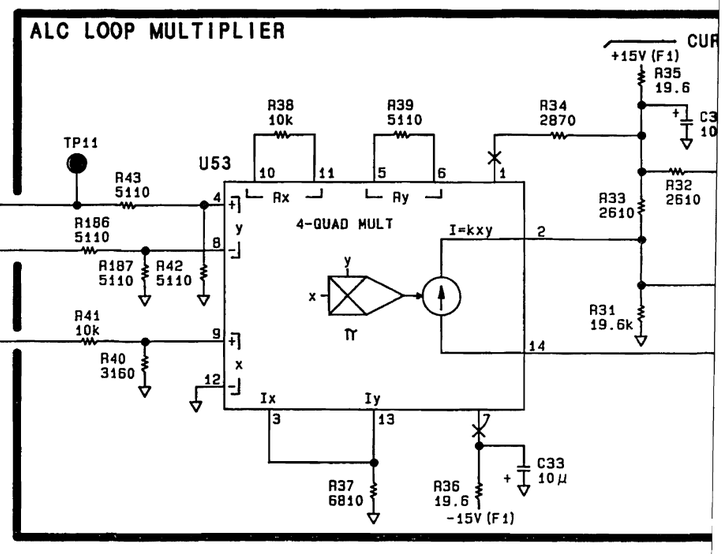




SERIAL PREFIX: 2427A







MUX 4
FV 16

ATTENTION
Static Sensitive
Devices

ALC INTEGRATOR
GAIN CONTROL
U37C
X3
GUARD TRACE
R46
3160
U38B
C36
1500p

ALC LOOP MULTIPLIER
CURRENT TO VOLTAGE
+15V (F1)
R35
19.6
C32
10
R38
10k
R39
5110
R34
2870
TP11
TP12
U53
R43
5110
R186
5110
R187
5110
R42
5110
R41
10k
R40
3160
Rx
Ry
4-QUAD MULT
I=kxy
R33
2610
R32
2610
R30
19.6k
R28
19.6
C30
10 µ
U54
R31
19.6k
R29
19.6
-15V (F1)
C31
10 µ
Ix
Iy
R37
6810
R36
19.6
-15V (F1)
C33
10 µ

ALC
LOOP
MULTIPLIER
ET 14

SS15
Figure 8J-107
8J-107

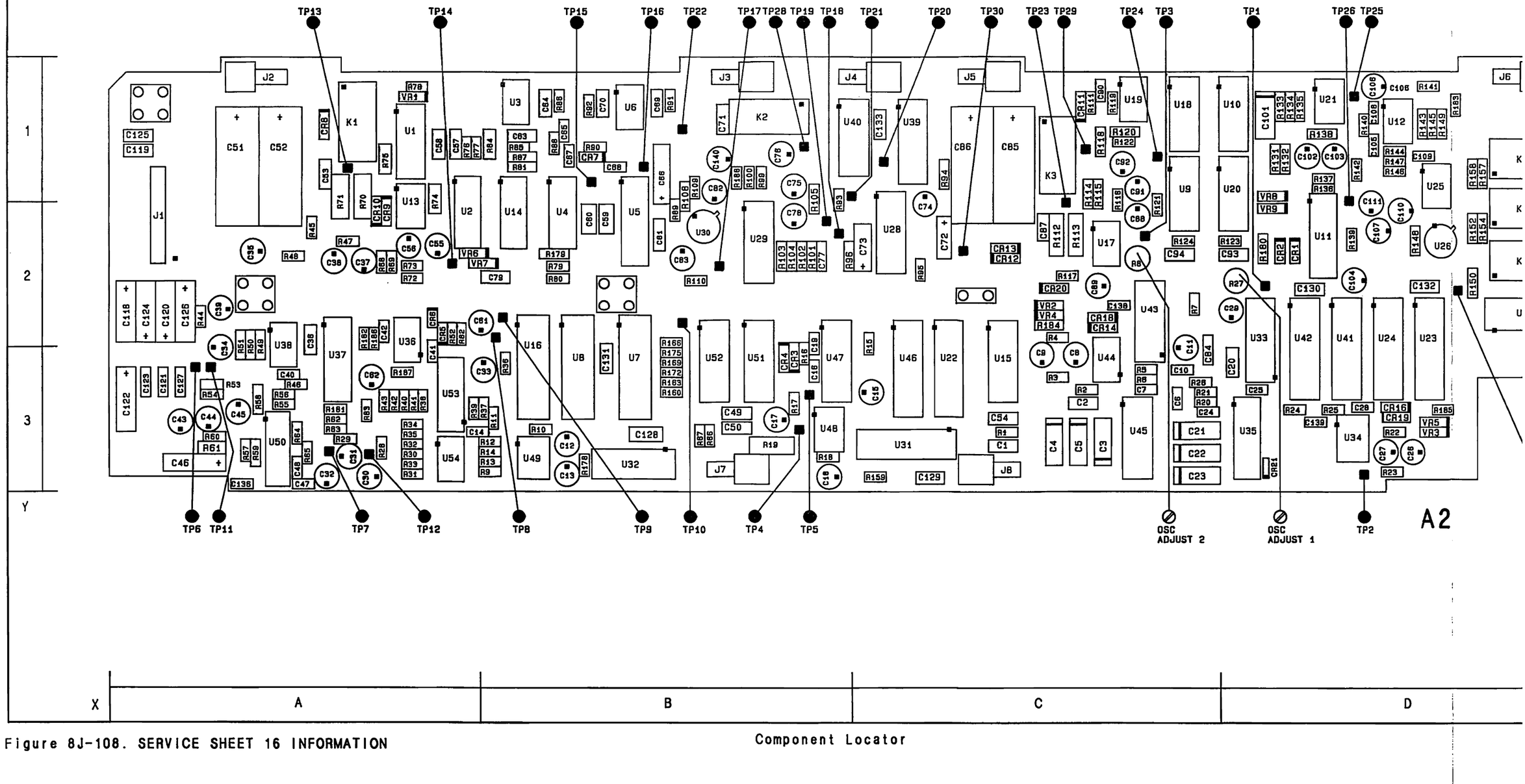
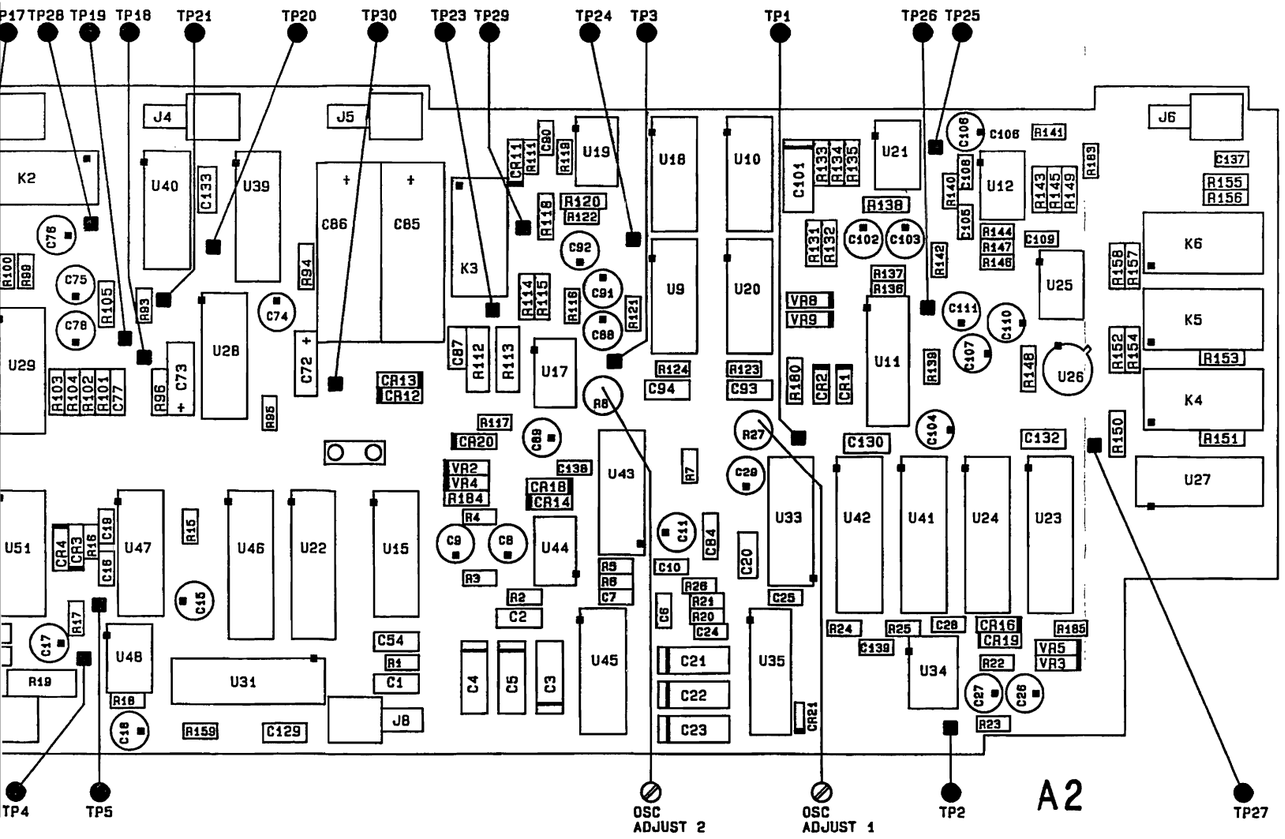


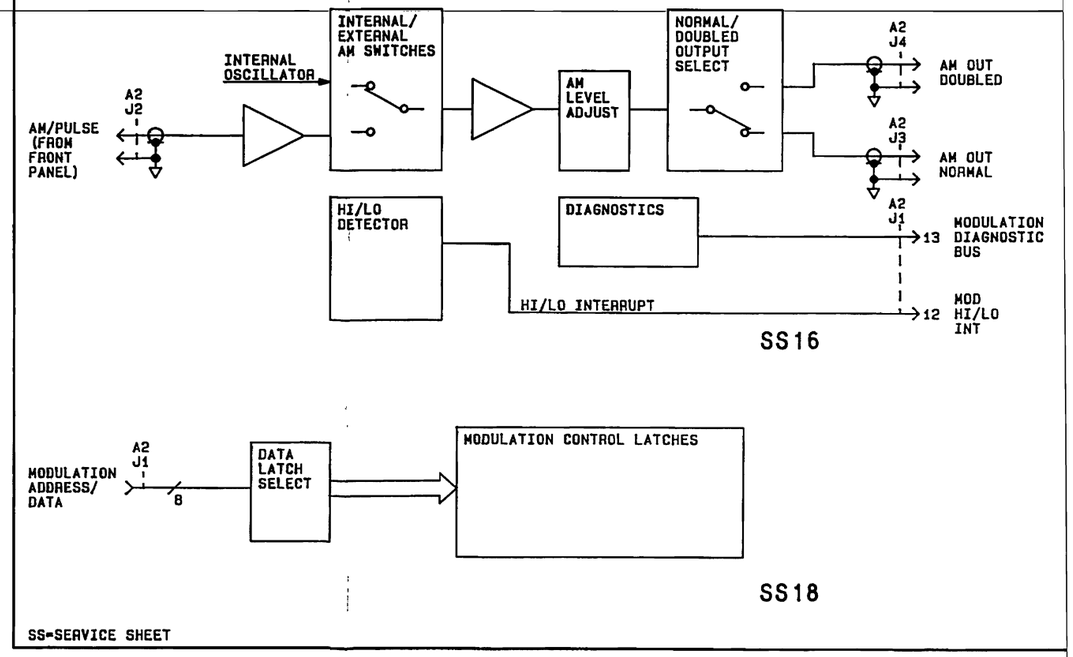
Figure 8J-108. SERVICE SHEET 16 INFORMATION

Component Locator



C D

Component Locator



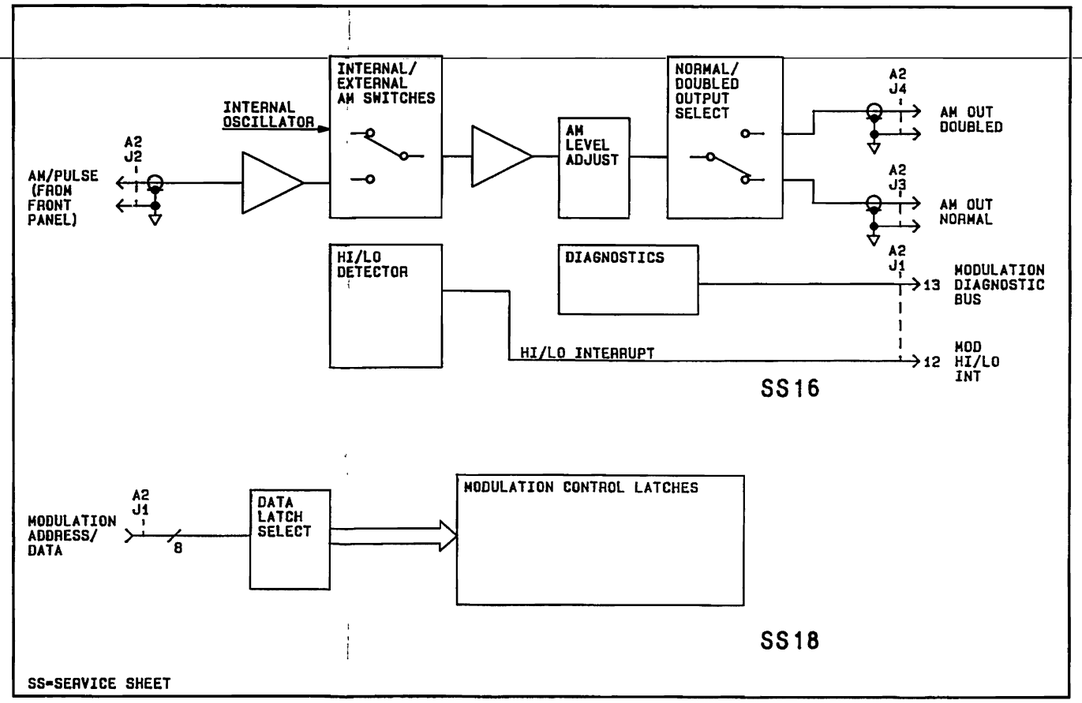
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C49	B,3	CR7	B,1	R103	B,2	U1	A,1								
C50	B,3	CR8	A,1	R104	B,2	U2	A,2								
C51	A,1	CR9	A,2	R105	B,1	U3	B,1								
C52	A,1	CR10	A,2	R108	B,1	U4	B,2								
C53	A,1	CR11	C,1	R109	B,1	U5	B,2								
C55	A,2			R110	B,2	U6	B,1								
C56	A,2	J1	A,2	R111	C,1	U13	A,1								
C57	A,1	J2	A,1	R160	B,3	U14	B,2								
C58	A,1	J3	B,1	R163	B,3	U15	C,3								
C59	B,2	J4	C,1	R166	B,2	U28	C,2								
C60	B,2			R169	B,3	U29	B,2								
C63	B,1	K1	A,1	R172	B,3	U30	B,2								
C64	B,1	K2	B,1	R175	B,3	U39	C,1								
C65	B,1			R179	B,2	U40	C,1								
C66	B,1			R188	B,1	U51	B,3								
C67	B,1	R77	A,1			U52	B,3								
C68	B,1	R78	A,1	TP13	A,1										
C69	B,1	R79	B,2	TP14	A,2	VR1	A,1								
C70	B,1	R80	B,2	TP15	B,1	VR6	A,2								
C71	B,1	R81	B,1	TP16	B,1	VR7	A,2								
C72	C,2	R84	B,1	TP17	B,2										
C73	C,2	R85	B,1	TP18	B,2										
C74	C,2	R86	B,1	TP19	B,2										
C75	B,1	R87	B,1	TP20	C,1										
C76	B,1	R88	B,1	TP21	C,1										
C77	B,2	R89	B,2	TP22	B,1										
C78	B,2	R90	B,1	TP28	B,1										
C81	B,2	R91	B,1												
C82	B,1	R92	B,1												
C83	B,2	R93	B,2												
C128	B,3	R94	C,1												
C140	B,1	R95	C,2												
		R96	B,2												
		R99	B,1												
		R100	B,1												
		R101	B,2												
		R102	B,2												

P/O A2 MODULATION MODULE **SS15**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C49	B,3	CR7	B,1	A103	B,2	U1	A,1								
C50	B,3	CR8	A,1	A104	B,2	U2	A,2								
C51	A,1	CR9	A,2	A105	B,1	U3	B,1								
C52	A,1	CR10	A,2	A108	B,1	U4	B,2								
C53	A,1	CR11	C,1	A109	B,1	U5	B,2								
C55	A,2			A110	B,2	U6	B,1								
C56	A,2	J1	A,2	A111	C,1	U13	A,1								
C57	A,1	J2	A,1	A160	B,3	U14	B,2								
C58	A,1	J3	B,1	A163	B,3	U15	C,3								
C59	B,2	J4	C,1	A166	B,2	U28	C,2								
C60	B,2			A169	B,3	U29	B,2								
C63	B,1	K1	A,1	A172	B,3	U30	B,2								
C64	B,1	K2	B,1	A175	B,3	U39	C,1								
C65	B,1			A179	B,2	U40	C,1								
C66	B,1			A188	B,1	U51	B,3								
C67	B,1	R77	A,1			U52	B,3								
C68	B,1	R78	A,1	TP13	A,1										
C69	B,1	R79	B,2	TP14	A,2	VR1	A,1								
C70	B,1	R80	B,2	TP15	B,1	VR6	A,2								
C71	B,1	R81	B,1	TP16	B,1	VR7	A,2								
C72	C,2	R84	B,1	TP17	B,2										
C73	C,2	R85	B,1	TP18	B,2										
C74	C,2	R86	B,1	TP19	B,2										
C75	B,1	R87	B,1	TP20	C,1										
C76	B,1	R88	B,1	TP21	C,1										
C77	B,2	R89	B,2	TP22	B,1										
C78	B,2	R90	B,1	TP28	B,1										
C81	B,2	R91	B,1												
C82	B,1	R92	B,1												
C83	B,2	R93	B,2												
C128	B,3	R94	C,1												
C140	B,1	R95	C,2												
		R96	B,2												
		R99	B,1												
		R100	B,1												
		R101	B,2												
		R102	B,2												

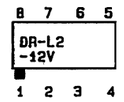
P/O A2 MODULATION MODULE **SS15**

SEE REVERSE SIDE

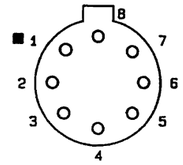
Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

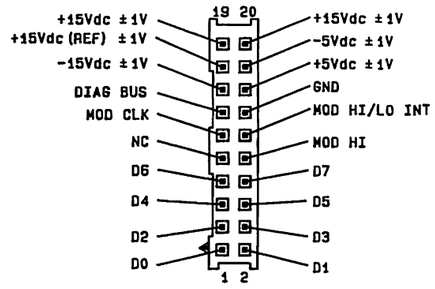
A2
K1-K6
TOP VIEW



A2
U29
TOP VIEW



A2J1
CABLE PLUG



Schematic General Information

CHANGES

All serial prefixes

On the Component Coordinates

- R66-75 - Add the following components;
  R66 B,3 R70 A,1 R74 A,1
  R67 B,3 R71 A,1 R75 A,1
  R68 A,2 R72 A,2
  R69 A,2 R73 A,2

On the schematic:

- To the right of **NORMAL/DOUBLED OUTPUT SELECT**, change "**45**" to "**43**" (next to bullet **FY**).
- To the left of **GENERAL DIAGNOSTICS INTERFACE**, change the bullet under "MUX 4" from "FY" to "FV".
- R68, R111 - In **AM/FM SELF TEST**, change the values of R68 and R111 to 1960.
- U51 - In **AM/FM SELF TEST**, change the connection for U51 pins 3 and 14 from +15V(F1) to +5V(F1).

2514A and above

On the schematic:

- Replace the appropriate portion of the schematic with the partial shown on 8J-108.3.
- In the upper left portion of the schematic, change the A2 part number to 08642-60223.

2714A and above

On the Component Locator:

- Use *Figure 8J-108 Component Locator* with *Figure 8J-108 Component Locator (2714A and above)* on page 8J-108.4.

In Schematic General Information:

- Add note 3; *TP13, 18, and 28 are test pads, not post types.*

On the Component Coordinates:

- Delete the following components;
  C57-60, R76-80, U1,2,4,14, and VR1,6,7.

On the schematic:

- In the upper left portion of the schematic, change the A2 part number to 08642-60323.
- Replace the schematic with the new SS16 foldout on page 8J-108.5.
- R68 - In **AM/FM SELF TEST**, locate R68 and change the value to 1.96k.

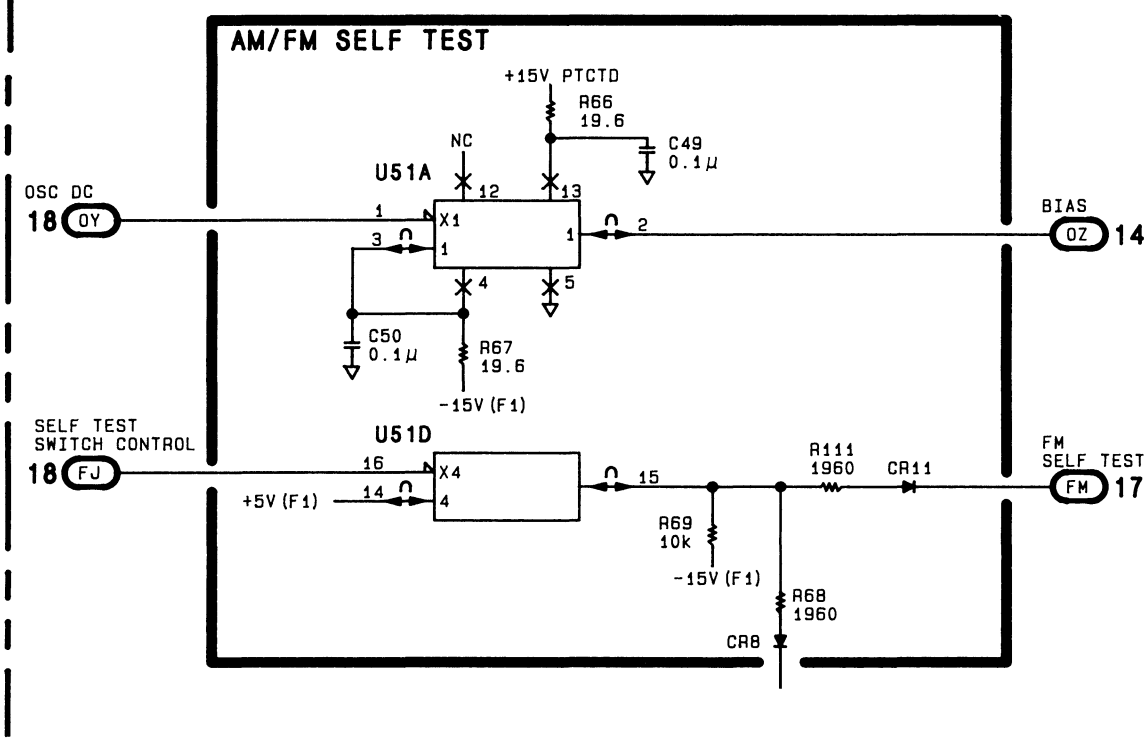
CHANGES

2727A and above

On the schematic:

- R195 - In **AM SUMMING AMPLIFIER,** change R195 to ZERO ohm.
- R196 - In **AM LEVEL ADJUST,** change R196 to ZERO ohm.

P/O A2 MODULATION MODULE (08642-60223)



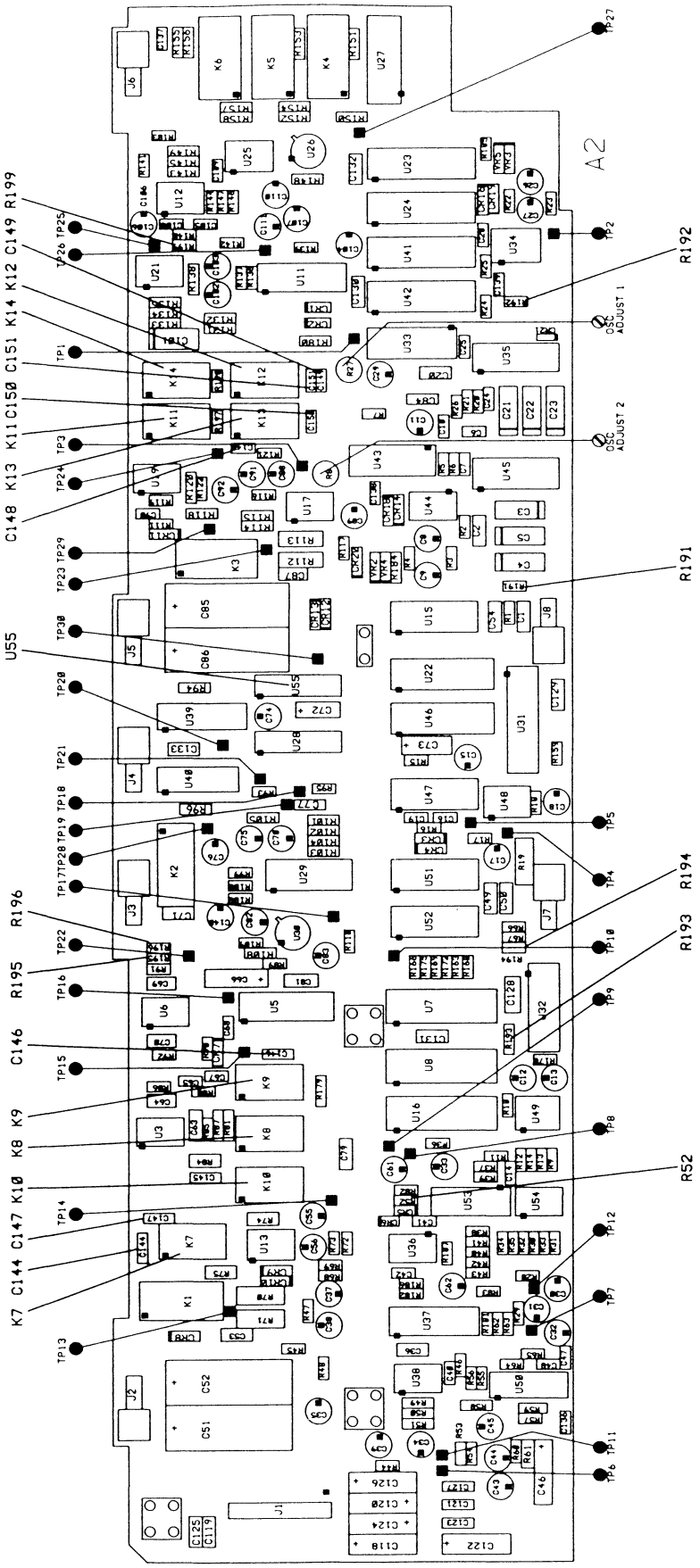


Figure 8J-108 Component Locator (2714A and above)

P/O A2 MODULATION MODULE (08642-60123)

OPTION 002

AM/ PULSE (FROM REAR PANEL) J6 W202 945

AM/ PULSE (FROM FRONT PANEL) J1 W18 945 J2

AM/FM SELF TEST

+15V PTCTD R66 19.6 C49 0.1µ

NC U51A 12 13

1 3 X1 1 1 2

4 5

C50 0.1µ R67 19.6 -15V (F1)

SELF TEST SWITCH CONTROL 18 FJ

U51D 16 X4 4 14 +15V (F1) 15

R111 1k CR11 FM SELF TEST FM 17

R69 10k -15V (F1)

R68 1k CR8

AM INPUT AC/DC COUPLER

AM AC/DC 18 FK 2

U15F AM AC 6 11

K1 +15V (F1) 7 2 TP13

C51 470µ C52 470µ 8 4 1 5

R71 600

U15E AM DC 5 12 6 3

C53 0.1µ

POWER SUPPLY AND GND

+15V PROTECTED 14 EP +15V PTCTD

POWER SUPPLY AND GND 14 FG 5

+15V (F1)
+5V (F1)
−15V (F1)
−5V (F1)

FET SWITCH REFERENCE

+5V (F1) R78 562

VR1 2.4V

AM LNA GAIN 18 FN

AF FL 17

AM LOW NOISE AMPLIFIER

+15V (F1) R72 215 C55 10µ

+5V (F1) CR9 R70 562 CR10 -5V (F1)

U13 3 7 6 2 4

R73 215 -15V (F1) C56 10µ

R74 5900

LNA GAIN SELECT +15V PTCTD R76 19.6 C57 0.1µ

NC U1 9 11

X1 X2 13 VREF

R75 1k

8 1 1 7 1 14 2 2 6 1 1 5 3 2 2 2

10 12

R77 19.6 -15V (F1) C58 0.1µ

INTERNAL AM SWITCH

+15V PTCTD R79 19.6 C59 0.1µ

INT/EXT AM 18 F0 2

INT AM U4 4 11 9 X1 X2 13 VREF

INT OSC 14, 17 EU R179 1k

8 1 1 7 14 2 2 1 6 1 1 5 2 2 2 3

10 12

R80 19.6 -15V (F1) C60 0.1µ

EXTERNAL AM SWITCH

NC U2 11 4 9 X1 X2 13 VREF

EXT AM

FET SWITCH PROTECT

VR6 8.2V VR7 8.2V TP14

8 1 1 7 14 2 2 1 6 1 1 5 2 2 2

10 12

HI/LO DETECTOR

HI/LO AM/FM SELECT 18 FP

NC U14 11 4 9 X1 X2 13 VREF

8 1 1 7 14 2 2 1 6 1 1 5 2 2 2

10 12

C81 1µ R108 162k

U30 3 2

R110 19.6 -15V

FM LNA 17 FQ

SERIAL PREFIX: 2427A

INTERNAL AM SWITCH

EXTERNAL AM SWITCH

FET SWITCH PROTECT

AM SUMMING AMPLIFIER

AM LEVEL ADJUST

LOW NOISE AMPLIFIER

LNA GAIN SELECT

HI/LO DETECTOR

WINDOW COMPARATOR

INT/EXT AM 18 FO

INT OSC 14, 17 EU

EXT AM

INT AM

AM DAC BITS 18 FR

+15V PTCTD

+15V (F1)

-15V (F1)

+5V (F1)

+15V (REF) 14, 15 EQ

HI/LO FM SELECT 18 FP

FM 17 LNA FQ

EXT CNT EZ 14

HI/LO RESET 18 FW

MUX SE 18 17 14 15

U1 U2 U3 U4 U5 U6 U13 U14 U28 U29C U29D U30 U39

U4 X1 X2 VREF

U5 [D/A CONV.] (CMOS)

AM DB0 AM DB1 AM DB2 AM DB3 AM DB4 AM DB5 AM DB6 AM DB7 AM DB8 AM DB9 AM DB10 AM DB11

[V REF±] [R FB]

[Io1] [Io2]

U6

U28 RX/CX CX

U39 S1 S2 S3 S4

R79 19.6

C59 0.1µ

R179 1k

R81 9k

R80 19.6

C60 0.1µ

R84 10k

R86 19.6

C64 0.1µ

R87 7.853k

R88 3160

C65 39p

R85 19.6

C63 0.1µ

TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21

VR6 8.2V VR7 8.2V

R89 19.6

C66 6.8 µ

R90 2370

C67 56p

CR7

R91 19.6

C69 0.1µ

R92 19.6

C70 0.1µ

C68 10p

R93 10k

R95 1k

C74 10 µ

R96 196k

C73 2.2 µ

R94 196k

C72 2.2 µ

R99 19.6

R188 19.6

C75 10 µ

C140 10 µ

R104 7.853k

R103 273.2

C78 10 µ

R100 19.6

C76 10 µ

R102 6750

R101 681k

C77 16p

R105 95

R109 19.6

C82 10 µ

C81 1µ

R108 162k

R110 19.6

C83 10 µ

R72 215

C55 10 µ

R73 215

C56 10 µ

CR9 CR10

R74 5900

R75 1k

R76 19.6

C57 0.1 µ

R77 19.6

C58 0.1 µ

AM DAC BITS
18 FR 12

AM LEVEL ADJUST

+15V PTCTD
R89 19.6
C66 6.8 µ

U5
AM DB0 15
AM DB1 14
AM DB2 13
AM DB3 12
AM DB4 11
AM DB5 10
AM DB6 9
AM DB7 8
AM DB8 7
AM DB9 6
AM DB10 5
AM DB11 4
[D/A CONV.] (CMOS)
A 0/4095
[Io1]
[Io2]
[V REF±]
[R FB]

TP16

+15V (F1)
R91 19.6
C69 0.1µ
U6
R92 19.6 -15V (F1)
C70 0.1µ
R90 2370
C67 56p
CR7
C68 10p

AM SUMMING AMPLIFIER
R87 7.853k
+15V (F1)
R86 19.6
C64 0.1µ
U3
R88 3160
C65 39p
R85 19.6 -15V (F1)
C63 0.1µ
TP15

NORMAL/DOUBLED OUTPUT SELECT
+15V (F1)
K2
U15D
DBL AM 3
U15C
NOR AM 4
NOR/DBL AM 18 FS 2
C71 0.1µ
J4
J3
W33
W22
AM OUT DOUBLED FX 49 (8642B ONLY)
AM OUT NORMAL FY 45

GENERAL DIAGNOSTICS INTERFACE
MUX SELECT LINES 18 FU 3
MUX 1 17 FT
MUX 2 14 FC
MUX 4 15 FY
MUX 5 14 FD
MUX 6 14 EX
R166 10k
R169 10k
R175 10k
R163 10k
R172 10k
R160 10k
+15V PTCTD
C128 0.1µ
U52
MUXDMUX
+5V (F1)
S0
S1
S2
EN
V+
V-
-15V (F1)
P/O J1
TP22
MODULATION DIAGNOSTIC BUS FZ 9

+15V (REF) 14, 15 EQ

WINDOW COMPARATOR
R105 95
TP17
+15V (F1)
R99 19.6
+5V (F1)
R188 19.6
C75 10 µ
U29C
C140 10 µ
TP18
R104 7.853k
C78 10 µ
R103 273.2
R100 19.6 -15V (F1)
C76 10 µ
TP19
U29D
R102 6750
R101 681k
C77 16p
+5V (F1)
R95 1k
U28
C74 10 µ
R96 196k
C73 2.2 µ
R94 196k
C72 2.2 µ
TP21
R93 10k
TP20
U39
U40D
U40C
U40B
TP28
ATTENTION Static Sensitive Devices
MOD HI/LO INT GA 9
MOD HI GB 9
P/O A5 DISTRIBUTION ASSY (08642-60126) SS56
EXT CNT EZ 14
HI/LO RESET 18 FW

SS16
Figure 8J-109
8J-109

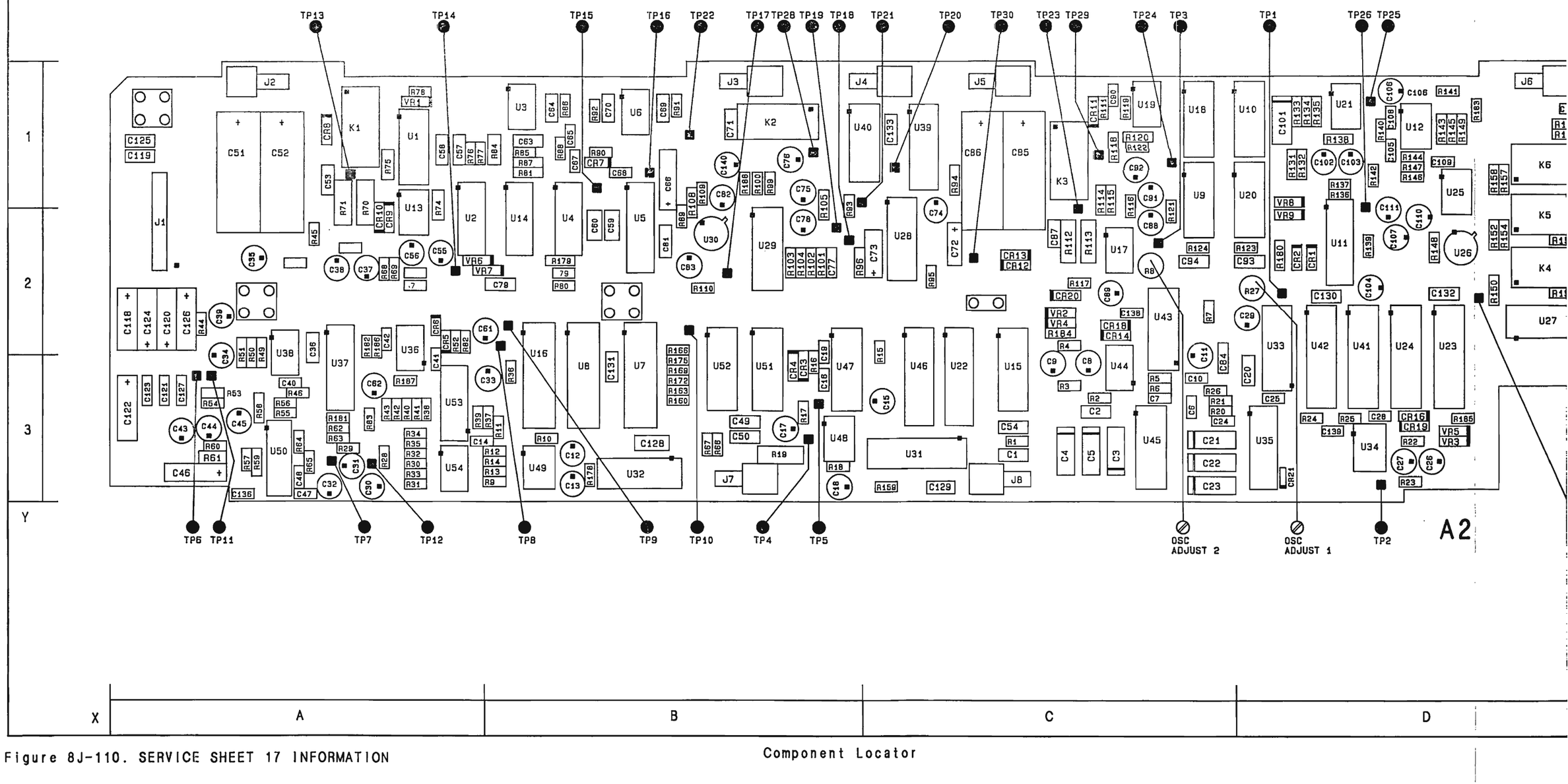
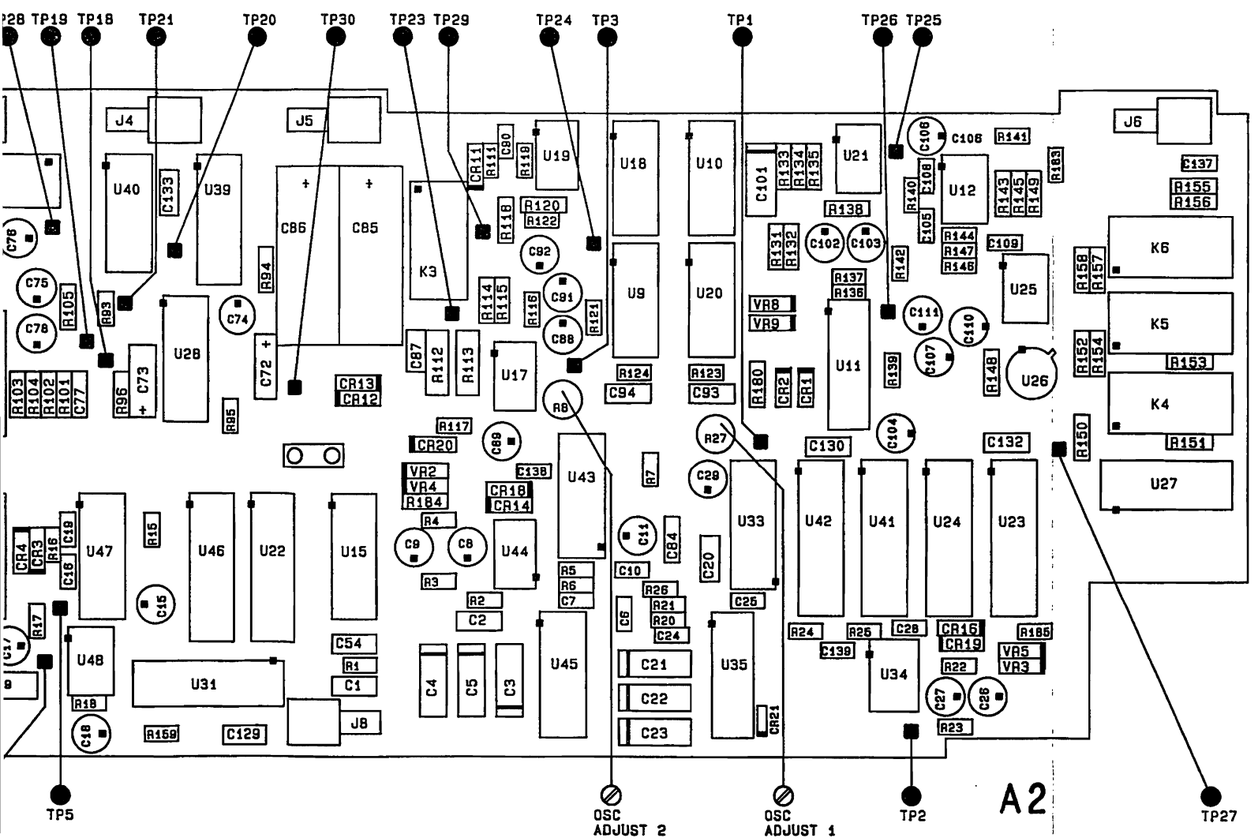
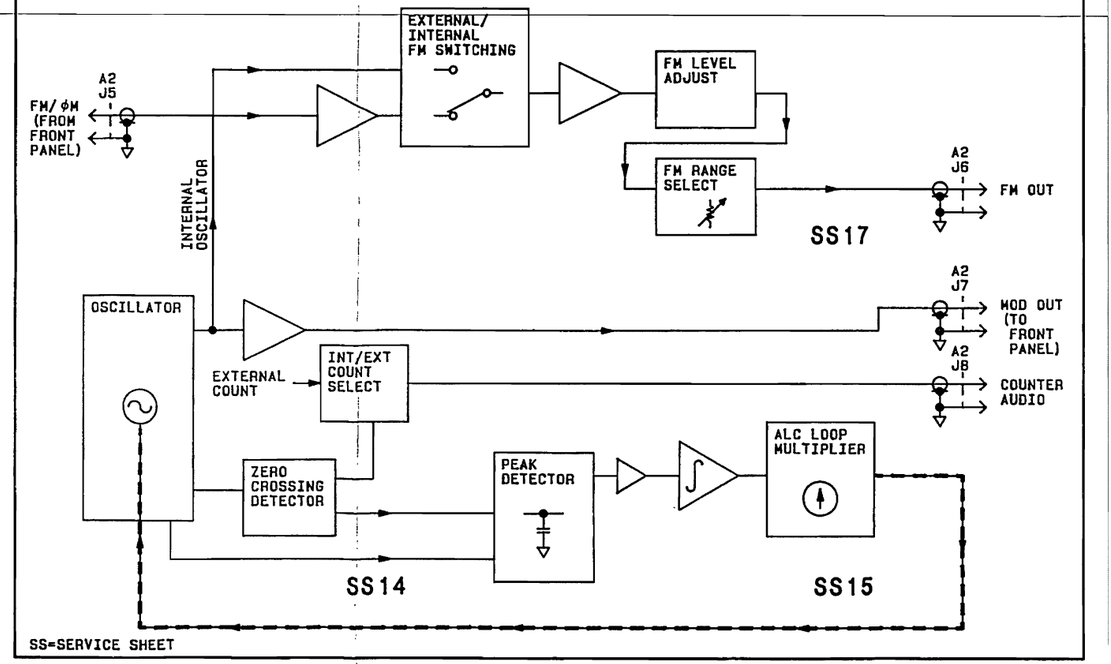


Figure 8J-110. SERVICE SHEET 17 INFORMATION

Component Locator





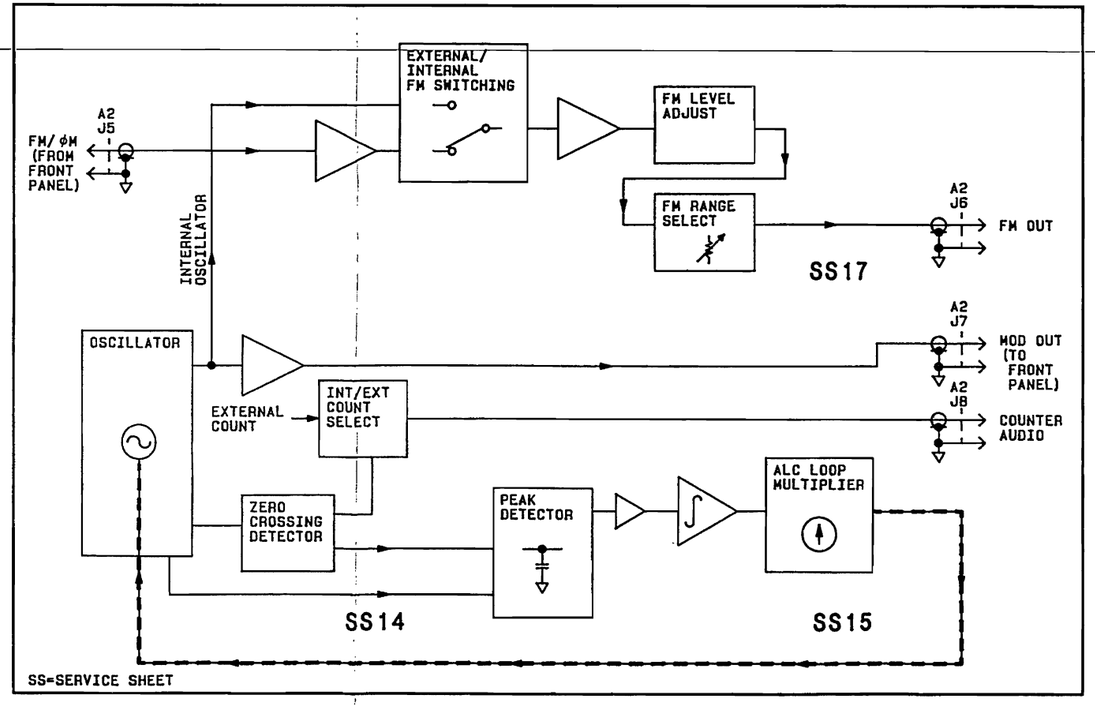
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y
C85	C, 1	R112	C, 2	R155	D, 1
C86	C, 1	R113	C, 2	R156	D, 1
C87	C, 2	R114	C, 1	R157	D, 1
C88	C, 2	R115	C, 1	R158	D, 1
C89	C, 2	R116	C, 2	R180	D, 2
C90	C, 1	R117	C, 2	R183	D, 1
C91	C, 1	R118	C, 1		
C92	C, 1	R119	C, 1	TP23	C, 2
C93	D, 2	R120	C, 1	TP24	C, 1
C94	C, 2	R121	C, 2	TP25	D, 1
C101	D, 1	R122	C, 1	TP26	D, 1
C102	D, 1	R123	D, 2	TP27	D, 2
C103	D, 1	R124	C, 2	TP29	C, 1
C104	D, 2	R131	D, 1		
C105	D, 1	R132	D, 1	U9	C, 1
C106	D, 1	R133	D, 1	U10	D, 1
C107	D, 2	R134	D, 1	U11	D, 2
C108	D, 1	R135	D, 1	U12	D, 1
C109	D, 1	R136	D, 1	U15	C, 3
C110	D, 2	R137	D, 1	U17	C, 2
C111	D, 2	R138	D, 1	U18	C, 1
C137	D, 1	R139	D, 2	U19	C, 1
		R140	D, 1	U20	D, 1
CR12	C, 2	R141	D, 1	U21	D, 1
CR13	C, 2	R142	D, 1	U25	D, 1
		R143	D, 1	U26	D, 2
J5	C, 1	R144	D, 1	U27	D, 2
J6	D, 1	R145	D, 1		
		R146	D, 1	VR8	D, 1
K3	C, 1	R147	D, 1	VR9	D, 2
K4	D, 2	R148	D, 2		
K5	D, 2	R149	D, 1		
K6	D, 1	R150	D, 2		
		R151	D, 2		
		R152	D, 2		
		R153	D, 2		
		R154	D, 2		

P/O A2 MODULATION MODULE **SS16**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

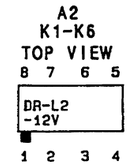
COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C85	C, 1	R112	C, 2	R155	D, 1										
C86	C, 1	R113	C, 2	R156	D, 1										
C87	C, 2	R114	C, 1	R157	D, 1										
C88	C, 2	R115	C, 1	R158	D, 1										
C89	C, 2	R116	C, 2	R180	D, 2										
C90	C, 1	R117	C, 2	R183	D, 1										
C91	C, 1	R118	C, 1												
C92	C, 1	R119	C, 1	TP23	C, 2										
C93	D, 2	R120	C, 1	TP24	C, 1										
C94	C, 2	R121	C, 2	TP25	D, 1										
C101	D, 1	R122	C, 1	TP26	D, 1										
C102	D, 1	R123	D, 2	TP27	D, 2										
C103	D, 1	R124	C, 2	TP29	C, 1										
C104	D, 2	R131	D, 1												
C105	D, 1	R132	D, 1	U9	C, 1										
C106	D, 1	R133	D, 1	U10	D, 1										
C107	D, 2	R134	D, 1	U11	D, 2										
C108	D, 1	R135	D, 1	U12	D, 1										
C109	D, 1	R136	D, 1	U15	C, 3										
C110	D, 2	R137	D, 1	U17	C, 2										
C111	D, 2	R138	D, 1	U18	C, 1										
C137	D, 1	R139	D, 2	U19	C, 1										
		R140	D, 1	U20	D, 1										
CR12	C, 2	R141	D, 1	U21	D, 1										
CR13	C, 2	R142	D, 1	U25	D, 1										
		R143	D, 1	U26	D, 2										
J5	C, 1	R144	D, 1	U27	D, 2										
J6	D, 1	R145	D, 1												
		R146	D, 1	VR8	D, 1										
K3	C, 1	R147	D, 1	VR9	D, 2										
K4	D, 2	R148	D, 2												
K5	D, 2	R149	D, 1												
K6	D, 1	R150	D, 2												
		R151	D, 2												
		R152	D, 2												
		R153	D, 2												
		R154	D, 2												

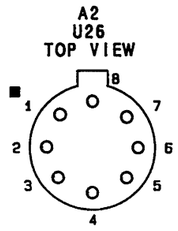
P/O A2 MODULATION MODULE **SS16**

SEE REVERSE SIDE

Notes:

1. Each module in the HP 8642 has a nine digit module indentification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. ⏚1 is a common connect point to circuitry shown in FM range select. It is connected to the outer conductor of J6.
3. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.





Schematic General Information

CHANGES

2514 and above

On the schematic:

- In the upper left portion of the schematic, change the A2 part number to 08642-60223.

2714A and above

On the Component Locator:

- Replace *Figure 8J-110 Component Locator* with the new *Figure 8J-110 Component Locator* on page 8J-110.3.

On the Component Coordinates:

- Delete the following components;
  C93-94, R123-124, U9,10, U18,20, VR8 and VR9.

In Schematic General Information:

- Add note 3; *"TP23 and TP29 are test pads, not the post type.*

On the schematic:

- In the upper left portion of the schematic, change the A2 part number to 08642-60323.
- Replace the schematic with the new SS17 foldout on page 8J-110.4. In **FM LEVEL ADJUST** locate U12 and add R199 5.11k from pin 3 to ground.

2727A and above

On the schematic:

- R197 - In **FM UNITY GAIN AMP,** change R197 to ZERO ohm.
- R198 - In **FM SUMMING AMPLIFIER,** change R198 to ZERO ohm.
- R199 - In **FM LEVEL ADJUST,** change R199 to ZERO ohm.

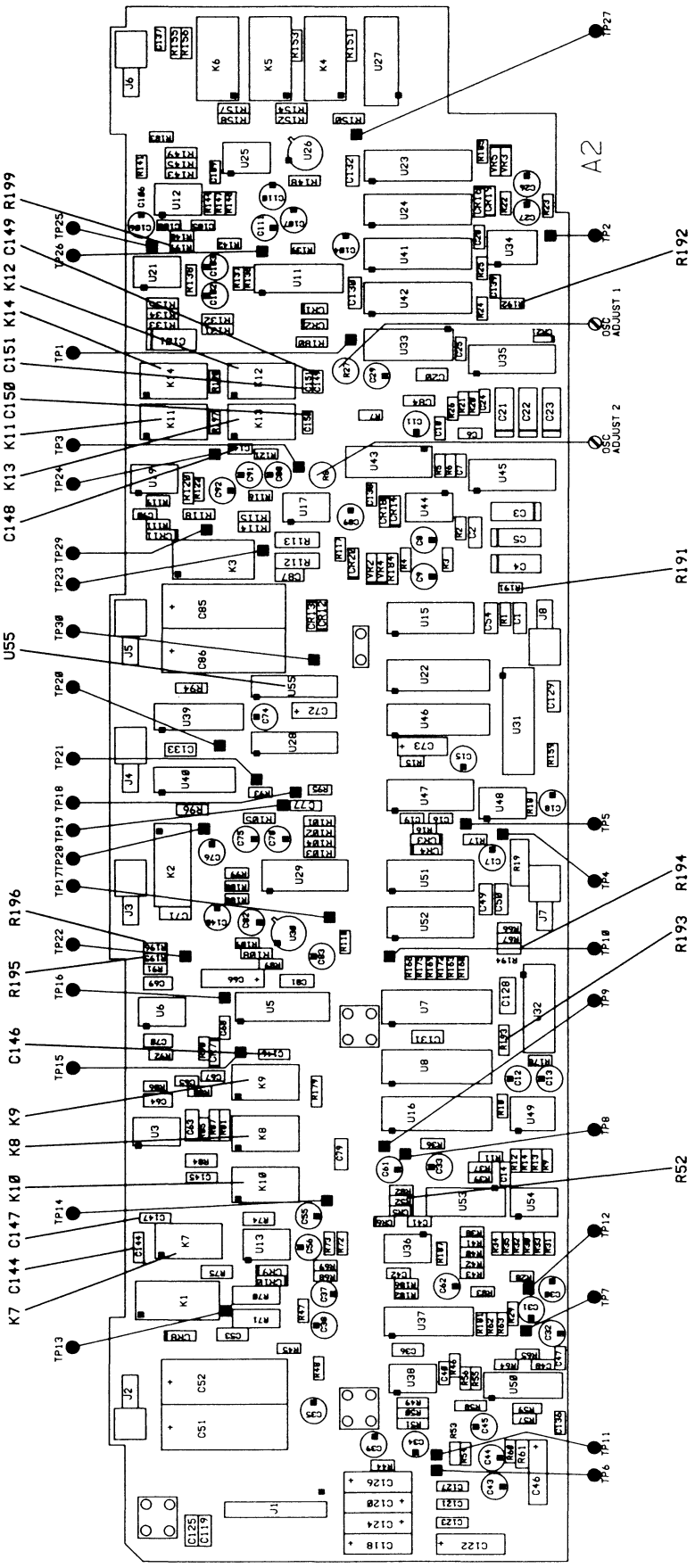


Figure 8J-110. Component Locator (2714A and above)

P/O A2 MODULATION MODULE (08642-60123)

OPTION 002

FM/ϕM (FROM REAR PANEL) J9 W201 98

FM/ϕM (FROM FRONT PANEL) J2 W19 98 J5

FM SELF TEST 16 FM

FM AC/DC 18 GD 2

FM INPUT AC/DC COUPLER

U15B FM AC 2 15

U15A FM DC 1 16 8 +15V (F1) 9

K3 +15V (F1) 7 2 8 4 1 6 3 5

C85 470 µ C86 470 µ

C87 0.1µ

TP23

R112 600

FM LOW NOISE AMPLIFIER

+5V (F1) CR12

R113 562

CR13 -5V (F1)

U17 3 7 2 4 6

+15V (F1) R116 215 C88 10µ

R117 215 C89 10µ -15V (F1)

TP29

R114 1k

R115 5900

VR8 8.2V

VR9 8.2V

FM ± UNITY GAIN AMP

R120 10k

R118 10k

R119 3480

C90 36p

U19 2 7 3 4 6

+15V (F1) R121 19.6 C91 10µ

R122 19.6 C92 10µ -15V (F1)

TP24

+15V PTCTD R123 19.6

U18 NC 4 11 9 X1 X2 13 VREF 10 12

C93 0.1µ

C94 0.1µ

R124 19.6 -15V (F1)

FM INV HI 18 GE

AF 16 FL

INT/EXT FM 18 GN 2

INT OSC 14, 16 EU

FM LNA FQ 16

EXT FM W/PRE 18 GF

POWER SUPPLY AND GND

+15V PROTECTED 14 EP → +15V PTCTD

POWER SUPPLY AND GND 14 FG 5 → +15V (F1), +5V (F1), -15V (F1), -5V (F1)

SERIAL PREFIX: 2427A

INTERNAL FM SWITCH

INT/EXT FM 18 GN

INT FM

INT OSC 14, 16 EU

FM INV HI 18 GE

AF 16 FL

R160 1k

R131 9k

U20 NC

EXTERNAL FM SWITCH

EXT FM

R132 10k

U9 NC

M ± UNITY GAIN AMP

+15V PTCTD

R123 19.6

C93 0.1µ

U18 NC

+15V (F1)

R120 10k

R121 19.6

C91 10µ

TP24

U19

R118 10k

R119 3480

C90 36p

R122 19.6 -15V (F1)

C92 10µ

C94 0.1µ

R124 19.6 -15V (F1)

PRE-EMPHASIS

R135 2.429k

C101 2200p

R134 306k

R133 35k

U10 NC

EXT FM W/PRE 18 GF

FM SUMMING AMPLIFIER

+15V (F1)

R138 7.853k

R137 19.6

C103 10µ

U21

R136 19.6 -15V (F1)

C102 10µ

TP25

FM DAC BITS 18 GH 10

FM LEVEL ADJUST

+15V PTCTD

R139 19.6

C104 10µ

U11 [D/A CONV.] (CMOS)

FM DB0 13

FM DB1 12

FM DB2 11

FM DB3 10

FM DB4 9

FM DB5 8

FM DB6 7

FM DB7 6

FM DB8 5

FM DB9 4

[V REF±] 15

[R FB] 16

A 0/1023

[Io1] 1

[Io2] 2

R140 2370

C105 56p

C108 10p

+15V (F1)

R141 19.6

C106 10µ

U12

TP26

R142 19.6 -15V (F1)

C107 10µ

MUX 1 FT 16

FM RANGE SELECT

FM OUTPUT DRIVE

36 dB ATTENUATOR

18 dB A

TP27

R143 10k

R148 10k

+15V (F1)

R146 10

C110 10µ

U25

U26

R144 3160

C109 39p

R147 10 -15V (F1)

C111 10µ

R145 50

R149 50

1 (NOTE 2)

R150 50

R151 3.056k

K4

+15V (F1)

U27F

36 dB OUT

R152 50

1 (NOTE 2)

36 dB IN

U27A

U27E

18 dB OUT

R154 54.47

1 (NOTE)

U27B

18 dB IN

ATT RELAY CONTROL 18 GG 6

AL FM SWITCH

U20 NC

R131 9k

AL FM SWITCH

U9

R132 10k

PRE-EMPHASIS

U10

R135 2.429k

C101 2200p

R134 306k

R133 35k

FM DAC BITS 18 GH 10

FM LEVEL ADJUST

+15V PTCTD

R139 19.6

C104 10 µ

U11 [D/A CONV.] (CMOS)

FM DB0 13
FM DB1 12
FM DB2 11
FM DB3 10
FM DB4 9
FM DB5 8
FM DB6 7
FM DB7 6
FM DB8 5
FM DB9 4
15 [V REF±]
16 [R FB]

A 0/1023

[Io1] 1
[Io2] 2

R140 2370

C105 56p

C108 10p

+15V (F1)

R141 19.6

C106 10 µ

TP26

U12

R142 19.6 -15V (F1)

C107 10 µ

FM SUMMING AMPLIFIER

+15V (F1) R138 7.853k

R137 19.6

C103 10 µ

U21

R136 19.6 -15V (F1)

C102 10 µ

TP25

MUX 1 FT 16

FM RANGE SELECT

FM OUTPUT DRIVE

TP27

R143 10k

R148 10k

+15V (F1)

R146 10

C110 10 µ

U25

U26

R144 3160

C109 39p

R147 10 -15V (F1)

C111 10 µ

R145 50

R149 50

1 (NOTE 2)

R150 50

36 dB ATTENUATOR

R151 3.056k

K4 +15V (F1)

U27F

36 dB OUT 7 10

R152 50

1 (NOTE 2)

36 dB IN 2

U27A 1, 16

18 dB ATTENUATOR

R153 350

K5 +15V (F1)

U27E

18 dB OUT 6 11

R154 54.47

1 (NOTE)

18 dB IN 3

U27B 14

9 dB ATTENUATOR

R156 50

R155 40

K6 +15V (F1)

U27D

9 dB OUT 5 12

R158 46.5

R157 31.62

1 (NOTE)

9 dB IN 4

U27C 13

J6

1 (NOTE 2)

W20 FM OUT 967 GI 24

C137 1000p

ATT RELAY CONTROL 18 GG 6

ATTENTION
Static Sensitive
Devices

SS17
Figure 8J-111
8J-111

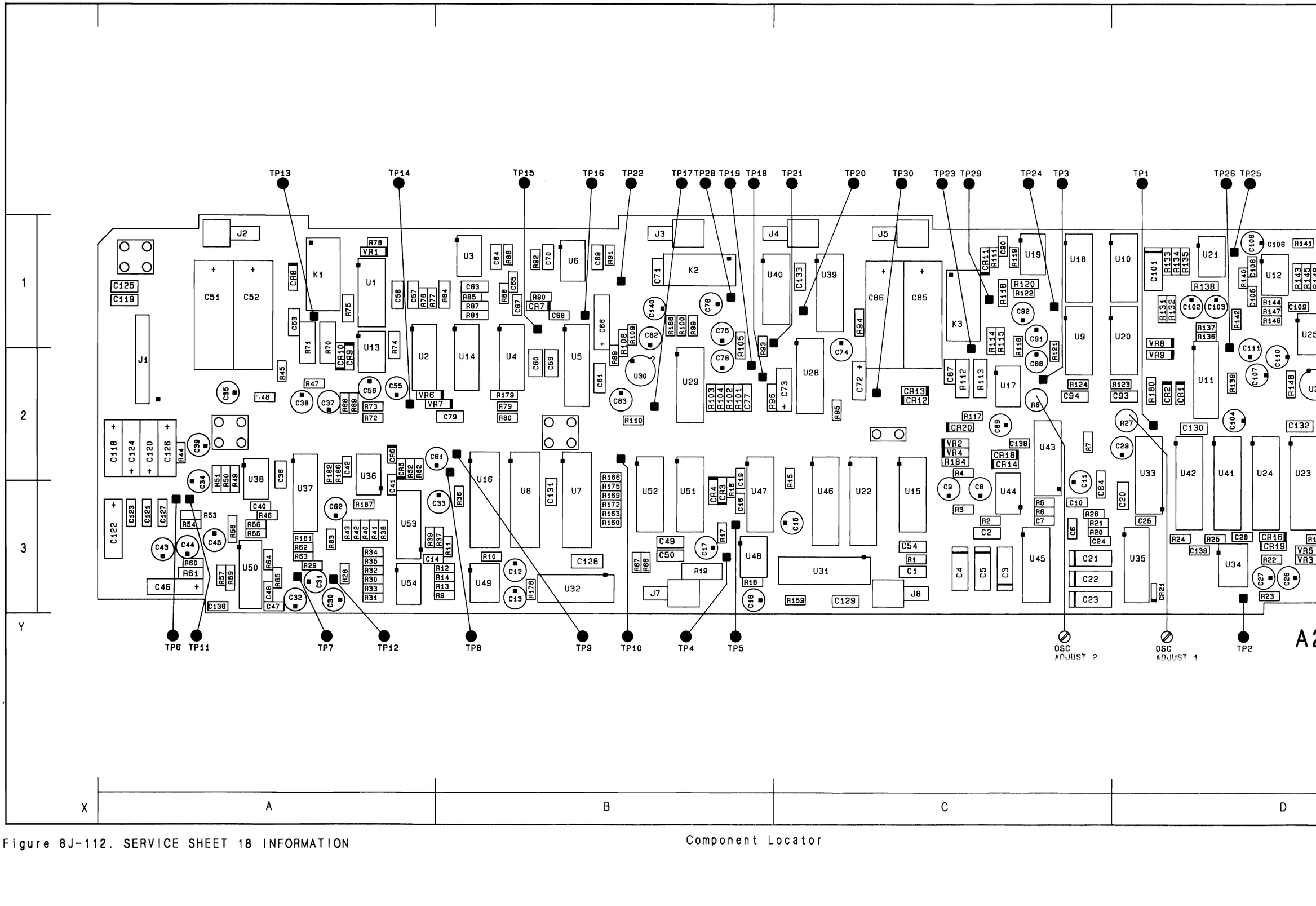
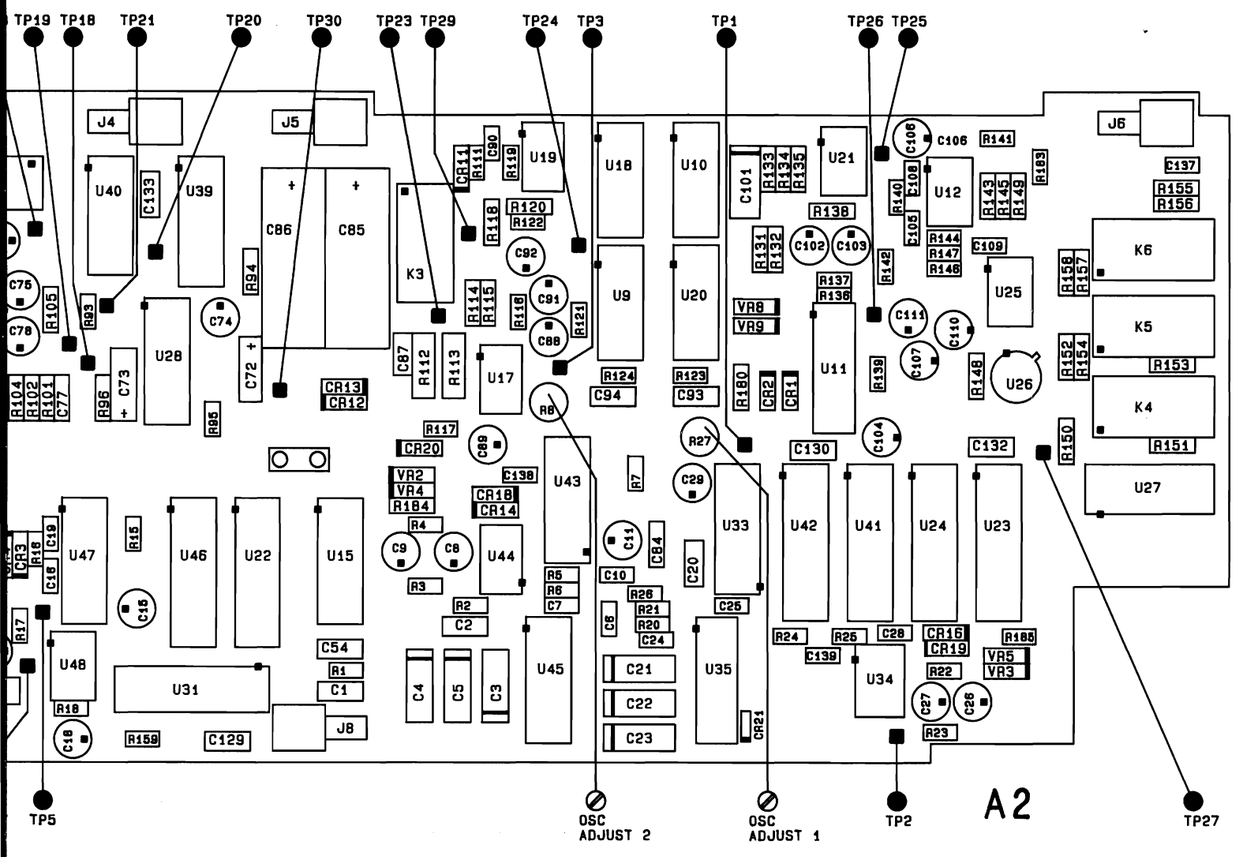
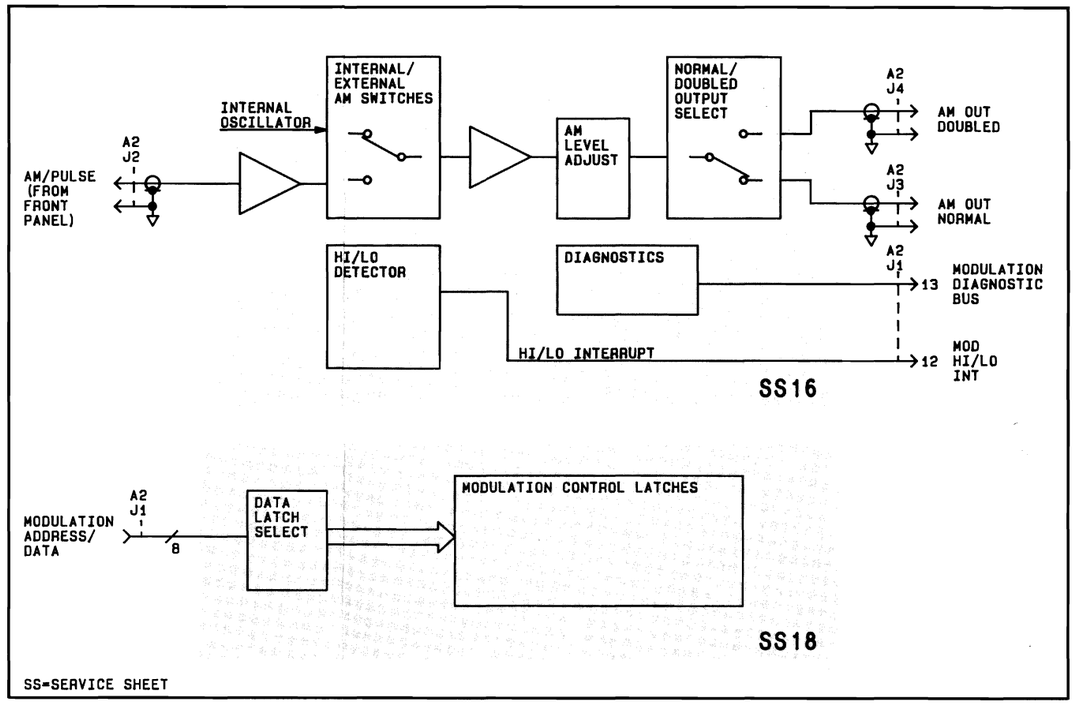


Figure 8J-112. SERVICE SHEET 18 INFORMATION

Component Locator



oonent Locator



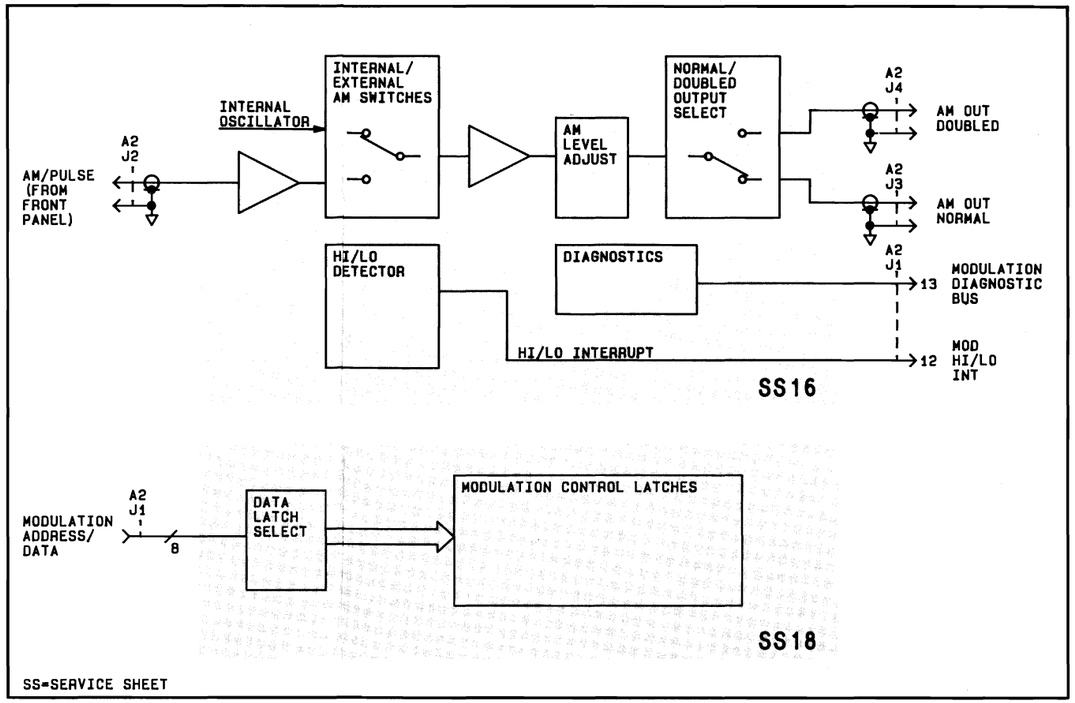
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C54	C, 3														
C79	B, 2														
C129	C, 3														
C130	D, 2														
C131	B, 3														
C132	D, 2														
C133	C, 1														
J1	A, 2														
R178	B, 3														
U7	B, 3														
U8	B, 3														
U16	B, 3														
U22	C, 3														
U23	D, 2														
U24	D, 2														
U31	C, 3														
U32	B, 3														
U40	C, 1														
U41	D, 2														
U42	D, 2														
U46	C, 3														

P/O A2 MODULATION MODULE **SS17**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C54	C, 3																
C79	B, 2																
C129	C, 3																
C130	D, 2																
C131	B, 3																
C132	D, 2																
C133	C, 1																
J1	A, 2																
R178	B, 3																
U7	B, 3																
U8	B, 3																
U16	B, 3																
U22	C, 3																
U23	D, 2																
U24	D, 2																
U31	C, 3																
U32	B, 3																
U40	C, 1																
U41	D, 2																
U42	D, 2																
U46	C, 3																

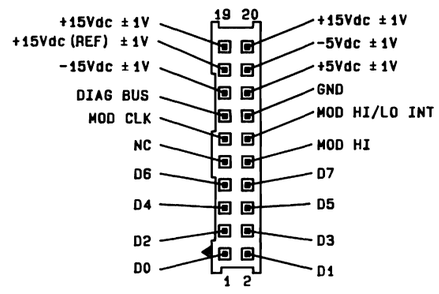
P/O A2 MODULATION MODULE **SS17**

SEE REVERSE SIDE

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

A2J1
CABLE PLUG



CHANGES

All Serial Prefixes

On the schematic:

- To the left of **POWER SUPPLY AND GND,** change the bullet under "POWER SUPPLY AND GND" from "SX" to "FG".

2432A to 2513A

On the schematic:

- U32 - In **DATA LATCH SELECT,** delete bullet "OY" (OSC DC) from U32 pin 15 and label the line "NC" (no connect).

2514A and above

On the schematic:

- U32 - To the right of **DATA LATCH SELECT**, change U32 pin 15 to bullet "OY", (OSC DC), service sheet 16.
- In the upper left portion of the schematic, change the A2 part number to 08642-60223.

2714A and above

On the Component Locator:

- Replace *Figure 8J-112 Component Locator* with the new *Figure 8J-112 Component Locator* on page 8J-112.3.

On the schematic:

- In the upper left portion of the schematic, change the A2 part number to 08642-60323.

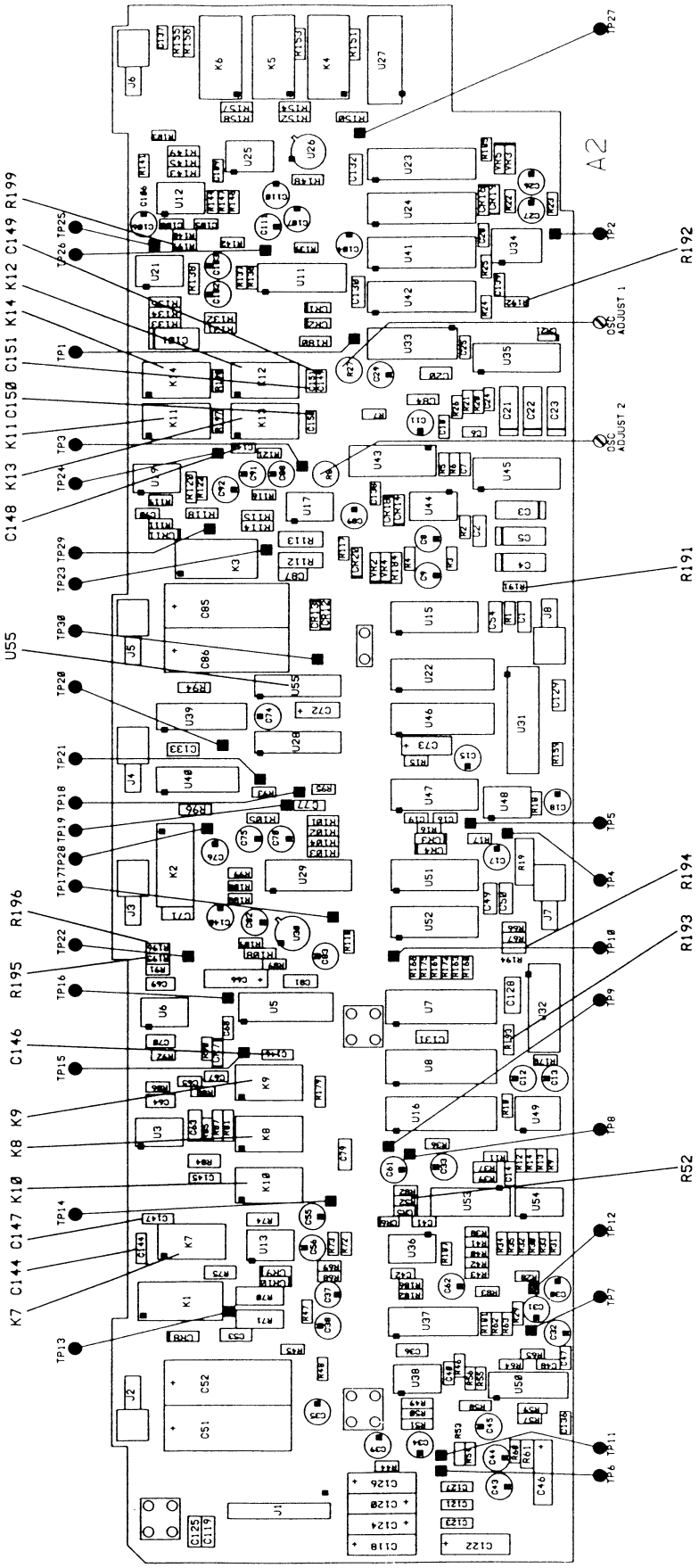


Figure 8J-112 Component Locator (2714A and above)

P/O A2 MODULATION MODULE (08642-60123)

DATA LATCH SELECT

ADDRESS HOLDING LATCH

MODULATION CLK 11 GJ

MODULATION ADDRESS/ DATA LINES 11 GK 8

P/O A5 DISTRIBUTION ASSY SS56

P/O J1

MOD D3, MOD D1, MOD D4, MOD D2, MOD D5, MOD D6, MOD D7, MOD D0

U31 +5V (F1) C129 0.1µ

U32 BIN/OCT +5V (F1) R178 1k

EN 1, EN 2, EN 3, EN 4, EN 5, EN 6, EN 7, EN 8, EN 9, EXT, INT, NC

OSC DC OY 14

CNT INT/EXT EY 14

MODULATION CONTROL LATCHES

U42 +5V (F1)

MOD D2, MOD D0, MOD D1, MOD D7, MOD D6, MOD D3, MOD D5, MOD D4

OSC DB2, OSC DB0, OSC DB1, OSC DB7, OSC DB6, OSC DB3, OSC DB5, OSC DB4

U41 +5V (F1)

MOD D2, MOD D5, MOD D3, MOD D0, MOD D1, MOD D7, MOD D6, MOD D4

+5V (F1) C133 0.1µ U40A

U7 +5V (F1) C131 0.1µ

MOD D6, MOD D7, MOD D0, MOD D1, MOD D2, MOD D3, MOD D4, MOD D5

AM DB6, AM DB7, AM DB0, AM DB1, AM DB2, AM DB3, AM DB4, AM DB5

U8

MOD D6, MOD D7, MOD D5, MOD D4, MOD D3, MOD D2, MOD D1, MOD D0

POWER SUPPLY AND GND

POWER SUPPLY AND GND 14 SX

+5V (F1)

SERIAL PREFIX: 2427A

AM AC/DC 2 FK 16
OSC DAC BITS 10 ES 14
OSC FET BITS 4 ER 14

EN 1
+5V (F1)
C54 0.1µ
U46 20
1 G1
11 1C2
1 2D

MOD D0 3 — 2 DAC 0
MOD D7 4 — 5 DAC 7
MOD D6 7 — 6 DAC 6
MOD D5 8 — 9 DAC 5
MOD D4 13 — 12 DAC 4
MOD D3 14 — 15 DAC 3
MOD D2 17 — 16 DAC 2
MOD D1 18 — 19 DAC 1

10

C130 0.1µ
DC
OSC FB1
AC
OSC DB8
2 OSC DB9
5 OSC FB3
6 OSC FB2
9 OSC FB0

+5V (F1)
U22 20
1 G1
11 1C2
1 2D

MOD D0 3 — 2 DAC 8
MOD D7 4 — 5
MOD D6 7 — 6
MOD D5 8 — 9 S2
MOD D4 13 — 12 S1
MOD D3 14 — 15 S0
MOD D2 17 — 16 NC
MOD D1 18 — 19 DAC 9

10

MOD OUT DAC 10 EW 14
AM LNA GAIN FN 16
SELF TEST SWITCH CONTROL FJ 16
MUX SELECT LINES 3 FU 16

ATTENTION
Static Sensitive
Devices

EN 7
+5V (F1)
C79 0.1µ
U16 20
1 G1
11 1C2
1 2D

MOD D0 3 — 2 NOR AM
MOD D1 4 — 5 DBL AM
MOD D2 7 — 6 FM DC
MOD D3 8 — 9 FM AC
MOD D4 13 — 12 INT FM
MOD D5 14 — 15 EXT FM
MOD D7 17 — 16
MOD D6 18 — 19

10

5V (F1) 20
2
2
5
6 INT AM
9 EXT AM
12 AM DB11
15 AM DB10
16 AM DB9
19 AM DB8
10

EN 8
EN 9
+5V (F1)
C132 0.1µ
U24 20
1 G1
11 1C2
1 2D

MOD D5 3 — 2 FM DB5
MOD D4 4 — 5 FM DB4
MOD D6 7 — 6 FM DB6
MOD D3 8 — 9 FM DB3
MOD D7 13 — 12 FM DB7
MOD D2 14 — 15 FM DB2
MOD D1 17 — 16 FM DB1
MOD D0 18 — 19 FM DB0

10

+5V (F1)
U23 20
1 G1
11 1C2
1 2D

MOD D5 3 — 2 18dB IN
MOD D4 4 — 5 18dB OUT
MOD D6 7 — 6 36 dB OUT
MOD D3 8 — 9 9 dB IN
MOD D7 13 — 12 36 dB IN
MOD D2 14 — 15 9 dB OUT
MOD D1 17 — 16 FM DB9
MOD D0 18 — 19 FM DB8

10

ATT RELAY CONTROL 6 GG 17
NOR/DBL AM FS 16
FM AC/DC GD 17
INT/EXT FM GN 17
FM INV HI GE 17
EXT FM W/PRE GF 17
HI/LO RESET FW 16
HI/LO AM/FM SELECT FP 16
INT/EXT AM 2 FO 16
AM DAC BITS 12 FR 16
FM DAC BITS 10 GH 17

SS18
Figure 8J-113
8J-113

A6 Module

Troubleshooting and Adjustments Contents

Troubleshooting

Adjustments

Troubleshooting

A6 TROUBLESHOOTING INFORMATION

Before Proceeding With Module Troubleshooting

- You should have confidence that A6 is the faulty module from Module Level Diagnostics (MLD) results. (Refer to Instrument Level Troubleshooting, HP 8642 Service Manual.)
- Open the HP 8642 manual to Figure 8K-100. There are 3 diagrams of A6A2 (the A6 Module Counter/Timebase). Now, open the HP 8642 manual to the foldout on page 8K-102. There are 3 diagrams of A6A1 (the A6 Module FM Loop). One diagram is titled Simplified Block Diagram. It is a block diagram intended to be used to understand the basic operation of A6A1.
- Open the foldout on page 8K-101 (BD7). There, you will see a more detailed Block Diagram of the Counter/Timebase. **This Troubleshooting Block Diagram is meant to be used during Checks 1 and 2. The Troubleshooting Block Diagram on the next foldout (BD8) is meant to be used during Checks 3 and 4.**
- The objective of Troubleshooting Checks is to isolate the malfunction to an area of circuitry represented on one Service Sheet. The Checks are intended to be done in the order they are numbered.

NOTE

After the A6 module is repaired and adjusted, the A6A2 Auto-Adjustments must be performed to generate new module calibration date. Refer to Section 5 before proceeding with the A6A2 Auto-Adjustments procedures.

- Once the malfunction is isolated, refer to the Component Level Repair Directory. There, you will find tables that contain information useful for locating faulty components.
- Specification failures (for example, phase noise, spurs, etc.) might not be found by Troubleshooting Checks. Manual Adjustments and Auto Adjust Procedures can be done, and the HP 8642 then re-tested to see if the specific failure condition still exists. At this point, if repair is necessary, Module Performance Checks may be helpful to pinpoint a failure condition in the module. (Consult Service Notes and/or Hewlett-Packard if needed.)

Overall Equipment List

Signal Generator No. 1	HP 8642A/B
Signal Generator No. 2	HP 8642A/B
Oscilloscope	HP 1980B
Digital Voltmeter (DVM)	HP 3456A
Measuring Receiver	HP 8902A
Spectrum Analyzer	HP 8566A/B
HP 8642 Bench Service Kit	HP 11802A
Sensor Module	HP 11722A
Step Attenuator	HP 355D
HP-IB Printer	HP 82906A
Audio Analyzer	HP 8903A
Pulse/Function Generator	HP 8116A

Essentials of A6 Module Operation

The A6 module consists of two assemblies, A6A1 and A6A2. The first assembly shown is the Counter/Timebase. Refer to the Simplified Block Diagram on page 8K-100 for the following discussion of A6A2.

The A6A2 assembly consists of the Counter and the Timebase. They are two independent circuits.

The Timebase is shown on SS21 and SS22. There is an input port, A6A2 J7, that allows an external reference signal to be used to phase lock the internal 45 MHz VCO. When no external reference is present, the oscillator is mechanically tuned to 45 MHz. The 45 MHz signal is buffered, divided, and output to several other modules to serve as reference signals. There is also a 10 MHz output to the rear panel that comes directly from the Timebase.

The Counter is shown on SS19 and SS20. There are three inputs to the Counter.

- The FM Loop 135 MHz is a signal from A6A1, the FM Loop. It is divided down to 125 kHz and returned to A6A1. It is also further divided to 10 Hz and is used by the Counter as a Count Period. The Count Period is a time period during which the Counters shift registers load the signal being counted (Counted Signal).
- The 250 kHz TTL reference signal is a signal from the FM Loop that is also divided down to 10 Hz to be used as a Count Period.
- The Counter Audio is an audio frequency signal that comes from the Modulation (A2) module. It can be used as a Count Period, or as the Counted Signal.

There is one other signal that can be switched in as the Counted Signal. It is the Counter 45 MHz, and it comes directly from the Timebase by way of a circuit trace.

For a further discussion of Counter operation, see Check 5 and Check 6 Essentials of Operation.

Refer to the Simplified Block Diagram on page 8K-102 for the following discussion of A6A1.

The A6A1 assembly consists of the FM VCO Assembly. It is a phase locked loop, locked to the Timebase by the 500 kHz FM Reference. Frequency and Phase (angle) modulation (internal or external) comes from the Modulation Module (A2) on the line labeled FM. It is directed through crossover and shaping circuitry and applied to the loop integrator or the loop VCO. There is also a highly stable DCFM Reference voltage that is applied to the loop VCO when the HP 8642 is in DCFM mode.

The output of the FM VCO Assembly is a 135 MHz signal, carrying angle modulation. It is called the FM Loop Output, and goes to the Reference Loop Module (A11).

CHECK 1: A6A2 TIMEBASE CIRCUITRY (SS21)

Essentials of SS21 Circuit Operation

Refer to BD7. Located on SS21 you will find part of the phase locked loop circuitry for the Timebase. There is an input port for connecting an external reference signal from the instrument's rear panel, A6A2 J7 (AP) . The external reference must be 1, 2, 5, or 10 MHz. It is converted to TTL levels and divided by 2 in the **COMPARATOR**. The output of the **COMPARATOR** is directed to the **PULSE GENERATOR** where each TTL rising edge is converted to a negative pulse. These pulses have a duration of ≈7 to 10 ns. The **PULSE GENERATOR** output is compared with the loop VCO output (heavy dashed line) in the **PHASE DETECTOR**. The error signal is integrated and filtered before becoming the loop Tune Voltage.

When no external reference is applied, the Tune Voltage is set by a manual adjustment in the **LOW-PASS FILTER** that tunes the VCO to 45 MHz.

The **EXTERNAL REFERENCE DETECTOR** is used by the instrument's microprocessor to detect when an external reference is being used. The **TIMEBASE DIAGNOSTICS** provide out-of-lock sense information to the instrument's microprocessor.

Description of Check 1

The instrument's Counter and Timebase phase locked loop are both located on the A6A2 assembly (see Module Test Point/Adjustment Locations on page 8K-100).

This check tests part of the phase locked loop circuitry for the Timebase. It is intended to identify failures that would lead you to SS21 for component repair. First, you will test the **POWER SUPPLY** lines. Then, you will inject signals at the External Reference input port of A6A2 and the input to the phase detector, and verify the output waveform to identify **COMPARATOR**, **PHASE DETECTOR**, or **INTEGRATOR** failures.

The **EXTERNAL REFERENCE DETECTOR** and **TIMEBASE DIAGNOSTICS** circuitry is also tested.

If a test fails, refer to the Component Level Repair Directory. (Found at the end of these procedures after Check 6.)

Required Equipment:

Signal Generator No. 1	HP 8642A/B
Signal Generator No. 2	HP 8642A/B
Oscilloscope	HP 1980B
Digital Voltmeter (DVM)	HP 3456A

Test the A6 Power Supply and Ground

1. Setup:

   Switch the HP 8642 to standby (STBY).

   Extend A6 module on extender posts (refer to the Disassembly Procedure if you are not familiar with this procedure).

   Remove the A6A2 cover (see the Assembly Locator on the foldout opposite BD7 for location of A6A2 cover).

   Switch the HP 8642 on.

2. Measure Voltage Levels:

   Check the **POWER SUPPLY AND GND** line voltages at the inductors given in Table 8K-1. (Inductor locations can be found on page 8K-108, and measurements can be made on either side of inductor.)

Table 8K-1. *A6 Power Supply Lines*

Inductor	Nominal Voltage
L23	+15Vdc
L12	+5Vdc
L24	−15Vdc
L25	−15Vdc

Test the Phase Detector Input (from SS22)

3. Setup:

   Switch the HP 8642 to Standby.

   Connect the Oscilloscope to the junction of CR2 and CR3 (AS) .

4. Verify Waveform:

   Switch the HP 8642 on.

   The Phase Detector Input waveform should be 45 MHz and ≈3V p/p. If this signal is good, it is not necessary to do the Signal Generator No. 1 setup in the next test. If the signal is not good, proceed with Signal Generator No. 1 setup.

Test the Phase Detector and Integrator

5. Signal Generator No. 1 Setup:

   Switch the HP 8642 to Standby.

   Desolder the lead of A6A2 C27 that is connected to A6A2 Q6. (See component locator on page 8K-112.)

   Set Signal Generator No. 1 to 45 MHz and 10 dBm.

   Connect Signal Generator No. 1 to the lifted lead of A6A2 C27.

6. Signal Generator No. 2 Setup:

   Ensure that the HP 8642 is switched to Standby.

   If Signal Generator No. 1 is being used, lock the timebases of Signal Generator No. 1 and Signal Generator No. 2 together.

   Disconnect W27 from A6A2 J7 (AP) .

   Set Signal Generator No. 2 to 1.1 MHz and 0 dBm. Connect its output to A6A2 J7 (AP) .

   Switch the HP 8642 on.

7. Verify Signals Levels and Waveforms:

   Set Signal Generator No. 2 to each setting from Table 8K-2 and use the oscilloscope to verify the signal levels or waveform at each specified location.

Table 8K–2. *A6A2 SS21 Voltage*

Signal Generator No. 2 Setting	JCT of A6A2 C8, R13	A6A2 FL1	A6A2 FL2
	Tune Voltage (AV)	EXT REF Sense (AV)	OOL Sense (AW)
1.1 MHz at 0 dBm	see figure 8K-1	≈5 Vdc	≈ 0 Vdc **
1 MHz at 0 dBm	−15 to +15 Vdc *	≈5 Vdc	≈ 5 Vdc **
Remove sig gen 2 from J7	−15 to +15 Vdc	≈0 Vdc	≈5 Vdc **

* steady state (no ramp)
** Allow 3 seconds settling time.

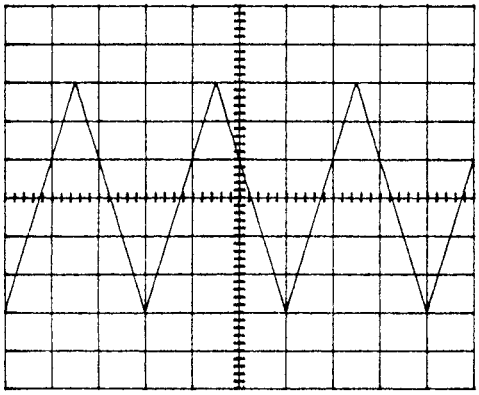


Figure 8K–1. *A6 Integrator Output Signal*

Test the Timebase Disable

8. Measure Voltage Levels:

   Key in [SHIFT] [SPCL] [3] to enter Service Mode.

   For each Function No. in Table 8K-3, verify correct TTL logic levels at the circuit points indicated.

Table 8K–3. *Timebase Voltages*

Service Function	Explanation	DVM Measurements at A6A2		
		TB Disable	Divider Disable	OSC Disable
		J1FL6 (AQ)	U30 Pin 16 (JX)	U30 Pin 14 (AT)
[6][0][1][1][4]	Disable TB	≈5 Vdc	≈5 Vdc	≈4 Vdc
[6][0][2][1][4]	Enable TB	≈0 Vdc	≈0 Vdc	≈−15 Vdc

Restore Module

9. Replace cables:

   Remove Signal Generator No. 2 from A6A2 J7.

   Reconnect W27 to A6A2 J7.

10. If Signal Generator No. 1 was used, remove from circuit, and solder A6A2 C27 back in circuit.

CHECK 2: A6A2 CONTROL CIRCUITRY (SS22)

Essentials of SS22 Circuit Operation

Refer to BD7. On SS22 you will find a voltage controlled **45 MHz OSCILLATOR**, **BUFFER AMPLIFIERS**, and some dividers. These components are part of the Timebase phase locked loop. (The rest of the phase locked loop is on SS21.)

The voltage controlled **45 MHz OSCILLATOR** is a crystal oscillator that outputs a 45 MHz signal that is locked to an external reference signal or a fixed voltage from SS21. This output is directed to a chain of cascoded **BUFFER AMPLIFIERS**. At each stage of the amplifier chain, signals are output to be used as reference signals for other modules. One of the outputs is split and divided to provide 10 MHz and 500 kHz reference signals.

Description of Check 2

This check tests the Timebase reference outputs from the A6A2 control circuitry for correct frequency and power levels. You will also check the Divider Disable function.

If a test fails, refer to the Component Level Repair Directory. (Found at the end of these procedures after Check 6.)

Required Equipment:

Oscilloscope HP1980B
Sensor Module ..... HP 11722A
Measuring Receiver ..... HP 8902A

Test the Timebase Reference Outputs

1. Measure Frequency and Power Levels:

   Measure each output signal listed in Table 8K-4, by removing the cable from each jack listed and connecting the Measuring Receiver in its place.

Table 8K-4. *Timebase Outputs (To Other Modules)*

Output Signal	Cable	A6A2 Jack	*Frequency	Power
HET 45 MHz (HN)	W29	J9	45 MHz ± 90 Hz	3 to 15 dBm
SAWR 45 MHz (AY)	W28	J8	45 MHz ± 90 Hz	3 to 15 dBm
10 MHz Out (AZ)	W23	J5	10 MHz ± 20 Hz	> 7 dBm
500 kHz IF REF (BB)	W26	J6	500 kHz ± 10 Hz	> −21 dBm

* With no external time base, frequency accuracy is not specified. Frequency should be adjustable within this range. (See Adjustment section.)

Test the Phase Detector Input and the Counter 45 MHz

2. Setup:

   Re-connect all cables removed in Table 8K-4.

3. Verify Waveforms:

   Use the Oscilloscope to verify each signal listed in Table 8K-5. Refer to the Component Location Diagram on page 8K-110.

Table 8K–5. *Timebase Outputs (A6)*

Signal Name	Location	Frequency	Level
Phase Detector Input (AS)	A6A2 CR2, CR3	45 MHz ±90 Hz	≈ 2.5 Vpp
Counter 45 MHz (AG)	A6A2 U34,Pin 3	45 MHz ±90 Hz	≈ 1 Vpp
500 kHz FM REF (BA)	A6A2 J2,Pin 2	500 kHz ±10 Hz	TTL

Test the Oscillator Disable Circuitry

4. Setup:

   Ensure that the Oscilloscope is connected to A6A2 J2 pin 2.

5. Verify Waveform:

   Observe 500 kHz signal.

   Key in: [SHIFT] [SPCL] [3] [6] [0] [1] [1] [4] [Hz]

   Signal should diminish to 0 volts.

NOTE

This front panel setting should cause all Timebase outputs from Table 8K-4 and 8K-5 to go to 0 volts.

CHECK 3: A6 CONTROL CIRCUITRY (SS24)

Essentials of SS24 Circuit Operation

Refer to BD8. The left side of this Block Diagram shows the control circuitry for the A6 module. Data from the instruments microprocessor is converted from serial to parallel form in the **SERIAL DATA INTERFACE.**

FM is input on A6A1 J4. It comes from the A2 (Modulation) Module, and although called "FM", it can also carry phase modulation. This audio signal (Audio For Angle Modulation) is directed to the inputs of three blocks of crossover circuitry, **PHASE MODULATION SELECT**, **FM CROSSOVER**, and **FM/PM LINE SELECT.**

Phase modulation is enabled or disabled in **PHASE MODULATION SELECT**. If disabled, the phase modulation circuitry is not going to load the modulation source during FM. If enabled, the audio signal is differentiated (if outside the loop BW). The output of **PHASE MODULATION SELECT** is on two signal paths, FM In BW or FM Out BW.

Audio For Angle Modulation is fed directly to the **FM/PM LINE SELECT** on the signal path labeled "FM Out BW".

FM that is inside the loops 100 Hz bandwidth is integrated in **FM CROSSOVER**. There are two modes of operation in **FM CROSSOVER**; 3 Hz (normal), or DPL (Digital Private Line). In normal operation, the gain of the **FM CROSSOVER** circuitry is 0 dB at 3 Hz. In DPL mode a Low Frequency Feedback path is activated, changing the RC constant of the integrator. (The gain changes to 0 dB at 0.3 Hz). This mode allows for integration at very low rates of modulation.

In **FM/PM LINE SELECT**, phase modulation outside the loop bandwidth and phase modulation inside the loop bandwidth are selected simultaneously, or FM in BW and FM out BW are selected simultaneously.

Angle modulation outside the loop bandwidth is pre-distorted in **SHAPER** (if Shaper is switched in) to compensate for non-linearities in the loop VCO's varactors (found on SS23). There should be unity gain from input to output of the **SHAPER.**

The **DCFM REFERENCE** provides a stable + 40 Vdc to the **VOLTAGE CONTROLLED OSCILLATOR** on SS23 when DCFM is selected on the front panel.

Description of Check 3

This check will test the control circuitry and the angle (FM and PM) modulation sources for the FM VCO assembly.

The **SERIAL DATA INTERFACE** is tested by setting control bits to a predetermined state. This is done by entering key sequences provided in tables, then testing lines with a DVM.

The DCFM reference is tested for the correct voltage level.

PHASE MODULATION SELECT, FM CROSSOVER, and FM/PM SELECT are tested by connecting a known good audio signal to the Audio For Angle Modulation line, then verifying each angle modulation output line.

If a test fails during Check 3, refer to the Component Level Repair Directory. (Found at the end of these procedures after Check 6.)

Required Equipment:

Audio Analyzer	HP 8903A
Oscilloscope	HP1980B
Digital Voltmeter (DVM)	HP3456A

Test the Power Supply and Ground

1. Setup:

   Switch the HP 8642 to standby.

   Remove the A6A1 cover (see assembly locator on page 8K-102).

   Switch the HP 8642 on.

2. Measure Voltage Levels:

   Use the DVM to measure the Power Supply lines at the measurement points shown in Table 8K-6. (Component locations can be found in the Component Locator diagram on page 8K-114).

Table 8K-6. *A6A1 Power Supply Lines*

Measurement at	Nominal Voltage
L9	+50 Vdc
FL13	+15 Vdc
U5 Pin 2	+5 Vdc
L7	+5 Vdc
J5 Pin 4	+5 Vdc
J5 Pin 10	−5 Vdc
FL9	−15 Vdc
J5 Pin 12	GND

Test the Serial Data Interface

3. Measure Voltage Levels:

   Key in [SHIFT] [SPCL] [3], to Enter Service Mode, then for each Service Function in Table 8K-7, use the DVM to measure TTL levels at the A6A1 U18 pin numbers shown. (A6A1 U18 location can be found in the Component Locator diagram on page 8K-114).

Table 8K-7. *FM Loop Control Lines*

Service Function	Line Description and U18 Pin Numbers							
	AC/DC FM U18 Pin19	SHAPER IN/OUT U18 Pin16	MUX SO U18 Pin15	FM/PM Select U18 Pin12	3HZ/DPL Select U18 Pin9	Crossover In/Out U18 Pin6	MUX S1 U18 Pin5	MUX S2 U18 Pin2
[6][0][5][8][5][HZ]	1	0	1	0	1	0	1	0
[6][0][5][1][7][0][HZ]	0	1	0	1	0	1	0	1

Test the Counter Control Lines

4. Measure Voltage Levels:

   Key in [SHIFT] [SPCL] [3] to enter Service Mode, then each Service Function in Table 8K-8, use the DVM to measure TTL levels at the A6A1 J5 pin numbers (See (AO) on the Test Point Locator).

Table 8K–8. *Counter Control Lines*

Service Function	Line Label	Dvm Measurement at A6AU5 Pin	TTL level
60174 Hz	Count Period Select (AC)	9	High
60274 Hz	Count Period Select (AC)	9	Low
60175 Hz	Count Signal Select (AC)	8	High
60275 Hz	Count Signal Select (AC)	8	Low
60173 Hz	Take Reading Strobe (AM)	7	High
60273 Hz	Take Reading Strobe (AM)	7	Low
60172 Hz	Counter Clock (AN)	6	High
60272 Hz	Counter Clock (AN)	6	Low

Test the DCFM Reference Voltage

Connect the Oscilloscope to A6A1 TP5 (HX) .

Select External DCFM by keying in: [FM] [EXT DC] [ON]

5. Measure Voltage Level:

   The amplitude at TP 5 should measure 38V to 41.3V. The voltage should not drift more than 8 mV/hr and should be free from supply line noise.

Test the Modulation Signals

6. Setup:

   Switch the HP 8642 to standby.

   Remove W20 from A6A1 J4 (GI) .

   Set the Audio Analyzer amplitude to 1V p/p and frequency to 20 Hz.

   Connect the Audio Analyzer to A6A1 J4 (GI) .

   Switch the HP 8642 on.

7. Measure Voltage Levels:

   First, enter service mode with [SHIFT] [SPCl] [3], then select the Modulation Source, with service special function from Table 8–9, set the Audio Analyzer Freq and amplitude, then use the Oscilloscope to measure the voltage levels at the U12 and U14 pin numbers specified in Table 8K–9.

Table 8K–9. *Angle Modulation Signals*

Service Function	Audio Analyzer Freq	DVM Measurements	
		Inside (HY) * U12 Pin 14	Outside (IA) ** U14 Pin 2
[6][0][5][5][7][Hz] (Inside FM)	20 Hz 1 Vpp	18 Vpp	1 Vpp
[6][0][5][5][7][HZ] (Inside FM)	100 Hz 1 Vpp	1.4 Vpp	1 Vpp
[6][0][5][1][7][Hz] (Inside PM)	1 kHz 4 Vpp	60 mVpp	176 mV
[6][0][5][4][2] Out FM with shaper	1kHZ 4 Vpp	1.4 Vpp	4 Vp-p
[6][0][5][3] Out PM with shaper	1kHZ 4 Vpp	60 mV	176 mVp–p
[6][0][5][1] OutPM w/out shaper	1kHZ 4 Vpp	10 mVpp	176 mVp–p
* Angle MOD inside BW A6A1 U12Pin 14 Vpp at 0 Vdc ±.1Vdc ** Angle MOD outside BW A6A1 U14 Pin 2 Vpp at 0 Vdc ±.1Vdc			

Test the Modulation Signal Sense Line

8. Setup:

   Set the Audio Analyzer amplitude for 4Vpp and frequency to 10 Hz.

   Key in [SHIFT] [SPCL] [3][6][0][5][4][2][Hz] to set up the HP 8642 for ACFM.

9. Measure Voltage Level:

   Move the Oscilloscope probe to U22 pin 4 (IC) . The signal should measure 10 Hz at ≈900 mVpp.

Restore Module

10. Disconnect the Audio Analyzer from A6A1 J4.

11. Reconnect W20 to A6A1 J4.

CHECK 4: A6A1 FM VCO PHASE LOCKED LOOP ASSEMBLY (SS23)

Essentials of SS23 Circuit Operation

Refer to BD8. The right side of this Block Diagram shows the **PHASE DETECTOR, INTEGRATOR, AND VOLTAGE CONTROLLED OSCILLATOR**. These blocks are the heart of the Timebase phase locked loop.

The reference signal to the loop comes from the Timebase and is called 500 kHz FM Reference. Its signal path is from A6A2, through the center of the A6 module, to A6A1 J5 pin 2.

The 500 kHz Reference signal is divided first to 250 kHz, then to 125 kHz in the **FM REFERENCE DIVIDER**, and directed to the **PHASE DETECTOR**. The other signal to the **PHASE DETECTOR** also comes from A6A2. This signal is the result of the FM Loop 135 MHz signal (from the **VOLTAGE CONTROLLED OSCILLATOR on SS23)** being divided by 1080 on A6A2 (SS19). The output of the **PHASE DETECTOR** is an error signal proportional to the phase difference between these two signals.

In normal (or ACFM) mode, the error signal is directed to the **INTEGRATOR**, and to the **OUT-OF-LOCK DETECTOR**.

In DCFM mode, the error signal is switched out and the **DCFM REFERENCE**, from SS24, controls the VCO.

NOTE

All A6A1 checks are performed with the A6A1 cover on. Because of this requirement, the A6A2 cover will be removed and many of the measurement points and signal injection points for this Check will be on A6A2. The Test Point Locator opposite BD7 will be used in these instances.

Description of Check 4

This check tests the FM VCO Assembly's phase locked loop circuitry, shown on SS23. In the course of checking this circuitry you will also test the Divide-by-1080 circuitry shown on SS19.

The loop VCO is tested in DCFM mode. It is tested first without modulation, then by using an external dc source to modulate the VCO. The VCO output is tested using the Spectrum Analyzer.

The loop Integrator and Divide-by-1080 circuitry is tested in ACFM (normal) mode by measuring the VCO Tune Voltage and the output of the Divide-by-1080 while substituting a signal in the loops feedback path. The Integrator is further tested by applying a modulation signal at a rate inside the loops bandwidth and measuring the VCO Tune Voltage.

The **OUT-OF-LOCK DETECTOR** is tested by simulating out-of-lock conditions and measuring the Diagnostic Bus voltage at the A4 assembly VM (voltmeter) OUT test point.

Required Equipment:

Oscilloscope	HP1980B
Spectrum Analyzer	HP8566A/B
Signal Generator No. 1	HP 8642A/B
Audio Analyzer	HP 8903A
Function Generator	HP 8116A

Verify the 250 kHz TTL Signal

1. Setup:

   Switch the HP 8642 to standby.

   Replace the A6A1 cover.

   Remove the A6A2 cover.

   Connect the Oscilloscope to A6A2 J2 pin 1 (AB) (Refer to Test Point Locator on BD7.)

   Switch the HP 8642 on.

2. Verify waveform:

   Signal should be a 250 kHz TTL waveform.

   Remove the Oscilloscope from circuit.

Test the Loop VCO (DCFM Mode, No Modulation)

3. Setup:

   Locate W24 using the inside of the top cover of the instrument. Disconnect the FM Loop Output by removing W24 from A11A1 J3 [CU].

   Connect W24 to the input of the Spectrum Analyzer.

   Remove W20 from A6A1 J4 (GI) .

   Terminate A6A1 J4 (GI) with a 50Ω load, HP 1250-0839 (part of Bench Service Kit).

   Key in: [SHIFT] [SPCL] [3] [6] [0] [5] [2] [4] [Hz]. This key sequence sets the HP 8642 to External DC.

4. Measure Signal Level and Frequency:

   Signal level on W24 should measure between 0 dBm and 3 dBm. Signal frequency should be between 134.8 MHz and 135.2 MHz.

   Remove A6 W1 from A6A2 J4 (AA) . (Refer to Test Point Locator opposite BD7.)

   Connect A6W1 to the input of the Spectrum Analyzer.

   Signal level should measure between 5 dBm and 17 dBm. Signal frequency should measure between 134.8 MHz and 135.2 MHz.

   If signals do not meet frequency specifications adjust A6A1 C5 as instructed in Adjustment procedures.

Test VCO Flatness (DCFM Mode, With Modulation)

5. Setup:

   On Function Generator set MODE to NORM, Freq to 0.5 Hz (500 mHz), AMP to 6V, OFS to 0.00. Set for triangle wave.

   Remove 50Ω termination from A6A1 J4 (GI) .

   Connect the Function Generator output to the Mod Input at A6A1 J4 (GI) .

   Signal should shift +1.5 MHz and −1.5 MHz. Signal level should remain at between 5 dBm and 17 dBm.

   Connect the FM Loop Output on W24 (previously disconnected) back to the input of the Spectrum Analyzer.

Signal should shift +1.5 MHz and −1.5 MHz. Signal level should remain at between 0 dBm and 3 dBm.

Remove the Spectrum Analyzer from W24.

Reconnect W24 to A11A1 J3.

Remove Function Generator from A6A1 J4.

Test The Divide-By-1080 and Loop VCO (ACFM Mode)

6. Setup:

Key in [SHIFT] [SPCL] [3] [6] [0] [5] [5] [7] [Hz]. This key sequence selects ACFM.

Set Signal Generator No. 1 frequency to 135.000100 MHz.

Set Signal Generator No. 1 amplitude to 10 dBm.

Lock the timebases of Signal Generator No. 1 and the HP 8642 under test together.

Connect Signal Generator No. 1 to A6A2 J4 (AA) . (Refer to Test Point Locator opposite BD7.) This is the input to the **DIVIDE BY-1080** circuitry from SS19. It is tested during the SS23 check and you may want to refer to BD7 to see cable and connector designators.

Connect the Oscilloscope input to A6A2 J2 pin 3 (AM) . (Refer to Test Point Locator opposite BD7.)

Key in [SHIFT] [SPCL] [3] [2] [2] [8] [Hz]. This key sequence selects the VCO Tune Voltage Sense line to be multiplexed at **FM LOOP DIAGNOSTICS INTERFACE**, and routed to A4 TP2.

7. Verify waveforms:

Signal should be a 125 kHz TTL waveform.

Connect the Oscilloscope input ot A4 TP2 VM OUT. Signal should be similar to Figure 8K-2. Signal has a 50% duty cycle

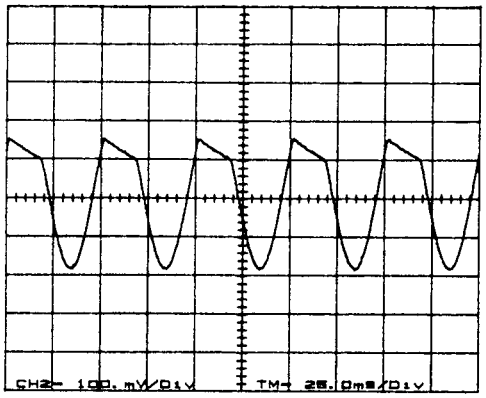


Figure 8K–2.

Remove Signal Generator No. 1 from A6A2 J4 (AA) .

Reconnect A6 W1 to A6A2 J4.

Set Audio Analyzer frequency to 20 Hz.

Adjust the Audio Analyzer amplitude to 1 Vpp.

Connect Audio Analyzer output to A6A1 J4 (GI) .

Signal at A4 TP2 should be similar to Figure 8K-3.

Remove the Audio Analyzer from A6A1 J4.

Reconnect W20 to A6A1 J4.

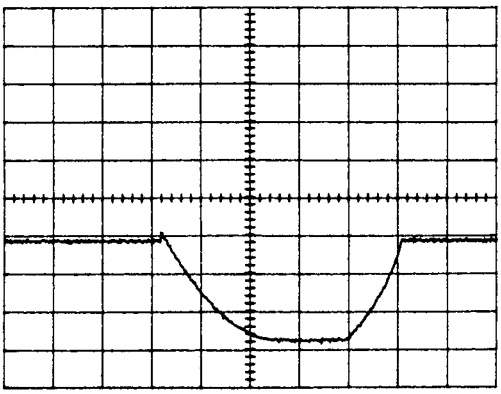


Figure 8K–3.

Test the Out-of-Lock Detector

8. Setup:

Key in [SHIFT] [SPCL] [3] [2] [2] [7] [Hz]. This key sequence selects the output of the **OUT-OF-LOCK DETECTOR** (not shown on BD8), to be multiplexed at **FM LOOP DIAGNOSTICS INTERFACE** and routed to A4 TP2 (VM OUT). Perform each function in Table 10 and verify voltage at A4 TP2.

Table 8K–10. *Diagnostics Interface Output*

Function	A4TP2 Measurement
Remove A6 W1 from A6A1 J3 (AA) (135 MHz)	≈0 Vdc
Re-connect A6 W1 to A6A1 J3 (135 MHz)	≈+5 Vdc
[SHIFT] [SPCL] [3] [6] [0] [1] [1] [4] [Hz] (Disables 500 kHz)	≈ 0 Vdc
[SHIFT] [SPCL] [3] [6] [0] [2] [1] [4] [Hz] (Enables 500 kHz)	≈ +5 Vdc

CHECK 5: A6A2 COUNTER/TIMEBASE ASSEMBLY (SS19, P/O SS20)

Essentials of SS19 Circuit Operation

Refer to BD7. The upper left portion of the Block Diagram shows SS19. The circuitry represented on SS19 performs a **DIVIDE-BY-12,500 OR 25,OOO** function for the counter circuitry (represented on SS20). The circuitry on SS19 also gates and then outputs one line each through **COUNT PERIOD SELECT** and **COUNTED SIGNAL SELECT** to the counter. The **DIVIDE- BY-1080** circuitry divides the FM loop VCO output from 135 MHz to 125 kHz.

The output of **COUNT PERIOD SELECT** is either 10 Hz or a TTL Audio signal from the Modulation (A2) Module. If the Count Period Select line selects 10 Hz, a 10 Hz signal is selected by the switch in **COUNT PERIOD SELECT**. This 10 Hz signal can be either the 250 kHz TTL signal (divided by 25000), or the FM Loop 135 MHz signal (divided by 1080, then by 12,500).

If the Count Period Select line selects Audio, then the Counter Audio signal at A6A2 J3 is gated through **COUNT PERIOD SELECT** (after passing through **COUNTED SIGNAL SELECT**) to the counter.

The output of **COUNTED SIGNAL SELECT** is either a TTL Audio signal or a TTL 45 MHz signal. If the Counted Signal Select line selects Audio, then the Counter Audio signal at A6A2 J3 is gated through **COUNTED SIGNAL SELECT** to the counter. If the Counted Signal Select line selects 45 MHz, then the 45 MHz signal from **RF TO TTL TRANSLATION** is gated through **COUNTED SIGNAL SELECT** to the counter.

The HP 8642 microprocessor controls the **COUNT PERIOD SELECT and COUNTED SIGNAL SELECT** gating. There are three modes of operation.

1. Direct Audio: The Audio signal is counted and the 10 Hz (250 kHz TTL divided by 25000) signal is the Count Period.

2. Reciprocal Audio: The 45 MHz signal is counted and the Audio signal is the Count Period.

3. Reciprocal DCFM: The 45 MHz signal is counted and the 10 Hz (FM Loop 135 MHz signal divided by 1080, then by 12,500) signal is the Count Period.

Direct Audio is used to count Audio Frequencies greater than 10 kHz. Reciprocal Audio is used to count Audio Frequencies less than 10 kHz. Reciprocal DCFM is used when the FM VCO is set up for DCFM.

Description of Check 5

This check begins by having you enter Service Mode and verify TTL levels on the the Counter Select Lines. Then, the output waveforms of the **COUNT PERIOD SELECT, COUNTED SIGNAL SELECT, and DIVIDE-BY-1080** are verified. The Divider Enable line to **DIVIDE-BY- 12,500 OR 25,OOO** is also tested.

If a test fails during Check 5, refer to the Component Level Repair Directory, unless instructed otherwise. (Found at the end of these procedures after Check 6.)

Required Equipment:

Oscilloscope	HP 1980B
DVM	HP 3456A
Pulse/Function Generator	HP 8116A

Test the SS19 Power Supplies

1. Setup:

   Switch the HP 8642 to standby.

   Remove the A6A2 cover.

   Switch the HP 8642 on.

2. Measure Voltage Levels:

   Check the Counter Power Supply Lines at the inductors specified in Table 8K-11. (Refer to the Component Locator on page 8K-104 for inductor locations).

Table 8K-11. *Power Supply Voltages*

Inductor	Nominal Voltage
L21	+5 Vdc
L22	−5 Vdc

Test the Divider Enable Line

3. Setup:

   Switch the HP 8642 to standby.

   Connect the Oscilloscope probe to Divider Enable (A6A2 U17 pin 13 (AH)).

   Switch the HP 8642 on.

4. Measure Voltage Level:

   Verify that the Divider Enable line is a TTL low on the oscilloscope.

5. Setup:

   Locate A6A2 U7 using the Component Locator on page 8K-106. Using a test lead, ground A6A2 U7 pin 5. This forces the Divider Enable line to its high state. (Leave this point grounded until instructed to disconnect ground)

   Key in: [SHIFT] [SPCL] [3] [6] [4] [5] [Hz]

6. Measure Voltage Level:

   Verify that the Divider Enable line is a TTL high on the oscilloscope.

NOTE

Even if the Divider Enable Line test fails, continue with Check 5. If no other tests fail, go on to Check 6 where the Divider Enable Line will be further tested.

Test the TTL High Reference

7. Setup:

   Connect the Oscilloscope probe to A6A2 U17 pin 1 (AI) .

8. Measure Voltage Level:

   Signal should be ≈ +5V dc (TTL High).

Test the Divide-By-1080

9. Setup:

   Connect the Oscilloscope probe to A6A2 J2 pin 3 (AL) .

10. Verify Waveform:

    Set Oscilloscope to verify waveform in Figure 8K-4.(135 Hz divide by 1080 waveform (125 KHz TTL)

Test the Count Period and Counted Signal Lines

11. Setup:

    Ensure that the ground lead for A6A2 U7 pin 5 is still connected (see Divider Enable Line test).

    Disconnect the Counter Audio line W21 from A6A2 J3 (FF) .

    Set up the Pulse/Function Generator for a 20 Hz TTL signal.

    Connect the Pulse/Function Generator to A6A2 J3 (FF) .

    Disconnect the Oscilloscope from A6A2 J2 pin 3.

12. Measure Voltage Levels:

    Key in [SHIFT] [SPCL] [3] to enter Service Mode.

    Key in the Service Functions from Table 8K-12, and use the Oscilloscope to verify that Counter Select Lines are the correct TTL state. Use the Oscilloscope to verify that the Counted Signal and Count Period signals are similar to the figure specified.

Table 8K-12. *Counter Signal Selects*

Service Function	Counter Mode	Count Period		Counted Signal	
		J2 Pin 9	U7 Pin 8	J2 Pin 8	U33 Pin 8
[6][4][0][Hz]	Invalid State	0	Figure 8K-4	0	Figure 8K-4
[6][4][1][Hz]	Reciprocal Audio	0	Figure 8K-4	1	Figure 8K-6
[6][4][2][Hz]	Direct Audio	1	Figure 8K-5	0	Figure 8K-4
[6][4][3][Hz]	Reciprocal DCFM	1	Figure 8K-5	1	Figure 8K-6

Restore Module

13. Switch the HP 8642 to Standby.

14. Remove the Oscilloscope from circuit.

15. Remove the test lead from A6A2 U7 pin 5.

16. Remove the Pulse/Function Generator from circuit.

17. Reconnect W21 to A6A2 J3 (FF) .

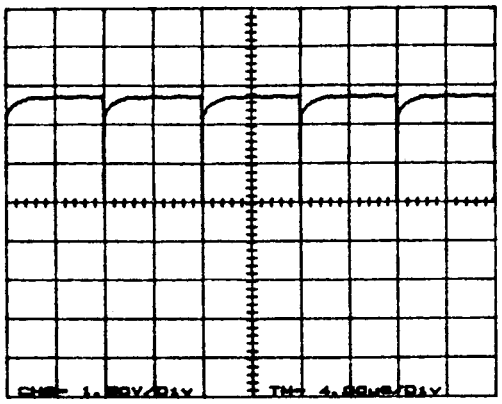


Figure 8K–4.

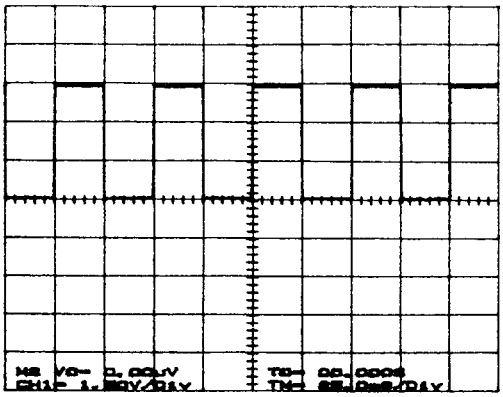


Figure 8K–5.

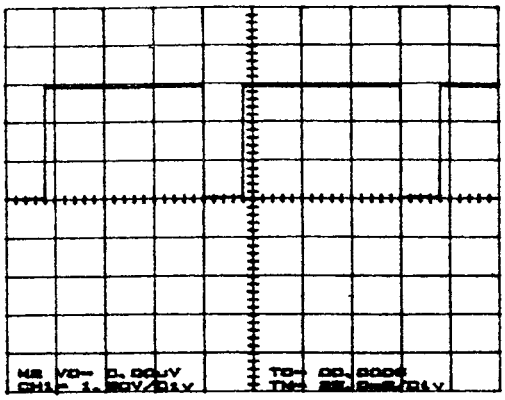


Figure 8K–6.

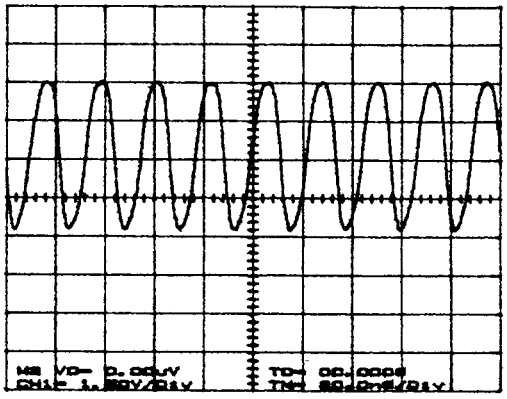


Figure 8K–7.

CHECK 6: A6A2 COUNTER/TIMEBASE ASSEMBLY SS20

Essentials of SS20 Circuit Operation

Refer to BD7. The upper right portion of the Block Diagram shows SS20. There are two main blocks of Counter circuitry, **CONTROL LOGIC, and 24 BIT COUNT CHAIN.**

For the following discussion, refer to **CONTROL LOGIC** on SS20. Upon power up or reset, the HP 8642 pulses the Take Reading Strobe line (J2 pin 7). This action forces the 1D input of the Edge Latch (U8B) to a high state. (This happens through U36A, U36B, U8A, U20D, and U18A). With the 1D input of U8B held at a high state, the Edge Latch is ready to detect the first positive going edge to occur on the Count Period 10 Hz or Audio line.

When a positive going edge is detected by the Edge Latch, the high on the 1D input of U8B is latched. The outputs of U8B are input to a state machine consisting mainly of U9 and U19. The Count Period line (U19A pin 3 under the bracketed label "Flip-Flops") goes to a high state. When this happens, the Count Period line enables the **COUNT GATE**, allowing the Counted 45 MHz or Audio signal to be gated into the counters (U23, 27-29 in **24 BIT COUNT CHAIN**). When the Count Period line goes to a high state it also resets the **EDGE LATCH** through U10 pin 2. A high state on U10 pin 2 triggers a 5mS pulse through U7A and U7B, and resetting U8B.

When the next positive edge is detected by the Edge Latch, the Count Period line at U19A pin 3 goes to a low state. When this happens, the Count Period line disables the **COUNT GATE**, which stops the count. The output of U19B (pin 6) goes high almost simultaneously, which triggers One Shot U11 (pin 2). One output of U11 (pin 4) activates loading of data to the latches (U24-26 in **24 BIT COUNT CHAIN**). Another output of U11 (pin 13) sends a 5mS pulse (the time period of the one shot) to the microprocessor, on the line labeled Load 1. The Load 1 line also triggers U11 (pin 9). The output labeled "Clear" (U11 pin 5) clears the count chain (U28, U29 in **24 BIT COUNT CHAIN).** Clear (L U11 pin 12) resets the Edge Latch by pulsing its reset line through U7A and U7B, and resets U8A (pin 1) to enable the **SERIAL DATA OUT SWITCH.**

The HP 8642 microprocessor then clocks out the latched data by pulsing the Counter Clock line (on J2 pin 6).

Description of Check 6

This Check tests the A6A2 counter circuitry on SS20.

The Counter Control Lines are tested by entering Service Mode functions and measuring control line signals.

The Counter is checked by connecting the 500 kHz IF Reference from the Timebase circuitry (also on A6A2) to the Counter Audio input. Then, you will enter a Service Mode function that will output a value on the front panel display. This value will tell you if the Counter is operating correctly.

If a test fails during Check 6, refer to the Component Level Repair Directory. (Found at the end of these procedures after Check 6.)

Required Equipment:

Oscilloscope ..... HP 1980B

NOTE

If steps 1 and 2 fail, then proceed with steps 3 through 6. If steps 1 and 2 pass, then Checks 3 through 6 have passed.

Test the Counter Under Normal Conditions

1. Setup:

   Switch the HP 8642 on.

   Key in: [SHIFT] [MOD FREQ] [ON] to turn on the Modulation Oscillator.

   Key in: [MOD FREQ] [1] [0] [kHz] to set the modulation frequency to 10 kHz.

2. Verify Counter Output:

   Key in [SHIFT] [SPCL] [3] to enter the service mode.

   Key in each service mode function and verify front panel display.

Table 8K–13. *Display Counter Count*

Function	Counter Mode	Front Panel Display
6131 Hz	Direct Audio Count	≈ 100000
6133 Hz	Reciprocal Count	≈ 100000
6134 Hz	DCFM Count	≈ 1350000000

Test the Counter Control Lines

3. Setup:

   Switch the HP 8642 to on.Key in [SHIFT] [SPCL] [3] to enter the service mode.

   Key in each special function while verifying the signal with the oscilloscope at the location listed in Table 8K-13.

Table 8K–14. *Counter Control Lines*

Function	Checked	Scope Probe At	Signal
644 Hz	(AN) Counter CLK	J2 Pin 6	NEG Pulse ≈ 20 mS
645 Hz	(AM) Take Reading Strobe	J2 Pin 7	NEG Pulse ≈ 20 mS
645 Hz	(AH) Divider Enable	U18 Pin 3	POS Pulse ≈ 200 mS

Test the Counter For Correct Operation

4. Setup:

   Switch the HP 8642 to standby.

   Connect the Oscilloscope to U25 pin 9 (Use the Component Locator on page 8K-106.)

   Disconnect W26 from A6A2 J6 (BB) .

   Disconnect W21 from A6A2 J3 (FF) .

   Connect A6A2 J6 (BB) to A6A2 J3 (FF) using a cable supplied in the HP 11802A Bench Service Kit.

   Switch the HP 8642 on.

   Key in: [SHIFT] [SPCL] [3] [6] [4] [2] [Hz] to set up the counter select lines.

   Key in: [SHIFT] [SPCL] [3] [6] [4] [5] [Hz] to shift the counter data into the latches.

NOTE

Any error message that may come up on the HP 8642 front panel should be ignored.

5. Measure TTL Voltage Levels:

   Verify that the TTL level at U25 pin 9 is a TTL low. This value corresponds to the MSB in the following binary coded decimal.

   0000 0000 1100 0011 0101 0000
   MSB LSB

NOTE

The decimal equivalent of this number is 50000. This number equals the counted frequency (500 kHz) divided by the Count Period Signal frequency (10 Hz).

   Key in: [6] [4] [4] [Hz] for each of the remaining 23 bits (MSB to LSB), while verifying correct TTL levels. (This clocks the 24 bit word from above, out 1 bit at a time.)

Test the Counter Output

Key in: [SHIFT] [SPCL] [3] [6] [1] [3] [1] [Hz].

6. Verify Counter Output:

   The HP 8642 front panel display should read [5000000].

Restore Module

7. Switch the HP 8642 to standby.
8. Disconnect the cable at A6A2 J3 (FF) and A6A2 J6 (BB) and return cable to Bench Service Kit.
9. Reconnect W26 to A6A2 J6 (BB) .
10. Reconnect W21 to A6A2 J3 (FF) .

COMPONENT LEVEL REPAIR DIRECTORY

The following tables contain information to aid in component level repairs. These tables are designed to be used after the module troubleshooting procedures have verified a failure in circuitry represented on one of the module service sheet schematics. In general the tables supply one of the following types of information:

* Special function codes relevant to the module.

* Transistor emitter, base and collector voltages.

* Frequency and power levels at different circuit points.

* Module control line and power supply interconnections in the module and instrument.

NOTE

SHIFT SPCL 3 needs to be entered only once, after which Service Functions can be entered in continuously. Each special function table's first column is labeled "Enter Service Mode", and the column has SHIFT SPCL 3 in it. This only needs to be entered once before proceeding with the service functions.

SERVICE SHEET 19

Table 8K–15. SS19 Tables Set Up Counter Lines

Enter Service Mode	Service Function	Description	Counter Selects	
			Count Period	Counted Signal
SHIFT	6 4 0 HZ	Invalid State	0	0
SPCL	6 4 1 HZ	Reciprocal Audio	0	1
3	6 4 2 HZ	Direct Audio	1	0
	6 4 3 HZ	Reciprocal DCFM	1	1

SERVICE SHEET 20

Table 8K–16. SS20 Tables/Read Counter Data

Enter Service Mode	Service Function	Counter Mode	Description
	6 1 3 0 Hz	EXT Direct Audio	Sets up Counter and Outputs Data to Display in 0.1 Hz Units.
SHIFT	6 1 3 1 Hz	INT Direct Audio	
SPCL	6 1 3 2 Hz	EXT Reciprocal Audio	
3	6 1 3 3 Hz	INT Reciprocal	
	6 1 3 4 Hz	Reciprocal DCFM	

*Table 8K–17. Determine Counter Data**

Counter Mode	Contents Of Counter
Direct Audio	Audio FREQ÷ 10
Reciprocal Audio	45 E+6÷ Audio FREQ
Reciprocal DCFM	6.075E+14÷ FMVCO FREQ

* NOTE: This would be the actual number in the counter latches.

SERVICE SHEET 21

Table 8K–18. A6A2 Power Supply Lines

Supply	A17	A5		A6A2
	Output	Input	Output	Input
+50 Vdc	J2 Pins 3&4	J12 Pins 3&4		
+15 Vdc	J2 Pins 9–18	J12 Pins 9–18	J1 Pin 13	J1 Pin 2
−5 Vdc	J2 Pins 23–26	J12 Pins 23–26		
+5 Vdc	J2 Pins 35–50	J12 Pins 35–50	J1 Pin 14	J1 Pin 1
−15 Vdc	J2 Pins 19–22	J12 Pins 19–22	J1 Pin 11	J1 Pin 4
GND		Chassis GND	J1 Pin 2,4,6,7,10,12	J1 Pin3,5,7,9,10,11,13, 14

SERVICE SHEET 22

Table 8K–19. *SS22 DC Voltage*

Transistor	Collector	Base	Emitter
Q3	−6.8 to −7.8	−4 to −6	−3.2 to −5.2
Q4	−3.2 to −5.2	−.75 to −2.5	−.5 to −1.5
Q5	5 to 5.3	2 to 3	1.3 to 2.3
Q6	−9.8 to −11.2	−7.5 to −8.5	−6.8 to −7.8
Q7	−14.5 to −13.5	−10.5 to −12	−9.8 to −11.2
Q8	14 to 15	GND	≈ −.5

Table 8K–20. *SS22 RF Power Levels*

Stage	Input Level	Output Level
45 MHz HET (HN)	2.5	2.5 Vpp
45 MHz SAWR (AY)	2.5	2.5 Vpp
45 MHz Phase DET (AS)	2.5	2.5 Vpp
45 MHz Counter (AG)	2.5	1.0 Vpp
Doubler	2 Vpp	1 Vpp
90 MHz BPA	1 Vpp	3 Vpp
Divide-By-9	3 Vpp	4 Vpp
TTL Buffer	4 Vpp	6 Vpp
Divide-By-20	4 Vpp	
500 kHz FM REF (BA)		4 Vpp
500 kHz IF REF (BB)		4 Vpp

SERVICE SHEET 23

Table 8K–21. *SS23 DC Voltage*

Mode	U9		(HY)
	Pin 2	Pin 3	
EXT ACFM*	≈ .6 Vdc	≈ .64 Vdc	0 Vdc
EXT DCFM*	≈ .64 Vdc	≈ .1Vdc	0 Vdc

Table 8K–22. *SS23 Integrator Voltages*

Mode	Q10			Q11		
	Collector	Base	Emitter	Collector	Base	Emitter
EXT ACFM*	46 to 48 Vdc	−11.3 to −13.3 Vdc	−12 to −14 Vdc	≈50 Vdc	46 to 48 Vdc	45.5 to 47.5 Vdc
EXT DCFM*	48 to 50 Vdc	−13.5 to −14.5 Vdc	−14 to −15 Vdc	≈50 Vdc	48.5 to 49.5 Vdc	48 to 49 Vdc

* Voltages are with loop locked and no modulation applied.

Table 8K–23. *Power Splitter A6A1U23*

Pin 2	Pin 3	Pin 5	Pin 8
−4.6 to−4.9 Vdc	−7 to −8 Vdc	−.8 to −1.2 Vdc	−.8 to −1.2 Vdc

Table 8K–24. *Isolation Amplifier*

Transistor	Collector	Base	Emitter
Q6	−.5 to −.9 Vdc	−7 to −8 Vdc	−7.7 to −8.7 Vdc
Q7	9.5 to 10.5 Vdc	−7.7 to −8.7 Vdc	−.5 to −.9 Vdc

Table 8K–25. *A6A1 Power Supply Lines*

Supply	A17	A5		A6A1
	Output	Input	Output	Input
+50 Vdc	J2 Pins 3&4	J12 Pins 3&4	J1 Pin 40	J1 Pin 1
+15 Vdc	J2 Pins 9–18	J12 Pins 9–18	J1 Pin 37–39	J1 Pins 2–4
−5 Vdc	J2 Pins 23–26	J12 Pins 23–26	J1 Pin 31–33	J1 Pins 8–10
+5 Vdc	J2 Pins 35–50	J12 Pins 35–50	J1 Pin 34–36	J1 Pins 5–7
−15 Vdc	J2 Pins 19–22	J12 Pins 19–22	J1 Pin 30	J1 Pin 11
GND		Chassis GND	J1 Pin 29	J12–24(even numbers)

Table 8K–26. *SS23 Power Levels*

Stage	Input Level	Output Level	Stage Gain
Power Splitter	−3 to +3 dBm	0 to 5 dBm	2.5 dBm*
Isolation Amplifier	0 to 3 dBm	0 to 10 dBm	6.5 dBm
* With an input level of −3 to + 3dBm the output will remain 2.2 to 2.4 dBm.			

SERVICE SHEET 24

Table 8K–27. *SS 24 DC Voltage*

Transistor	Collector	Base	Emitter
Q12	50 Vdc	38.7 to 42 Vdc	38 to 41.3 Vdc
Q13	38.7 to 42 Vdc	−-8 to −10 Vdc	-8.7 to −-10.7 Vdc

Table 8K–28. *Counter Control Mode (To be used with Bit 74 and 75)*

CNT Gate SEL*	+ CNT COUNT SEL	Mode
0	1	Reciprocal Audio
1	0	Direct Audio
1	1	Reciprocal
* 0 = Audio input 1 = FM Input + 0 = Audio Input 1 = 45 MHz Input		

MISCELLANEOUS

Table 8K-29. *FM/Timebase Diagnostic Line Enable*

Enter Service Mode	Service Function	Line Label	Explanation
	[8] [HZ]	Time Base sense	
[SHIFT]	[2] [7] [HZ]	FM OOL	
[SPCL]	[2] [8] [HZ]	FM Tune Voltage	M=13.12
[3] [2]	[2] [9] [HZ]	FM MOD Sense	O=9.259 M=4.782
	[5] [1] [HZ]	MOD BD FM OUT	

Table 8K-30. *Control Sequence*

Enter Service Mode	Select a Function		Select a Line	
			[1] [4] [HZ]	TB Disable
			[1] [9] [HZ]	TB OOL Mask
			[2] [0] [HZ]	FM OOL Mask
			[4] [6] [HZ]	FM Clock
[SHIFT]	[6] [0] [0][1]	Read Lines state	[4] [7] [HZ]	FM Data
[SPCL]	[6] [0] [1][2]	Set Bit to 1	[7] [2] [HZ]	CNT Clock
[3]	[6] [0] [2][3]	Set Bit to 0	[7] [3] [HZ]	CNT Enable
	[6] [1] [5][4]	Continuous Toggle	[7] [4] [HZ][5]	CNT Gate SEL
			[7] [5] [HZ][5]	CNT Count SEL
			[1] [0] [7] [HZ]	TB OOL
			[1] [0] [8] [HZ]	FM OOL
			[1] [1] [5] [HZ]	CNT RDY INT
			[1] [2] [0] [HZ]	CNT Data Back

[1] Example [600] [14] [H2] reads the TB Disable line and will display a "1" or "0" depending on its state.

[2] Example [601] [14] [H2] set the TB Disable line to TTL "1".

[3] Example [602] [14] [H2] sets the TB Disable line to TTL "0".

[4] Example [615] [14] [H2] toggles the TB Disable line continuously. This can only be disabled by turning the power on the HP 8642 off and then back on.

[5] See counter control mode table for more info.

Table 8K-31. *Control Line Interconnections*

Line Label	A4			A5		A6
	IC	Pin	Latch Out	DIST In	Dist Out	FM Module
TB DIS	U12	2	P2 Pin 44	J17 Pin 44	J1 Pin 7	A6A2 J1 Pin 8
TB OOL Mask	U13	2	A9U32 Pin 19			
FM OOL Mask	U13	12	A9U32 Pin 16			
FM Clock	U16	16	P2 Pin 46	J16 Pin 46	J1 Pin18	A6A1J1 J1 Pin 23
FM Data	U16	19	P2 Pin 44	J16 Pin 44	J1 Pin 16	A6A1J1 J1 Pin 25
CNT Clock	U6	5	P2 Pin 39	J16 Pin 39	J1 Pin 22	A6A1 J1 Pin 19
CNT Enable	U6	9	P3 Pin 5	J15 Pin 5	J1 Pin 24	A6A1 J1 Pin 17
CNT Gate SRL	U6	12	P3 Pin 6	J15 Pin 6	J1 Pin 28	A6A1 J1 Pin 13
CNT Count SRL	U6	6	P3 Pin 4	J15 Pin 4	J1 Pin 26	A6A1 J1 Pin 15
TB OOL	U35	4	P3 Pin 28	J15 Pin 28	J1 Pin 3	A6A2 J1 Pin 12
FM OOL	U35	8	P2 Pin 7	J16 Pin 7	J1 Pin 15	A6A1 J1 Pin 26
CNT RDY INT	U18	12	A11U38 Pin 1			
CNT Data Back	U31	13	P3 Pin 45	J15 Pin 45	J1 Pin 20	A6A1 J1 Pin 21

Table 8K-32. *A6 Output Specifications*

Signal	Power	Harmonics	Spurs
135 MHz (CU)	0 to 5 dBm	f3 <−9 dBc	≤ 500 kHz <−100 dBc
		All others < −20 dBc	≥500kH < −105 dBc
45 MHz (HN)	3 to 15 dBm	<−15 dBc	<−100 dBc
45 MHz (AY)	3 to 15 dBm	<−15 dBc	5 MHz <−50 dBc
			All others < −100 dBc
10 MHz (AZ)	>7 dBm	<− 35 dBc	< −50 dBc
500 kHz (BB)	≤−20 dBm	f2 <− 30 dBc	
		f3 <− 5 dBc	
		f4 <− 30 dBc	
		f5 <− 5 dBc	

Adjustments

DESCRIPTION OF A6 ADJUSTMENTS

Overall Equipment List

Digital Voltmeter (DVM)	HP3456A
Measuring Receiver	HP8902A
Spectrum Analyzer	HP8566A/B
HP 8642 Bench Service Kit	HP 11802A
Sensor Module	HP11722A
Attenuator	HP 355D
HP-IB Printer	HP 82906A
Audio Analyzer	HP 8903A/B

NOTE

Each adjustment procedure assumes the HP 8642 internal cabling is connected normally and all circuitry is functioning properly.

Using the Measuring Receiver and Sensor Module, the 45 MHz Oscillator power and frequency is adjusted in Adjustment 1.

In Adjustment 2, the 135 MHz VCO sensitivity is adjusted by applying a modulating signal with the Audio Analyzer, measuring the voltage of the audio signal with the Digital Voltmeter, and then measuring the resulting FM deviation with the Measuring Receiver. These measurements are then used to calculated what the resulting deviation should be, and the VCO sensitivity is adjusted. The audio signal is then removed and the HP 8642 is set to DCFM mode. The DCFM center frequency is then adjusted to be within proper limits as read on the Measuring Receiver.

FM Flatness is then adjusted by deviating the 135 MHz VCO with the Audio Analyzer at a 1 KHz rate, and measuring the audio signal level with the Digital Voltmeter and the deviation with the Measuring Receiver. The audio rate is then changed to 20 Hz and the audio signal level measured with the Digital Voltmeter. The desired FM deviation is then calculated and the FM Crossover adjusted to for the desired deviation.

Phase Modulation Flatness is adjusted last. The HP 8642 internal modulation source is used for this adjustment. The internal modulation source is set to 20 Hz and phase modulation set to 100 radians. The phase modulation is then measured with the Measuring Receiver. Tolerance limits are then calculated for a 1 kHz rate and the internal modulation source set to 1 kHz. The phase modulation flatness is then adjusted within the tolerance limits.

ADJUSTMENT 1: A6A2 TIMEBASE PHASE LOCKED LOOP

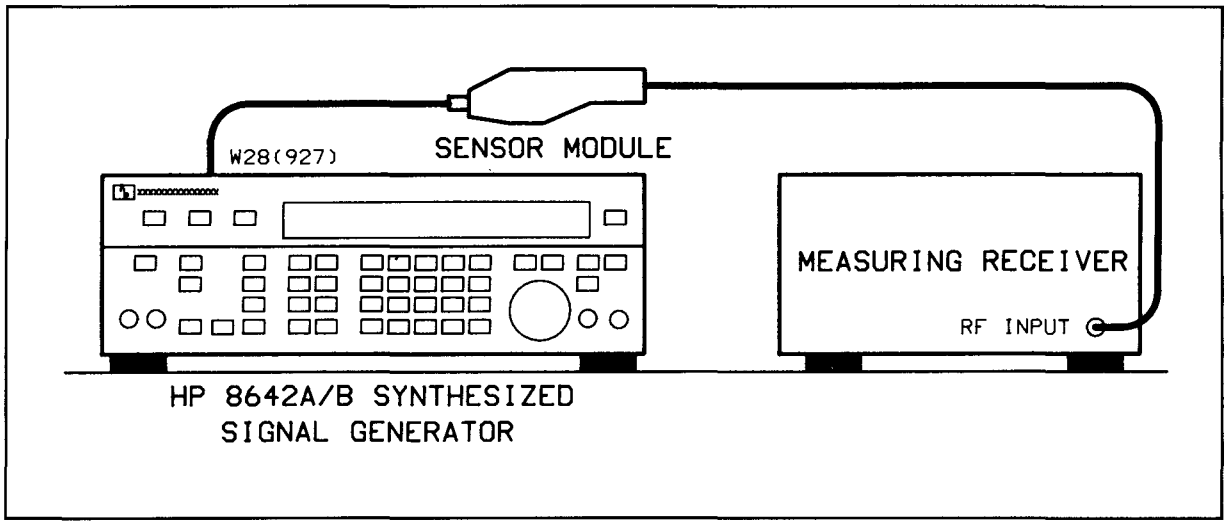


Figure 8K–8. *Timebase Adjustment Setup*

Required Equipment:

Measuring Receiver ..... HP 8902A
Sensor Module ..... HP 11722A

Procedure

45 MHz Oscillator Power Adjustment

1. Setup:

   Disconnect any reference from the EXT REF INPUT on the HP 8642 rear panel. Disconnect W28 from A7A1J2. Connect W28 to the sensor module. Set the Measuring Receiver mode to RF Power.

2. Adjust A6A2 C15 for maximum power. The measured power must be greater than +3 dBm.

45 MHz Oscillator Frequency Adjustment

3. Setup:

   Set the Measuring Receiver to frequency mode with 10 Hz resolution (7.1 SPCL on the HP 8902A). Connect a 10 MHz frequency standard to the External Reference input of the Measuring Receiver.

4. Adjust A6A2 R11 for a Measuring Receiver reading of between 45.00001 and 44.99999 MHz.

5. Reconnect W28 to A7A1J2.

ADJUSTMENT 2: A6A1 FM PHASE LOCKED LOOP

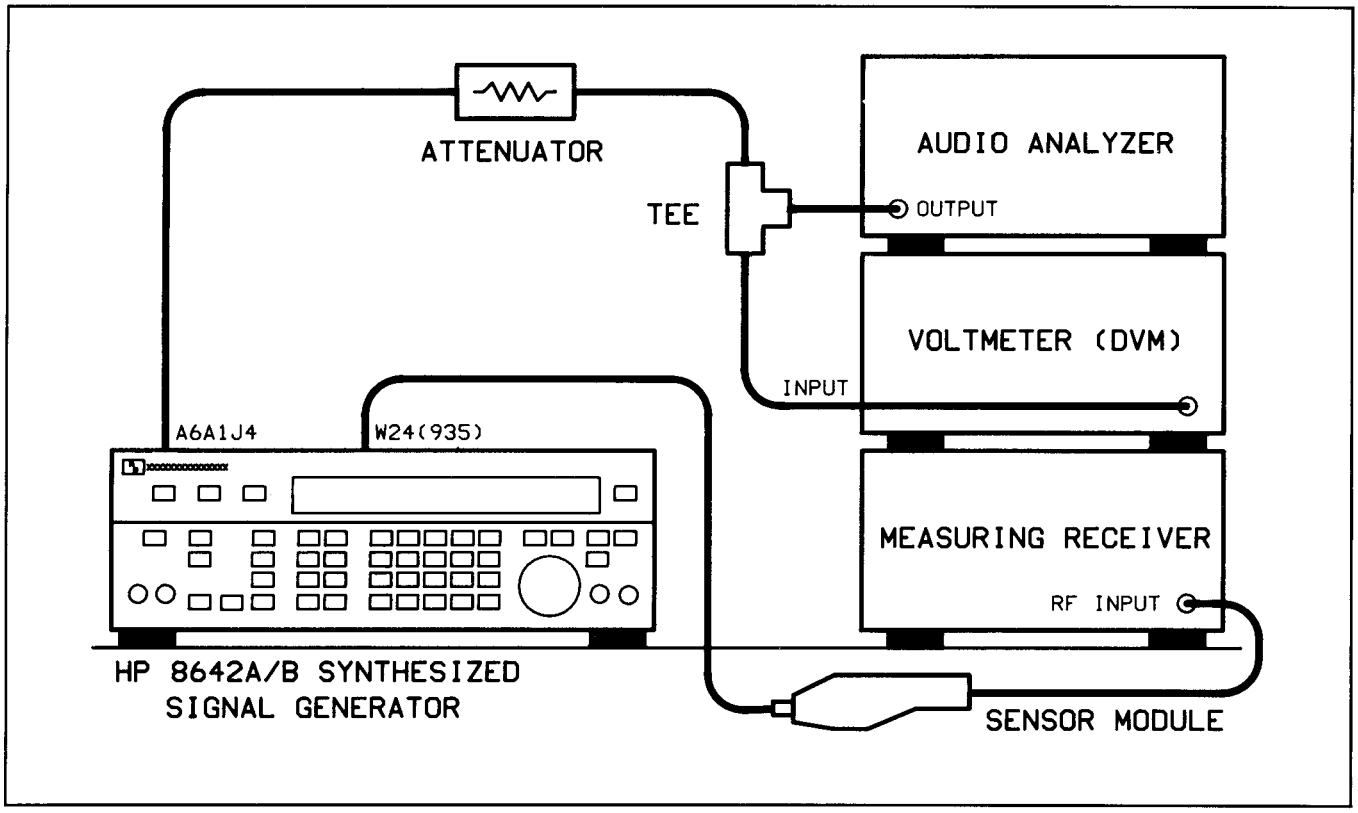


Figure 8K–9. *A6A1 FM Phase Locked Loop Adjustment Setup*

Required Equipment:

Measuring Receiver	HP 8902A
Sensor Module	HP 11722A
Audio Analyzer	HP 8903A
Digital Voltmeter	HP 3456A
Attenuator	HP 355D
HP-IB Printer	HP 82906A

Procedure

VCO Sensitivity/DCFM Center Frequency Adjustment

1. Setup (For VCO Sensitivity Adjustment):

   Disconnect W24 from A11A1 J3.

   Connect W24 to the sensor module.

   Disconnect W20 from A6A1 J4.

   Set the Audio Analyzer to AC level, 190 mV and 10 kHz.

   Set the HP 8642 to INSTR PRESET and FM ON.

2. Connect a BNC TEE to the Audio Analyzer Output.

   Connect a BNC cable between A6A1J4 and the BNC TEE on the Audio Analyzer output.

   Connect a BNC cable between the digital voltmeter and the TEE on the Audio Analyzer output.

   Set the Measuring Receiver mode to FM and detector to average.

   Key in 135 MHz on Measuring Receiver.

   Set the digital voltmeter to AC volts.

   Set the HP 8642 to EXT AC.

3. Measure Audio Analyzer output ($Volts$) on the Digital Voltmeter.

4. Calculate the upper $DevU$ and lower $DevL$ limit of the Measuring Receiver using the following formula:

$$DevU = Volts \times 507.01 = \_\_\_\_kHz$$

$$DevL = Volts \times 477.48 = \_\_\_\_kHz$$

NOTE

When adjusting A6A1 C5 in the next step, use a ceramic adjustment tool. Metallic adjustment tools will adversely effect the accuracy of the readings.

5. Adjust VCO Sensitivity:

   Adjust A6A1 C5 until the Measuring Receiver reads within the upper ($DevU$) and lower ($DevL$) limits calculated in step 4.

6. Setup (For DCFM Center Frequency Adjustment):

   Set the Measuring Receiver mode to frequency.

   Set the HP 8642 to EXT DC.

   Disconnect the voltmeter and Audio Analyzer from A6A1 J4.

7. Adjust DCFM Center Frequency:

   Adjust A6A1 R66 until the Measuring Receiver reads between 135.0010 to 134.9990 MHz. If R66 will not adjust the frequency to within these limits then continue with step 8. Otherwise, go on to FM Flatness Adjustment, step 11.

8. Re-Adjust VCO Sensitivity:

   Adjust R66 to get as close as possible to 135.0000 MHz.

NOTE

In the following step, do not adjust C5 more than necessary.

9. *Carefully* adjust C5 slightly to bring the Measuring Receiver reading to within 135.01000 to 134.99000 MHz.

10. Repeat steps 2 thru 5.

FM Flatness Adjustment (<10 kHz)

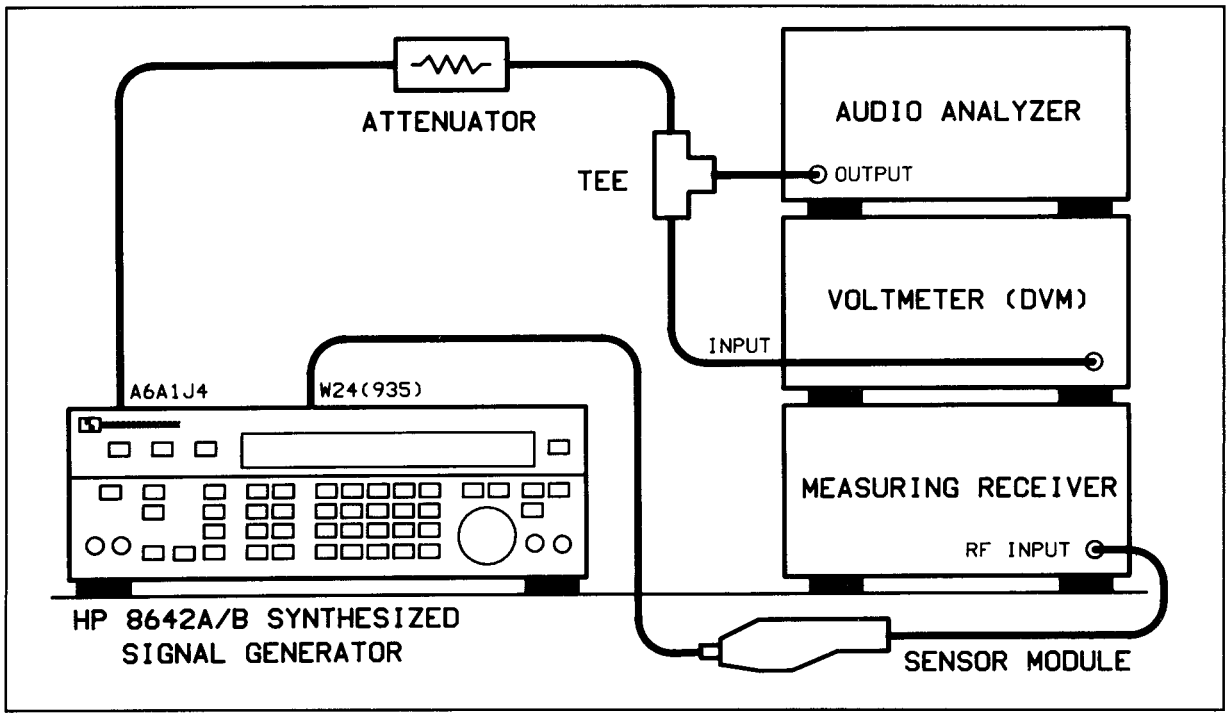


Figure 8K-10. *FM Flatness Adjustment Setup*

11. Setup:

    Connect a BNC TEE to the Audio Analyzer output.

    Connect a BNC cable between the TEE and the Digital Voltmeter.

    Connect the Attenuator between the TEE and A6A1 J4 using two BNC cables.

    For an Audio Analyzer with 50Ω source impedance set the Attenuator to 40 dB. Set the Audio Analyzer to 1 kHz and 4 volts.

    For an Audio Analyzer with 600Ω source set the Attenuator to 20 dB. Set the Audio Analyzer to 1 kHz and 2 volts.

    Set the Measuring Receiver mode to FM, and set 3 kHz low pass filter to on.

    Set the HP 8642 to EXT AC.

12. Adjust the output level of the Audio Analyzer until the Measuring Receiver reads between 13.4 kHz and 15.3 kHz. Enable DVM averaging if available.

13. Record the Digital Voltmeter reading ($DVM1$) and the Measuring Receiver reading ($FM1$) below:

$$DVM1 = \_\_\_\_V$$

$$FM1 = \_\_\_\_kHz$$

14. Set the Audio Analyzer to 20 Hz. Record the Digital Voltmeter reading ($DVM2$) below:

$$DVM2 = \_\_\_\_V$$

15. Calculate the upper (FMU) and lower (FML) limits of the desired Measuring Receiver reading as follows:

$$FMU = FM1 \times \frac{DVM2}{DVM1} \times .989 = \_\_\_\_kHz$$

$$FML = FM1 \times \frac{DVM2}{DVM1} \times .988 = \_\_\_\_kHz$$

16. Adjust R36 (FM Crossover Adjustment) for a Measuring Receiver reading within the limits computed in step 15.

17. Set the Audio Analyzer to 1 kHz. If the reading on the Measuring Receiver is between ($FM1$ + 0.05 kHz) and ($FM1$ − 0.05 kHz), then continue with ΦM Flatness. Otherwise, repeat FM Flatness Adjustment.

ΦM Flatness Adjustment

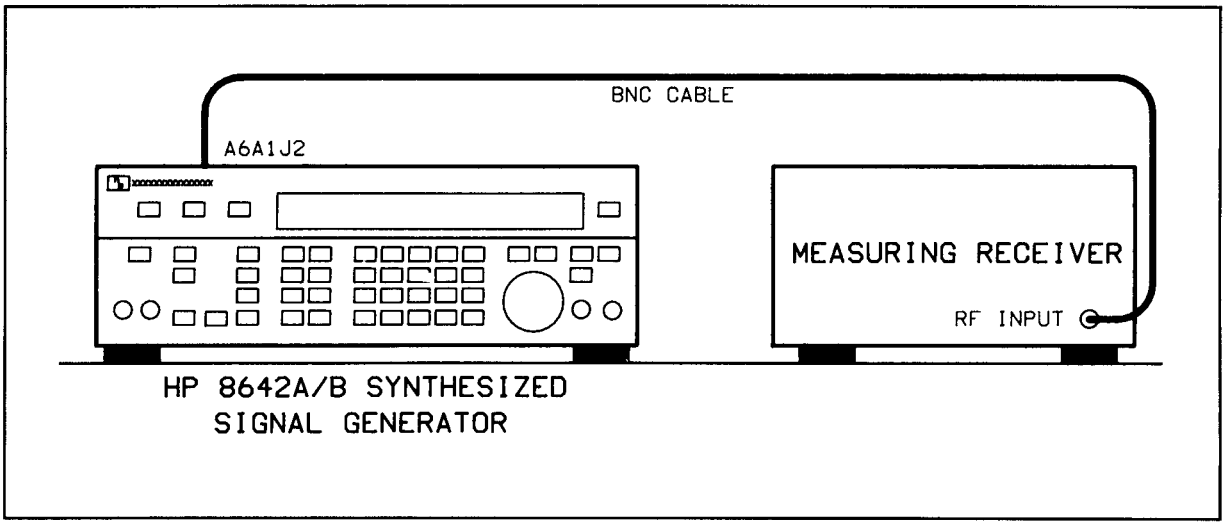


Figure 8K–11. *ΦM Flatness Adjustment Setup*

18. Setup:

    Preset the instruments.

    Connect the Measuring Receiver to A6A1 J2 .

    Set the Measuring Receiver to FM mode and Detector to Average and 3 kHz low pass filter on.

    Manually tune the Measuring Receiver to 135 MHz.

    Set the HP 8642 to FREQ 1 GHz, ΦM and 100 rad.

    Reconnect W20 to A6A1 J4.

19. Set the HP 8642 to MOD FREQ 20 Hz. Record the Measuring Receiver reading $f1$ below:

$$f1 = \_\_\_\_ \text{ kHz}$$

20. Calculate the upper $f3$ and lower $f2$ limits of the desired Measuring Receiver reading below:

$$f3 = f1 \times 50.50 = \_\_\_\_kHz$$

$$f2 = f1 \times 49.50 = \_\_\_\_kHz$$

21. Set the HP 8642 to MOD FREQ 1 kHz. Adjust R49 until the Measuring Receiver reads within $f3$ and $f2$.

22. Set the HP 8642 to MOD FREQ 20 Hz. If the Measuring Receiver reading is within ($f1 \times 1.01$) and ($f1 \times 0.99$), then reconnect all cables and continue with A6A2 Auto Adjust. Otherwise, repeat steps 19 through 22.

A6A2 AUTO-ADJUSTMENTS

Description

See Section 5 for a description of the Auto Adjustment routines. Section 5 should be read before proceeding with any auto adjustments.

Required Equipment:

Measuring Receiver	HP 8902A
Digital Voltmeter	HP 3456A
Printer	HP 2225A
Resistor	50Ω 0.5%

NOTE

See Section 5 for Alternate equipment.

1. Initialize Auto Adjustments Routine:

   Key in: [INST PRESET]

   Key in: [SHIFT] [SPCL] [3] [8] [8] [Hz] [8] [0] [Hz]

2. When **"ENTER ROUTINE NUM .G8000"** appears:

   Key in: [3] [Hz].

   Follow the prompts on the HP 8642 display to enter the Month, Day, and Year. (See Section 5 for explanation of key sequence).

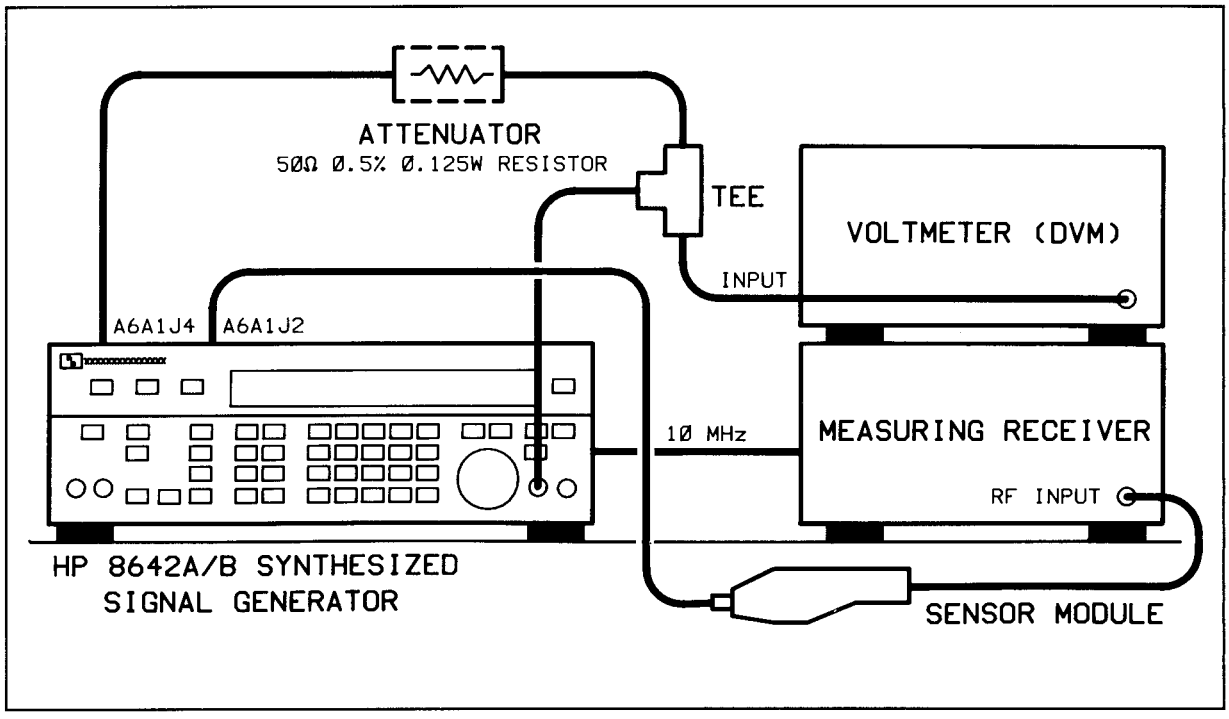


Figure 8K–12. *A6A2 Auto Adjustments Setup*

3. When **"WAITING FOR SET-UP 1 .V24"** appears:

   Connect a BNC TEE connector to the MOD OUTPUT port on the HP 8642.

   Connect a BNC cable from the TEE connector to the DVM Measurement Input.

   Set DVM to measure Volts ac.

   Connect a 50Ω , 0.5% resistor to the TEE Connector and connect a BNC cable to the other end of the resistor. (50Ω resistor is in series with the center conductor.)

   Disconnect cable W20 from the A6 module at A6A1 J4 (967).

   Connect the other end of the BNC cable to the A6 module using an adapter at A6A1 J4.

   Connect a BNC cable from the Timebase Output of the Measuring Receiver to the EXT REF input of the HP 8642.

   Disconnect cable W24 (935) from the A6 module at A6A1 J2.

   Connect the HP 11722A to the A6 Module at A6A1 J2.

   CAUTION

   Use a short piece of flexible coax cable to minimize the strain on A6A1 J2.

   Key in: [Hz] to continue.

Store Data

4. When **"UNPROTECT CAL. MEMORY .G24"** appears:

   Switch A3 S2 toward the rear of the instrument to unprotect the EEPROM's.

   Key in: [Hz] to continue.

5. When **"PROTECT CAL. MEMORY .G26"** appears:

   Switch A3 S2 towards the front of the instrument to protect the EEPROM's.

   Key in: [Hz] to continue.

6. When**"RECONNECT ALL CABLES .V29"** appears:

   Disconnect test equipment and re-install the A6 module.

   Key in: [Hz] to continue.

   Key in: [INST PRESET] and wait for "100 MZ −140 DM" to appear on the display.

   Key in: [SHIFT] [SPCL] [3] [3] [0] [Hz].

7. When **"WAITING FOR SETUP 1 .Z24"** appears:

   Connect the MOD OUT output to the AM/PULSE INPUT and FM/PM input.

   Key in: [Hz] to continue.

8. **"DIAG DONE HIT MSSGS .V1"** appears:

   Press the [MSSG] key to view the message buffer. If "NO MESSAGES .00" is contained in the message buffer, the HP 8642 is operating properly.

9. Upload Data:

Switch the HP 8642 to standby.

Remove the A20 Cal Module. (See Disassembly Procedures).

Plug the A20 Module on to A3 J3.

Switch the HP 8642 on.

Switch A20 S1 to the CHANGE position.

Key in: [SHIFT] [SPCL] [3] [7] [4] [Hz].

HP 8642A: When "08 SECTIONS STORED .U610" appears on the display, move A20 S1 up to its PROTECTED position. **HP 8642B**: When "10 SECTIONS STORED .U610" appears on the display, move A20 S1 up to its PROTECTED position.

Key in: [Hz] to end the routine.

Switch the HP 8642 to Standby.

Reconnect the A20 module to the rear panel (See Disassembly Procedures).

OPTIONAL ADJUSTMENTS

Low Distortion FM Adjustment

Required Equipment:

Measuring Receiver ..... HP 8902A
Sensor Module ..... HP 11722A
Audio Analyzer ..... HP 8903A
Spectrum Analyzer ..... HP 8566A

1. Setup:

   Disconnect W24 from A11A1 J3. Connect W24 to the Sensor Module. Connect the FM output of the Measuring Receiver to the Audio Analyzer and the Oscilloscope. Connect the monitor output of the Audio Analyzer to the Spectrum Analyzer. Setup the instruments as follows:

   HP 8642:

   Key in: INST PRESET

   Mod Frequency ..... 1 kHz
   FM (Deviation) ..... 100 kHz

   Measuring Receiver:

   Measurement Mode ..... FM

   Audio Analyzer:

   Measurement Mode ..... AC
   Post Notch Gain ..... 0 dB*

   Spectrum Analyzer:

   Span ..... 100 Hz
   Center Frequency ..... 1 kHz
   Resolution Bandwidth ..... 10 Hz
   Reference Level ..... 10 dBm

2. Rotate R71 and R75 fully clockwise.

   If the Measuring Receiver deviation is less than *Dref*, adjust R71 counter clockwise until the deviation equals *Dref*.

   If the Measuring Receiver deviation is greater than *Dref*, adjust R75 counter clockwise until the deviation equals *Dref*.

3. Adjust R71 enough to increase the deviation about 2 kHz. Adjust R75 clockwise until the deviation is again equal to *Dref*.

   Observe the level of the second harmonic on the Spectrum Analyzer.

4. Repeat step 5 until a minimum of the second harmonic is reached while maintaining a constant deviation.

*On the HP 8903, enter 3.1 SPCL.

NOTE

As a second harmonic minimum is approached it is recommended that deviation changes made (by adjusting R71) be reduced to 0.3 – 0.8 kHz.

5. After a second harmonic null has been reached, record the second Harmonic Amplitude measurement *Aharm* on the Spectrum Analyzer:

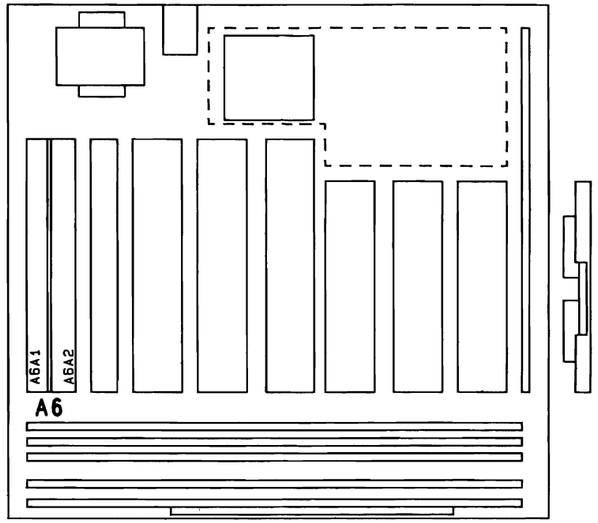
$$Aharm = \_\_\_\_dBm$$

6. Verify the adjustment by calculating the distortion (*Dist*) as follows:

$$Dist = Aharm - Aref - 40 = \_\_\_\_dB$$

The distortion (*Dist*) should be less than −70 dB.

Assembly Locator



Simplified Block Diagram

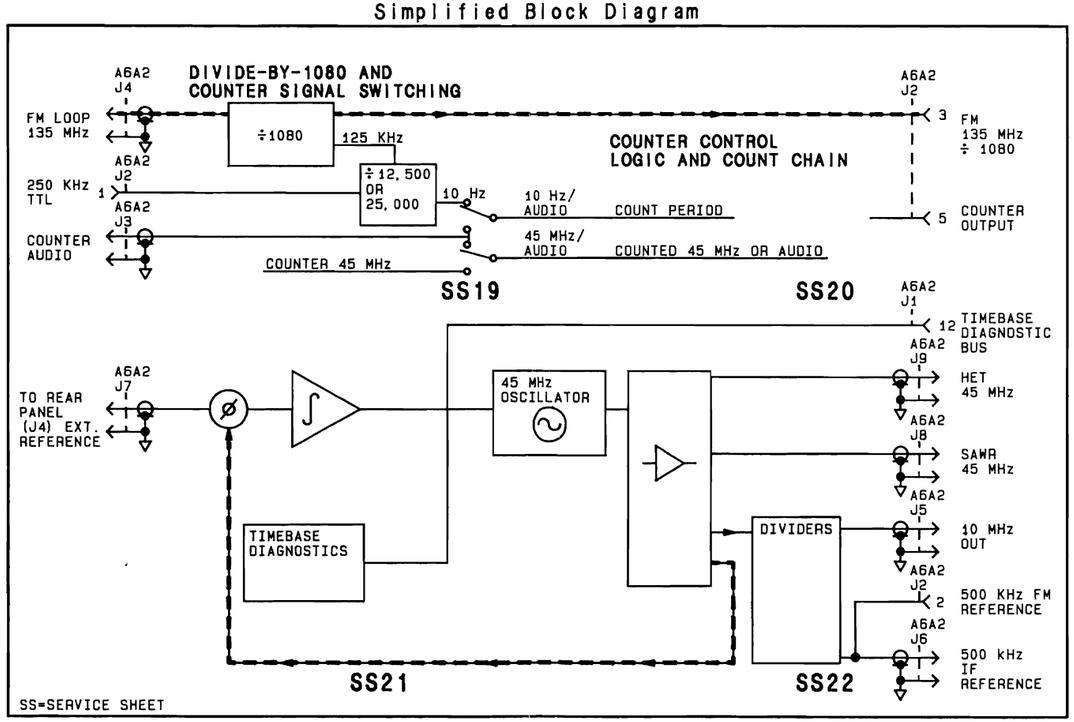
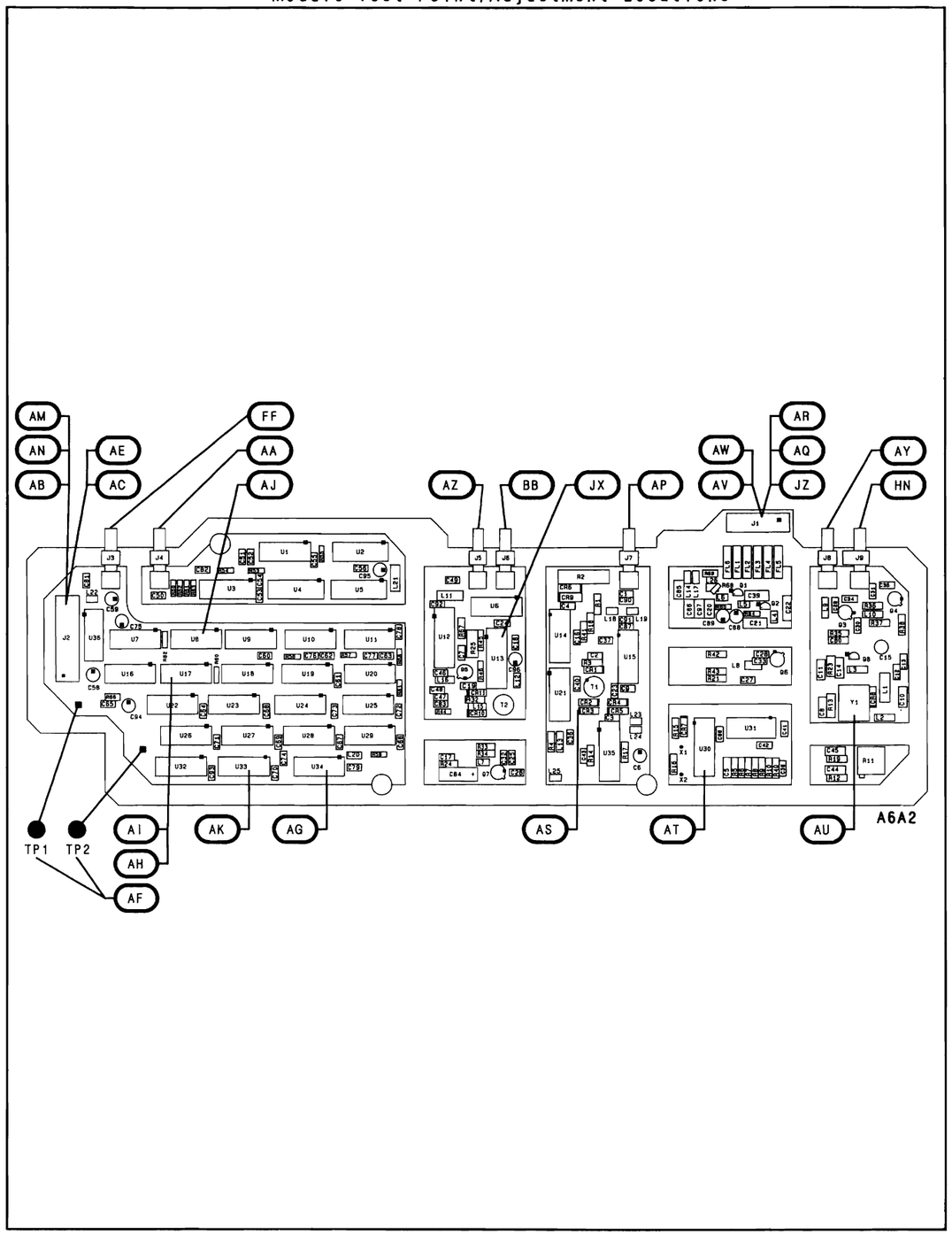


Figure 8K-100 BD7 General Information.

Module Test Point/Adjustment Locations



A6A2 COUNTER/TIMEBASE ASSEMBLY (08642-60102)

TAKE READING STROBE
BD8 AM 2
P/O J2

FM LOOP 135 MHz
BD8 AA
A6 W1 93
J4

250 KHz TTL
BD8 AB 1
P/O J2

COUNTER SELECT LINES
BD8 AC 2 9 COUNT PERIOD SELECT
8 COUNTED SIGNAL SELECT

COUNTER AUDIO
BD6 FF
W21 93
J3

POWER SUPPLY LINES
BD8 AE 3
P/O J2
4 +5V (F3)
10 -5V (F2)
12 GND

COUNTER CLOCK
BD8 AN 6

DIVIDE-BY-1080

NARROW PULSE 125 kHz

DIVIDE-BY-12,500 OR 25,000

DIVIDER ENABLE

COUNT PERIOD SELECT

COUNT PERIOD 10 Hz OR AUDIO

AI

AJ

AH

AK

COUNTED SIGNAL SELECT

COUNTED 45 MHz OR AUDIO

COUNTER 45 MHz

RF TO TTL TRANSLATION

POWER SUPPLY AND GND
2 AF 20

SS19

AG

TO REAR PANEL (J4) EXTERNAL REFERENCE
BD17 AP
W27 907
J7

COMPARATOR

PULSE GENERATOR

PHASE DETECTOR

INTEGRATOR

AT

OSCILLATOR DISABLE

LOW-PASS FILTER

TUNE VOLTAGE

TIMEBASE DISABLE
BD4 AQ 8
P/O J1

TB POWER SUPPLY AND GROUND
JZ 4
2 +15V
1 +5V
4 -15V
3, 5, 7, 9, 10, 11, 13, 14 GND

POWER SUPPLY AND GND
5 AR 22

EXTERNAL REFERENCE DETECTOR

EXT REF SENSE
P/O J1 6
AV BD4

AU

TIMEBASE DIAGNOSTICS

OOL SENSE
12
TIMEBASE DIAGNOSTIC BUS
AW BD4

AS

JX

SS21

DIVIDER DISABLE

SERIAL PREFIX: 2427A

500

AI

AJ

COUNT PERIOD SELECT

COUNT PERIOD 10 Hz OR AUDIO

AH

ED

COUNTED 45 MHz OR AUDIO

AK

SS19

CONTROL LOGIC

COUNT GATE

2

24 BIT COUNT CHAIN

SERIAL DATA OUT SWITCH

COUNTER CLOCK

19 AF 2

POWER SUPPLY AND GND

+5V (F3)
GND

COUNTER 45 MHz

AG

INTEGRATOR

45 MHz OSCILLATOR

BUFFER AMPLIFIERS

AT

OSCILLATOR DISABLE

LOW-PASS FILTER

TUNE VOLTAGE

P/O J1

EXT REF SENSE

6

AV BD4

EXT REF SENSE

AU

TIMEBASE DIAGNOSTICS

OOL SENSE

12

TIMEBASE DIAGNOSTIC BUS

AW BD4

AS

SS21

JX

21 AR 5

POWER SUPPLY AND GND

+15V (F1)
+5V (F2)
-15V (F1)
-15V (F4)
GND

DOUBLER

90 MHz BAND PASS AMPLIFIER

DIVIDE-BY-9

TTL BUFFER

DIVIDE-BY-20

DIVIDER DISABLE

PHASE DETECTOR INPUT

DIVIDER DISABLE

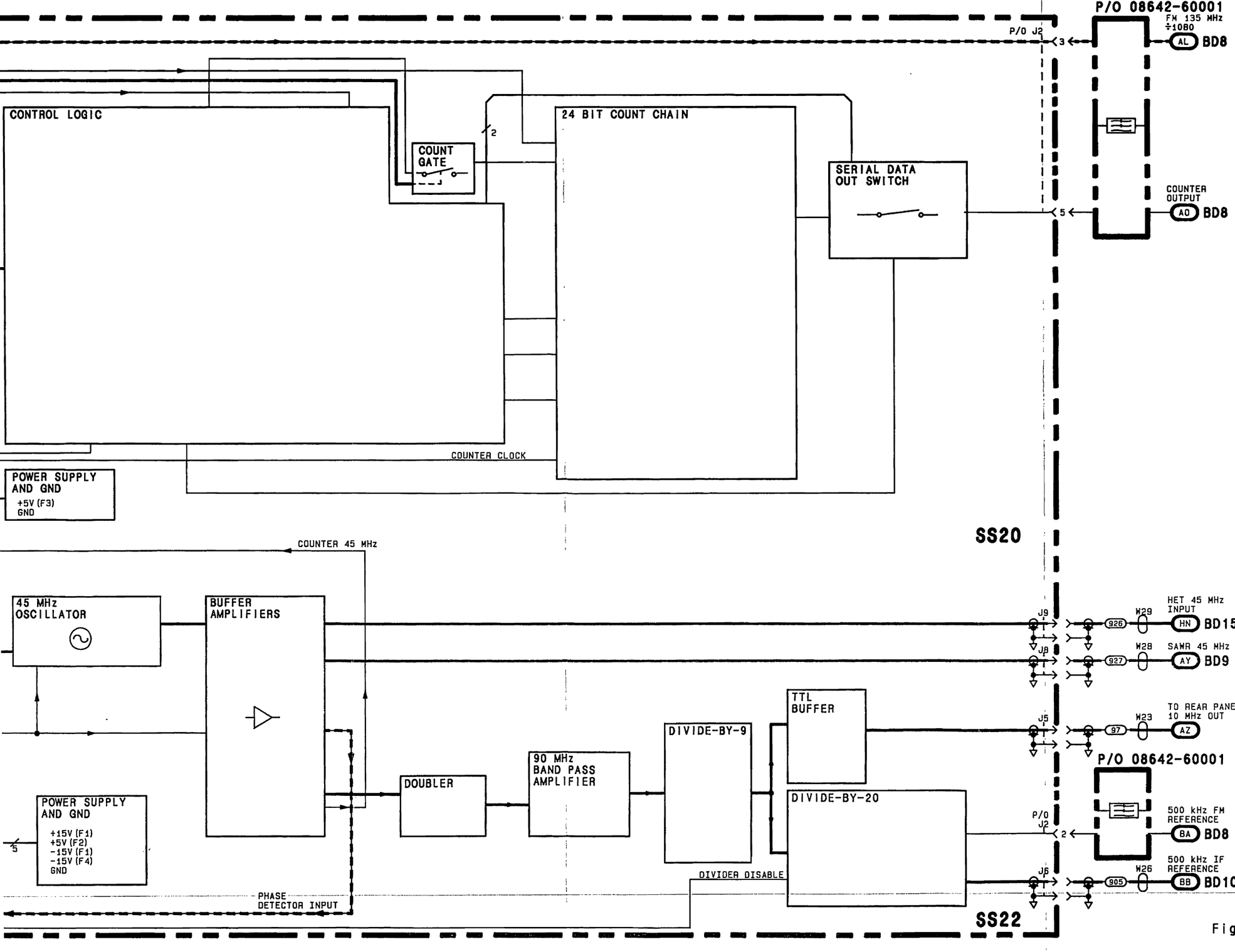
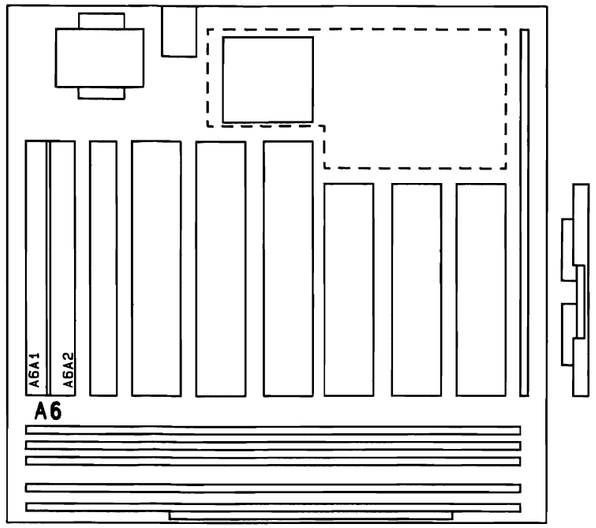


Figure 8K-101
8K-101

Assembly Locator



Simplified Block Diagram

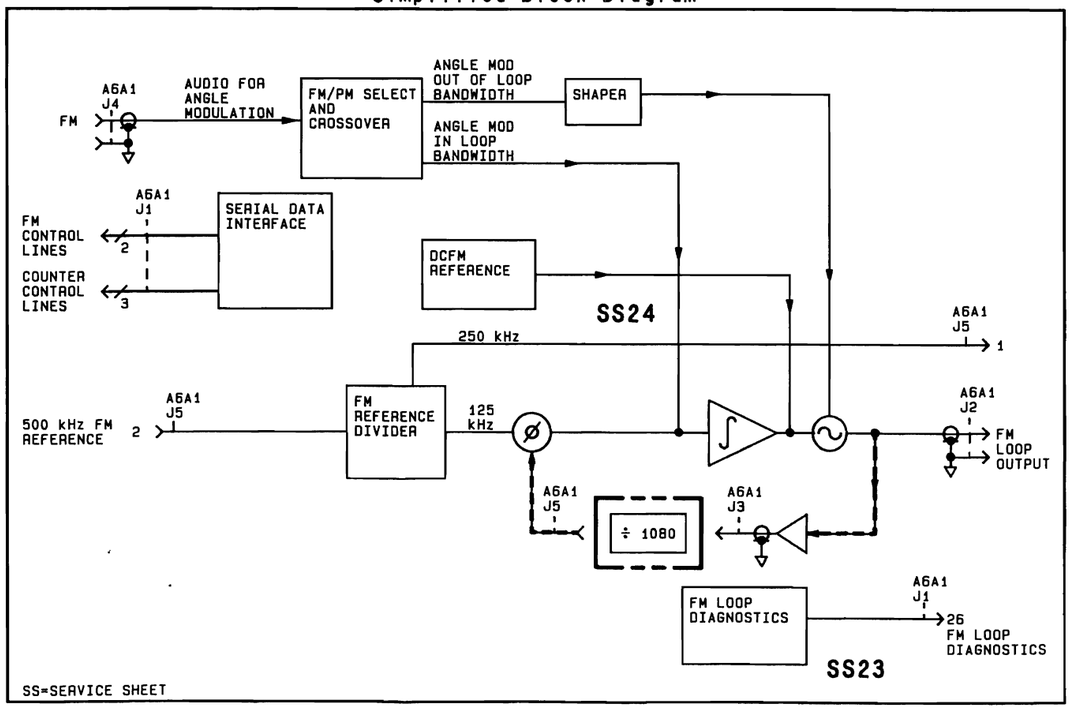
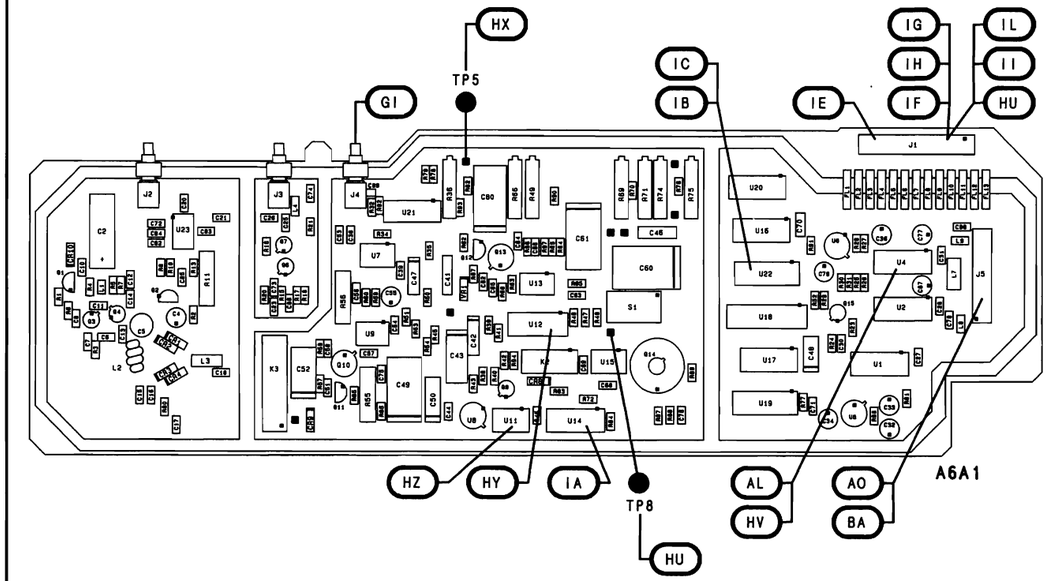


Figure 8K-102 BD8 General Information.

P/O A6 MODULE **BD 7**

SEE REVERSE SIDE

Module Test Point/Adjustment Locations



A6A1 FM VCO ASSEMBLY (08642-60101)

FM
BD5 (GI) W20 (967) J4

FM CONTROL LINES
BD4 (IF) 2 → 23 P/O J1 FM CLK
→ 25 FM DATA

COUNTER CONTROL LINES
BD4 (IG) 3 → 13 COUNT PERIOD SELECT
→ 15 COUNTED SIGNAL SELECT
→ 17 TAKE READING STROBE

COUNTER CLOCK
BD4 (IH) → 19 COUNTER CLK

COUNTER OUTPUT
BD7 (A0) → 5 P/O J5

LOW-PASS FILTER

AUDIO FOR ANGLE MODULATION

SERIAL DATA INTERFACE

MUX SELECT LINES (3)
FM LOOP DISABLE
DCFM SELECT

COUNTER OUTPUT (4)

POWER SUPPLY AND GROUND
23 (HU) 5
+50V (F1)
+15V (F1)
+5V (F1
-15V (F1)
GND
-5V (F1)
+5V (F3)
GND (3)

PHASE MODULATION SELECT
PM IN BW
PM OUT BW
dv/dt

FM OUT BW

VREF

FM/PM LINE SELECT
ANGLE MOD OUTSIDE BW
ANGLE MOD INSIDE BW

SHAPER

FM CROSSOVER
FM IN BW
FM IN BW

DCFM REFERENCE

HZ HV IB

500 kHz FM REFERENCE
BD7 (BA) → 2 P/O J5 500 kHz FM REFERENCE

POWER SUPPLY AND GROUND
64 (TL) 6
P/O J1
1 +50V
2, 3, +15V
4
5, 6, +5V
7
8, 9
10 -5V
11 -15V
12
14 GND
16
18
20
22
24

SERIAL PREFIX: 2427A

PM IN BW

PM OUT BW

FM/PM
LINE SELECT

VREF

ANGLE MOD
OUTSIDE BW

ANGLE MOD
INSIDE BW

SHAPER

MOD SIGNAL
SENSE LINE

ANGLE MOD
OUTSIDE BW

IA

HY

HX

FM
IN BW

DCFM REFERENCE

SS24

DCFM
REF VOLTAGE
(+40 Vdc)

250 kHz

FM REFERENCE
DIVIDER

125 kHz

PHASE DETECTOR

ANGLE MOD
INSIDE BW

DCFM
REF VOLTAGE
(+40 Vdc)

INTEGRATOR

VOLTAGE CONTR
OSCILLATOR

125 kHz

FM LOOP DISABLE

DCFM SELECT

500 kHz FM
REFERENCE

P/O A6A2 COUNTER/TIMEBASE
ASSEMBLY (08642-60102)

FM 135 MHz
÷ 1080

AL BD7

BD7 AA

FM LOOP
135 MHz

P/O
J5

J3

135 MHz

125 kHz

ISOLATION
AMPLIFIER

OUT-OF-LOCK
DETECTOR

POWER SUPPLY
AND GROUND

5

HU 24

5

MOD SIGNAL SENSE LINE

IA

IC

HY

ANGLE MOD OUTSIDE BW

J5 1

1

250 kHz TTL

AB BD7

250 kHz

FM REFERENCE DIVIDER

PHASE DETECTOR

ANGLE MOD INSIDE BW

INTEGRATOR

VOLTAGE CONTROLLED OSCILLATOR

POWER SPLITTER

125 kHz

DCFM REF VOLTAGE (+40 Vdc)

J2 1

935 W24

FM LOOP OUTPUT

CU

125 kHz

DCFM SELECT

P/O 08642-60001

FM LOOP DISABLE

P/O A6A2 COUNTER/TIMEBASE ASSEMBLY (08642-60102)

FM 135 MHz ÷ 1080

AL BD7

BD7 FM LOOP 135 MHz AA

P/O J5

J3

135 MHz

ISOLATION AMPLIFIER

OUT-OF-LOCK DETECTOR

COUNTED PERIOD SELECT

COUNTED SIGNAL SELECT

TAKE READING STROBE

COUNTER CLK

+5V (F3)

GND

-5V (F1)

P/O J5

9

8

7

6

12

10

4

COUNTER SELECT LINES

AC BD7

TAKE READING STROBE

AM BD7

COUNTER CLK

AN BD7

POWER SUPPLY LINES

AE BD7

POWER SUPPLY AND GROUND

HU 24

5

5

MOD SIGNAL SENSE LINE

VCO TUNE VOLTAGE SENSE

MUX SELECT LINES

FM LOOP DIAGNOSTICS INTERFACE

SS23

FM LOOP DIAGNOS. BUS

P/O J1

26

FM LOOP DIAGNOSTICS BUS

IE BD4

COUNTER OUTPUT

21

COUNTER OUTPUT

IL BD4

BD8

Figure 8K-103

8K-103

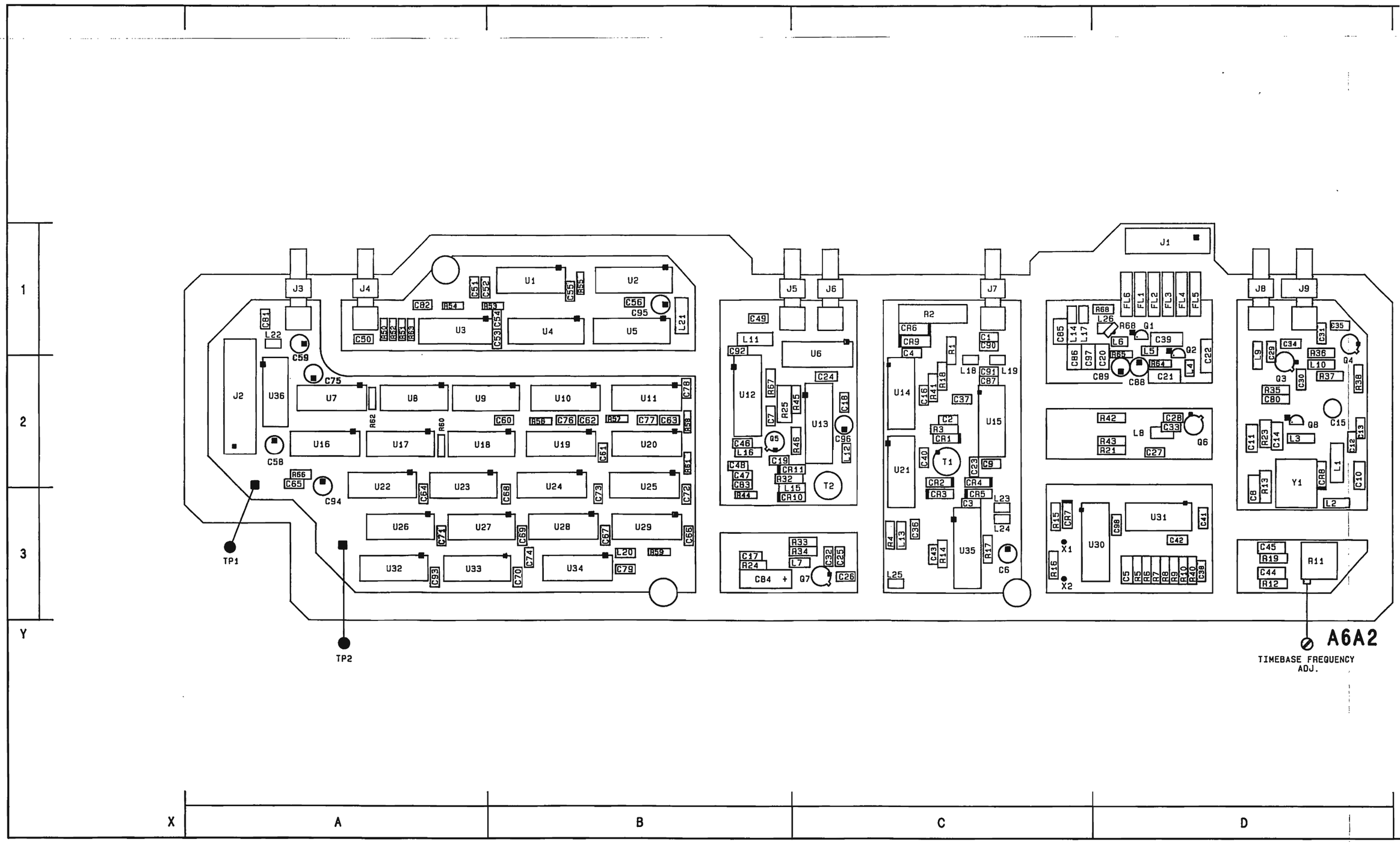
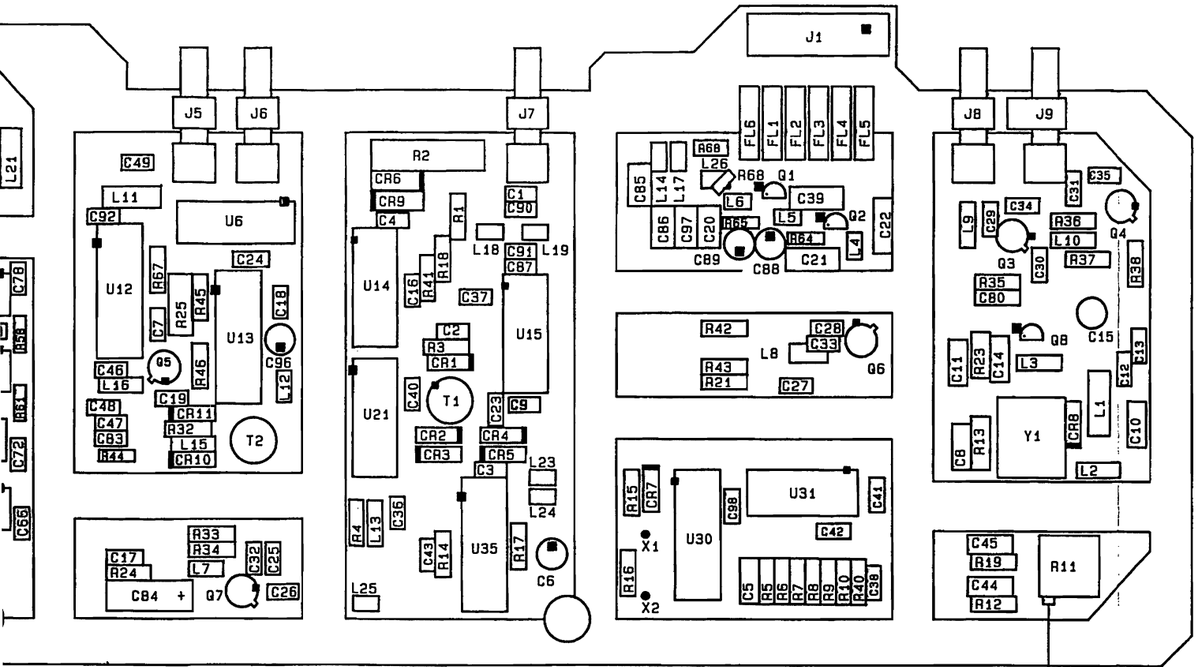


Figure 8K-104. SERVICE SHEET 19 INFORMATION

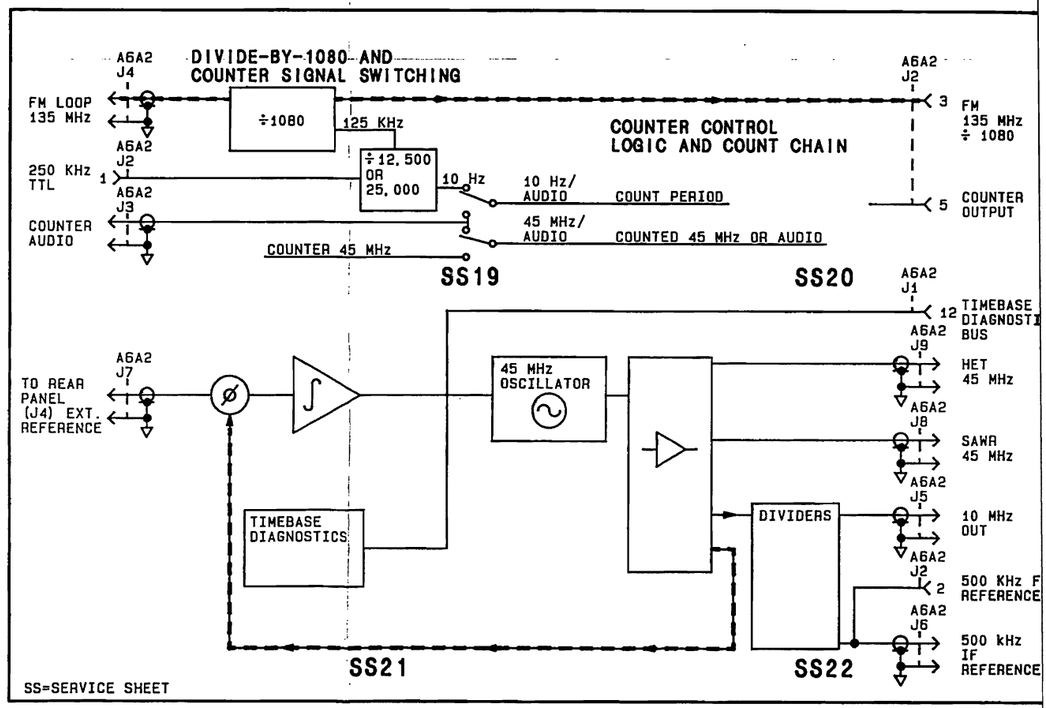
Component Locator



C

D

Component Locator



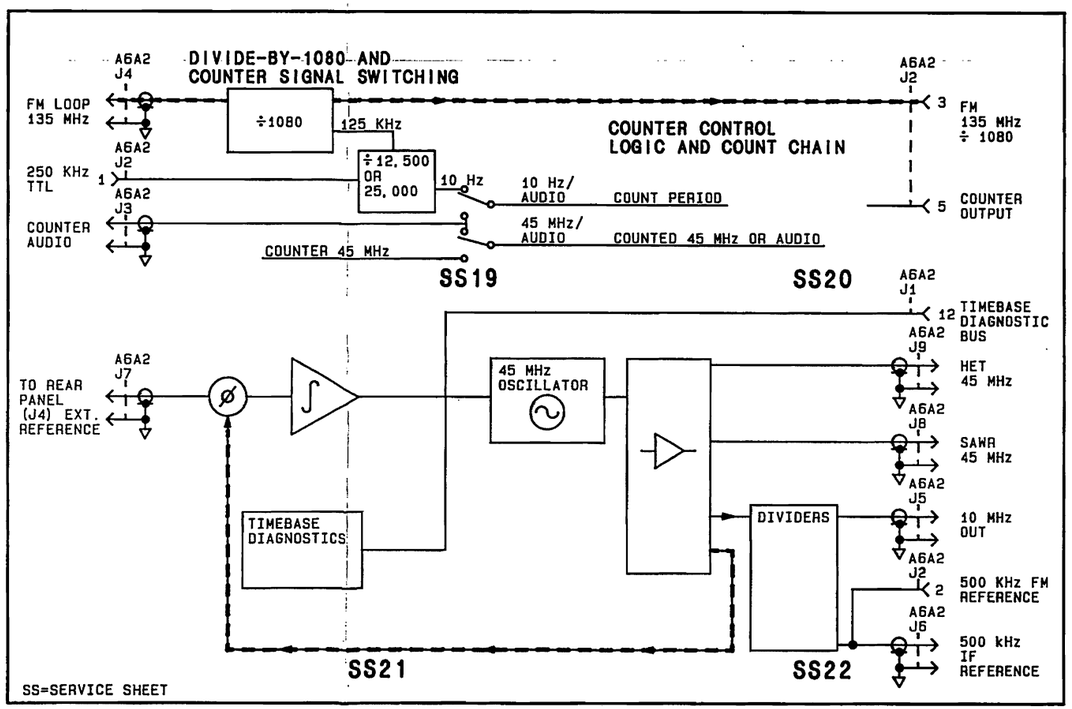
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C50	A, 1	TP1	A, 2														
C51	A, 1	TP2	A, 3														
C52	A, 1																
C53	B, 1	U1	B, 1														
C54	B, 1	U2	B, 1														
C55	B, 1	U3	A, 1														
C56	B, 1	U4	B, 1														
C58	A, 2	U5	B, 1														
C59	A, 1	U7	A, 2														
C64	A, 3	U16	A, 2														
C70	B, 3	U17	A, 2														
C74	B, 3	U18	A, 2														
C79	B, 3	U22	A, 2														
C81	A, 1	U32	A, 3														
C82	A, 1	U33	A, 3														
C93	A, 3	U34	B, 3														
C95	B, 1	U36	A, 2														
J2	A, 2																
J3	A, 1																
J4	A, 1																
L20	B, 3																
L21	B, 1																
L22	A, 1																
R50	A, 1																
R51	A, 1																
R52	A, 1																
R53	B, 1																
R54	A, 1																
R55	B, 1																
R59	B, 3																
R60	A, 2																
R63	A, 1																

P/O A6 MODULE **BD8**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C50	A, 1	TP1	A, 2												
C51	A, 1	TP2	A, 3												
C52	A, 1														
C53	B, 1	U1	B, 1												
C54	B, 1	U2	B, 1												
C55	B, 1	U3	A, 1												
C56	B, 1	U4	B, 1												
C58	A, 2	U5	B, 1												
C59	A, 1	U7	A, 2												
C64	A, 3	U16	A, 2												
C70	B, 3	U17	A, 2												
C74	B, 3	U18	A, 2												
C79	B, 3	U22	A, 2												
C81	A, 1	U32	A, 3												
C82	A, 1	U33	A, 3												
C93	A, 3	U34	B, 3												
C95	B, 1	U36	A, 2												
J2	A, 2														
J3	A, 1														
J4	A, 1														
L20	B, 3														
L21	B, 1														
L22	A, 1														
R50	A, 1														
R51	A, 1														
R52	A, 1														
R53	B, 1														
R54	A, 1														
R55	B, 1														
R59	B, 3														
R60	A, 2														
R63	A, 1														

P/O A6 MODULE **BD8**

SEE REVERSE SIDE

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

CHANGES

All Serial Prefixes

On the schemat1

- In the right hand portion of **DIVIDE-BY-1080**, locate U5 and remove the active low indicator from the input line labeled pin number 14.

- In the left portion of **DIVIDE-BY-12,500 OR 25,000**, next to U18B, remove (NOTE). Also, in U22A remove the active low indicator from the input line labeled pin number 2. Do the same for U22B pin14, U32A pin 2, and U32B pin 14.

2714A and above

On the Component Locator:

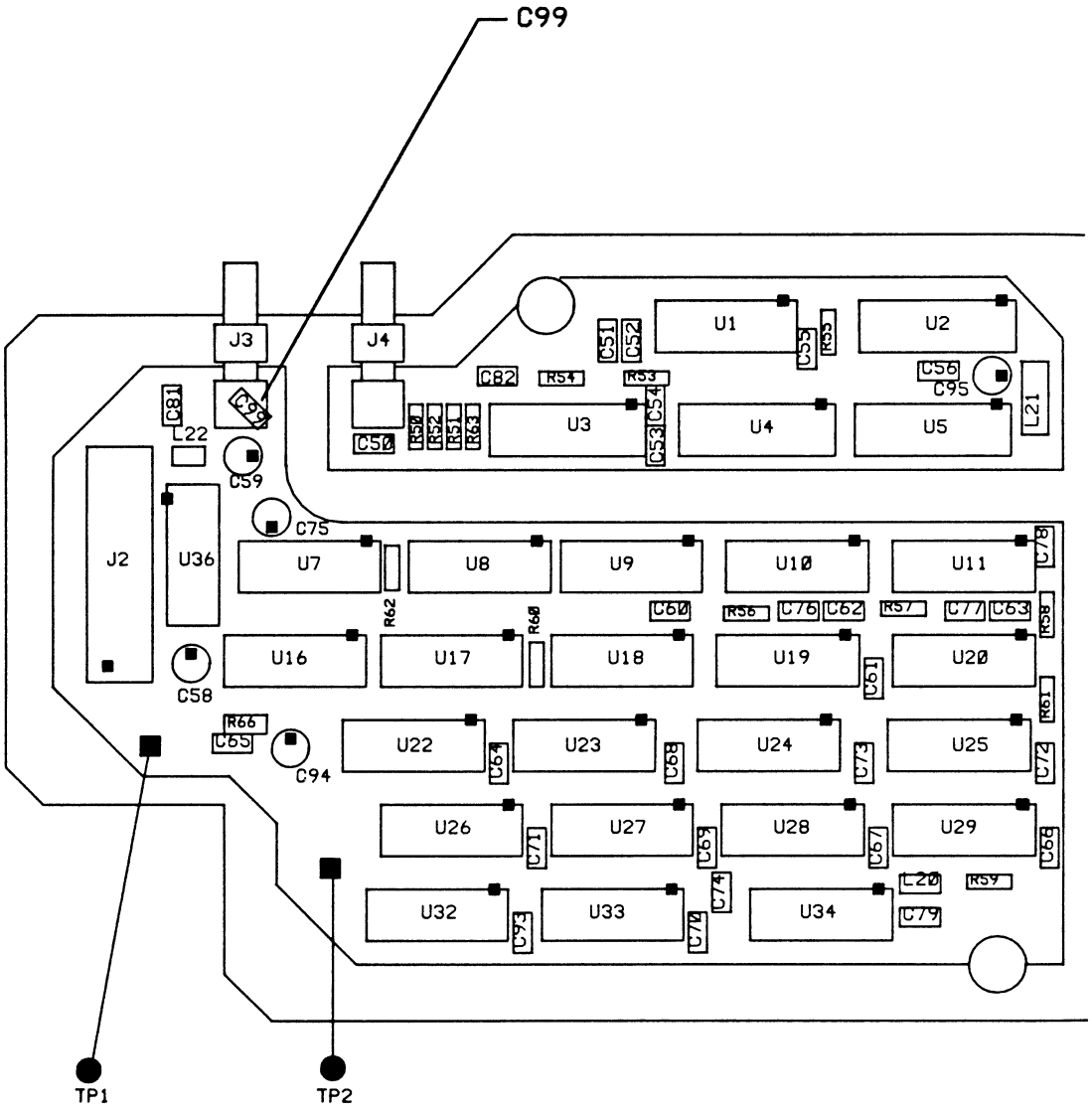
- C99 - Use the compon nt locator with the partial component locator on page 8K-104.3.

On the Component Coordinates:

- C99 Add C99 A,1, to the component coordinates.

On the schematic:

- C99 - On the left hand side of the schematic, locate J3 and to the right of J3 add C99, 100p from the main line to ground.



CHANGES TO FIGURE 8K-104 (2714A AND ABOVE)

P/O A6A2 COUNTER/TIMEBASE ASSEMBY (08642-60102)

DIVIDE-BY-1080

DIVIDE-BY-2

ECL TO TTL TRANSLATOR

DIVIDE-BY-4

DIVIDE-BY-9

DIVIDE-BY

FM LOOP 135 MHz 23 AA — A6W1 — 94 — J4

C50 1000p

R50 511

R51 1470 — -5V (F3)

R52 51.1

C82 0.01µ

R63 51.1

U3

R53 316

R54 100 — -5V (F2)

C52 0.1µ

+5V (F4)

C53 0.1µ

U4

C51 0.1µ — -5V (F3)

C54 0.1µ — -5V (F3)

R55 1k

U1

C55 0.1µ

U2

C56 0.1µ

U5

250 KHz TTL 23 AB — P/O J2 — 1

COUNTER SELECT LINES 24 AC — 2

9 — COUNT PERIOD SELECT

8 — COUNTED SIGNAL SELECT

COUNTER AUDIO 14 FF — W21 — 93 — J3

POWER SUPPLY AND GND

TP2

TP1

L21 15 µ

L22 15 µ

C58 33 µ

C95 33 µ

C81 0.01µ

C59 33 µ

J2

4 — +5V (F3) — +5V (F4)

10 — -5V (F2) — -5V (F3)

12 — GND

POWER SUPPLY LINES 24 AE — 3

POWER SUPPLY AND GROUND AF 20 — 2

RF TO TTL TRANSLATION

COUNTER 45 MHz 22 AG

C79 1000p

L20

R59 61.9

U34

C74 0.1µ — -5V (F3)

SERIAL PREFIX: 2427A

VIDE-BY-4

DIVIDE-BY-9

DIVIDE-BY-15

NARROW PULSE 125 kHz

+5V (F4)

C55 0.1µ

C56 0.1µ

U2 VCC CTRDIV16

M1 [LOAD]
M2 [COUNT]
M3 [UP]
M4 [DOWN]
G5
G6
2, 3, 5, 6+/C7
2, 4, 5, 6-
1, 7D
3, 5CT=15
4, 5CT=0
[1] [2] [4] [8]

U5 VCC CTRDIV10

G1
M2 [DOWN] 2 (CT=0) Z6
M3 [UP] 3 (CT=15) Z6
1, 2-/1, 3+
G4
C5
6, 1, 4
5D [1] +-1 [2] [4] [8]

NC

DIVIDER ENABLE
20 AH

125 kHz

DIVIDE-BY-12,500 OR 25,000

DIVIDE BY 12,500 SELECT

+5V (F3)

R60 1k

U17 CTR
C1
CT=0
DIV 2
1D
DIV 5
1CT CT

U18B (NOTE)
U18C
U18D
U7D

U22A VCC CTR CT=0 DIV 2 DIV 5 CT

C64 0.1µ

U22B CTR CT=0 DIV 2 DIV 5 CT

U32A VCC CTR CT=0 DIV 2 DIV 5 CT

C93 0.1µ

U32B CTR CT=0 DIV 2 DIV 5 CT

COUNT PERIOD SELECT

COUNTED SIGNAL SELECT

AUDIO

U36D
U33D
U33C
U16D
U33A

C70 0.1µ

AUDIO

45 MHz

RF TO TTL TRANSLATION

COUNTER 45 MHz
22 AG

C79 1000p

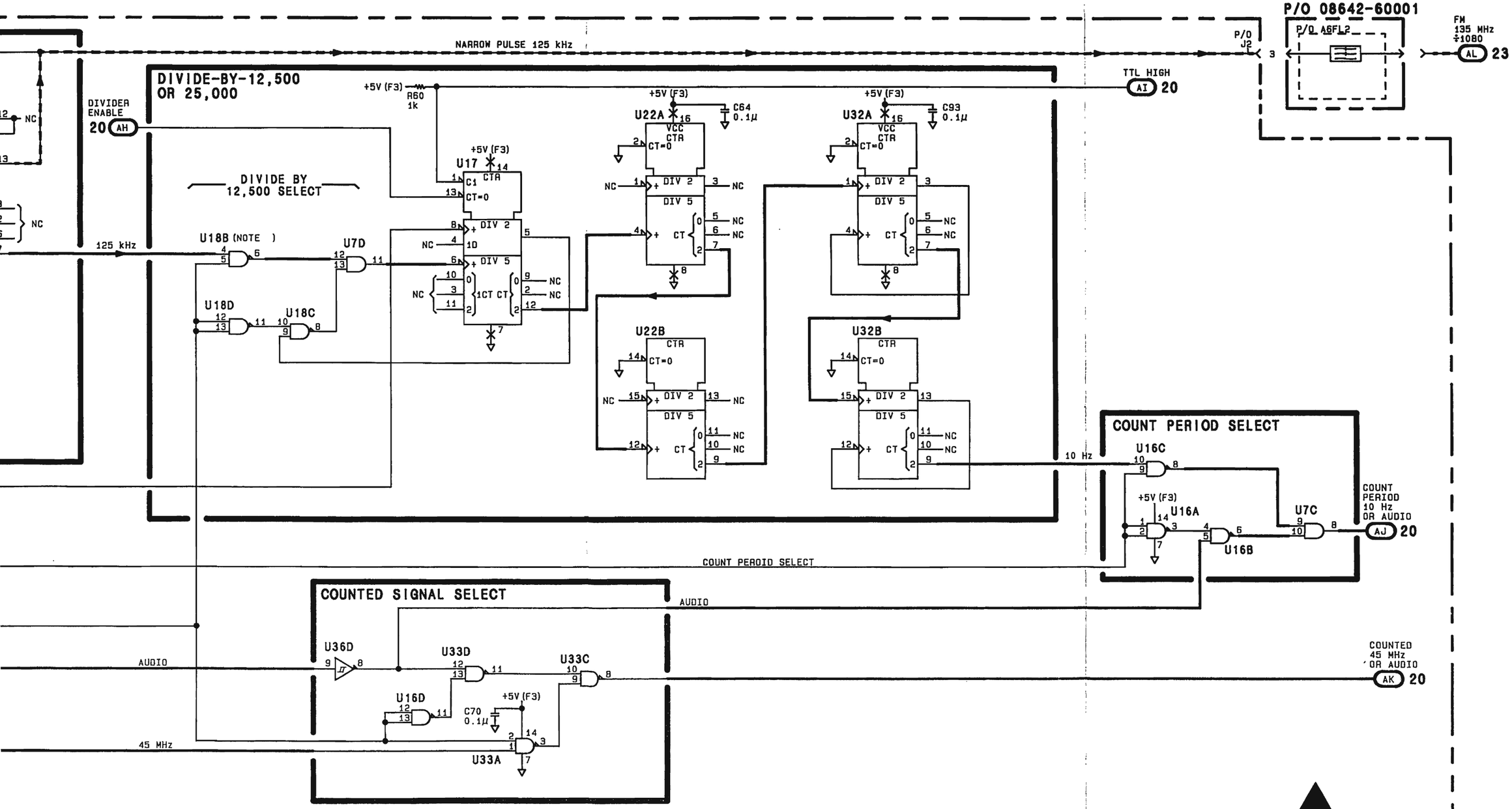
L20

R59 61.9

U34 VCC ECL/TTL VREF VEE

C74 0.1µ

-5V (F3)



SS19
Figure 8K-105
8K-105

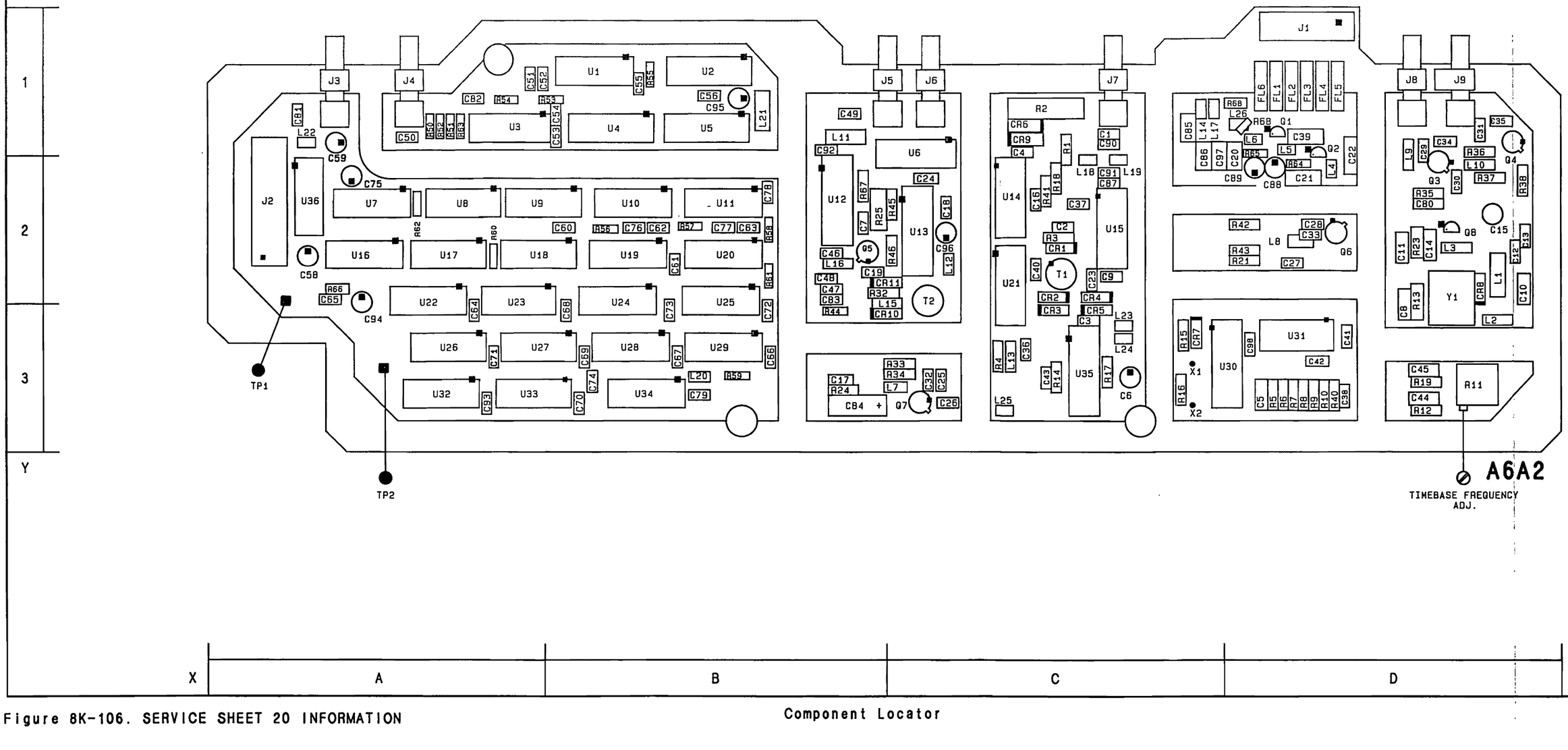
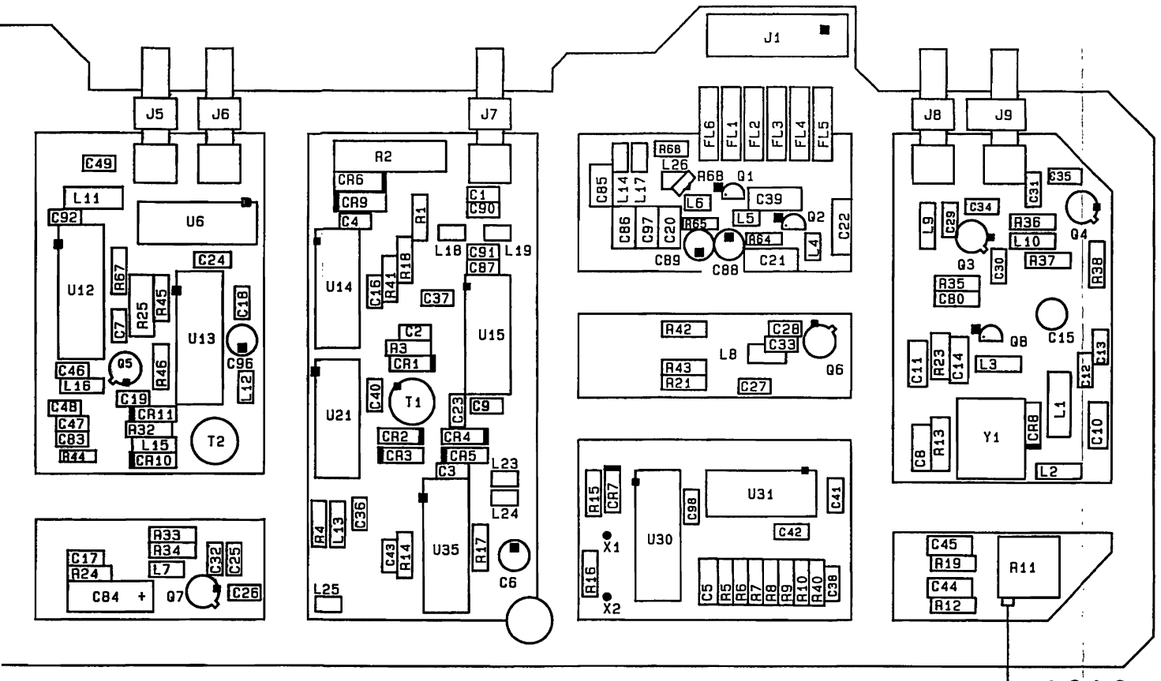


Figure 8K-106. SERVICE SHEET 20 INFORMATION

Component Locator

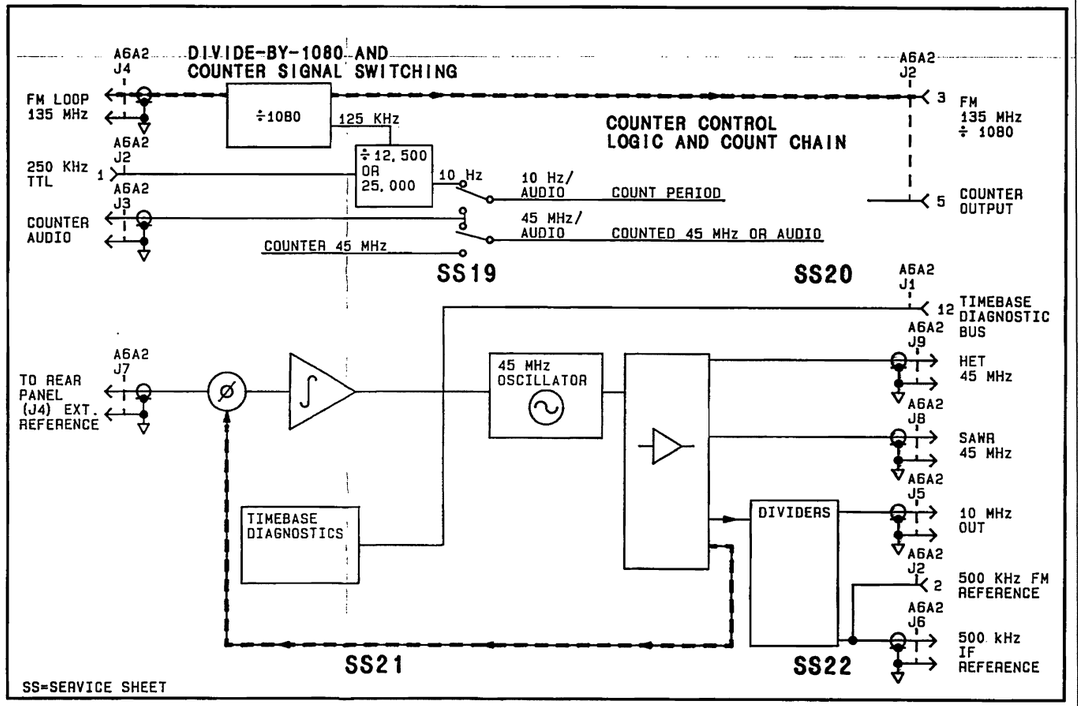


A6A2

TIMEBASE FREQUENCY ADJ.

C D

Component Locator



Reference Block Diagram

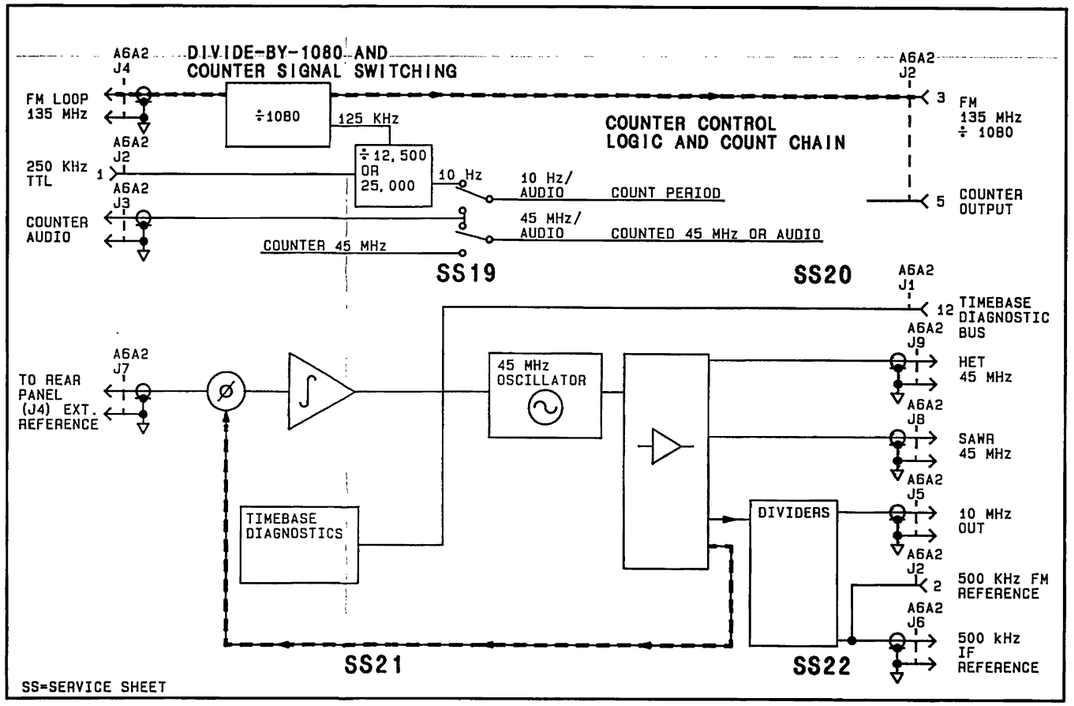
Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C60	B, 2	U25	B, 2												
C61	B, 2	U26	A, 3												
C62	B, 2	U27	A, 3												
C63	B, 2	U28	B, 3												
C65	A, 2	U29	B, 3												
C66	B, 3	U33	A, 3												
C67	B, 3	U36	A, 2												
C68	B, 3														
C69	B, 3														
C71	A, 3														
C72	B, 3														
C73	B, 3														
C75	A, 2														
C76	B, 2														
C77	B, 2														
C78	B, 2														
C94	A, 3														
J2	A, 2														
R56	B, 2														
R57	B, 2														
R58	B, 2														
R61	B, 2														
R62	A, 2														
R66	A, 2														
U7	A, 2														
U8	A, 2														
U9	A, 2														
U10	B, 2														
U11	B, 2														
U18	A, 2														
U19	B, 2														
U20	B, 2														
U23	A, 2														
U24	B, 2														

SEE REVERSE SIDE

P/O A6A2 COUNTER/ TIMEBASE ASSEMBLY

SS19



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C60	B, 2	U25	B, 2												
C61	B, 2	U26	A, 3												
C62	B, 2	U27	A, 3												
C63	B, 2	U28	B, 3												
C65	A, 2	U29	B, 3												
C66	B, 3	U33	A, 3												
C67	B, 3	U36	A, 2												
C68	B, 3														
C69	B, 3														
C71	A, 3														
C72	B, 3														
C73	B, 3														
C75	A, 2														
C76	B, 2														
C77	B, 2														
C78	B, 2														
C94	A, 3														
J2	A, 2														
R56	B, 2														
R57	B, 2														
R58	B, 2														
R61	B, 2														
R62	A, 2														
R66	A, 2														
U7	A, 2														
U8	A, 2														
U9	A, 2														
U10	B, 2														
U11	B, 2														
U18	A, 2														
U19	B, 2														
U20	B, 2														
U23	A, 2														
U24	B, 2														

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
3. A6FL2 is an array of feedthrough filters passing through the center of the module to make connections between two (2) printed circiut boards.

SEE REVERSE SIDE

P/O A6A2 COUNTER/ TIMEBASE ASSEMBLY **SS19**

Schematic General Information

CHANGES

All Serial Prefixes

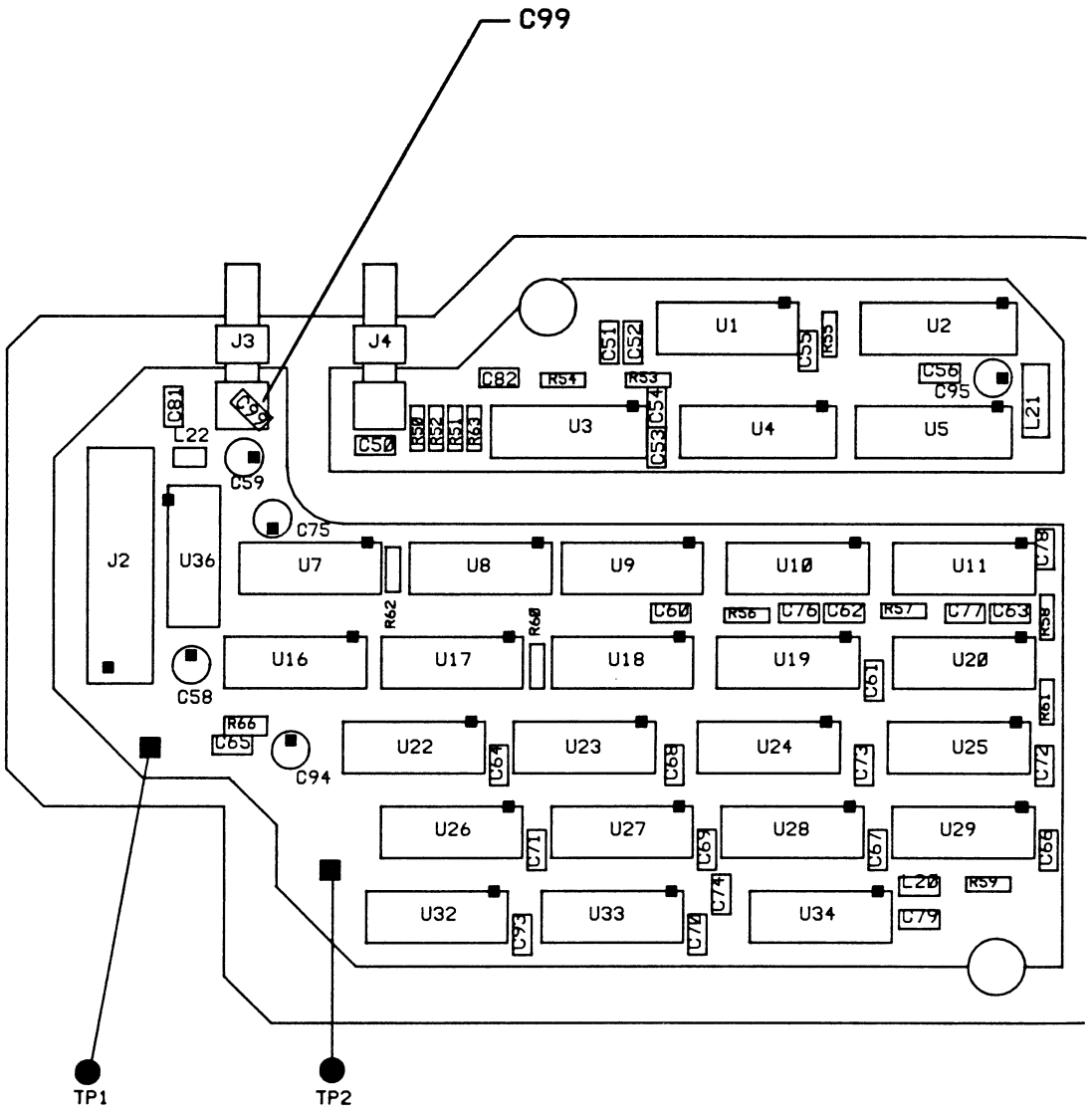
On the schematic:

- In the extreme left portion of **CONTROL LOGIC** locate U7B and remove the active low indicator from the output line labeled pin 6.

2714A and above

On the Component Locator:

- C99 - Use the component locator with the partial component locator on page 8K-106.3.



CHANGES TO FIGURE 8K-106 (2714A AND ABOVE)

P/O A6A2 COUNTER/TIMEBASE ASSEMBLY (08642-60102)

TAKE READING STROBE
24 AM

P/O J2

CONTROL LOGIC

+5V (F3)
R66 42.2
C65 0.1µ
C94 1µ
U18A
INT ENABLE/READ

EDGE LATCH
COUNT PERIOD 10 Hz OR AUDIO
19 AJ
U8B
+5V (F3)
R62 10k
C75 1µ
U7B

FLIP-FLOPS
U9A
C60 0.1µ
U19D
U9B
U19C
U9C
U19B
U9D
U19A
+5V (F3)
C61 0.1µ

COUNT PERIOD

ONE SHOTS
+5V (F3)
U10
C62 0.1µ
+VCC
C76 820p
R56 9090
CX
RX/CX
NC
U11
C63 0.1µ
C77 820p
R57 9090
13 LOAD 1
4 LOAD (L)
C78 820p
R58 9090
LOAD 1
5 CLEAR
12 CLEAR (L)

COUNTED 45 MHz OR AUDIO
19 AK
COUNT GATE
U33B

+5V (F3)
R61 1k
U36A
U36B
U8A
U7A

COUNTER CLOCK
24 AN
P/O J2

POWER SUPPLY AND GND
POWER SUPPLY AND GROUND
19 AF
+5V (F3)

DIVIDER ENABLE
AH 19

INT ENABLE/REQ

SERIAL PREFIX: 2427A

ONE SHOTS

24 BIT COUNT CHAIN

COUNT GATE

COUNTED 45 MHz OR AUDIO — 19 (AK)

COUNT PERIOD

TTL HIGH — 19 (AI)

DATA OUT EN (L)

LOAD 1

13 LOAD 1

4 LOAD (L)

5 CLEAR

12 CLEAR (L)

+5V (F3)

U10, U11, U23, U24, U26, U27, U28, U29

U33B, U36A, U36B, U36E, U36F, U7A, U8A

C62 0.1µ, C63 0.1µ, C67 0.1µ, C68 0.1µ, C69 0.1µ, C71 0.1µ, C73 0.1µ

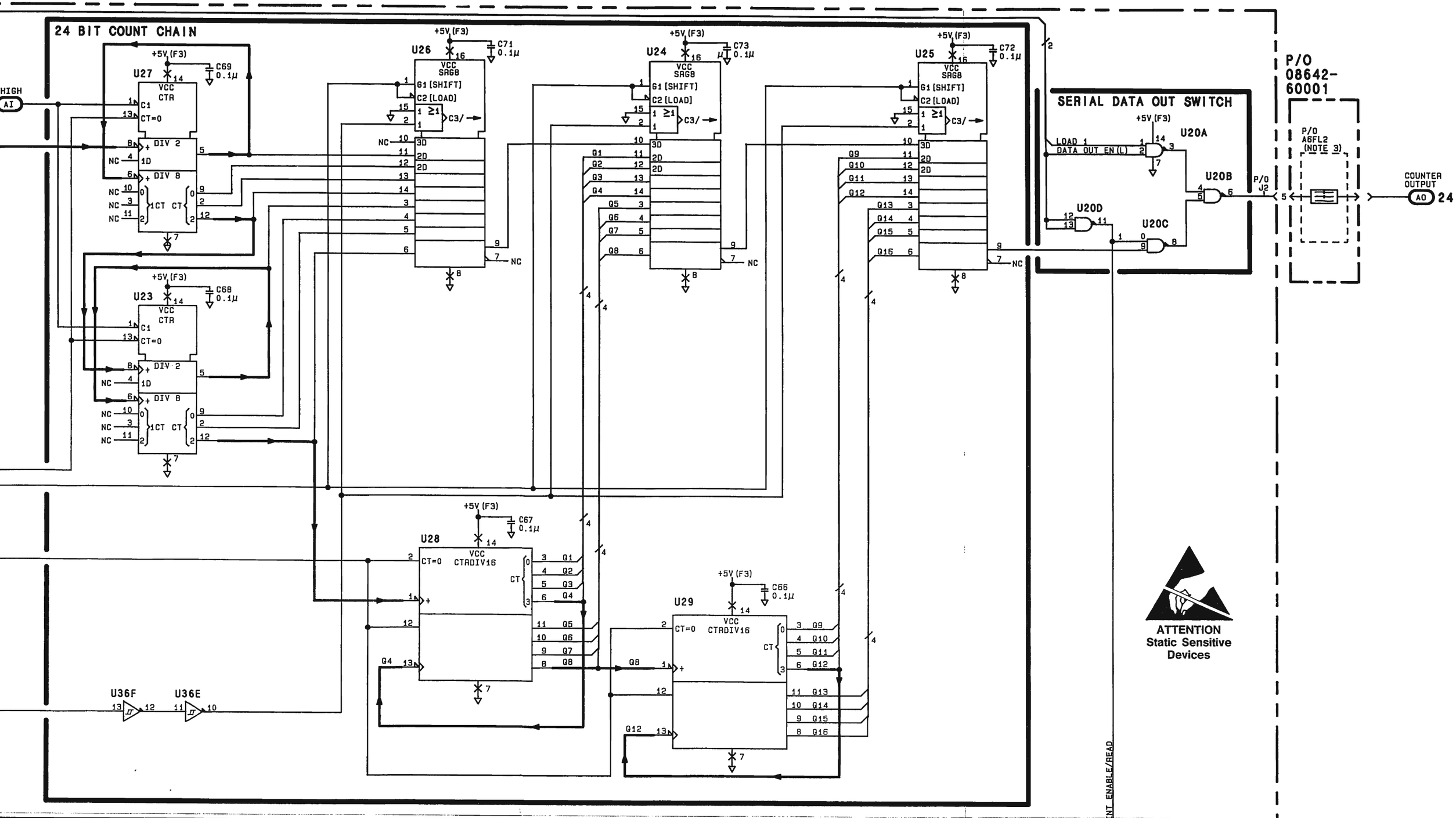
C76 820p, C77 820p, C78 820p

R56 9090, R57 9090, R58 9090, R61 1k

VCC CTR — C1, CT=0, DIV 2, DIV 8, 1CT CT

VCC SRG8 — G1 [SHIFT], C2 [LOAD], C3/, 3D, 2D

VCC CTRDIV16 — CT=0, CT, Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16



SS20
Figure 8K-107
8K-107

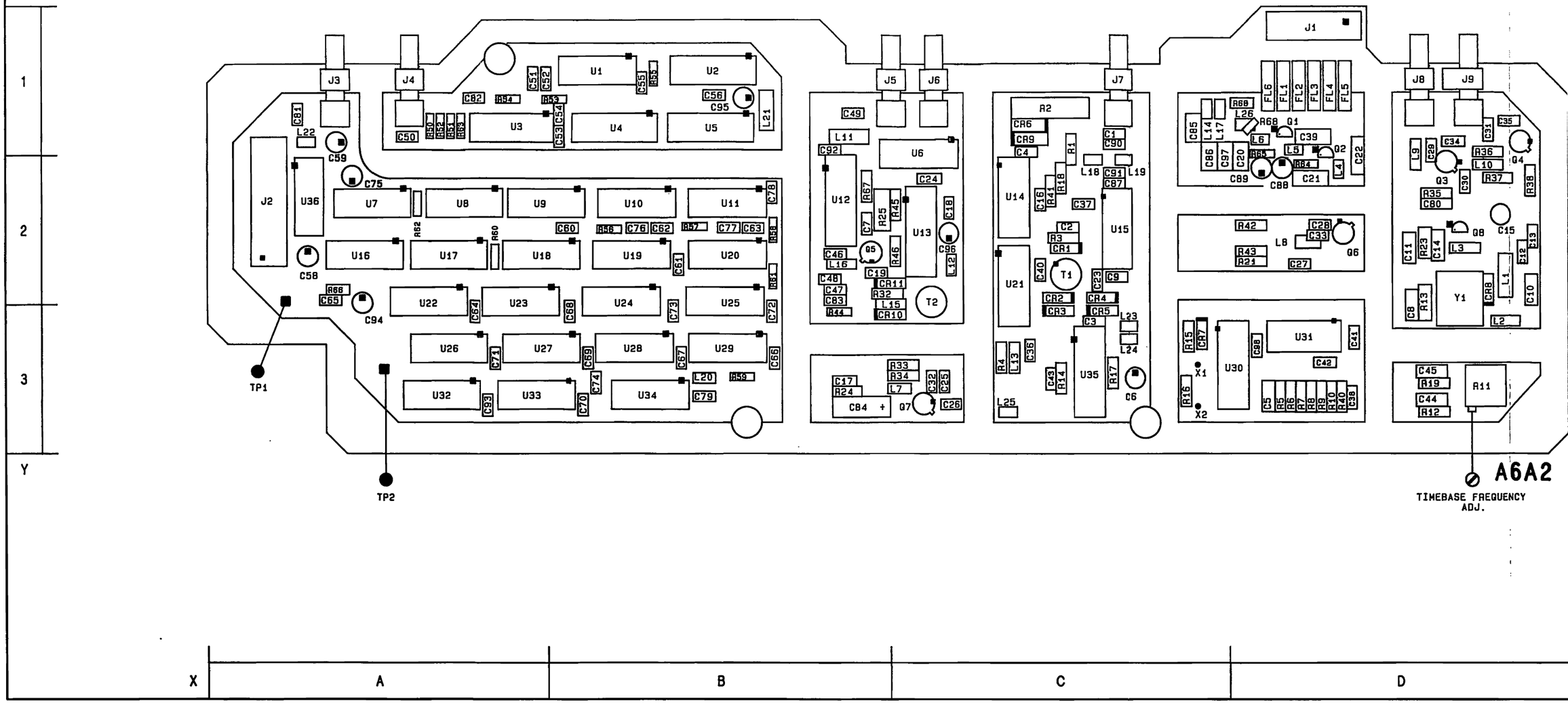
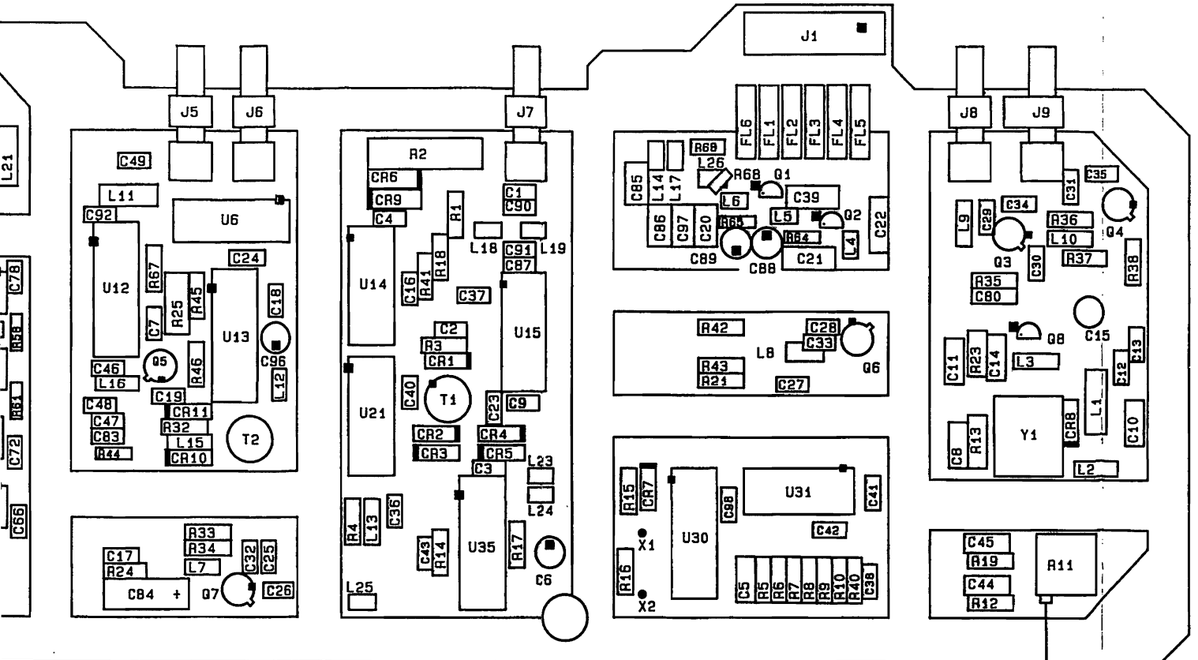


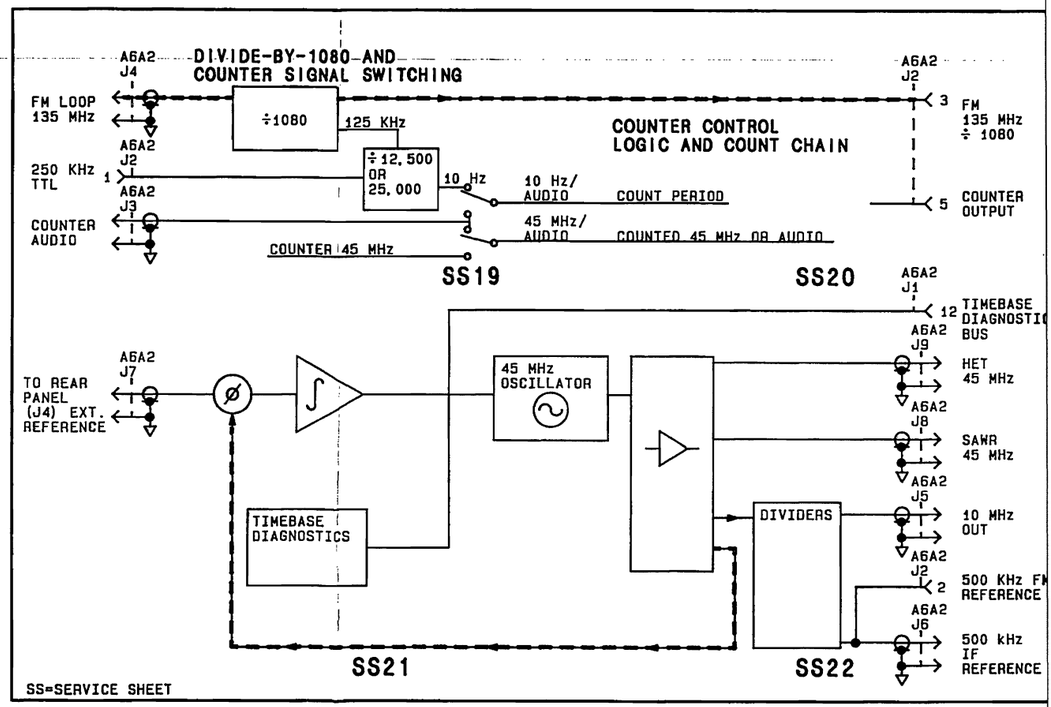
Figure 8K-108. SERVICE SHEET 21 INFORMATION

Component Locator



C D

Component Locator



Reference Block Diagram

Component Coordinates

COMP	X,Y
C1	C, 1
C2	C, 2
C3	C, 3
C4	C, 1
C5	D, 3
C6	C, 3
C8	D, 3
C9	C, 2
C20	D, 2
C21	D, 2
C22	D, 1
C23	C, 2
C36	C, 3
C37	C, 2
C38	D, 3
C39	D, 1
C40	C, 2
C41	D, 3
C42	D, 3
C43	C, 3
C44	D, 3
C45	D, 3
C85	C, 1
C86	C, 2
C87	C, 2
C88	D, 2
C89	D, 2
C90	C, 1
C91	C, 2
C96	C, 2
C97	C, 2

COMP	X,Y
CR1	C, 2
CR2	C, 2
CR3	C, 3
CR4	C, 2
CR5	C, 3
CR6	C, 1
CR7	C, 3
CR9	C, 1
FL1	D, 1
FL2	D, 1
FL3	D, 1
FL4	D, 1
FL5	D, 1
FL6	D, 1
J1	D, 1
J7	C, 1
L4	D, 2
L5	D, 1
L6	D, 1
L12	C, 2
L13	C, 3
L14	C, 1
L17	C, 1
L18	C, 2
L19	C, 2
L23	C, 3
L24	C, 3
L25	C, 3
L26	D, 1
Q1	D, 1
Q2	D, 1

COMP	X,Y
R1	C, 1
R2	C, 1
R3	C, 2
R4	C, 3
R5	D, 3
R6	D, 3
R7	D, 3
R8	D, 3
R9	D, 3
R10	D, 3
R11	D, 3
R12	D, 3
R13	D, 2
R14	C, 3
R15	C, 3
R16	C, 3
R17	C, 3
R18	C, 2
R19	D, 3
R40	D, 3
R41	C, 2
R64	D, 2
R65	D, 2
R68	D, 1
T1	C, 2
U14	C, 2
U15	C, 2
U21	C, 2
U30	D, 3
U31	D, 3
U35	C, 3
X1	C, 3
X2	C, 3

COMP	X,Y

COMP	X,Y

COMP	X,Y

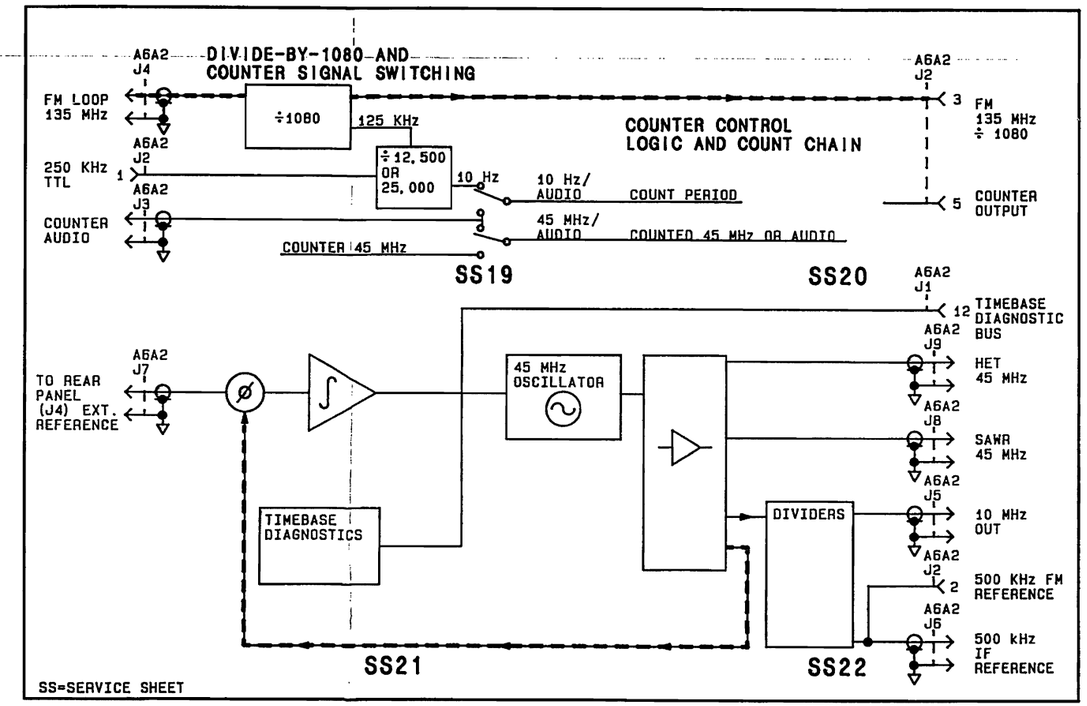
COMP	X,Y

COMP	X,Y

COMP	X,Y

P/O A6A2 COUNTER/ TIMEBASE ASSEMBLY **SS20**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

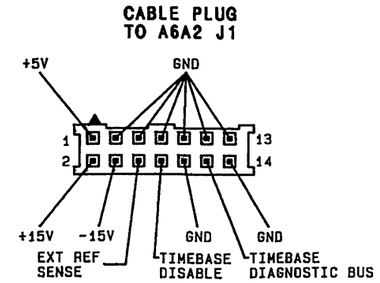
COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	C, 1	CR1	C, 2	R1	C, 1										
C2	C, 2	CR2	C, 2	R2	C, 1										
C3	C, 3	CR3	C, 3	R3	C, 2										
C4	C, 1	CR4	C, 2	R4	C, 3										
C5	D, 3	CR5	C, 3	R5	D, 3										
C6	C, 3	CR6	C, 1	R6	D, 3										
C8	D, 3	CR7	C, 3	R7	D, 3										
C9	C, 2	CR9	C, 1	R8	D, 3										
C20	D, 2			R9	D, 3										
C21	D, 2	FL1	D, 1	R10	D, 3										
C22	D, 1	FL2	D, 1	R11	D, 3										
C23	C, 2	FL3	D, 1	R12	D, 3										
C36	C, 3	FL4	D, 1	R13	D, 2										
C37	C, 2	FL5	D, 1	R14	C, 3										
C38	D, 3	FL6	D, 1	R15	C, 3										
C39	D, 1			R16	C, 3										
C40	C, 2	J1	D, 1	R17	C, 3										
C41	D, 3	J7	C, 1	R18	C, 2										
C42	D, 3			R19	D, 3										
C43	C, 3	L4	D, 2	R40	D, 3										
C44	D, 3	L5	D, 1	R41	C, 2										
C45	D, 3	L6	D, 1	R64	D, 2										
C85	C, 1	L12	C, 2	R65	D, 2										
C86	C, 2	L13	C, 3	R68	D, 1										
C87	C, 2	L14	C, 1												
C88	D, 2	L17	C, 1	T1	C, 2										
C89	D, 2	L18	C, 2												
C90	C, 1	L19	C, 2	U14	C, 2										
C91	C, 2	L23	C, 3	U15	C, 2										
C96	C, 2	L24	C, 3	U21	C, 2										
C97	C, 2	L25	C, 3	U30	D, 3										
		L26	D, 1	U31	D, 3										
				U35	C, 3										
		Q1	D, 1												
		Q2	D, 1	X1	C, 3										
				X2	C, 3										

P/O A6A2 COUNTER/ TIMEBASE ASSEMBLY **SS20**

SEE REVERSE SIDE

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. X1 and X2 are pads on the ciruit board. No connection between them is provided.
3. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.



Schematic General Information

CHANGES

All Serial Prefixes

On the schematic:

- In **INTEGRATOR**, locate U30 and add the active low indicators to inputs labeled as pins 1,8,9, and 16. Directly below the control block for U30, in the element with pin 11 as the input and pin 10 as the output, label the inside with a 3. This indicates that an active (low) control signal on the line labeled X3 (pin 9), turns on the switch. Label the element with pins 15 and 14 with a 4. Label the element with pins 6 and 7 with a 2. Label the element with pins 3 and 2 with a 1.

2516A and above

On the schematic:

- U31 - In **INTEGRATOR**, add the symbol for an operational amplifier (same as U31B and U31C) anywhere in the white space. Designate it U31D. Number the pins as follows: Pin 1 = Output, Pin 2 = Inverting(-) input, Pin 3 = Non-inverting(+) input. Connect pins 1 and 2 together, and connect pin 3 to ground. These connections are made on the circuit board by wire jumpers.

2701A and above

On the Component Locator:

- L14 - Replace L14 with R69.
- L17 - Replace L17 with R70.

On the Component Coordinates:

- L14 - Delete L14 and add R69, C 1.
- L17 - Delete L17 and add R70, C 1.

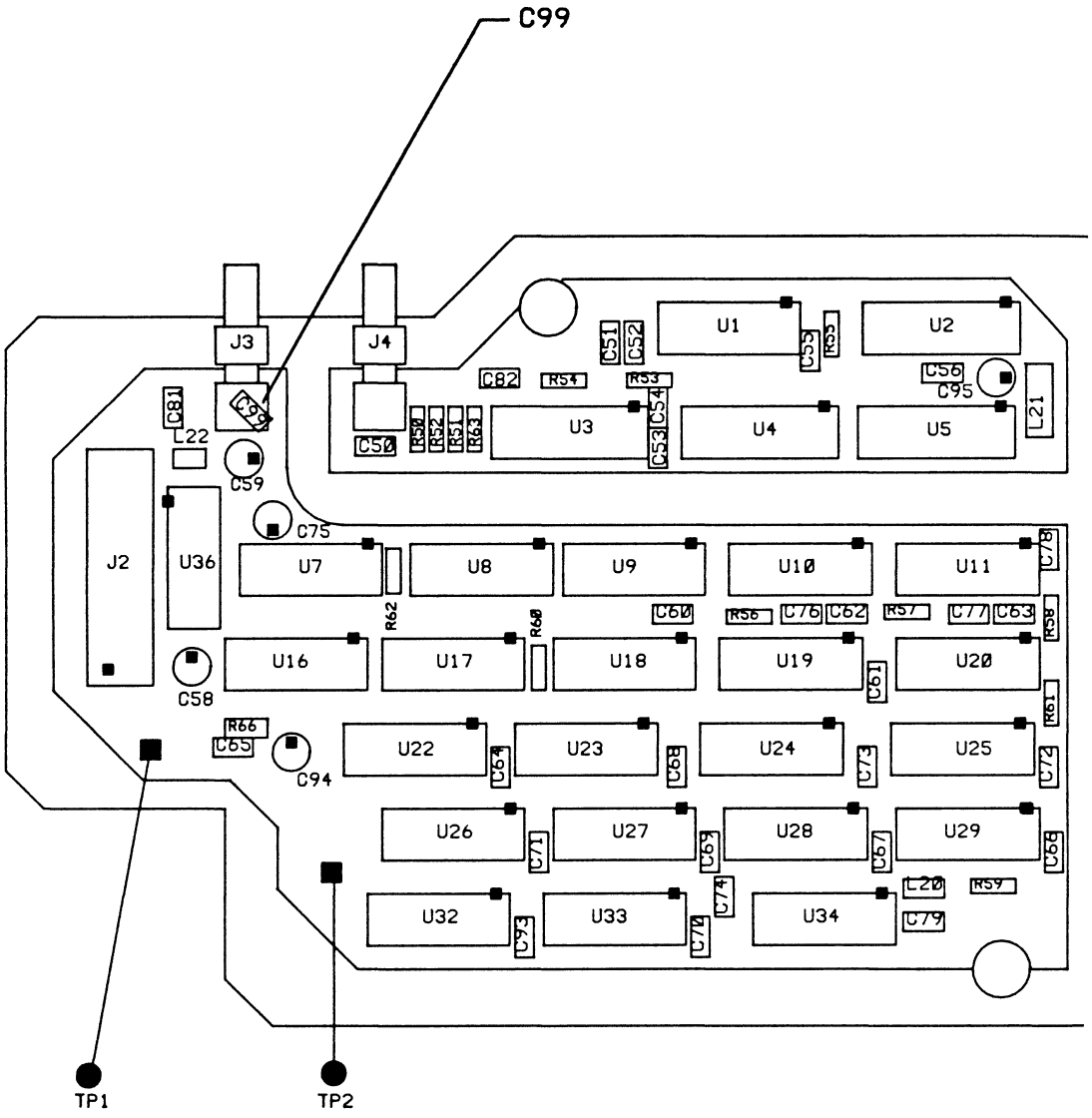
On the schematic:

- L14 - In **TIMEBASE DIAGNOSTICS**, delete L14 and replace it with R69, 215 ohm.
- L17 - In **EXTERNAL REFERENCE DETECTOR**, delete L17 and replace it with R70, 215 ohm.

2714A and above

On the Component Locator:

- C99 - Use the component locator with the partial component locator on page 8K-108.3.


C99
J3
J4
C81
C99
L22
C59
C75
J2
U36
U7
U8
U9
U10
U11
U1
U2
U3
U4
U5
C51
C52
C53
C54
C55
R55
C56
C95
L21
C82
R54
R53
C50
R50
R52
R51
R63
R62
R60
C60
R56
C76
C62
R57
C77
C63
R58
C78
U16
U17
U18
U19
U20
C58
C61
R61
R66
C65
C94
U22
U23
U24
U25
C64
C66
C73
C72
U26
U27
U28
U29
C71
C69
C67
C68
C74
L20
R59
U32
U33
U34
C79
C93
C70
TP1
TP2

P/O A6A2 COUNTER/TIMEBASE ASSEMBLY (08642-60102)

COMPARATOR

PEAK LIMITER

DIVIDE-BY-2

PULSE GENERATOR

PHASE DETECTOR

SAMPLING BRIDGE

TO REAR PANEL (J4) EXTERNAL REFERENCE 53 AP W27 907 J7

C1 0.01µ R2 100 C4 0.01µ CR6 CR9 R18 422

C37 0.01µ R1 121k C87 0.01µ +15V (F2) +5V (F1)

U15 COMP G1 G2 NC 2,5,7,12

C9 0.01µ -15V (F2)

R41 1k C16 0.01µ

U14A U14B S D C R NC

U21A U21B U21C U21D

C40 0.01µ R4 19.6 L13 0.1µ C36 100p

T1 CR1 CR2 CR3 CR4 CR5 C23 0.01µ C2 0.01µ R3 100k

PHASE DETECTOR INPUT 22 AS

TIMEBASE DISABLE 11 AQ P/O A5 SS64 B P/O J1

POWER SUPPLY AND GND

TB POWER SUPPLY AND GROUND 64 JZ 4

+15V 2 FL4 Q2 R64 1330 C88 10µ C39 0.1µ L5 3µ C90 0.1µ L18 3µ L23 3µ

+5V 1 FL5 C22 0.1µ L4 3µ C21 0.1µ L12 3µ C96 10µ

-15V 4 FL3 Q1 R65 1330 C89 10µ C20 0.1µ L6 3µ C91 0.1µ L19 3µ L24 3µ L25 3µ

GND 3,5,7,9,11,13

+15V (F1) +15V (F2) +15V (F3) +5V (F1) +5V (F2) -15V (F1) -15V (F2) -15V (F3) -15V (F4) GND

POWER SUPPLY AND GND AR 22 5

EXTERNAL REFERENCE DETECTOR

U35B G R RX/CX CX

R14 100k C43 0.01µ L17 3µ C86 0.1µ FL1

SERIAL PREFIX: 2427A

OR

R4 19.6
L13 0.1µ
C36 100p
U21D
11
12
11

PHASE DETECTOR

T1
SAMPLING BRIDGE
BUFFER
CR1
+5V (F1)
C23 0.01µ
C2 0.01µ
R3 100k
CR2
CR5
CR3
CR4
C3 22p
U31A
+15V (F3)
C41 0.01µ
C42 0.01µ
-15V (F3)

PHASE DETECTOR INPUT
22 AS

INTEGRATOR

R6 46.4k
C5 0.1µ
R5 147k
U31B
R7 162
R8 10k
LOOP ACQUISITION
(NOTE 2)
X1
X2
U31C
R10 10k
R9 1620

LOOP SWITCH
NC
+15V (F3)
P/O U30
VREF
+V
X1
X2
X3
X4
(CMOS)
P/O U30
-15V (F1)

FL6
R68 100 Ω
L26 3µ
C97 1000p

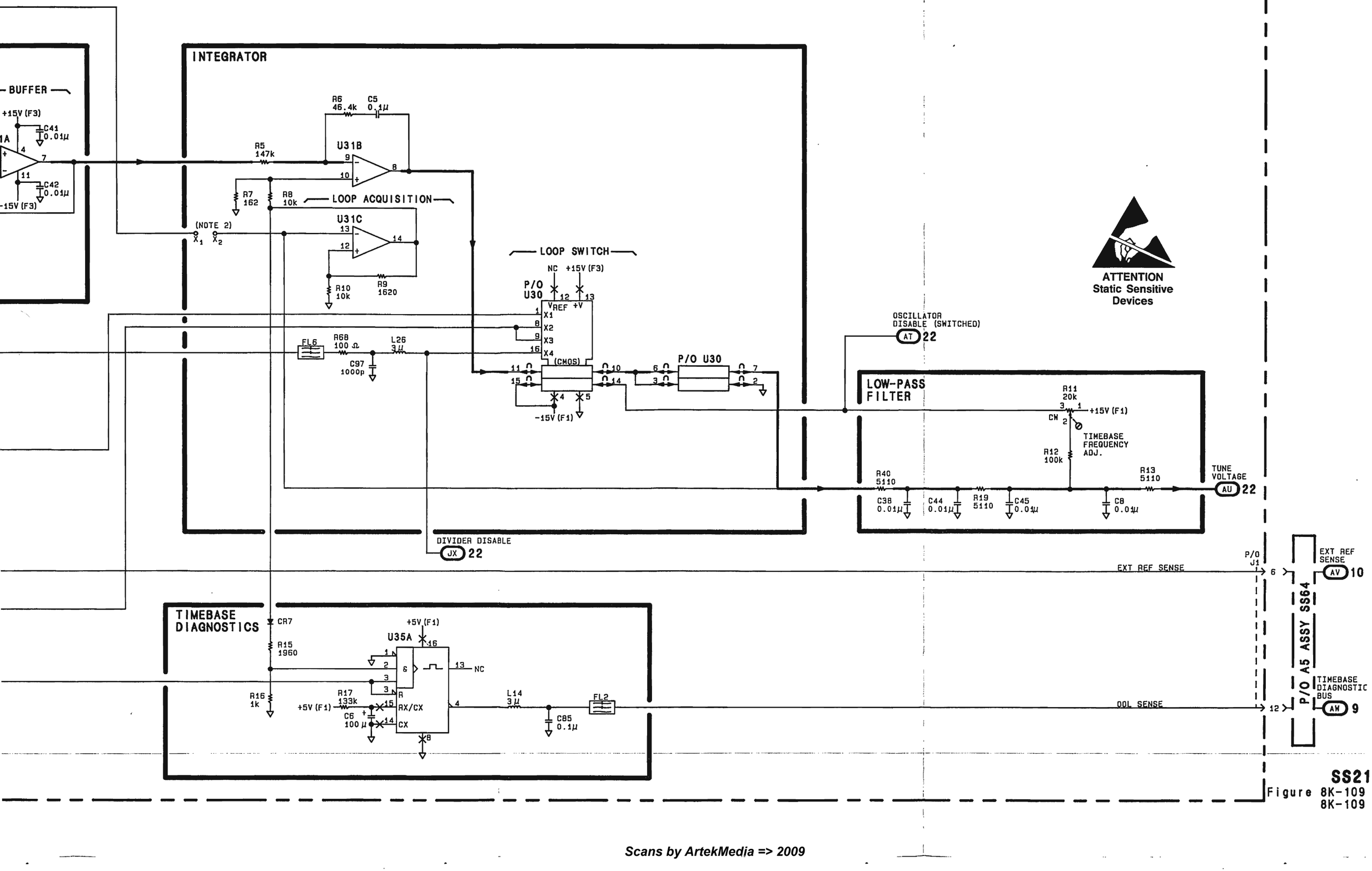
DIVIDER DISABLE
JX 22

EXTERNAL REFERENCE DETECTOR

U35B
&
A
RX/CX
CX
+5V (F1)
R14 100k
C43 0.01µ
L17 3µ
C86 0.1µ
FL1

TIMEBASE DIAGNOSTICS

CR7
R15 1960
R16 1k
U35A
+5V (F1)
R17 133k
C6 100 µ
NC
L14 3µ
C85 0.1µ
FL2



SS21

Figure 8K-109

8K-109

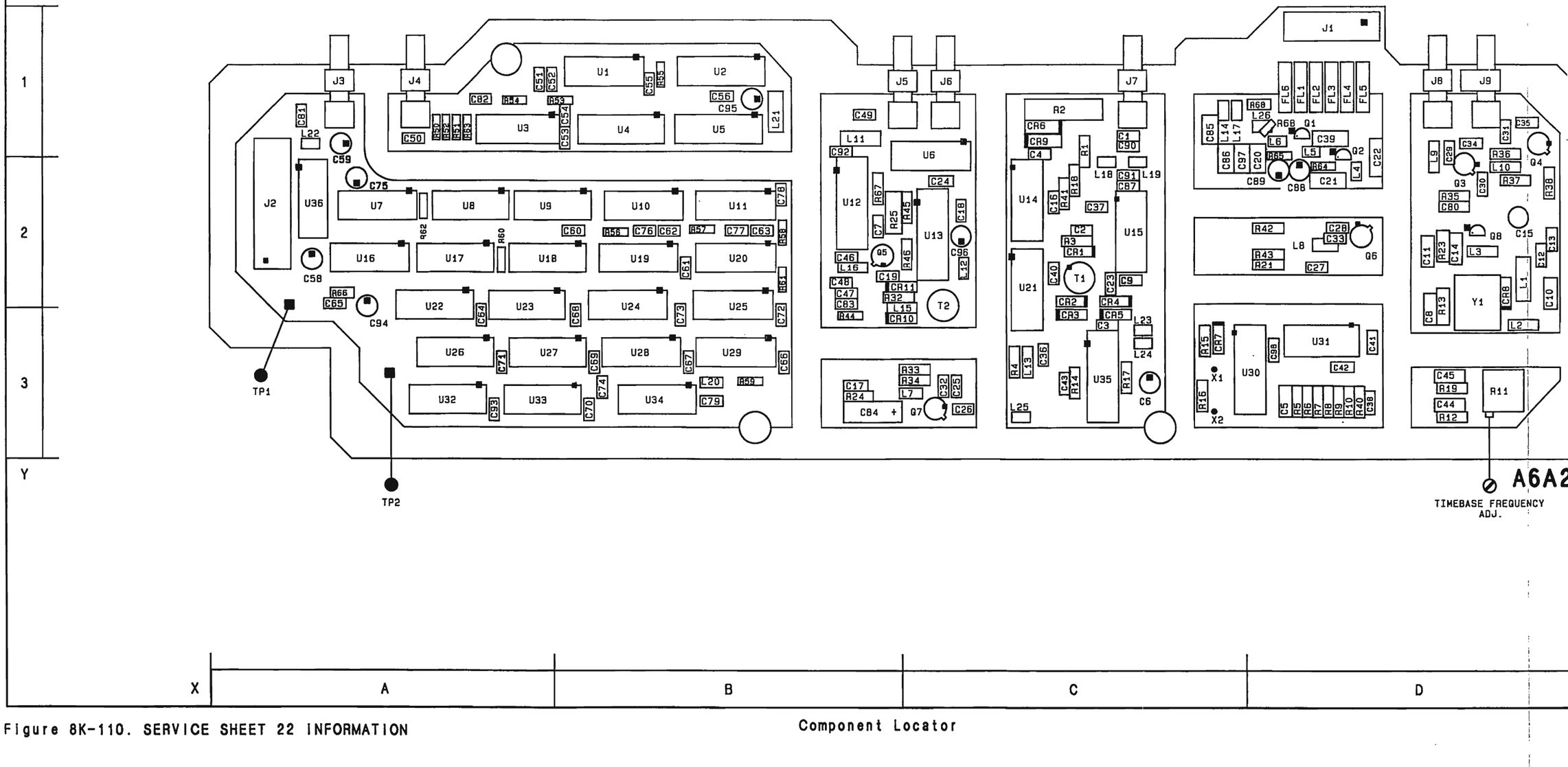
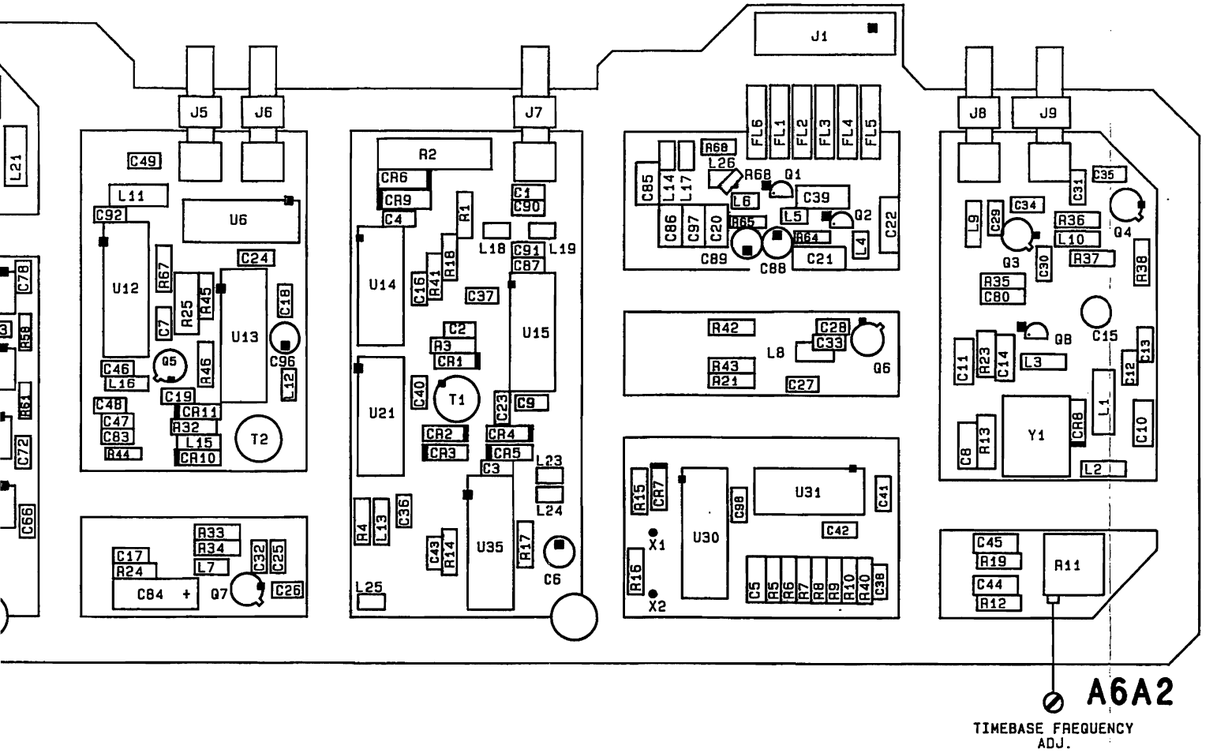


Figure 8K-110. SERVICE SHEET 22 INFORMATION

Component Locator

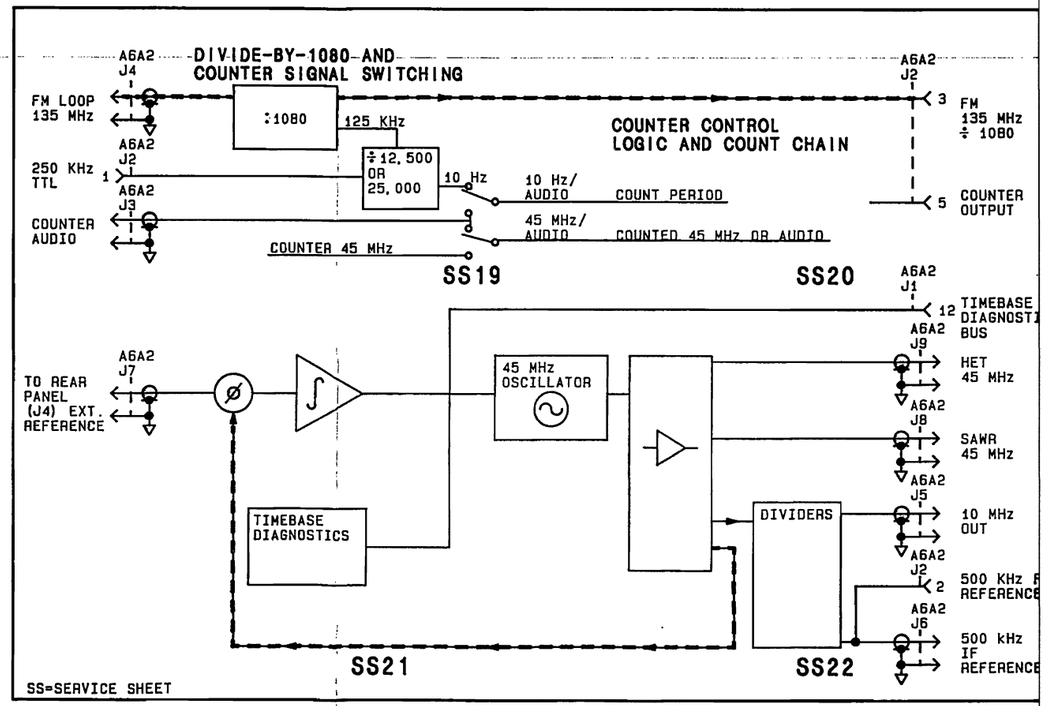


A6A2

TIMEBASE FREQUENCY ADJ.

C D

Component Locator



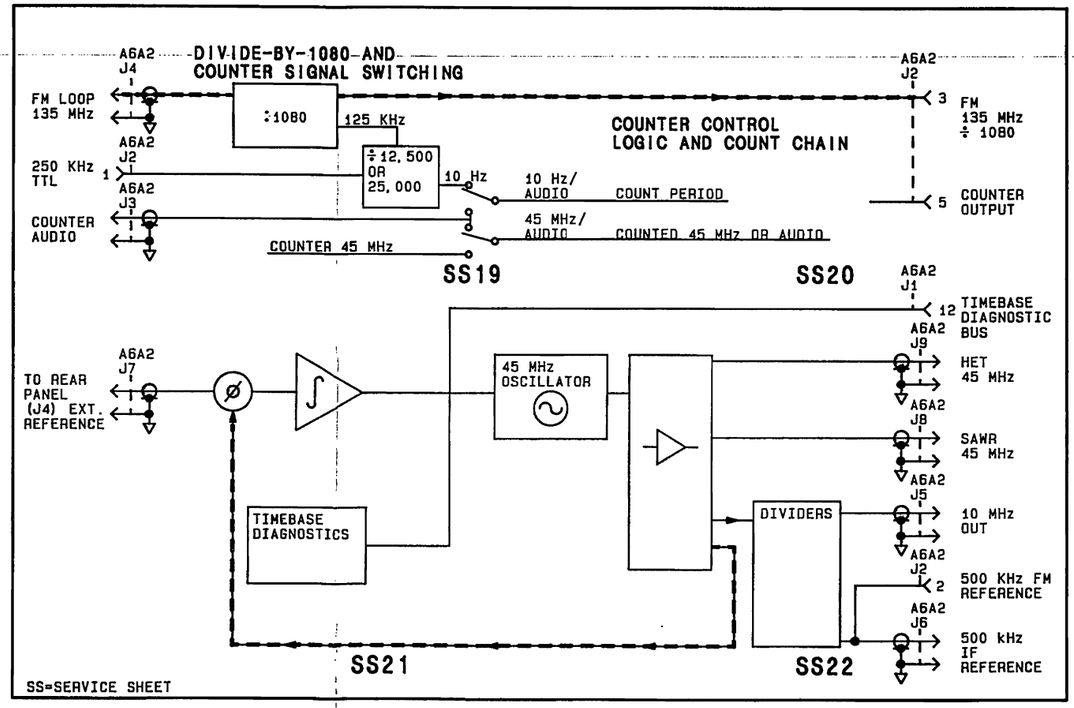
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,
C7	B, 2	J2	A, 2	R44	B, 3										
C10	D, 2	J5	C, 1	R45	C, 2										
C11	D, 2	J6	C, 1	R46	C, 2										
C12	D, 2	J8	D, 1	R67	B, 2										
C13	D, 2	J9	D, 1	T2	C, 2										
C14	D, 2														
C15	D, 2	L1	D, 2	U6	C, 1										
C16	C, 2	L2	D, 3	U12	B, 2										
C17	B, 3	L3	D, 2	U13	C, 2										
C18	C, 2	L7	C, 3												
C19	B, 2	L8	D, 2	Y1	D, 2										
C24	C, 2	L9	D, 1												
C25	C, 3	L10	D, 2												
C26	C, 3	L11	B, 1												
C27	D, 2	L15	B, 3												
C28	D, 2	L16	B, 2												
C29	D, 1														
C30	D, 2	Q3	D, 2												
C31	D, 1	Q4	D, 1												
C32	C, 3	Q5	B, 2												
C33	D, 2	Q6	D, 2												
C34	D, 1	Q7	C, 3												
C35	D, 1	Q8	D, 2												
C46	B, 2														
C47	B, 2	R21	D, 2												
C48	B, 2	R23	D, 2												
C49	B, 1	R24	B, 3												
C80	D, 2	R25	B, 2												
C83	B, 2	R32	B, 2												
C84	B, 3	R33	C, 3												
C92	B, 1	R34	C, 3												
C98	D, 3	R35	D, 2												
		R36	D, 1												
CR8	D, 2	R37	D, 2												
CR10	B, 3	R38	D, 2												
CR11	B, 2	R42	D, 2												
		R43	D, 2												

P/O A6A2 COUNTER/ TIMEBASE ASSEMBLY **SS21**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

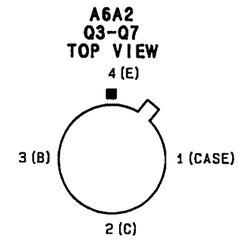
COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C7	B, 2	J2	A, 2	R44	B, 3												
C10	D, 2	J5	C, 1	R45	C, 2												
C11	D, 2	J6	C, 1	R46	C, 2												
C12	D, 2	J8	D, 1	R67	B, 2												
C13	D, 2	J9	D, 1														
C14	D, 2			T2	C, 2												
C15	D, 2	L1	D, 2														
C16	C, 2	L2	D, 3	U6	C, 1												
C17	B, 3	L3	D, 2	U12	B, 2												
C18	C, 2	L7	C, 3	U13	C, 2												
C19	B, 2	L8	D, 2														
C24	C, 2	L9	D, 1	Y1	D, 2												
C25	C, 3	L10	D, 2														
C26	C, 3	L11	B, 1														
C27	D, 2	L15	B, 3														
C28	D, 2	L16	B, 2														
C29	D, 1																
C30	D, 2	Q3	D, 2														
C31	D, 1	Q4	D, 1														
C32	C, 3	Q5	B, 2														
C33	D, 2	Q6	D, 2														
C34	D, 1	Q7	C, 3														
C35	D, 1	Q8	D, 2														
C46	B, 2																
C47	B, 2	R21	D, 2														
C48	B, 2	R23	D, 2														
C49	B, 1	R24	B, 3														
C80	D, 2	R25	B, 2														
C83	B, 2	R32	B, 2														
C84	B, 3	R33	C, 3														
C92	B, 1	R34	C, 3														
C98	D, 3	R35	D, 2														
		R36	D, 1														
CR8	D, 2	R37	D, 2														
CR10	B, 3	R38	D, 2														
CR11	B, 2	R42	D, 2														
		R43	D, 2														

P/O A6A2 COUNTER/ TIMEBASE ASSEMBLY **SS21**

SEE REVERSE SIDE

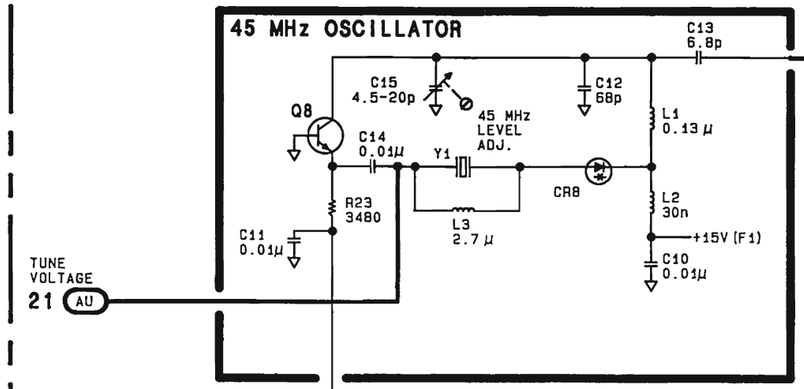
Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
3. A6FL2 is an array of feedthrough filters passing through the center of the module to make connections between two (2) printed circuit boards.



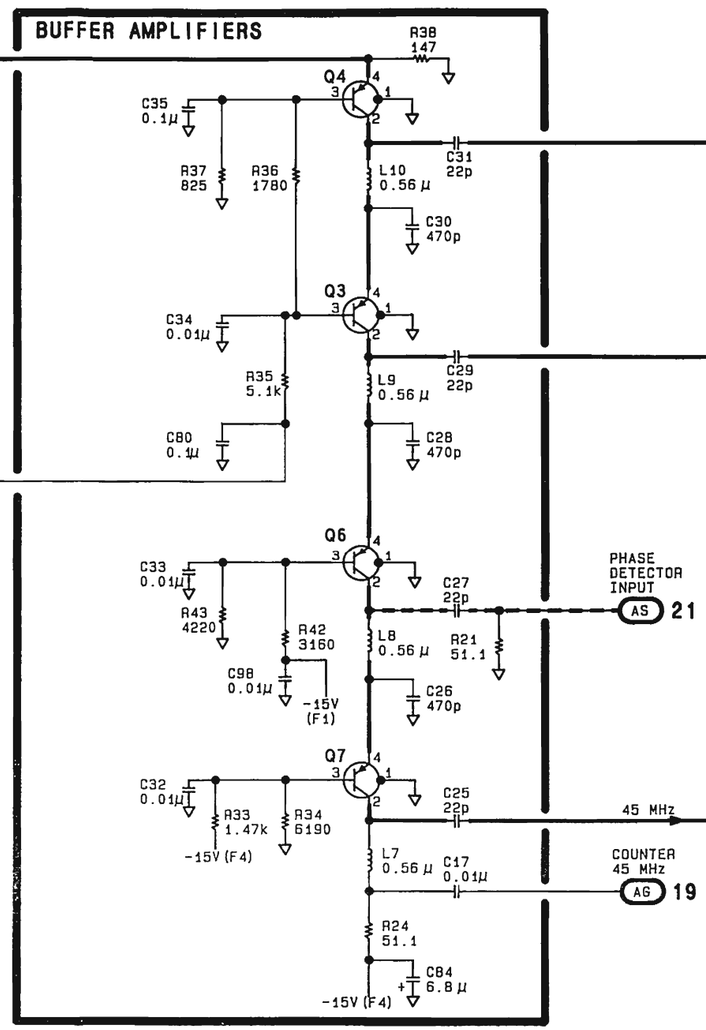
Schematic General Information

P/O A6A2 COUNTER/TIMEBASE ASSEMBLY (08642-60102)



TUNE VOLTAGE
21 AU

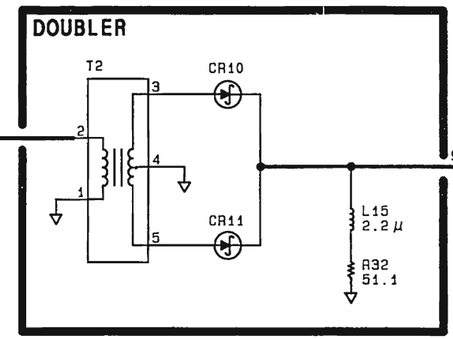
OSCILLATOR DISABLE (SWITCHED)
21 AT



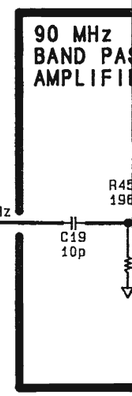
PHASE DETECTOR INPUT
AS 21

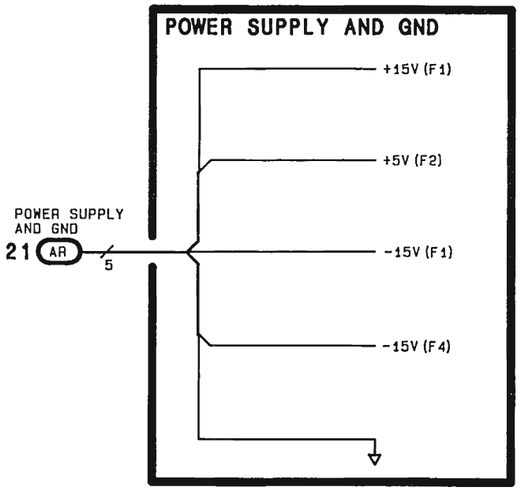
COUNTER 45 MHz
AG 19

45 MHz



90 MHz





POWER SUPPLY AND GND
21 AR
5

SERIAL PREFIX: 2427A

R38
147

C31
22p

6 µ

C30
470p

C29
22p

6 µ

C28
470p

C27
22p

PHASE
DETECTOR
INPUT
AS 21

6 µ

R21
51.1

C26
470p

C25
22p

45 MHz

6 µ C17
0.01µ

COUNTER
45 MHz
A6 19

1

L C84
6.8 µ

DOUBLER

T2

CR10

CR11

L15
2.2 µ

R32
51.1

90 MHz

90 MHz
BAND PASS
AMPLIFIER

+5V (F2)

C47
1000p

C48
30p

L16
0.1µ

C46
10p

R45
1960

Q5

C19
10p

R46
1960

R44
196

C83
100p

90 MHz

DIVIDE-BY-9

+5V (F2)

C92
0.1µ

U12

VCC
VCCO
TTL VCC

≥1
G1

[ECL]

DIV 8
CT=8
1Z2

DIV 9
CT=9
1Z3

ECL/TTL
VEE
VREF

R67
14.7k

R25
1k

C7
0.1µ

10 MHz

TTL BUFFER

+5V (F2)

C24
0.01µ

10 MHz
BAND PASS
FILTER

L11
21.9 µ

C49
10p

U6B

U6C

U6D

U6E

DIVIDE-BY-20

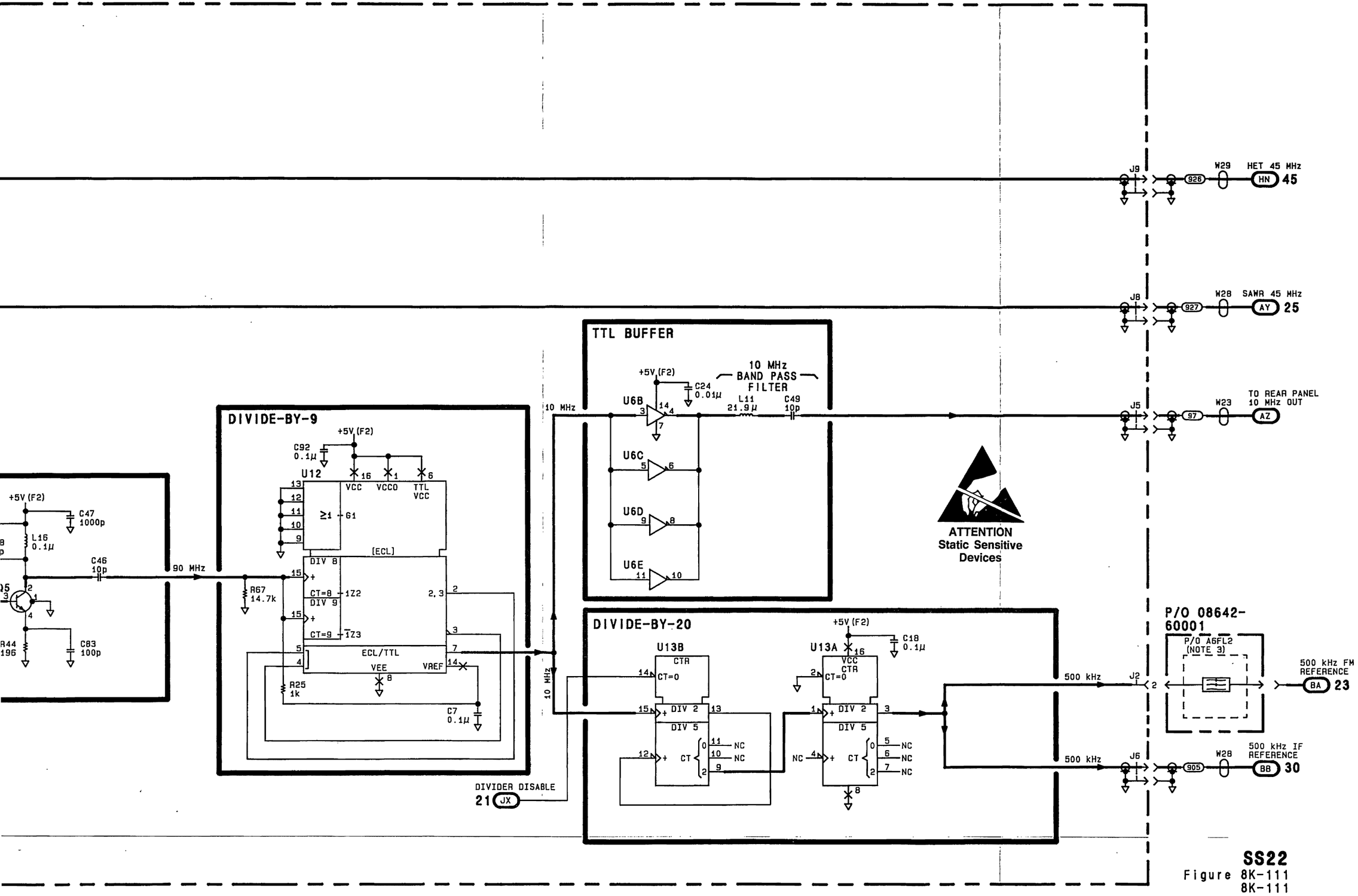
+5V (F2)

U13B

U13A

CTR
CT=0
DIV 2
DIV 5
CT
NC

DIVIDER DISABLE
21 JX



SS22
Figure 8K-111
8K-111

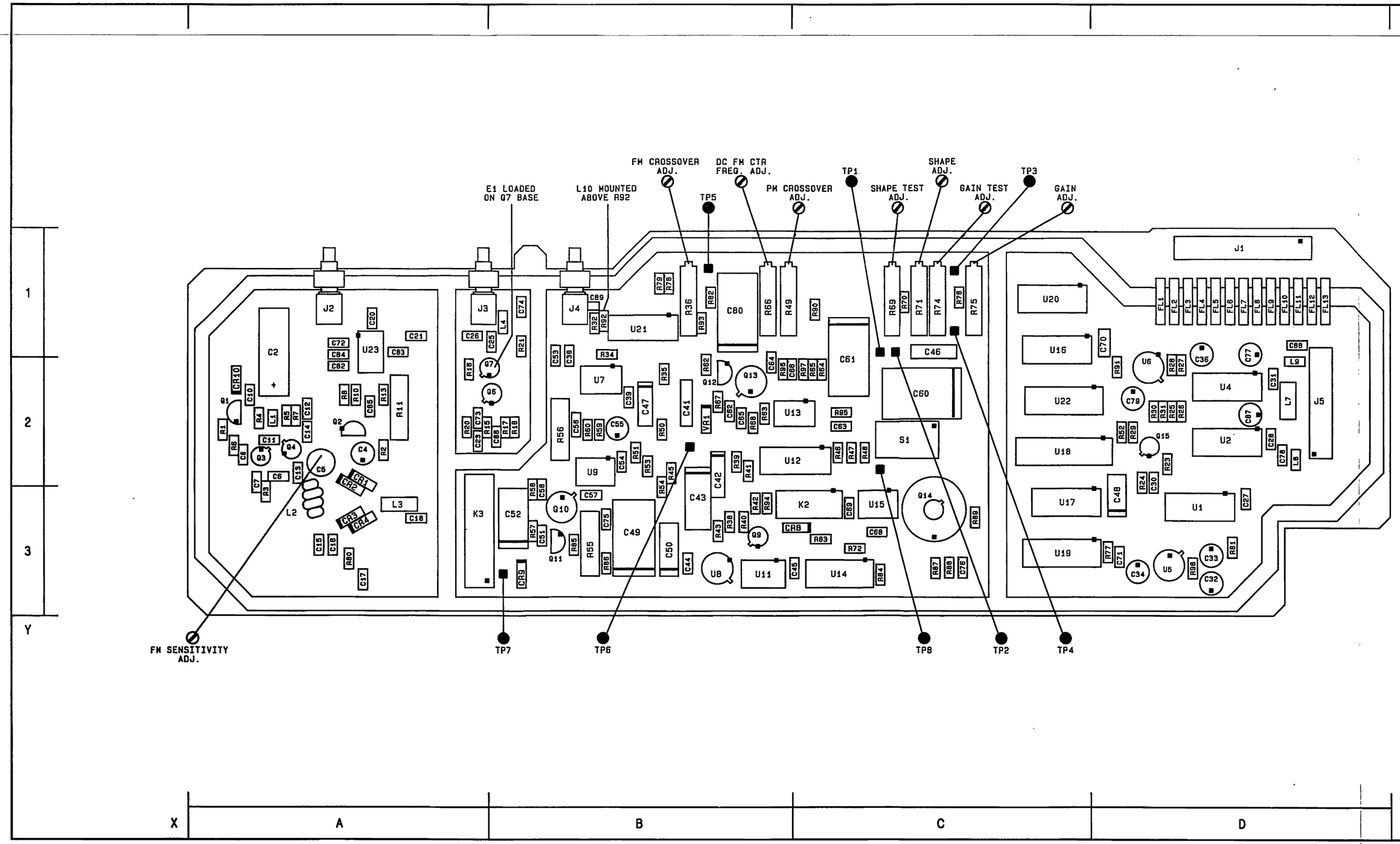
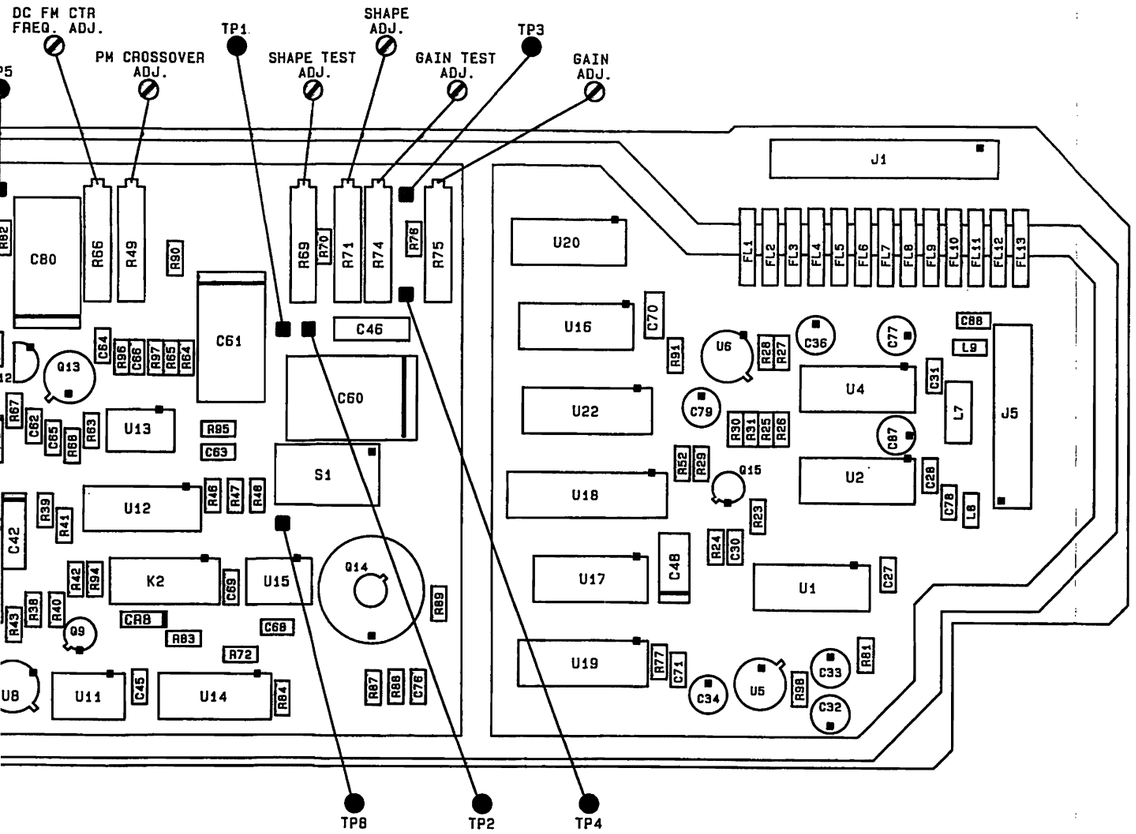


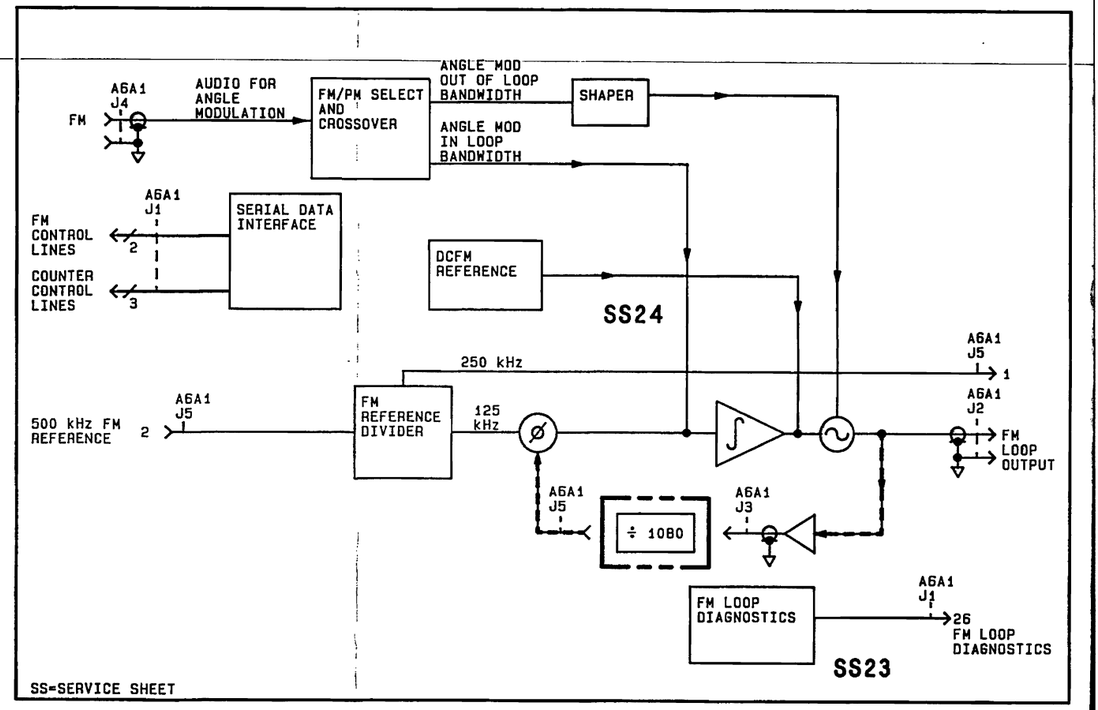
Figure 8K-112. SERVICE SHEET 23 INFORMATION

Component Locator



C D

Component Locator



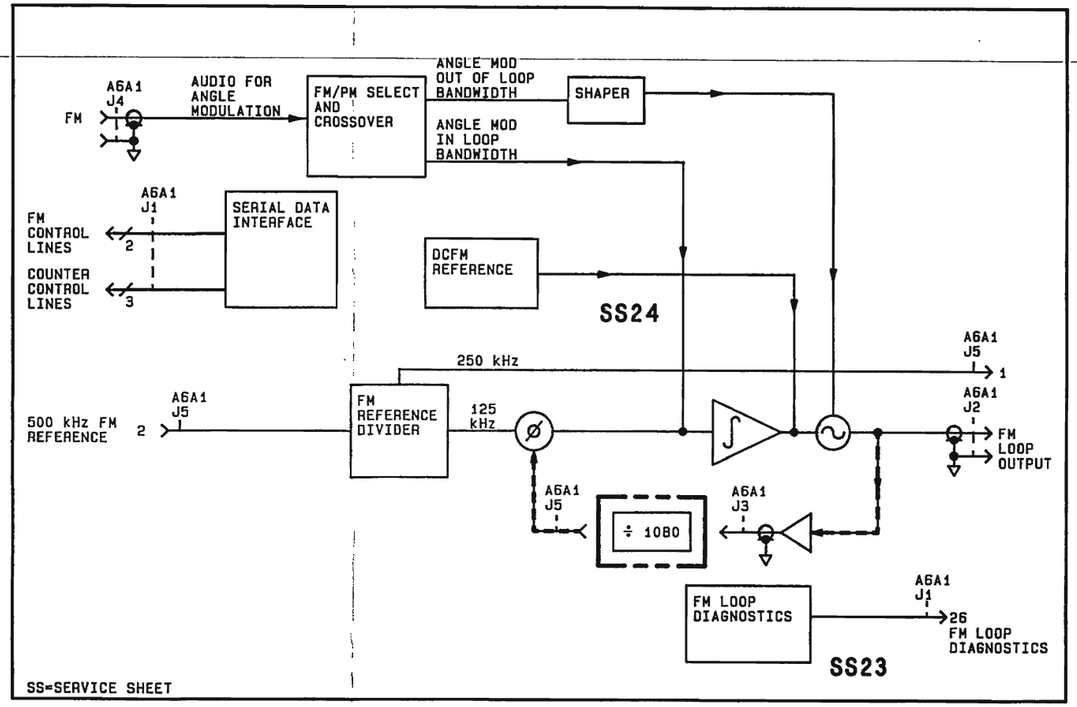
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C2	A, 1	C56	B, 2	K3	A, 3	R24	D, 2	U1	D, 3						
C4	A, 2	C57	B, 3			R25	D, 2	U2	D, 2						
C5	A, 2	C58	B, 3	L1	A, 2	R26	D, 2	U4	D, 2						
C6	A, 2	C72	A, 1	L2	A, 3	R27	D, 2	U5	D, 3						
C7	A, 2	C73	A, 2	L3	A, 3	R28	D, 2	U6	D, 2						
C8	A, 2	C74	B, 1	L4	B, 1	R29	D, 2	U9	B, 2						
C10	A, 2	C75	B, 3	L7	D, 2	R30	D, 2	U11	B, 3						
C11	A, 2	C77	D, 1	L9	D, 2	R31	D, 2	U22	C, 2						
C12	A, 2	C79	D, 2			R50	B, 2	U23	A, 1						
C13	A, 2	C82	A, 2	Q1	A, 2	R51	B, 2								
C14	A, 2	C83	A, 1	Q2	A, 2	R52	D, 2								
C15	A, 3	C84	A, 1	Q3	A, 2	R53	B, 2								
C16	A, 3	C85	A, 2	Q4	A, 2	R54	B, 2								
C17	A, 3	C86	B, 2	Q6	B, 2	R55	B, 3								
C18	A, 3	C87	D, 2	Q7	B, 2	R56	B, 2								
C20	A, 1	C88	D, 1	Q10	B, 3	R57	B, 3								
C21	A, 1			Q11	B, 3	R58	B, 3								
C23	A, 2	CR1	A, 2	Q15	D, 2	R59	B, 2								
C25	B, 1	CR2	A, 2			R60	B, 2								
C26	A, 1	CR3	A, 3	R1	A, 2	R80	A, 3								
C27	D, 3	CR4	A, 3	R2	A, 2	R81	D, 3								
C28	D, 2	CR9	B, 3	R3	A, 3	R85	B, 3								
C30	D, 2	CR10	A, 2	R4	A, 2	R86	B, 3								
C31	D, 2			R5	A, 2	R91	D, 2								
C32	D, 3	E1	B, 2	R6	A, 2	R98	D, 3								
C33	D, 3			R7	A, 2										
C34	D, 3	FL1	D, 1	R8	A, 2	TP7	B, 3								
C36	D, 1	FL9	D, 1	R10	A, 2	TP8	C, 2								
C47	B, 2	FL11	D, 1	R11	A, 2										
C48	D, 3	FL12	D, 1	R13	A, 2										
C49	B, 3	FL13	D, 1	R15	A, 2										
C50	B, 3			R16	A, 2										
C51	B, 3	J1	D, 1	R17	B, 2										
C52	B, 3	J2	A, 1	R18	B, 2										
C53	B, 1	J3	A, 1	R20	A, 2										
C54	B, 2	J4	B, 1	R21	B, 1										
C55	B, 2	J5	D, 2	R23	D, 2										

P/O A6A2 COUNTER/ TIMEBASE ASSEMBLY **SS22**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C2	A, 1	C56	B, 2	K3	A, 3	R24	D, 2	U1	D, 3						
C4	A, 2	C57	B, 3			R25	D, 2	U2	D, 2						
C5	A, 2	C58	B, 3	L1	A, 2	R26	D, 2	U4	D, 2						
C6	A, 2	C72	A, 1	L2	A, 3	R27	D, 2	U5	D, 3						
C7	A, 2	C73	A, 2	L3	A, 3	R28	D, 2	U6	D, 2						
C8	A, 2	C74	B, 1	L4	B, 1	R29	D, 2	U9	B, 2						
C10	A, 2	C75	B, 3	L7	D, 2	R30	D, 2	U11	B, 3						
C11	A, 2	C77	D, 1	L9	D, 2	R31	D, 2	U22	C, 2						
C12	A, 2	C79	D, 2			R50	B, 2	U23	A, 1						
C13	A, 2	C82	A, 2	Q1	A, 2	R51	B, 2								
C14	A, 2	C83	A, 1	Q2	A, 2	R52	D, 2								
C15	A, 3	C84	A, 1	Q3	A, 2	R53	B, 2								
C16	A, 3	C85	A, 2	Q4	A, 2	R54	B, 2								
C17	A, 3	C86	B, 2	Q6	B, 2	R55	B, 3								
C18	A, 3	C87	D, 2	Q7	B, 2	R56	B, 2								
C20	A, 1	C88	D, 1	Q10	B, 3	R57	B, 3								
C21	A, 1			Q11	B, 3	R58	B, 3								
C23	A, 2	CR1	A, 2	Q15	D, 2	R59	B, 2								
C25	B, 1	CR2	A, 2			R60	B, 2								
C26	A, 1	CR3	A, 3	R1	A, 2	R80	A, 3								
C27	D, 3	CR4	A, 3	R2	A, 2	R81	D, 3								
C28	D, 2	CR9	B, 3	R3	A, 3	R85	B, 3								
C30	D, 2	CR10	A, 2	R4	A, 2	R86	B, 3								
C31	D, 2			R5	A, 2	R91	D, 2								
C32	D, 3	E1	B, 2	R6	A, 2	R98	D, 3								
C33	D, 3			R7	A, 2										
C34	D, 3	FL1	D, 1	R8	A, 2	TP7	B, 3								
C36	D, 1	FL9	D, 1	R10	A, 2	TP8	C, 2								
C47	B, 2	FL11	D, 1	R11	A, 2										
C48	D, 3	FL12	D, 1	R13	A, 2										
C49	B, 3	FL13	D, 1	R15	A, 2										
C50	B, 3			R16	A, 2										
C51	B, 3	J1	D, 1	R17	B, 2										
C52	B, 3	J2	A, 1	R18	B, 2										
C53	B, 1	J3	A, 1	R20	A, 2										
C54	B, 2	J4	B, 1	R21	B, 1										
C55	B, 2	J5	D, 2	R23	D, 2										

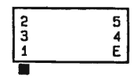
P/O A6A2 COUNTER/ TIMEBASE ASSEMBLY **SS22**

SEE REVERSE SIDE

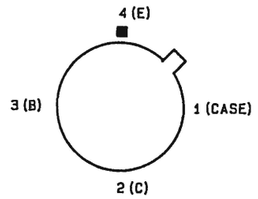
Notes:

1. Each module in the HP 8642 has a nine-digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. Feedthrough filter outer body must be soldered to the shielding in the area where shielding is notched.
3. A6FL2 is an array of feedthrough filters passing through the center of the module to make connections between two (2) printed circuit boards.
4. Do not touch guard trace on solder side of board with solder iron.
5. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

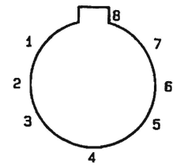
A6A1 K3 TOP VIEW



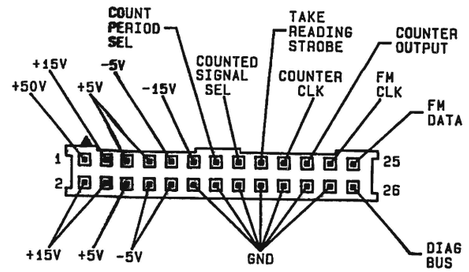
A6A1 Q6,Q7 TOP VIEW



A6A1 U6 TOP VIEW



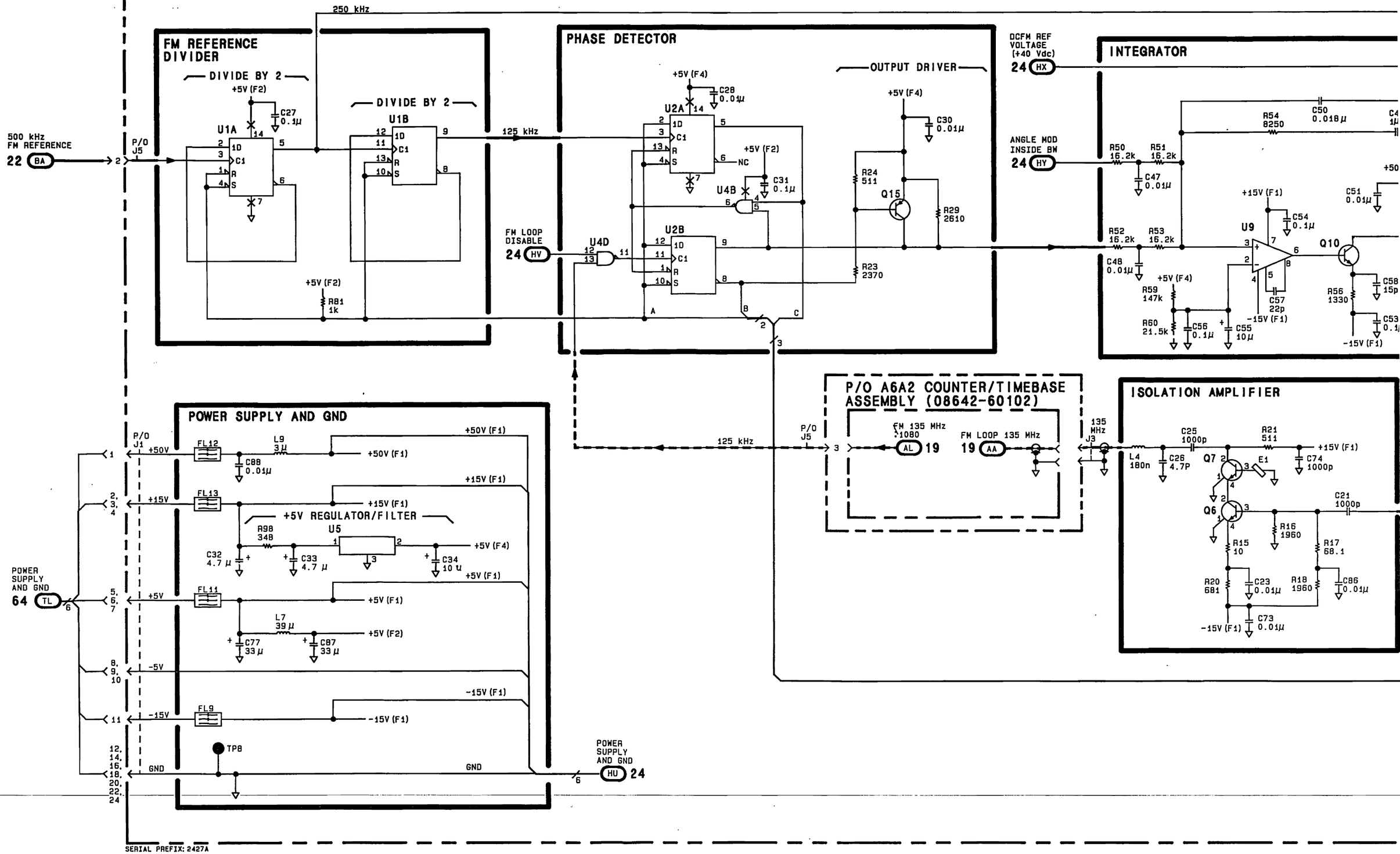
CABLE PLUG TO A6A1 J1



CHANGES

All serial prefixes	On the A6A1 schematic: • C13, R4, R5 - In **VOLTAGE CONTROLLED OSCILLATOR**, change C13 to 3.9p, R4 to 1k, and, R5 to 1k. • C4 - In the block **VOLTAGE CONTROLLED OSCILLATOR**, change the polarity of C4 to the ground side. On the A6A1 Component Locator: • A6A1 - Add L10 above U21 and to the right of R92. Add C25 above Q7. Add C89 between C38 and R32.
2550A to 2751A	On the A6A1 Component Locator: • C90 - In grid location (A,1) add C90 to the left of C2 and just above CR10, following the contour of the EMI strip. In Component Coordinates: • C90 - Add C90 A,1. On the A6A1 schematic: • C90 - In the **VOLTAGE CONTROLLED OSCILLATOR**, add C90 from +15V(F1) to ground and assign it a value of .1uf.
2824A and above	On the A6A1 Component Locator: • C90 - In grid location (A,1) add C90 to the left of C2 and just above CR10, following the contour of the EMI strip. In Component Coordinates: • C90 - Add C90 A,1. On the A6A1 schematic: • C90 - In the **VOLTAGE CONTROLLED OSCILLATOR**, change the value of C90 to .22uf.

P/O A6A1 FM VCO ASSEMBLY (08642-60101)



SERIAL PREFIX: 2427A

OUTPUT DRIVER

+5V (F4)
C30 0.01µ
R24 511
Q15
R29 2610
R23 2370

DCFM REF VOLTAGE (+40 Vdc)
24 HX

ANGLE MOD INSIDE BW
24 HY

INTEGRATOR

R50 16.2k
R51 16.2k
C47 0.01µ
R54 8250
C50 0.018µ
C49 1µ
R52 16.2k
R53 16.2k
C48 0.01µ
+15V (F1)
C54 0.1µ
U9
+5V (F4)
R59 147k
R60 21.5k
C56 0.1µ
C55 10µ
C57 22p
-15V (F1)
+50V (F1)
C51 0.01µ
R55 2370
Q10
Q11
R56 1330
C58 15p
C53 0.1µ
-15V (F1)
R57 90.9k

DCFM SWITCH

R58 1k
C52 0.15µ
+5V (F1)
CR9
K3
SHIELDED
R85 100k
R86 8250
C75 1000p
TP7

DCFM SELECT
24 HZ
+5V (F1)
U11B

VOLTAGE CONTROLLED OSCILLATOR

+15V (F1)
R1 10k
CR10
Q1
C2 100µ
L1 3µ
C13 3.3p
C5 1.3-5.4p
FM SENSITIVITY ADJ.
CR2
CR1
CR4
CR3
L2 50n
L3 1µ
C6 5.6p
R6 316
R7 316
Q3
C8 1000p
Q4
C7 13p
R3 34.8k
C11 1000p
C14 10p
C15 1000p
C18 330p
R4 1780
R5 1780
R80 51.1
C17 1000p
C16 1000p
C10 1000p
Q2
C12 39p
C4 10µ
R2 1k
-15V (F1)

ANGLE MOD OUTSIDE BW
24 IA

P/O A6A2 COUNTER/TIMEBASE ASSEMBLY (08642-60102)

FM 135 MHz 1080
AL 19
FM LOOP 135 MHz
19 AA
135 MHz
J3

ISOLATION AMPLIFIER

L4 180n
C26 4.7P
C25 1000p
Q7
E1
R21 511
+15V (F1)
C74 1000p
Q6
C21 1000p
R16 1960
R15 10
R17 68.1
R20 681
C23 0.01µ
R18 1960
C86 0.01µ
C73 0.01µ
-15V (F1)

OUT-OF-LOCK DETECTOR

+5V (F2)
R25 5110
R28 51.1k
C36 10 µ
U4C
R26 3830
R27 51.1k
U6
R91 5110
R31 2370
R30 750
C79 1µ

MUX SELECT LINES
24 IB

VCO TUNE VOLTAGE

MOD SIGNAL SENSE LINE
24 IC

ATTENTION
Static Sensitive
Devices

P/O (08642-60101)

P/O A6FL2 (NOTE 3)

J5 1 → 250 kHz TTL AB 19

VOLTAGE CONTROLLED OSCILLATOR

+15V (F1)

R1 10k, CR10, Q1, C2 100µ, L1 3µ, C13 3.3p, C5 1.3-5.4p, CR2, CR1, FM SENSITIVITY ADJ., L2 50n, CR4, CR3, L3 1µ, C6 5.6p, R6 316, R7 316, Q3, C8 1000p, Q4, C7 13p, R3 34.8k, C11 1000p, R4 1780, R5 1780, C14 10p, C15 1000p, C18 330p, R80 51.1, C17 1000p, C16 1000p, C10 1000p, Q2, C12 39p, C4 10µ, R2 1k, -15V (F1)

DCFM SWITCH

R58 1k, R57 90.9k, C52 0.15µ, +5V (F1), CR9, K3, SHIELDED, R85 100k, R86 8250, TP7, C75 1000p

DCFM SELECT 24 HZ → 6, 7 U11B 4, 8 5, +5V (F1)

ANGLE MOD OUTSIDE BW 24 IA

POWER SPLITTER

U23 pins 1, 3, 5, 8

C20 0.01µ, J2, W24, 935, FM LOOP OUTPUT CU 32 (135 MHz 2.4 dBm), R13 110, C82 0.01µ, C72 0.01µ, C83 0.01µ, R10 2150, R8 1K, C84 0.01µ, R11 383, C85 0.01µ, -15V (F1)

OUT-OF-LOCK DETECTOR

+5V (F2)

R25 5110, R28 51.1k, C36 10 µ, U4C, R26 3830, R27 51.1k, U6, R91 5110, R31 2370, R30 750, C79 1µ

3 → MUX SELECT LINES 24 IB

FM LOOP DIAGNOSTICS INTERFACE

+5V (F1)

U22 16, EN 6, MUX, S0 11, S1 10, S2 9, G 0/7, 0 13, 1 14, 2 15, 3 12, 4 1, 5 5, 6 2, 7 4, NC, B 7

FL1 (NOTE 2) 3 → P/O J1 25 → P/O A5 SS64 FM LOOP DIAGNOSTIC BUS IE 9

VCO TUNE VOLTAGE SENSE

MOD SIGNAL SENSE LINE 24 IC

ATTENTION Static Sensitive Devices

SS23

Figure 8K-113

8K-113

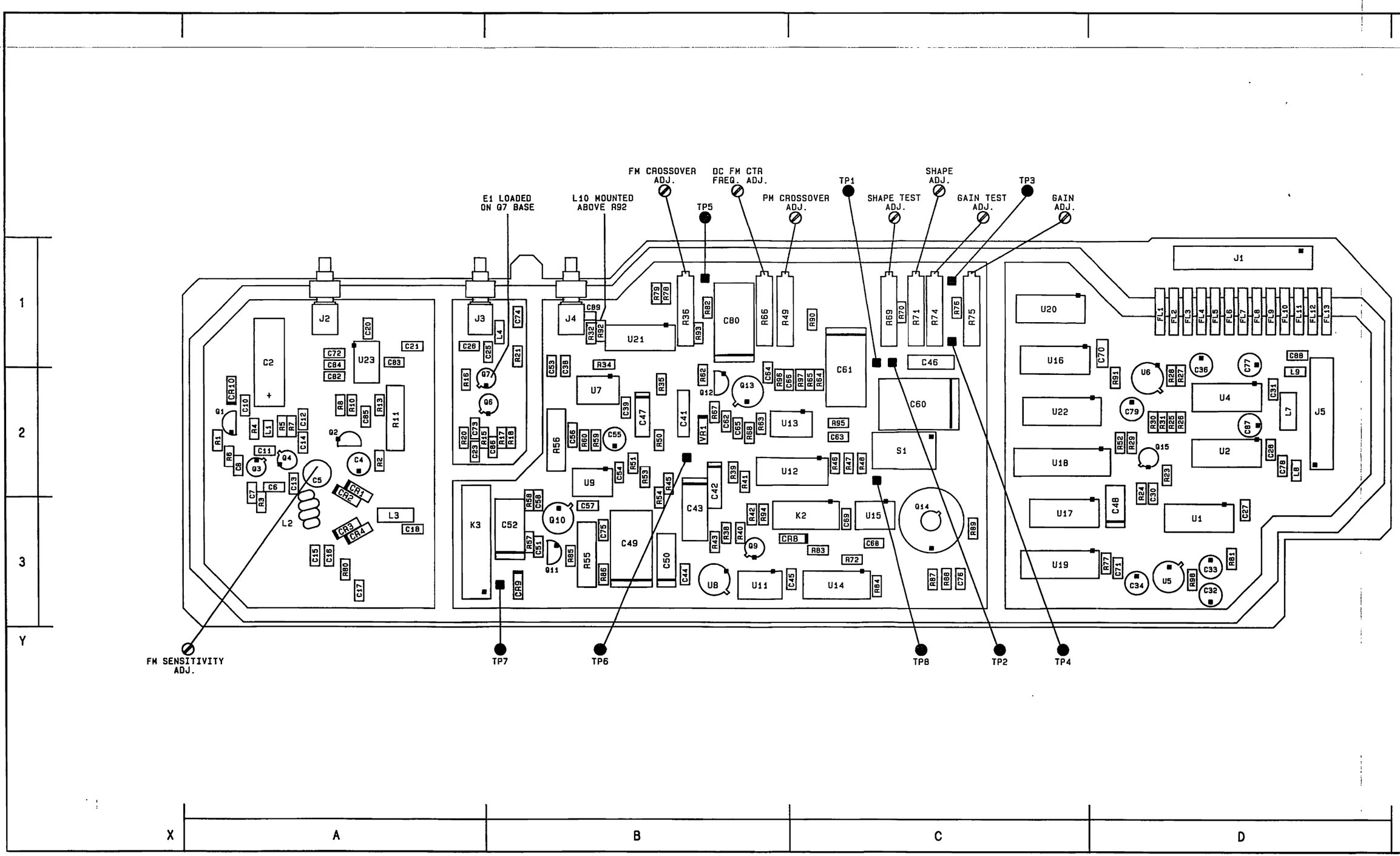
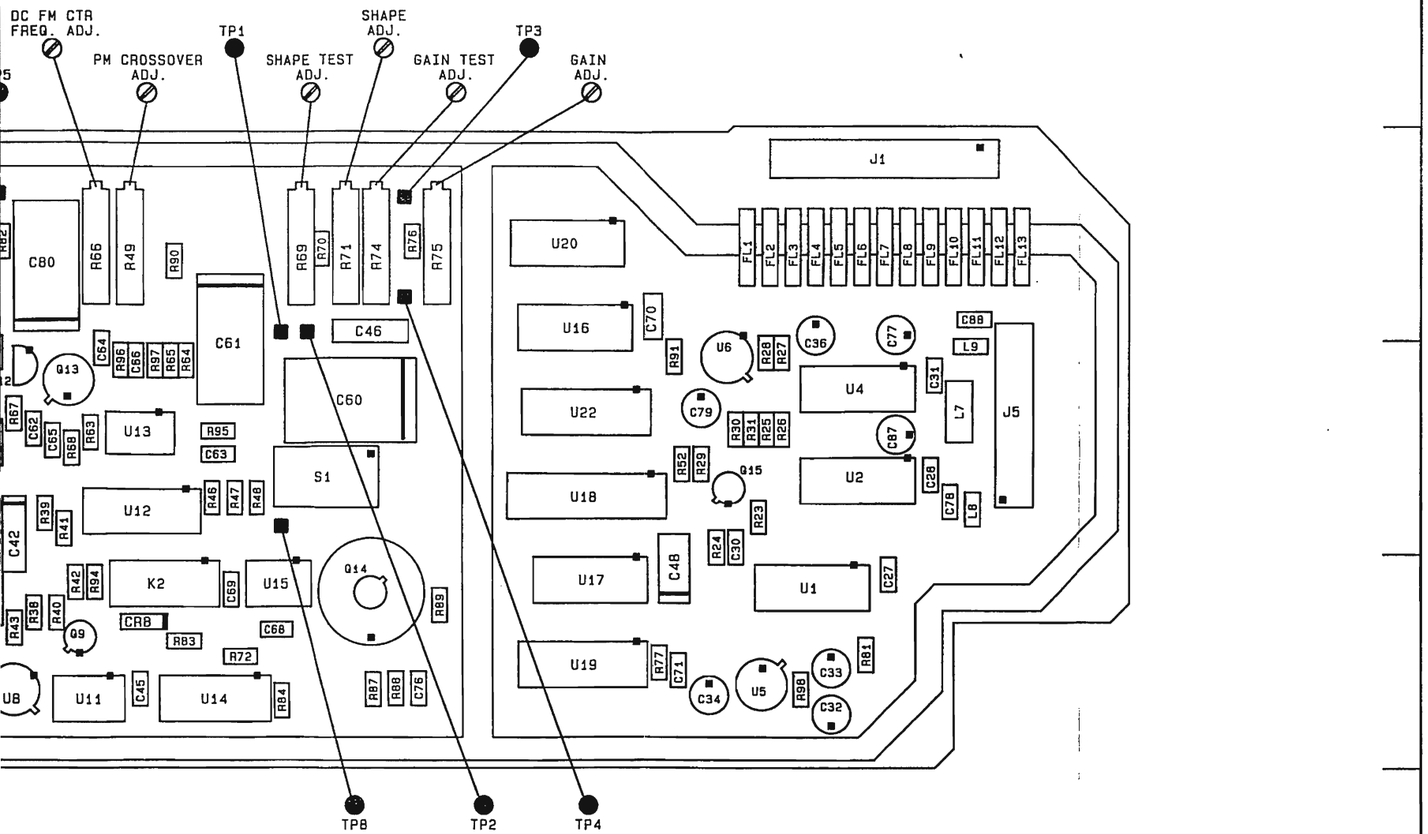
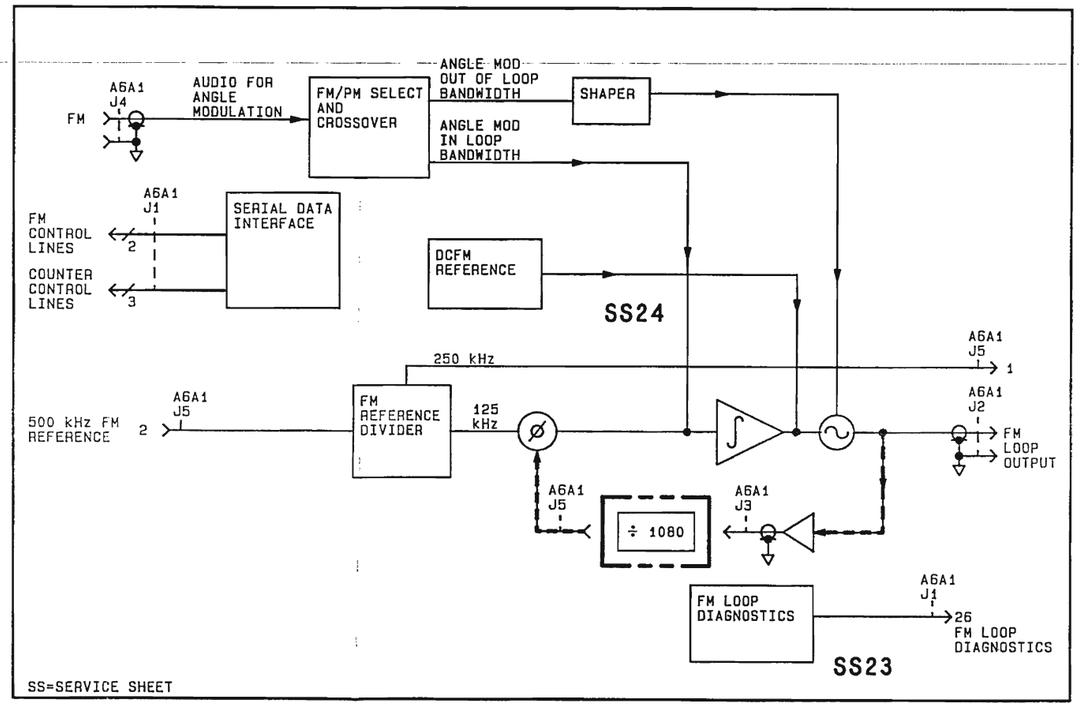


Figure 8K-114. SERVICE SHEET 24 INFORMATION

Component Locator



Component Locator



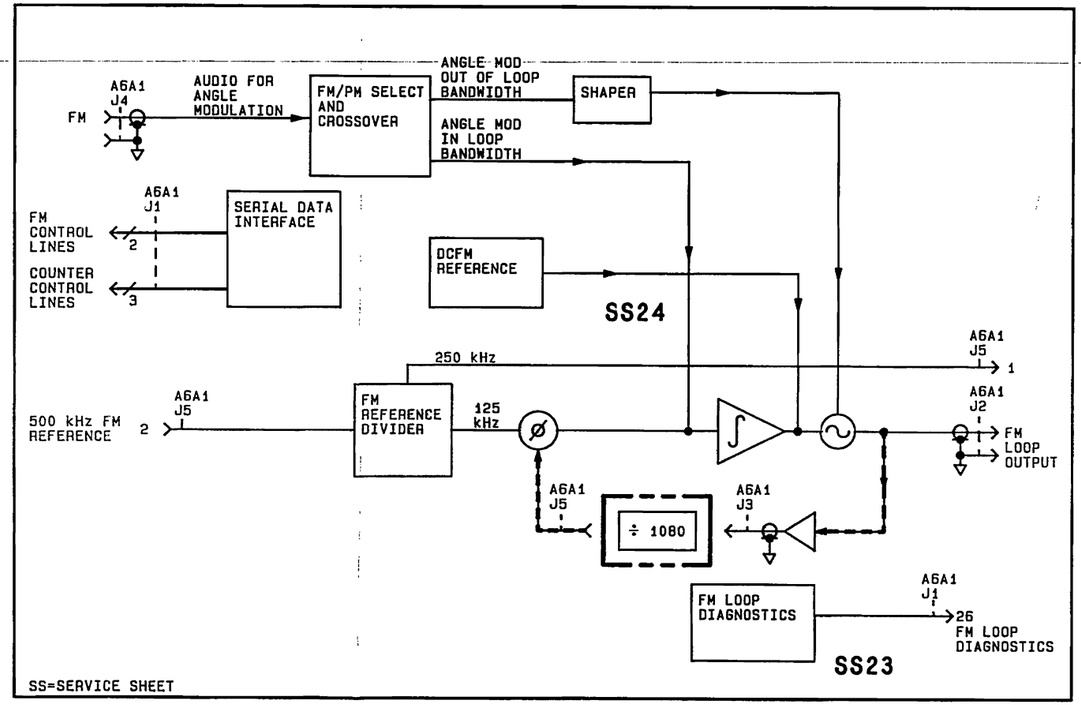
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C38	B, 1	K2	C, 3	R75	C, 1	U19	C, 3								
C39	B, 2			R76	C, 1	U20	C, 1								
C41	B, 2	L8	D, 2	R77	D, 3	U21	B, 1								
C42	B, 2	L10	B, 1	R78	B, 1										
C43	B, 3			R79	B, 1	VR1	B, 2								
C44	B, 3	Q9	B, 3	R82	B, 1										
C45	C, 3	Q12	B, 2	R83	C, 3										
C46	C, 1	Q13	B, 2	R84	C, 3										
C60	C, 2	Q14	C, 3	R87	C, 3										
C61	C, 1			R88	C, 3										
C62	B, 2	R32	B, 1	R89	C, 3										
C63	C, 2	R34	B, 1	R90	C, 1										
C64	B, 2	R35	B, 2	R92	B, 1										
C65	B, 2	R36	B, 1	R93	B, 1										
C66	B, 2	R38	B, 3	R94	B, 3										
C68	C, 3	R39	B, 2	R95	C, 2										
C69	C, 3	R40	B, 3	R96	B, 2										
C70	D, 1	R41	B, 2	R97	C, 2										
C71	D, 3	R42	B, 3												
C76	C, 3	R43	B, 3	S1	C, 2										
C78	D, 2	R45	B, 2												
C80	B, 1	R46	C, 2	TP1	C, 1										
C89	B, 1	R47	C, 2	TP2	C, 1										
		R48	C, 2	TP3	C, 1										
CR8	C, 3	R49	B, 1	TP4	C, 1										
		R62	B, 2	TP5	B, 1										
FL2	D, 1	R63	B, 2	TP6	B, 2										
FL3	D, 1	R64	C, 2												
FL4	D, 1	R65	C, 2	U7	B, 2										
FL5	D, 1	R66	B, 1	U8	B, 3										
FL6	D, 1	R67	B, 2	U12	B, 2										
FL7	D, 1	R68	B, 2	U13	B, 2										
FL8	D, 1	R69	C, 1	U14	C, 3										
FL10	D, 1	R70	C, 1	U15	C, 3										
		R71	C, 1	U16	C, 1										
J1	D, 1	R72	C, 3	U17	C, 3										
		R74	C, 1	U18	C, 2										

SEE REVERSE SIDE

P/O A6A1 FM VCO ASSEMBLY **SS23**



SS=SERVICE SHEET

Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C38	B, 1	K2	C, 3	R75	C, 1	U19	C, 3								
C39	B, 2			R76	C, 1	U20	C, 1								
C41	B, 2	L8	D, 2	R77	D, 3	U21	B, 1								
C42	B, 2	L10	B, 1	R78	B, 1										
C43	B, 3			R79	B, 1	VR1	B, 2								
C44	B, 3	Q9	B, 3	R82	B, 1										
C45	C, 3	Q12	B, 2	R83	C, 3										
C46	C, 1	Q13	B, 2	R84	C, 3										
C60	C, 2	Q14	C, 3	R87	C, 3										
C61	C, 1			R88	C, 3										
C62	B, 2	R32	B, 1	R89	C, 3										
C63	C, 2	R34	B, 1	R90	C, 1										
C64	B, 2	R35	B, 2	R92	B, 1										
C65	B, 2	R36	B, 1	R93	B, 1										
C66	B, 2	R38	B, 3	R94	B, 3										
C68	C, 3	R39	B, 2	R95	C, 2										
C69	C, 3	R40	B, 3	R96	B, 2										
C70	D, 1	R41	B, 2	R97	C, 2										
C71	D, 3	R42	B, 3												
C76	C, 3	R43	B, 3	S1	C, 2										
C78	D, 2	R45	B, 2												
C80	B, 1	R46	C, 2	TP1	C, 1										
C89	B, 1	R47	C, 2	TP2	C, 1										
		R48	C, 2	TP3	C, 1										
CR8	C, 3	R49	B, 1	TP4	C, 1										
		R62	B, 2	TP5	B, 1										
FL2	D, 1	R63	B, 2	TP6	B, 2										
FL3	D, 1	R64	C, 2												
FL4	D, 1	R65	C, 2	U7	B, 2										
FL5	D, 1	R66	B, 1	U8	B, 3										
FL6	D, 1	R67	B, 2	U12	B, 2										
FL7	D, 1	R68	B, 2	U13	B, 2										
FL8	D, 1	R69	C, 1	U14	C, 3										
FL10	D, 1	R70	C, 1	U15	C, 3										
		R71	C, 1	U16	C, 1										
J1	D, 1	R72	C, 3	U17	C, 3										
		R74	C, 1	U18	C, 2										

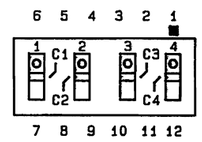
SEE REVERSE SIDE

P/O A6A1 FM VCO ASSEMBLY SS23

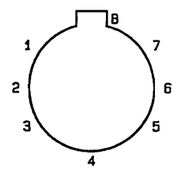
Notes:

1. Each module in the HP 8642 has a nine-digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. Feedthrough filter outer body must be soldered to the shielding in the area where shielding is notched.
3. A6FL2 is an array of feedthrough filters passing through the center of the module to make connections between two (2) printed circuit boards.
4. HR1, Q14, R70, R71, R75 and R76 are part of FM FET Kit (08642-80016).
5. Do not touch guard trace on solder side of board with solder iron.
6. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

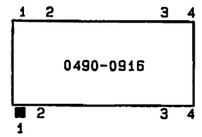
A6A1 S1 TOP VIEW



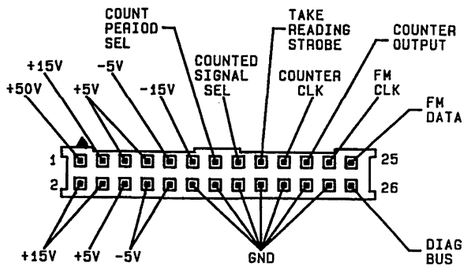
A6A1 U8 TOP VIEW



A6A1 K2 TOP VIEW



CABLE PLUG TO A6A1 J1



Schematic General Information

P/O A6A1 FM VCO ASSEMBLY (08642-60101)

FM OUT 17 GI — W20 — 967 — J4

LOW-PASS FILTER: L10 180n; C89 150p

AUDIO FOR ANGLE MODULATION

SERIAL DATA INTERFACE

FM CONTROL LINES 11 IF — 2

P/O A5 DISTRIBUTION ASSEMBLY SS64

P/O J1: 23 FM CLK — FL3 — U16C (NOTE 2); 25 FM DATA — FL2 — U16A (NOTE 2)

+5V (F1); C70 0.1µ

U17 SR68; U18

MUX SELECT LINES IB 23 — S2, S1, 3 Hz/OPL, S0

U19A; U19B; R77 1k +5V (F1); C71 0.1µ

FM LOOP DISABLE HV 23

DCFM SELECT HZ 23

COUNTER CONTROL LINES 11 IG — 3

13 COUNT PERIOD SELECT — FL8

15 COUNTED SIGNAL SELECT — FL7

17 TAKE READING STROBE — FL6

COUNTER CLOCK 11 IH — 19 COUNTER CLK — FL5

COUNTER OUTPUT 20 AO — P/O J5: 5 — FL4

4

POWER SUPPLY AND GND

FL10

-5V — -5V (F1)

+50V (F1) — +50V (F1)

+15V (F1) — +15V (F1)

+5V (F1) — +5V (F1); LB 3µ; +5V (F3); C78 0.01µ

-15V (F1) — -15V (F1)

GND — GND

POWER SUPPLY AND GND 23 HU — 6

4

PHASE MODULATION SELECT

PM ENABLE SWITCH

+5V (F1); CR8; K2; U11A 1,2 3

R48 4220; R47 511; R46 75

PM IN BW

PM CROSSOVER; C45 0.047µ

PM CROSSOVER ADJ. R49 100 CW; R90 121

PM OUT BW

FM OUT BW — 2

FM IN BW

FM CROSSOVER

SWITCH DRIVE

LOW FREQUENCY FEEDBACK

U20B; +15V (F1); -15V (F1); 3 Hz/OPL; R94 10K

+15V; R78 6190; R79 1K

C43 1,25µ; R43 75K; R38 1.1M; C

Q9; R42 90.9K

C45 0.1µ; U8; R40 619K; R39 619K; R41 68.1K

GUARD TRACE

CROSSOVER IN/OUT; R45 196k

C44 0.1µ

CROSSOVER INTEGRATOR

U21; SUMMING AMP

R34 1960; C41 0.12µ

C39 0.1µ

FM CROSSOVER ADJ

U7A; U7B

R32 1960; R92 1960; R35 3160; R36 1K CW

C38 0.1µ

SERIAL PREFIX: 2427A

PHASE MODULATION SELECT

PM ENABLE SWITCH

+5V (F1)

CR8

K2

U11A

R48 4220

R47 511

R46 75

PM IN BW

PM CROSSOVER

C46 0.047 µ

PM CROSSOVER ADJ.

R49 100

R90 121

PM OUT BW

VREF

FM OUT BW

SHAPER

SHAPER TEST FIXTURE

TP2

SHAPE TEST ADJ

TP1

R69

ANALOG FET SWITCHES

P/O +15V (F1)

U14

EN

X1

X2

VRef

-15V (F1)

U15A

+15V (F1)

C68 0.1µ

SHAPING

SHAPE ADJ.

P/O S1

R70 (NOTE 4)

R71 (NOTE 4)

R72 1k

R83 100k

C69 0.1µ

Q14 (NOTE 4)

MP1 (NOTE 4)

FM/PM LINE SELECT

U12

+15V (F1)

EN

X1

X2

VRef

PM OUT BW

FM OUT BW

FM IN BW

PM IN BW

ANGLE MOD OUTSIDE BW

ANGLE MOD INSIDE BW

HY 23

-15V (F1)

FM CROSSOVER

SWITCH DRIVE

LOW FREQUENCY FEEDBACK

U20B

+15V (F1)

3 Hz/OPL

R94 10K

-15V (F1)

+15V

R78 6190

R79 1K

C43 1.25 µ

R43 75K

R38 1.1M

C42 0.082 µ

Q9

R42 90.9K

C45 0.1µ

U8

R40 619K

R39 619K

R41 68.1K

GUARD TRACE

C44 0.1µ

R45 196k

CROSSOVER IN/OUT

U21

X1

X2

VREF

R32 1960

R92 1960

CROSSOVER INTEGRATOR

SUMMING AMP

R34 1960

C41 0.12 µ

U7A

C39 0.1 µ

FM CROSSOVER ADJ

R35 3160

R36 1K

U7B

TP6

C38 0.1µ

FM IN BW

DCFM REFERENCE

C61 1µ

DCFM CTR FREQ ADJ

GUARD TRACE

R65 100k

R66 10k

OPERATIONAL AMPLIFIER

+50V (F1)

C62 0.01µ

R67 2370

Q12

U13

C63 0.1µ

R96 5110

Q13

C66 0.47p

R64 19.6K

R97 1210

C64 0.1µ

C65 15p

R68 1330

R62 4530

R95 5110

R63 15.2k

C60 4µ

VR1 6.3V

SHAPER

GAIN TEST FIXTURE

SHAPER TEST FIXTURE

ANALOG FET SWITCHES

SHAPING

FM/PM LINE SELECT

DCFM REFERENCE

OPERATIONAL AMPLIFIER

160 Hz LOW-PASS FILTER

ATTENTION Static Sensitive Devices

P/O 08642-60001

P/O A6FL2 (NOTE 3)

P/O A5 SS64

SS24

Figure 8K-115

8K-115

A7 Module

Troubleshooting and Adjustments Contents

Troubleshooting

Adjustments

A7 Critical Specifications

Troubleshooting

A7 TROUBLESHOOTING INFORMATION

Before Proceeding With Module Troubleshooting

- You should have confidence that A7 is the faulty module based on the results of Module Level Diagnostics (MLD).
- Open the manual to the foldout on page 8L-100. There are 3 diagrams of the A7 module. One of the diagrams is titled Simplified Block Diagram. It is intended to be used to understand the operation of A7. (There is a brief discussion of the circuit operation on page 8L-3).
- Open the next foldout on page 8L-101 (BD9). There, you will see a more detailed Block Diagram of the SAWR loop. **This Block Diagram is meant to be used during Checks 1 and 2.** Notice there is one assembly shown, A7A1. This assembly is shown on two Service Sheets, SS25 and SS26.
- The objective of Troubleshooting Checks is to isolate the malfunction to an area of circuitry represented on one Service Sheet. The Checks are intended to be done in the order they are numbered.
- Once the malfunction is isolated, refer to the Component Level Repair Directory. There, you will find information useful for locating faulty components.
- Specification failures (for example, phase noise, spurs, etc.) might not be found by Troubleshooting Checks. Manual Adjustment Procedures can be done, and the HP 8642 then re-tested to see if the specific failure condition still exists. At this point, if repair is necessary, Module Performance Checks may be helpful to pinpoint a failure condition in the module.

Overall Equipment List

Signal Generator No.1	45 MHz, 8 dBm
Signal Generator No.2	HP 8642A/B
Oscilloscope	HP 1980B
DVM	HP 3456A
Spectrum Analyzer	HP 8566A/B
HP 8642 Bench Service Kit	HP 11802A

Essentials of A7 Module Operation

Refer to the Simplified Block Diagram opposite the foldout on BD9. The A7 Module contains one phase locked loop circuit. The phase locked loop employs a sampling **PHASE DETECTOR** which enables the circuit to lock to multiples of the reference signal. The SAWR Oscillator Select Lines, SAWR A and SAWR B, are decoded to select one of three Surface Acoustic Wave Resonator (SAWR) oscillators. The decode circuitry is shown on SS26 (see **OSCILLATOR SELECT**). Each oscillator frequency is a multiple of 22.5 MHz. (The SAWR 45 MHz timebase signal divided by 2).

The SAWR Oscillator Output is the UHF reference for the A11 Reference Loop Module. Depending on which of the three oscillators is selected, the SAWR Oscillator Output can be 742.5, 787.5, or 832.5 MHz.

See the A7 Module block diagram (BD9, page 8L-101) for further understanding of the A7 Module's internal operation.

CHECK 1: A7 PHASE DETECTOR/INTEGRATOR CIRCUITRY (SS25)

NOTE

Use the Module Test Point/Adjustment Locations diagram on the foldout opposite BD9 to locate test points on A7A1. Test point designators ((XX)) will be used when applicable. Points not located on the Module Test Point/Adjustment Locations diagram can be found using the Component Locator diagrams opposite SS25 or SS26.

Essentials of SS25 Circuit Operation

Service Sheet 25 shows the **RF TO TTL TRANSLATION, PHASE DETECTOR, INTEGRATOR, LOW PASS FILTERS, LOOP LIMITING** and **ISOLATING AMPLIFIERS, SAWR LOOP DIAGNOSTICS, POWER SUPPLY** and **GND** circuitry.

The **RF TO TTL TRANSLATION** circuitry, translates the 45 MHz timebase signal to a TTL signal and then divides it by two resulting in a 22.5 MHz TTL signal.

The **PHASE DETECTOR** circuitry produces a 22.5 MHz comb signal in the **PULSE TRAIN GENERATOR**, which is used to drive the **SAMPLING MIXER**. The other input to the **SAMPLING MIXER** is the output from one of the three Surface Acoustic Wave Resonator **(SAWR)** oscillators from SS26 through the **LOOP LIMITING** and **ISOLATION AMPLIFIERS**. The output from the **SAMPLING MIXER** is an error signal generated by the difference in phase between the **SAWR** oscillator and the 22.5 MHz harmonic of the same frequency.

The **INTEGRATOR** circuitry integrates the error signal and outputs a voltage of the same sign and proportional to the phase difference between the **SAWR** oscillator and the 22.5 MHz harmonic. The **INTEGRATOR** has two bandwidths, 700 Hz when the loop is locked and approximately 10 KHz when the loop is unlocked. This allows for fast loop acquisition when switching to a different **SAWR** oscillator.

The **LOW PASS FILTERS** remove unwanted sampling products from the **SAWR** oscillator tune voltage. Two bandwidths are used. A 6.6 KHz low pass filter is switched in when the loop is locked. It is followed by a 20 MHz low pass filter. The output from the filters goes to SS26 and is the **SAWR** oscillator tune voltage. The **LOOP LIMITING** and **ISOLATION AMPLIFIERS** amplify and limit the **SAWR** oscillator output (SS26) and isolate it from the **SAMPLING MIXER.**

The **SAWR LOOP DIAGNOSTICS** sense three points for an out of lock condition;

1. If the 45 MHz signal at A7A1J2 is not received by the phase detector, an acquisition signal will be present at U9 Pin 7.

2. If there is a difference in phase between the two phase detector inputs, a beat note will be at U3 Pin 6.

3. If the UHF Reference loop IF signal (output from the **LOOP LIMITING** and **ISOLATING AMPLIFIERS)** is not present, this condition will be sensed by the Loop IF sense line.

If one of these conditions exists, U11 (one shot multivibrator) will hold the out of lock line low through U8B for 10 ms. The out of lock line also changes the bandwidths on the **INTEGRATOR** and **LOW PASS FILTERS THROUGH U10**. The out of lock line will stay low until the out of lock condition is resolved.

The **POWER SUPPLY** and **GND** circuitry filters and de-couples the power supplies for the A7 **SAWR LOOP ASSEMBLY.**

Description of Check 1

The first test of Check 1 verifies that the power supply voltages on the A7A1 circuit board are correct.

Then, the operation of the Phase Detector, Integrator, and related circuitry is tested using signal substitution to simulate a difference in frequencies being sampled at the phase detector.

The last test is the SAWR Loop Diagnostics. This test also uses signal substitution to simulate out of lock conditions. An Oscilloscope is used to observe the integrator and diagnostic lines during out of lock conditions.

Required Equipment:

Signal Generator No.1* ..... 45 MHz, 8 dBm
Signal Generator No.2 ..... HP 8642A/B
Oscilloscope ..... HP 1980B
DVM ..... HP 3456A

*The 45 MHz signal from A6A2 J8 (W28) can be used if A6 passed MLD or is known to be good.

Test the Power Supplies

1. Setup:

   Extend the A7 module on extender posts (Refer to DISASSEMBLY PROCEDURES in the Service Manual or MECHANICAL PROCEDURES in the On Site Service Manual).

   Remove the A7A1 cover.

2. Measure Voltage Levels:

   Check power supply lines at the points given in Table 8L-1 with the DVM. (Locations can be found on the A7A1 Component Locator opposite SS25).

Table 8L-1. *A7 Power Supply Lines*

Component	Nominal Voltage
L 105	≈ +15V
L 112	≈ +15V
L 9	≈ −15V
L 1	≈ +5V

Test the Phase Detector, Integrator, and Related Circuitry

3. Setup:

   Switch the HP 8642 to STANDBY.

   Set Signal Generator No.1 to 45 MHz and 8.0 dBm output. (45 MHz signal from A6A2 J8 can be used if known good.)

   Set Signal Generator No.2 to 742.6 MHz and 0 dBm output.

   Lock the timebases of Signal Generator No.1 and No.2 together.

   Locate C131 (BF) on test point locator 8L-100, and de-solder the bottom lead on C131 (connected to R138). Bend C131 and remove the de-soldered lead from the board.

NOTE

The A7A1 circuit board may have to be removed from the module casting to de-solder C131 without damaging it. Refer to Disassembly Procedures in Service Manual.

Connect Signal Generator No.1 to A7A1 J2 (AY) . If the A6A2 J8 (AY) output is being used as Signal Generator No.1, it will already be connected to A7A1 J2.

Inject the signal from Signal Generator No.2 at the de-soldered lead of C131 (BE) .

Connect the Oscilloscope to A7A1 L102 (BF) (SAWR OSCILLATOR TUNE VOLTAGE).

Switch the HP 8642 to ON.

4. Verify Waveforms (Phase Detector and Integrator Outputs):

Enter the following special function sequence:

[SHIFT] [SPCL] [3] [6] [0] [1] [3] [0] [HZ] [6] [0] [1] [3] [1] [HZ]. This turns off all of the SAWR oscillators to insure that they do not interfere with these checks. (The front panel display should show a "1" indicating that a bit was set to its high state).

Adjust the Oscilloscope (DC coupled) so that the display appears similar to Figure 8L-1. This sweep-to-lock signal should be between +20 and +30 Volts peak to peak with a 10 mS time period.

Adjust the Oscilloscope (DC coupled) so that the display appears similar to Figure 8L-2. This is a 100 kHz beat note signal superimposed on the sweep-to-lock signal. The beat note amplitude should be approximately +.5 to +1 Volts peak to peak.

Change the frequency of Signal Generator No.2 to 745 MHz.

Adjust the scope so that the display is similar to Figure 8L-3. The signal should be approximately 25 Volts peak to peak with approximately a 250 mS time period. Notice that at the end of each 250 mS cycle (sawtooth waveform) there is 1 cycle of a 10 mS signal (triangle waveform).

Move the Oscilloscope probe to FL9 (BG) (TUNE VOLTAGE SENSE), located in the upper right corner of the A7A1 components locator.

The signal should be similar to Figure 8L-4.

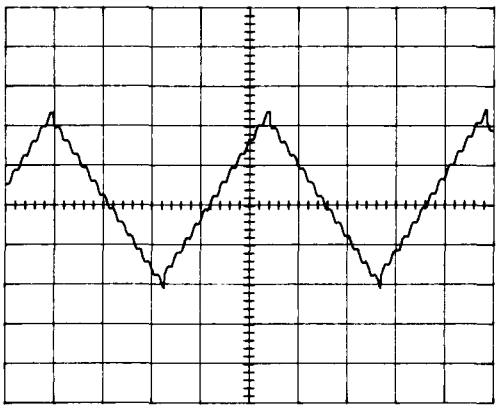


Figure 8L-1. *5.0V/DIV 2.0mS/DIV*

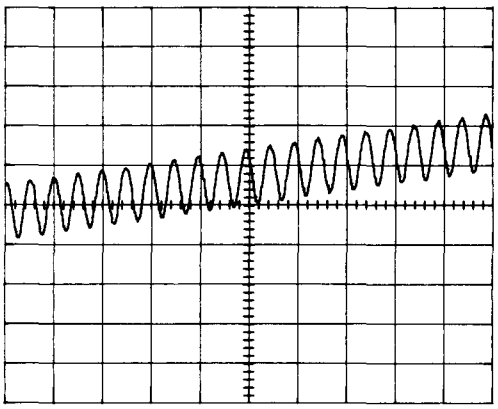


Figure 8L-2. *Delayed 0.5V/DIV 2.0μS/DIV*

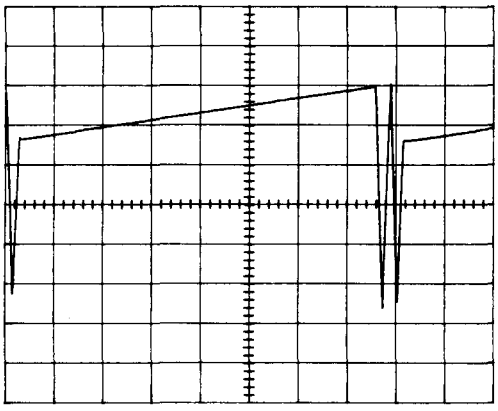


Figure 8L–3. *1.0/div 30.0mS/div*

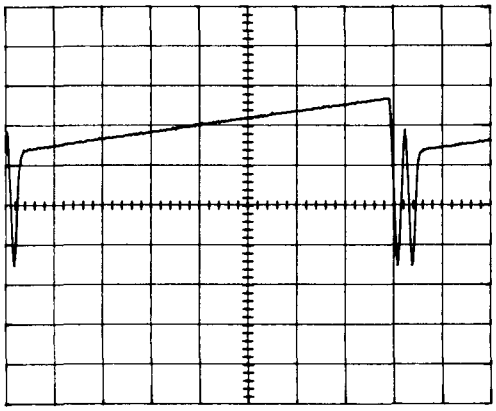


Figure 8L–4. *2.0v/div 50.0mS/div*

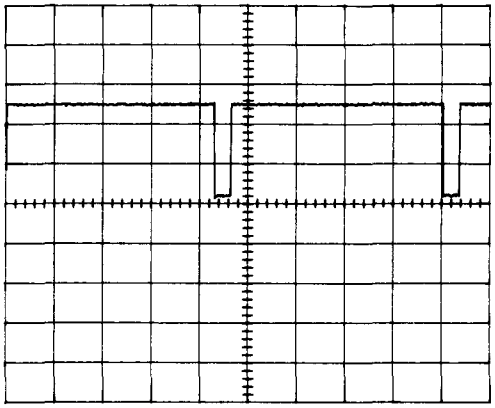


Figure 8L–5. *2.0/div 50.0mS/div*

Test SAWR Loop Diagnostic Circuitry

5. Setup:

   Ensure that Signal Generator No.2's frequency is 745.0 MHz. (Signal Generator No.2's amplitude should be 0 dBm).

   Using the Component Locator on page 8L-102, locate FL14.

   Connect the Oscilloscope to A7A1 FL14 (BH) .

6. Verify Waveforms (SAWR Loop Diagnostics outputs):

   Change Signal Generator No.2's output frequency as indicated in Table 8L-2. Verify that the Oscilloscope display is correct for all FL14 settings.

   Using the Component Locator opposite SS25, locate FL12. Connect the Oscilloscope to A7A1 FL12.

   Change Signal Generator No.2's output frequency as indicated in the Table 8L-2. Verify that the Oscilloscope display is correct for all FL12 settings in Table 8L-2.

Table 8L–2. *SAWR Loop Diagnostic Points*

TEST POINT	SIGNAL GENERATOR #2 FREQUENCY	OSCILLOSCOPE DISPLAY
FL14 (BH)	745.0 MHz	Figure 8L–5
FL14 (BH)	742.6 MHz	≈0 Vdc
FL14 (BH)	REMOVED*	≈0 Vdc
FL12 (BH)	REMOVED*	≥3.4 Vdc
FL12 (BH)	742.6 MHz	2.5 to 3.4 Vdc
* Signal Generator #2 should be removed at A7A1 C131. Re-solder A7A1 C131 into place on the A7A1 board.		

Restore Module

7. Re-solder A7A1 C131 into place on the A7A1 board.

CHECK 2: A7A1 SAWR OSCILLATORS CIRCUITRY (SS26)

Essentials of SS26 Circuit Operation

Service Sheet 26 shows the **OSCILLATOR SELECT, 742.5, 787.5** and **832.5 MHz SAWR OSCILLATORS**, and the **OUTPUT LIMITING AND ISOLATION AMPLIFIERS** circuitry for the A7 **SAWR LOOP ASSEMBLY**.

The **OSCILLATOR SELECT** circuitry decodes the **SAWR A** and **SAWR B** ((BI)) lines, and supplies collector current through Q7 to the selected **SAWR** oscillator.

The three **SAWR OSCILLATORS** are identical with the exception of the **SAWR** (Y1, Y2 and Y3) frequency (refer to the 742.5 MHz **SAWR OSCILLATOR** for this discussion). The **SAWR** device (Y3) is the high Q tank for the feedback in this common emitter oscillator. The varactors (CR109, CR110) allow the oscillator to be pulled in frequency by + 130 ppm and − 80 ppm. (ppm = parts per million).

The **OUTPUT LIMITING** and **ISOLATION AMPLIFIERS** supply the output from the A7 **SAWR LOOP ASSEMBLY** at A7A1J3. The **UHF REFERENCE LOOP IF** ((BE)) signal comes from the collector of Q103 and is feedback to the **LOOP LIMITING** and **ISOLATING AMPLIFIERS** on SS25.

Description of Check 2

This check selects each of the SAWR oscillators individually and checks for proper **OSCILLATOR SELECT** input states, output frequency and level, and UHF Reference Loop IF level. The Spectrum Analyzer is used to verify UHF levels and frequency, and a DVM is used to verify the input select line states. Then, the pull range of the voltage controlled SAWR oscillators is tested by varying the input (control) voltage while observing the output frequency on a Spectrum Analyzer. If a SAWR oscillator does not have sufficient pull range to pass this test, the SAWR device (Y1, Y2, or Y3) should be checked.

If any test fails during CHECK 2, refer to the Component Level Repair Directory.

Required Equipment:

Signal Generator No. 2	HP 8642A/B
DVM	HP 3456A
Spectrum Analyzer	HP 8566A/B
HP 8642 Bench Service Kit	HP 11802A
RF Probe	1250-1589

Test the Oscillator Select inputs and SAWR Oscillator Output (SS26)

1. Setup:

   Switch the HP 8642 to standby.

   Remove W25 from A7A1 J3.

   Connect the Spectrum Analyzer to A7A1 J3 (BJ) (SAWR Oscillator Output)

   Switch the HP 8642 to ON.

2. Measure Levels:

   On the HP 8642, key in each of the frequencies from Table 8L-3 and verify correct TTL levels at A7A1 FL4 (BI) (SAWR A) and A7A1 FL5 (BI) (SAWR B) with the DVM. Next, observe the SAWR Oscillator Output on the Spectrum Analyzer display. Then, with the RF probe measure the UHF Reference Loop IF at the collector of Q103 (see Component Locator on page 8L-104).

Table 8L–3. *SAWR Oscillator Select Lines and Output*

Front Panel Frequency	SAWR Oscillator Select Lines (BI) *		UHF Level ** (Collector Q103)	SAWR OUTPUT (A7A1 J3)	
	SAWR A (FL4)	SAWR B (FL5)		Frequency	Level
550 MHz	0	1	≈0 dBm	742.5 MHz	≈4 dBm
600 MHz	1	0	≈0 dBm	787.5 MHz	≈4 dBm
650 MHz	0	0	≈0 dBm	832.5 MHz	≈ 4 dBm

* SAWR A and SAWR B levels are listed in TTL logic levels. Logic level "0" is less than 0.8 Vdc and logic level "1" is greater than 2.0 Vdc.

** UHF Reference Loop IF level is measured with a Spectrum Analyzer using a 1000 pf RF probe, HP part 1250-1589 (Part of 11802A Bench Service Kit).

Enter the following special function sequence:

[SHIFT] [SPCL] [3] [6] [0] [1] [3] [0] [HZ] [6] [0] [1] [3] [1] [HZ]

(This turns off the all of the SAWR oscillators)

Verify that the SAWR A and SAWR B (BI) select lines are both at TTL high (greater than 2.0 Vdc), and that there is no output from the A7 module at A7A1 J3 (BJ) .

Test the Voltage Controlled SAWR Oscillators Pull Range

3. Setup:

   Switch the HP 8642 to Standby.

   Set Signal Generator No.1 to sweep up and down between the frequencies of 44.9964 MHz and 45.00585 MHz.

   Set Signal Generator No.2 to ≈ 8 dBm.

   Disconnect W28 (SAWR 45 MHz) at A7A1 J2 (AY) .

   Connect Signal Generator No.2 to A7A1 J2 (AY) .

   Disconnect W25 (SAWR OSCILLATOR OUTPUT) at A7A1 J3 (BJ) .

   Connect the Spectrum Analyzer to A7A1 J3 (BJ) .

   Switch the HP 8642 on.

   Ensure that Signal Generator No.1 is sweeping (HP 8642 will have SWPNG annunciator lit).

4. Measure Power Levels and Observe Frequency Stability:

   For each HP 8642 front panel in Table 8L-4, verify that the output displayed on the Spectrum Analyzer is ≥0 dBm, and a stable frequency, sweeping up in frequency by approximately + 130 ppm and down by − 80 ppm.

Table 8L–4.

HP 8642 Frequency	A7 Output Frequency
550 MHz	742.5 MHz
600 MHz	787.5 MHz
650 MHz	832.5 MHz

COMPONENT LEVEL REPAIR DIRECTORY

The following tables contain information to aid in component level repairs. These tables are designed to be used after the module troubleshooting procedures have verified a failure in circuitry represented on one of the module service sheet schematics. In general the tables supply one of the following types of information:

* Special function codes relevant to the module.
* Transistor emitter, base and collector voltages.
* Frequency and power levels at different circuit points.
* Module control line and power supply interconnections in the module and instrument.

NOTE

Start with the tables that are labeled with a Service Sheet number (Example: **Table 8L-5 SS25 DC Voltage***). Other tables are more general and are to be used at your discretion. It is suggested that you familiarize yourself with the contents of these tables so you can determine if they will be effective in solving your particular troubleshooting need.*

SERVICE SHEET 25

Table 8L–5. *SS25 DC Voltages*

Transistor	Collector	Base
Q4, Q106, Q107	5.1 to 6.5 Vdc	0.3 to 0.9 Vdc

Transistor	Emitter	Base
Q6	1 to 2 Vdc	1.7 to 2.7 Vdc

Table 8L–6. *SS25 RF Power Levels*

Stage	Input Level	Output Level	Stage Gain*
LOOP LIMITING AMPLIFIER	0 to 4 dBm	5 to 10 dBm	≈ 5 dB*

* With an input level low enough to eliminate gain compression, (−49 dBm) the stage gain is approximately 18 dBm. This stage is normally driven into compression.

SERVICE SHEET 26

Table 8L–7. *SS26 DC Voltages*

Transistor	Collector	Base
Q101, Q105, Q108, Q110	5.2 to 6.0 Vdc	0.3 to 0.9 Vdc

Table 8L–8. *SS26 RF Power Levels*

Stage	Input Level	Output Level	Stage Gain*
OSCILLATORS		≈ 0 dBm	
OUTPUT LIMITING AMP	≈ 0 dBm	3.65 to 4.35 dBm	≈ 4 dB*

* With an input level low enough to eliminate gain compression, (−49 dBm) the stage gain is approximately 18 dBm. This stage is normally driven into compression.

Table 8L–9. *Power Supply Lines*

Supply	A17	A5		A7
	Output	Input	Output	Input
+15 Vdc	J2 pins 9-18	J12 pins 9-18	J2 pin 2	J1 pin 2
+5 Vdc	J2 pins 35-50	J12 pins 35-50	J2 pins 1	J1 pins 1
−15 Vdc	J2 pins 19-22	J12 pins 19-22	J2 pin 4	J1 pin 4
GND		Chassis GND	J2 pins 3,5,7,9, 11,13	J1 pins 3,5,7,9, 11,13

Table 8L–10. *Setting Control Lines*

(Refer to Table 8L–14, Control Line Interconnections, for line pin No.'s.)

Enter Service Mode	Select a Function		Select a Line	
SHIFT SPCL 3	6 0 0	Reads line state	2 1 Hz	OOL Disable
	6 0 1	Sets Line to 1	3 0 Hz *	SAWR A
	6 0 2	Sets Line to 0	3 1 Hz *	SAWR B
	6 1 5 **	Continuous Toggle	1 0 9 Hz ***	SAWR OOL

* Selects SAWR frequency (see Table 8L–3 in SS26 troubleshooting.)

** Read is the only function that can be selected for REF OOL.

*** Toggling continues until HP 8642 power is turned off

Example: To read "REF DATA" line state, key in: SHIFT SPCL 3 6 0 0 4 3 Hz

Example: to read "SAWR A" line state, key in: SHIFT SPCL 3 6 O O 3 0 HZ

Table 8L–11. *VM Select Lines*

Enter Service Mode	Function	Line Label	Explanation
SHIFT SPCL 3 2	9 HZ	SAWR SENSE S1 (VCO DETECT)	No VCO > 3.4 Vdc
		(VCO Detect)	VCO present 3.2 to 3.4 Vdc
	1 0 HZ	SAWR SENSE S2	
		(Tune Voltage)	

Example: SHIFT SPCL 3 2 0 would output the VCO detect voltage to A4TP3 (VM OUT) and the display.

Table 8L–12. *A7 Output Specifications*

Output Power Level	3.65 to 4.35 dBm
Spurs	< − 100 dBc
Harmonics 2nd	< − 10 dBc
Pull Range	− 80 ppm to + 130 ppm
Time Base Return Power	< − 60 dBc

Table 8L–13. *A7 Special Functions*

Enter Service Mode	Select a Function	
SHIFT SPCL 3	6 2 0 0 Hz	Reads SAW Selected Output

Table 8L–14. *Control Line Interconnections (Between Modules)*

Line Label	A7	A5		A4	
	Input Connector Pin	Output Connector Pin	Input Connector Pin	Output Connector Pin	Latch IC Pin
OOL Disable*					U13 15
SAW A	A7J1 10	A5J2 10	A5J16 40	A4P2 40	U14 16
SAW B	A7J1 8	A5J2 8	A5J16 42	A4P2 42	U14 5
SAW OOL	A7J1 12	A5J2 12	A5J15 32	A4P3 32	U35 7

* OOL Disable: Circuitry Located on A4. Disables all out of lock interrupts to the DCU.

Adjustments

DESCRIPTION OF A7 ADJUSTMENTS

Overall Equipment List

Oscilloscope ..... HP 1980B
Measuring Receiver ..... HP 8902A
Sensor Module ..... HP 11722A

NOTE

Each adjustment procedure assumes the HP 8642 cabling is connected normally and all circuitry is functioning properly.

Whenever a repair has been done to A7, this manual adjustment procedure must be followed to be sure that the module meets its specifications.

In the adjustment the DC Voltage Compensation Adjustment (**INTEGRATOR** circuitry SS25) is adjusted for symmetry and maximum frequency on the loop acquisition signal. Then the power level out of the module is adjusted in the **OUTPUT LIMITING** and **ISOLATION AMPLIFIERS** (SS26) for proper levels.

ADJUSTMENT 1: A7 MODULE

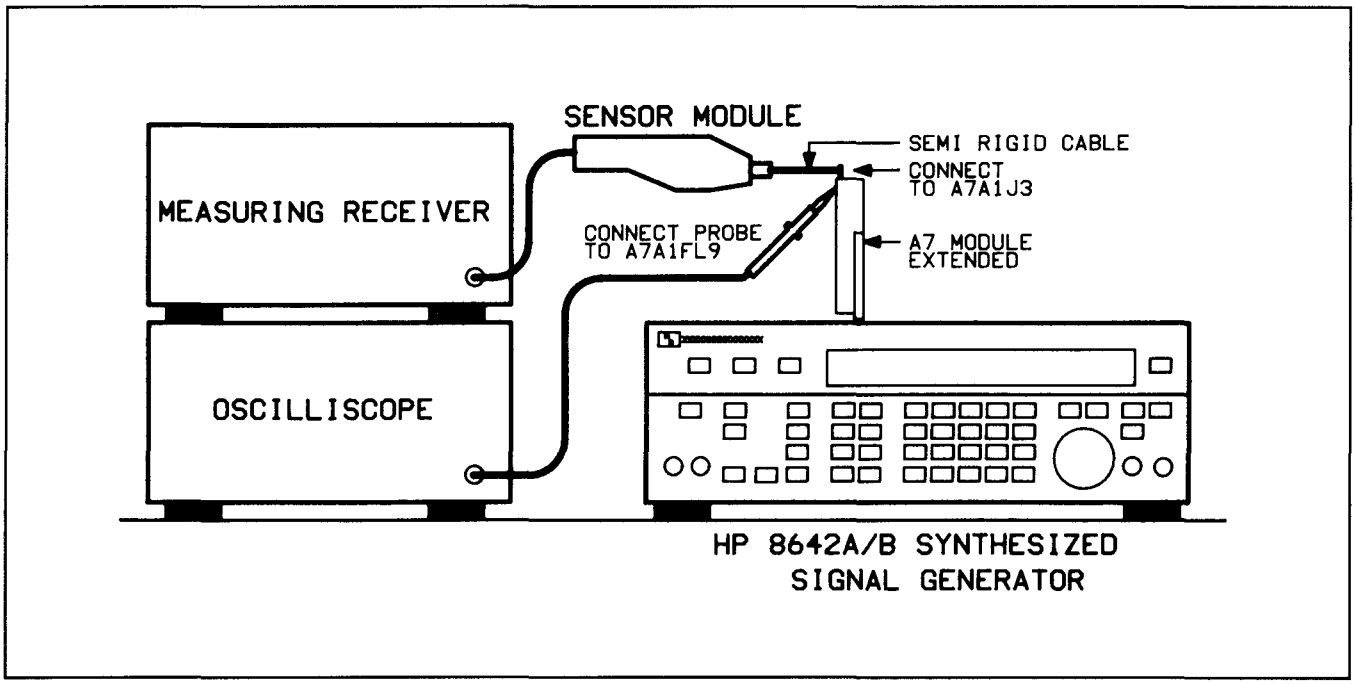


Figure 8L–6. *Set-up 1*

Required Equipment:

Oscilloscope ..... HP 1980B
Measuring Receiver ..... HP 8902A
Sensor Module ..... HP 11722A

Procedure

DC Voltage Compensation Adjustment

1. Setup:(Refer to Figure 8L-6 and 8L-7)

   Extend the A7 module, using extender posts.

   On the HP 8642, key in: [SHIFT] [SPCL] [3] [6] [0] [1] [3] [0] [Hz] [6] [0] [1] [3] [1] [Hz] to disable SAWRs.

   Connect the Oscilloscope probe to A7A1 FL9.

   Set the Oscilloscope to 2 msec/div and 2 volts/div.

2. Adjust:

   If no wave form appears on the Oscilloscope, adjust R33 (Figure 8L-7) until a waveform appears. Adjust R33 for symmetry and maximum frequency. (Symmetry and maximum frequency occur at the same time while adjusting R33. When symmetry and maximum frequency occur the oscilloscope should display a symmetrical sine wave with approximately a 100 Hz frequency and 12 vpp.)

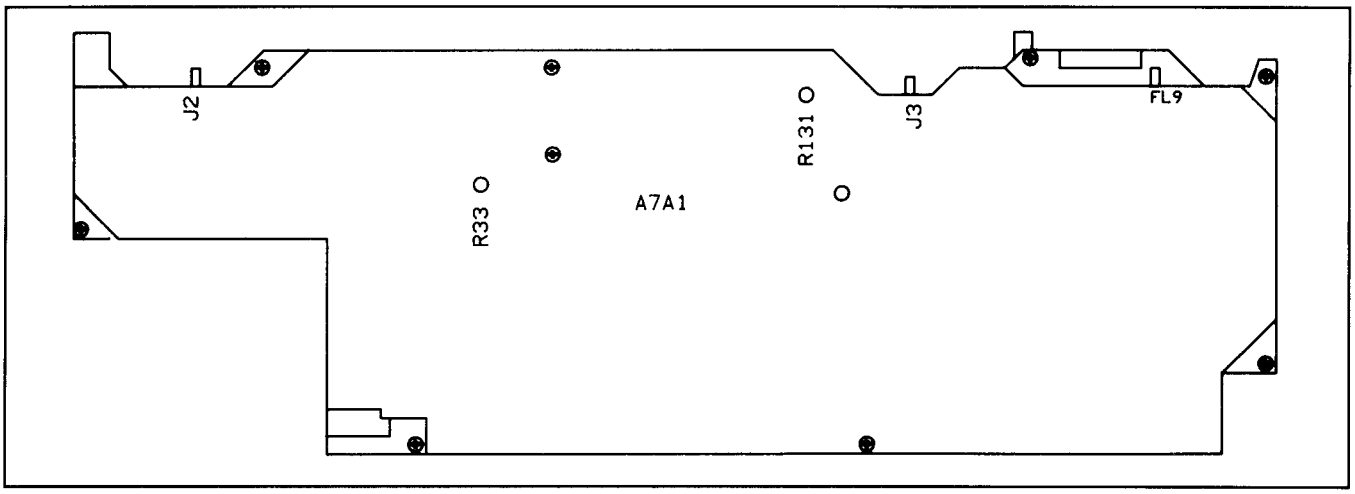


Figure 8L–6. *A7 Module, leftside*

UHF Output Level Adjustment

3. UHF Output level:

   On the HP8642, press INSTR PRESET

   Set the Measuring Receiver to RF Power mode.

   Connect the Measuring Receiver/Power Sensor Module to A7A1J3 through a very short piece of semi rigid cable.

4. Adjust:

   For each HP 8642 frequency listed in Table 8L-15, key in the A7 output frequency into the measuring receiver. (This ensures that the measuring receiver uses the correct calibration factor for the RF Power measurement.) If adjustment is needed recheck all points and re-adjust if needed until all three measurements fall within the limits in Table 8L-15 without needing adjustment.

   Adjust R131 so that the Measuring Receiver reading is between 3.65 dBm and 4.35 dBm for all three settings in the Table 8L-15.

Table 8L–15.

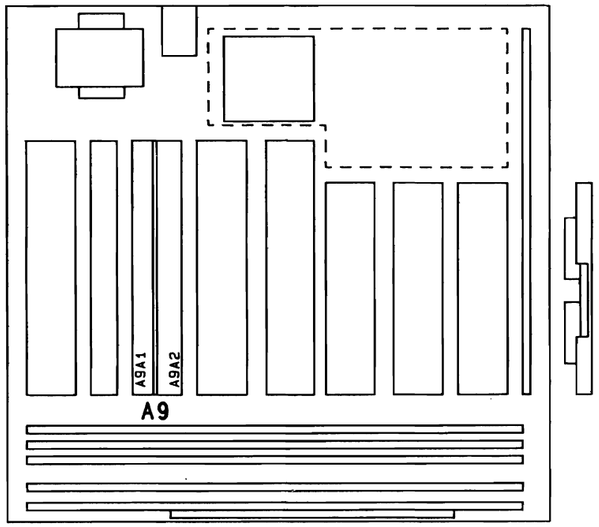
HP 8642 Frequency	A7 Output Frequency	Power Reading (dBm)		
		Min	Actual	Max
550 MHz	742.5 MHz	3.65	_____	4.35
600 MHz	787.5 MHz	3.65	_____	4.35
650 MHz	832.5 MHz	3.65	_____	4.35

A7 CRITICAL SPECIFICATIONS

Table 8L–16. *A7 Output Specifications*

Output Power Level	3.65 to 4.35 dBm
Spurs	< − 100 dBc
Harmonics 2nd	< − 10 dBc
SAWR Oscillator Pull Range	− 80 ppm to + 130 ppm
Time Base Return Power	< − 60 dBc

Assembly Locator



Simplified Block Diagram

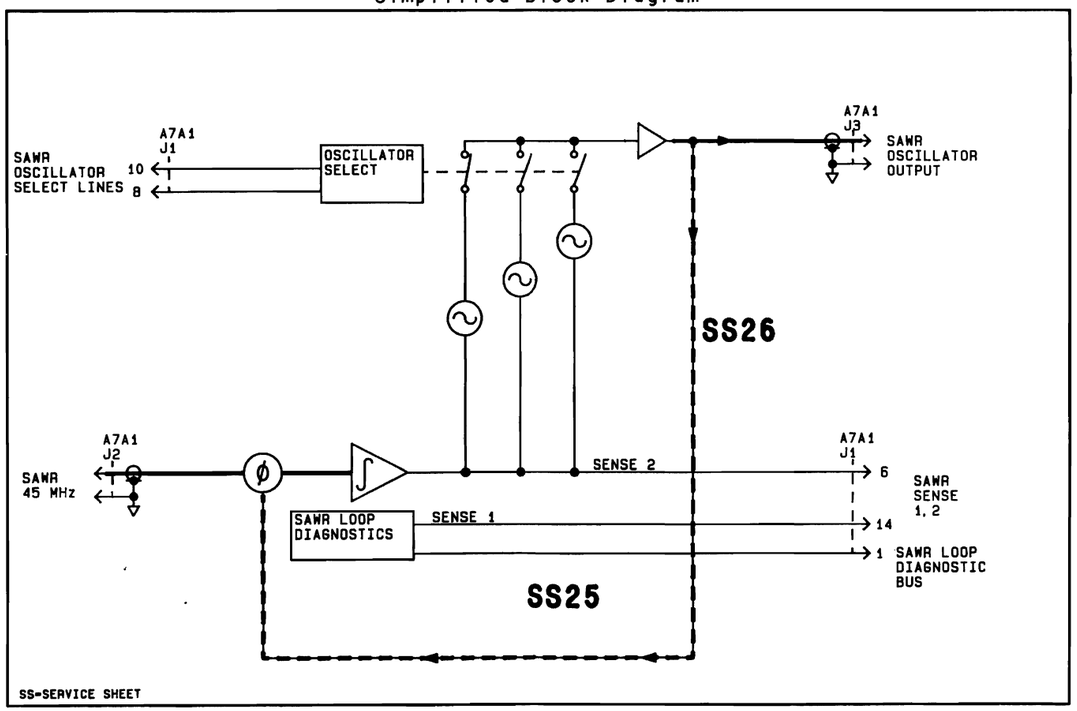
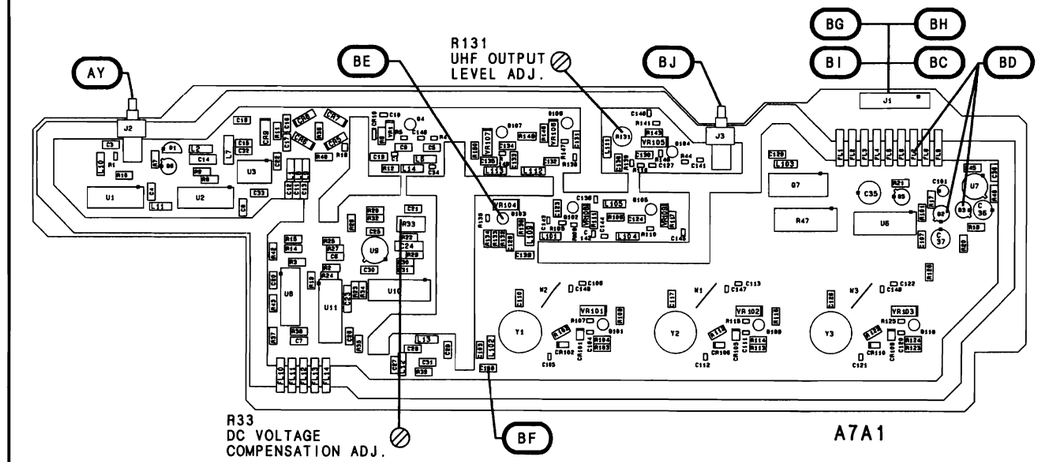


Figure 8L-100 BD9 General Information.

Module Test Point/Adjustment Locations



A7A1 SAWR LOOP ASSEMBLY (08642-60103)

SAWR OSCILLATOR SELECT LINES
BD4 (BI) 2

P/O J1
10 SAWR A
8 SAWR B

OSCIL

25 (BD)

SAWR 45 MHz
BD6 (AY) W28 927

J2

RF TO TTL TRANSLATION (AND DIVIDE BY 2)

PHASE DETECTOR

INTEGRATOR

LOW-PASS FILTERS

TUNE VOLTAGE SENSE (S2)

SAWR LOOP DIAGNOSTICS

ACQUISITION SIGNAL SENSE

BEAT NOTE SENSE

LOOP LIMITING AND ISOLATING AMPLIFIERS

LOOP IF SENSE

SAWR LOOP DIAGNOSTIC BUS

S1

UHF REFERENCE LOOP IF

POWER SUPPLY AND GND
65 (BC) 4

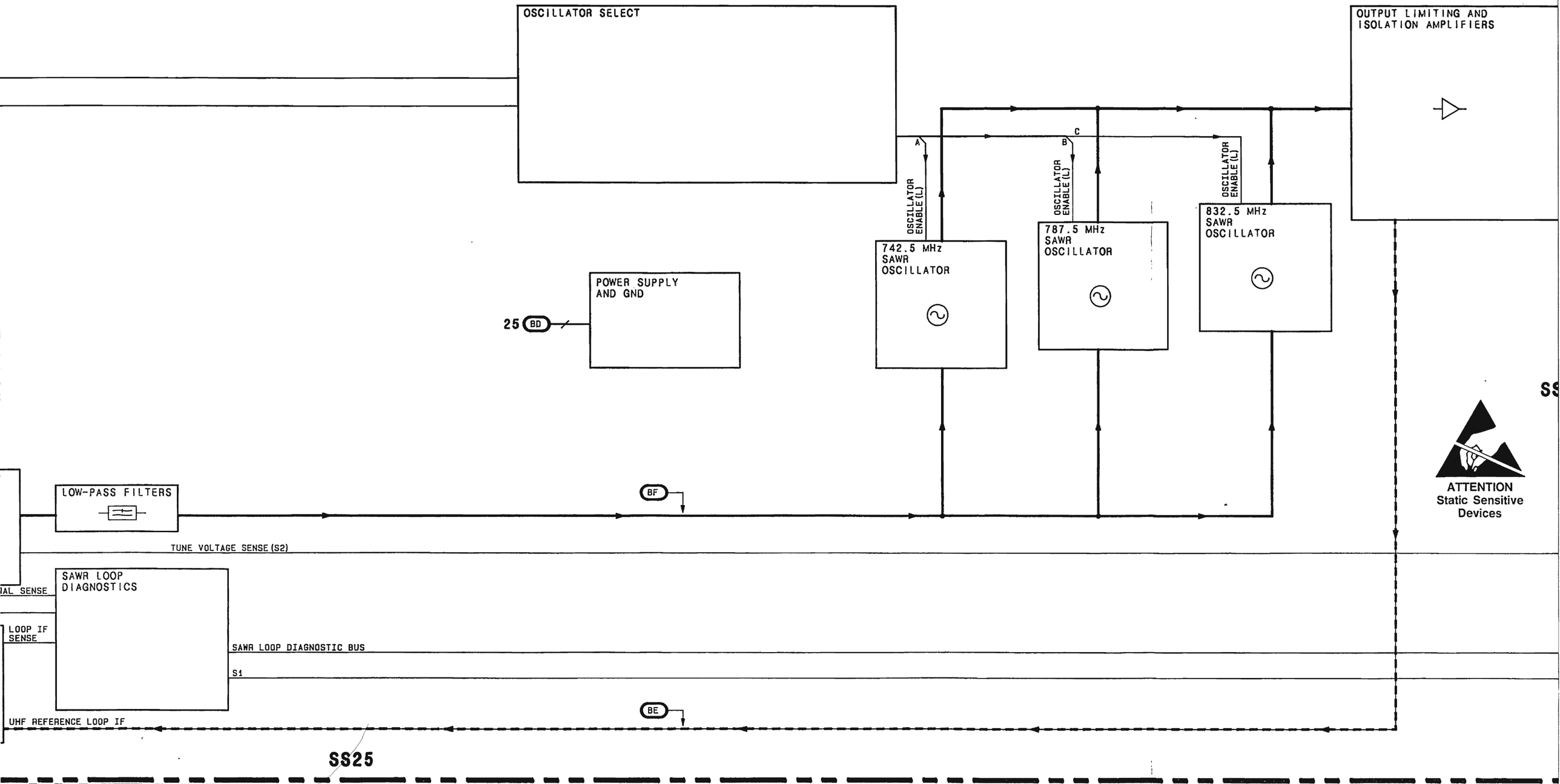
P/O J1
2 +15V
1 +5V
4 -15V
3, 5, 7, 9, 11, 13 GND

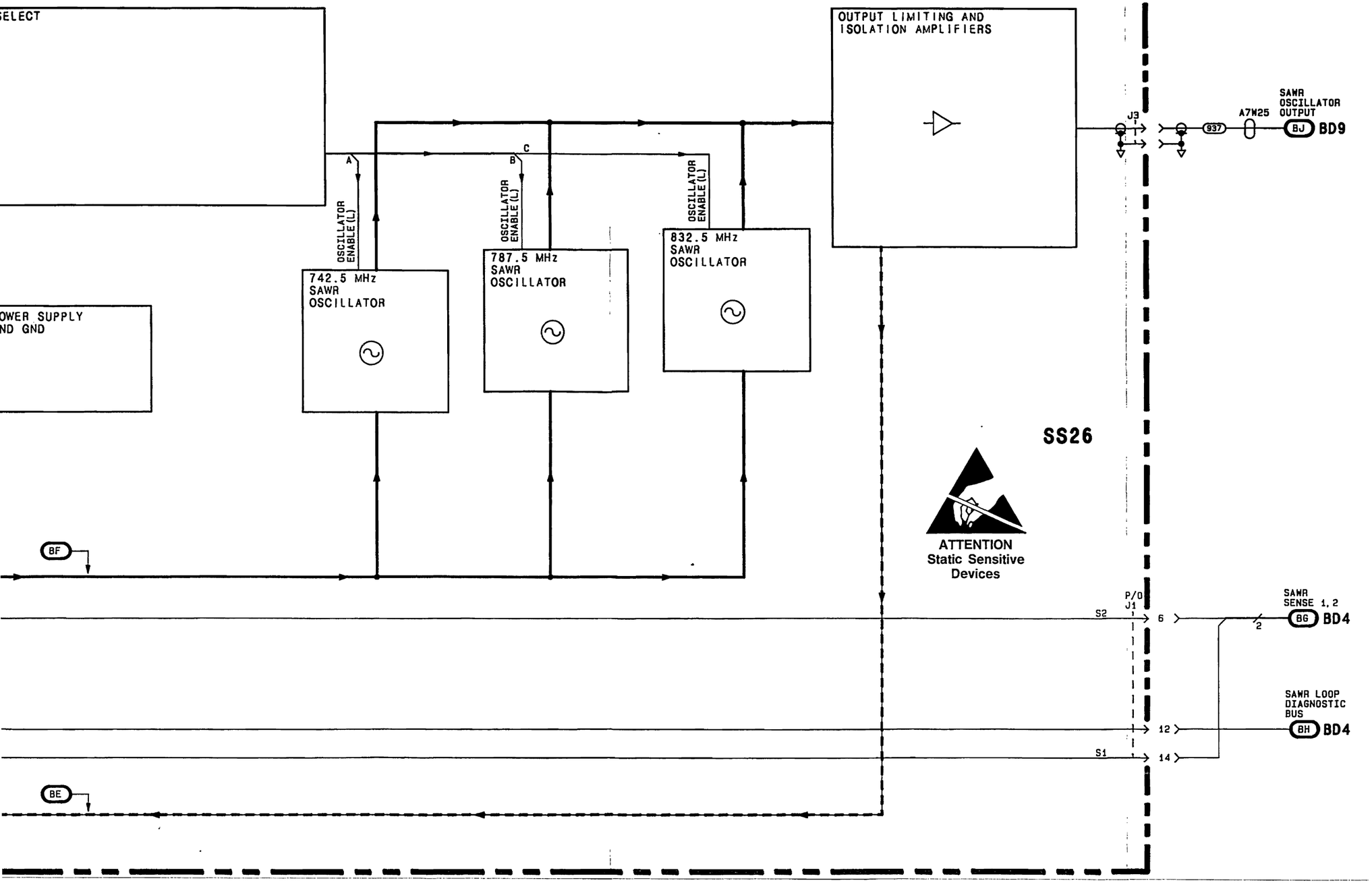
POWER SUPPLY AND GND

8 (BD) 26

SS25

SERIAL PREFIX: 2427A





BD9

Figure 8L-101
8L-101

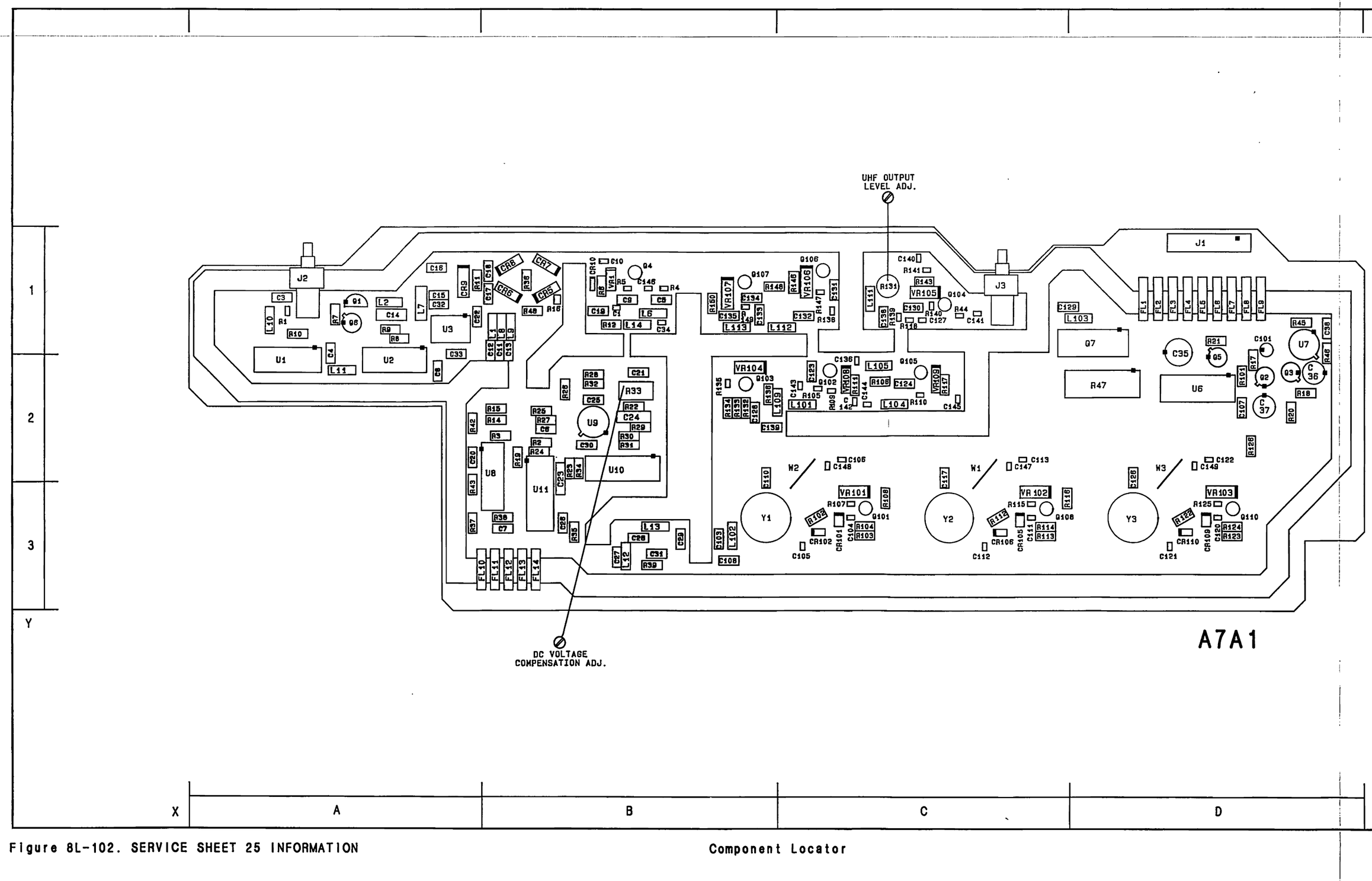
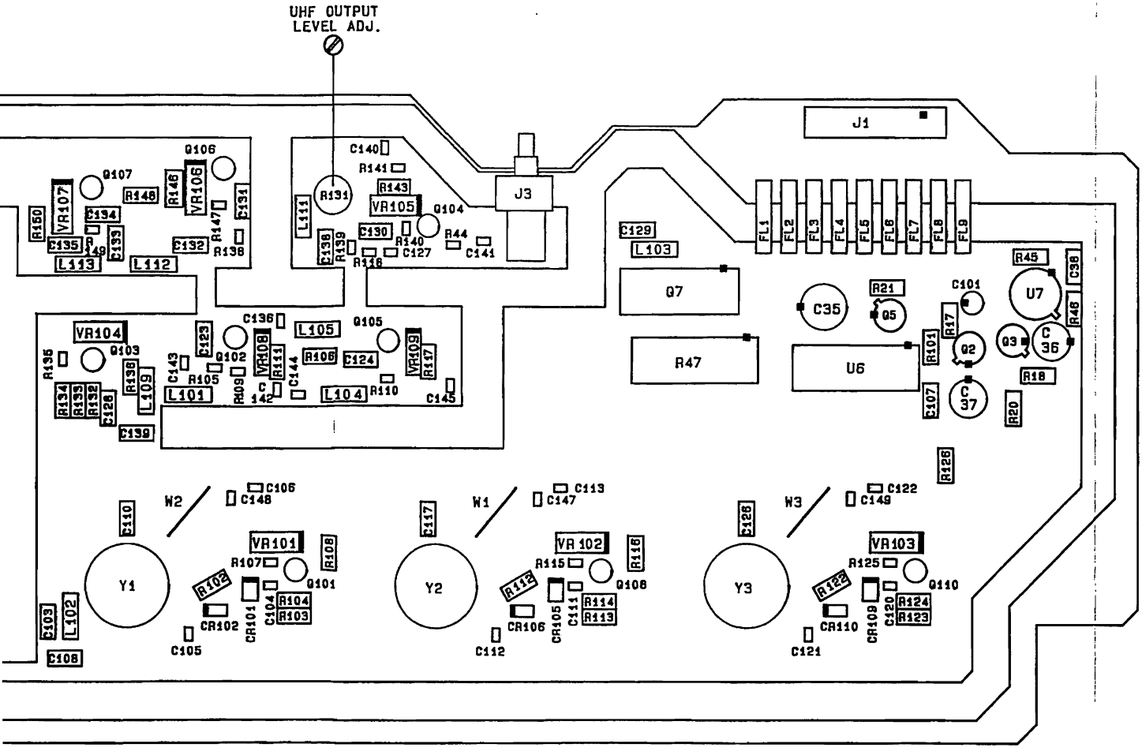
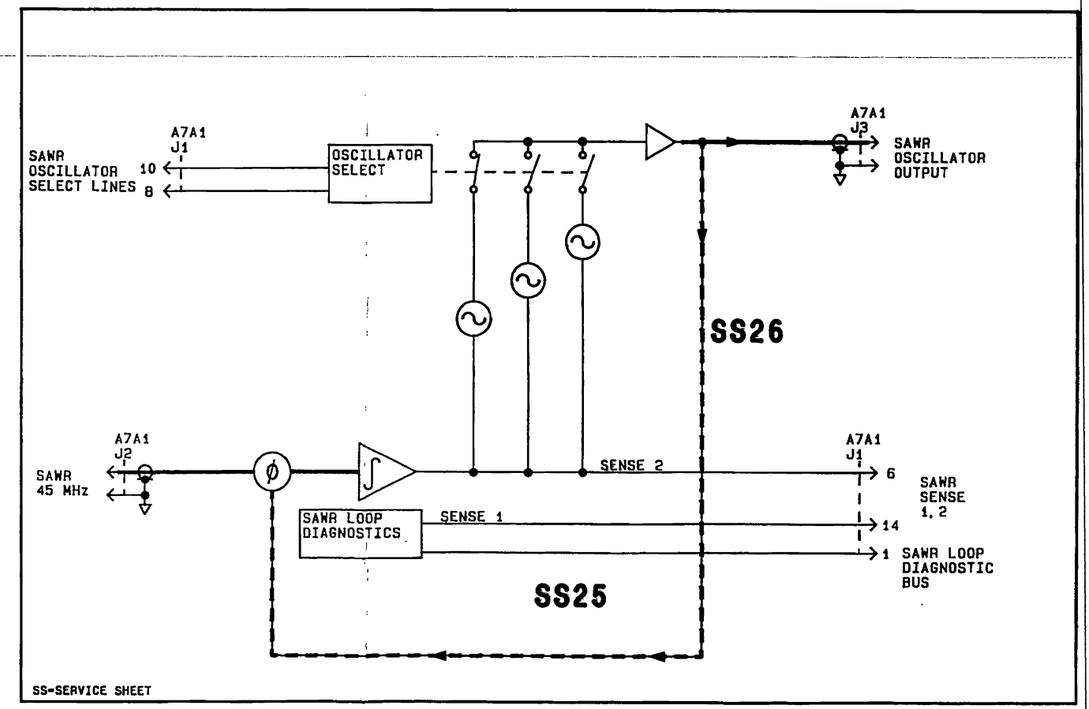


Figure 8L-102. SERVICE SHEET 25 INFORMATION

Component Locator



A7A1



Reference Block Diagram

Component Coordinates

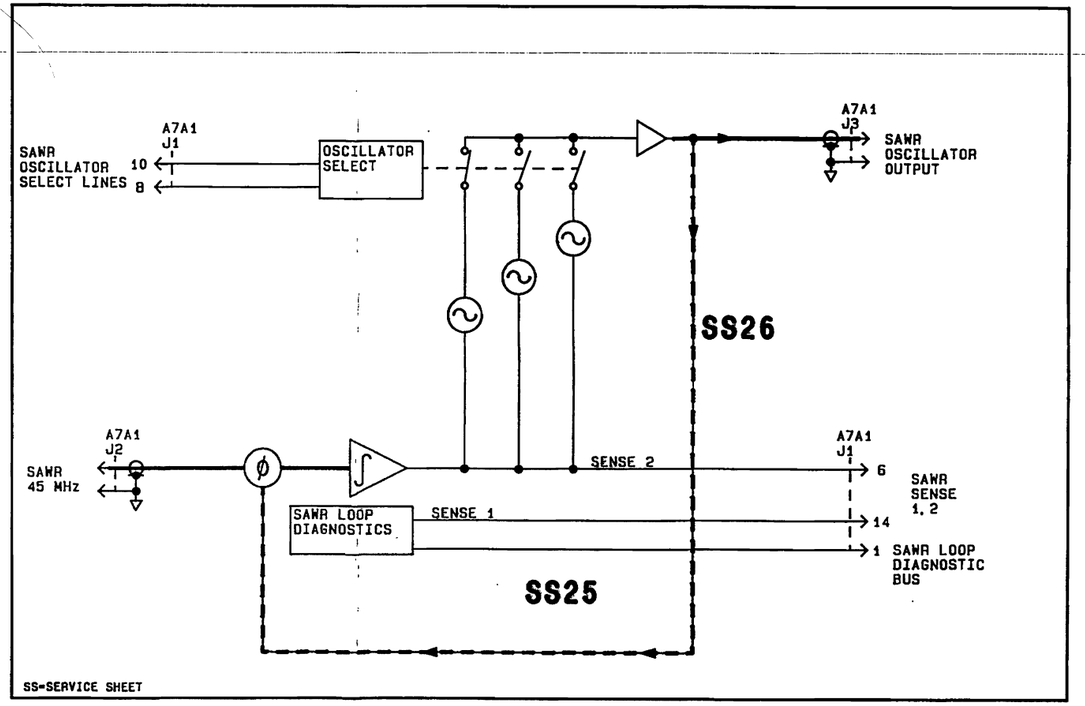
COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	B, 1	C101	D, 1	FL1	D, 1	Q1	A, 1	R30	B, 2						
C3	A, 1	C103	B, 3	FL2	D, 1	Q2	D, 2	R31	B, 2						
C4	A, 1	C108	B, 3	FL3	D, 1	Q3	D, 2	R32	B, 2						
C5	B, 1	C128	B, 2	FL6	D, 1	Q4	B, 1	R33	B, 2						
C6	B, 2	C129	D, 1	FL7	D, 1	Q5	D, 2	R34	B, 2						
C7	B, 3	C131	C, 1	FL8	D, 1	Q6	A, 1	R35	B, 3						
C8	A, 2	C132	C, 1	FL9	D, 1	Q106	C, 1	R36	B, 1						
C9	B, 1	C133	B, 1	FL10	B, 3	Q107	B, 1	R37	A, 3						
C10	B, 1	C134	B, 1	FL11	B, 3			R38	B, 3						
C11	B, 1	C135	B, 1	FL12	B, 3	R1	A, 1	R39	B, 3						
C12	B, 1	C136	C, 2	FL13	B, 3	R2	B, 2	R42	A, 2						
C13	B, 1	C138	C, 1	FL14	B, 3	R3	B, 2	R43	A, 3						
C14	A, 1	C139	B, 2			R4	B, 1	R45	D, 1						
C15	A, 1	C142	C, 2	J1	D, 1	R5	B, 1	R46	D, 1						
C16	A, 1	C143	C, 2	J2	A, 1	R6	B, 1	R48	B, 1						
C17	B, 1	C144	C, 2			R7	A, 1	R138	C, 1						
C18	B, 1	C145	C, 2	L1	B, 1	R8	A, 1	R146	C, 1						
C19	B, 1	C146	B, 1	L2	A, 1	R9	A, 1	R147	C, 1						
C20	A, 2			L6	B, 1	R10	A, 1	R148	B, 1						
C21	B, 2	CR5	B, 1	L7	A, 1	R11	A, 1	R149	B, 1						
C22	A, 1	CR6	B, 1	L8	B, 1	R12	B, 1	R150	B, 1						
C23	B, 2	CR7	B, 1	L9	B, 1	R14	B, 2								
C24	B, 2	CR8	B, 1	L10	A, 1	R15	B, 2	U1	A, 2						
C25	B, 2	CR9	A, 1	L11	A, 2	R16	B, 1	U2	A, 2						
C26	B, 3	CR10	B, 1	L12	B, 3	R17	D, 2	U3	A, 1						
C27	B, 3			L13	B, 3	R18	D, 2	U7	D, 1						
C28	B, 3			L14	B, 1	R19	B, 2	U8	B, 2						
C29	B, 3			L101	C, 2	R20	D, 2	U9	B, 2						
C30	B, 2			L102	B, 3	R21	D, 1	U10	B, 2						
C31	B, 3			L103	D, 1	R22	B, 2	U11	B, 3						
C32	A, 1			L104	C, 2	R23	B, 2								
C33	A, 1			L105	C, 2	R24	B, 2	VR1	B, 1						
C34	B, 1			L109	B, 2	R25	B, 2	VR106	C, 1						
C35	D, 1			L112	C, 1	R26	B, 2	VR107	B, 1						
C36	D, 2			L113	B, 1	R27	B, 2								
C37	D, 2					R28	B, 2								
C38	D, 1					R29	B, 2								

C D

Component Locator

SEE REVERSE SIDE

A7 MODULE **BD9**



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	B, 1	C101	D, 1	FL1	D, 1	Q1	A, 1	R30	B, 2						
C3	A, 1	C103	B, 3	FL2	D, 1	Q2	D, 2	R31	B, 2						
C4	A, 1	C108	B, 3	FL3	D, 1	Q3	D, 2	R32	B, 2						
C5	B, 1	C128	B, 2	FL6	D, 1	Q4	B, 1	R33	B, 2						
C6	B, 2	C129	D, 1	FL7	D, 1	Q5	D, 2	R34	B, 2						
C7	B, 3	C131	C, 1	FL8	D, 1	Q6	A, 1	R35	B, 3						
C8	A, 2	C132	C, 1	FL9	D, 1	Q106	C, 1	R36	B, 1						
C9	B, 1	C133	B, 1	FL10	B, 3	Q107	B, 1	R37	A, 3						
C10	B, 1	C134	B, 1	FL11	B, 3			R38	B, 3						
C11	B, 1	C135	B, 1	FL12	B, 3	R1	A, 1	R39	B, 3						
C12	B, 1	C136	C, 2	FL13	B, 3	R2	B, 2	R42	A, 2						
C13	B, 1	C138	C, 1	FL14	B, 3	R3	B, 2	R43	A, 3						
C14	A, 1	C139	B, 2			R4	B, 1	R45	D, 1						
C15	A, 1	C142	C, 2	J1	D, 1	R5	B, 1	R46	D, 1						
C16	A, 1	C143	C, 2	J2	A, 1	R6	B, 1	R48	B, 1						
C17	B, 1	C144	C, 2			R7	A, 1	R138	C, 1						
C18	B, 1	C145	C, 2	L1	B, 1	R8	A, 1	R146	C, 1						
C19	B, 1	C146	B, 1	L2	A, 1	R9	A, 1	R147	C, 1						
C20	A, 2			L6	B, 1	R10	A, 1	R148	B, 1						
C21	B, 2	CR5	B, 1	L7	A, 1	R11	A, 1	R149	B, 1						
C22	A, 1	CR6	B, 1	L8	B, 1	R12	B, 1	R150	B, 1						
C23	B, 2	CR7	B, 1	L9	B, 1	R14	B, 2								
C24	B, 2	CR8	B, 1	L10	A, 1	R15	B, 2	U1	A, 2						
C25	B, 2	CR9	A, 1	L11	A, 2	R16	B, 1	U2	A, 2						
C26	B, 3	CR10	B, 1	L12	B, 3	R17	D, 2	U3	A, 1						
C27	B, 3			L13	B, 3	R18	D, 2	U7	D, 1						
C28	B, 3			L14	B, 1	R19	B, 2	U8	B, 2						
C29	B, 3			L101	C, 2	R20	D, 2	U9	B, 2						
C30	B, 2			L102	B, 3	R21	D, 1	U10	B, 2						
C31	B, 3			L103	D, 1	R22	B, 2	U11	B, 3						
C32	A, 1			L104	C, 2	R23	B, 2								
C33	A, 1			L105	C, 2	R24	B, 2	VR1	B, 1						
C34	B, 1			L109	B, 2	R25	B, 2	VR106	C, 1						
C35	D, 1			L112	C, 1	R26	B, 2	VR107	B, 1						
C36	D, 2			L113	B, 1	R27	B, 2								
C37	D, 2					R28	B, 2								
C38	D, 1					R29	B, 2								

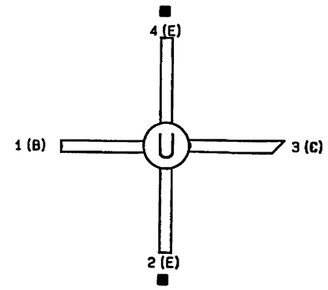
SEE REVERSE SIDE

A7 MODULE **BD9**

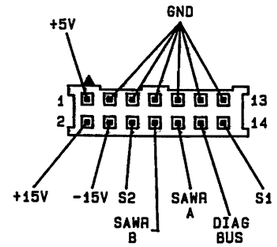
Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. W4-W13 are printed circuit trace inductors.
3. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

A7A1
Q4,106,107
(TOP VIEW)



CABLE PLUG
TO A7A1 J1



Schematic General Information

P/O A7A1 SAWR LOOP ASSEMBLY (08642-60103)

RF TO TTL TRANSLATION

DIVIDE BY 2

PHASE DETECTOR

LOW-PASS FILTER

PULSE TRAIN GENERATOR

SAMPLING MIXER

SAMPLE AND HOLD

POWER SUPPLY AND GND

+15V LOW PASS FILTER

+5V LOW PASS FILTER

-15V LOW PASS FILTER

45 MHz SAWR 22 AY W28 927 J2

P/O J1 +15V

POWER SUPPLY AND GND 65 BC

POWER SUPPLY AND GROUND 8 BD 26

ATTENTION Static Sensitive Devices

LOOP LIMITING AND IS

SERIAL PREFIX: 2427A

LOW-PASS FILTER

PULSE TRAIN GENERATOR

SAMPLING MIXER

SAMPLE AND HOLD

L2 390n

C14 120p

L7 30 µ

C15 470p

C16 0.1µ

W4 ≈10n (NOTE 2)

W5 ≈10n (NOTE 2)

CR9

R11 100

C17 10p

C18 10p

CR5 CR6 CR7 CR8

R36 31.6k

R48 316k

R16 100

C22 22p

(F2)

INTEGRATOR

P/O NC U10

+15V (F7)

VREF +V

X1 X2 X3 X4

(CMOS)

R31 619

-15V (F3)

P/O U10

R29 1780

C24 0.068µ

R30 4220

BUFFER

U3

C33 0.1µ

C32 0.1µ

R22 348k

U9A

C30 0.01µ

C25 0.01µ

DC VOLTAGE COMPENSATION ADJ.

R33 100k

CW

R32 110k

R28 11k

LOOP ACQUISITION

U9B

R27 196k

R25 1k

R26 10k

R39 100k

C31 0.01µ

FL9

TUNE VOLTAGE SENSE

ACQUISITION SIGNAL SENSE

LOW PASS FILTERS

6.6 KHz LOW PASS

P/O U10

20 MHz L

R34 5110

R35 5110

L12 1.2 µ

L13 1.2 µ

C26 4700p

C27 4700p

C28 47p

SAWR LOOP DIAGNOSTICS

+5V (F2)

R2 100k

C6 0.01µ

R3 11k

R14 100k

R15 10k

C21 0.022

BEAT NOTE SENSE

OSCILLATOR SIGNAL DETECT

R38 51.1k

R37 51.1k

CR10

C19 22p

R12 75k

R42 100k

R43 68.1k

LOOP IF SENSE

+15V (F1)

+15V (F2)

+15V (F3)

+15V (F4)

+15V (F5)

+15V (F6)

L105 3µ

C138 470p

+15V (F10)

C132 470p

+5V (F1)

GND

POWER SUPPLY AND GROUND

BD 26

ATTENTION
Static Sensitive Devices

LOOP LIMITING AND ISOLATING AMPLIFIERS

+15V (F8)

R6 348

VR1 5.2V

R5 1470

C10 47p

Q4

C146 4.7p

R4 100

+15V (F9)

R150 681

VR107 5.2V

Q107

R149 1470

C134 4.7p

R148 100

+15V (F10)

R146 681

VR106 5.2V

Q106

R147 1470

C131 4.7p

R138 100

UHF REFERENCE LOOP IF

BE 26

RATOR

+15V (F7)
P/O U10 NC
VREF +V
X1
X2
X3
X4
(CMOS)
R31 619
-15V (F3)
P/O U10
R29 1780
C24 0.068µ
R30 4220
FER
F7)
C33 0.1µ
C32 0.1µ
R22 348k
U9A
C30 0.01µ
C25 0.01µ
-15V (F3)
+15V (F7)
DC VOLTAGE COMPENSATION ADJ.
R33 100k
CW
R32 110k
-15V (F2)
R28 11k
LOOP ACQUISITION
R27 196k
U9B
R25 1k
R26 10k
R39 100k
C31 0.01µ
FL9
TUNE VOLTAGE SENSE
ACQUISITION SIGNAL SENSE
BEAT NOTE SENSE
LOOP IF SENSE

LOW PASS FILTERS
6.6 KHz LOW PASS
P/O U10
20 MHz LOW PASS
R34 5110
R35 5110
L12 1.2µ
L13 1.2µ
L102 1.2µ
C26 4700p
C27 4700p
C28 47p
C29 47p
C103 47p
C108 47p
SAWR OSCILLATOR TUNE VOLTAGE
BF 26

SAWR LOOP DIAGNOSTICS
+5V (F2)
R2 100k
U8D
R19 2370
C6 0.01µ
R3 11k
R14 100k
R15 10k
U8C
C21 0.022
OSCILLATOR SIGNAL DETECT
R38 51.1k
R37 51.1k
CR10
C19 22p
R12 75k
U8A
C20 0.01µ
R42 100k
R43 68.1k
U8B
C7 470p
R24 5110
R23 147k
C23 0.33µ
U11
RX/CX
CX
NC
FL14
FL12
P/O J1
S2
S1
P/O A5 ASSY SS65
SAWR SENSE 1, 2
BG 10
SAWR LOOP DIAGNOSTIC BUS
BH 9

G AMPLIFIERS
+15V (F9)
R150 681
VR107 5.2V
Q107
R149 1470
C134 4.7p
R148 100
+15V (F10)
R146 681
VR106 5.2V
Q106
R147 1470
C131 4.7p
R138 100
UHF REFERENCE LOOP IF
BE 26

SS25
Figure 8L-103
8L-103

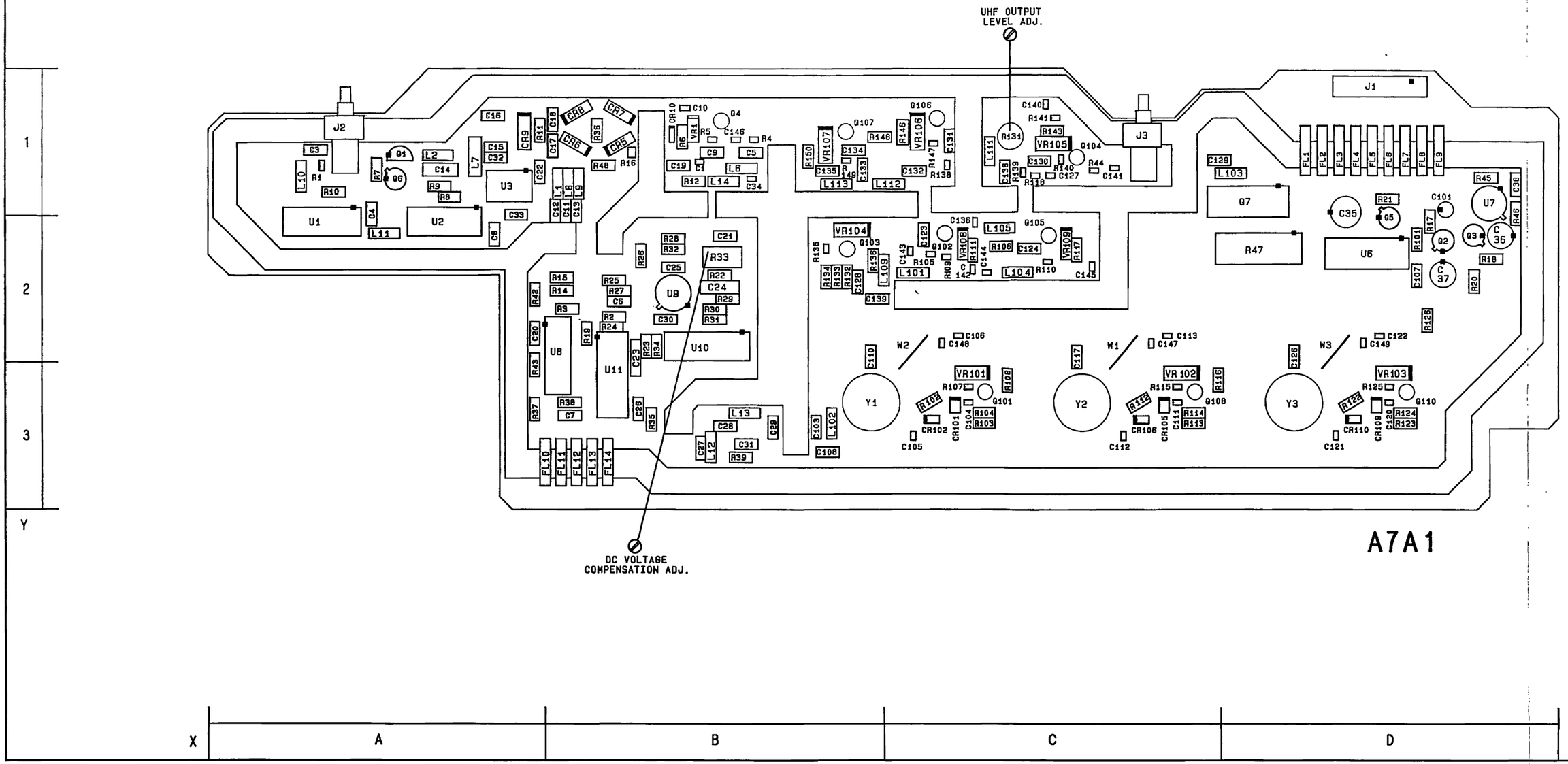
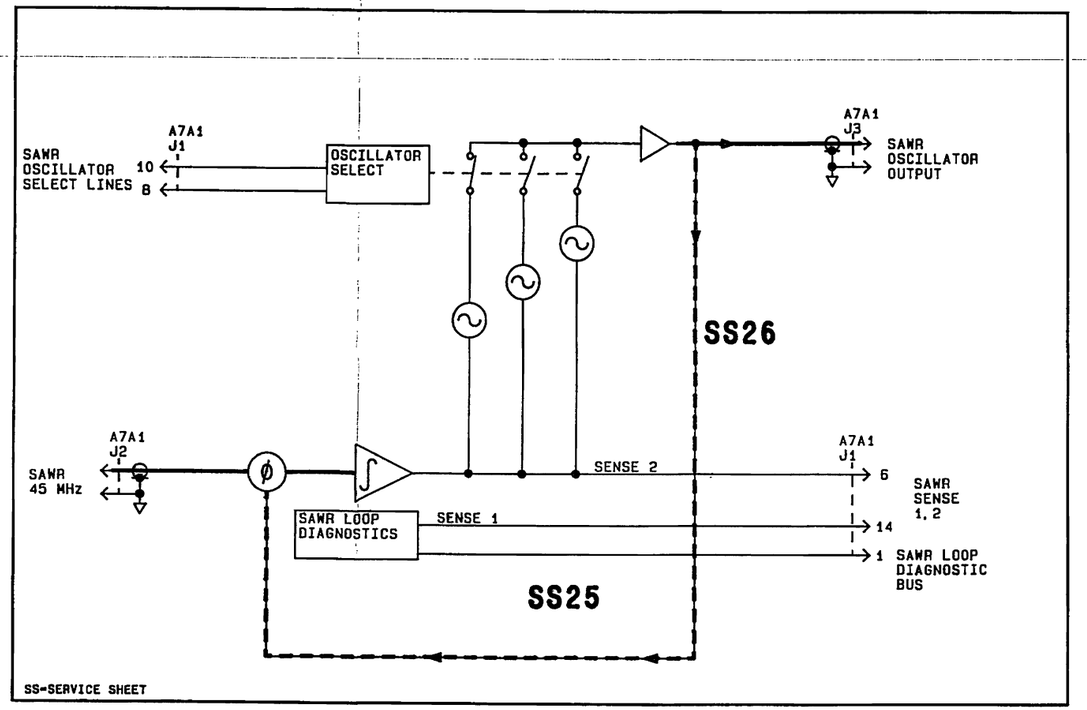


Figure 8L-104. SERVICE SHEET 26 INFORMATION

Component Locator



Reference Block Diagram

Component Coordinates

COMP	X,Y
C104	C, 3
C105	C, 3
C106	C, 2
C107	D, 2
C110	B, 2
C111	C, 3
C112	C, 3
C113	C, 2
C117	C, 2
C120	D, 3
C121	D, 3
C122	D, 2
C123	C, 2
C124	C, 2
C126	D, 2
C127	C, 1
C130	C, 1
C140	C, 1
C141	C, 1
C147	C, 2
C148	C, 2
C149	D, 2
CR101	C, 3
CR102	C, 3
CR105	C, 3
CR106	C, 3
CR109	D, 3
CR110	D, 3
FL4	D, 1
FL5	D, 1
J1	D, 1
J3	C, 1
L111	C, 1

COMP	X,Y
Q7	D, 1
Q101	C, 3
Q102	C, 2
Q103	B, 2
Q104	C, 1
Q105	C, 2
Q108	C, 3
Q110	D, 3
R44	C, 1
R47	D, 2
R101	D, 2
R102	C, 3
R103	C, 3
R104	C, 3
R105	C, 2
R106	C, 2
R107	C, 3
R108	C, 3
R109	C, 2
R110	C, 2
R111	C, 2
R112	C, 3
R113	C, 3
R114	C, 3
R115	C, 3
R116	C, 3
R117	C, 2
R118	C, 1
R122	D, 3
R123	D, 3
R124	D, 3
R125	D, 3
R126	D, 2
R131	C, 1
R132	B, 2
R133	B, 2

COMP	X,Y
R134	B, 2
R135	B, 2
R136	B, 2
R139	C, 1
R140	C, 1
R141	C, 1
R143	C, 1
W1	C, 2
W2	C, 2
W3	D, 2
U6	D, 2
VR101	C, 3
VR102	C, 3
VR103	D, 3
VR104	B, 2
VR105	C, 1
VR108	C, 2
VR109	C, 2
Y1	B, 3
Y2	C, 3
Y3	D, 3

COMP	X,Y

COMP	X,Y

COMP	X,Y

COMP	X,Y

COMP	X,Y

COMP	X,Y

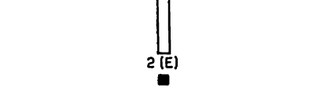
Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. W4-W13 are printed circuit trace inductors.
3. Logic Levels (TTL) at J1 pins 8, 10 select the oscillator shown in table.

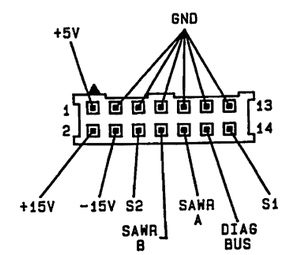
SAWR A	SAWR B	SAWR OSCILLATOR
0	0	832.5
0	1	742.5
1	0	787.5
1	1	NO OUTPUT

4. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

A7A1
Q101,102,103,104,
105,108,110
(TOP VIEW)



CABLE PLUG
TO A7A1 J1



P/O A7A1 SAWR LOOP ASSEMBLY (08642-60103)

P/O A5 DISTRIBUTION ASSEMBLY SS65

SAWR OSCILLATOR SELECT
11 BI

P/O J1
10 SAWR A
8 SAWR B

FL4
FL5

OSCILLATOR SELECT

+5V (F1)
R101 5110
+5V (F1)
C107 0.01
U6
BIN/7-SEG ▷ [T2]
≥1
&
G21
CT=0
V20
a 20, 21
b 20, 21
c 20, 21
d 20, 21
e 20, 21
f 20, 21
g 20, 21
NC

+15V (F2)
R47 3.3k

Q7
+15V (F2)

OSCILLATOR ENABLE (L)

POWER SUPPLY AND GND
+15V (F1)
+15V (F2)
+15V (F3)
+15V (F4)
+15V (F5)
+15V (F6)
+5V (F1)

POWER SUPPLY AND GROUND
25 BD

742.5 MHz SAWR OSCILLATOR
R132 90.9
R126 422
C126 10p
Y3
C122 47p
C149 5.6p
W3
W7 (NOTE 2)
W6 (NOTE 2)
VR103 5.2V
R125 1470
Q110
+15V (F1)
R122 10k
R124 2150
C120 47p
CR109
CR110
C121 47p
R123 5110

787.5 MHz SAWR OSCILLATOR
R134 90.9
R108 422
C110 10p
C106 47p
C148 3.9p
VR101 5.2V
R107 1470
Q101
R104 2150
C104 47p

SAWR OSCILLATOR TUNE VOLTAGE
25 BF

SERIAL PREFIX: 2427A

OUTPUT LIMITING AND
ISOLATION AMPLIFIERS

+15V (F4)
R11
422
+15V (F3)
R136
422
VR104
5.2V
VR108
5.2V
R135
150
Q103
1
3
2, 4
C123
2.2p
R105
50
R109
150
Q102
1
3
2, 4

UHF
REFEARENCE
LOOP IF
25 BE

OSCILLATOR ENABLE (L)

832.5 MHz
SAWR
OSCILLATOR

R116
422
R133
90.9
C117
10p
Y2
C113
47p
C147
3.3p
W1
W9
(NOTE 2)
W8
(NOTE 2)
VR102
5.2V
R115
1470
Q108
1
3
2, 4
+15V (F1)
R114
2150
R112
10k
C111
47p
CR105
CR106
C112
47p
R113
5110

OSCILLATOR ENABLE (L)

787.5 MHz
SAWR
OSCILLATOR

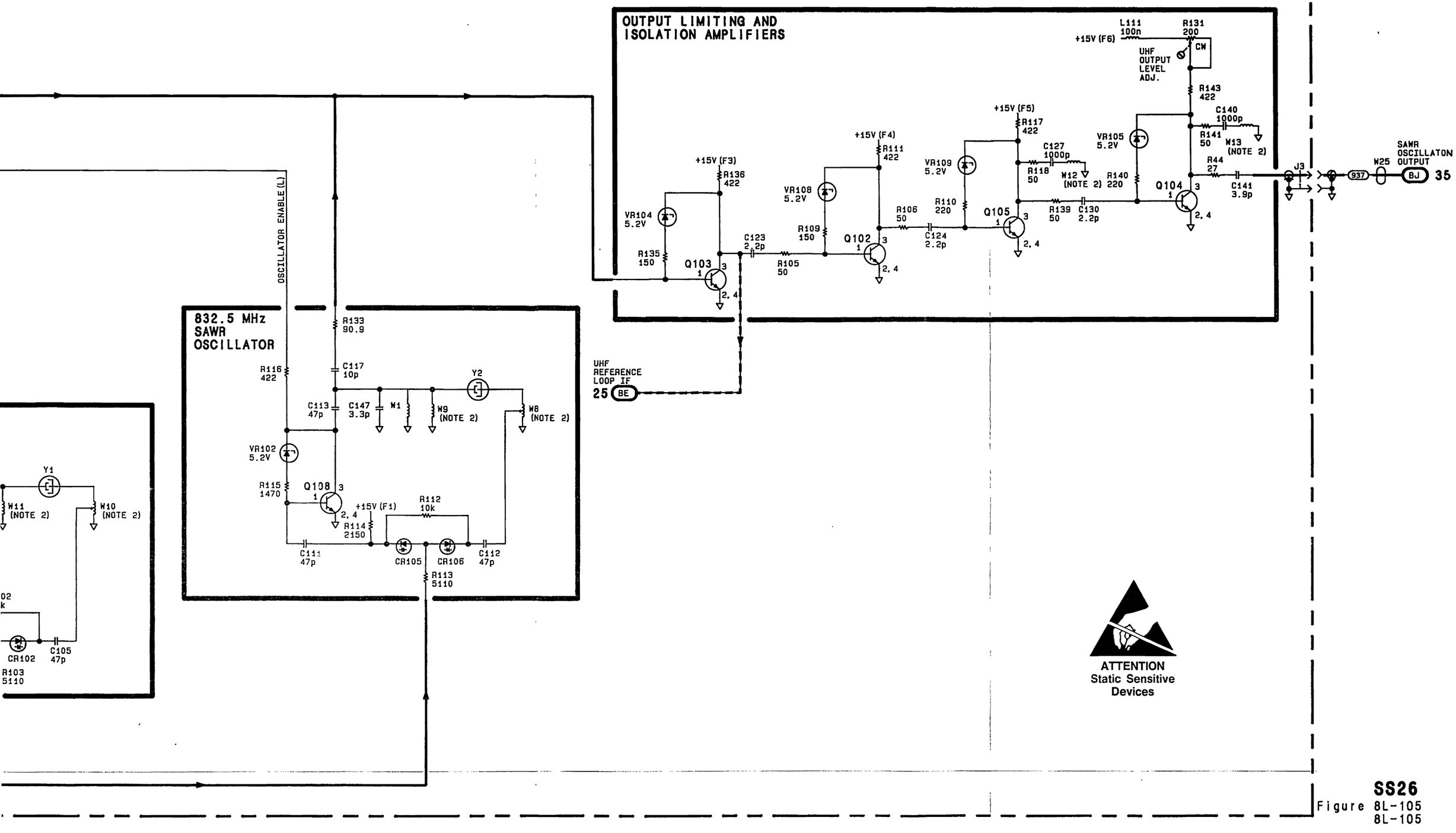
R134
90.9
R108
422
C110
10p
Y1
C106
47p
C148
3.9p
W2
W11
(NOTE 2)
W10
(NOTE 2)
VR101
5.2V
R107
1470
Q101
1
3
2, 4
+15V (F1)
R102
10k
R104
2150
C104
47p
CR101
CR102
C105
47p
R103
5110

OSCILLATOR ENABLE (L)

MHz
LATOR

R132
90.9
R126
422
C126
10p
Y3
C122
47p
C149
5.6p
W3
W7
(NOTE 2)
W6
(NOTE 2)
VR103
5.2V
R125
1470
Q110
1
3
2, 4
+15V (F1)
R122
10k
R124
2150
C120
47p
CR109
CR110
C121
47p
R123
5110

SAWR
OSCILLATOR
TUNE VOLTAGE
25 BF



ATTENTION
Static Sensitive
Devices

SS26

Figure 8L-105
8L-105

A9 Module

Troubleshooting and Adjustments Contents

Troubleshooting

Adjustments

Troubleshooting

A9 TROUBLESHOOTING INFORMATION

Before Proceeding with Module Troubleshooting

- You should have confidence that A9 is the faulty module from Module Level Diagnostics (MLD) results. (Refer to Instrument Level Troubleshooting, HP 8642 Service Manual.)
- Open the HP 8642 manual to Figure 8M-100. There are three diagrams of the A9 Module(A9A1 Voltage Controlled Oscillators and A9A2 Fractional-N). One diagram is titled Simplified Block Diagram. It is a block diagram intended to be used to understand the basic operation of the A9 Module. The Voltage Controlled Oscillators block, SS27, is for the A9A1 part of the Module and the other four blocks, SS28, 29, 30, and 31 are for the A9A2 part of the Module.
- Open the foldout on page 8M-101 (BD10.) There, you will see a more detailed Block Diagram of the A9 Module. This Troubleshooting Block Diagram is meant to be used during the A9 module checks.
- The objective of Troubleshooting checks is to isolate the malfunction to an area of circuitry represented on one service sheet. The checks are intended to be done in the order they are numbered.
- Once the malfunction is isolated to a service sheet, refer to the Component Level Repair Directory for the service sheet. There, you will find tables that contain information useful for locating faulty components.
- Specification failures (for example, phase noise, spurs, etc.) might not be found by Troubleshooting Checks. Manual Adjustments and Auto Adjust Procedures can be done, and the HP 8642 then retested to see if the specific failure condition still exists. At this point, if repair is necessary, Module Performance Checks may be helpful to pinpoint a failure condition in the module.

Overall Equipment List

Signal Generator No.1	HP 8642B
Oscilloscope	HP 1980B
Digital Voltmeter (DVM)	HP 3456A
Spectrum Analyzer	HP 8566A
Variable DC Supply	HP 6218B
SMC 50Ω Termination	1250-0839
Spectrum Analyzer	HP 3585A

Essentials of A9 Module Operation

NOTE

This procedure is written with the understanding that the 500 KHz IF Reference Signal has been verified good.

The A9 module consists of two assemblies, A9A1 and A9A2. Refer to the Simplified Block Diagram on page 8M-101 for the following discussion of the A9A1 and A9A2 assemblies.

The A9A1 assembly consists of the IF Voltage Controlled Oscillators (VCO). The VCOs are shown on SS27. There is an input, A9A1 J1, that connects the VCO Tune/Error voltage from the Fractional-N assembly to tune and lock the VCO selected to the correct frequency.

The Pretune and VCO select inputs to the VCO assembly are connected from the Fractional-N A9A2 assembly by the A9 interconnect between assemblies A9A1 and A9A2.

The A9A2 assembly consists of the Fractional-N. The Fractional-N circuits are shown on SS28, 29, 30 and 31. There is an RF input, A9A2 J3, 500 kHz IF Reference, from BD6 A6A2 Counter/Time Base assemblies, and an RF input A9A2 J2, FN Loop Feedback 45-90 MHz, from SS27 A9A1 VCO assembly. The digital inputs to the A9A2 assembly are the Fractional-N Control Lines and Oscillator Control Enable from BD4 A4 Latch Module.

CHECK 1: A9A2 FRACTIONAL N DIVIDER CIRCUITRY (SS28 & P/O SS29)

Essentials of SS28 and Divider Counter of SS29 Circuit Operation

Refer to BD10. Located on SS28 you will find the Pre-Scaler, Timing and Output Synchronization circuitry for the IF Loop. Located on SS29 you will find the Divide Counter. The Pre-Scaler requires the IF Loop VCO input at A9A2 J1 and the Divide Counter's Prescale select, cycle reset and LS Bit 1 inputs for correct operation.

Description of Check 1

This check tests the Pre-Scaler and Divide Counter. The shift registers are disabled, data to the Divide Counters can not be changed, and the Pulse remove input to the Pre-Scaler is disabled.

The VCO output of the Pre-Scaler Buffer is checked. The Pre-Scaler and Divide Counter are checked for dividing the VCO frequency to the correct divide frequency.

If a test fails, refer to the Component Level Repair Directory. (Found at the end of the procedures after Check 5)

Required Equipment:

Oscilloscope ..... HP 1980B
Digital Voltmeter (DVM) ..... HP 3456A

Test the A9A2 Power Supply and Ground

1. Setup:

   Switch the HP 8642 to standby (STBY).

   Extend module on extender posts (refer to the Disassembly Procedure if you are not familiar with this procedure).

   Remove the A9A2 cover (see the assembly locator on the foldout opposite BD 10 for location of A9A2 cover).

   Switch the HP 8642 on.

2. Measure Voltage Levels:

   Check the **POWER SUPPLY AND GND** line voltages at the inductors given in Table 8M-1. (Inductor locations can be found on page 8M-104, and measurements can be made on either side of inductor.)

Table 8M–1. *A9A2 Power Supply Lines*

Inductor	Nominal Voltage
L1	+50Vdc
L2,L11	+15Vdc
L3,L12	+5Vdc
L4,L13	−15Vdc

Test the IF Loop Dividers

3. Setup:

   Switch the HP 8642 to STANDBY.

   Using an external test lead connect TP7 and TP8 to ground. (this disables the Divide Count shift registers, and sets the IF LOOP to the top of Oscillator No. 5.)

   Switch the HP 8642 to ON.

4. Verify Divider Waveforms:

   Connect the Oscilloscope to each TP listed in the Table 8M-2 and verify that the signals are similar to the waveform in Figure 8M-1 through Figure 8M-10. Oscilloscope input is AC.

Table 8M-2. *Pre-Scaler and Divider Counter Waveforms*

TP No.	Description	Waveform
3	VCO FREQ	8M-1
6	VCO FREQ/2	8M-2
10	VCO FREQ/4	8M-3
5	VCO FREQ/20	8M-4
9	VCO FREQ/200	8M-5
12	VCO FREQ/2000	8M-6
13	VCO FREQ/2000	8M-7
4	VCO FREQ/20	8M-8
11	VCO FREQ/2000	8M-9
14	VCO FREQ/2000	8M-10

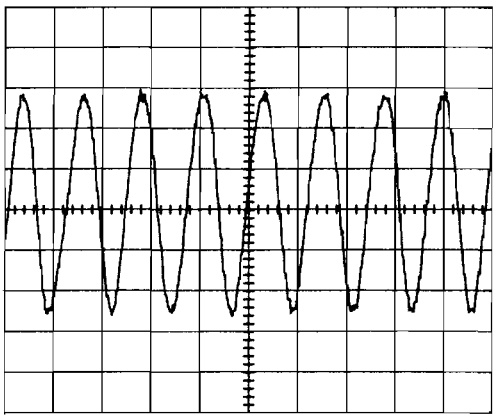


Figure 8M-1. *VCO Freq 180mV/DIV 9nS/DIV*

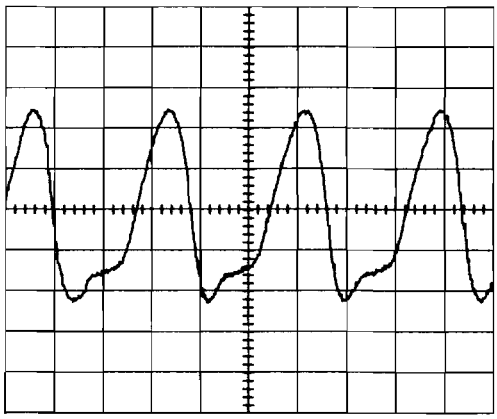


Figure 8M-2. *VCO Freq/2 1V/DIV 8nS/DIV*

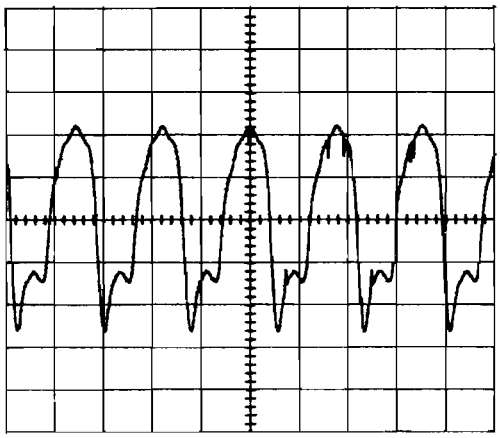


Figure 8M–3. *VCO Freq/4 1V/DIV 25nS/DIV*

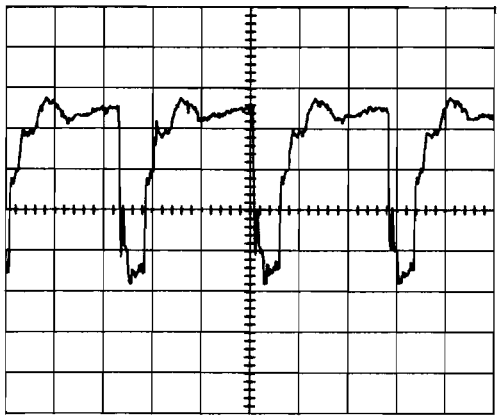


Figure 8M–4. *VCO Freq/20 1V/DIV 80nS/DIV*

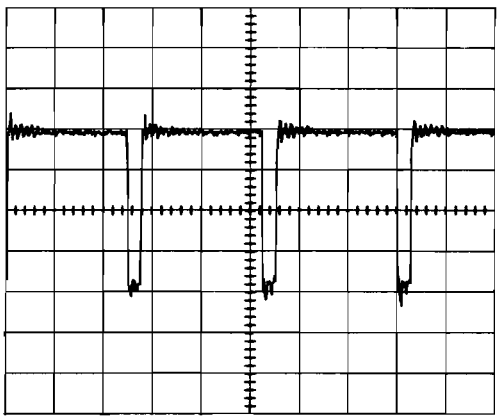


Figure 8M–5. *VCO Freq/200 1V/DIV 800nS/DIV*

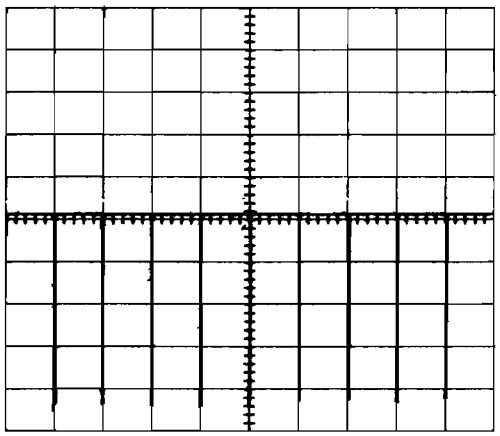


Figure 8M–6. *VCO Freq/2000 2V/DIV 22μS/DIV*

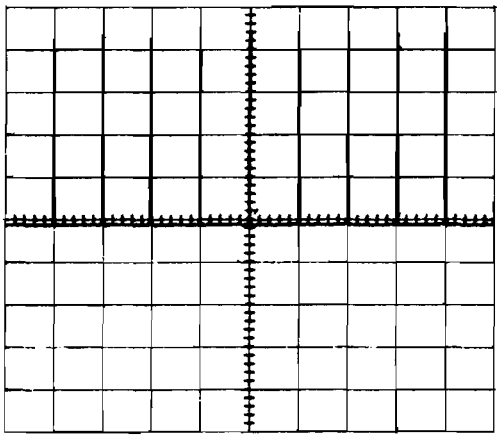


Figure 8M–7. *VCO Freq/2000 1V/DIV 22μS/DIV*

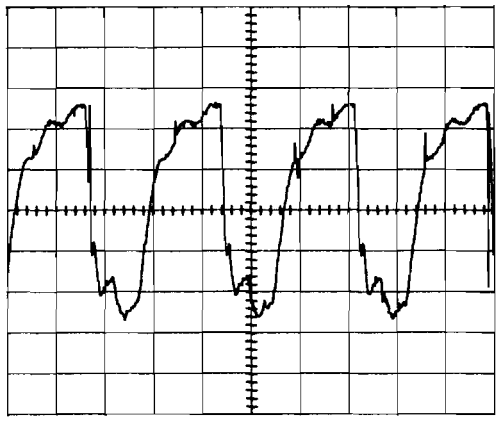


Figure 8M–8. *VCO Freq/20 1V/DIV 80nS/DIV*

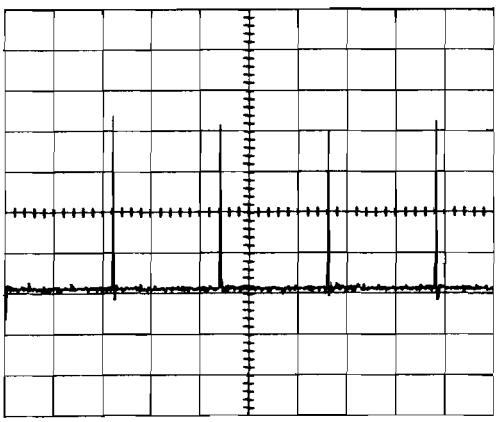


Figure 8M–9. *VCO Freq/2000 1V/DIV 10 μS/DIV*

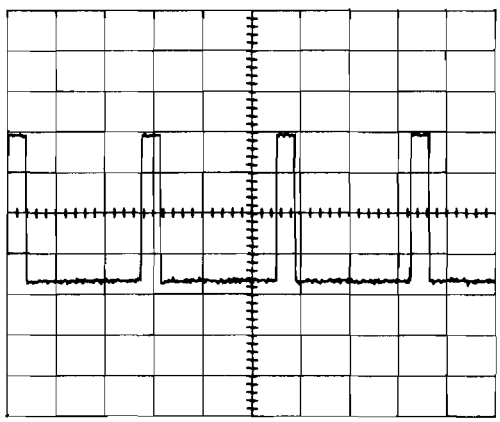


Figure 8M–10. *VCO Freq/2000 1/DIV 8μ/DIV*

Restore Module

5. Switch the HP 8642 to STANDBY.
6. Remove the test lead from TP7 and TP 8.
7. Switch the HP 8642 ON.

CHECK 2: A9A2 FRACTIONAL N INPUTS/OUTPUTS (SS29)

Essentials of SS29 Fractional-N and Oscillator Control Circuit Operation

Refer to BD10. Located on SS29 you will find the Fractional-N Chip, Oscillator Control and Divide Counter. The Divide Counter was checked in Check 1.

The Fractional-N chip requires data and a data clock from the A4 Latch Module. The cycle start (pulse to start each cycle of the IF Loop) and FN chip clock (Fractional N clock, IF Loop VCO divided-by-20) are required inputs from SS28.

The Oscillator control requires the enable bits from the A4 Latch Module and the Oscillator control clock from SS28. The Oscillator control circuits select the correct IF Loop VCO and the VCO's Pretune voltage.

Description of Check 2

This check tests the Fractional-N chip and the Oscillator Control circuits inputs and outputs.

If a test fails, refer to the Component Level Repair Directory. (Found at the end of these procedures after Check 5.)

Required Equipment:

Oscilloscope ..... HP 1980B
Digital Voltmeter (DVM) ..... HP 3456A

NOTE

Component locations for SS29 can be found on 8M-106

Verify the Fractional-N Inputs from the Processor

1. Setup:

   Preset the HP 8642

2. Verify TTL Levels:

   Key in [SHIFT] [SPCL] [3] to enter Service Mode. Key in the Function and Data for each data line listed in Table 8M-3. Verify the correct TTL levels at the U20 pin numbers listed.

   EXAMPLE:"[SHIFT] [SPCL] [3] [6] [0] [1] [3] [2] [HZ]"

   Enter [6] [0] [2] [3] [2] [Hz] to set the line low, Entering [6] [0] [1] sets a bit high and [6] [0] [2] sets a bit low.

Table 8M-3. *Fractional-N Inputs*

Function	Data	Line Label	U20 Pin No.
	32 Hz	FN C0	23
601 (sets line to 1)	33 Hz	FN C1	22
	34 Hz	FN C2	21
602 (sets line to 0)	35 Hz	FN C3	20
	36 Hz	INV	24
	37 Hz	EXT CLOCK	26

Verify the Fractional N Data Output signals

3. Setup:

   Preset the HP 8642

   Set the HP 8642 to sweep

   Start Frequency: 607.500001 MHz

   Stop Frequency: 652.5 MHz

   Sweep Time: 10 SECONDS

   Sweep Mode: AUTO

4. Verify Data and Clock Outputs:

   Connect the Oscilloscope to each of the U20 pins listed in Table 8M-4. Verify that each signal is a series of positive TTL pulses.

Table 8M-4. *Fractional N Data Outputs*

U20 Pin Number	Line Label
13	D8
14	D4
15	D2
16	D1
17	CLK

5. Verify the Bias Output Waveform:

   Connect the Oscilloscope to U20 Pin 10. The waveform should be a 100 KHz TTL signal with its duty cycle varying from 30 to 60%.

6. Verify the Sample Control Waveform:

   Connect the Oscilloscope to U20 Pin 11. The waveform should be a 100 KHz TTL signal with its duty cycle varying from 5 to 10%.

Verify the SLF/CO output Waveform

7. Setup:

   Preset the HP 8642.

   Select Phase Continuous Sweep "[SHIFT] [SPCL] [1] [2] [3]"

   SET Set the HP 8642 to sweep:

   Start Frequency: 652.0 MHz

   Stop Frequency: 652.2 MHz

   Sweep Time: 500 mS

   Sweep Mode: AUTO

8. Verify Waveform:

   Connect the Oscilloscope to U20 Pin 18. Waveform should be a series of positive TTL pulses.

Verify the Pulse Remove Waveform

9. Setup:

   Preset the HP 8642.

   Set the HP 8642 to an IF frequency of 45.1 MHz by keying in the following: SHIFT SPCL 3 6 1 0 4 5 1 0 0 0 0 0 0 HZ

10. Verify Waveform:

    Connect the Oscilloscope to U20 Pin 12. The signal should resemble waveform in Figure 8M-11.

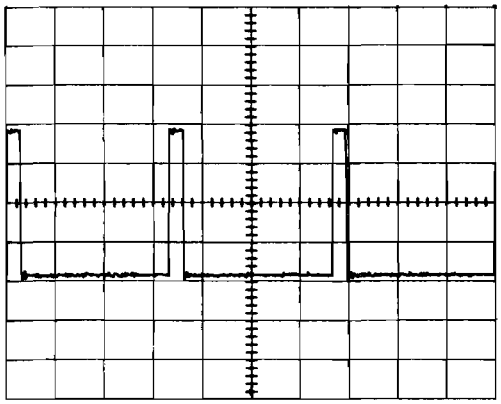


Figure 8M-11. *1V/DIV3μS/DIV*

Verify the API Outputs

11. Setup:

    Set the HP 8642 to an IF frequency of 44.999999 MHz by keying in the following: SHIFT SPCL 3 6 1 0 4 4 9 9 9 9 9 9 9 HZ

12. Verify Waveforms:

    Connect the Oscilloscope to each of the API outputs (U20 Pins 2 thru 6) while verifying the signal. The waveform should be a 100 kHz TTL square wave with the duty cycle varying from 55 to 95%. Figure 8M-12, a and b, shows the change in API 1. The API rate of change increases for each API waveform. API 5's rate of change is the highest.

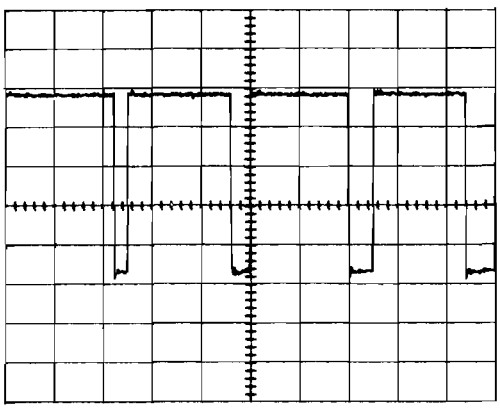


Figure 8M-12a. *1V/DIV 4μS/DIV*

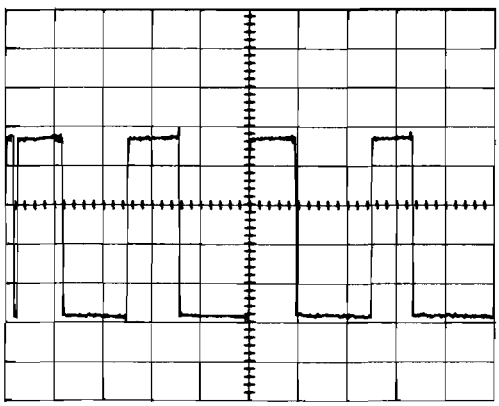


Figure 8M-12b. *1V/DIV 4μS/DIV*

NOTE

The API's are a BCD output occuring at a 100 KHz rate with API 1 being the most significant and API 5 being the least significant. The resultant waveform is a 100 KHz signal with its duty cycle varying from 55 to 95%. Because of the limitations of the Oscilloscope, it may be difficult to see the duty cycle varying on the least significant API's. Figure 8M-12 is a representation of the API 1 output. Observing API 1 gives you a better understanding of what the waveforms look like.

Test the Oscillator Control Circuitry

13. Setup:

    Preset the HP 8642

14. Verify the Oscillator Control Inputs:

    Key in [SHIFT] [SPCL] [3] to enter Service Mode.

    Key in the Service Function in Table 8M-5 while verifying the correct TTL level at the U9 input pin listed.

NOTE

The CONTROL ROM inputs are a 2.5 digit BCD number which changes every 200 KHz. When the IF LOOP is changed from 40 to 90 MHz in 200 KHz steps the inputs are addressed from 399 to 149.

Table 8M-5. *Control ROM Inputs*

Service Function	U9_Pin No's									
	22	23	1	2	3	4	5	6	7	8
610 622000000 MHz	1	0	1	0	0	0	1	0	0	0
610 754000000 MHz	1	0	0	0	1	0	0	0	1	0
610 888000000 MHz	0	1	0	1	0	1	0	1	0	1

15. Test the Oscillator Select Lines:

    Manually sweep the HP 8642 across each oscillators frequency band with frequency steps of 200 kHz,(see Table 8M- 6 for the front panel frequencies to sweep each oscillator) while verifying that each **OSCILLATOR SELECT LINE** in Table 8M-7 is at the correct level.

Table 8M-6. *Front Panel frequencies For Each IF VCO Frequency Range*

VCO No.	IF FREQUENCY	FRONT PANEL FREQUENCY
1	45.0 to 52.599999 MHz	652.5 TO 644.900001 MHz
2	52.6 to 59.999999 MHz	644.9 TO 637.500001 MHz
3	60.0 to 67.599999 MHz	637.5 TO 629.900001 MHz
4	67.6 to 74.999999 MHz	629.9 TO 622.500001 MHz
5	75.0 to 82.599999 MHz	622.5 TO 614.900001 MHz
6	82.6 to 89.999999 MHz	614.9 TO 607.500001 MHz

Table 8M–7. *Oscillator Select Lines*

VCO No.	IF VCO Frequency	U7 Pin No.			J5 Pin No. *					
		3	2	1	6	7	8	9	10	11
1	45.0 to 52.599999 MHz	0	0	0	H	L	L	L	L	L
2	52.6 to 59.999999 MHz	0	0	1	L	H	L	L	L	L
3	60.0 to 67.599999 MHz	0	1	0	L	L	H	L	L	L
4	67.6 to 74.999999 MHz	0	1	1	L	L	L	H	L	L
5	75.0 to 82.599999 MHz	1	0	0	L	L	L	L	H	L
6	82.6 to 89.999999 MHz	1	1	1	L	L	L	L	L	H

* A high (H) is ≈ +15 Vdc and a low (L) is ≈ −15 Vdc

16. Test The Pretune Level Control Circuitry:

    Key in [SHIFT] [SPCL] [3] to enter Service Mode.

    Key in the Service Function from the Table 8M-8 and verify that the Pretune Level Control lines are at the correct TTL voltage.

Table 8M–8. *Pretune Select Lines*

Service Function	J6 Pin No.'s				
	8 (P16)	7 (P8)	6 (P4)	5 (P2)	4 (P1)
610 498000000 MHz	0	1	0	1	0
610 472000000 MHz	1	0	1	0	1

CHECK 3: A9A2 BIAS AND API CIRCUITRY (SS31)

Essentials of SS31 BIAS and API Circuit Operation

Refer to BD10. Located on SS31 you will find the Bias and API Control Latch, Bias and API Current Sources, and Bias and API current summing.

The Bias Enable, API Enables, and Latch clock are required from the Fractional-N chip from SS29. The Bias Enable and API enables are pulses determined by the Fractional-N chip to sum together a precise amount of API current with the Bias current. Delayed Bias is gated on SS29 with Bias for Output Synchronization and with Latch Enable for the Latch Clk.

Description of Check 3

This check tests that the Bias and API Switch Drivers are being turned on by the output of the Bias and API Control Latch. The Bias and API current summing switch Q33 is also checked.

If a test fails, refer to the Component Level Repair Directory. (Found at the end of these procedures after Check 5.)

Required Equipment:

Oscilloscope ..... HP 1980B
Digital Voltmeter (DVM) ..... HP 3456A

NOTE

Component locations for SS31 can be found on page 8M-110.

Test the Bias and API Circuitry

1. Setup:

   Preset the HP 8642

   Set the IF LOOP frequency to 45 MHz by keying in the following: SHIFT SPCL 3 6 1 0 4 5 0 0 0 0 0 0 0 HZ

2. Verify the API's Waveform:

   Connect the Oscilloscope to the location listed in the Table 8M-9 for each of the API's, and verify that the signal is similar to the waveforms in Figure 8M-13 through 8M-17.

Table 8M-9. *API Outputs*

Signal	Location	Waveform	Signal's High Level	Pulse Level
API 1	Anode CR9	8M-13*	≈ 5.2 Vdc	≈ −500 mVdc
API 2	Anode CR 10	8M-14*	≈ 5.2 Vdc	≈ −270 mVdc
API 3	Anode CR 11	8M-15*	≈ 5.2 Vdc	≈ −270 mVdc
API 4	JCT. of R92,R94	8M-16*	≈ 50 MVdc	≈ −50 mVdc
API 5	JCT. of R89,90	8M-17*	≈ 5.2 VDC	≈ −50 mVdc

* The Duty Cycle of the API waveforms can be between 55 and 95%.

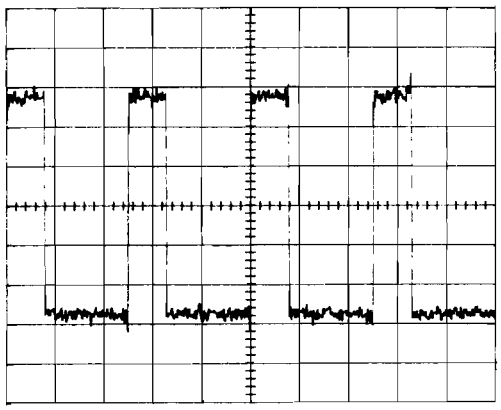


Figure 8M–13. *API 1 100mV/DIV 4μS/DIV*

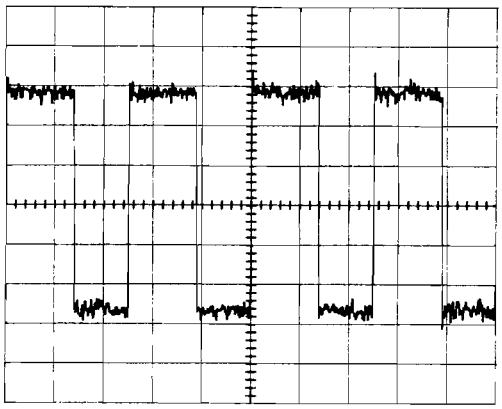


Figure 8M–14. *API 2 50mV/DIV 4μ/DIV*

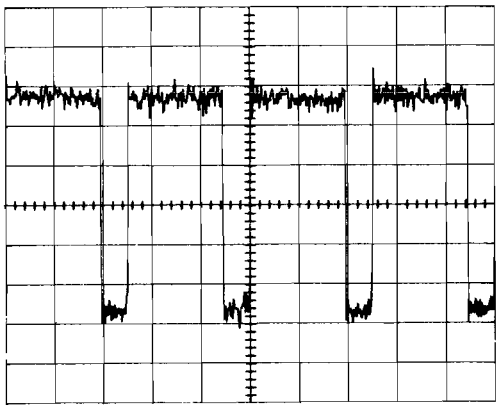


Figure 8M–15. *API 3 50mV/DIV 4μS/DIV*

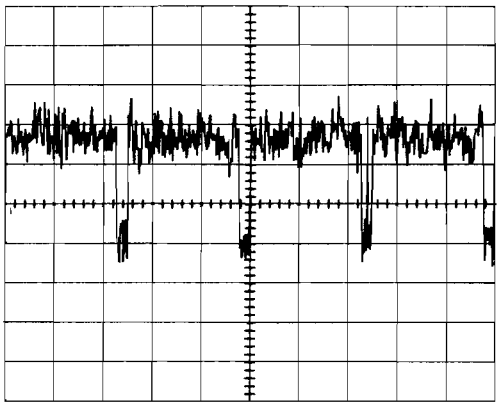


Figure 8M–16. *API 4 20mV/DIV 4μ/DIV*

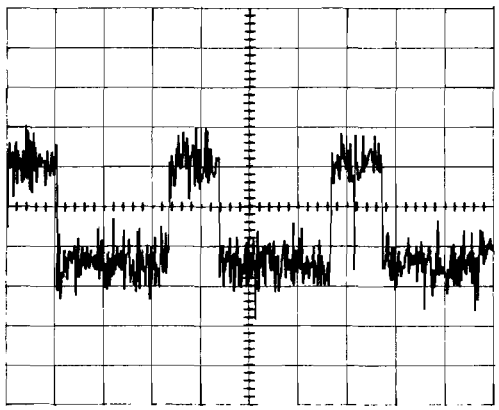


Figure 8M–17. *API 5 20mV/DIV 3μS/DIV*

3. Verify the Delayed Bias Signal (CO):

   Connect the Oscilloscope to U36 pin 7, verify that the waveform is a 100 kHz TTL signal with a duty cycle between 30 to 60%.

4. Verify the Bias and API Current:

   Measure the Source Voltage of Q33. It should be 5.1 to 5.2 Vdc.

CHECK 4: A9A2 IF LOOP PHASE LOCK LOOP CIRCUITRY (SS30)

Essentials of SS30 Phase Detector, Integrator, and Sample and Hold Circuit operation

Refer to BD10. Located on SS30 you will find the Phase Detector, Integrator, and Sample and Hold.

The Reference Signal A9A2 J3 (500 kHz from the FM Loop/Counter/Timebase Module A6) and IF Loop VCO signal divided-by-F.N from SS28 are required for Phase Detector operation. The Integrator Current Source output to SS31 is required to set the Integrator to correct for phase lock error. The summed Bias and API current input from SS31 is required to reset the Integrator after the correct voltage is stored on the Sample and Hold capacitor. The Sample and Hold output A9A2 J4 to the If Loop VCO SS27 is required to lock the VCO to the correct frequency. The Sample and Hold circuit is turned on to sample the Integrator voltage at the correct time by the Sample and Hold pulse input from the Fractional-N Chip on SS29.

Description of Check 4

This check tests that the output of the Phase Detector will ramp the Integrator's Voltage to the +15 Vdc and −15 Vdc rail voltage as the IF frequency is varied above and below the IF Loop VCO lock frequency. The Integrator's voltage is stored on sample and hold capacitor C77 and measured at TP17.

The HP 8642's IF Loop's Divide Counter and Pre-Scaler are set to lock at a frequency of 90 MHz. The VCO input to the Pre-Scaler is replaced by a second 8642. The 8642's frequency is changed to a frequency above and below the 90 MHz lock frequency, and the VCO Tune Voltage is checked at TP17. The Loop Out-Of-Lock Detector is checked at it's output FL1.

If a test fails, refer to the Component Level Repair Directory. (Found at the end of these procedures after Check 5.)

Required Equipment:

Oscilloscope	HP 1980B
Digital Voltmeter (DVM)	HP 3456A
Signal Generator No.1	HP 8642B

NOTE

Component locations for SS30 can be found on page 8M-108.

Test the Phase Detector and Switch Drivers

1. Setup:

   Switch the HP 8642 to STANDBY.

   Disconnect the FN LOOP FEEDBACK (BP) A9W2 (934), FROM A9A2 J2 . Set Signal Generator No. 1 frequency to 90 MHz.

   Set Signal Generator No. 1 amplitude to 0 dBm.

   Lock the timebases of Signal Generator No. 1 and the HP 8642 under test together.

   Connect Signal Generator No. 1 to A9A2 J2.

   Switch the HP 8642 on. Set the HP 8642's IF frequency to 90 MHz by keying in the following: SHIFT SPCL 3 6 1 0 9 0 0 0 0 0 0 0 0 HZ

   Connect the Oscilloscope to TP17.

2. Verify the VCO Tune Voltage Line:

   Set Signal Generator No. 1 to each frequency listed in Table 8M-10 while verifying the voltage at TP17.

Table 8M-10. *VCO Tune Line Voltage*

Sig. Gen. No. 1 Frequency	Voltage at TP17
90.1 MHz	≈ +15 Vdc
89.9 MHz	≈ −15 Vdc

NOTE

When the Fractional Loop IF Frequency (TP14) is greater than the 500 KHz IF Reference Frequency (TP15), you should see positive pulses at TP21 and the Integrator should ramp to the positive rail. When TP14 is lower in frequency than TP15, you should see positive pulses at the collector of Q20 and the Integrator should ramp to the negative rail.

3. Verify the IF Reference Diagnostic Bus Line:

   Ensure that the IF frequency is still at 90 MHz as set in step 1. Set Signal Generator No. 1 to each frequency listed in Table 8M-11 below while verifying the voltage at A9A2 FL1.

Table 8M-11. *Diagnostic Buss Outputs*

Condition	Sig. Gen. No. 1 Frequency	Voltage at A9A2 FL1
Out Of Lock	91.0 MHz	≈ 0Vdc
Locked	90.0 MHz	≈ 4 Vdc

Restore Module

4. Switch the HP 8642 to STANDBY
5. Disconnect Signal Generator No. 1 from A9A2 J2
6. Reconnect A9W2 FN LOOP FEEDBACK (BP),(934) to A9A2 J2.
7. Re-install the A9A2 cover (refer to the Disassembly Procedure if you are not familiar with this procedure).

CHECK 5: A9A1 IF VCO CIRCUITRY (SS27)

Essentials of SS27 Circuit Operation

Refer to BD10. Located on SS27 you will find the Pretune, Tune/Error Signal, Impedance Buffer, Loop Control, Voltage Control Oscillators, and Power Splitter.

The five pretune level control bits of data input to the Pretune DAC from the Oscillator control SS29 are required to tune the VCO close to the correct frequency. The VCO Tune Voltage input from the sample and hold SS30 is required to tune and keep the VCO tuned to the correct frequency. The six Oscillator Select Lines of data input to the VCO from the Oscillator Control SS29 are required to select the correct VCO for the IF Reference Loop. The two Power Splitter outputs are the IF Reference Output A9A1 J4 and the IF Loop VCO feedback to the Pre-Scaler A9A1 J3.

Description of Check 5

This check tests the output voltage of the five bit Pretune DAC and the VCO Tune Voltage at the input of the Impedance Buffer. Each of the six VCO's frequency range and the IF Loop VCO's outputs at the Power Splitter are checked.

If a test fails, refer to the Component Level Repair Directory. (Found at the end of this procedure Check 5.)

Required Equipment:

Digital Voltmeter (DVM) ..... HP 3456A
Spectrum Analyzer ..... HP 8566A
Variable DC Supply ..... HP 6218B
SMC 50Ω Termination 1250-0839

NOTE

Component locations for SS27 can be found on page 8M-102.

Test the A9A1 Power Supply and Ground

1. Setup:

   Switch the HP 8642 to standby (STBY).

   Extend the module on extender posts (refer to the Disassembly Procedure if you are not familiar with this procedure).

   Remove the A9A1 cover (see the assembly locator on the foldout opposite BD 10 for location of A9A1 cover).

   Switch the HP 8642 on.

2. Measure Voltage Levels:

   Check the POWER SUPPLY AND GND line voltages at the Locations given in Table 8M-12.

Table 8M-12. *A9A1 Power Supply Lines*

Location	Nominal Voltage
TP2	+46.5 to 47.5Vdc
TP5	+13.0 to 14.0Vdc
TP6	−13.0 to −14.0Vdc
J5 Pin 5	GND

Test the Pretune DAC

3. Setup:

   Switch the HP 8642 to standby (STBY).

   Remove A9W1 (947) from A9A1J1

   Terminate the TUNE/ERROR SIGNAL input A9A1J1 with a 50Ω Termination

4. Verify Pretune Voltage:

   Switch the HP 8642 on.

   Key in [SHIFT] [SPCL] [3] to enter Service Mode.

   Key in each function in Table 8M-13 while verifying the correct voltage level at Test Point 1.

Table 8M-13. *Pretune Voltage*

Service Function	Pretune Bit	Voltage at TP1
610 525000000 MHz	NONE	45.2 to 48Vdc
610 516000000 MHz	P1	44.0 to 46.7Vdc
610 514000000 MHz	P2	43.0 to 45.4Vdc
610 510000000 MHz	P4	40.6 to 43.1Vdc
610 502000000 MHz	P8	36.1 to 38.3Vdc
610 484000000 MHz	P16	27.4 to 29.0Vdc
610 450000000 MHz	ALL	18.4 to 19.6Vdc

TEST THE VCO TUNE VOLTAGE

5. Setup:

   Remove the 50Ω load from A9A1J1

   Set the DC Power Supply to +13 Vdc

   Connect the DC Power Supply to A9A1 J1

6. Verify Pretune Voltage:

   Key in [SHIFT] [SPCL] [3] to enter Service Mode.

   Key in each function in Table 8M-14 below while verifying the correct voltage level at Test Point 1.

Table 8M-14. *VCO Tune Voltage*

Service Function	Pretune Bit	Voltage at TP1
610 525000000 MHz	None	33.2 to 35.2Vdc
610 516000000 MHz	P1	32.3 to 34.3Vdc
610 514000000 MHz	P2	31.4 to 33.4Vdc
610 510000000 MHz	P4	29.7 to 31.5Vdc
610 502000000 MHz	P8	26.4 to 28.0Vdc
610 484000000 MHz	P16	20.5 to 21.7Vdc
610 450000000 MHz	ALL	13.1 to 14.1Vdc

Verify the VCO's and Power Splitter

7. Setup:

   Insure that the +13Vdc source is still connected to A9A1J1

   Remove W30 (956) IF REFERENCE LOOP OUTPUT from A9A1J4.

   Remove A9W2 (934) FM LOOP FEEDBACK from A9A1J3

8. Verify Output Level:

   Select the front panel frequency from Table 8M-15 and Manually sweep each VCO across it's frequency range (maximum step size is 200 KHz) while verifying that the power level at A9A1J4 is 0 to 7 dBm and that the power level at A9A1 J3 is −4.5 to +2.5 dBm using the Spectrum Analyzer.

Table 8M-15. *IF VCO Frequency Ranges*

VCO No.	IF Frequency	Front Panel Frequency
1	45.0 to 52.599999 MHz	652.5 TO 644.900001 MHz
2	52.6 to 59.999999 MHz	644.9 TO 637.500001 MHz
3	60.0 to 67.599999 MHz	637.5 TO 629.900001 MHz
4	67.6 to 74.999999 MHz	629.9 TO 622.500001 MHz
5	75.0 to 82.599999 MHz	622.5 TO 614.900001 MHz
6	82.6 to 89.999999 MHz	614.9 TO 607.500001 MHz

NOTE

With the loop unlocked and the +13 Vdc source as the tune voltage, the IF frequency will not be accurate.

Restore Module

9. Switch the HP 8642 to standby (STBY).
10. Remove the DC Power Supply from A9A1J1
11. Reconnect A9W1 (947) to A9A1J1
12. Reconnect W30 (956) IF REFERENCE LOOP OUTPUT to A9A1J4.
13. Reconnect A9W2 (934) FM LOOP FEEDBACK to A9A1J3
14. Re-install the A9A1 cover (refer to the Disassembly Procedure if you are not familiar with this procedure).

COMPONENT LEVEL REPAIR DIRECTORY

The following tables contain information to aid in component level repairs. These tables are designed to be used after the module troubleshooting procedures have verified a failure in circuitry represented on one of the module service sheet schematics. In general the tables supply one of the following types of information:

* Special function codes relevant to the module.

* Transistor emitter, base and collector voltages.

* Frequency and power levels at different circuit points.

* Module control line and power supply interconnections in the module and instrument.

NOTE

Start with the tables that are labeled with a Service Sheet number (Example: **Table 8M-16. SS27 DC Voltages***). Other tables are more general and are to be used at your discretion. It is suggested all tables be reviewed so their usefulness for component level repair can be determined.*

SERVICE SHEET 27

Table 8M–16. SS27 DC Voltages

Device	Collector	Base	Emitter
Q6		5.5 to 6.5Vdc	
Q9		10 to 11 Vdc	9.3 to 10.3Vdc
Q14	48 to 49 Vdc	32 to 34 Vdc	31.3 to 33.3 Vdc
Q15	49 to 50 Vdc	32 to 34 Vdc	31.3 to 33.3 Vdc
Q16-18 31-33	−14 to −13Vdc	−13 to −12Vdc	
	Source	**Drain**	**Gate**
Q19-30	2 to 5 Vdc	−14 to −13 Vdc	GND
Q22	2 to 5Vdc	−14 to −13 Vdc	GND
CR10,15,20,25 30,35 (Anode)	ON .6 to 1 Vdc OFF −15 to −14 Vdc		
Device	**Collector**	**Base**	**Emitter**
Q34	1 to 2 Vdc	0 Vdc	−1 to −.6Vdc
Q35	4.3 to 5.3 Vdc	0 Vdc	−1 to −.6Vdc
Q36,Q37	7 to 9 Vdc	0 Vdc	−1 to −.6Vdc

Table 8M–17. SS27 RF Power Levels

Location	Description	Power Level
TP 4	Power Splitter input	approx. 0 DBm
A9A1 J3	FN LOOP FEEDBACK	− 4.5 to + 2.5 DBm
A9A1 J4	IF REFERENCE LOOP OUTPUT	0 to 7 DBm

Table 8M–18. SS27 IF VCO Frequency Ranges

VCO No.	IF VCO Frequency
1	40.0 to 52.599999 MHz
2	52.6 to 59.999999 MHz
3	60.0 to 67.599999 MHz
4	67.6 to 74.999999 MHz
5	75.0 to 82.599999 MHz
6	82.6 to 95.0 MHz

Table 8M–19. *SS27 IF Reference Loop Output Specifications*

Measurement	Specification A9A1 J4
Power Level	0 to 7 dBm
Harmonics	f3 < −10 dBc All others < −20dBc
Spurs	< −100 dBc
Residual FM	< −65 dBc

SERVICE SHEET 28

Table 8M–20. *SS28 DC Voltages*

Device	Collector	Base	Emitter
Q1	4.5 to 5.2 Vdc	0 Vdc	−1 to −.5 Vdc
Q2	3.3 to 4.3 Vdc	GND	−1 to −.5 Vdc
Q3	4.5 to 5.2 Vdc	0 Vdc	−1 to −.5 Vdc
Q4	2.2 to 3.2 Vdc	GND	−1 to −.5 Vdc

SERVICE SHEET 29

Table 8M–21. *SS29 Control Line Interconnections*

Line Label	A4 Latch			A5 Distribution		A9A2 IF Module
	IC	Pin	Latch Out	Input	Output	
FN C0	U15	15	P2 Pin 20	J16 Pin 20	J3 Pin 18	J1 Pin 18
FN C1	U15	9	P2 Pin 21	J16 Pin 21	J3 Pin 19	J1 Pin 19
FN C2	U15	6	P2 Pin 17	J16 Pin 17	J3 Pin 21	J1 Pin 21
FN C3	U15	16	P2 Pin 16	J16 Pin 16	J3 Pin 22	J1 Pin 22
H INV	U15	5	P2 Pin 15	J16 Pin 15	J3 Pin 16	J1 Pin 16
H EXT CLK	U15	2	P2 Pin 14	J16 Pin 14	J3 Pin 14	J1 Pin 14
OSC CONTROL	U15	12	P2 Pin 38	J16 Pin 38	J3 Pin 25	J1 Pin 25
OUT OF LOCK	U35	3	P3 Pin 7	J16 Pin 7	J3 Pin 26	J1 Pin 26
LOW SWEEP	U33	4	P3 PIN 37	J16 Pin 37	J3 Pin 24	J1 Pin 24
DISABLE	U13	5	A4U30 Pin 2			

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Table 8M–22. SS30 DC Voltages

Device	Collector	Base	Emitter
Q21	GND	3.5 to 4.5 Vdc	3.5 to 4.5 Vdc
Q22	1.5 to 2.5 Vdc	3.5 to 4.5 Vdc	3.5 to 4.5 Vdc
Q15	−15 to −14 Vdc	.3 to 1.0 Vdc	.5 to 1.5 Vdc
Q24	4.5 to 5.2 Vdc	1.5 to 2.0 Vdc	.5 to 1.5 Vdc
Q19	GND	3.0 to 4.5 Vdc	3.5 to 4.5 Vdc
Q22	−1 to −.3 Vdc	3.0 to 4.5 Vdc	3.5 to 4.5 Vdc
Sample and Hold			
Cathode VR4	−12.9 to −11.9 Vdc		
Q25	−12.7 to −11.7 Vdc	0Vdc	.1 to .5Vdc
Q27	−11.7 to −10.7 Vdc	−.2 to −.08 Vdc	.1 to .5 Vdc
Q16	1.5 to 2.5 Vdc	−12.7 to −11.7 Vdc	−12.3 to −11.3 Vdc
Q17	−5.0 to −4.0 Vdc	−11.8 to −10.8 Vdc	−12.2 to −11.2 Vdc

Table 8M–23. SS30 IF Loop Out-of-Lock

Line Label	A4 Latch			A5 Distribution		A9A2
	IC	Pin	Latch Out	Input	Output	IF Module
FN Out of Lock	U35	3	P3 Pin 7	J16 Pin 7	J3 Pin 26	J1 Pin 26
Out of Lock Disable	U13	5	A4U30 Pin 2			

SERVICE SHEET 31

Table 8M–24. SS31 DC Voltages

Device	Collector (Source)	Base (Gate)	Emitter (Drain)
API Voltages			
Q31,Q29,Q32	+15 VDc	5 to 6.5 Vdc	4.5 to 6.0 Vdc
Q34	−2 to −1Vdc	−5 to −2 Vdc	5.0 to 6.0 Vdc
Bias Current Source and Summing			
Q36	8.0 to 9.0 Vdc	9.0 to 10.5 Vdc	4.5 to 6.0 Vdc
Q33	4.5 to 6.0 Vdc	6.0 to 7.5 Vdc	1.0 to 0 Vdc
Current Source			
Q35	−6.0 to −4.5Vdc	−7.0 to −6.0 Vdc	−2.0 to −1.0 Vdc
U35 Pins 2,4,6,9	−9.0 to −7.0 Vdc		
U35 Pins 3,7,10	−10.0 to −8.0 Vdc		
U35 Pins 1,5,8,11	−6.0 to −4.5 Vdc		
U35 Pins 12,14	−14.5 to −13.5 Vdc		
U35 Pin 13	−15 to −14Vdc		

Table 8M–25. *A9 Power Supply Voltages*

Supply	A17 Output	A5 Input	A5 Output	A9A Input
+ 50 Vdc	J2 Pins 3&4	J12 Pins 3&4	J3 Pin 1	J1 Pin 1
+15 Vdc	J2 Pins 9-18	J12 Pins 9-18	J3 Pin 2-4	J1 Pins 2-4
+5 Vdc	J2 Pins 35-50	J12 Pins 35-50	J3 Pin 5-7	J1 Pin 5-7
−15 Vdc	J2 Pins 19-22	J12 Pins 19-22	J3 Pin 11	J1 Pin 11
GND	_____	Chassis GND	J3 Pins 12,13 15,17,20,23	J1 Pins 12,13 15,17,20,23

Table 8M–26. *A9 IF Loop Special Functions*

Enter Service Mode	Function	Description
6 0 9 HZ SHIFT SPCL 3 6 2 0 3 Hz	* Displays the current 6 1 0 Hz Displays the current	IF Loop Frequency ** Sets the IF Loop Frequency IF Loop Frequency

* The IF Frequency must be entered in tenth Hz units.

** The IF Frequency must be entered in tenth Hz units ie 45 MHz would be entered as 6 1 0 4 5 0 0 0 0 0 0 0 Hz

Table 8M–27. *A9 Special Functions to Set Control Lines*

Enter	Function	Description	Line	Description
			3 2 Hz	FN C0
			3 3 Hz	FN C1
			3 4 Hz	FN C2
			3 5 Hz	FM C3
SHIFT	6 0 0	Reads line state	3 6 Hz	H INV
SPCL	6 0 1	Sets Bit to 1	3 7 Hz	H EXT CLK
3	6 0 2	Sets Bit to 0	3 8 Hz	OSC CONTROL
	6 1 5 **	Continuous Toggle	* 1 0 4 Hz	Out of Lock
			* 1 1 7 Hz	LOW SWEEP
			1 6 Hz	Out of Lock

* This line can not be set, read is the only function for this line.

** To stop bit from toggling you must shut the HP 8642 off.

Adjustments

DESCRIPTION OF A9 ADJUSTMENTS

Overall Equipment List

Spectrum Analyzer HP3585A
DVM HP3456A

There is no Auto-Adjust Procedure for the A9 Module. There are two manual adjustment procedures: one for the VCOs' tune range and one for the current source DAC bits in the Fractional N circuitry. To adjust the VCOs' tune range the module is set to the lowest operating frequency (40 MHz) and the pretune is adjusted for the correct tune voltage. This sets the tune range lower limit. Then each VCO is set to its maximum frequency and adjusted for the correct tune voltage. This sets the tune range upper limit on each VCO. To adjust the Fractional-N circuitry, the module is set to a frequency that activates only one of the current source DAC bits. That bit is then adjusted to null the 10 kHz spur on the tune line. This is done for the most significant bit first and least significant bit last.

ADJUSTMENT 1: A9A2 FRACTIONAL-N SPUR ADJUSTMENT, SS31

1. Setup:

   Connect the Spectrum Analyzer time base input to the HP 8642 10 MHz Output.

   Connect the Spectrum Analyzer 1 MHz Input to A9A2 TP17.

   Set the Spectrum Analyzer as follows:

   Cent Freq ..... 10 kHz
   Span ..... 0 Hz
   Res BW ..... 3 Hz
   Vid BW ..... 1 Hz
   Impedance ..... 1 MΩ

2. Adjustment:

   For each Potentiometer, enter the HP 8642 Key Sequence given in the table below and adjust the 10 kHz signal for a null. The null should be below −80 dBm.

Adjustment	HP8642 Key Sequence
R73	SHIFT SPCL 3 610 90 020 000 0 Hz
R75	SHIFT SPCL 3 610 90 002 000 0 Hz
R76	SHIFT SPCL 3 610 90 000 200 0 Hz
R95	SHIFT SPCL 3 610 90 000 020 0 Hz
*	SHIFT SPCL 3 610 90 000 002 0 Hz
* Verify that the 10 kHz signal at this point is comparable to the null of R95.	

ADJUSTMENT 2: A9A1 IF VCO ADJUSTMENT SS27

1. Setup:

   Set the DVM to DC Volts mode.

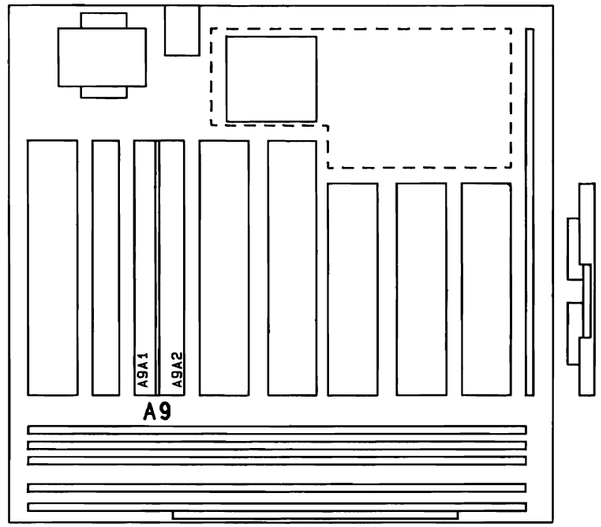
   Connect the DVM to A9A1 TP3.

2. Adjustment:

   Enter the HP8642 Key Sequence for each Adjustment given in the table below and adjust for a DVM reading between the Min and Max voltage.

Adjustment	HP8642 Key Sequence	Min	Actual	Max
R27	SHIFT SPCL 3 610 40 000 000 0 Hz	12.95	_____	13.05
C28	SHIFT SPCL 3 610 52 599 999 0 Hz	43.90	_____	44.10
C38	SHIFT SPCL 3 610 59 999 999 0 Hz	43.90	_____	44.10
C48	SHIFT SPCL 3 610 67 599 999 0 Hz	43.90	_____	44.10
C58	SHIFT SPCL 3 610 74 999 999 0 Hz	43.90	_____	44.10
C68	SHIFT SPCL 3 610 82 599 999 0 Hz	43.90	_____	44.10
C78	SHIFT SPCL 3 610 89 999 999 0 Hz	43.90	_____	44.10

Assembly Locator



Simplified Block Diagram

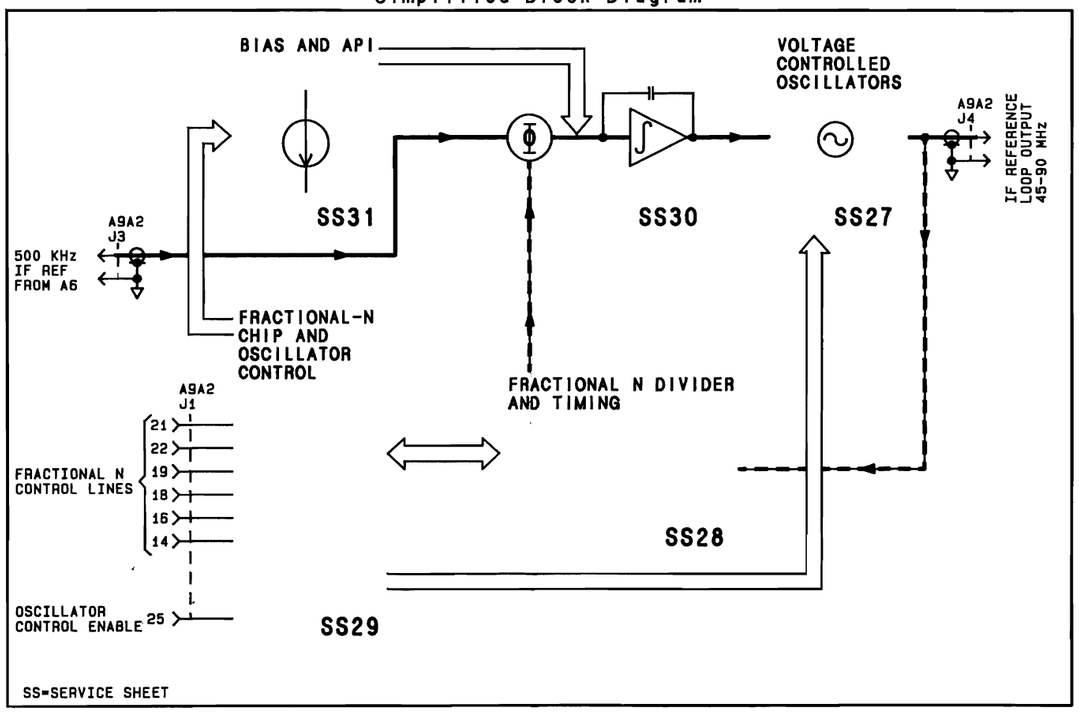
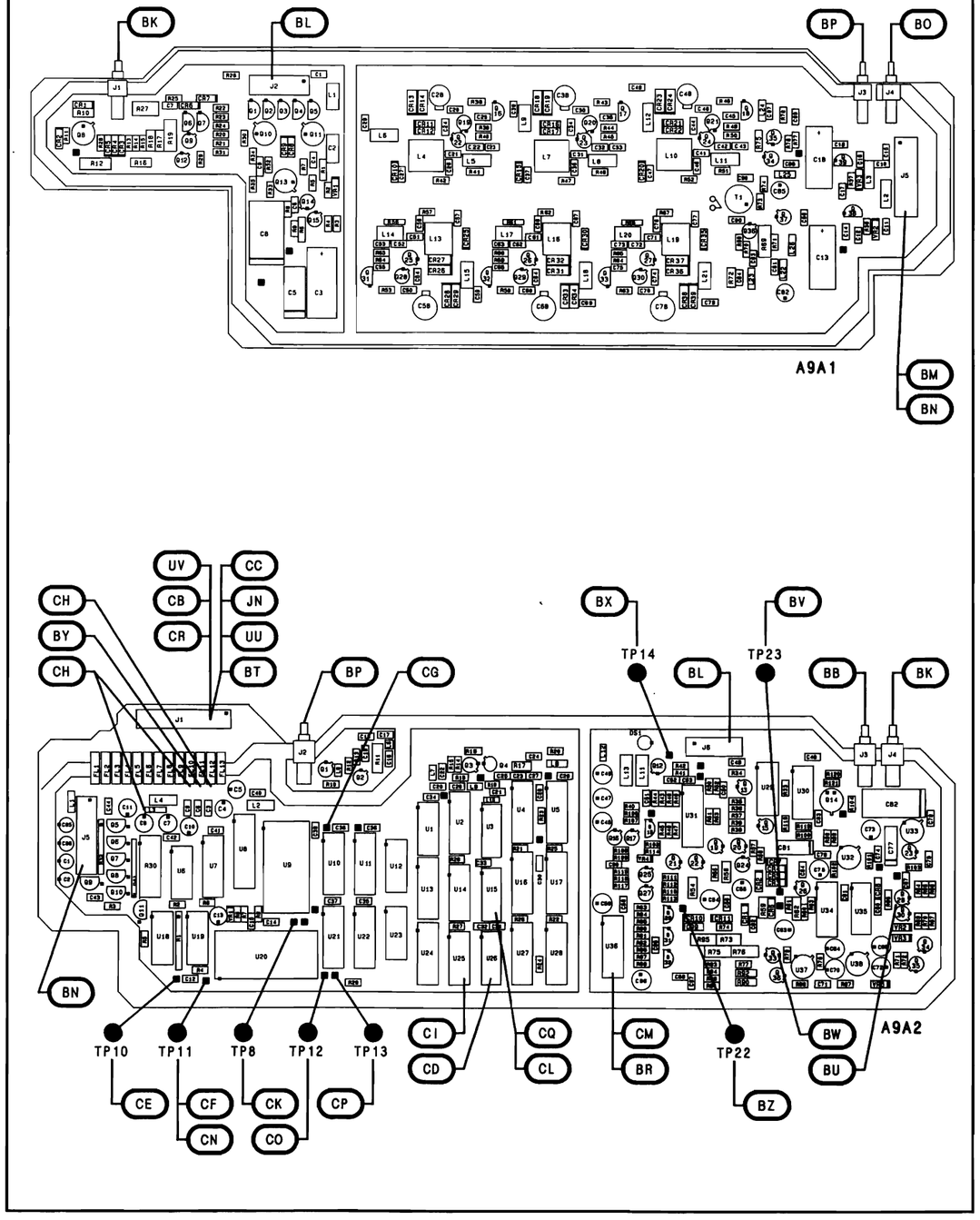


Figure 8M-100 BD10 General Information.

Module Test Point/Adjustment Locations



BIAS AND API CONTROL LATCH

A1-A5

API 1 TO 5

DELAYED BIAS

BIAS SWITCH DRIVE

BIAS SWITCHING DRIVE

API 1-3 CURRENT SOURCE

CURRENT SOURCE

BIAS AND API ENABLE

LATCH CLK

BIAS AND API CURRENT SUMMING

BIAS AND API CURRENT

INTEGRATOR CURRENT SOURCE

BIAS CURRENT SOURCE

BW

BV

BU

FN LOOP DIVIDE F.N

PHASE DETECTOR

SWITCH DRIVERS

REFERENCE SIGNAL

POWER SUPPLY AND GND

30 BT /4

28 BY /4

POWER SUPPLY AND GND

/4 BT 31

SS31

500kHz IF REFERENCE

A9W26

BD6 BB

905

J3

CM

BR

CO

BX

FRANCIONAL N CONTROL LINES

BD4 CB /6

P/O J1

21 FNC2

22 FNC3

19 FNC1

18 FNC0

16 H INV

14 H EXT CLK

FRACTIONAL N CHIP

PULSE REMOVE

SAMPLE AND HOLD

DIVIDE COUNTER

PRESCALE SELECT

CYCLE RESET

LS BIT 1

CK

CO

CP

CQ

CN

CG

CF

CE

CI

CL

OUTPUT SYNCHRONIZATION

LATCH ENALBLE

OUTPUT SYNCHRONIZATION

ECL TO TTL TRANSLATOR

PULSE REMOVE

OSCILLATOR CONTROL ENABLE

BD4 CC

25

OSCILLATOR CONTROL

P/O 08642-60003

P/O J5

P/O J6

F 11

E 10

D 9

C 8

B 7

A 6

P1 4

P2 5

P4 6

P8 7

P16 8

OSCILLATOR CONTROL CLOCK

FN CHIP CLOCK

CYCLE START

PRESCALE SELECT

CYCLE RESET

LS BIT 1

LATCH ENABLE

VCO ÷4 OR 6

TIMING

DIVIDE BY 2 OR 3 PRESCALER

/6

/5

BL

BN

POWER SUPPLY AND GROUND

BD17 CR /5

1 +50V

2-4 +15V

5-7 +5V

11 -15V

12, 13, 15, 17, 20, 23 GND

28 CH /4

POWER SUPPLY AND GND

SS29

SERIAL PREFIX: 2427A

A9A1 IF VCO ASSEMBLY (08642-60104)

FN LOOP DIVIDE F.N
PHASE DETECTOR
SWITCH DRIVERS
INTEGRATOR
SAMPLE AND HOLD
REFERENCE SIGNAL
POWER SUPPLY AND GND
LOOP OUT-OF-LOCK DETECTOR
SS30
J4
A9W1
J1
TUNE/ERROR SIGNAL
IMPEDENCE BUFFER
LOOP CONTROL
PRETUNE
J2
P1
P2
P4
P8
P16
POWER SUPPLY AND GND
J5
GND
+50V (F2)
+15V (F2)
-15V (F3)
GND
A, B, C
D, E, F
P/O J1
IF REFERENCE DIAGNOSTIC BUS
BD4
FN LOW SWEEP LIMIT
BK
BW
BV
BU
BY
BT
BZ
BX
CQ
CE
CI
CL
BM
BP
A9W2
OUTPUT SYNCHRONIZATION
OUTPUT SYNCHRONIZATION
ECL TO TTL TRANSLATOR
PULSE REMOVE
VCO ÷2
PRE-SCALER
P/O 08642-60003
PRESCALE SELECT
CYCLE RESET
LS BIT 1
LATCH ENABLE
VCO ÷4 OR 6
DIVIDE BY 2 OR 3 PRESCALER
TIMING
OSCILLATOR CONTROL CLOCK
FN CHIP CLOCK
CYCLE START
POWER SUPPLY AND GND
CH
BY
+50V (F1)
+15V (F1)
-15V (F1)
GND
GND
SS28
BL
BN

A9A1 IF VCO ASSEMBLY (08642-60104)

INTEGRATOR

SAMPLE AND HOLD

LOOP OUT-OF-LOCK DETECTOR

SS30

PULSE REMOVE

TTL TOR

PRE-SCALER

VCO ÷2

POWER SUPPLY AND GND

SS28

P/O 08642-60003

J4

BK

947

A9W1

J1

TUNE/ERROR SIGNAL

PRETUNE

IMPEDENCE BUFFER

LOOP CONTROL

VOTAGE CONTROLLED OSCILLATORS

POWER SPLITTER

J2

P1

P2

P4

P8

P16

J5

GND

+50V (F2)

+15V (F2)

-15V (F3)

GND

POWER SUPPLY AND GND

A

B

C

D

E

F

A, B, C

D, E, F

6

SS27

P/O J1

26

IF REFERENCE DIAGNOSTIC BUS

JN

BD4

BZ

FN LOW SWEEP LIMIT

24

UU

BM

BP

J2

A9W2

934

P/O J5

+50V (F1)

+15V (F1)

-15V (F1)

GND

P/O J6

GND

CH

29

BY

30

5

6

J4

955

A9W30

IF REFERENCE LOOP OUTPUT

BO

BD10

J3

BD10

Figure 8M-101

8M-101

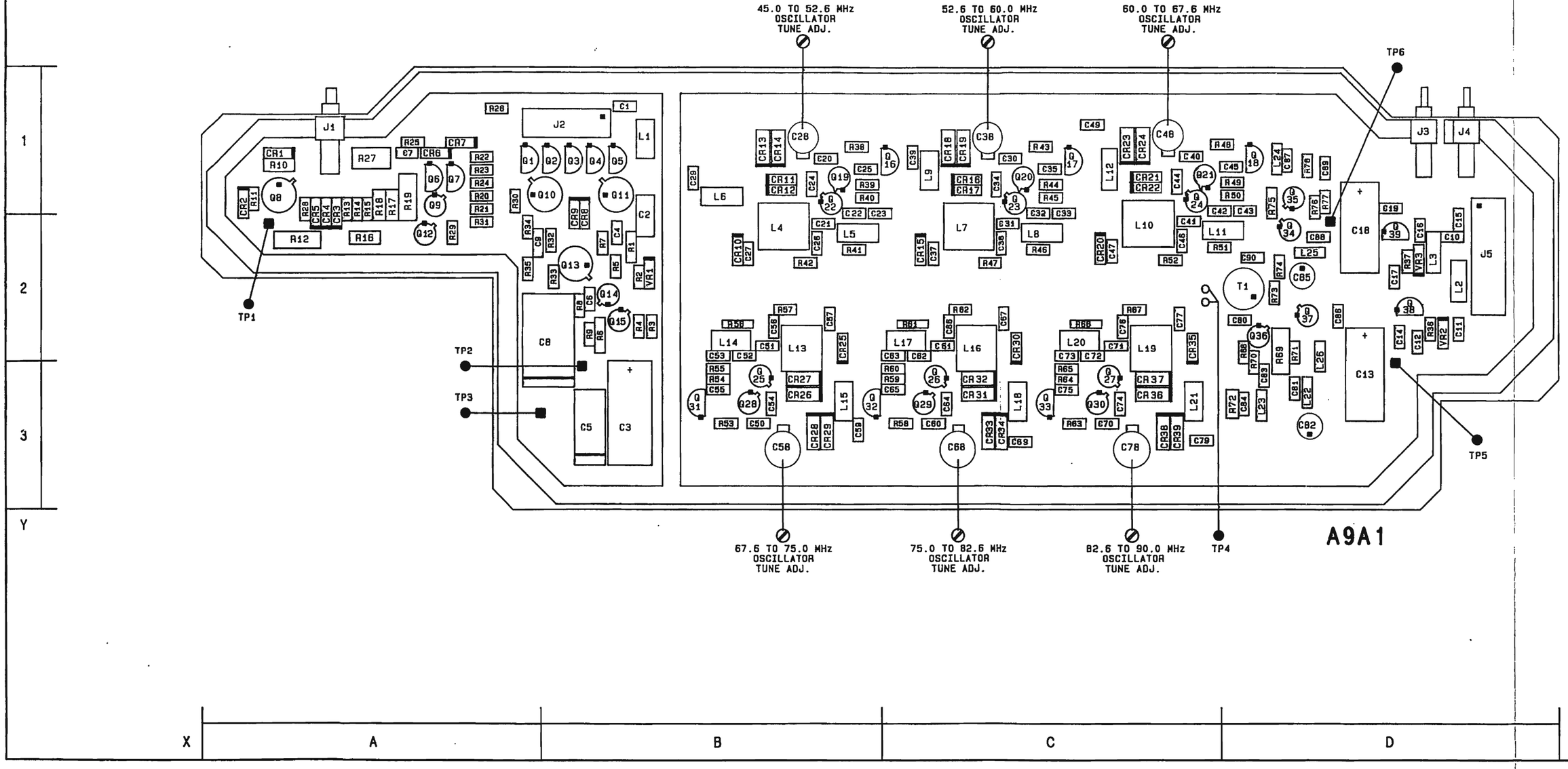
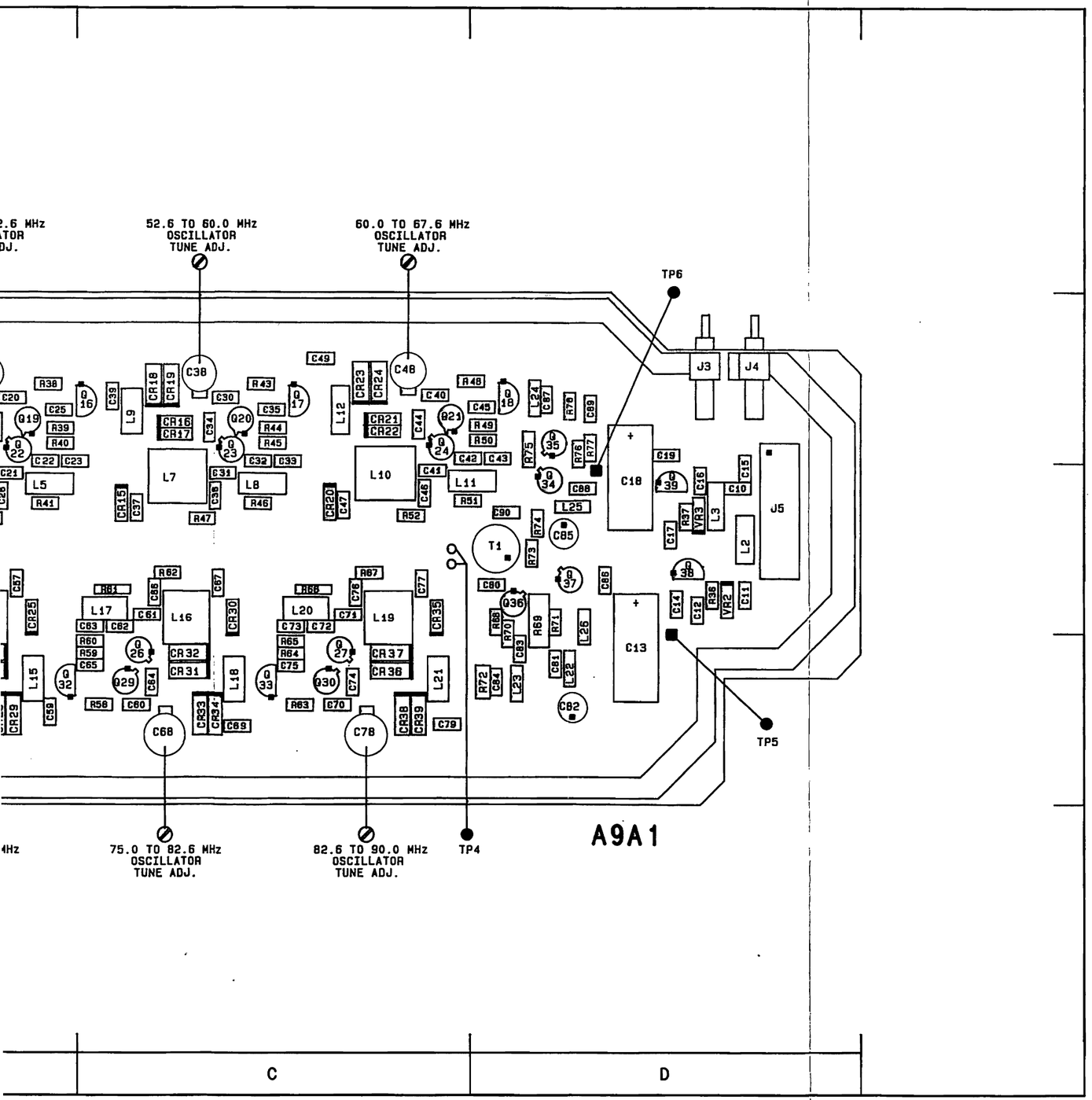


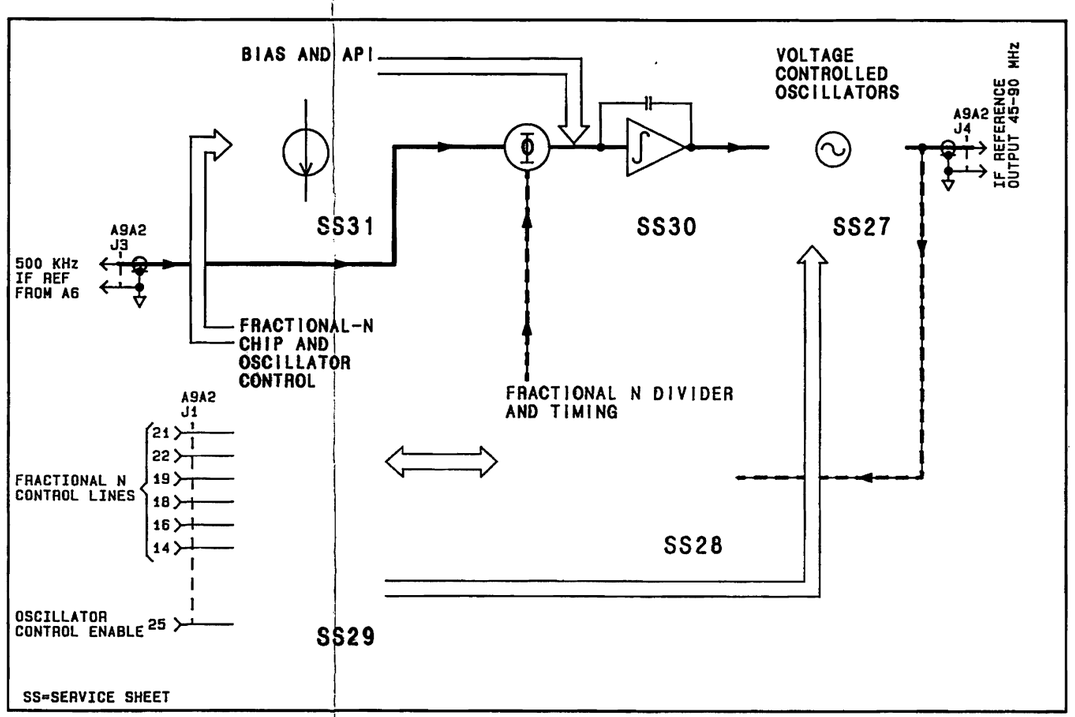
Figure 8M-102. SERVICE SHEET 27 INFORMATION

Component Locator



C D

Component Locator



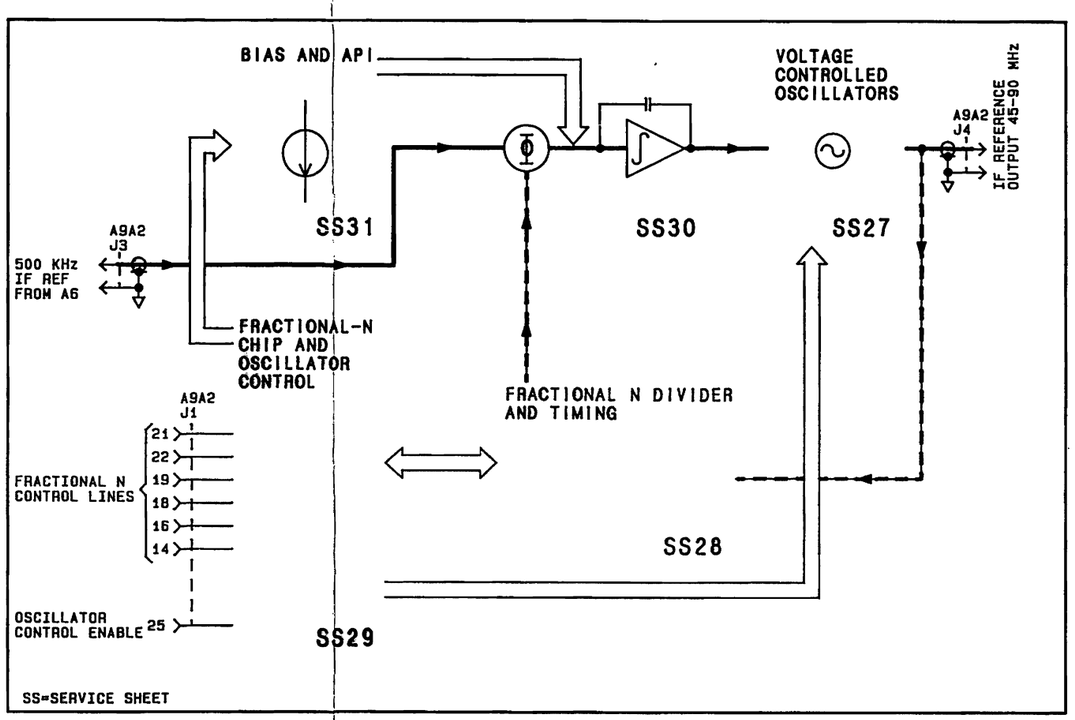
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	B, 1	C38	C, 1	C75	C, 3	CR21	C, 1	L12	C, 1	Q22	B, 1	R19	A, 1	R56	B, 2
C2	B, 1	C39	C, 1	C76	C, 2	CR22	C, 1	L13	B, 2	Q23	C, 1	R20	A, 1	R57	B, 2
C3	B, 3	C40	C, 1	C77	C, 2	CR23	C, 1	L14	B, 2	Q24	C, 1	R21	A, 1	R58	C, 3
C4	B, 2	C41	C, 2	C78	C, 3	CR24	C, 1	L15	B, 3	Q25	B, 3	R22	A, 1	R59	C, 3
C5	B, 3	C42	C, 1	C79	C, 3	CR25	B, 2	L16	C, 2	Q26	C, 3	R23	A, 1	R60	C, 3
C6	B, 2	C43	D, 1	C80	D, 2	CR26	B, 3	L17	C, 2	Q27	C, 3	R24	A, 1	R61	C, 2
C7	A, 1	C44	C, 1	C81	D, 3	CR27	B, 3	L18	C, 3	Q28	B, 3	R25	A, 1	R62	C, 2
C8	B, 2	C45	D, 1	C82	D, 3	CR28	B, 3	L19	C, 2	Q29	C, 3	R26	A, 1	R63	C, 3
C9	A, 2	C46	C, 2	C83	D, 3	CR29	B, 3	L20	C, 2	Q30	C, 3	R27	A, 1	R64	C, 3
C10	D, 2	C47	C, 2	C84	D, 3	CR30	C, 2	L21	C, 3	Q31	B, 3	R28	A, 1	R65	C, 3
C11	D, 2	C48	C, 1	C85	D, 2	CR31	C, 3	L22	D, 3	Q32	B, 3	R29	A, 2	R66	C, 2
C12	D, 2	C49	C, 1	C86	D, 2	CR32	C, 3	L23	D, 3	Q33	C, 3	R30	A, 1	R67	C, 2
C13	D, 3	C50	B, 3	C87	D, 1	CR33	C, 3	L24	D, 1	Q34	D, 2	R31	A, 2	R68	D, 2
C14	D, 2	C51	B, 2	C88	D, 2	CR34	C, 3	L25	D, 2	Q35	D, 1	R32	B, 2	R69	D, 2
C15	D, 2	C52	B, 2	C89	D, 1	CR35	C, 2	L26	D, 2	Q36	D, 2	R33	B, 2	R70	D, 3
C16	D, 2	C53	B, 2	C90	D, 2	CR36	C, 3			Q37	D, 2	R34	A, 2	R71	D, 2
C17	D, 2	C54	B, 3			CR37	C, 3	Q1	A, 1	Q38	D, 2	R35	A, 2	R72	D, 3
C18	D, 2	C55	B, 3	CR1	A, 1	CR38	C, 3	Q2	B, 1	Q39	D, 2	R36	D, 2	R73	D, 2
C19	D, 1	C56	B, 2	CR2	A, 1	CR39	C, 3	Q3	B, 1			R37	D, 2	R74	D, 2
C20	B, 1	C57	B, 2	CR3	A, 1			Q4	B, 1	R1	B, 2	R38	B, 1	R75	D, 1
C21	B, 2	C58	B, 3	CR4	A, 1	J1	A, 1	Q5	B, 1	R2	B, 2	R39	B, 1	R76	D, 1
C22	B, 1	C59	B, 3	CR5	A, 1	J2	B, 1	Q6	A, 1	R3	B, 2	R40	B, 1	R77	D, 1
C23	B, 1	C60	C, 3	CR6	A, 1	J3	D, 1	Q7	A, 1	R4	B, 2	R41	B, 2	R78	D, 1
C24	B, 1	C61	C, 2	CR7	A, 1	J4	D, 1	Q8	A, 1	R5	B, 2	R42	B, 2		
C25	B, 1	C62	C, 2	CR8	B, 1	J5	D, 2	Q9	A, 1	R6	B, 2	R43	C, 1	T1	D, 2
C26	B, 2	C63	C, 2	CR9	B, 1			Q10	B, 1	R7	B, 2	R44	C, 1		
C27	B, 2	C64	C, 3	CR10	B, 2	L1	B, 1	Q11	B, 1	R8	B, 2	R45	C, 1	TP1	A, 2
C28	B, 1	C65	C, 3	CR11	B, 1	L2	D, 2	Q12	A, 2	R9	B, 2	R46	C, 2	TP2	B, 3
C29	B, 1	C66	C, 2	CR12	B, 1	L3	D, 2	Q13	B, 2	R10	A, 1	R47	C, 2	TP3	A, 3
C30	C, 1	C67	C, 2	CR13	B, 1	L4	B, 2	Q14	B, 2	R11	A, 1	R48	D, 1	TP5	D, 2
C31	C, 2	C68	C, 3	CR14	B, 1	L5	B, 2	Q15	B, 2	R12	A, 2	R49	D, 1	TP6	D, 2
C32	C, 1	C69	C, 3	CR15	C, 2	L6	B, 1	Q16	C, 1	R13	A, 1	R50	D, 1		
C33	C, 1	C70	C, 3	CR16	C, 1	L7	C, 2	Q17	C, 1	R14	A, 1	R51	C, 2	VR1	B, 2
C34	C, 1	C71	C, 2	CR17	C, 1	L8	C, 2	Q18	D, 1	R15	A, 1	R52	C, 2	VR2	D, 2
C35	C, 1	C72	C, 2	CR18	C, 1	L9	C, 1	Q19	B, 1	R16	A, 2	R53	B, 3	VR3	D, 2
C36	C, 2	C73	C, 2	CR19	C, 1	L10	C, 2	Q20	C, 1	R17	A, 1	R54	B, 3		
C37	C, 2	C74	C, 3	CR20	C, 2	L11	C, 2	Q21	C, 1	R18	A, 1	R55	B, 3		

A9 MODULE **BD10**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	B, 1	C38	C, 1	C75	C, 3	CR21	C, 1	L12	C, 1	Q22	B, 1	R19	A, 1	R56	B, 2		
C2	B, 1	C39	C, 1	C76	C, 2	CR22	C, 1	L13	B, 2	Q23	C, 1	R20	A, 1	R57	B, 2		
C3	B, 3	C40	C, 1	C77	C, 2	CR23	C, 1	L14	B, 2	Q24	C, 1	R21	A, 1	R58	C, 3		
C4	B, 2	C41	C, 2	C78	C, 3	CR24	C, 1	L15	B, 3	Q25	B, 3	R22	A, 1	R59	C, 3		
C5	B, 3	C42	C, 1	C79	C, 3	CR25	B, 2	L16	C, 2	Q26	C, 3	R23	A, 1	R60	C, 3		
C6	B, 2	C43	D, 1	C80	D, 2	CR26	B, 3	L17	C, 2	Q27	C, 3	R24	A, 1	R61	C, 2		
C7	A, 1	C44	C, 1	C81	D, 3	CR27	B, 3	L18	C, 3	Q28	B, 3	R25	A, 1	R62	C, 2		
C8	B, 2	C45	D, 1	C82	D, 3	CR28	B, 3	L19	C, 2	Q29	C, 3	R26	A, 1	R63	C, 3		
C9	A, 2	C46	C, 2	C83	D, 3	CR29	B, 3	L20	C, 2	Q30	C, 3	R27	A, 1	R64	C, 3		
C10	D, 2	C47	C, 2	C84	D, 3	CR30	C, 2	L21	C, 3	Q31	B, 3	R28	A, 1	R65	C, 3		
C11	D, 2	C48	C, 1	C85	D, 2	CR31	C, 3	L22	D, 3	Q32	B, 3	R29	A, 2	R66	C, 2		
C12	D, 2	C49	C, 1	C86	D, 2	CR32	C, 3	L23	D, 3	Q33	C, 3	R30	A, 1	R67	C, 2		
C13	D, 3	C50	B, 3	C87	D, 1	CR33	C, 3	L24	D, 1	Q34	D, 2	R31	A, 2	R68	D, 2		
C14	D, 2	C51	B, 2	C88	D, 2	CR34	C, 3	L25	D, 2	Q35	D, 1	R32	B, 2	R69	D, 2		
C15	D, 2	C52	B, 2	C89	D, 1	CR35	C, 2	L26	D, 2	Q36	D, 2	R33	B, 2	R70	D, 3		
C16	D, 2	C53	B, 2	C90	D, 2	CR36	C, 3			Q37	D, 2	R34	A, 2	R71	D, 2		
C17	D, 2	C54	B, 3			CR37	C, 3	Q1	A, 1	Q38	D, 2	R35	A, 2	R72	D, 3		
C18	D, 2	C55	B, 3	CR1	A, 1	CR38	C, 3	Q2	B, 1	Q39	D, 2	R36	D, 2	R73	D, 2		
C19	D, 1	C56	B, 2	CR2	A, 1	CR39	C, 3	Q3	B, 1			R37	D, 2	R74	D, 2		
C20	B, 1	C57	B, 2	CR3	A, 1			Q4	B, 1	R1	B, 2	R38	B, 1	R75	D, 1		
C21	B, 2	C58	B, 3	CR4	A, 1	J1	A, 1	Q5	B, 1	R2	B, 2	R39	B, 1	R76	D, 1		
C22	B, 1	C59	B, 3	CR5	A, 1	J2	B, 1	Q6	A, 1	R3	B, 2	R40	B, 1	R77	D, 1		
C23	B, 1	C60	C, 3	CR6	A, 1	J3	D, 1	Q7	A, 1	R4	B, 2	R41	B, 2	R78	D, 1		
C24	B, 1	C61	C, 2	CR7	A, 1	J4	D, 1	Q8	A, 1	R5	B, 2	R42	B, 2				
C25	B, 1	C62	C, 2	CR8	B, 1	J5	D, 2	Q9	A, 1	R6	B, 2	R43	C, 1	T1	D, 2		
C26	B, 2	C63	C, 2	CR9	B, 1			Q10	B, 1	R7	B, 2	R44	C, 1				
C27	B, 2	C64	C, 3	CR10	B, 2	L1	B, 1	Q11	B, 1	R8	B, 2	R45	C, 1	TP1	A, 2		
C28	B, 1	C65	C, 3	CR11	B, 1	L2	D, 2	Q12	A, 2	R9	B, 2	R46	C, 2	TP2	B, 3		
C29	B, 1	C66	C, 2	CR12	B, 1	L3	D, 2	Q13	B, 2	R10	A, 1	R47	C, 2	TP3	A, 3		
C30	C, 1	C67	C, 2	CR13	B, 1	L4	B, 2	Q14	B, 2	R11	A, 1	R48	D, 1	TP5	D, 2		
C31	C, 2	C68	C, 3	CR14	B, 1	L5	B, 2	Q15	B, 2	R12	A, 2	R49	D, 1	TP6	D, 2		
C32	C, 1	C69	C, 3	CR15	C, 2	L6	B, 1	Q16	C, 1	R13	A, 1	R50	D, 1				
C33	C, 1	C70	C, 3	CR16	C, 1	L7	C, 2	Q17	C, 1	R14	A, 1	R51	C, 2	VR1	B, 2		
C34	C, 1	C71	C, 2	CR17	C, 1	L8	C, 2	Q18	D, 1	R15	A, 1	R52	C, 2	VR2	D, 2		
C35	C, 1	C72	C, 2	CR18	C, 1	L9	C, 1	Q19	B, 1	R16	A, 2	R53	B, 3	VR3	D, 2		
C36	C, 2	C73	C, 2	CR19	C, 1	L10	C, 2	Q20	C, 1	R17	A, 1	R54	B, 3				
C37	C, 2	C74	C, 3	CR20	C, 2	L11	C, 2	Q21	C, 1	R18	A, 1	R55	B, 3				

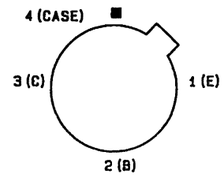
SEE REVERSE SIDE

A9 MODULE **BD10**

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

A9A1
Q36,Q37
TOP VIEW



All Serial Prefixes

On the component locator:

- C85 - Delete C85.

In component coordinates:

- C85 - Delete C85.

In Schematic General Information (Notes):

- Q36, Q37 - On the Top View diagram of Q36, Q37, the pin numbering should be changed as follows: Going counterclockwise from the key - square pad pin 1 (E), pin 2 (B), pin 3 (C), pin 4 (CASE).

On the schematic:

- C9 - In **LOOP CONTROL**, change C9 to 0.047μ.
- C28, C38, C48 - In **VOLTAGE CONTROLLED OSCILLATORS**, change C28, C38, and C48 (all labeled "OSCILLATOR TUNE ADJUST") ranges to span 1.7 to 7.4p.
- C85 - In **POWER SPLITTER**, delete C85. In the same location, change +15V(F2) to +15V(F3).
- C30, C31, C32 - In **VOLTAGE CONTROLLED OSCILLATORS**, under the "52.6-60.0 MHz bracket, change C30 and C31 to 6.8p. In the same location, change C32 to 10p.

2615A and above

On the schematic:

- C70 - In **VOLTAGE CONTROLLED OSCILLATORS**, under the "82.6 - 90.0 MHz bracket, change C70 from 2.7p to 2.2 pF.
- C71 - In **VOLTAGE CONTROLLED OSCILLATORS**, under the "82.6 - 90.0 MHz bracket, change C71 from 2.7p to 3.3 pF.
- R78 - In the lower portion of **POWER SPLITTER**, connect the base of Q35 to ground and delete R78.

CHANGES

2729A and above

On the Schematic:

- L5, L6, L8, L9, L11, L12, L14, L15, L17, L18,L,20, L21, -

  In **VOLTAGE CONTROLLED OSCILLATORS** change the following;

  Under *45.0 - 52.6 MHz* change L5 and L6 to 6.8 uH.
  Under *52.6 - 60.0 MHz* change L8 and L9 to 4.7 uH.
  Under *60.0 - 67.6 MHz* change L11 and L12 to 4.7 uH.
  Under *67.5 - 75.0 MHz* change L14 and L15 to 4.7 uH.
  Under *75.0 - 82.6 MHz* change L17 and L18 to 4.7 uH.
  Under *82.6 - 90.0 MHz* change L20 and L21 to 3.9 uH.

A9A1 IF VCO ASSEMBLY (08642-60104)

TUNE/ERROR SIGNAL

V TO I — SHAPING NETWORK

VCO TUNE VOLTAGE A9M1
30 BK (847) — J1

+47V
R10 21.5K
CR1
Q8
CR2
R11 5110
CR3 CR4 CR5
R12 5110
R13 14.7k
R14 10k
R15 6810
+47V
R16 750
R17 619
R18 422
R19 1620

IMPEDENCE BUFFER

R28 100

LOOP CONTROL

SPEED-UP CIRCUITRY

Q10
+47V
R32 511
CR9
CR8
Q11
R33 464

Q12
+47V

R29 38.3k
R30 11k
Q9
R31 10k

LEAD/LAG FILTER
R34 31.6k
R35 2150
C8 1µ
C9 0.022µ
TP3

PRETUNE

5 BIT DAC — V TO I

J2
P1 Q4 R20 19.6k
P2 Q5 R21 10k
P4 Q1 R22 5110
P8 Q2 R23 2610
P16 Q3 R24 1210

TP1
Q7
Q6
PRETUNE ADJ.
R25 38.3k
CW
R27 10k
+47V
C7 0.1µ
CR6
CR7
R26 5110

PRETUNE LEVEL CONTROL
29 BL — 4 5 6 7 8

POWER SUPPLY AND GND

+47V REGULATOR/FILTER

J5
1 +50V (F2)
L1 47µ
C1 470p
C2 0.047µ
R1 1k
R2 26.1k
C4 56p
R5 825
R4 100
VR1 24V
C3 50µ
R3 51.1k
R7 34.8
Q13
Q14
Q15
R6 8250
C5 0.068µ
R8 11k
R9 26.1k
C6 0.1µ
TP2
+47V

4 +15V (F2)
L2 47µ
C10 0.1µ
C11 0.1µ
VR2 2.4V
Q38
R36 10k
C12 0.1µ
C13 150µ
C14 0.1µ
TP5
+15V (F3)

3 -15V (F3)
L3 47µ
C15 0.1µ
C16 0.1µ
VR3 2.4V
Q39
R37 10k
C17 0.1µ
C18 150µ
C19 0.1µ
TP6
-15V (F3)

5 GND

POWER SUPPLY LINES AND GND
28 BN — 5

OSCILLATOR SELECT LINES
29 BN — 6
6 7 8 9 10 11
A B C D E F

VOLTAGE CONTROLLED OSCILLATORS

45.0-52.6 MHz

+15V (F3)
C20 7.5p
C23 0.01µ
L5 22µ
Q19
Q22
R38 34.8k
R39 4640
C24 0.01µ
R40 4640
C21 7.5p
C22 11p
C26 0.01µ
L4 320n
CR10
C28 1.3-5.4P
OSCILLATOR TUNE ADJ.
CR11 CR12
L6 22µ
CR13 CR14
C29 4700P
C25 0.01µ
Q16
R41 100k
-15V (F3)
R42 2150
C27 0.047µ
ENABLE
VCO TUNE

67.6-75.0 MHz

+15V (F3)
C50 3.9p
C53 0.01µ
L14 15µ
Q28
Q25
R53 34.8k
R54 4640
C54 0.01µ
R55 4640
C51 3.9p
C52 5.6P
C56 0.01µ
L13 200n
CR25
C58
OSCILLATOR TUNE ADJ.
CR26 CR27
L15 15µ
CR28 CR29
C59 4700P
C55 0.01µ
Q31
R56 100k
-15V (F3)
R57 2150
C57 0.047µ
ENABLE

A, B, C 3

SERIAL PREFIX: 2427A

52.6-60.0 MHz

+15V (F3)

L8 18µ

C31 5.6p

L7 220n

C38 1.3-5.4P

OSCILLATOR TUNE ADJ.

CR16 CR17

C32 8.2p

C36 0.01µ

CR15

L9 18µ

CR18 CR19

C39 4700P

Q20 Q23

R44 4640 C34 0.01µ R45 4640

Q17

R46 100k

-15V (F3)

R47 2150

C37 0.047µ

ENABLE

VCO TUNE

B

2

60.0-67.6 MHz

+15V (F3)

L11 18µ

C40 4.7p C43 0.01µ

C41 4.7p

L10 200n

C42 6.8p

C48 1.3-5.4P

OSCILLATOR TUNE ADJ.

CR21 CR22

R48 34.8k

Q21 Q24

R49 4640 C44 0.01µ R50 4640

C46 0.01µ

CR20

L12 18µ

CR23 CR24

C49 4700P

C45 0.01µ

Q18

R51 100k

-15V (F3)

R52 2150

C47 0.047µ

ENABLE

VCO TUNE

C

75.0-82.6 MHz

+15V (F3)

L17 15µ

C61 2.7p

L16 180n

C68 1.3-5.4P

OSCILLATOR TUNE ADJ.

CR31 CR32

C62 3.9p

C66 0.01µ

CR30

L18 15µ

CR33 CR34

C69 4700P

Q29 Q26

R59 4640 C64 0.01µ R60 4640

Q32

R61 100k

-15V (F3)

R62 2150

C67 0.047µ

ENABLE

E

2

82.6-90.0 MHz

+15V (F3)

L20 12µ

C70 2.7p C73 0.01µ

C71 2.7p

L19 160n

C78 1.3-5.4P

OSCILLATOR TUNE ADJ.

CR36 CR37

C72 3.9p

R63 34.8k

Q30 Q27

R64 4640 C74 0.01µ R65 4640

C76 0.01µ

CR35

L21 12µ

CR38 CR39

C79 4700P

C75 0.01µ

Q33

R66 100k

-15V (F3)

R67 2150

C77 0.047µ

ENABLE

F

2

POWER SPLITTER

BUFFER AMPLIFIER

+15V (F3)

ATTENTION Static Sensitive Devices

L23 3µ

R72 316

C84 0.01µ

C83 0.01µ

L26 3µ

C86 0.01µ

J4

W30

950

80

38

IF REFERENCE LOOP OUTPUT

C80 0.01µ

Q36

Q37

R70 10

R71 10

E1

R68 56.2

R69 750

L22 3µ

C81 0.01µ

C82 +10µ

-15V (F3)

TP4

T1

R73 26.1

BUFFER AMPLIFIER

+15V (F2)

L25 3µ

+ C85 10µ

C88 0.01µ

R76 1960

R77 1960

C89 0.01µ

J3

A9W2

G93

BP

28

FN LOOP FEEDBACK (45-90 MHz)

C90 0.01µ

Q34

Q35

R74 56.2

R78 100

R75 1210

C87 0.01µ

L24 3µ

-15V (F3)

SS27

Figure 8M-103
8M-103

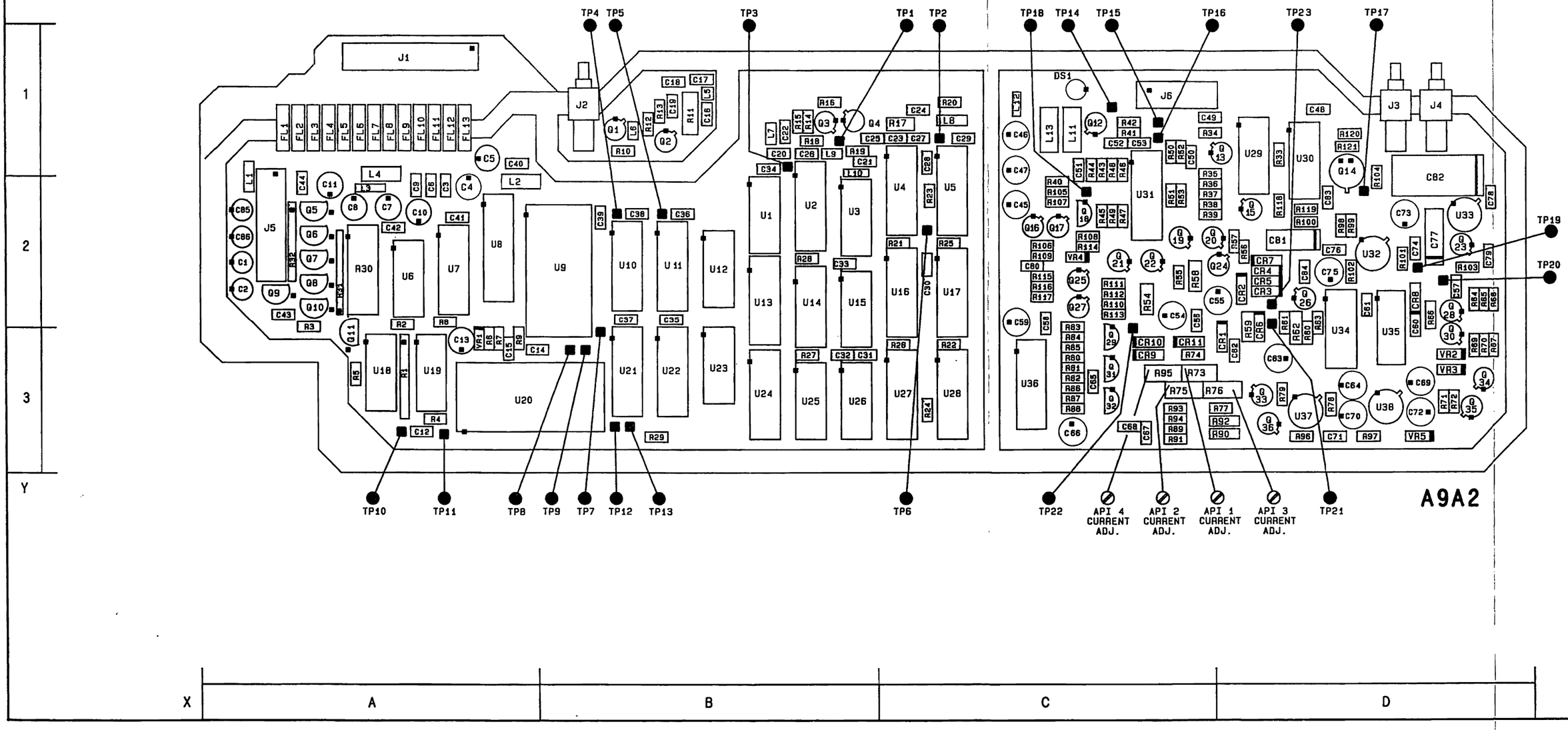
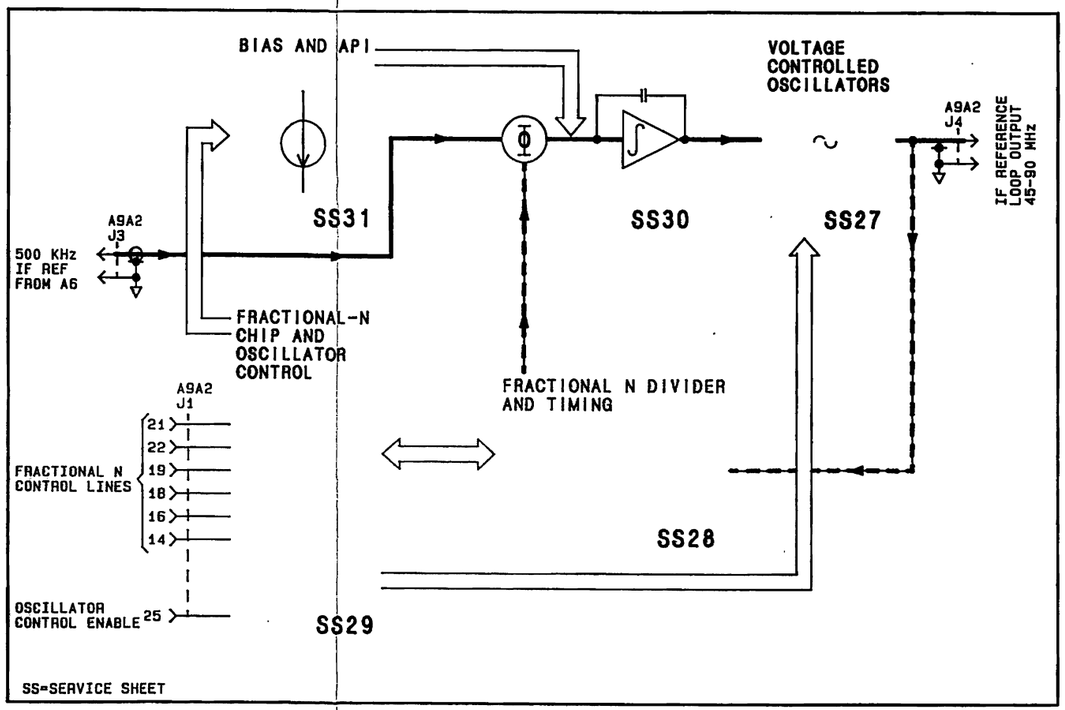


Figure 8M-104. SERVICE SHEET 28 INFORMATION

Component Locator



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	A, 2	J1	A, 1	TP1	B, 1										
C2	A, 2	J2	B, 1	TP2	C, 1										
C3	A, 2	J5	A, 2	TP3	B, 1										
C4	A, 2	J6	C, 1	TP4	B, 2										
C5	A, 1			TP6	C, 2										
C6	A, 2	L1	A, 2	TP8	B, 3										
C7	A, 2	L2	A, 2	TP10	A, 3										
C8	A, 2	L3	A, 2	TP11	A, 3										
C9	A, 2	L4	A, 1												
C10	A, 2	L5	B, 1	U2	B, 2										
C11	A, 2	L6	B, 1	U3	B, 2										
C16	B, 1	L7	B, 1	U4	C, 2										
C17	B, 1	L8	C, 1	U5	C, 2										
C18	B, 1	L9	B, 1	U15	B, 2										
C19	B, 1	L10	B, 1	U16	C, 2										
C20	B, 1			U17	C, 2										
C21	B, 1	Q1	B, 1	U26	B, 3										
C22	B, 1	Q2	B, 1	U27	C, 3										
C23	C, 1	Q3	B, 1	U28	C, 3										
C24	C, 1	Q4	B, 1												
C25	B, 1														
C26	B, 1	R10	B, 1												
C27	C, 1	R11	B, 1												
C28	C, 1	R12	B, 1												
C29	C, 1	R13	B, 1												
C30	C, 2	R14	B, 1												
C85	A, 2	R15	B, 1												
C86	A, 2	R16	B, 1												
		R17	C, 1												
FL10	A, 1	R18	B, 1												
FL11	A, 1	R19	B, 1												
FL12	A, 1	R20	C, 1												
FL13	A, 1	R21	C, 2												
		R22	C, 3												
		R23	C, 2												
		R24	C, 3												
		R25	C, 2												

SEE REVERSE SIDE

A9A1 IF VCO ASSEMBLY **SS27**

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. A9 FL1, A9 FL2 are low pass feedthrough filters passing through the center of the module to make connections between two (2) printed circuit boards.
3. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

PRE-SCALER

BUFFER AMPLIFIER — DIVIDE-BY-2 PRESCALE

FN LOOP FEEDBACK (45-90 MHz) A9W2

27 BP — 834 — J2

+5V (F2)

L6 3µ — C18 0.01µ — C19 0.01µ — TP3 V.C.O.

R12 10 — R13 147 — Q1 — Q2

R10 75 — R11 750

L5 3µ — C17 0.01µ — C16 0.01µ — -15V (F2)

+5V (F2)

L7 3µ — C20 0.01µ — C21 0.01µ

U2

1		16
7	S	2
5	1D	
6	=1 C1	
9		
4	R (ECL)	3
12	S	15 NC
10	1D	
11	=1 C1	
9		
13	R (ECL)	14 NC
		8

R14 1k

TP1 V.C.O. ÷2 — R15 1k — VCO ÷2

ECL TO TTL TRANSLATOR

ISOLATION BUFFER

+5V (F2)

L9 3µ — C25 0.01µ — C26 0.01µ

R18 100 — R19 383 — Q3 — Q4

R17 1210

L8 3µ — C24 0.01µ — C23 0.01µ — -15V (F2)

C22 0.01µ — R16 75

L10 3.9µ

+5V (F2) — C28 0.01µ

TP2 V.C.O. ÷2 — C27 0.01µ — U3 — TP6

13 — 14 — 12 — 7, 1, 3, 5, 9, 11

VCO ÷2

POWER SUPPLIES AND GND

P/O J1

1	+50V	FL13	C85 2.2µ + C86 2.2µ	L1 3.9µ — C1 2.2µ + C2 2.2µ
2, 3, 4	+15V	FL12	C3 0.1µ	L2 27µ — C4 10µ — C5 10µ
5, 6, 7	+5V	FL11	C6 0.1µ	L3 3µ — C7 33µ — C8 33µ
11	-15V	FL10	C9 0.1µ	L4 27µ — C10 10µ — C11 10µ
12, 13, 15, 17, 20, 23	GND			

POWER SUPPLY AND GND 66 CR

+50V (F1) — +15V (F1) — +15V (F2) — +5V (F1) — +5V (F2) — -15V (F1) — -15V (F2) — GND — GND — GND

POWER SUPPLY AND GND CH 29

POWER SUPPLY AND GND BY 30

P/O J5 — P/O J6

P/O 8642-60003

P/O FL1 (NOTE 2)

1	+50V (F1)	+50V (F2)
4	+15V (F1)	+15V (F2)
3	-15V (F1)	-15V (F2)
5	GND	GND
1	GND	GND

P/O FL2 (NOTE 2)

POWER SUPPLY LINES AND GROUND BM 27

DIVIDE BY 2 OR 3 PRESCALER

+5V (F2) — R21 10k

ODD/EVEN LATCH — PULSE REMOVE GATING

+5V (F2) — U15A

2	1D	5
3	C1	
1	R	
4	S	6 NC
		7

+5V (F2) — U26A — U26D

LS BIT 1 29 CQ

PRE-SCALE SELECT 29 CO

PULSE REMOVE 29 CK

TP8 PULSE REMOVE

+5V (F2) — R22 10k — U27A

3	1J	
1	C1	
2	1K	
4	S	
15	R	

PUL

SERIAL PREFIX: 2427A

OUTPUT SYNCHRONIZATION

+5V (F2)
R20
10k
+5V (F2)
C29
0.01µ
OUTPUT SYNCHRONIZATION
29 CL
U15B
U5A
U5B
VCO ÷N.F
FN LOOP IF
BX 30
NC

ATTENTION
Static Sensitive Devices

LATCH ENABLE
CI 29

PULSE REMOVE FLIP-FLOP
PRESCALER
TP10
V.C.O. ÷4 OR 6
CE 29
VCO ÷2
+5V (F2)
C30
0.01µ
U27A
U27B
U16A
U16B
R23
10k
U4B
U4A
NC

TIMING
CHIP CLOCK
+5V (F2)
R24
10k
U28A
U28B
VCO ÷20
TP4
FN CHIP CLOCK
CG 29
CYCLE START
+5V (F2)
R25
10k
TP11
CF 29
U17A
U17B
OSCILLATOR CONTROL CLOCK
CN 29

CYCLE RESET
29 CP

SS28
Figure 8M-105
8M-105

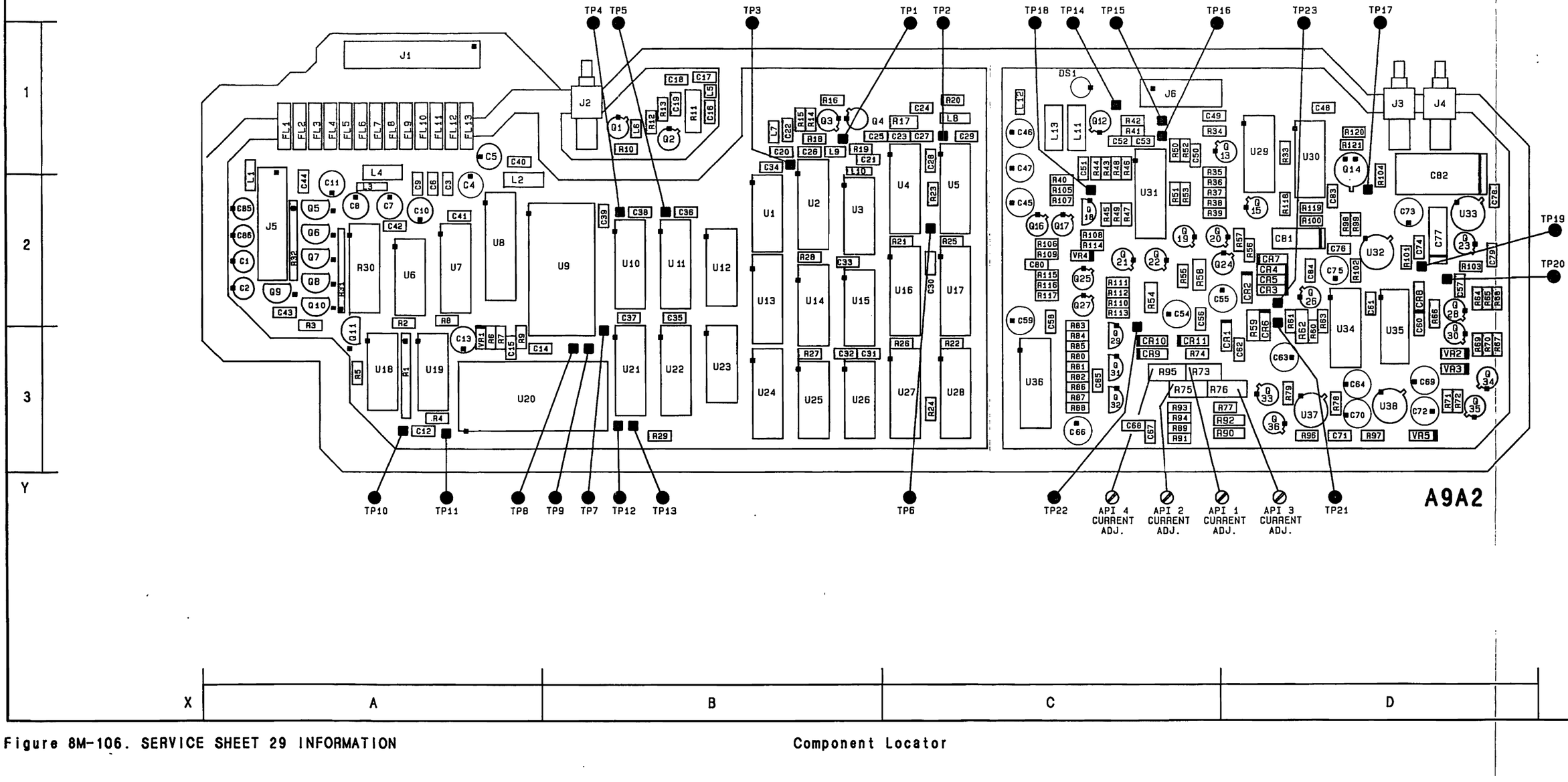
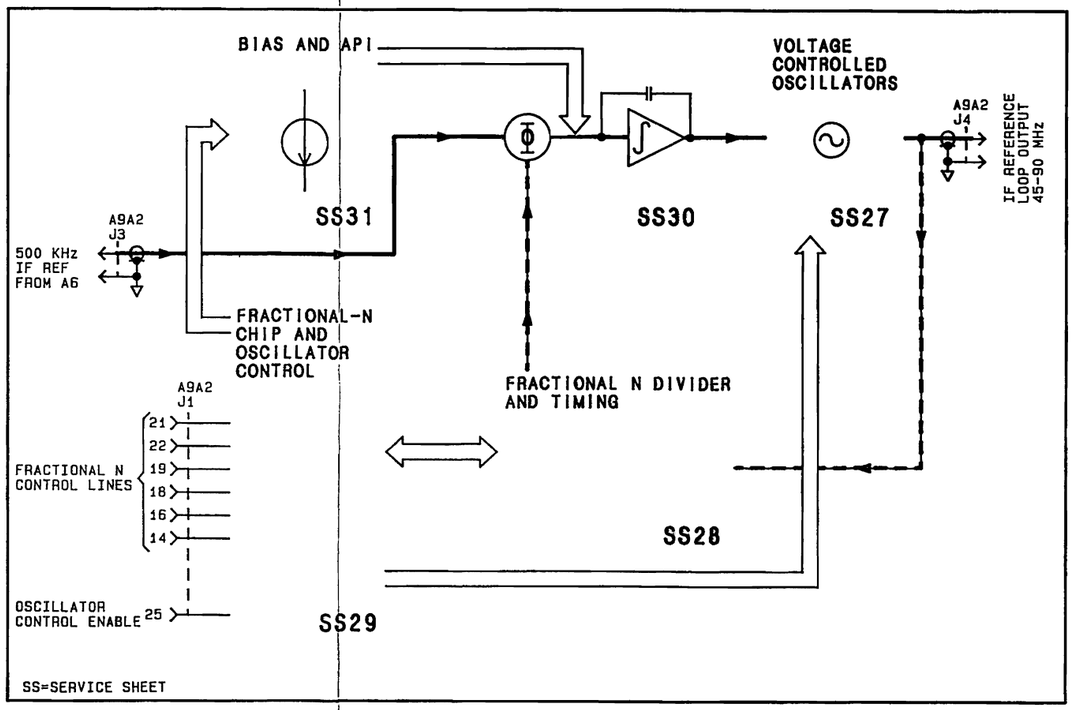


Figure 8M-106. SERVICE SHEET 29 INFORMATION

Component Locator



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C12	A, 3	Q5	A, 2	U1	B, 2												
C13	A, 3	Q6	A, 2	U6	A, 2												
C14	A, 3	Q7	A, 2	U7	A, 2												
C15	A, 3	Q8	A, 2	U8	A, 2												
C31	B, 3	Q9	A, 2	U9	B, 2												
C32	B, 3	Q10	A, 2	U10	B, 2												
C33	B, 2	Q11	A, 3	U11	B, 2												
C34	B, 1			U12	B, 2												
C35	B, 2	R1	A, 3	U13	B, 2												
C36	B, 2	R2	A, 2	U14	B, 2												
C37	B, 2	R3	A, 2	U18	A, 3												
C38	B, 2	R4	A, 3	U19	A, 3												
C39	B, 2	R5	A, 3	U20	A, 3												
C40	A, 1	R6	A, 3	U21	B, 3												
C41	A, 2	R7	A, 3	U22	B, 3												
C42	A, 2	R8	A, 2	U23	B, 3												
C43	A, 2	R9	A, 3	U24	B, 3												
C44	A, 2	R26	C, 3	U25	B, 3												
		R27	B, 3	U26	B, 3												
FL2	A, 1	R28	B, 2														
FL3	A, 1	R29	B, 3	VR1	A, 3												
FL4	A, 1	R30	A, 2														
FL5	A, 1	R31	A, 2														
FL6	A, 1	R32	A, 2														
FL7	A, 1																
FL8	A, 1	TP5	B, 2														
FL9	A, 1	TP7	B, 3														
		TP9	B, 3														
J1	A, 1	TP12	B, 3														
J5	A, 2	TP13	B, 3														
J6	C, 1																

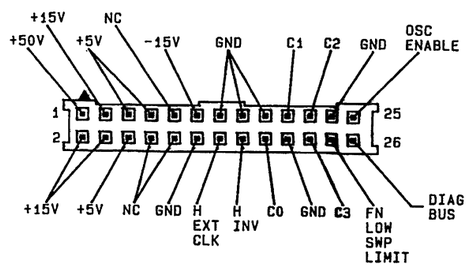
SEE REVERSE SIDE

P/O A9A2 FRACTIONAL-N ASSEMBLY **SS28**

Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. A9 FL4-FL9 must have solder connection from notched portion of shielding to outer body of feedthroughs.
3. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
4. A9 FL1, A9 FL2 are low pass feedthrough filters passing through the center of the module to make connections between two (2) printed circuit boards.

CABLE PLUG TO A9A2 J1



CHANGES

2637A and above

On the Component Locator:

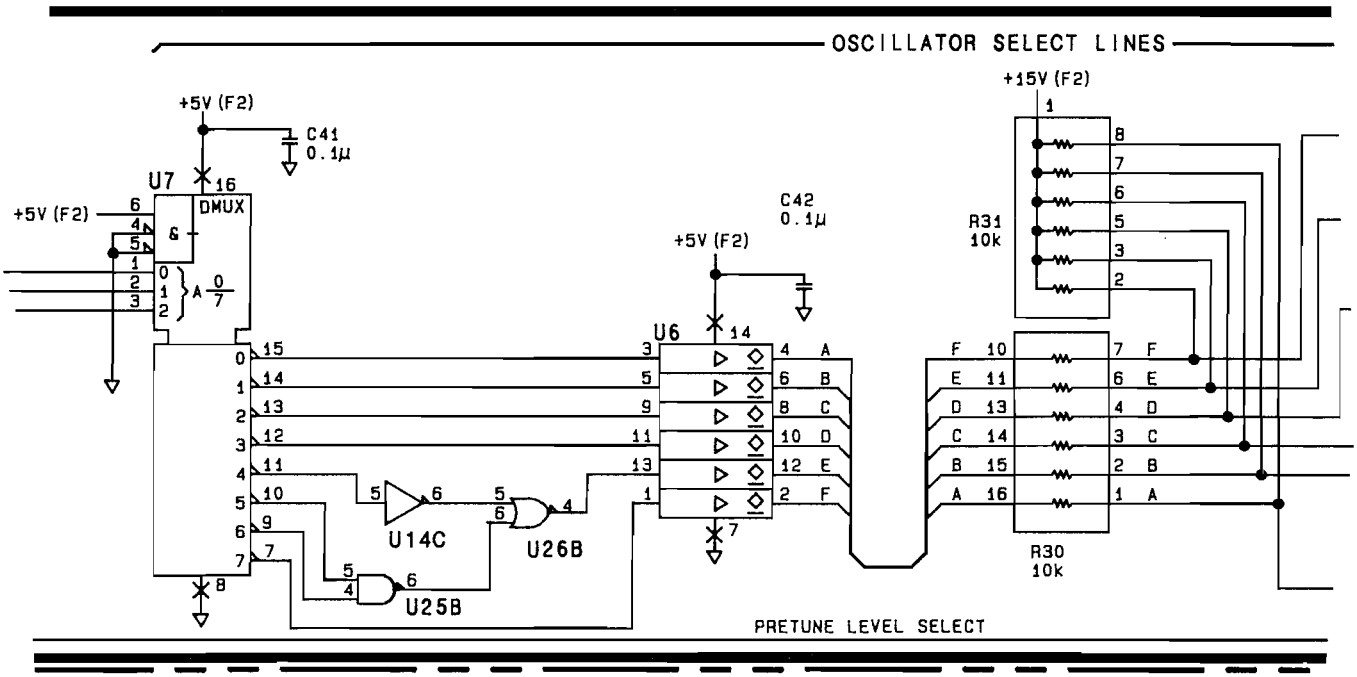
- R122 - Between R5 and Q11, add a resistor R122. Note that R122 is added to the back (solder) side of the board.

In Component Coordinates:

- R122 - Add R122 A,3

On the Schematic:

- In **FRACTIONAL-N CHIP**, add a resistor from the base of Q11 to ground. Designate it R122, and assign a value of 10k ohms.
- In **OSCILLATOR CONTROL**, change the description of U9 from "EPROM" to "PROM".
- In **OSCILLATOR CONTROL**, replace the appropriate portion of circuitry with the partial provided on page 8M-106.3



CHANGES TO FIGURE 8M-107 (All Serial Prefixes)

P/O A5A2 FRACTIONAL-N ASSEMBLY (08642-60107)

P/O A5 DISTRIBUTION ASSY SS66

FRACTIONAL-N CONTROL LINES 11 (C8)

DELAYED BIAS 31 (CD)

P/O J1

FN C2 — FL4 (NOTE 2)

FN C3 — FL5 (NOTE 2)

FN C1 — FL6 (NOTE 2)

FN C0 — FL7 (NOTE 2)

FN H INV — FL8 (NOTE 2)

FN H EXT CLK — FL9 (NOTE 2)

V.C.O. ÷4 OR 6 28 (CE)

CYCLE START 28 (CF)

FN CHIP CLOCK 28 (CG)

FRACTIONAL N CHIP

U18 — C2, C3, C1, C0, EXT CLK

U19 — R2 2150, C12 0.01µ, R4 3160, INV

R1 10k

FRACTIONAL-N CONTROL

U20 — VDD, VGG, VBG, GND

VR1 3.3V

C13 10µ, C14 0.01µ

CYCLE REMOVE, BIAS, R CLK, S/H CONT

DATA CONT: C0, C1, C2, C3

PHASE DATA: API 1 … API 5

SLF/CO, ÷N CLK, DATA: D1, D2, D4, D8

INST VLD, DV, EXT CLK, CYCLE START, CHIP CLK, SWP LIM

FRACTIONAL-N CONTROLLER (NMOS)

R5 10k, R3 10k, Q11, FL3

R6 12.1k, C15 0.01µ, R7 4640, -15V (F2)

R8 3160, R9 1960

PULSE REMOVE (CK) 28

SAMPLE CONTROL (BZ) 30

OUTPUT SYNCHRONIZATION (CL) 28

BIAS AND API ENABLE (BR) 31

LATCH CLK (CM) 31

U26C, U14F, U25A

DIVIDE COUNTER

SHIFT REGISTERS

R29 10k, C37 0.01µ, P/O U21

C38 0.01µ, P/O U10

TP7

M1, M2, M4

OSCILLATOR CONTROL ENABLE 11 (CC)

P/O J1 — FN OSC CON

OSCILLATOR CONTROL

FL2

CONTROL RO

U9 EPROM 2048

L1, L2, L4, L8, S1, S2, S4, S8, M1, M2

(PWR DWN)

OSCILLATOR CONTROL CLOCK 28 (CN)

LATCH ENABLE 28 (CI)

P/O J1 — 24 — P/O A5 ASSY SS66 — FN LOW SWEEP LIMIT (UU) 9

ATTENTION Static Sensitive Devices

POWER SUPPLIES AND GND

POWER SUPPLY AND GND 28 (CH) 4

+15V (F2), +5V (F2), -15V (F2), GND

SERIAL PREFIX: 2427A

DIVIDE COUNTER

PULSE REMOVE CK 28

SAMPLE CONTROL BZ 30

OUTPUT SYNCHRONIZATION CL 28

BIAS AND API ENABLE BR 31

LATCH CLK CM 31

SHIFT REGISTERS

P/O U21

P/O U10

DIVIDE BY 10 COUNTER (SECOND DIGIT)

DIVIDE BY 10 COUNTER (MOST SIG. DIGIT)

PRELOAD ONE-SHOT

DIVIDE BY 5 COUNTER (LEAST SIG. DIGIT)

OSCILLATOR CONTROL

FL2

CONTROL ROM

U9 EPROM 2048x8

U8

U7 DMUX

OSCILLATOR SELECT LINES

PRETUNE LEVEL SELECT

FN LOW SWEEP LIMIT UU 9

P/O A5 ASSY SS66

ATTENTION Static Sensitive Devices

OSCILLATOR CONTROL CLOCK 28 CN

Scans by ArtekMedia => 2009

DIVIDE BY 10 COUNTER (MOST SIG. DIGIT)

DIVIDE BY 10 COUNTER (SECOND DIGIT)

SHIFT REGISTERS

DIVIDE BY 5 COUNTER (LEAST SIG. DIGIT)

PRELOAD ONE-SHOT

PRELOAD ENABLE FLIP-FLOP

PRELOAD FLIP-FLOP

PRESCALE SELECT

CYCLE RESET

LS BIT 1

OSCILLATOR SELECT LINES

PRETUNE LEVEL SELECT

P/O 08642-60003

P/O A9FL1 (NOTE 4)

P/O A9FL2 (NOTE 4)

OSCILLATOR SELECT LINES

PRETUNE LEVEL CONTROL

SS29

Figure 8M-107
8M-107

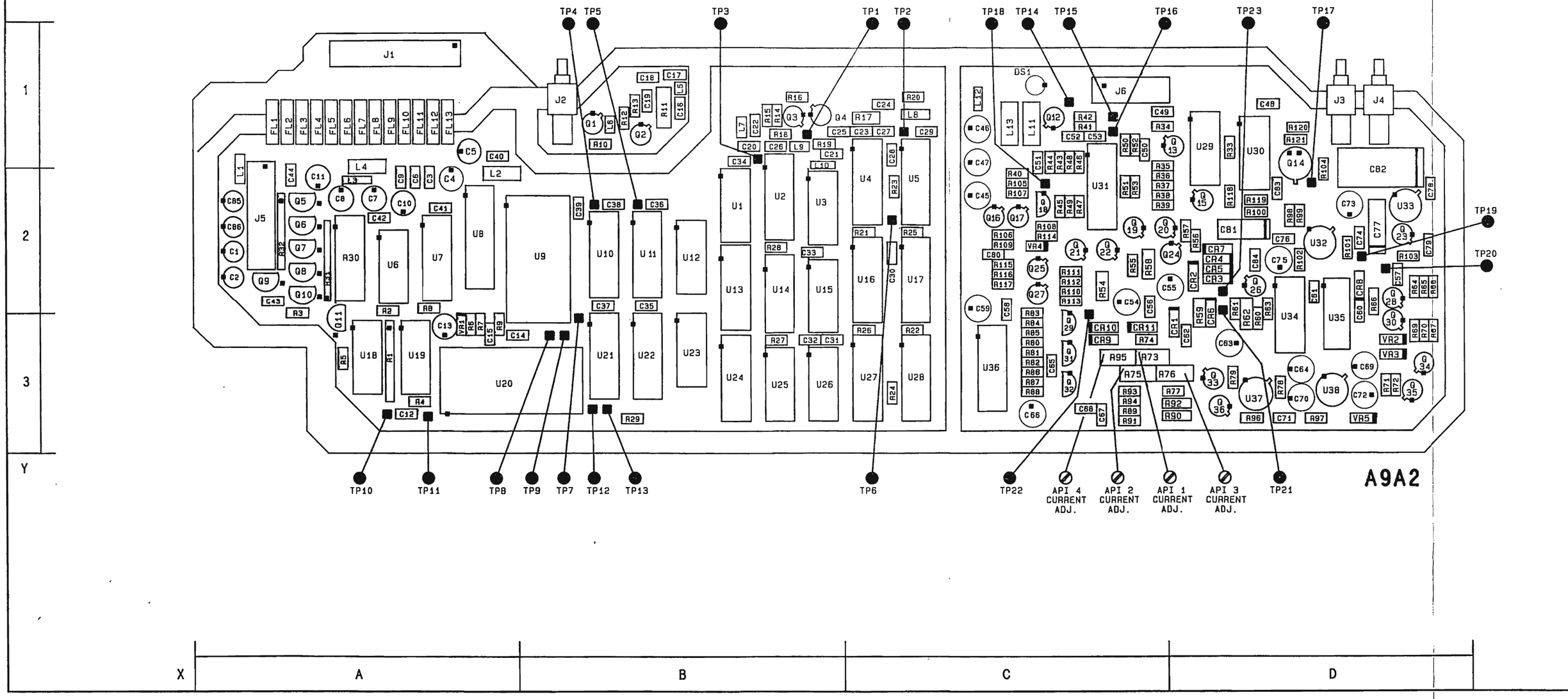
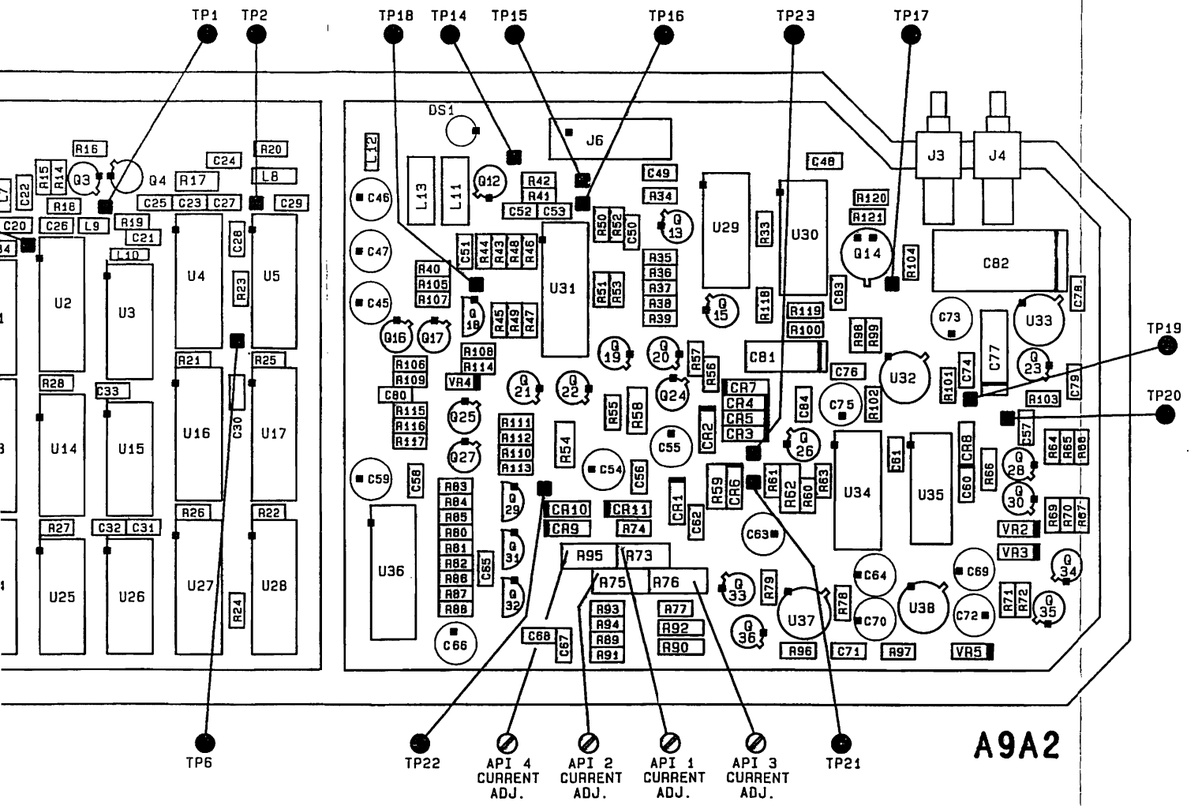


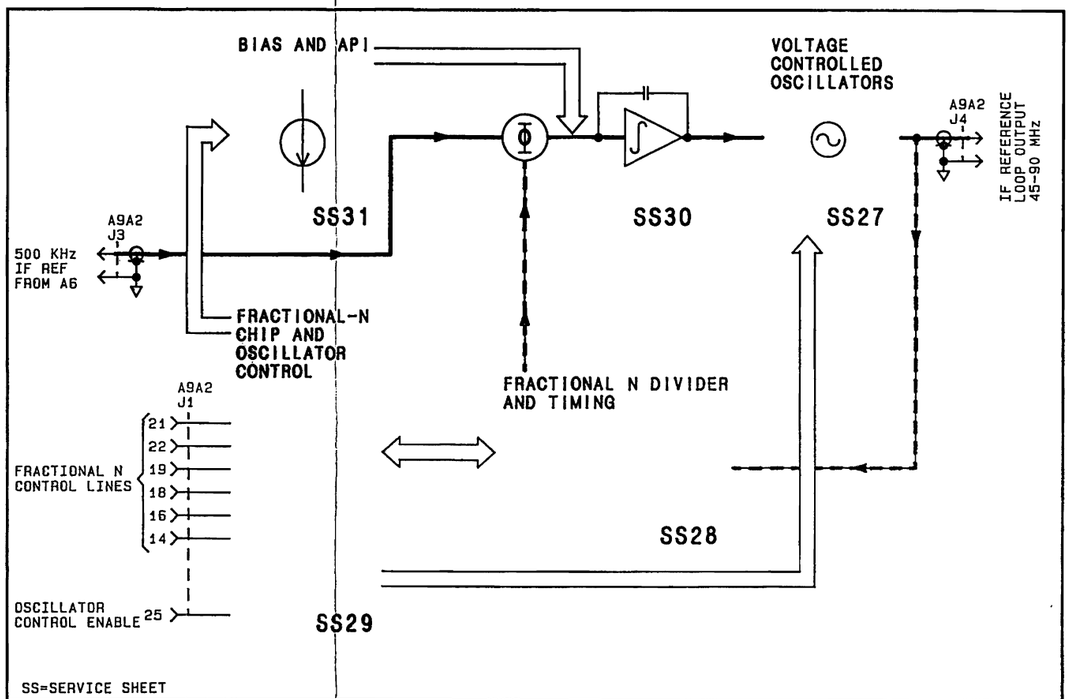
Figure 8M-108. SERVICE SHEET 30 INFORMATION

Component Locator



A9A2

Component Locator



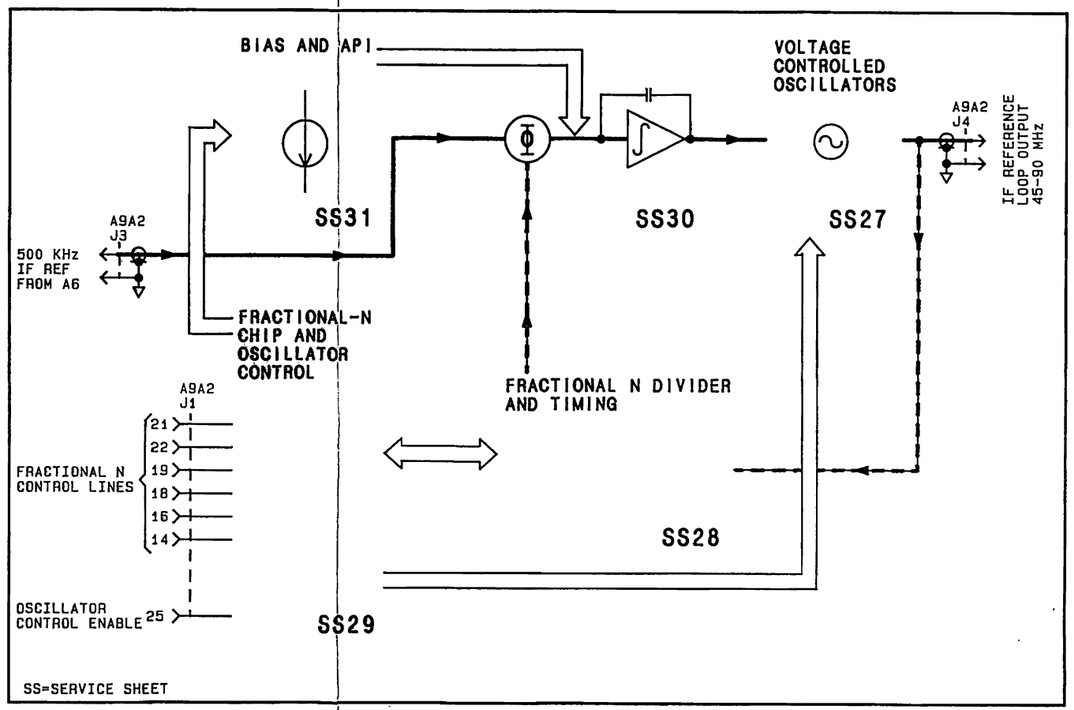
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C45	C, 2	DS1	C, 1	R33	D, 1	R108	C, 2								
C46	C, 1			R34	C, 1	R109	C, 2								
C47	C, 1	FL1	A, 1	R35	C, 1	R110	C, 2								
C48	D, 1			R36	C, 2	R111	C, 2								
C49	C, 1	J3	D, 1	R37	C, 2	R112	C, 2								
C50	C, 1	J4	D, 1	R38	C, 2	R113	C, 2								
C51	C, 1			R39	C, 2	R114	C, 2								
C52	C, 1	L11	C, 1	R40	C, 2	R115	C, 2								
C53	C, 1	L12	C, 1	R41	C, 1	R116	C, 2								
C54	C, 2	L13	C, 1	R42	C, 1	R117	C, 2								
C55	D, 2			R43	C, 1	R118	D, 2								
C56	C, 2	Q12	C, 1	R44	C, 1	R119	D, 2								
C73	D, 2	Q13	D, 1	R45	C, 2	R120	D, 1								
C74	D, 2	Q14	D, 1	R46	C, 1	R121	D, 1								
C75	D, 2	Q15	D, 2	R47	C, 2										
C76	D, 2	Q16	C, 2	R48	C, 1	TP14	C, 1								
C77	D, 2	Q17	C, 2	R49	C, 2	TP15	C, 1								
C78	D, 2	Q18	C, 2	R50	C, 1	TP16	C, 1								
C79	D, 2	Q19	C, 2	R51	C, 2	TP17	D, 2								
C80	C, 2	Q20	C, 2	R52	C, 1	TP18	C, 2								
C81	D, 2	Q21	C, 2	R53	C, 2	TP19	D, 2								
C82	D, 2	Q22	C, 2	R54	C, 2	TP20	D, 2								
C83	D, 2	Q23	D, 2	R55	C, 2	TP21	D, 2								
C84	D, 2	Q24	D, 2	R56	D, 2	TP22	C, 2								
		Q25	C, 2	R57	D, 2	TP23	D, 2								
CR1	D, 3	Q27	C, 2	R58	C, 2										
CR2	D, 2			R59	D, 3	U29	D, 1								
CR3	D, 2			R98	D, 2	U30	D, 1								
CR4	D, 2			R99	D, 2	U31	C, 2								
CR5	D, 2			R100	D, 2	U32	D, 2								
CR6	D, 3			R101	D, 2	U33	D, 2								
CR7	D, 2			R102	D, 2										
CR8	D, 2			R103	D, 2	VR4	C, 2								
				R104	D, 1										
				R105	C, 2										
				R106	C, 2										
				R107	C, 2										

SEE REVERSE SIDE

P/O A9A2 FRACTIONAL-N ASSEMBLY **SS29**



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C45	C, 2	DS1	C, 1	R33	D, 1	R108	C, 2								
C46	C, 1			R34	C, 1	R109	C, 2								
C47	C, 1	FL1	A, 1	R35	C, 1	R110	C, 2								
C48	D, 1			R36	C, 2	R111	C, 2								
C49	C, 1	J3	D, 1	R37	C, 2	R112	C, 2								
C50	C, 1	J4	D, 1	R38	C, 2	R113	C, 2								
C51	C, 1			R39	C, 2	R114	C, 2								
C52	C, 1	L11	C, 1	R40	C, 2	R115	C, 2								
C53	C, 1	L12	C, 1	R41	C, 1	R116	C, 2								
C54	C, 2	L13	C, 1	R42	C, 1	R117	C, 2								
C55	D, 2			R43	C, 1	R118	D, 2								
C56	C, 2	Q12	C, 1	R44	C, 1	R119	D, 2								
C73	D, 2	Q13	D, 1	R45	C, 2	R120	D, 1								
C74	D, 2	Q14	D, 1	R46	C, 1	R121	D, 1								
C75	D, 2	Q15	D, 2	R47	C, 2										
C76	D, 2	Q16	C, 2	R48	C, 1	TP14	C, 1								
C77	D, 2	Q17	C, 2	R49	C, 2	TP15	C, 1								
C78	D, 2	Q18	C, 2	R50	C, 1	TP16	C, 1								
C79	D, 2	Q19	C, 2	R51	C, 2	TP17	D, 2								
C80	C, 2	Q20	C, 2	R52	C, 1	TP18	C, 2								
C81	D, 2	Q21	C, 2	R53	C, 2	TP19	D, 2								
C82	D, 2	Q22	C, 2	R54	C, 2	TP20	D, 2								
C83	D, 2	Q23	D, 2	R55	C, 2	TP21	D, 2								
C84	D, 2	Q24	D, 2	R56	D, 2	TP22	C, 2								
		Q25	C, 2	R57	D, 2	TP23	D, 2								
CR1	D, 3	Q27	C, 2	R58	C, 2										
CR2	D, 2			R59	D, 3	U29	D, 1								
CR3	D, 2			R98	D, 2	U30	D, 1								
CR4	D, 2			R99	D, 2	U31	C, 2								
CR5	D, 2			R100	D, 2	U32	D, 2								
CR6	D, 3			R101	D, 2	U33	D, 2								
CR7	D, 2			R102	D, 2										
CR8	D, 2			R103	D, 2	VR4	C, 2								
				R104	D, 1										
				R105	C, 2										
				R106	C, 2										
				R107	C, 2										

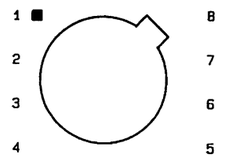
P/O A9A2 FRACTIONAL-N ASSEMBLY **SS29**

SEE REVERSE SIDE

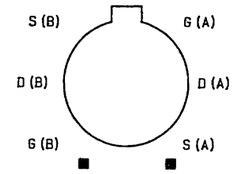
Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

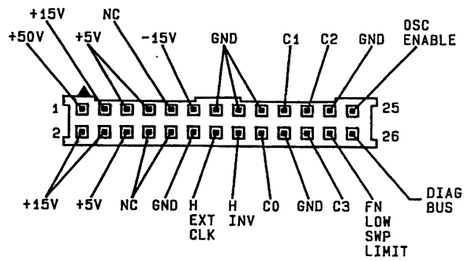
A9A2 U33 TOP VIEW



A9A2 Q14A,B TOP VIEW



CABLE PLUG TO A9A2 J1



Schematic General Information

FN LOOP DIVIDE N.F
PULSE SHAPER
TTL TO ECL TRANSLATOR
FN LOOP IF 28 BX
VCO ÷NF
TP14
R40 51.1
Q12
+5V (F3)
C51 56p
R41 75
C52 56p
R43 681
TP18
R42 56.2
R44 1330
R45 46.4

PHASE DETECTOR
U31A
+5V (F3)
C53 0.01µ
R47 46.4
R46 464
R49 46.4
R48 464

SWITCH DRIVERS
CURRENT SOURCE SWITCH
+15V (F3)
C54 10 µ
R54 825
Q21
Q22
+5V (F3)
C55 33 µ
Q24
TP21
R55 196
CR1
CR2
R57 23.7
Q15
R56 5110
-15V (F3)
-15V (F3)

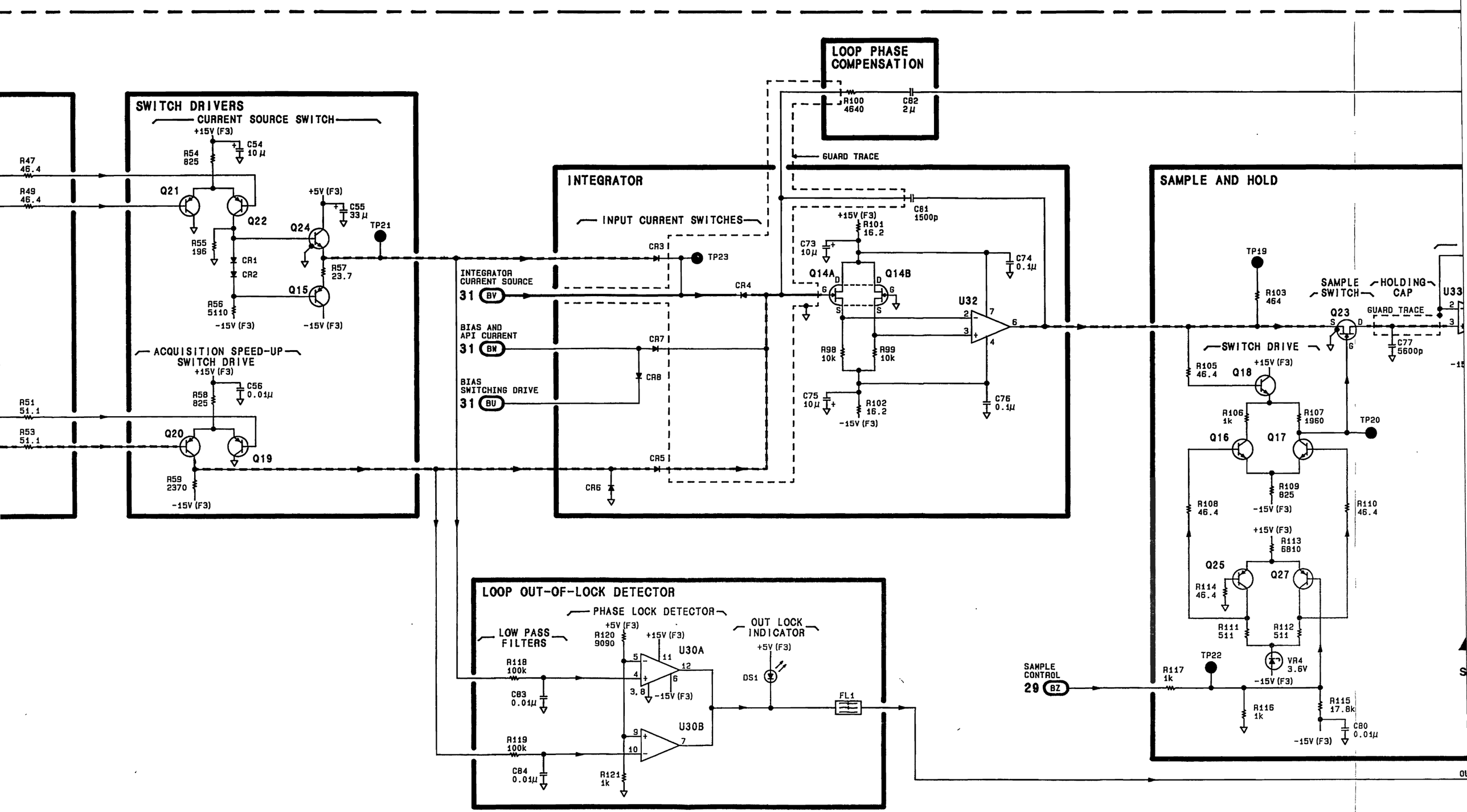
REFERENCE SIGNAL
DIVIDE BY 5
+5V (F3)
R33 10k
U29 CTR
C48 0.1µ
CT=0
500 kHz IF REFERENCE 22 BB
W26
J3
TTL TO ECL TRANSLATOR
TP15
R34 100
Q13
C49 56p
R35 75
C50 56p
R37 681
TP16
R36 56.2
R38 1330
R39 46.4

U31B
R51 51.1
R50 464
R53 51.1
R52 464

ACQUISITION SPEED-UP SWITCH DRIVE
+15V (F3)
C56 0.01µ
R58 825
Q20
Q19
R59 2370
-15V (F3)

POWER SUPPLIES AND GND
POWER SUPPLY AND GND 28 BY
+15V (F1)
L11 27µ
C45 10 µ
+15V (F3)
+5V (F1)
L12 27µ
C46 33 µ
+5V (F3)
-15V (F1)
L13 27µ
C47 10 µ
-15V (F3)
GND
POWER SUPPLY AND GND BT 31

SERIAL PREFIX: 2427A



LOOP PHASE COMPENSATION
R100 4640
C82 2µ

GUARD TRACE

INTEGRATOR
INPUT CURRENT SWITCHES
INTEGRATOR CURRENT SOURCE 31 BV
BIAS AND API CURRENT 31 BW
BIAS SWITCHING DRIVE 31 BU
CR3
CR4
CR5
CR6
CR7
CR8
TP23
+15V (F3)
R101 16.2
C81 1500p
C73 10µ
C74 0.1µ
Q14A
Q14B
U32
R98 10k
R99 10k
C75 10µ
R102 16.2
-15V (F3)
C76 0.1µ

SAMPLE AND HOLD
TP19
R103 464
SAMPLE SWITCH
HOLDING CAP
Q23
GUARD TRACE
C77 5600p
BUFFER
U33
+15V (F3)
C78 0.01µ
-15V (F3)
C79 0.01µ
TP17
R104 21.5k
J4
A9W1
VCO TUNE VOLTAGE
847
BK 27
SWITCH DRIVE
R105 46.4
Q18
+15V (F3)
R106 1k
R107 1960
TP20
Q16
Q17
R109 825
R108 46.4
-15V (F3)
R110 46.4
+15V (F3)
R113 6810
Q25
Q27
R114 46.4
R111 511
R112 511
TP22
VR4 3.6V
-15V (F3)
SAMPLE CONTROL 29 BZ
R117 1k
R116 1k
R115 17.8k
C80 0.01µ
-15V (F3)

ATTENTION
Static Sensitive Devices

LOOP OUT-OF-LOCK DETECTOR
PHASE LOCK DETECTOR
LOW PASS FILTERS
OUT LOCK INDICATOR
+5V (F3)
R120 9090
+15V (F3)
U30A
R118 100k
C83 0.01µ
-15V (F3)
DS1
FL1
U30B
R119 100k
C84 0.01µ
R121 1k

OUT-OF-LOCK SENSE
J1
26
P/O A5 DISTRIBUTION ASSY SS66
IF REFERENCE DIAGNOSTIC BUS
JN 9

SS30
Figure 8M-109
8M-109

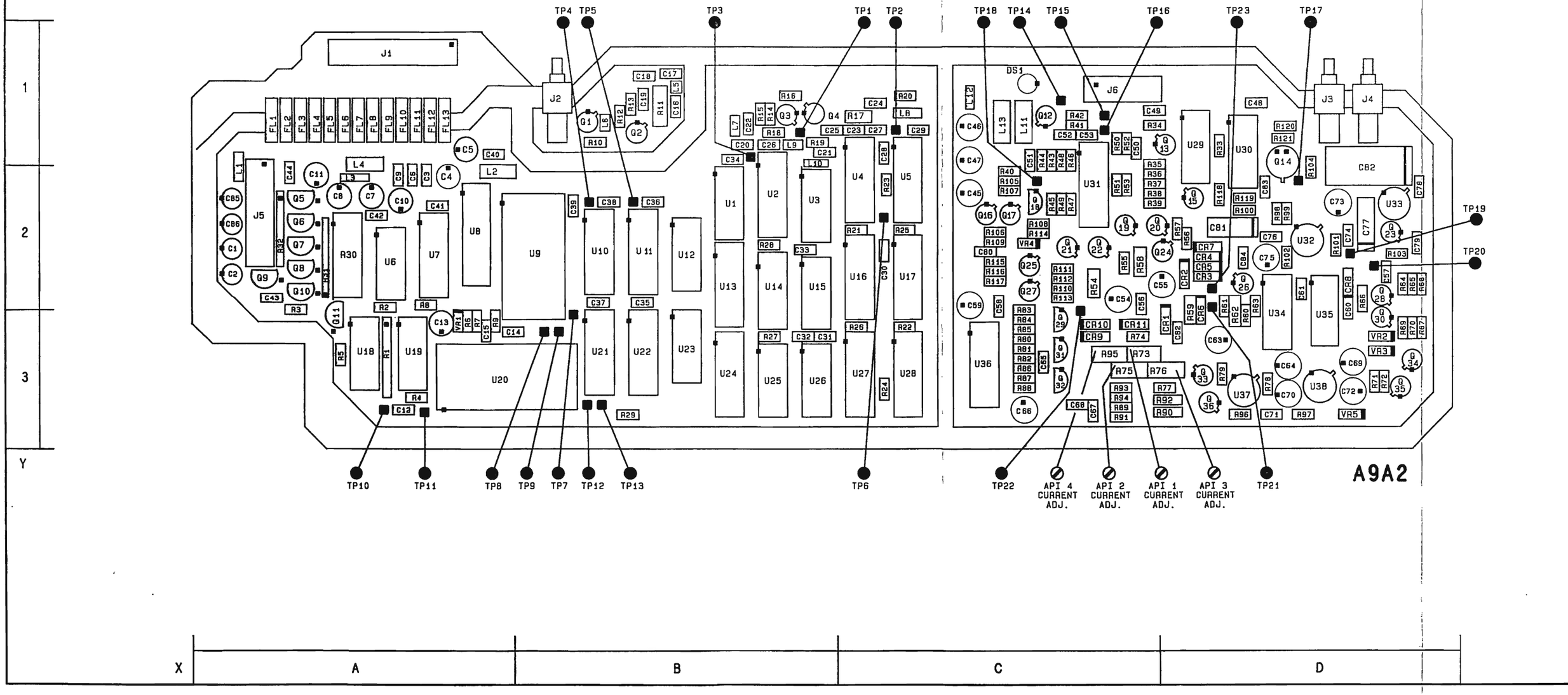
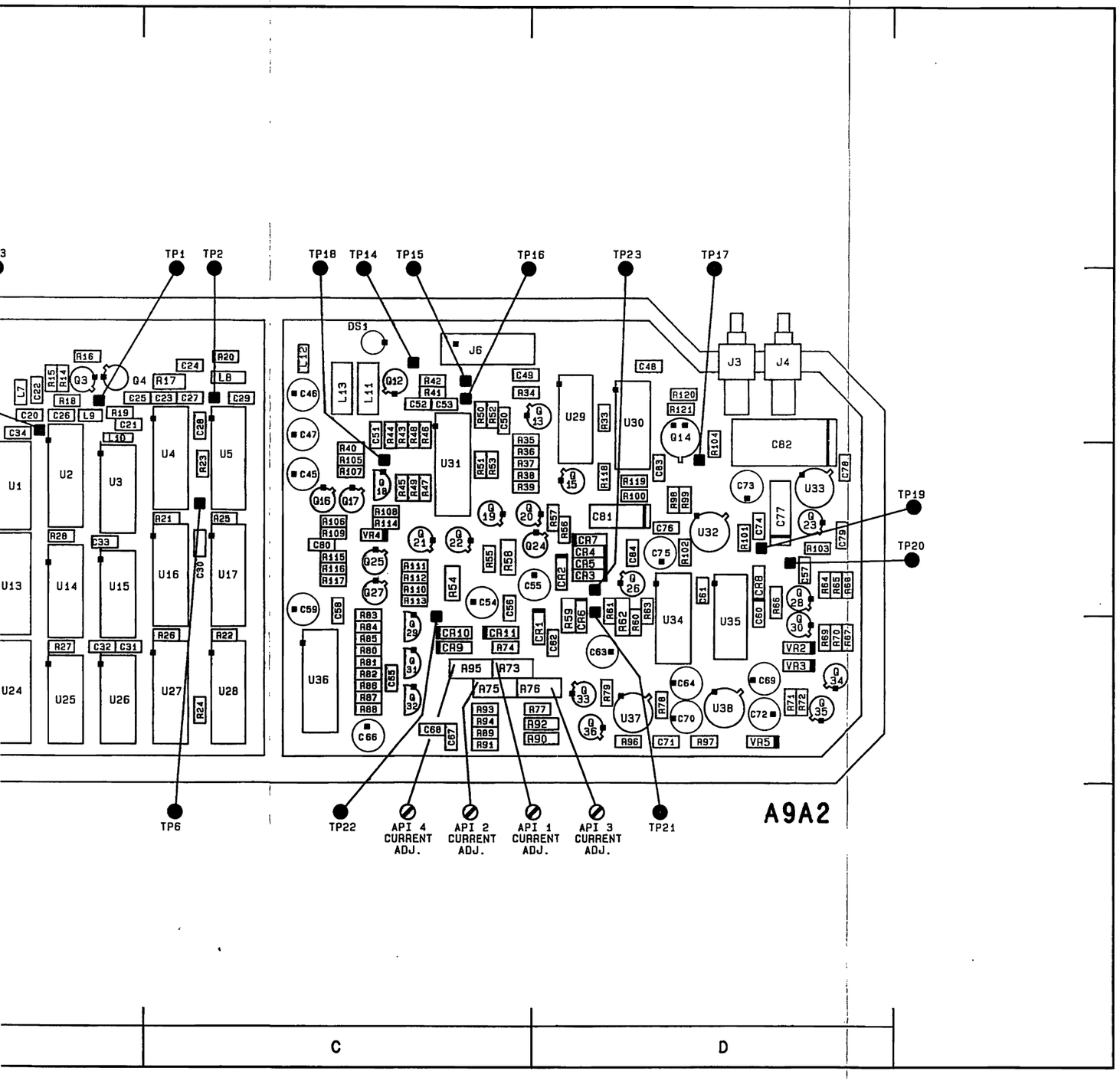


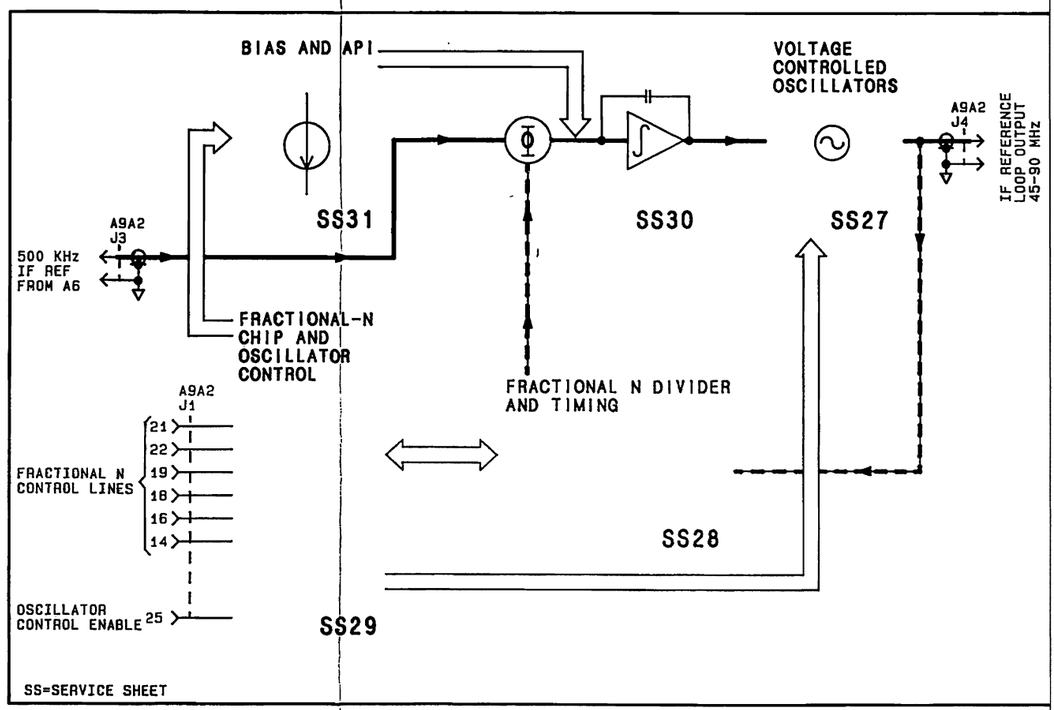
Figure 8M-110. SERVICE SHEET 31 INFORMATION

Component Locator



A9A2

Component Locator



Reference Block Diagram

Component Coordinates

COMP	X,Y
C57	D, 2
C58	C, 2
C59	C, 2
C60	D, 3
C61	D, 2
C62	D, 3
C63	D, 3
C64	D, 3
C65	C, 3
C66	C, 3
C67	C, 3
C68	C, 3
C69	D, 3
C70	D, 3
C71	D, 3
C72	D, 3
CR9	C, 3
CR10	C, 3
CR11	C, 3
Q26	D, 2
Q28	D, 2
Q29	C, 3
Q30	D, 3
Q31	C, 3
Q32	C, 3
Q33	D, 3
Q34	D, 3
Q35	D, 3
Q36	D, 3

COMP	X,Y
R60	D, 3
R61	D, 2
R62	D, 3
R63	D, 2
R64	D, 2
R65	D, 2
R66	D, 2
R67	D, 3
R68	D, 2
R69	D, 3
R70	D, 3
R71	D, 3
R72	D, 3
R73	C, 3
R74	C, 3
R75	C, 3
R76	D, 3
R77	D, 3
R78	D, 3
R79	D, 3
R80	C, 3
R81	C, 3
R82	C, 3
R83	C, 2
R84	C, 3
R85	C, 3
R86	C, 3
R87	C, 3
R88	C, 3
R89	C, 3
R90	D, 3
R91	C, 3
R92	D, 3
R93	C, 3
R94	C, 3
R95	C, 3
R96	D, 3

COMP	X,Y
R97	D, 3
U34	D, 3
U35	D, 3
U36	C, 3
U37	D, 3
U38	D, 3
VR2	D, 3
VR3	D, 3
VR5	D, 3

COMP	X,Y

COMP	X,Y

COMP	X,Y

COMP	X,Y

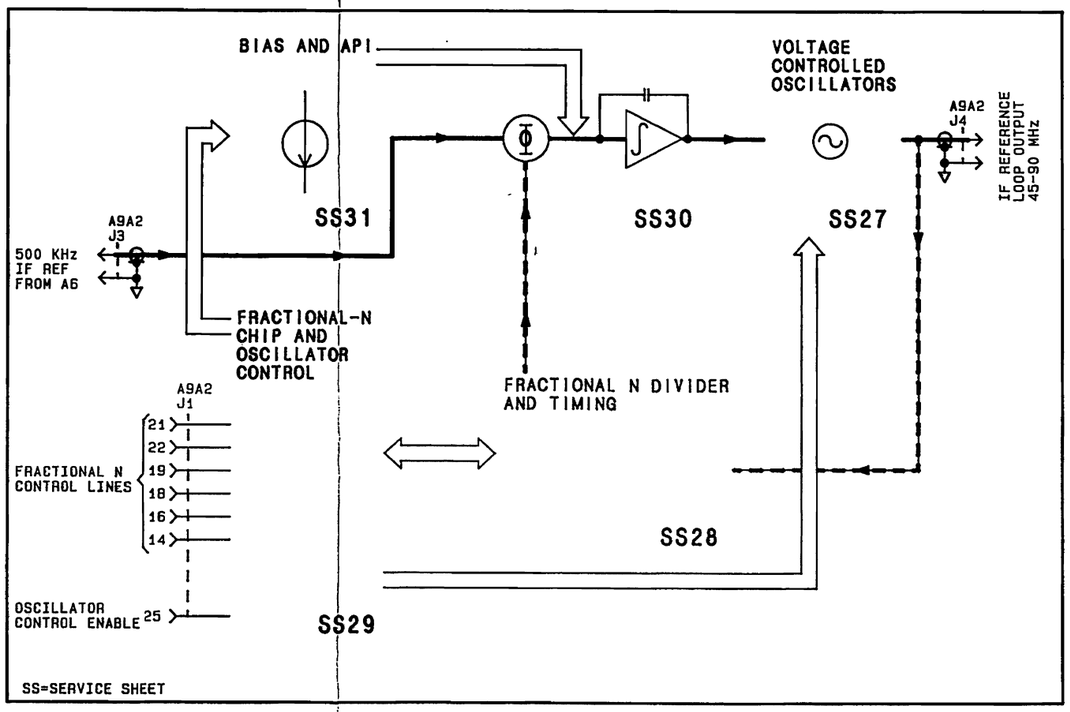
COMP	X,Y

COMP	X,Y

P/O A9A2 FRACTIONAL-N ASSEMBLY

SS30

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y
C57	D, 2
C58	C, 2
C59	C, 2
C60	D, 3
C61	D, 2
C62	D, 3
C63	D, 3
C64	D, 3
C65	C, 3
C66	C, 3
C67	C, 3
C68	C, 3
C69	D, 3
C70	D, 3
C71	D, 3
C72	D, 3
CR9	C, 3
CR10	C, 3
CR11	C, 3
Q26	D, 2
Q28	D, 2
Q29	C, 3
Q30	D, 3
Q31	C, 3
Q32	C, 3
Q33	D, 3
Q34	D, 3
Q35	D, 3
Q36	D, 3

COMP	X,Y
R60	D, 3
R61	D, 2
R62	D, 3
R63	D, 2
R64	D, 2
R65	D, 2
R66	D, 2
R67	D, 3
R68	D, 2
R69	D, 3
R70	D, 3
R71	D, 3
R72	D, 3
R73	C, 3
R74	C, 3
R75	C, 3
R76	D, 3
R77	D, 3
R78	D, 3
R79	D, 3
R80	C, 3
R81	C, 3
R82	C, 3
R83	C, 2
R84	C, 3
R85	C, 3
R86	C, 3
R87	C, 3
R88	C, 3
R89	C, 3
R90	D, 3
R91	C, 3
R92	D, 3
R93	C, 3
R94	C, 3
R95	C, 3
R96	D, 3

COMP	X,Y
R97	D, 3
U34	D, 3
U35	D, 3
U36	C, 3
U37	D, 3
U38	D, 3
VR2	D, 3
VR3	D, 3
VR5	D, 3

COMP	X,Y

COMP	X,Y

COMP	X,Y

COMP	X,Y

COMP	X,Y

COMP	X,Y

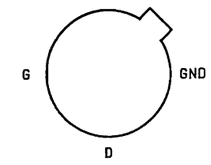
P/O A9A2 FRACTIONAL-N ASSEMBLY **SS30**

SEE REVERSE SIDE

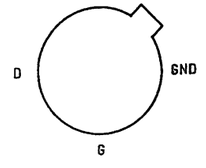
Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

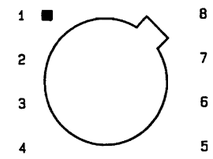
A9A2 Q33,Q36 TOP VIEW



A9A2 Q34,Q35 TOP VIEW



A9A2 U37,U38 TOP VIEW



P/O A9A2 FRACTIONAL-N ASSEMBLY (08642-60105)

BIAS AND API CONTROL LATCH

+5V (F3)

C59 33µ

C58 0.01µ

+5V (F3)

U36

LATCH CLK 29 CW

BIAS AND API ENABLE 29 BR 6

API 2 3 1D 2 A2

API 3 4 5 A3

BIAS 6 7

API 4 11 10 A4

API 5 13 12 A5

API 1 14 15 A1

DELAYED BIAS CD 29

BIAS SWITCH DRIVE

TTL TO ECL

+15V (F3)

R61 681

R62 1470

R60 1780

+5V (F3)

R63 46.4

Q26

SWITCH DRIVE

+15V (F3)

R66 3480

BIAS SWITCHING DRIVE BU 30

+15V (F3)

R67 7.5k

Q28

Q30

R68 619

R64 12.1k

R65 1780

C57 0.1µ

-15V (F3)

-15V (F3)

R69 5110

R70 5110

-15V (F3)

POWER SUPPLIES AND GND

POWER SUPPLY AND GND 30 BT 4

+15V (F3)

+5V (F3)

-15V (F3)

GND

API 1

SWITCH DRIVE

+15V (F3)

R82 3830

Q31

C65 0.1µ

R81 1k

R80 1960

SWITCH

G

S D

Q34

+5V (F3)

C62 0.1µ

CURRENT ADJ.

R73 50k

R74 10k

CR9

P/O U34

7

1, 3, 4, 5, 6, 12

+5V (F3)

C63 33µ

100

10k

API 1 CURRENT SOURCE

CURRENT SOURCE

Q35

S D

G

GUARD TRACE

INTEGRATOR CURRENT SOURCE BV 30

VR3 6.2V

API 2 CURRENT SOURCE

API 3 CURRENT SOURCE

U35

1 5 11 8

2

3 4 14 12 13 10 9 7 6

R71 681

R72 46.4

VR2 6.2V

C60 0.01µ

-15V (F3)

P/O U34

15 14 13

1150 2.3k 2.3k

16

C61 0.1µ

-15V (F3)

SERIAL PREFIX: 2427A

A2 3 A3 2 A4 A5

SWITCH DRIVE
+15V (F3)
R82 3830
Q31
C65 0.1µ
C62 0.1µ
+5V (F3)
R73 50k
CURRENT ADJ.
R74 10k
CR9
SWITCH
G S T D
Q34
P/O U34
1, 3, 4, 5, 6, 12
7
100
10k
+5V (F3)
C63 33 µ

API 2 SWITCH DRIVER
+15V (F3)
R85 3830
R84 1k
Q29
R83 1960
CURRENT ADJ.
R75 1k
CR10
P/O U34
8
11
50k
100

API 3 SWITCH DRIVER
+15V (F3)
+15V (F3)
R88 3830
R87 1k
Q32
C66 10 µ
R86 1960
CR11
CURRENT ADJ.
R76 50k
P/O U34
10
9
100
500k
2

API 4
+15V (F3)
C68 0.1µ
R93 5620
R94 1960
R95 50
CURRENT ADJ.
R92 909k
+5V (F3)

API 5
+5V (F3)
C67 0.1µ
R91 100
R89 10k
R90 10M

BIAS AND CURRENT

API 1 CURRENT SOURCE

GUARD TRACE

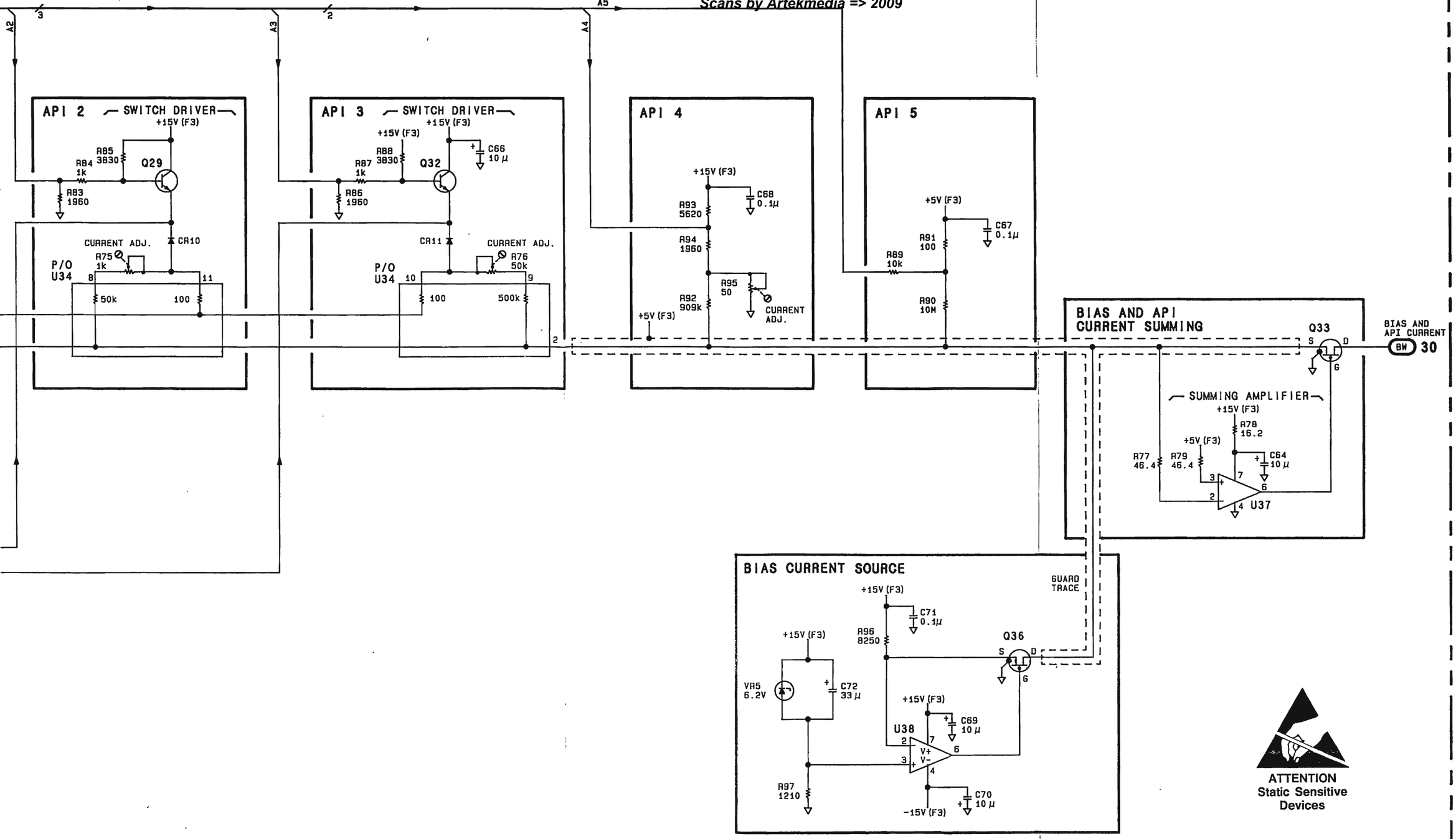
INTEGRATOR CURRENT SOURCE
BV 30

API 2 CURRENT SOURCE

API 3 CURRENT SOURCE

11 8
R71 681
13 10 9 7 6
R72 46.4
C60 0.01µ
-15V (F3)
VR2 6.2V
14 13
2.3k 2.3k
C61 0.1µ
15V (F3)

BIAS CURRENT SOURCE
GUARD TRACE
+15V (F3)
C71 0.1µ
R96 8250
Q36
S D
6
+15V (F3)
VR5 6.2V
C72 33 µ
+15V (F3)
C69 10 µ
U38
2
7
V+
V-
6
3
4
R97 1210
C70 10 µ
-15V (F3)



ATTENTION
Static Sensitive
Devices

SS31
Figure 8M-111
8M-111

A11 Module

Troubleshooting and Adjustments Contents

Troubleshooting

Adjustments

Troubleshooting

A11 MODULE TROUBLESHOOTING INFORMATION

Before Proceeding With Module Troubleshooting

- You should have confidence that A11 is the faulty module from Module Level Diagnostics (MLD) results. (Refer to Instrument Level Troubleshooting, HP 8642 On Site Service Manual).
- Open the HP 8642 manual to the foldout on page 8N-100. There are 3 diagrams of the A11 Module (Reference Loop). One diagram is titled Simplified Block Diagram. It is a block diagram intended to be used to understand the basic operation of A11. (There is a brief discussion of the circuit operation on this page).
- Open the next foldout on page 8N-101 (BD11). There, you will see a more detailed Block Diagram of the reference loop. **This Troubleshooting Block Diagram is meant to be used during Checks 1 through 4.** Assemblies A11A1, A11A2, and A11A3 are represented on four Service Sheets (SS32-35).
- The objective of Troubleshooting Checks is to isolate the malfunction to an area of circuitry represented on one Service Sheet. The Checks are intended to be done in the order they are numbered.
- Once the malfunction is isolated, refer to the Component Level Repair Directory. There, you will find tables that contain information useful for locating faulty components.
- Specification failures (for example, phase noise, spurs, etc.) might not be found by Troubleshooting Checks. Manual Adjustments and Auto Adjust Procedures can be done, and the HP 8642 then re-tested to see if the specific failure condition still exists. At this point, if repair is necessary, Module Performance Checks may be helpful to pinpoint a failure condition in the module.

Overall Equipment List

Signal Generator No. 1	135 MHz, +2.5 dBm
Signal Generator No. 2	HP8642B
Oscilloscope	HP1980B
Digital Voltmeter(DVM)	HP3456A
Measuring Receiver	HP 8902A
Spectrum Analyzer	HP8566A/B
HP 8642 Bench Service Kit	HP 11802A
Sensor Module	HP 11722A

Essentials of A11 Module Operation

Refer to the Simplified Block Diagram on page 8N-100. The A11 Module contains a phase locked loop which combines the FM Loop Output signal (from A6) with the SAWR Oscillator Output signal (from A7) to produce one of six output frequencies shown at the A11 output. This output goes to the Sum Loop/Divider Module (A12). The FM Loop Output signal, 135 MHz + Angle Mod, carries the internal phase and frequency modulation of the instrument. The SAWR Oscillator Output is one of three highly stable UHF reference frequencies.

In the center of the Simplified Block Diagram, notice that there are two voltage controlled oscillators (VCO's) on SS34. Each VCO generates one of three frequencies, for a total of six frequencies in two bands. This signal is amplified and output through A11A3 J2 to the Sum Loop/Divider Module (A12).

CHECK 1: A11A1 ANALOG CIRCUITRY (SS32)

Essentials of SS32 Circuit Operation

Refer to BD11. Located on the A11A1 board is an input port for the FM Loop Output signal (from the A6 module). It is A11A1 J3. There is also an input port for the Ref Loop IF, which is the main feedback signal in the Reference Loop. It is A11A1 J2. These signals are amplified and sent to a mixer functioning as a **PHASE DETECTOR**. The **PHASE DETECTOR** outputs an error signal at Z1 (pins 3 and 4) which is filtered, then directed through **DIPLEXERS** and an **INTEGRATOR**. After being integrated, the error signal is buffered (in the **LOOP EMITTER FOLLOWER**), shaped, and output at A11A1 J4 to A11A2 as the Ref Loop Tune Voltage.

If the loop is not phase locked, the integrator is forced to sweep in an attempt to achieve lock (referred to as sweep-to-lock). If switch A11A1 S1 (shown on SS32) is in its OPEN (open loop) position,the sweep to lock is discontinued and the integrator output is held at approximately half its maximum value.

NOTE

Use the Module Test Point/Adjustment Locations diagram on the foldout opposite the Block Diagram (BD) to locate test points. Test point designators ((XX)) will be used in text whenever applicable.

Description of Check 1

The largest board in the A11 module is the A11A1 Reference Loop Phase Detector and Integrator (see top board shown on Module Test Point/Adjustment Locations on page 8N-100).

This is a check of the A11A1 analog circuitry, and is intended to identify failures that would lead you to SS32 for component repair. First, you will test the **POWER SUPPLY** lines. Then, you will substitute signals at the two RF inputs to the board, and verify the output waveform with an Oscilloscope to check for correct **PHASE DETECTOR** and **INTEGRATOR** operation. The **SHAPER** and four diagnostic sense points are also tested.

If a test fails, refer to Component Level Repair Directory.

Required Equipment:

Signal Generator No. 1*	135 MHz, +2.5 dBm
Signal Generator No. 2	HP8642B
Oscilloscope	HP1980B
Digital Voltmeter (DVM)	HP3456A

*The FM Loop Output on *W24* can be used if A6 module is known to be good.

Test the A11 Power Supply and Ground

1. Setup:

   Switch the HP 8642 to standby (STBY).

   Extend module on extender posts (refer to the Disassembly Procedure if you are not familiar with this procedure).

   Remove the A11A1 cover (See the Assembly Locator on the foldout opposite BD11 for location of A11A1 cover).

   Switch the HP 8642 on.

2. Measure Voltage Levels:

   Check the **POWER SUPPLY AND GND** line voltages at the filters given in Table 8N-1. Filter locations can be found in the upper right corner of the A11A1 assembly. See the component locator on the back side of BD11. Measurements can be made on either side of filter.

Table 8N-1. *A11 Power Supply Lines*

Filter	Nominal Voltage
A11A1 FL7	+50V ± 100 mV
A11A1 FL6	+15V ± 30 mV
A11A1 FL8	+5.2V ±10 mV
A11A1 FL4	−15V ± 30 mV

Test the Phase Detector and Integrator

3. Setup:

   Switch the HP 8642 to Standby.

   Set Signal Generator No. 1 to 135 MHz and 2.5 dBm. (The FM Loop Output on *W24* can be used if A6 is known to be good). Connect its output to A11A1 J3 (CU) (FM loop output is already connected to A11A1 J3).

   Set Signal Generator No. 2 to 135.1 MHz and −10 dBm. Connect its output to A11A1 J2 (DL) .

   Lock the timebases of Signal Generator No. 1 and Signal Generator No. 2 together.

   Disconnect A11W2 from A11A2 J1 (DE) and connect A11W2 to the Oscilloscope input.

4. Verify Waveforms:

   Switch the HP 8642 on.

   Adjust the scope (DC coupled) so that the display appears similar to the Sweep to Lock Signal (Figure 8N-1). The amplitude should be 3 to 9 V_{pp}, 4 ms period.

   Adjust the scope so that the display appears similar to Figure 8N-2. This is a 100 kHz beat note superimposed on the Sweep-to-Lock Signal. Its amplitude should be 0.5 to 1.5 V_{pp}, μs period.

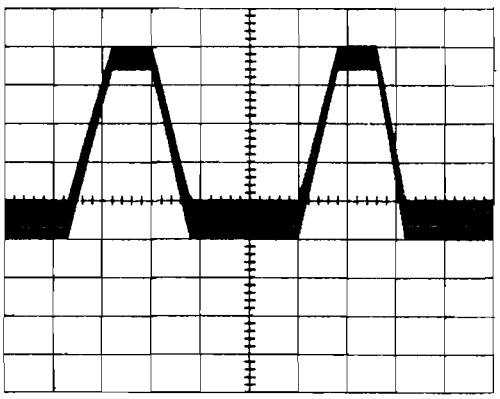


Figure 8N–1. *Integrator Sweep to lock Signal (3-9 V_{pp} and ≈ 4.0 ms period.)*

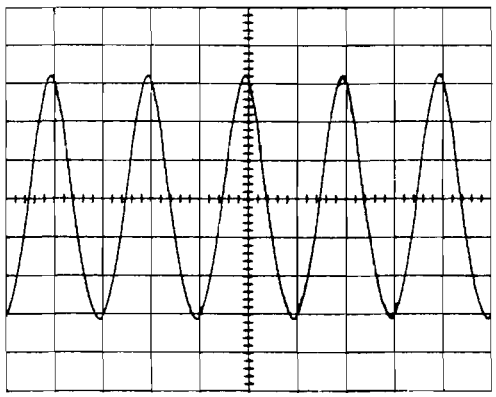


Figure 8N–2. *100 KHz Difference Signal (0.5 to 1.5 V_{pp} 10 µs period.)*

Test the Shaper DAC

5. Setup:

   Remove Signal Generator No. 2 from A11A1 J2 (DL) . Leave A11 W1 disconnected.

   Set A11A1 S1 (see Component Locator on page 8N-102 for S1 location) to open loop (OPEN) position. This halts the loop sweep-to-lock action.

6. Measure Voltage Levels at Shaper DAC input lines:

   Key in [SHIFT] [SPCL] [3], to enter Service Mode, then key in the Service Functions from Table 8N-2. Use the DVM to measure TTL levels at AllA1 U1A pin numbers shown in Table 8N-2. (A11A1 U1A's location can be found on the Component Locator diagram on page 8N-102)

Table 8N–2. *Shaper DAC Input Lines*

Service Function	DVM Measurement at A11A1 U1 Pin #					
	11 (SB0)	9 (SB1)	5 (SB2)	3 (SB3)	13 (SB4)	1 (SB5)
6 3 1 0 HZ (All Off)	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc
6 3 1 1 HZ	≈5 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc
6 3 1 2 HZ	≈0 Vdc	≈5 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc
6 3 1 4 HZ	≈0 Vdc	≈0 Vdc	≈5 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc
6 3 1 8 HZ	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈5 Vdc	≈0 Vdc	≈0 Vdc
6 3 1 16 HZ	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈5 Vdc	≈0 Vdc
6 3 1 32 HZ	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈5 Vdc
6 3 1 63 HZ (All On)	≈5 Vdc	≈5 Vdc	≈5 Vdc	≈5 Vdc	≈5 Vdc	≈5 Vdc

7. Measure Voltage Levels at Output Line:

   Disconnect A11W2 from Oscilloscope input. Connect A11W2 to DVM input.

   Key in SHIFT SPCL 3 to enter Service Mode. Key in the Service Functions from Table 8N-3. Record the DVM measurement for each service function in Table 8N-3 in the column labeled "DVM Measurement at A11W2". Determine the actual results as indicated in the "Actual" column.

Table 8N–3. *Shaper DAC Output Lines*

Service Function	DVM Measurement at A11W2	Limits		
		Min.	Actual	Max.
6 3 1 0 HZ	A= 1.50	1.33 Vdc	A= 1.5	1.57 Vdc
6 3 1 1 HZ	B= 1.617	15 mVdc	B-A= 17 mV	21 mVdc
6 3 1 2 HZ	C= 1.535	15 mVdc	C-B= 18 mV	21 mVdc
6 3 1 4 HZ	D= 1.572	32 mVdc	D-C= 37 mV	44 mVdc
6 3 1 8 HZ	E= 1.658	68 mVdc	E-D= 78 mV	93 mVdc
6 3 1 16 HZ	F= 1.829	155 mVdc	F-E= 179 mV	211 mVdc
6 3 1 32 HZ	G= 2.311 ↑	421 mVdc	G-F= 482 mV	571 mVdc
6 3 1 63 HZ	H= 5.490 ↓	5.1 Vdc	H= 5.490 V	5.7 Vdc

Test the Diagnostic Circuitry

8. Setup:

   Switch the HP 8642 to standby.

   Disconnect A11W2 from DVM input. Reconnect A11W2 to A11A2 J1 (DE)

   Set A11A1 S1 to CLOSED position.

   Connect an Oscilloscope probe to A11A1 TP4 (Located at top of A11A1 board next to J1).

   Switch the HP 8642 to on.

9. Verify Waveforms at Sense Lines: Key in [SHIFT] [SPCL] [3] [2] to enter Service Mode and internal voltmeter measurements. Key Service Function's from Table 8N-4. Verify that the Oscilloscope display matches the figure indicated in Table 8N-4. The 8642 display will indicate a voltage measurement disregard this during this check.

NOTE

The Diagnostic Sense Lines are measured at A11A1 TP4 (the output of the **REFERENCE LOOP DIAGNOSTICS** *on SS33) for convenience. If the signal doesn't match the figure, observe the signal at its source (refer to Table 8N-4). This will determine if the fault is located on SS32 or SS33.*

Table 8N-4. *Diagnostic Sense Lines*

Service Function	Figure	Line Label	SS32 Signal Source
[1] [3] [HZ]	8N-3	Integrator Output Sense (DA)	A11A1U11 pin 11
[1] [6] [HZ]	8N-4	Comparator Output Sense (CY)	A11A1U11 pin 14
[1] [1] [HZ]	8N-5	Out-of-Lock Sense (CZ)	A11A1S1 pin 5
[1] [4] [HZ]	8N-6	Shaper Sense (ZZ)	A11A1 J4

Restore Module

10. Replace cables:

    Reconnect A11W1 to A11A1 J2.

    If Signal Generator No. 1 was an external signal source, disconnect it from A11A1 J3 (CU) , and reconnect W24.

11. Replace A11A1 cover (unless proceeding to Check 2).

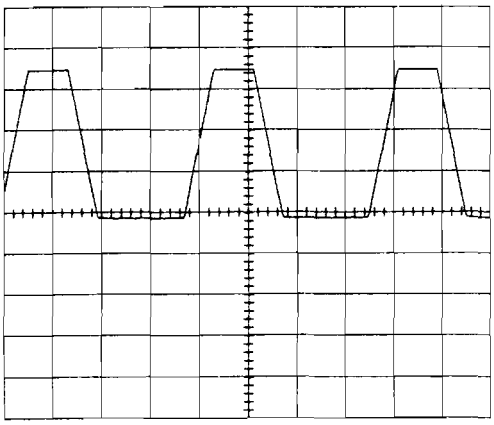


Figure 8N–3. *Integrator Output Sense Signal (4.0V/DIV 1.2mS/DIV)*

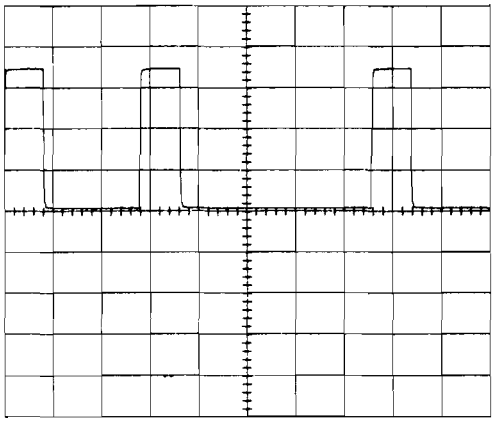


Figure 8N–4. *Comparator Output Sense Signal (1.5V/DIV 600 μS/DIV)*

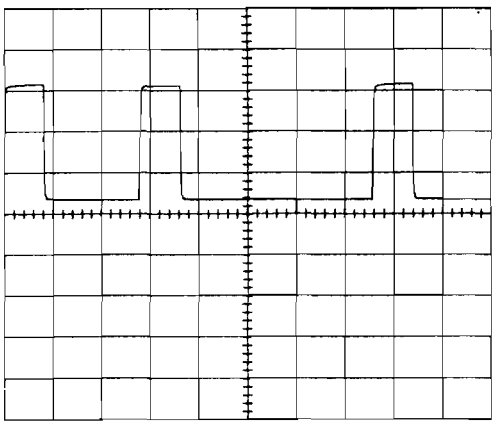


Figure 8N–5. *Out-of-Lock Sense (1.5V/DIV 600 μS/DIV)*

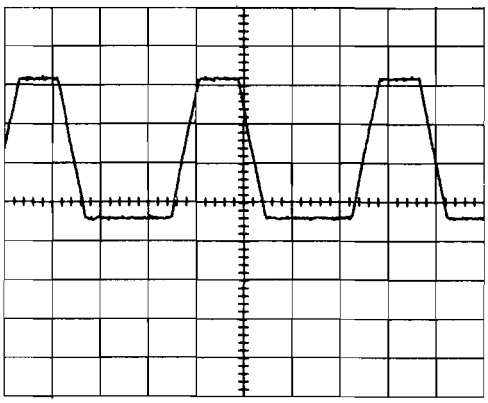


Figure 8N–6. *Shaper Sense Point (1.5V/DIV 1.2 mS/DIV)*

CHECK 2: A11A1 CONTROL CIRCUITRY (SS33)

Essentials of SS33 Circuit Operation

Refer to BD11. Serial data comes from the microprocessor to the Reference Loop Module and is received at J1 pins 12 and 14. Data is converted to a parallel bus in **SERIAL DATA INTERFACE** and sent to other functional blocks. The functional blocks labeled **REFERENCE LOOP OUTPUT LEVEL CONTROL** and **PRETUNE** perform control functions through Digital to Analog Converters (DACs).

Description of Check 2

This check tests the control circuitry for the A11 module (see Service Sheet 33). The A11 control circuitry is located on A11A1. By keying in [SHIFT] [SPCL] [3] in Tables 8N-5, 6, and 7, you will enter the HP 8642 Service Mode.

You will use the DVM to verify the output level of each DAC as different bit numbers are input. Then, you will calculate the output level change from data number to data number. If a test fails during Check 2, refer to Component Level Repair Directory.

Required Equipment:

Oscilloscope HP1980B
Digital Voltmeter (DVM) HP3456A

Test the Serial Data Interface

1. Setup:

   Swith the HP 8642 to standby(STBY).

   Extend A11 module on extender posts (refer to Disassembly Procedures if you are not familiar with the module extension).

   Remove the A11A1 cover (see the Assembly locator on the foldout opposite BD11 for location of A11A1 cover).

   Switch the HP 8642 on.

2. Measure TTL Levels:

   Key in Service Function 1 (SF1), use the oscilloscope to verify TTL levels listed in Table 8N-5 in the column labeled SF1. Then key in Service Function 2 (SF2), verify TTL levels listed in Table 8N-5 in the column labeled SF2.

   SF1 = [SHIFT] [SPCL] [360711184810] [Hz]

   SF2 = [SHIFT] [SPCL] [36075592405] [Hz]

Table 8N-5. REF Loop Control Lines

Line Label	A11A1 Ref.Des.	Bit No.	TTL Levels *	
			SF1	SF2
PTO	U6 Pin 16	0	L	H
PT1	U6 Pin 15	1	H	L
PT2	U6 Pin 6	2	L	H
PT3	U6 Pin 9	3	H	L
PT4	U6 Pin 12	4	L	H
PT5	U6 Pin 5	5	H	L
Band 1	U6 Pin 2	6	L	H
Band 2	U6 Pin 19	7	H	L
DAC0	U18 Pin5	8	L	H
DAC1	U18 Pin 15	9	H	L
DAC2	U18 Pin 12	10	L	H
DAC3	U18 Pin 9	11	H	L
DAC4	U18 Pin 6	12	L	H
DAC5	U18 Pin 16	13	H	L
DAC6	U18 Pin 19	14	L	H
SEL2	U18 Pin 2	15	H	L
SEL1	U2 Pin 2	16	L	H
SEL0	U2 Pin 5	17	H	L
SB0	U2 Pin 6	18	L	H
SB1	U2 Pin 9	19	H	L
SB2	U2 Pin 12	20	L	H
SB3	U2 Pin 15	21	H	L
SB4	U2 Pin 16	22	L	H
SB5	U2 Pin 19	23	H	L

* TTL High (H) 2.0 to 5.0 VDC
TTL Low (L) = 0.0 to 0.8 VDC

Test the Control DACs

3. Setup:

   Switch the HP 8642 to standby.

   On A11A1 set S1 to the open loop (OPEN) position. This halts sweep-to-lock action. Switch the HP 8642 on.

   Connect DVM at A11A1 TP4 (Top of A11A1 board next to ribbon connector J1).

4. Measure Voltage Levels (**REFERENCE LOOP OUTPUT LEVEL CONTROL** DAC):

   Key in: [SHIFT] [SPCL] [3] [2] [1] [7] [Hz] to enable measurement of **REFERENCE LOOP OUTPUT LEVEL CONTROL** DAC output at A11A1 TP4.

   Key in [SHIFT] [SPCL] [3] to enter Service Mode. Then key in the Service Functions listed in Table 8N-6. Record the DVM measurements in the column labeled "DVM Measurement", A11A1 TP4. Determine the actual results as indicated in the "Actual" column in Table 8N-6.

NOTE

The Reference Loop Output Level Control DAC output is prescaled before being multiplexed by A11A1U4. To calculate the actual output of the DAC (at Q4 emitter), multiply the measurement at A11A1 TP4 by 2.000.

Table 8N–6. *Reference Loop Output Level Control DAC*

Service Function	DVM Measurement A11A1 TP4	Limits		
		Min.	Actual	Max.
6 3 2 0 HZ	A= 5.635	5.5Vdc	A= 5.635	5.75 Vdc
6 3 2 1 HZ	B= 5.649	14 mVdc	B-A= 14 mV	18mVdc
6 3 2 2 HZ	C= 5.664	14 mVdc	C-B= 15 mV	18 mVdc
6 3 2 4 HZ	D= 5.693	28mVdc	D-C= 29 mV	35 mVdc
6 3 2 8 HZ	E= 5.752	55mVdc	E-D= 59 mV	68 mVdc
6 3 2 1 6 HZ	F= 5.869	110mVdc	F-E= 117 mV	135 mVdc
6 3 2 3 2 HZ	G= 6.104	220 mVdc	G-F= 235 mV	270 mVdc
6 3 2 6 4 HZ	H= 6.573	440mVdc	H-G= 469 mV	546 Vdc
6 3 2 1 2 7 HZ	I= 7.415	7.25Vdc	I= 7.415	7.5 Vdc

5. Measure Voltage Levels (**Pretune** DAC):

   Key in: SHIFT SPCL 3 2 1 2 Hz to enable measurement of the **PRETUNE** DAC output at A11A1 TP4.

   Key in SHIFT SPCL 3 to enter Service Mode. Then key in the Service Functions listed in Table 8N-7. Record the DVM measurements in the column labeled "DVM Measurements, A11A1 TP4". Determine the actual results as indicated in the "Actual" column in Table 8N-7.

NOTE

The Pretune DAC output is prescaled before being multiplexed by U4 (at pin 5). To Calculate the actual output of the DAC (at the Collector of Q10), multiply the measurement at A11A1 TP4 by 4.333.

Table 8N–7. *Pretune DAC*

Service Function	DVM Measurement A11A1 TP4	RESULTS Min.	Actual	Max.
6 3 0 0 HZ	A= 1.976	1.7 Vdc	A= 1.978	2.3 Vdc
6 3 0 1 HZ	B= 2.046	64 mVdc	B-A= 76 mV	89 mVdc
6 3 0 2 HZ	C= 2.124	64 mVdc	C-B= 78 mV	89 mVdc
6 3 0 4 HZ	D= 2.282	134 mVdc	D-C= 158 mV	183 mVdc
6 3 0 8 HZ	E= 2.617	282 mVdc	E-D= 395 mV	383 mVdc
6 3 0 1 6 HZ	F= 3.632	625 mVdc	F-E= (415 mV)	847 mVdc
6 3 0 3 2 HZ	G= 3.945	1.56 Vdc	G-F= (.313 mV)	2.12 Vdc
6 3 0 6 3 HZ	H= 4.199	10.95 Vdc	H= (4.199)	12.12 Vdc

Test the SS33 Reference Loop Diagnostic Circuitry

6. Setup:

   No change from previous (Test the Control DACs) setup.

7. Measure Voltage Levels:

   Enter SHIFT SPCL 3 2 5 Hz, to enter Service Mode and enable internal voltage measurements.

   Key in the functions in Table 8N-8 and measure the voltages for each Function in Table 8N-8. Verify that the voltages are correct.

Table 8N–8. *SS33 Reference Loop Diagnostic Inputs*

Function	Signal Source	Voltage
1 5 HZ	A11A1 U4 Pin 12	5.9 to 6.5 Vdc
1 8 HZ	A11A1 U4 Pin 9	≈5.2 Vdc

Test the Oscillator Band Select Lines

8. Setup:

   Connect DVM at A11A1 U15A pin 3. See component locator on page 8N-104.

9. Measure Voltages:

   Set the following HP 8642 frequencies at the front panel and verify the DVM Measurements in Table 8N-9.

Table 8N–9. Oscillator Band Select Lines Measurements

HP 8642 Front Panel Setting	DVM Measurements	
	A11A1 U15A pin 3 (BAND 1)	A11A1 U15A pin 5 (BAND 2)
640 MHz	≈ 0 Vdc	≈+15 Vdc
900 MHz	≈+15 Vdc	≈0 Vdc

Restore Module

10. Set A11A1 S1 to CLOSED (closed loop) position.
11. Replace A11A1.

CHECK 3: A11A2 VCO BOARD (SS34)

Essentials of SS34 Circuit Operation

Refer to BD11. Each of the two VCOs on SS34 are electronically tunable to three frequencies giving a total of six frequencies (frequencies are listed as Band No. 1 and Band No. 2 on BD 11). There is a functional block called **VCO SWITCH DRIVE** that enables the VCO required for the correct frequency output. The **PRETUNE FILTER,** filters the voltage from the Pretune DAC which tunes the selected VCO to near the correct frequency. The **BUFFER** buffers the error signal that phase locks the selected VCO. The VCO is locked to the 135 MHz signal from the A6 module and one of the three (742.5, 787.5, 832.5) signals from the A7 module. The six output frequencies are the result of mixing the VCO output with A7 module frequencies for a sum or difference of 135 MHz. This 135 MHz is the A11 IF Freq which is phase locked to the A6 135 MHz inpact.

Description of Check 3

The smallest board in the A11 module is A11A2 (see middle board shown on Module Test Point/Adjustment Locations on p 8N-100). This check is a verification that the 2 Voltage Controlled Oscillators (**VCO BAND 1** and **VCO BAND 2**) on A11A2 are at the correct frequency and power levels for the front panel settings given in Table 9. The power splitter adapter allows you to observe the output of the VCOs while the instrument is being cycled through different frequencies. If a test fails during Check 3, refer to SS34 Component Level Repair Directory.

Required Equipment:

Spectrum Analyzer	HP8566A/B
HP 8642 Bench Service Kit	HP 11802A
Power-Spitter Adapter	HP 8642-60079

Test the VCOs

1. Setup:

   Switch the HP 8642 to standby.

   Remove Power Splitter A11A3 Z1. (If the A11A2/A11A3 cover is not removed, use needle nose pliers to remove (by pulling) Z1 through the access hole labeled Z1).

   Install Power Splitter Adapter (HP 08642-60079) in place of Z1. (The notch in the adapter should face the front of HP 8642).

   Connect the Pin 1 Jack of the adapter to the input of the spectrum analyzer.

   Ensure that A11A1 S1 is set to its open (open loop) position.

   Disconnect cable A11W1 (925) from A11A3 J3.

   Turn on the HP 8642.

2. Measure Power Levels and Frequency:

   Select the HP 8642 front panel frequencies shown in Table 8N-10, and compare the measured power levels and frequencies with the Table 8N-10 values.

Table 8N–10. VCO Frequency Select Table

HP 8642 Front Panel Setting	VCO Band	VCO Frequency	VCO Power
540 MHz	1	600 to 615 MHz	6 to 10 dBm
575 MHz	1	645 to 660 MHz	6 to 10 dBm
650 MHz	1	690 to 705 MHz	6 to 10 dBm
800 MHz	2	870 to 885 MHz	6 to 10 dBm
850 MHz	2	915 to 930 MHz	6 to 10 dBm
900 MHz	2	960 to 975 MHz	6 to 10 dBm

Restore Module

3. Return S1 to its CLOSED (closed loop) position.
4. Reconnect A11W1 to A11A3 J3.
5. Replace A11A3 Z1.

CHECK 4: A11A3 POWER SPLITTER/MIXER BOARD (SS35)

Essentials of SS35 Circuit Operation

Refer to BD11. The A11A2 REFERENCE LOOP VCO OUTPUT is connected to the A11A3 REFERENCE LOOP POWER SPLITTER by semi-rigid coax cable from A11A2 J3 to A11A3 J6. On A11A3, the input signal is split into two signals and amplified. The output from **POWER SPLITTER** Z1 pin 5, drives the **OUTPUT LIMITER/AMPLIFIER**. The gain of the last transistor stage (A11A3Q1) is controlled by the **OUTPUT LEVEL CONTROL DAC** on SS33 (DD) . This enables the instrument processor to maintain the output level from the A11 module at 2.9 dbm +1 −0.1 dbm, for all six frequencies generated by this module.

The other output from **POWER SPLITTER** Z1 pin 6, drives the **LO LIMITER/AMPLIFIER**. This amplifier supplies **LO** drive for the **REFERENCE LOOP MIXER**.

The **REFERENCE LOOP MIXER** mixes the reference loop output with one of the three **SAWR OSCILLATOR** frequencies from the A7 module. The difference between these two frequencies is the **REFERENCE LOOP IF**. This is always 135 MHz. It is filtered in the 1st **LOW-PASS FILTER**, and fed back to the phase detector on SS32, to phase lock to the **FM LOOP OUTPUT** signal.

Description of Check 4

The A11A3 assembly (see lower board on Module Test Point/Adjustment Locations on foldout opposite BD11) is the board situated alongside A11A2. This check verifies that the A11A3 circuitry has the correct power and frequency levels at its output. Then, the output of the feedback path is tested to verify correct **POWER SPLITTER** and **REFERENCE LOOP MIXER** operation.

If a test fails during Check 4, refer to **SS35** Component Level Repair Directory.

Required Equipment:

Measuring Receiver ..... HP 8902A
Sensor Module ..... HP 11722A

Test the A11 Output Level Accuracy

1. Setup:

   Switch the HP 8642 to Standby.

   Remove W31 from SUM LOOP/DIVIDER MODULE connector A12A2 J2 (see instrument top cover) and connect the Measuring Receiver and Sensor Module to W31.

   Turn on the HP 8642.

2. Measure Power Level:

   Set the HP 8642 RF frequencies to the values given in Table 8N-11 and measure the RF Level output from the A11 module on W31.

NOTE

If the A11 Output level Accuracy test in Table 8N-11 fails by less than 1 db, performing the A11 Adjustments and Auto-Adjustment routines will probably correct this failure.

The A11 output frequency listed in Table 8N-11 is the "locked" output frequency expected from the A11 module. If the module is not "locked" this frequency will not be correct.

Table 8N-11. A11 Output Level Accuracy

HP 8642 Frequency	A11	Results		
	Output Frequency	Min.	Measured	Max.
528.751 MHz	607.5 MHz	2.8 dBm	_____	3.0 dBm
607.5 MHz	652.5 MHz	2.8 dBm	_____	3.0 dBm
607.6 MHz	697.5 MHz	2.8 dBm	_____	3.0 dBm
832.5 MHz	877.5 MHz	2.8 dBm	_____	3.0 dBm
832.6 MHz	922.5 MHz	2.8 dBm	_____	3.0 dBm
922.5 MHz	967.5 MHz	2.8 dBm	_____	3.0 dBm

3. Reconnect W31 to A12A2 J2.

Test the A11 Ref Loop IF Output

4. Setup:

   Remove A11W1 at A11A1 J2 (DL) .

   Set A11A1 S1 to the OPEN (open loop) position.

   Connect the Measuring Receiver and Power Sensor to A11W1.

5. Measure Power Levels and Frequencies:

   Set the HP 8642 front panel frequency to those listed in Table 8N-12 and verify that the signal is 135 MHz (±3 MHz) at −6 to −15 dBm.

Table 8N-12. HP 8642 Frequency Settings

Frequency
540 MHz
575 MHz
650 MHz
800 MHz
850 MHz
900 MHz

Restore Module

6. Reconnect A11W1 to A11A1 J2 (DL) .
7. Return A11A1 S1 to the CLOSED (closed loop) position.
8. Replace the A11A2/A11A3 cover (unless proceeding with SS35 Component Level Repair).

COMPONENT LEVEL REPAIR DIRECTORY

The following tables contain information to aid in component level repairs. These tables are designed to be used after the module troubleshooting procedures have verified a failure in circuitry represented on one of the module service sheet schematics. In general the tables supply one of the following types of information:

* Special function codes relevant to the module.

* Transistor emitter, base and collector voltages.

* Frequency and power levels at different circuit points.

* Module control line and power supply interconnections in the module and instrument.

NOTE

Start with the tables that are labeled with a Service Sheet number (Example: **Table 8N-13. SS32 DC Voltages***). Other tables are more general and are to be used at your discretion. It is suggested all tables be reviewed so their usefulness for component level repair can be determined.*

SERVICE SHEET 32

Table 8N–13. SS32 DC Voltages

Transistor	Collector	Base
Q1	4.9 to 6.9 Vdc	0.6 to 0.9 Vdc
Q2 and Q6	5.0 to 6.9 Vdc	0.7 to 1.0 Vdc
Q3 and Q9	5.3 to 6.9 Vdc	1.2 to 1.4 Vdc
Transistor	**Emitter**	**Base**
Q7	−6.1 to −5.3 Vdc	−5.2 to −4.8 Vdc
Q8	5.8 to 6.4 Vdc	6.5 to 7.3 Vdc

Table 8N–14. SS32 RF Power Levels

Stage	Input Level	Output Level	Stage Gain*
PHASE DETECTOR LO PORT DRIVER Stage 1 (Q2) Stage 2 (Q3)	0 to 6 dBm	16.5 to 19.5 dBm	≈20 dB ≈8 dB ≈12 dB
REFERENCE LOOP IF AMPLIFIER Stage 1 (Q1) Stage 2 (Q6)	−12.5 to −10.5dBm	4 to 9.5dBm	≈20 dB ≈12 dB ≈8 dB
PHASE DETECTOR RF PORT DRIVER	4.5 to 10.0 dBm	16.5 to 19.5dBm	≈12 dB
PHASE DETECTOR (LO Input) (RF Input) (IF Output)	16.5 to 19.5 dBm 16.5 to 19.5 dBm 16.5 to 19.5 dBm	 0 Vdc (loop locked) 0.7V triangle into 50Ω (unlock)	– – – – –

* Stage gain must be measured with an input level low enough to eliminate gain compression (≈ −40dBm).

Table 8N–15. SS32 Typical Filter Responses

Filter	Input Level	Cutoff Freq	Freq	Response
2nd IF Low Pass	6 to 10 dBm	150 MHz	150 MHz 200 MHz 400 MHz 1.3 GHz	0 dBc < −20 dBc < −75 dBc < −100 dBc
Ref Loop Filters				
45 MHz Low Pass			50 MHz 70 MHz 100 MHz 300 MHz	−5 dBc −20 dBc < −70 dBc < −70 dBc
22.5 MHz Notch			10 MHz 20 MHz 22.5 MHz 25 MHz 50 MHz	−3 dBc −10 dBc < −30 dBc −10 dBc −5 dBc

Table 8N–16. *Power Supply Line Interconnections (Between Modules)*

Supply	A17	A5		A11
	Output	Input	Output	Input
+50 Vdc	J2 pins 3&4	J12 pins 3&4	J4 pins 5&6	J1 pins 5&6
+15 Vdc	J2 pins 9-18	J12 pins 9-18	J4 pins 9&10	J1 pins 9&10
−5 Vdc	J2 pins 23-26	J12 pins 23-26	J4 pins 2&4	J1 pins 2&4
+5 Vdc	J2 pins 35-50	J12 pins 35-50	J4 pins 1&3	J1 pins 1&3
−15 Vdc	J2 pins 19-22	J12 pins 19-22	J4 pins 15&16	J1 pins 15&16
GND		Chassis gnd	J4 pins 11&13	J1 pins 11&13

SERVICE SHEET 33

Table 8N–17. *Serial Data Control Lines*

Enter Service Mode	Service Function	All Ref Des	Level	Line Label
SHIFT SPCL 3	60142 Hz	U13D pin 8	TTL High	REF Clock
	60242 Hz	U13D pin 8	TTL Low	REF Clock
	60143 Hz	U13E pin 10	TTL High	REF Data
	60243 Hz	U13E pin 10	TTL Low	REF Data

Table 8N–18. *Control Line Interconnections (Between Modules)*

Line Label	A11	A5		A4	
	Input Connector Pin	Output Connector Pin	Input Connector Pin	Output Connector Pin	Latch IC Pin
OOL Disable*	–	–	–	–	U13 19
REF CLK	A11A1J1 12	A5J4 12	A5J16 45	A4P2 45	U16 6
REF DATA	A11A1J1 14	A5J4 14	A5J16 50	A4P2 50	U16 9
REF OOL	A11A1J1 7&8	A5J4 7&8	A5J16 10	A4P2 10	U35 18

* OOL Disable: Circuitry Located on A4. Disables all out of lock interrupts to the DCU.

Table 8N–19. *Setting Serial Data Interface Outputs*

A11 Ref Des.	Line Label	Bit Number	Decimal Value
U6 pin 16	PT0	0	1
U6 pin 15	PT1	1	2
U6 pin 6	PT2	2	4
U6 pin 9	PT3	3	8
U6 pin 12	PT4	4	16
U6 pin 5	PT5	5	32
U6 pin 2	BAND 1	6	64
U18 pin 19	BAND 2	7	128
U18 pin 5	DAC 0	8	256
U18 pin 15	DAC 1	9	512
U18 pin 12	DAC 2	10	1,024
U18 pin 9	DAC 3	11	2,048
U18 pin 6	DAC 4	12	4,096
U18 pin 16	DAC 5	13	8,192
U18 pin 19	DAC 6	14	16,384
U2 pin 2	SEL 2	15	32,768
U2 pin 2	SEL 1	16	65,536
U2 pin 5	SEL 0	17	131,072
U2 pin 6	SB0	18	262,144
U2 pin 9	SB1	19	524,288
U2 pin 12	SB2	20	1,048,576
U2 pin 15	SB3	21	2,097,152
U2 pin 16	SB4	22	4,194,304
U6 pin 18	SB5	23	8,388,608

To set the outputs of the Serial Data Interface registers (U2, U18, and U6 on SS33), key in: [SHIFT] [SPCL] [3] [6] [0] [7] [Decimal Value*] [HZ]

* To determine the decimal value to enter you must first know what you want each bit to be, high or low. This gives you a 24 bit binary coded decimal (BCD). Convert this BCD to its decimal equivalent by adding the Decimal Values (from Table 24) of the Lines you want to be high.

NOTE

To determine which bits are set, key in [SHIFT] [SPCL] [3] [6] [0] [3] [3] [HZ], *then convert the decimal number on the display to a binary number. For example, if 5592405 is displayed, the following bit numbers are set: 0, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, and 22.*

To set all bits low, key in: [SHIFT] [SPCL] [3] [6] [0] [7] [0] [HZ]

To set all bits high, key in: [SHIFT] [SPCL] [3] [6] [0] [7] [16777215] [HZ]

Table 8N-20. *Reference Loop Internal Voltmeter Measurements*

Enter Service Mode	Function	Line Label	Explanation
SHIFT SPCL 3 2	1 1 HZ	REF OOL (U4 pin 4)	+5V (locked) 0V (unlocked)
	1 2 HZ	PRETUNE DAC (U4 pin 5)	≈ (8 to 49 Vdc) m=4.333
	1 3 HZ	INTEGRATOR OUTPUT SENSE (U4 pin 6)	≈ 2 to 12V (locked)
	1 4 HZ	SHAPER SENSE DAC (U4 pin 7)	≈ 1.5 to 5.5V With A11A1 S1 Open
	1 5 HZ	PRETUNE REF VOLTAGE (U4 pin 12)	≈ 6.2 vdc
	1 6 HZ	COMPARATOR OUTPUT SENSE (U4 pin 11)	+5V (locked) or (unlocked)
	1 7 HZ	LEVEL CONTROL DAV (U4 pin 10)	(11 to 15 vdc) m = 2.000
	1 8 HZ	+5V (F1)	≈ 5.10 vdc

NOTE

Internal voltmeter measurements come from sense lines that are multiplexed by A11A1 U4 and displayed on the front panel. Some lines require scaling down before being multiplexed. The HP 8642 firmware corrects this scaling factor before displaying the actual multiplexer output. If an external voltmeter were to be connected at A11A1 TP4 or A4 TP3 "VM OUT" you would need to multiply its reading by "m" (in the table) to match the reading on the HP 8642 front panel. All measurements can be repeated by keying in 1 HZ.

Table 8N-21. *Reference Loop DAC Control Service Functions*

Enter Service Mode	Service Function	Data	Results
SHIFT SPCL 3	630 = DATA + Hz	0 to 63	Pretune DAC ≈ 8 to 50V
	631 + DATA + Hz	0 to 63	Shaper DAC ≈ 1.5 tp 5.5V
	632 + DATA + Hz	0 to 127	Output Level DAC ≈ 11 to 15V

SERVICE SHEET 34

Table 8N–22. *SS34 DC Voltages*

Transistor	Collector	Base
Q1-Q3	5.1 to 6.5 Vdc	0.6 to 0.9 Vdc

Table 8N–23. *SS34 RF Power Levels*

Measurement Point	Level
TP4	≈−20 dBm
TP5	6 to 10 dBm

Table 8N–24. *VCO Frequency Select Table*

HP 8642 Front Panel Settings	VCO Band#	VCO Frequency
528.751 MHz to 562.5 MHz	1	607.5 MHz
562.6 MHz to 607.5 MHz	1	652.5 MHz
607.6 MHz to 652.5 MHz	1	697.5 MHz
787.6 MHz to 832.5 MHz	2	877.5 MHz
832.6 MHz to 877.5 MHz	2	922.5 MHz
877.6 MHz to 922.4 MHz	2	967.5 MHz

SERVICE SHEET 35

Table 8N–25. *SS35 DC Voltages*

Transistor	Collector	Base
Q1-Q8	5.1 to 6.5 Vdc	0.6 to 0.9 Vdc
Q9	6.0 to 8.4 Vdc	0.9 to 1.3 Vdc

Table 8N–26. *SS35 RF Power Levels*

Stage	Input Level	Output Level	Insertion Loss
Power Splitter	6 to 10 dBm	–	≈ 6dB
Output Limiter/Amp	0 to 6.5 dBm	4 to 5 dBm	–
LO Limiter/Amp	0 to 6.5 dBm	4 to 5 dBm	–
Mixer (LO Input) (RF Input)	16.5 to 20 dBm −4 to −5dBm	−10 to −11 dBm	– –

Table 8N–27. *SS35 Typical Filter Responses*

Filter	Input Level	Cutoff Freq	Freq	Response (dB relative to passband)
OUTPUT LIMITER/AMPLIFIER (OUTPUT FILTER)	+4 TO +5 dBm	1 GHz	1.2 GHz 1.3 GHz 1.4 GHz 2 to 5 GHz	< −40 dB < −50 dB < −60 dB < −50 dB
860 MHz RF FILTER	+4.5 to 5.5 dBm	930 MHz	880 MHz 1.2 GHz 1.4 GHz and above	< −1.6 dB < −30 dB < −40 dB
1st IF LOW PASS FILTER (120 MHz LOW PASS)	−10 to −11 dBm	150 MHz	135 MHz 200 MHz 300 MHz 400 MHz ≥500 MHz	< −1.5 dB < −5 dB < −25 dB < −50 dB < −60 dB

MISC A11 INFORMATION

Table 8N–28. *A11 Special Functions*

Enter Service Mode	Select a Function	
SHIFT SPCL 3	7 0 1 Hz	Turns off Reference Loop Cal Data
	7 1 1 Hz	Turns on Reference Loop Cal Data
	6 2 0 0 Hz	Displays SAWR Loop Frequency
	6 2 0 1 Hz	Displays REF Loop Frequency

Adjustments

DESCRIPTION OF A11 ADJUSTMENTS

Overall Equipment List

Spectrum Analyzer	HP 8566A/B
Signal Generator	HP 8642A/B
Measuring Receiver	HP 8901B or HP 8902A
Sensor Module	HP 11722A
DVM	HP 3456A
HP-IB Printer	HP 2225A
34 dB Attenuator	08642-60239
2 each SNC 50Ω Terminations	1250-0839
8 pin mixer Adapter	08642-60078
Power Splitter Adapter	08642-60079
RF Probe	08642-20089
Alignment Tool	8710-1515

NOTE

Each adjustment procedure assumes the HP 8642 internal cabling is connected normally and all circuitry is functioning properly.

There are two manual adjustment procedures for the A11 Module: the Loop Filter, and Beat Note Detector. The two adjustments can be done independently. The Loop Filter Adjustment reduces the 22.5 MHz side bands on the RF output of the module. The Beat Note Detector allows the module to acquire lock when the instrument is powered on. There are also VCO adjustments that are part of the Auto-Adjustment Procedure.

ADJUSTMENT 1: A11 LOOP FILTER AND BEAT NOTE DETECTOR

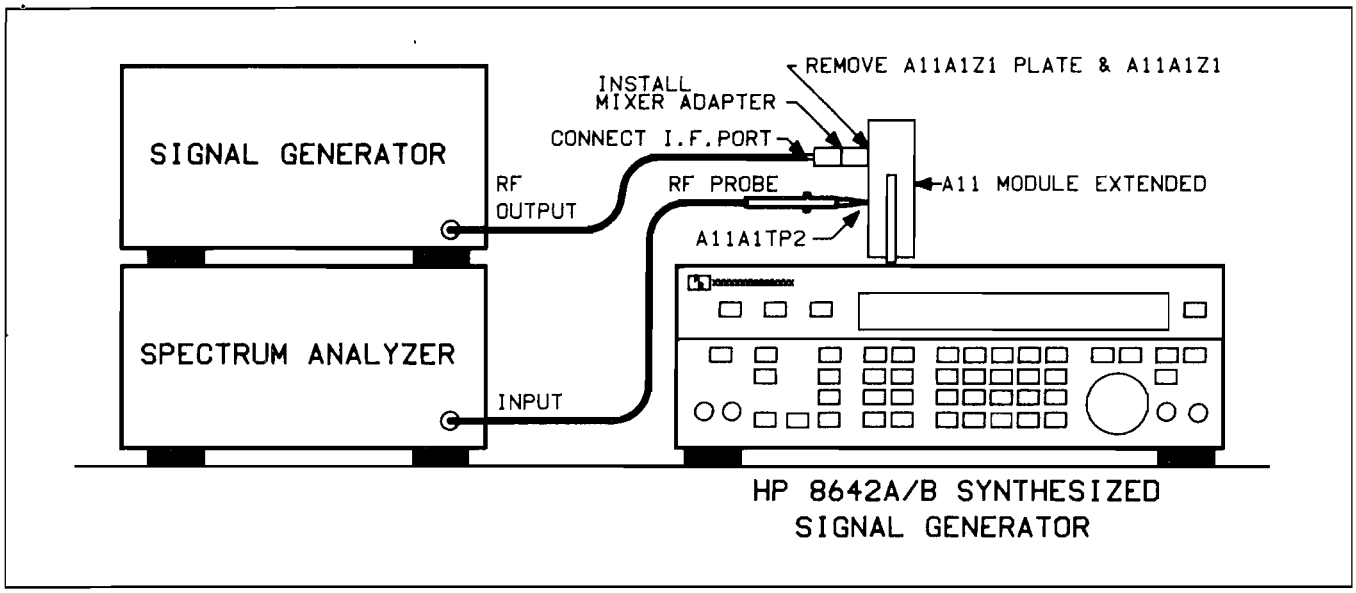


Figure 8N–6. *Loop Filter and Beat Note Detector Adjustment Setup*

Required Equipment:

Spectrum Analyzer	HP8566A/B
Signal Generator	HP8642B
8 Pin Mixer Adapter	08642-60078
RF Probe	08642-20089

Procedure

Loop Filter Adjustment

1. Setup:(Refer to Figures 8N-6 to 8N-8)

   Switch the HP 8642 to Standby.

   Extend the A11 module, using extender posts 08642-20041.

   Remove phase detector cover and phase detector A11A1 Z1. (A11A1 Z1 plugs in, gently remove with a pair of needle nose pliers)

   Set the Signal Generator power to 0 dBm and RF sweep for 15 to 30 MHz.

   Set the Spectrum Analyzer to start freq: 15 MHz, stop freq: 30 MHz, resolution BW: 300 kHz.

   Install 8 Pin Mixer Adapter in place of A11A1 Z1, with notch to the right and connect the RF Source to the IF Port of the adapter (Pin 3 Jack).

   Connect A11A1 TP2 to the spectrum analyzer using the RF Probe, 08642-20089.

   Switch the HP 8642 to ON.

2. Adjust Loop Filter Notch Depth:

   Manually sweep the Signal Generator while adjusting A11A1 C34 for a notch at 22.5 MHz that is less than −30 dBc.

Beat Note Detector Adjustment

3. Adjust Beat Note Detector Symmetry:

   Ensure that no test equipment is connected to A11A1 TP2.

   Adjust A11A1 R42 so that the out of lock LED, A11A1 DS1, is at about half intensity. (A11A1 DS1 can be seen by looking down at the top of the module.)

Restore Module

4. Switch the HP 8642 to Standby.
5. Move A11A1 S1 to its CLOSED position.
6. Remove the 8 Pin Mixer Adapter
7. Re-install the phase detector and cover.
8. Re-install the Module.
9. Re-install the top cover.

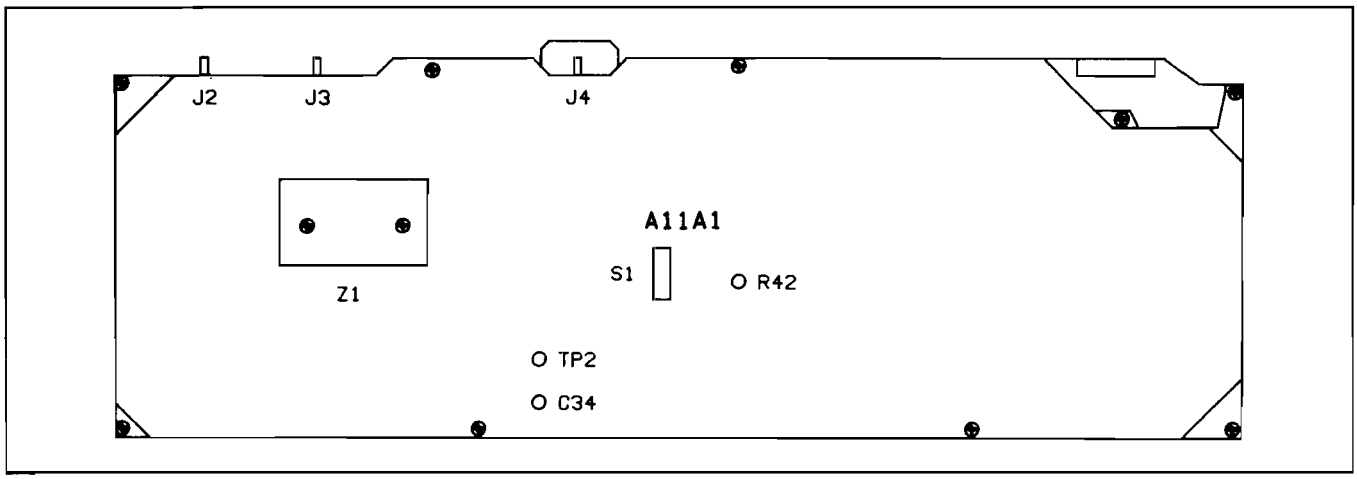


Figure 8N–7. *A11 Module, Leftside (AllA1Z1 is behind cover)*

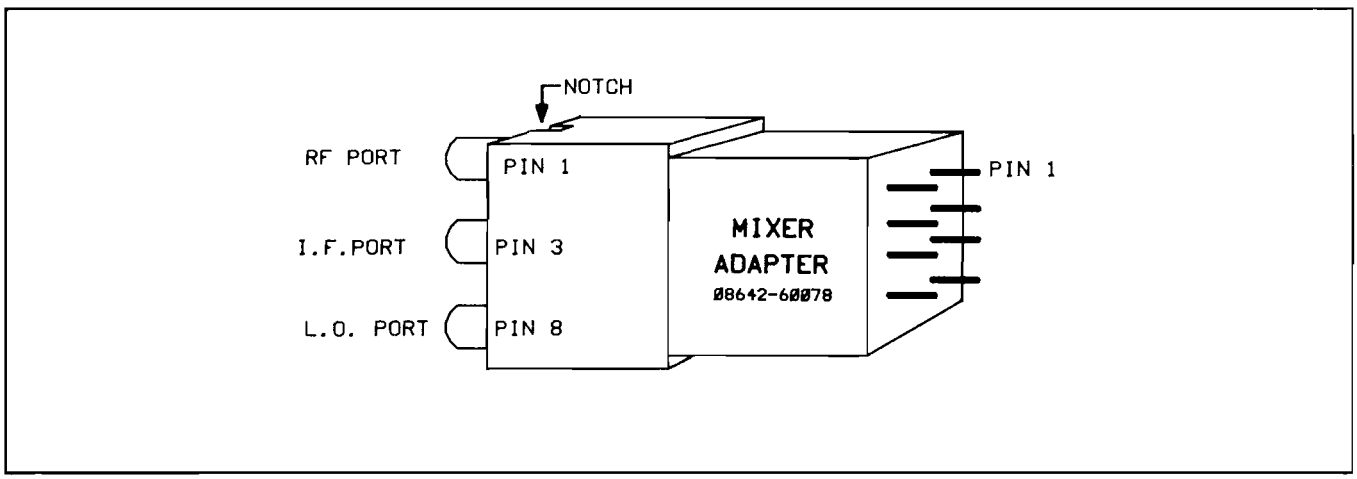


Figure 8N–8. *8 pin Mixer Adapter- 08642-60078*

A11 AUTO-ADJUSTMENTS

NOTE

Read section 5 before proceeding with this Auto-Adjustment procedure.

Description

The HP 8642A/B temperature must be allowed to stabilize with the covers on for one hour. Then the instrument top cover must be removed, A11 extended and the VCO frequencies must be adjusted and recorded ($f1$) before temperature rise can cause significant drift. Now the temperature must be allowed to stabilize again for one hour. Once this is done, the VCO frequencies are measured again ($f2$) and re-adjusted to the normal operating frequency ($f3$). The Auto Adjust Routine is now run to generate data for the DAC's in the A11 Module. This consists of six setups and then the Cal Data transfer. After the Auto Adjust Routine has been finished, the VCO's are measured ($f4$) and adjusted to the normal center frequency plus the frequency difference between normal and elevated temperature ($f4+f2-f3$). The Instrument Level Diagnostics are run to insure that the HP 8642 is functional. Then the new A11 Cal Data is copied to the A20.

Required Equipment:

Measuring Receiver	HP8902A
Sensor Module	HP11722A
DVM	HP3456A
HP-IB Printer	HP2225A
34 dB Attenuator	08642-60239
2 each SMC 50Ω Terminations	1250-0839
8 Pin Mixer Adapter	08642-60078
Power Splitter Adapter	08642-60079

Procedure

1. Before Beginning:

   Insure that you will be performing this procedure in a temperature controlled environment. The procedure will take several hours (mostly unattended) and must be done continuously. It is important that the time periods in the temperature stabilization steps be followed closely. A significant change in temperature will cause the VCO's to drift in frequency and the HP 8642 will abort the procedure.

   Connect the Measuring Receivers 10 MHz Timebase out to the HP 8642's Timebase in.

   Ensure that the Measuring Receiver is fully calibrated and that the calibration numbers for the Power Sensor have been correctly entered in to the Measuring Receiver.

2. Temperature Stabilization:

   With instrument power on and all internal and external covers in place, allow the instrument to warm up for 1 hour.

3. VCO Adjustment Setup: (Refer to Figures 8N-9 to 8N-11)

Connect the 10 MHz time base out from HP 8642 to HP 8902's 10 MHz time base in.

Disconnect cable W24 (935) from A11A1 J3 and connect a 50Ω load termination to J3.

Disconnect W25 (937) from A11A3 J4 and connect a 50Ω load termination to J4.

Extend A11 Module on extender posts.

Move LOOP SWITCH A11A1 S1, on left side of A11 Module, down to its OPEN position.

Remove power splitter cover from right side of A11 Module.

Remove power splitter (A11A3 Z1) by gently pulling out with needle nose pliers.

Connect adapter, 08642-60079, to power splitter sockets (orient adapter with notch to the left).

Connect Sensor Module to adapter, pin 1, using a short piece of flexible coax cable (2 inch).

Connect Sensor Module to Measuring Receiver.

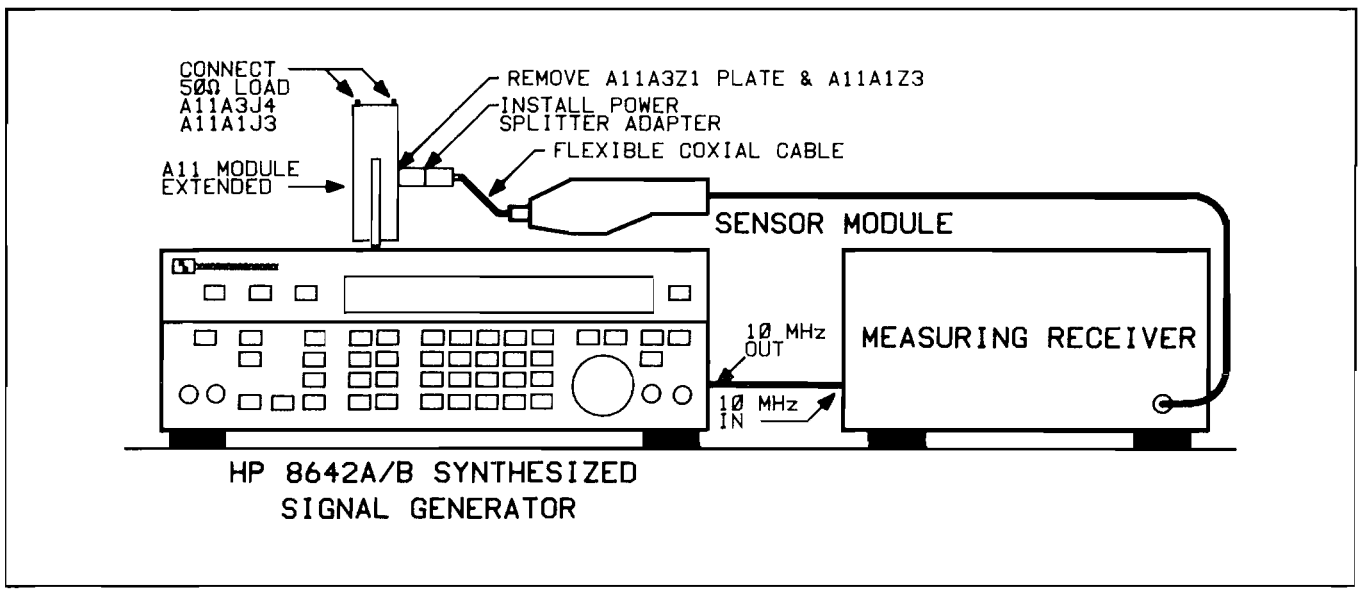


Figure 8N–9. *A11 VCO Adjustment Setup 1*

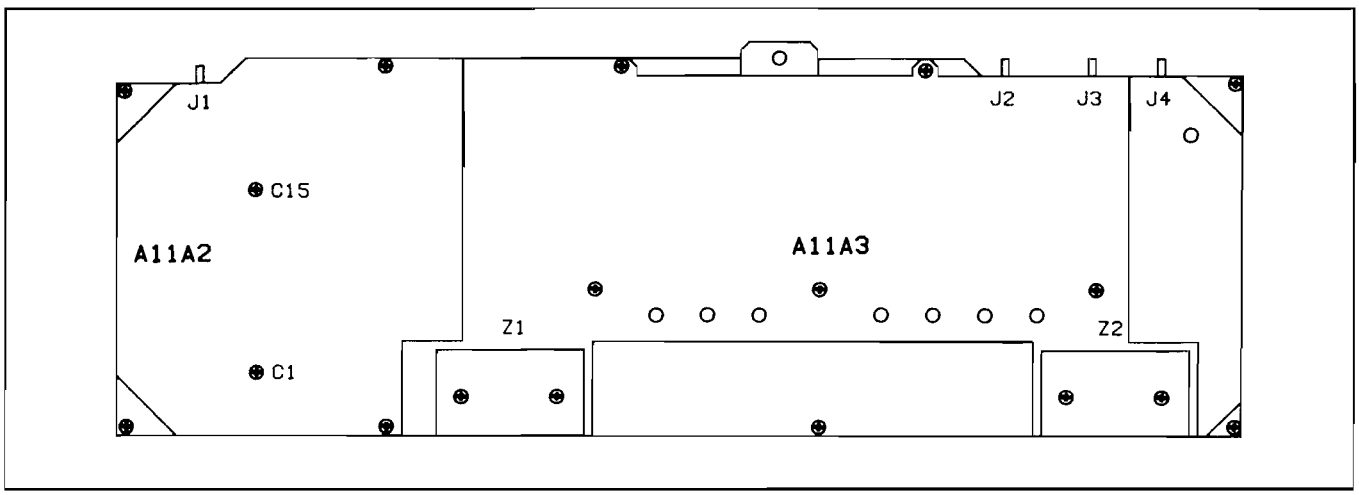


Figure 8N–10. *A11 Module Right Side (Access screws or covers must be removed to access components)*

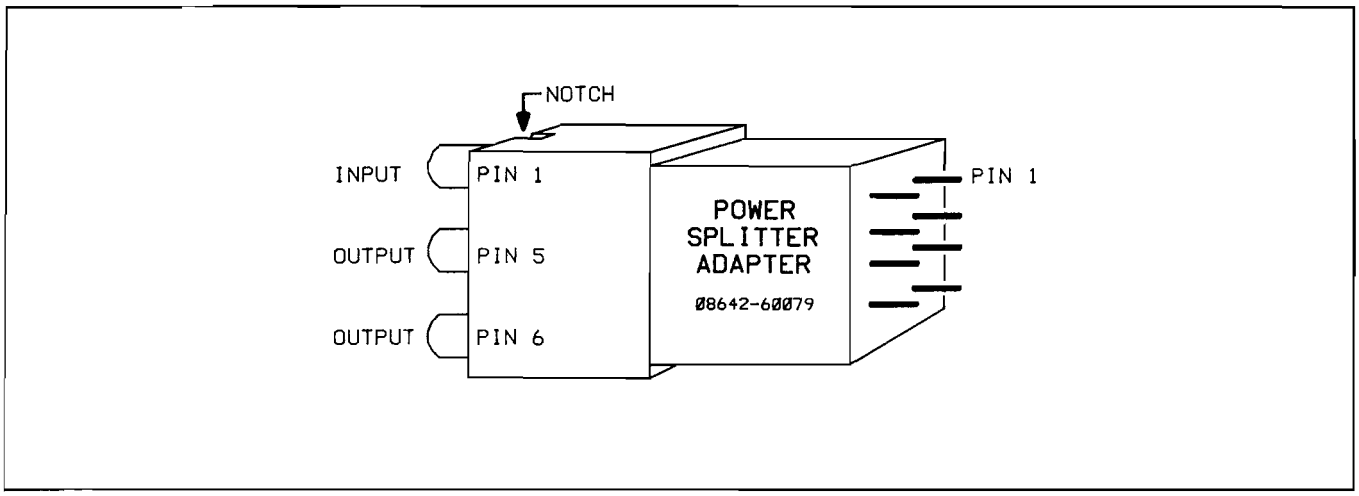


Figure 8N–11. *Power Splitter Adapter (HP 08642-60079)*

4. Adjust Initial VCO Frequency:

   (This must be done immediately after the module is extended so that the temperature is approximately the same as it is during normal operation.)

   Set the Measuring Receiver to measure frequency.

   Enter the key sequence given in the table below for each of the A11A2 Adjustments. Make the adjustment until the Measuring Receiver frequency reading ($f1$) is with in the limits given and record the value for later use.

   Set the Measuring Receiver to measure RF Power.

   Verify that the power level is greater than +4 dBm at each of the VCO frequencies.

Table 8N–29.

HP 8642 Key Sequence	A11A2 Adj.	$f1$ (MHz) Min	$f1$ (MHz) Actual	$f1$ (MHz) Max
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 63061 Hz, 63163 Hz	C1	696.500	___ . _____	698.500
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63061 Hz, 63163 Hz	C15	966.500	___ . _____	968.500

5. Verify VCO Range:

   Enter the key sequence given in the table below for each of the A11A2 Adjustments.

   Set the Measuring Receiver to measure frequency.

   Verify that the frequency reading is less than the Maximum given in the table below.

   Set the Measuring Receiver to measure RF Power.

   Verify that the power level is greater than +4 dBm at each of the VCO frequencies.

HP 8642 Key Sequence	Frequency (MHz) Actual	Frequency (MHz) Max
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 63020 Hz, 63132 Hz	___ . _____	607.500
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63015 Hz, 63132 Hz	___ . _____	877.500

6. Temperature Stabilization:

   With instrument power on and the module extended, allow the instrument to warm up for 1 hour.

7. Measure Extended Module Operating Frequency:

   After the 1 hour warm up, enter the key sequence given in the table below for each of the A11A2 Adjustments. Record each VCO's Frequency ($f2$) for later use.

HP 8642 Key Sequence	A11A2 Adj.	$f2$ (MHz) Actual
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 63061 Hz, 63163 Hz	C1	___ . _____
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63061 Hz, 63163 Hz	C15	___ . _____

8. Re-adjust Extended Module Frequency:

   Set the Measuring Receiver to Frequency.

   Enter the key sequence given in the table below for each of the A11A2 adjustments. Make the adjustments until the Measuring Receiver frequency reading (f3) is with in the limits given, and record the value for later use.

Table 8N-30.

HP 8642 Key Sequence	A11A2 Adj.	$f3$ (MHz) Min	Actual	Max
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 63061 Hz, 63163 Hz	C1	696.500	___ . _____	698.500
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63061 Hz, 63163 Hz	C15	966.500	___ . _____	968.500

9. Initialize Auto Adjust Routine:

   Connect the Required Equipment to the HP 8642 via HP-IB. (See section 5 for required equipment and information about Auto Adjust routines.)

   Key in: [INST PRESET]

   Key in: [SHIFT] [SPCL] [3] [8] [8] [Hz] [8] [0] [Hz].

   Key in: [1] [Hz] when **"ENTER ROUTINE NUMBER .G8000"** appears.

   Key in the the Day, Month, Year and Module Cal ID Number when prompted by the HP 8642 display. (See Section 5 for details.)

10. When **"WAITING FOR SET-UP 1 .V24"** appears:

    Verify the setup is unchanged from Step 3.

    Press [Hz] to continue. (Run time ≈ 30 seconds)

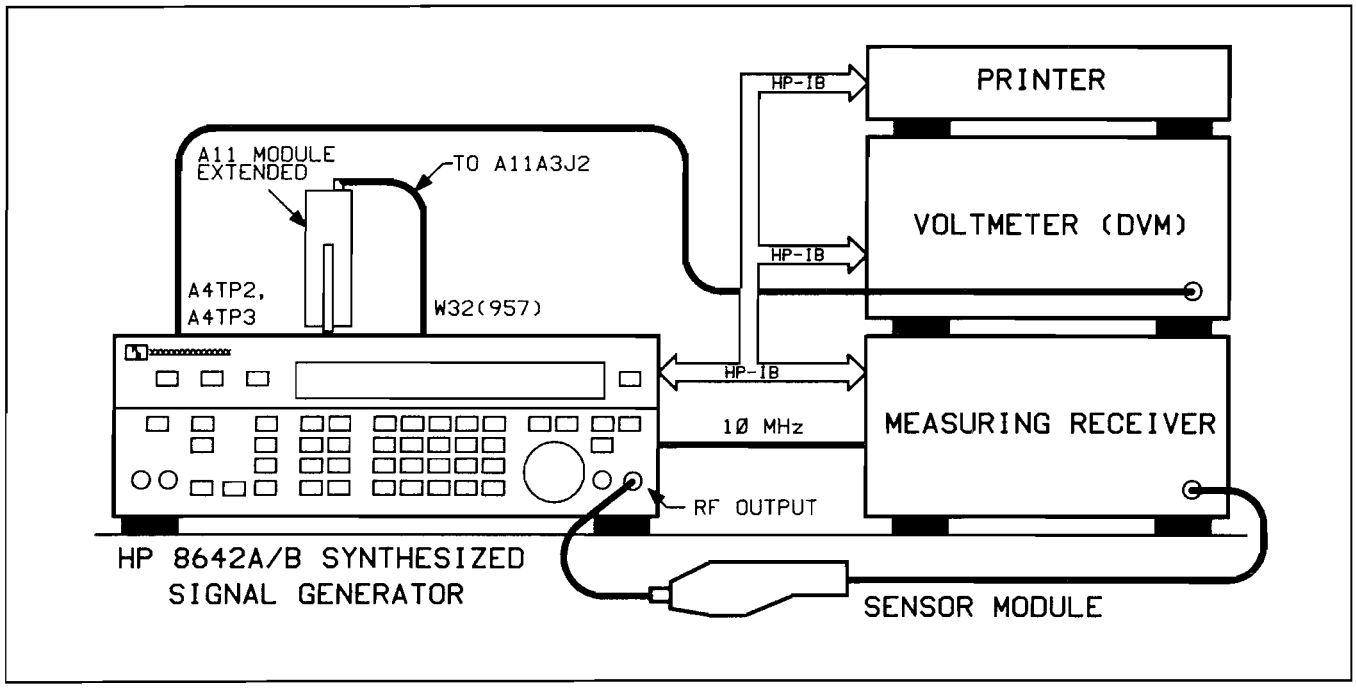


Figure 8N–12. *Set-up 2*

11. When **"WAITING FOR SET-UP 2 .V25"** appears: (Refer to Figure 8N-12.)

    Replace the Power Splitter A11A3Z1. A11A3Z1 pin 1 (Pin with blue on it's base), plugs into the square pad on the A11A3 board.

    Replace cover over Power Splitter.

    Connect Sensor Module to RF OUTPUT on HP 8642 Front Panel.

    Connect the DVM to the VM OUT (A4TP3) and ground (A4TP2) test points on the left side of the A4 Module.

    Set the DVM to measure Volts DC.

    Disconnect cable W31 (901) from A11 Module at A11A3 J2.

    Disconnect cable W32 (957) from A12 Module at A12A3 J3.

    Connect loose end of W32 (957) to A11 Module at A11A3 J2.

    Remaining set-up conditions from Step 10 are unchanged.

    Press [Hz] to continue. (Run time ≈ 60 minutes)

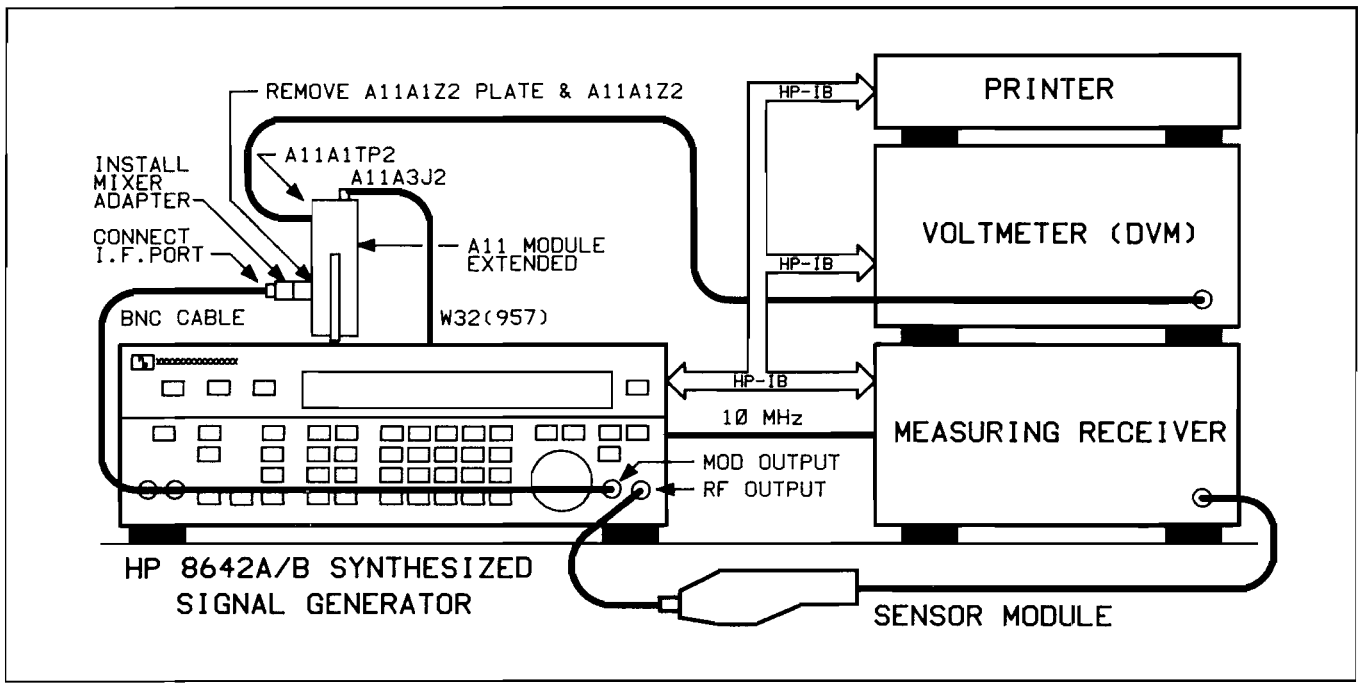


Figure 8N–13. *Set-up 3*

12. When **"WAITING FOR SET-UP 3 .V26"** appears: (Refer to Figure 8N-13.)

    Remove the phase detector Z1 cover from left side of the A11 Module. (Refer to Figure 8N-7.)

    Remove the phase detector (A11A1 Z1) by gently pulling with a needle nose pliers.

    Connect the 8 Pin Mixer Adapter (HP 08642-60078) to sockets on board. (Position adapter in sockets so that the crescent-shaped notch by SMC connectors is to the right toward front of instrument.)

    Connect a BNC cable from MOD OUTPUT port to center SMC connector on 8 Pin Mixer Adapter. (Pin 5)

    Connect DVM to A11 Module at A11A1 TP2. (Refer to Figure 8N-7.)

    Set DVM to measure AC Volts.

    All other Setup conditions are unchanged.

    Press [Hz] to continue. (Run time ≈ 30 seconds)

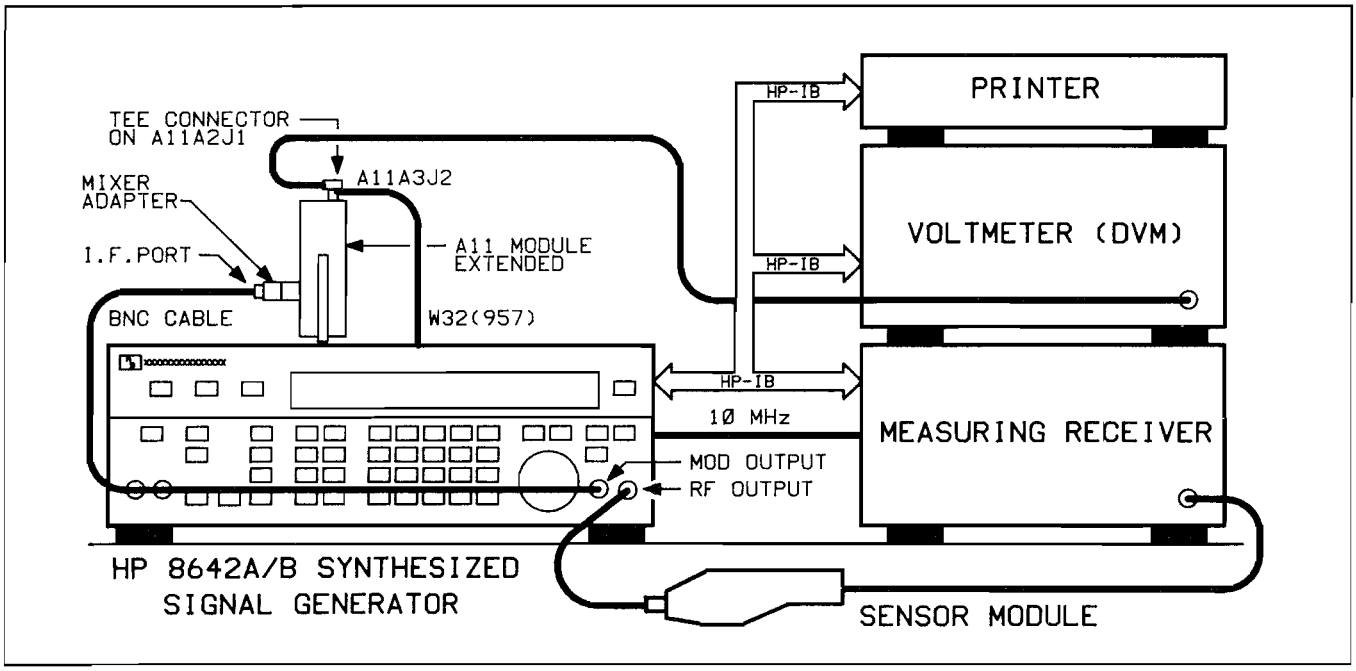


Figure 8N-14. *Set-up 4*

13. When **"WAITING FOR SET-UP 4 .V27"** appears:

    Disconnect cable A11 W2 (923) from A11A2 J1. Connect an SMC Tee connector to A11A2 J1. Connect cable A11 W2 to the Tee connector. Connect the DVM to the Tee connector.

    Set the DVM to measure AC Volts.

    All other setup conditions are unchanged.

    Press [Hz] to continue. (Run time ≈ 10 minutes)

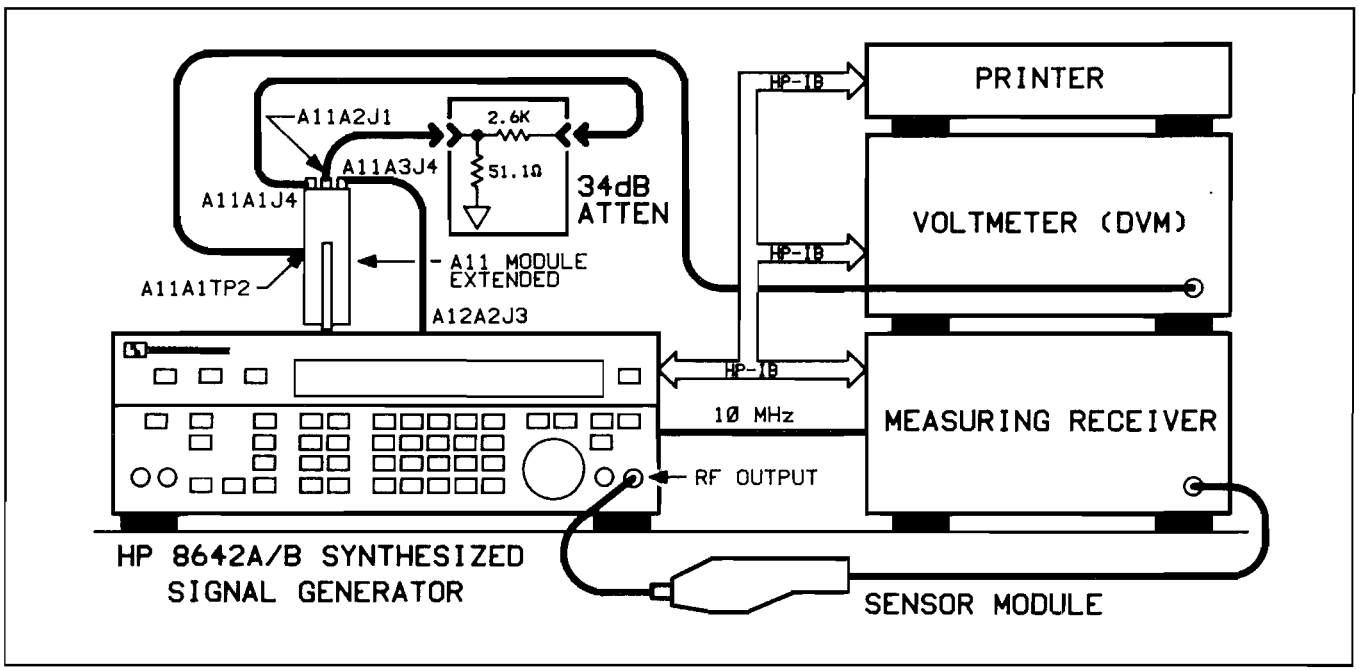


Figure 8N–15. *Set-up 5*

14. When **"WAITING FOR SET-UP 5 .V28"** appears:

    Disconnect MOD OUTPUT cable and 8 pin mixer adapter from A11 module.

    Replace the phase detector (A11A1 Z2) in instrument: Align pin 1 (pin with blue at it's base) on phase detector with square pad socket on board and insert. Replace cover over phase detector.

    Connect DVM to A11A1 TP2 on A11 Module.

    Set DVM to measure AC Volts.

    Disconnect 50Ω terminations from A11A1 J3 and A11A3 J4.

    Reconnect cable W24 (935) to A11A1 J3.

    Move A11A1 S1, on left side of module, up to its CLOSED position.

    Remove SMC Tee connector from A11A2 J1.

    Connect the 51.1Ω end of the 34 dB attenuator to A11A2 J1.

    Connect end of cable A11W2 from A11A1 J4 to the 2600Ω input of the 34 dB attenuator.

    Disconnect A12W2 (907) from A12 Module at A12A2 J3.

    Connect an external cable from A11A3 J4 to the A12 Module at A12A2 J3.

    Disconnect W31 (901) from A12A2 J2 (now W31 should be disconnect at both ends).

    Connect W25 (937) to A12 at A12A2 J2.

    Press [Hz] to continue. (Run time ≈ 2 minutes)

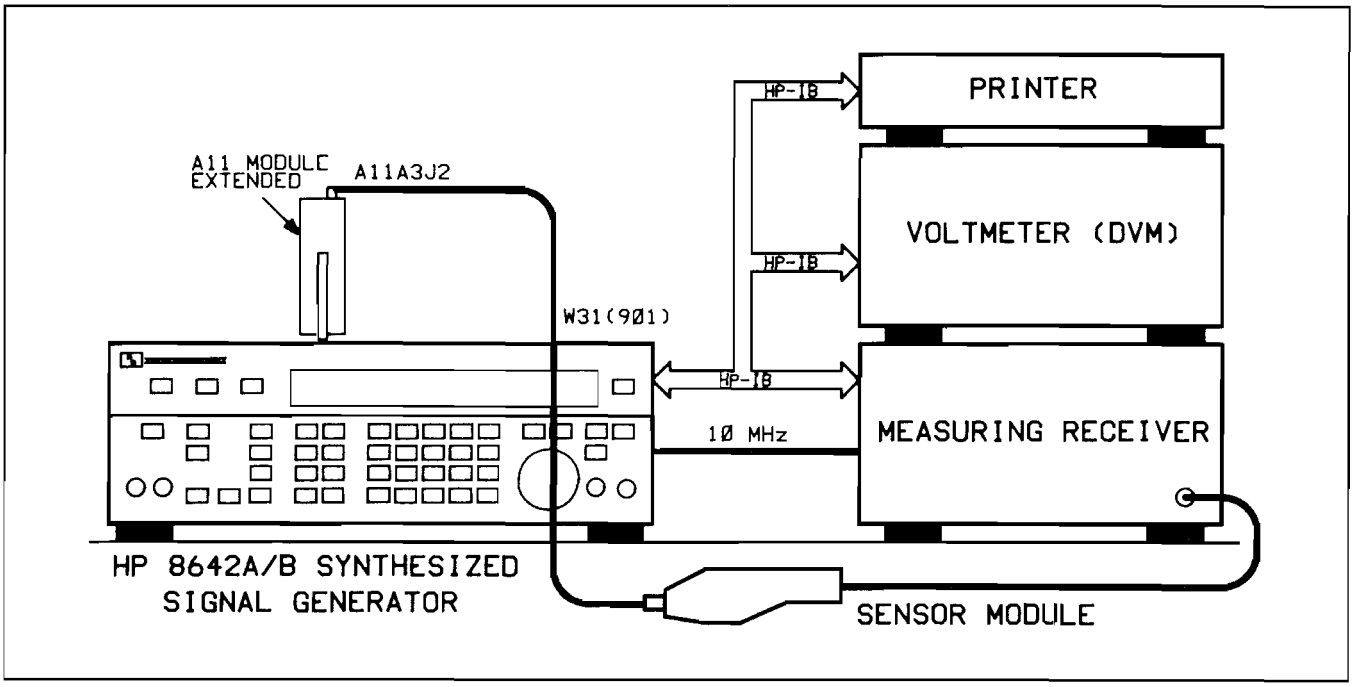


Figure 8N-16. *Set-up 6*

15. When **"WAITING FOR SET-UP 6 .V29"** appears:

    Disconnect DVM from instrument.

    Remove 34 dB pad from cable A11W2 and connect A11W2 to A11A2 J1.

    Disconnect W25 (937) from A12 at A12A2 J2.

    Disconnect the external cable from A11A3 J4 and A12A2 J3.

    Reconnect W25 (937) to A11A3 J4.

    Disconnect W32 (957) from A11A3 J2; reconnect W32 (957) to A12A3 J3.

    Reconnect A12W2 (907) to A12A2 J3.

    Reconnect W31 (901) to A11A3 J2; connect the other end of cable W31 to the Sensor Module.

    (All other cable connections should be in their normal position).

    Press [Hz] to continue. (Run time ≈ 3 minutes)

16. When **"UNPROTECT CAL. MEMORY .G8005"** appears:

    Switch A3 S2 toward the rear of the instrument to unprotect the EEPROM's.

    Press [Hz] to Continue.

17. When **"PROTECT CAL. MEMORY .G8006"** appears:

    Switch A3 S2 toward the front of the instrument to protect the EEPROM's.

    Press [Hz] to Continue.

18. When **"RECONNECT ALL CABLES .V29"** appears:

    Disconnect all test cables from the instrument.

Reconnect any instrument cables which are still disconnected.

Press [Hz] to Continue.

19. VCO Re-adjustment Setup:

Disconnect cable W24 from A11A1 J3; terminate A11A1 J3 with 50Ω.

Disconnect cable W25 from A11A3 J4; terminate A11A1 J4 with 50Ω.

Switch A11A1 S1 to its OPEN position.

Connect the Sensor Module to the front panel RF Output.

20. Measure VCO Frequencies:

Enter the key sequence given in the table below for each of the A11A2 Adjustments. Record each VCO's Frequency ($f4$).

HP 8642 Key Sequence	A11A2 Adj.	$f4$ (MHz) Actual
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 63061 Hz, 63163 Hz	C1	___ . _____
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63061 Hz, 63163 Hz	C15	___ . _____

21. Compute the correct re-adjustment frequency:

Adjustment C1: $(f4 + f2 - f3) - (1\text{MHz}) = f5$ **Min** = ____ . _____ MHz

$(f4 + f2 - f3) + (1\text{MHz}) = f5$ **Max** = ____ . _____ MHz

Adjustment C15: $(f4 + f2 - f3) - (1\text{MHz}) = f5$ **Min** = ____ . _____ MHz

$(f4 + f2 - f3) + (1\text{MHz}) = f5$ **Max** = ____ . _____ MHz

Record the ($f5$) Min and Max readings for adjustment C1 and C15 in the table below.

HP 8642 Key Sequence	A11A2 Adj.	$f5$ (MHz) Min	Actual	Max
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 63061 Hz, 63163 Hz	C1	___ .___	___ .___	___ .___
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63061 Hz, 63163 Hz	C15	___ .___	___ .___	___ .___

22. Re-adjust A11 Module:

Set the Measuring Receiver to measure frequency.

Enter the key sequences given in the table below for each of the A111A2 Adjustments and adjust the appropriate capacitor for a frequency reading between the ($f5$) Min and Max frequencies.

Restore Module

23. Re-install Module.
24. Re-connect all cables.
25. Re-install top cover.
26. Allow the instrument to stabilize (with power on) for one hour.
27. Run the instrument level diagnostics to verify operation:

    K ey in: [SHIFT] [SPCL] [3] [3] [0] [Hz].

    W hen **"WAITING FOR SETUP 1 .Z24"** appears, connect the MOD OUT to the AM/PULSE INPUT and FM/ΦM INPUT.

    P ress [Hz] to Continue.

28. When **"DIAG DONE HIT MSSGS .V1"** appears:

    Press the MSSG key to view the message buffer. If **"NO MESSAGES .00"** is contained in the message buffer, the HP 8642 is functioning properly.

29. Up Load Cal Data:

    Now that the functionality of the HP 8642 has been verified, used the following procedure to up load the new cal data.

    Switch the HP 8642 to standby.

    Remove the A20 Cal Module. (See Disassembly Procedures).

    Plug the A20 Module on to A3 J3.

    Switch the HP 8642 on.

    Switch A20 S1 to the CHANGE position.

    Key in: [SHIFT] [SPCL] [3] [7] [2] [routine_number] [Hz].

    When **"TRANSFER VERIFIED .U613"** appears on the display, move A20 S1 up to its PROTECTED position.

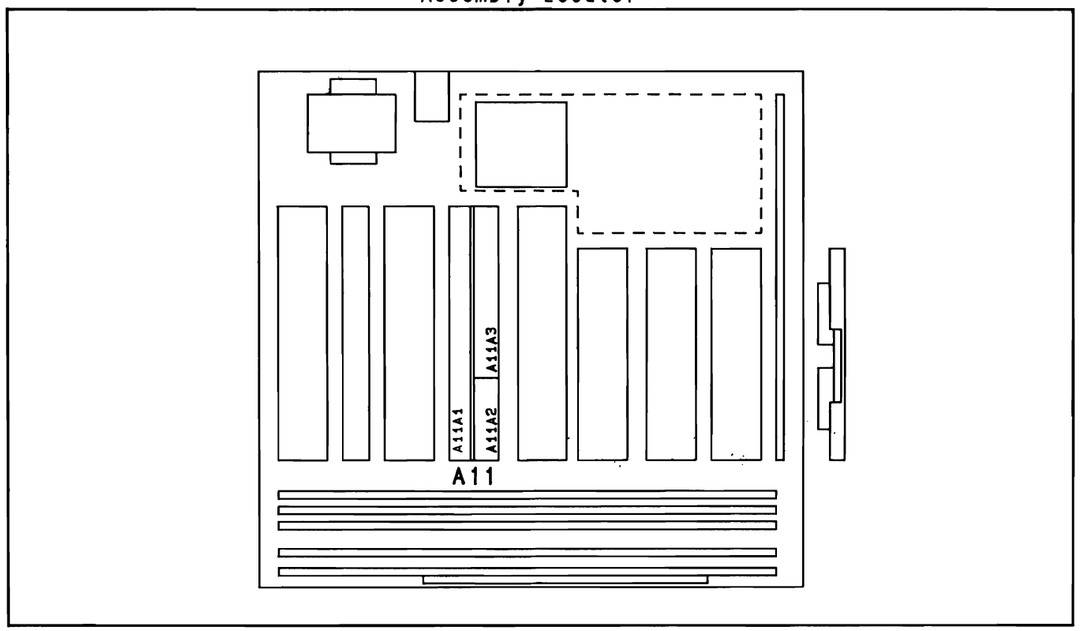
    Key in: [Hz] to end the routine.

    Switch the HP 8642 to Standby.

    Reconnect the A20 module to the rear panel (See Disassembly Procedures).

    Re-install the top cover.

Assembly Locator



Simplified Block Diagram

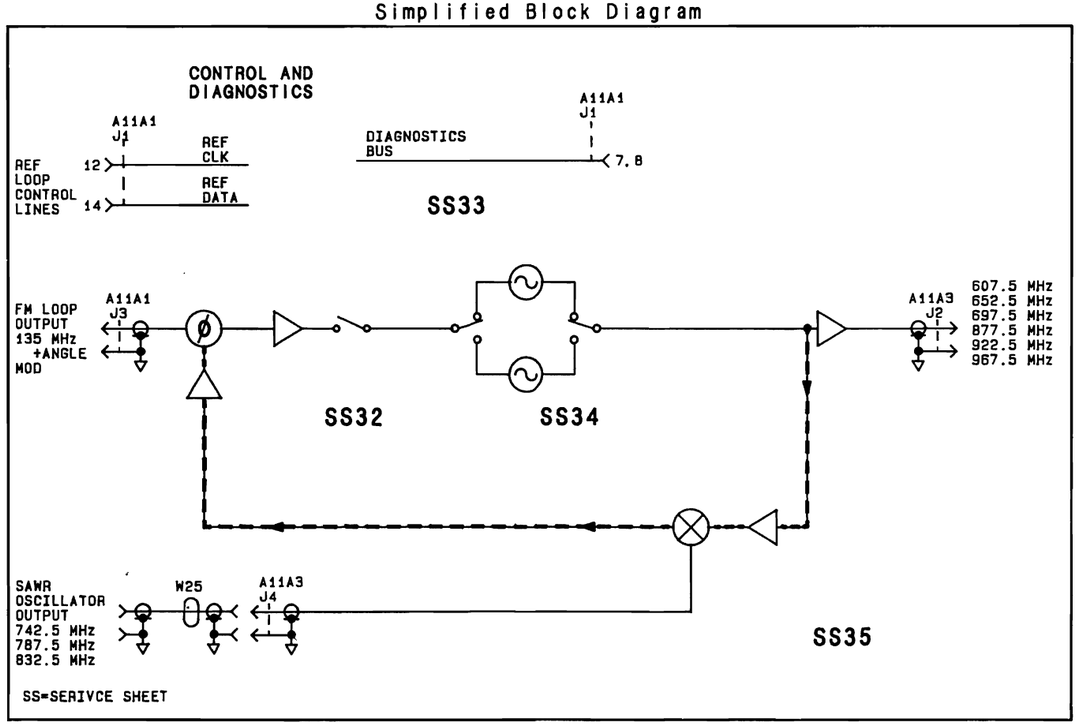
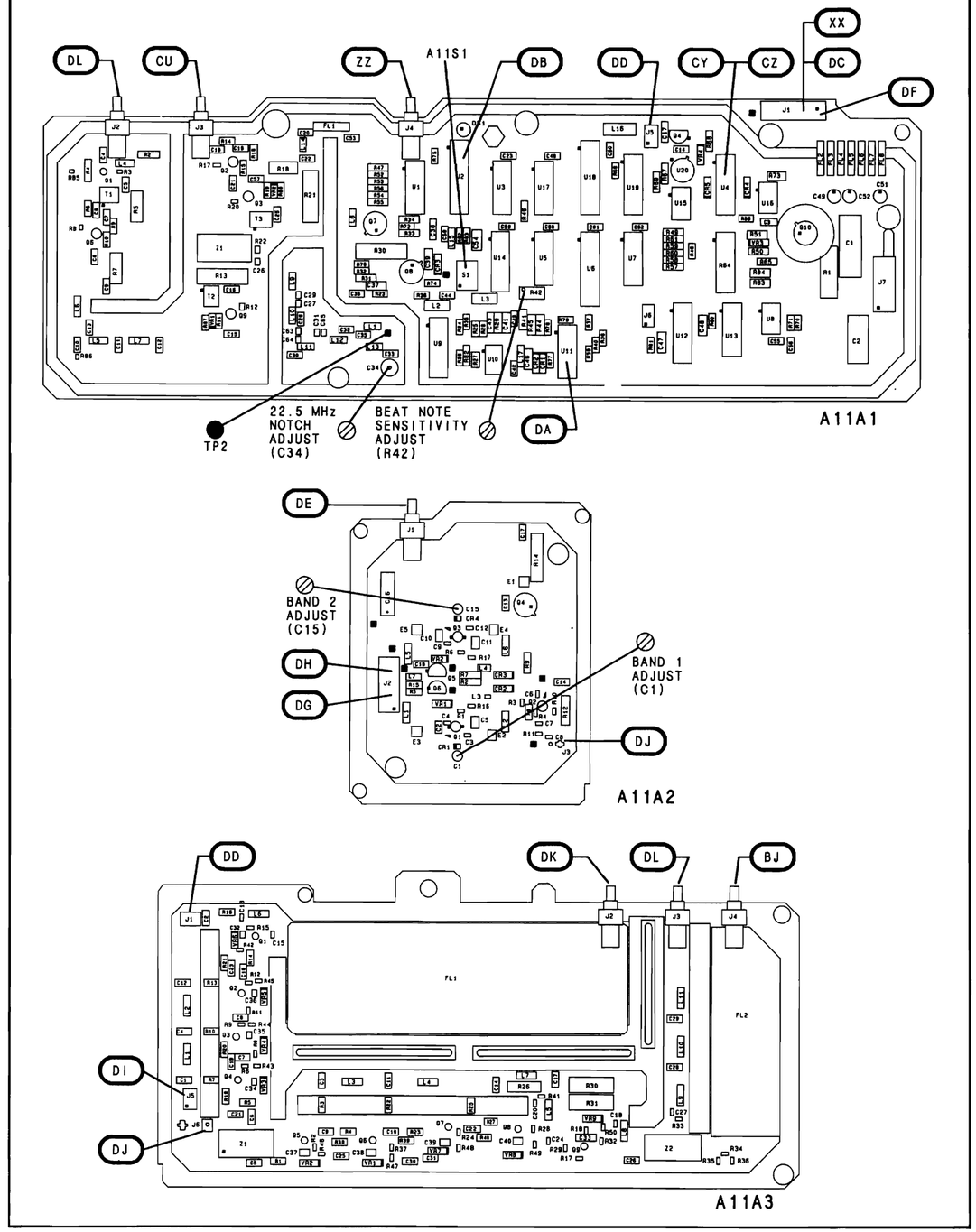


Figure 8N-100 BD11 General Information.

Module Test Point/Adjustment Locations



REF LOOP CONTROL LINES
BD4 DC 2
P/O J1
12 REF CLK
14 REF DATA

SERIAL DATA INTERFACE

U2-6, 9, 12, 15, 16, 19
U18-5, 6, 7, 12, 15, 16, 19
U6-5, 6, 9, 12, 15, 16
U6-2
U6-19

POWER SUPPLY AND GND
+50V (F1)
+15V (F1)
+5V (F1)
+5V (F2)
-15V (F1)
GND
32 CX 6

REFERENCE LOOP OUTPUT LEVEL CONTROL
LEVEL CONTROL
P/O J5 1, 2
P/O 08642-60005

PRETUNE
PRETUNE VOLTAGE
P/O J7 1

OSCILLATOR BAND SELECT
BAND 1
BAND 2
P/O J7 3

+15V (F1) P/O J7 4
GND 7
-15V (F1) 6
8
+15V (F1) P/O J6 1, 2
P/O 08642-60004
+15V (F SUPPLY

OUT-OF-LOCK SENSE
INTEGRATOR OUTPUT SENSE
COMPARATOR OUTPUT SENSE
REFERENCE LOOP DIAGNOSTICS
REF OOL P/O J1 7, 8
SS33
REF LOOP DIAGNOSTICS BUS DF BD4

DB CY CZ DA ZZ

SHAPER SENSE

DE

FM LOOP OUTPUT
BD8 CU W24 935
(0dBm TO 5dBm 135 MHz)
J3

PHASE DETECTOR LO PORT DRIVER
LO PORT Z1-1
PHASE DETECTOR
IF PORT Z1-3, 4
RF PORT Z1-8
REF LOOP FILTER
TP2

DIPLEXERS
INTEGRATOR
LOOP EMITTER FOLLOWER A=1
SHAPER
J4
A11W2 923 0V TO +10.5

FEED FORWARD AMPLIFIER

DL
A11W1 925 REF LOOP IF
(-9dBm TO -12dBm 135 MHz)
J2

REFERENCE LOOP IF AMPLIFIER
2ND IF LOW-PASS FILTER
PHASE DETECTOR RF PORT DRIVER

WINDOW COMPARATOR

1 MHz HIGH-PASS FILTER
BEAT NOTE DETECTOR
SWEEP-TO-LOCK CONTROL
OUT-OF-LOCK

POWER SUPPLY AND GROUND
67 TY 6
P/O J1
5, 6 +50V
9, 10 +15V
1, 3 +5V
15, 16 -15V
2, 4 -5V
11, 13
POWER SUPPLY AND GND
6 CX 33

SS32

SERIL PREFIX: 2427A

08642-60106

A11A3 REFERENCE LOOP P
SPLITTER ASSEMBLY (086

A11A2 REFERENCE LOOP V.C.O. (08642-60107)

P/O 08642-60005

P/O 08642-60004

OUTPUT LEVEL CONTROL

LEVEL CONTROL

PRETUNE VOLTAGE

BAND 1

BAND 2

OSCILLATOR SELECT LINES AND PRETUNE

POWER SUPPLY AND GROUND

+15V (F1)

GND

-15V (F1)

+15V (F2) SUPPLY

REF LOOP DIAGNOSTICS BUS

REF OOL

SS33

REFERENCE LOOP DIAGNOSTICS

SHAPER SENSE

SHAPER

A=1

FORWARD IFIER

OUT-OF-LOCK

SS32

PRETUNE FILTER

VCO SWITCH DRIVE

BUFFER

REF LOOP TUNE VOLTAGE

VCO BAND 1

VCO BAND 2

TP1

TP2

VCO BUFFER

REF LOOP VCO OUTPUT A11W3

POWER SPLITTER

BAND #1
607.5 MHz
652.5 MHz
697.5 MHz

BAND #2
877.5 MHz
922.5 MHz
967.5 MHz

POWER SUPPLY AND GND

+15V (F2)

-15V (F2)

SS34

A11W2

0V TO +10.5V (DC)

POWER SUPPLY AND GND

1ST IF LOW-PASS FILTER

IF PORT Z2-3

REF LOOP IF

A11W1

SAWR OSCILLATOR OUTPUT

BD9

(3.5dBm TO +5dBm)

W25

860 MHz RF FILTER

742.5 MHz
787.5 MHz
832.5 MHz

A11A2 REFERENCE LOOP V.C.O. (08642-60107)

A11A3 REFERENCE LOOP POWER SPLITTER ASSEMBLY (08642-60108)

DD

UTPUT EVEL ONTROL

D6

SCILLATOR ELECT LINES ND PRETUNE

DH

OWER SUPPLY ND GROUND

2)

I

V (DC)

P/O J2

1

PRETUNE VOLTAGE

PRETUNE FILTER

3

BAND 1

VCO SWITCH DRIVE

4

BAND 2

TP2

TP1

VCO BAND 2

VCO BAND 1

VCO BUFFER

J3

REF LOOP VCO OUTPUT A11W3

SR

DJ

J6

BAND #1
607.5 MHz
652.5 MHz
697.5 MHz

BAND #2
877.5 MHz
922.5 MHz
967.5 MHz

J1

REF LOOP TUNE VOLTAGE

BUFFER

P/O J2

7

+15V (F2)

8

-15V (F2)

6

POWER SUPPLY AND GND

SS34

P/O J1

1, 2

POWER SPLITTER

OUTPUT LIMITER/ AMPLIFIER

J2

W31

901

REF LOOP OUTPUT

DK

BD12

(+3dBm ±0.5dB)

P/O J5

1, 2

+15V (F2)

POWER SUPPLY AND GND

REF LOOP IF

A11W1

925

J3

1ST IF LOW-PASS FILTER

IF PORT Z2-3

REFERENCE LOOP MIXER

LO PORT Z2-8

LO LIMITER/ AMPLFILER

RF PORT Z2-1

SAWR OSCILLATOR OUTPUT

BD9

BJ

(3.5dBm TO +5dBm)

W25

937

J4

860 MHz RF FILTER

8dB ATTENUATOR

742.5 MHz
787.5 MHz
832.5 MHz

SS35

BD11

Figure 8N-101

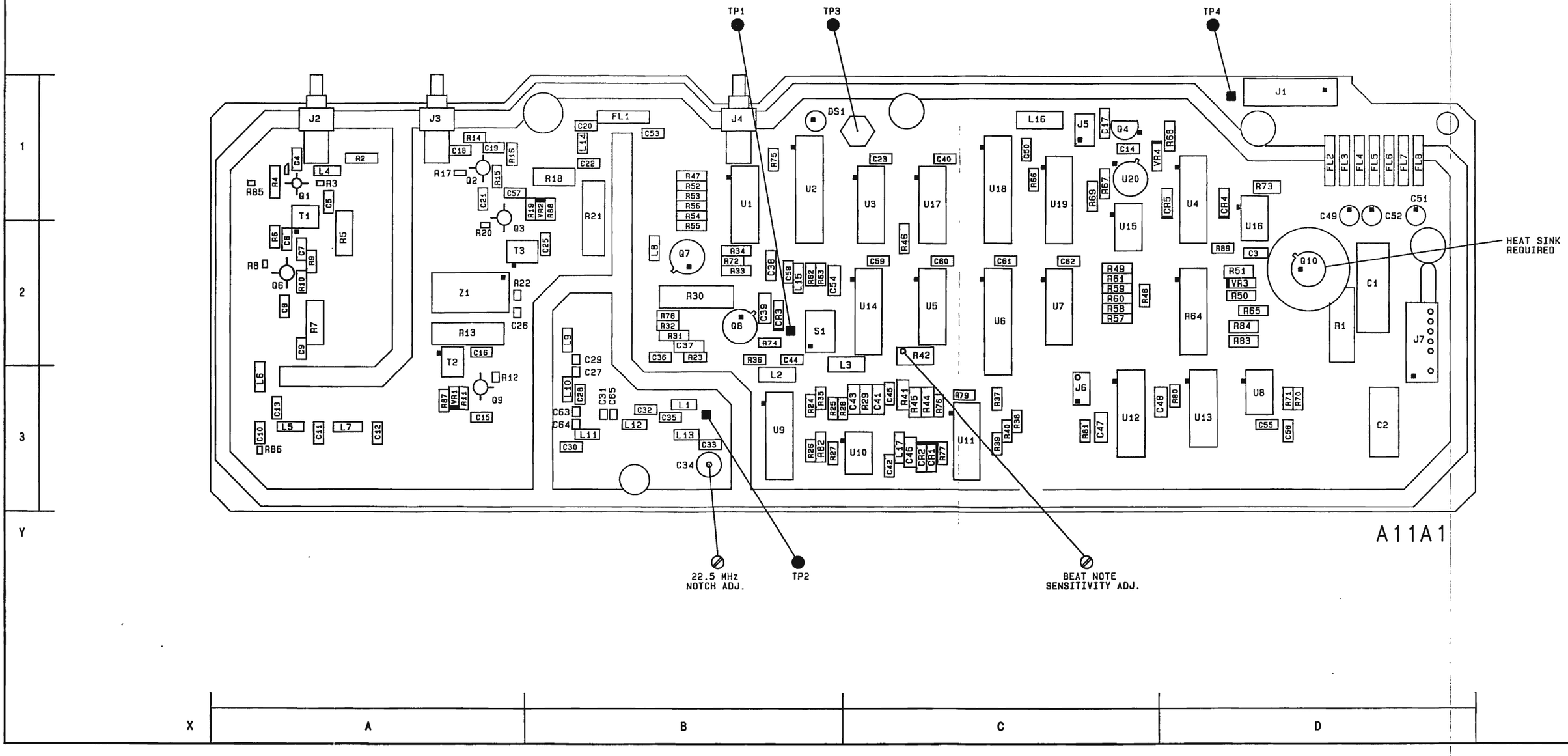
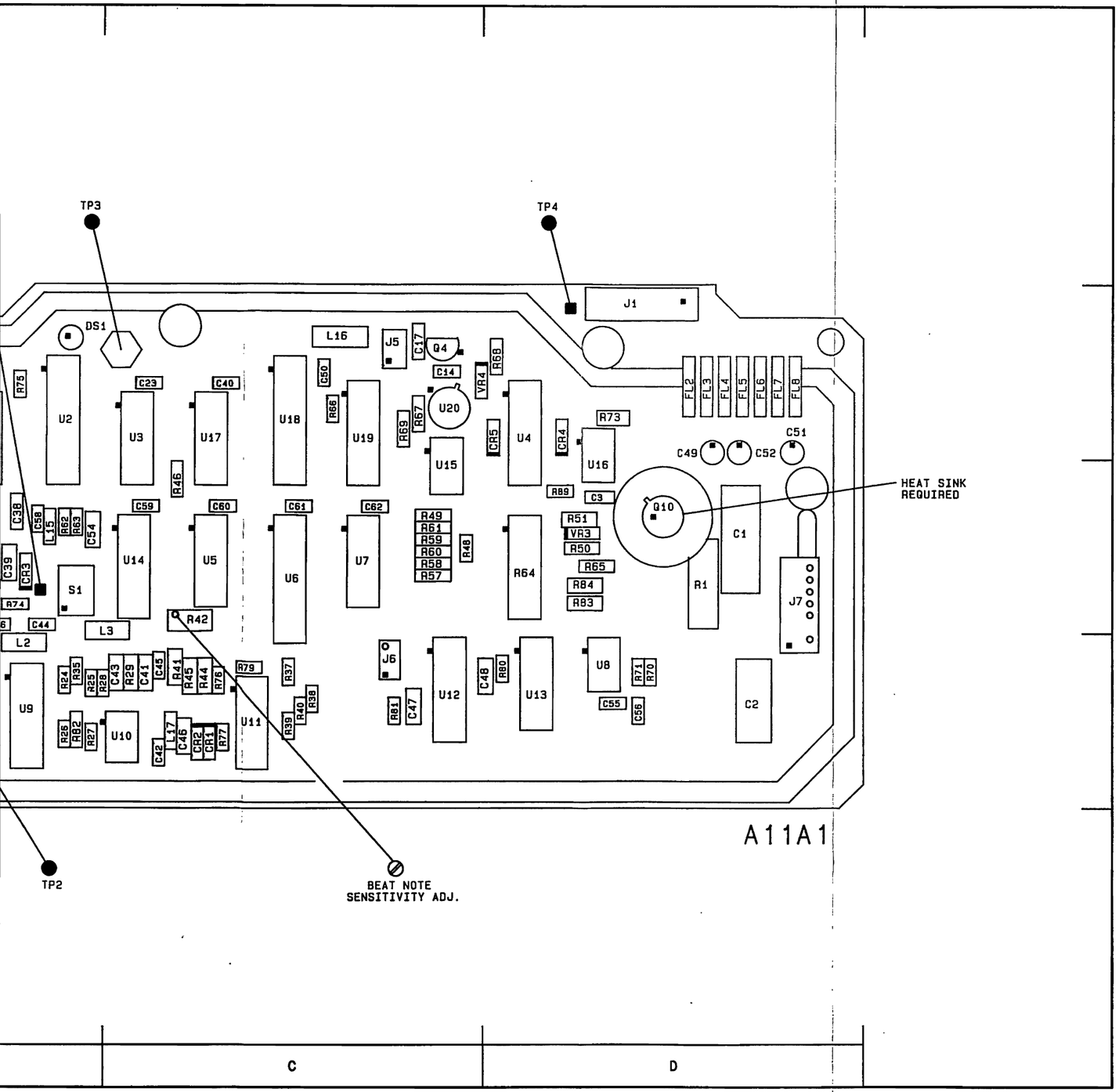
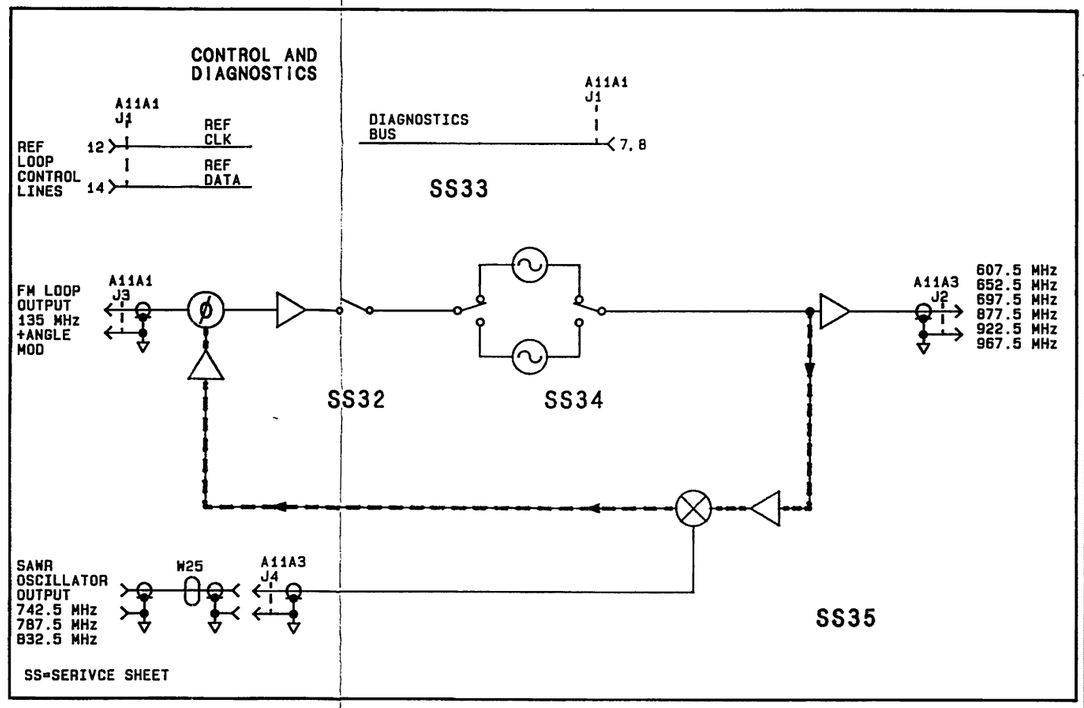


Figure 8N-102. SERVICE SHEET 32 INFORMATION

Component Locator



Component Locator



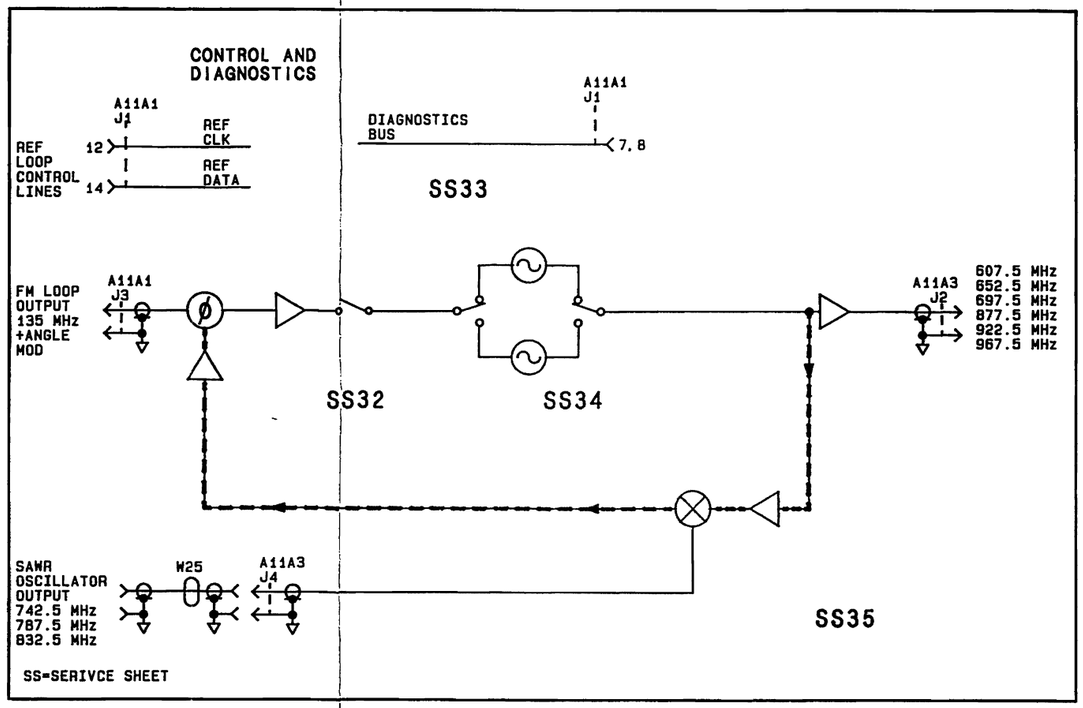
Reference Block Diagram

Component Coordinates

COMP	X,Y
J1	D, 2
C4	A, 1
C5	A, 1
C6	A, 2
C7	A, 2
C8	A, 2
C9	A, 2
C10	A, 3
C11	A, 3
C12	A, 3
C13	A, 3
C15	A, 3
C16	A, 2
C18	A, 1
C19	A, 1
C20	B, 1
C21	A, 1
C22	B, 1
C25	B, 2
C26	A, 2
C27	B, 3
C28	B, 3
C29	B, 2
C30	B, 3
C31	B, 3
C32	B, 3
C33	B, 3
C34	B, 3
C35	B, 3
C36	B, 2
C37	B, 2
C38	B, 2
C39	B, 2
C41	C, 3
C42	C, 3
C43	C, 3
C44	B, 2
C45	C, 3
C46	C, 3
C47	C, 3
C48	D, 3
C49	D, 1
C51	D, 1
C52	D, 1
C53	B, 1
C54	B, 2
C55	D, 3
C56	D, 3
C57	A, 1
C58	B, 2
C63	B, 3
C64	B, 3
C65	B, 3
CR1	C, 3
CR2	C, 3
CR3	B, 2
DS1	B, 1
FL1	B, 1
FL4	D, 1
FL6	D, 1
FL7	D, 1
FL8	D, 1
J1	D, 1
J2	A, 1
J3	A, 1
L1	B, 3
L2	B, 3
L3	B, 3
L4	A, 1
L5	A, 3
L6	A, 3
L7	A, 3
L8	B, 2
L9	B, 2
L10	B, 3
L11	B, 3
L12	B, 3
L13	B, 3
L14	B, 1
L15	B, 2
L17	C, 3
Q1	A, 1
Q2	A, 1
Q3	A, 2
Q6	A, 2
Q7	B, 2
Q8	B, 2
Q9	A, 3
R2	A, 1
R3	A, 1
R4	A, 1
R5	A, 2
R6	A, 2
R7	A, 2
R8	A, 2
R9	A, 2
R10	A, 2
R11	A, 3
R12	A, 3
R13	A, 2
R14	A, 1
R15	A, 1
R16	A, 1
R17	A, 1
R18	B, 1
R19	B, 1
R20	A, 2
R21	B, 1
R22	A, 2
R23	B, 2
R24	B, 3
R25	B, 3
R26	B, 3
R27	B, 3
R28	B, 3
R29	C, 3
R30	B, 2
R31	B, 2
R32	B, 2
R33	B, 2
R34	B, 2
R35	B, 3
R36	B, 2
R37	C, 3
R38	C, 3
R39	C, 3
R40	C, 3
R41	C, 3
R42	C, 2
R44	C, 3
R45	C, 3
R46	C, 2
R47	B, 1
R52	B, 1
R53	B, 1
R54	B, 1
R55	B, 2
R56	B, 1
R62	B, 2
R63	B, 2
R70	D, 3
R71	D, 3
R72	B, 2
R74	B, 2
R76	C, 3
R77	C, 3
R78	B, 2
R79	C, 3
R80	D, 3
R81	C, 3
R82	B, 3
R85	A, 1
R86	A, 3
R87	A, 3
R88	B, 1
S1	B, 2
T1	A, 1
T2	A, 2
T3	A, 2
TP1	B, 2
TP2	B, 3
TP3	C, 1
U1	B, 1
U8	D, 3
U9	B, 3
U10	C, 3
U11	C, 3
U12	C, 3
U13	D, 3
VR1	A, 3
VR2	B, 1
Z1	A, 2

A11 MODULE **BD11**

SEE REVERSE SIDE



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	D, 2	C45	C, 3	L1	B, 3	R2	A, 1	R39	C, 3	S1	B, 2						
C4	A, 1	C46	C, 3	L2	B, 3	R3	A, 1	R40	C, 3								
C5	A, 1	C47	C, 3	L3	B, 3	R4	A, 1	R41	C, 3	T1	A, 1						
C6	A, 2	C48	D, 3	L4	A, 1	R5	A, 2	R42	C, 2	T2	A, 2						
C7	A, 2	C49	D, 1	L5	A, 3	R6	A, 2	R44	C, 3	T3	A, 2						
C8	A, 2	C51	D, 1	L6	A, 3	R7	A, 2	R45	C, 3								
C9	A, 2	C52	D, 1	L7	A, 3	R8	A, 2	R46	C, 2	TP1	B, 2						
C10	A, 3	C53	B, 1	L8	B, 2	R9	A, 2	R47	B, 1	TP2	B, 3						
C11	A, 3	C54	B, 2	L9	B, 2	R10	A, 2	R52	B, 1	TP3	C, 1						
C12	A, 3	C55	D, 3	L10	B, 3	R11	A, 3	R53	B, 1								
C13	A, 3	C56	D, 3	L11	B, 3	R12	A, 3	R54	B, 1	U1	B, 1						
C15	A, 3	C57	A, 1	L12	B, 3	R13	A, 2	R55	B, 2	U8	D, 3						
C16	A, 2	C58	B, 2	L13	B, 3	R14	A, 1	R56	B, 1	U9	B, 3						
C18	A, 1	C63	B, 3	L14	B, 1	R15	A, 1	R62	B, 2	U10	C, 3						
C19	A, 1	C64	B, 3	L15	B, 2	R16	A, 1	R63	B, 2	U11	C, 3						
C20	B, 1	C65	B, 3	L17	C, 3	R17	A, 1	R70	D, 3	U12	C, 3						
C21	A, 1					R18	B, 1	R71	D, 3	U13	D, 3						
C22	B, 1	CR1	C, 3	Q1	A, 1	R19	B, 1	R72	B, 2								
C25	B, 2	CR2	C, 3	Q2	A, 1	R20	A, 2	R74	B, 2	VR1	A, 3						
C26	A, 2	CR3	B, 2	Q3	A, 2	R21	B, 1	R76	C, 3	VR2	B, 1						
C27	B, 3			Q6	A, 2	R22	A, 2	R77	C, 3								
C28	B, 3	DS1	B, 1	Q7	B, 2	R23	B, 2	R78	B, 2	Z1	A, 2						
C29	B, 2			Q8	B, 2	R24	B, 3	R79	C, 3								
C30	B, 3	FL1	B, 1	Q9	A, 3	R25	B, 3	R80	D, 3								
C31	B, 3	FL4	D, 1			R26	B, 3	R81	C, 3								
C32	B, 3	FL6	D, 1			R27	B, 3	R82	B, 3								
C33	B, 3	FL7	D, 1			R28	B, 3	R85	A, 1								
C34	B, 3	FL8	D, 1			R29	C, 3	R86	A, 3								
C35	B, 3					R30	B, 2	R87	A, 3								
C36	B, 2	J1	D, 1			R31	B, 2	R88	B, 1								
C37	B, 2	J2	A, 1			R32	B, 2										
C38	B, 2	J3	A, 1			R33	B, 2										
C39	B, 2					R34	B, 2										
C41	C, 3					R35	B, 3										
C42	C, 3					R36	B, 2										
C43	C, 3					R37	C, 3										
C44	B, 2					R38	C, 3										

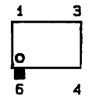
A11 MODULE **BD11**

SEE REVERSE SIDE

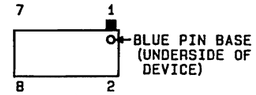
Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. Feedthrough filter outer body must be soldered to the shielding in the area where shielding is notched.
3. Test point requres high impedance (>500 Ω) probe. See Bench Service Kit (HP part number 11802A).
4. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

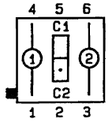
A11A1 T1,T2,T3 TOP VIEW



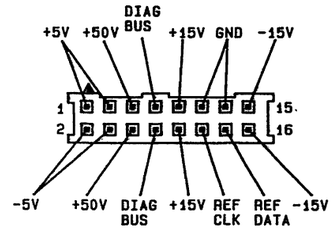
A11A1 Z1 TOP VIEW



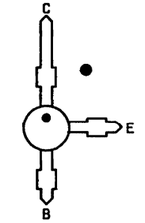
A11A1 S1 TOP VIEW



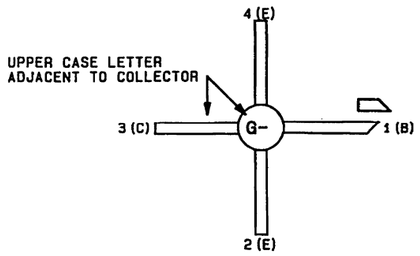
CABLE PLUG TO A11A1 J1



A11A1 Q2,Q3,Q6,Q9



A11A1 Q1



Schematic General Information

CHANGES

2736A and above

On the schematic:

- C33, C34 - In **REFERENCE LOOP FILTERS**, change the value of C33 to 36p and C34 to 6.0 - 22.0p.

P/O A11A1 REFERENCE LOOP PHASE DETECTOR AND INTEGRATOR (08642-60106)

PHASE DETECTOR LO PORT DRIVER

+15V (F3)
R21 261
4:1 IMPEDANCE TRANSFORMER
T3
+15V (F3)
R18 383
C25 1000p
NC
R19 619
R15 215
VR2 5.2V
C57 0.1μ
C19 0.1μ
R16 2370
R88 422
C18 1000p
C21 1000p
Q2
Q3
R20 12
R14 511
R17 12

FM LOOP OUTPUT (135 MHz 2.4 dBm)
23 CU W24 935
J3

PHASE DETECTOR

Z1
MIXER
LO 1
3, 4 IF
8
2, 5, 6, 7
RF

REFERENCE LOOP FILTERS

LOW-PASS FILTER
NOTCH FILTER
C28 10.1p
C30 5.6p
C32 470p
C35 470p
L9 100n
L10 180n
L11 180n
L12 120n
L1 120n
C26 47p
C29 47p
C27 33p
C63 47p
C64 47p
C65 33p
C31 22p
L13 1μ
C33 47p
C34 3.5-10p
22.5 MHz NOTCH ADJ.
R22 50

DIPLEXERS

L2 8.2 μ
R35 51.
TP2 (NO
R23 51.1
C36 3300p

REFERENCE LOOP IF AMPLIFIER

+15V (F4)
4:1 IMPEDANCE TRANSORMER
T1
R5 383
C5 1000p
NC
R4 619
C6 0.1μ
C7 0.1μ
R10 162
R7 383
R9 2370
C8 1000p
Q6
R6 511
R8 12
Q1
C4 1000p
L4 1 μ
R2 82.5
R85 12
R3 12

REFERENCE LOOP IF A11W1
35 DL 925
J2

2ND IF LOW-PASS FILTER

L5 82n
L7 82n
C10 24p
R86 50
C11 42p
C12 24p

PHASE DETECTOR RF PORT DRIVER

+15V (F2)
4:1 IMPEDENCE TRANSFORMER
R13 261
T2
C16 1000p
NC
R11 619
VR1 5.2V
R87 422
C15 0.1μ
Q9
R12 12

WINDOW COMPARATOR

+15V (F1)
R40 3160
R39 10k
U11C
U11D
+5V (F1)
R79 6810
COMPARATOR OUTPUT SENSE
CY 33
R38 1960

SWEEP-TO-L

P/O POWER SUPPLIES AND GND

P/O J1
+50V
FL7
C1 10 μ
+50V (F1)
+15V (F1)
5, 6
+15V
FL6
C52 10 μ
FL1
C53 0.01μ
C20 0.01μ
L14 3μ
C22 0.01
L6 1μ
C13 0.01μ
C9 0.01μ
+15V (F1)
+15V (F2)
+15V (F3)
+15V (F4)
9, 10
-5V
NC
2, 4
POWER SUPPLY AND GROUND
67 TY 6
+5V
FL8
C51 10 μ
R46 1k
+5V (F2)
+5V (F1)
1, 3
-15V
FL4
C49 10 μ
-15V (F1)
15, 16
GND
11, 13
POWER SUPPLY AND GND
6 CX 33

1 MHz HIGH PASS FILTER

R36 511
C44 100p
C45 100p
L3 56μ

BEAT NOTE DETECTOR

+15V (F1)
R41 14.7k
BEAT NOTE SENSITIVITY ADJ.
R42 500
CW
CR1
+5V (F1)
R76 6810
R44 681k
-15V (F1)
L17 56μ
CR2
R77 6810
C46 1000p
R45 681k
U11A
3, 7
6, 12

U13A

SERIAL PREFIX: 2427A

FERENCE LOOP FILTERS

LOW-PASS FILTER — NOTCH FILTER

C28 10.1p, C30 5.6p, C32 470p, C35 470p

L9 100n, L10 180n, L11 180n, L12 120n, L1 120n

C26 47p, C29 47p, C27 33p, C63 47p, C64 47p, C65 33p, C31 22p

R22 50

L13 1μ

C33 47p

C34 3.5-10p

22.5 MHz NOTCH ADJ.

DIPLEXERS

L2 8.2μ

R35 51.1

TP2 (NOTE 3)

R23 51.1

C36 3300p

INTEGRATOR (DC TO 20 kHz)

RAMP DOWN SWITCH

U9D

R24 68.1k

+15V (F1)

R28 1k

C43 0.01μ

R25 1210

U10

R29 1k

+15V (F1)

R82 1M

R27 1210

C42 22p

-15V (F1)

C41 0.01μ

RAMP UP SWITCH

+15V (F1)

U9C

R26 68.1k

-15V (F1)

LOOP EMITTER FOLLOWER

R37 6810

OPEN LOOP SWITCH

CLOSED LOOP

OPEN LOOP

S1A

TP1

CR3

+15V (F1)

R62 1k

R63 1k

TP3

C54 0.1μ

CTOR RF PORT

4:1 IMPEDENCE TRANSFORMER

T2

NC

R13 261

R11 619

C15 0.1μ

Q9

R12 12

WINDOW COMPARATOR

+15V (F1)

R40 3160

U11C

R39 10k

U11D

R38 1960

+5V (F1)

R79 6810

COMPARATOR OUTPUT SENSE

CY 33

SWEEP-TO-LOCK CONTROL

RAMP DOWN

RAMP UP

SWEEP TIMER

U8

C55 0.01μ

R71 5110

R70 5110

C56 0.01μ

+5V (F1)

U13F

U13A

U13B

+5V (F1)

U12A

+VCC

C EXT

R EXT/C EXT

R80 31.6k

C48 0.1μ

NC

+5V (F2)

U12B

R81 31.6k

C47 0.1μ

FEED FORWARD A (10 kHz TO 100

C37 0.1μ

R32 10k

-15V (F1)

OUT-OF-LOCK

OUT-OF-LOCK INDICATOR

+5V (F1)

DS1

BEAT NOTE DETECTOR

+15V (F1)

R41 14.7k

BEAT NOTE SENSITIVITY ADJ.

R42 500

CW

CR1

R76 6810

R44 681k

-15V (F1)

+5V (F1)

L17 56μ

CR2

R77 6810

C46 1000p

R45 681k

-15V (F1)

U11A

MHz HIGH ASS FILTER

R36 511

C44 100p

C45 100p

L3 56μ

INTEGRATOR (DC TO 20 kHz)

RAMP DOWN SWITCH

U9D

R24 68.1k

+15V (F1)

R28 1k

C43 0.01µ

U10

R25 1210

R29 1k

R82 1M

R27 1210

C42 22p

C41 0.01µ

-15V (F1)

RAMP UP SWITCH

U9C

R26 68.1k

LOOP EMITTER FOLLOWER

OPEN LOOP SWITCH

CLOSED LOOP

OPEN LOOP

S1A

TP1

R37 6810

R74 51.1

CR3

Q8

C39 0.1µ

R62 1k

R63 1k

C54 0.1µ

TP3

R30 147

L8 1µ

INTEGRATOR OUTPUT SENSE DA 33

SHAPER

DAC

U1A

U1F

U1B

U1C

U1D

U1E

R47 100

R52 200

R53 400

R54 800

R55 1600

R56 3200

SHAPER DATA 33 DB 6

J4

A11 W2

923

SHAPER SENSE ZZ 33

REF LOOP TUNE VOLTAGE DE 34

FEED FORWARD AMPLIFIER (10 kHz TO 100 MHz)

C37 0.1µ

R31 10

Q7

PHASE COMPENSATION

R72 56.2

C58 150p

L15 820n

R32 10k

R78 5110

R34 100

C38 1µ

R33 909

CONTROL

RAMP DOWN

RAMP UP

SWEEP TIMER

U12A

U12B

+VCC

C EXT

R EXT/C EXT

NC

R80 31.6k

C48 0.1µ

R81 31.6k

C47 0.1µ

U13F

Vcc

R71 5110

R70 5110

C56 0.01µ

+5V (F2)

OUT-OF-LOCK

OUT-OF-LOCK INDICATOR

OPEN LOOP SWITCH

DS1

CLOSED LOOP

OPEN LOOP

S1B

OUT-OF-LOCK SENSE CZ 33

ATTENTION
Static Sensitive Devices

SS32
Figure 8N-103
8N-103

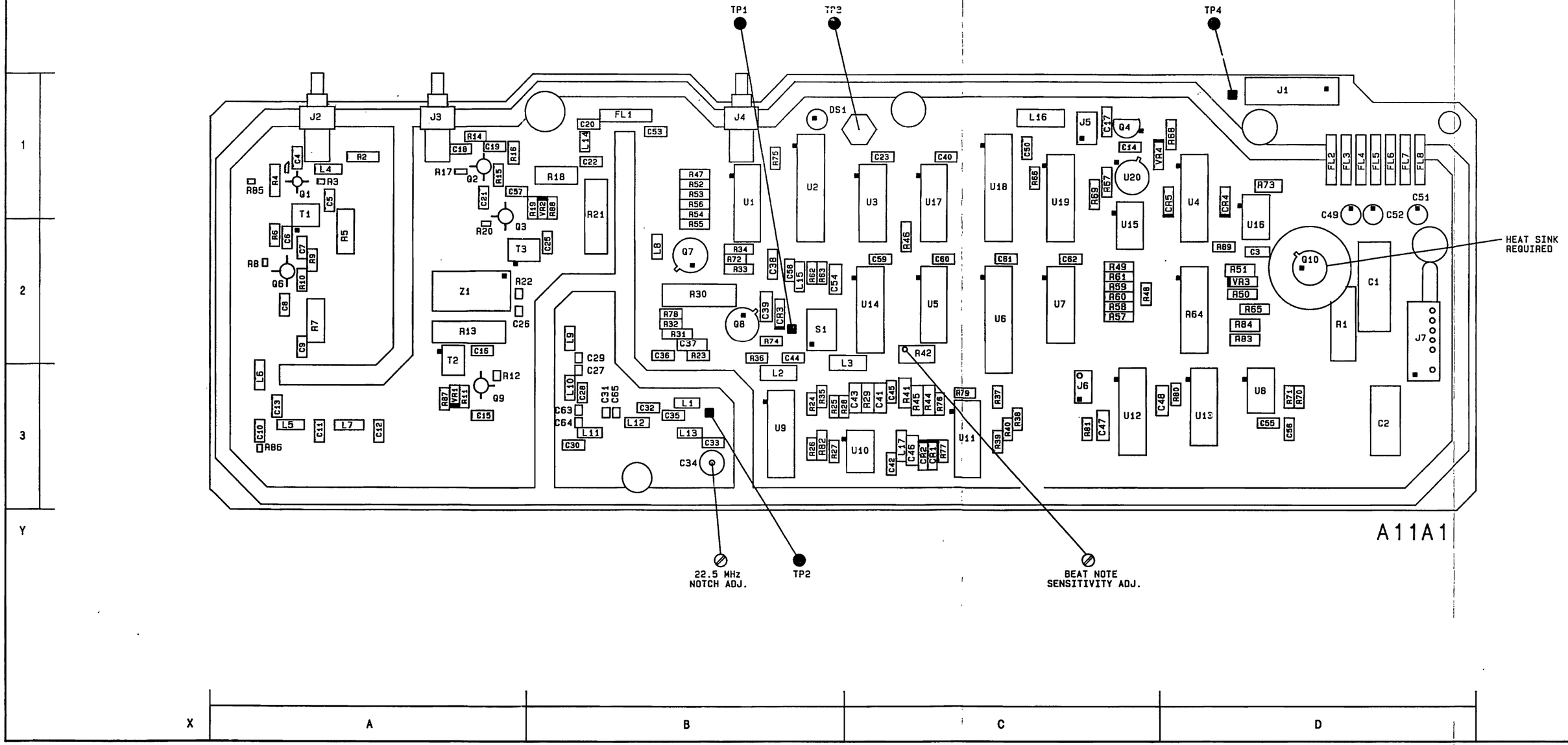
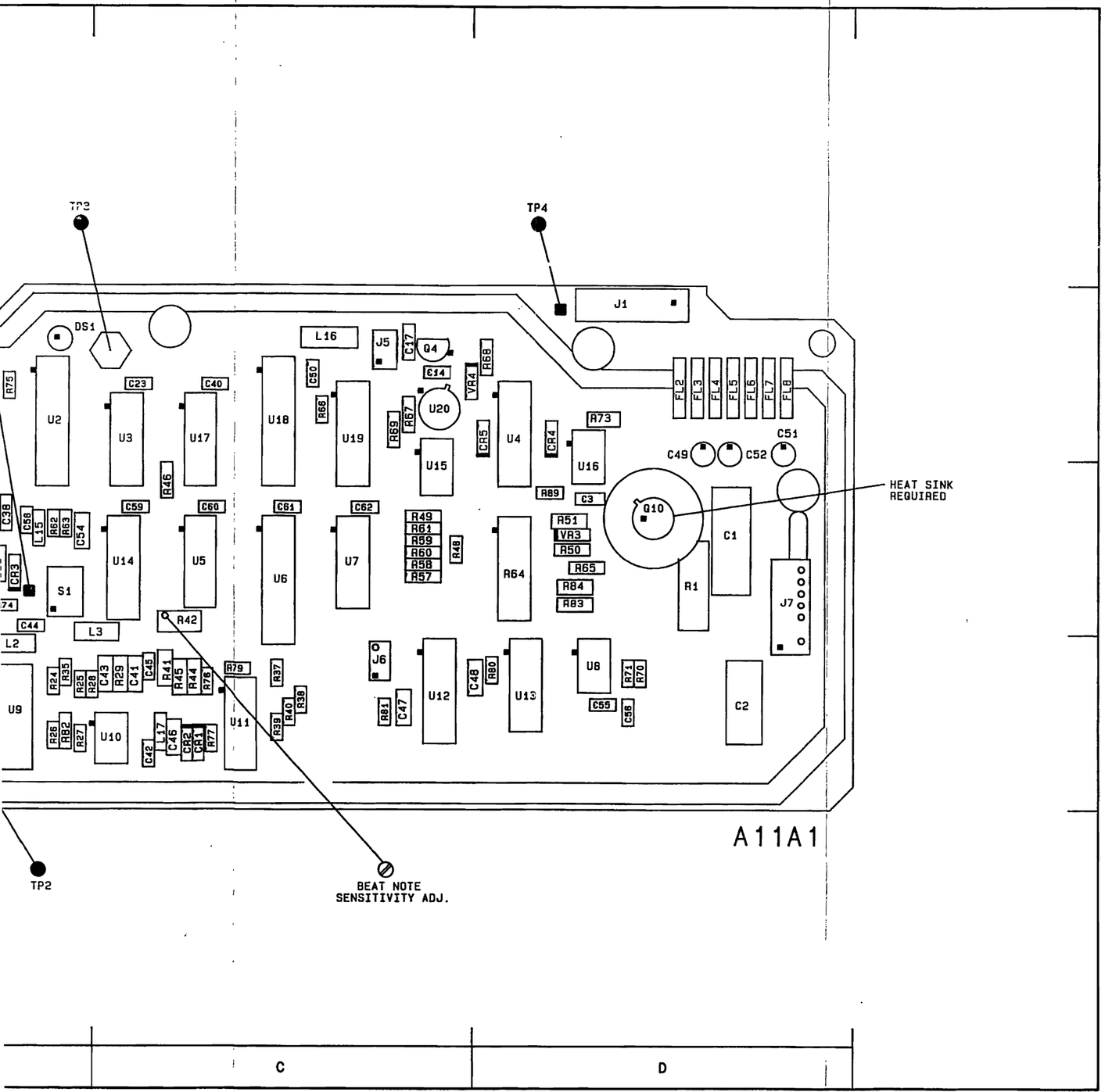
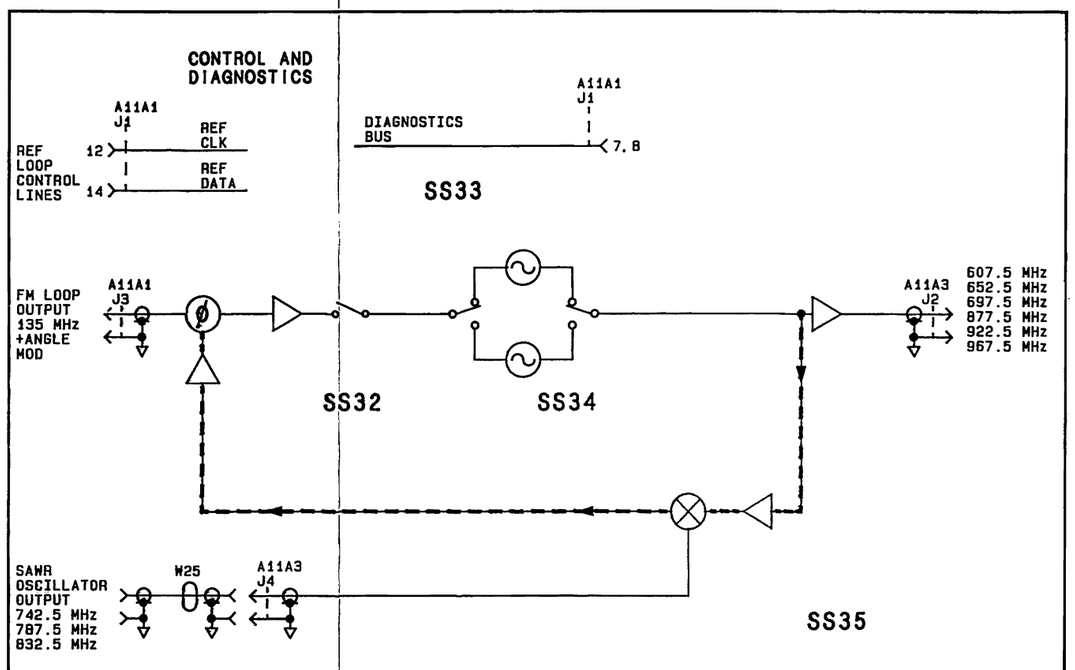


Figure 8N-104. SERVICE SHEET 33 INFORMATION

Component Locator



Component Locator



Reference Block Diagram

Component Coordinates

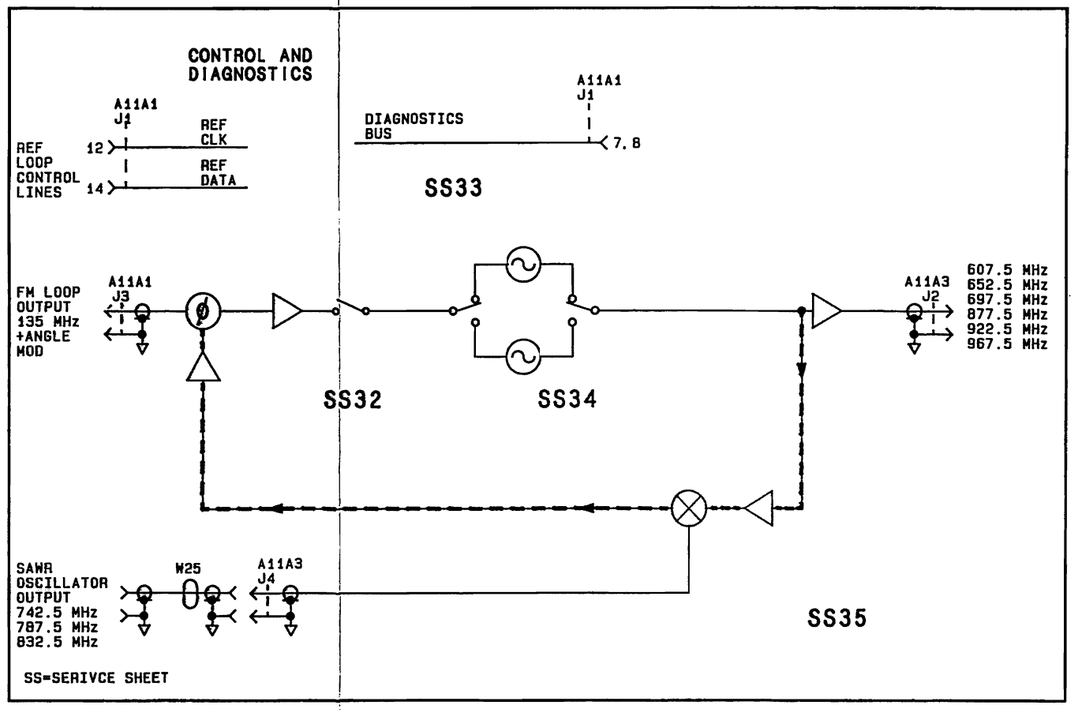
COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C2	D, 3	R1	D, 2	U2	B, 1										
C3	D, 2	R48	C, 2	U3	C, 1										
C14	C, 1	R49	C, 2	U4	D, 1										
C17	C, 1	R50	D, 2	U5	C, 2										
C23	C, 1	R51	D, 2	U6	C, 2										
C40	C, 1	R57	C, 2	U7	C, 2										
C50	C, 1	R58	C, 2	U13	D, 3										
C59	C, 2	R59	C, 2	U14	C, 2										
C60	C, 2	R60	C, 2	U15	C, 2										
C61	C, 2	R61	C, 2	U16	D, 2										
C62	C, 2	R64	D, 2	U17	C, 1										
		R65	D, 2	U18	C, 1										
CR4	D, 1	R66	C, 1	U19	C, 1										
CR5	D, 1	R67	C, 1	U20	C, 1										
		R68	D, 1												
FL2	D, 1	R69	C, 1	VR3	D, 2										
FL3	D, 1	R73	D, 1	VR4	C, 1										
FL5	D, 1	R75	B, 1												
		R83	D, 2												
J1	D, 1	R84	D, 2												
J4	B, 1	R89	D, 2												
J5	C, 1														
J6	C, 3	TP4	D, 1												
J7	D, 2														
L16	C, 1														
Q4	C, 1														
Q10	D, 2														

P/O A11A1

SEE REVERSE SIDE

REFERENCE LOOP PHASE DETECTOR AND INTEGRATOR

SS32



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C2	D, 3	R1	D, 2	U2	B, 1												
C3	D, 2	R48	C, 2	U3	C, 1												
C14	C, 1	R49	C, 2	U4	D, 1												
C17	C, 1	R50	D, 2	U5	C, 2												
C23	C, 1	R51	D, 2	U6	C, 2												
C40	C, 1	R57	C, 2	U7	C, 2												
C50	C, 1	R58	C, 2	U13	D, 3												
C59	C, 2	R59	C, 2	U14	C, 2												
C60	C, 2	R60	C, 2	U15	C, 2												
C61	C, 2	R61	C, 2	U16	D, 2												
C62	C, 2	R64	D, 2	U17	C, 1												
		R65	D, 2	U18	C, 1												
CR4	D, 1	R66	C, 1	U19	C, 1												
CR5	D, 1	R67	C, 1	U20	C, 1												
		R68	D, 1														
FL2	D, 1	R69	C, 1	VR3	D, 2												
FL3	D, 1	R73	D, 1	VR4	C, 1												
FL5	D, 1	R75	B, 1														
		R83	D, 2														
J1	D, 1	R84	D, 2														
J4	B, 1	R89	D, 2														
J5	C, 1																
J6	C, 3	TP4	D, 1														
J7	D, 2																
L16	C, 1																
Q4	C, 1																
Q10	D, 2																

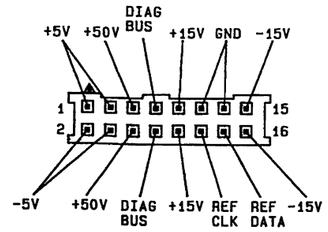
P/O A11A1 REFERENCE LOOP PHASE DETECTOR AND INTEGRATOR **SS32**

SEE REVERSE SIDE

Notes:

1. Each module in the HP 8642 has a nine digit module idenfification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. Feedthrough filter outer body must be soldered to the shielding in the area where shielding is notched.
3. A11 FL1 is an array of feed through filters passing through the center of the module to make connections between two (2) printed circuit boards.
4. A11 FL2, A11 FL3 are low pass feedthrough filters passing through the center of the module to make connections between two (2) printed circuit boards.
5. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

CABLE PLUG
TO A11A1 J1



CHANGES

All serial prefixes

On the schematic:

- VR3 - In **PRETUNE**, locate VR3 and change the value to 12.1 ohm. Change the symbol to a zerner diode symbol.

P/O A11A1 REFERENCE LOOP PHASE DETECTOR AND INTEGRATOR (08642-60106)

P/O A5 DISTRIBUTION ASSY SS67

REF LOOP CONTOL LINES 11 DC

P/O J1 12 REF CLOCK

P/O J1 14 REF DATA

SERIAL DATA INTERFACE

FL3 (NOTE 2)

FL2 (NOTE 2)

U13D

U13E

+5V (F1)

+5V (F2)

U3

U2

U17

U18

U5

U6

U14A

U14B

C23 0.1µ

C40 0.1µ

C50 0.1µ

C60 0.1µ

C61 0.1µ

C59 0.1µ

SHAPER DATA DB 32

SB5

SB4

SB3

SB2

SB1

SB0

SEL 0

SEL 1

SEL 2

DAC6

DAC5

DAC4

DAC3

DAC2

DAC1

DAC0

BAND 2

BAND 1

PT5

PT4

PT3

PT2

PT1

PT0

NC

PRETUNE

U7A

U7D

U7C

U7B

U7F

C62 0.1µ

POWER SUPPLY AND GND

POWER SUPPLY AND GND 32 CX

+50V (F1)

+15V (F1)

+15V (F1)

+5V (F2)

+5V (F1)

-15V (F1)

-15V (F1)

GND

SERIAL PREFIX: 2427A

REFERENCE LOOP OUTPUT LEVEL CONTROL

U19 [D/A CONV.] (CMOS)

+15V (F1)

DAC0
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6

+5V (F2)

[V REF±]
[R FB]

R66 10k

-15V (F1)

[Io1]
[Io2]

C14 100p

U20

+15V (F1)

-15V (F1)

VR4 5.2V

R68 2150

R69 147

Q4

R67 10k

C17 1/1

L16 1m

LEVEL CONTROL J5

P/O (08

SHAPER DATA DB 32

19 SB5
16 SB4
15 SB3
12 SB2
9 SB1
6 SB0
5 SEL 0
2 SEL 1
2 SEL 2
19 DAC6
16 DAC5
6 DAC4
9 DAC3
12 DAC2
15 DAC1
5 DAC0

+5V (F1)

C50 0.1/1

C61 0.1/1

19 BAND 2
2 BAND 1
5 PT5
12 PT4
9 PT3
6 PT2
15 PT1
16 PT0

PRETUNE DAC

U7A +5V (F1)

C62 0.1/1

PT5 R49 1k
PT4 U7D R57 2k
PT3 U7C R58 4k
PT2 U7B R59 8k
PT1 U7E R60 16k
PT0 U7F R61 32k

R48 511

R64F 100k

+50V (F1)

R1 6810

C2 0.1/1

R65 1M

R64B 100k
R64C 100k
R64D 100k

+15V (F1)

R50 1210
R51 100k
C3 1/1
VR3 6.2V

U16B

Q10

OUT-OF-LOCK SENSE 32 CZ

SHAPER SENSE 32 ZZ

INTEGRATOR OUTPUT SENSE 32 DA

COMPARATOR OUTPUT SENSE 32 CY

REFERENCE LOOP DIAGNOSTICS

+15V (F1)

CR4

+5V (F2)

U4 MUX

SEL 0
SEL 1
SEL 2

R75 100k
R64E 100k
R64A 100k

R89 100k

GND V-

CR5

-15V (F1)

U16A

R73 1k

FL5

TP4

P/O J1

7, 8

OSCILLATOR BAND SELECT

U15A +5V (F1)

R84 10k

BAND 1

U15B +5V (F1)

R83 10k

BAND 2

U14B

S
1J
C1
1K
R

NC

P/O J7

BAND 1
BAND 2
PRETUNE VOLTAGE
+15V (F1)
-15V (F1)
GND

P/O J6

+15V (F1)

ATTENTION
Static Sensitive
Devices

REFERENCE LOOP OUTPUT LEVEL CONTROL

U19 [D/A CONV.] (CMOS)
+15V (F1)
DAC0
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
+5V (F2)
A 0/511
[Io1]
[Io2]
[V REF±]
[R FB]
R66 10k
-15V (F1)
C14 100p
U20
VR4 5.2V
R68 2150
Q4
R69 147
R67 10k
C17 1/1
L16 1m
LEVEL CONTROL
J5
P/O (08642-60004)
A11FL2 (NOTE 4)
OUTPUT LEVEL CONTROL
DD 35

REFERENCE LOOP DIAGNOSTICS

U4
+5V (F2)
+15V (F1)
CR4
V+ MUX
SEL 0
SEL 1
SEL 2
A 0/7
GND
V-
CR5
-15V (F1)
R89 100k
OUT-OF-LOCK SENSE
32 CZ
SHAPER SENSE
32 ZZ
INTEGRATOR OUTPUT SENSE
32 DA
COMPARATOR OUTPUT SENSE
32 CY
R75 100k
R64E 100k
R64A 100k
U16A
R73 1k
FL5
TP4
P/O J1
7, 8
DISTRIBUTION ASSY SS67
P/O A5
REFERENCE LOOP DIAGNOSTICS BUS
DF 9

OSCILLATOR BAND SELECT

U15A
U15B
+5V (F1)
+15V (F1)
R84 10k
R83 10k
BAND 1
BAND 2

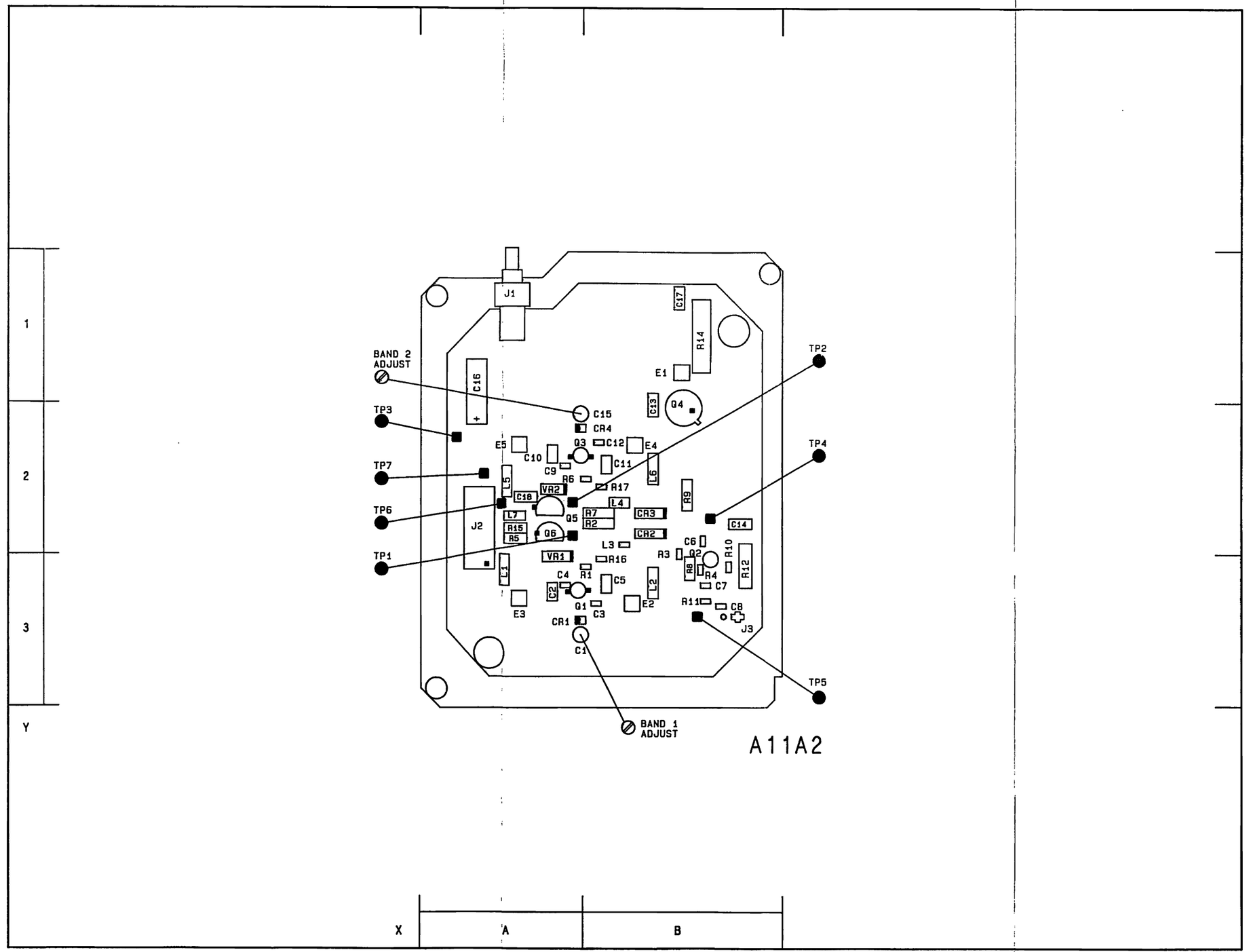
P/O (08642-60004)

P/O J7
A11FL1 (NOTE 3)
BAND 1
BAND 2
PRETUNE VOLTAGE
+15V (F1)
-15V (F1)
GND
OSCILLATOR SELECT LINES AND PRETUNE
D6 34
+15V (F2)
POWER SUPPLY AND GROUND
DH 34
P/O J6
A11FL3 (NOTE 4)
+15V (F2) SUPPLY
DI 35

ATTENTION
Static Sensitive Devices

U16B
+50V (F1)
R1 6810
C2 0.1µ
R65 1M
R64B 100k
R64C 100k
R64D 100k
R64F 100k
R50 1210
R51 100k
C3 1/1
VR3 6.2V
Q10
R48 511

SS33
Figure 8N-105
8N-105



1

2

3

Y

X A B

REF LOOP CONTROL LINES 12 14 A1 J1

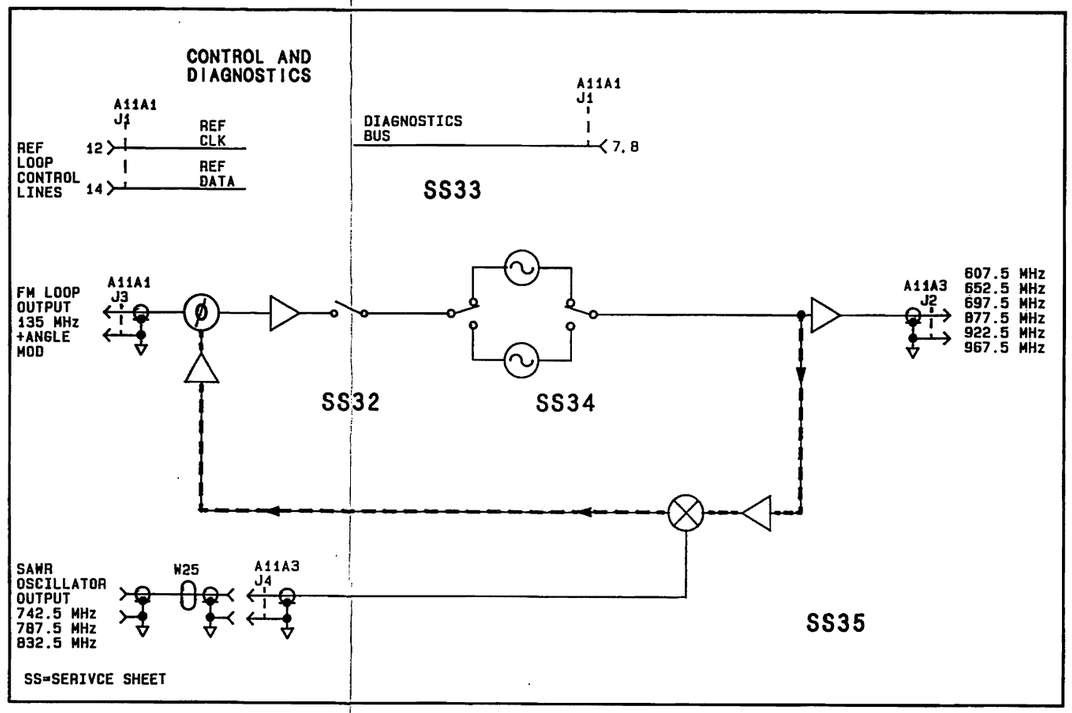
FM LOOP OUTPUT 135 MHz +ANGLE MOD A11 J3

SAWR OSCILLATOR OUTPUT 742.5 MHz 787.5 MHz 832.5 MHz

SS=SERIVCE S

COMP	X,Y
C1	A,3
C2	A,3
C3	B,3
C4	A,3
C5	B,3
C6	B,2
C7	B,3
C8	B,3
C9	A,2
C10	A,2
C11	B,2
C12	B,2
C13	B,2
C14	B,2
C15	B,2
C16	A,1
C17	B,1
C18	A,2
CR1	A,3
CR2	B,2
CR3	B,2
CR4	B,2
E1	B,1
E2	B,3
E3	A,3
E4	B,2
E5	A,2

Figure 8N-106. SERVICE SHEET 34 INFORMATION Component Locator



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	A, 3	J1	A, 1	R1	B, 3												
C2	A, 3	J2	A, 2	R2	B, 2												
C3	B, 3	J3	B, 3	R3	B, 2												
C4	A, 3			R4	B, 3												
C5	B, 3	L1	A, 3	R5	A, 2												
C6	B, 2	L2	B, 3	R6	B, 2												
C7	B, 3	L3	B, 2	R7	B, 2												
C8	B, 3	L4	B, 2	R8	B, 3												
C9	A, 2	L5	A, 2	R9	B, 2												
C10	A, 2	L6	B, 2	R10	B, 3												
C11	B, 2	L7	A, 2	R11	B, 3												
C12	B, 2			R12	B, 3												
C13	B, 2	Q1	A, 3	R14	B, 1												
C14	B, 2	Q2	B, 2	R15	A, 2												
C15	B, 2	Q3	A, 2	R16	B, 3												
C16	A, 1	Q4	B, 2	R17	B, 2												
C17	B, 1	Q5	A, 2														
C18	A, 2	Q6	A, 2	TP1	A, 2												
				TP2	A, 2												
CR1	A, 3			TP3	A, 2												
CR2	B, 2			TP4	B, 2												
CR3	B, 2			TP5	B, 3												
CR4	B, 2			TP6	A, 2												
				TP7	A, 2												
E1	B, 1																
E2	B, 3			VR1	A, 3												
E3	A, 3			VR2	A, 2												
E4	B, 2																
E5	A, 2																

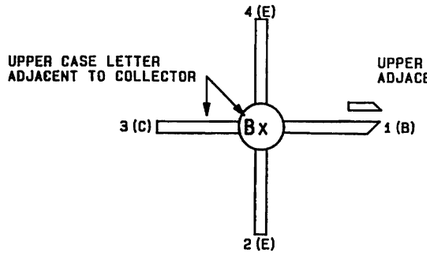
P/O A11A1 REFERENCE PHASE DETECTOR AND INTEGRATOR **SS33**

SEE REVERSE SIDE

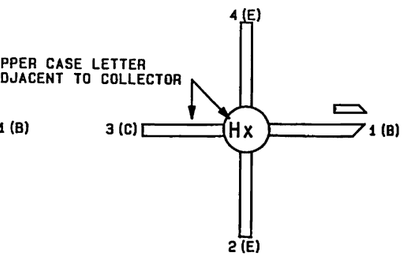
Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. A11A2 J3 consists of a clip and a single connector.
3. TP6 is labeled +15V on the printed circuit board.
4. TP7 is labeled -15V on the printed circuit board.
5. W100-W105 are printed circuit trace inductors.
6. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

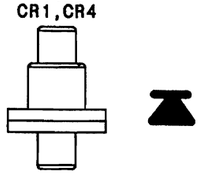
A11A2
Q1,Q3



A11A2
Q2



A11A2
CR1,CR4



Schematic General Information

CHANGES

2708A and above

On the Component Locator:

- CR5 - To the immediate right of J1, add CR5. It should be positioned vertically with the striped (cathode) end pointing up.

In the Component Coordinates:

- CR5 - Add CR5 with grid coordinates A,1.

On the Schematic:

- Change the part number of the A12A1 Assembly to 08642-60207.
- CR5 - In **BUFFER**, to the left of E9, connect the cathode of CR5 to the main signal line (from J1), and connect the anode to ground.

2731A Only

On the A11A2 Component Locator:

- C19, C20 - Locate C1 on the component locator, add C19 to the upper left side of C1 and add C20 to the upper right side of C1.
- C21, C22 - Locate C15 on the component locator, add C21 to the lower right side of C15, add C22 to the lower left side of C15.

On the Component Coordinates:

- C19, C20, C21, C22 - Add C19 A3, C20 B3, C21 B2, and C22 A2 to the component coordinates table.

On the A11A2 schematic:

- C19, C20 - In **VCO BAND 1**, add C19 100p in series with, and to the immediate left of C1, add C20 100p in series with, and to the immediate right of C1.
- C21, C22 - In **VCO BAND 2**, add C21 100p in series with, and to the immediate left of C15, add C22 100p in series with, and to the immediate right of C15.

A11A2 REFERENCE LOOP V.C.O. ASSEMBLY (08642-60107)

PRETUNE FILTER

TP3

P/O J2 PRETUNE VOLTAGE

C16 0.12µ

VCO SWITCH DRIVE

OSCILLATOR SELECT LINES AND PRETUNE
33 (DG) 3

BAND 2 — R15 3830 — Q5 — +15V (F3)

BAND 1 — R5 3830 — Q6 — +15V (F3)

BUFFER

REF LOOP TUNE VOLTAGE A11W2
32 (DE) (923) — J1

+15V (F3) — C13 0.01µ — Q4 — E1

R14 1470

C17 0.01µ — -15V (F2)

POWER SUPPLIES AND GND

POWER SUPPLY AND GROUND
33 (DH) 5

P/O J2

7 — +15V (F2) — TP6 (NOTE 3) +15V — L7 3µ — +15V (F3) — C18 0.01µ

8 — -15V (F2) — TP7 (NOTE 4) -15V — -15V (F2)

6 — GND

2 — NC

5 — NC

VCO BAND 1

TP1

R2 215 — L3 3µ

CR2

BAND 1 ADJ. C1 0.2-0.7p — CR1

R16 100

R1 1470

C3 1p

VR1 5.2V — Q1 — C4 10p

W101 (NOTE 5) — W100 (NOTE 5) — L1 100n

E2 — C5 100p — L2 0.1µ — E3

C2 100p

W102 (NOTE5)

VCO BAND 2

TP2

R7 215 — L4 3µ

CR3

BAND 2 ADJ. C15 0.2-0.7p — CR4

R17 100

R6 1470

C12 1p

VR2 5.2V — Q3 — C9 4.3p

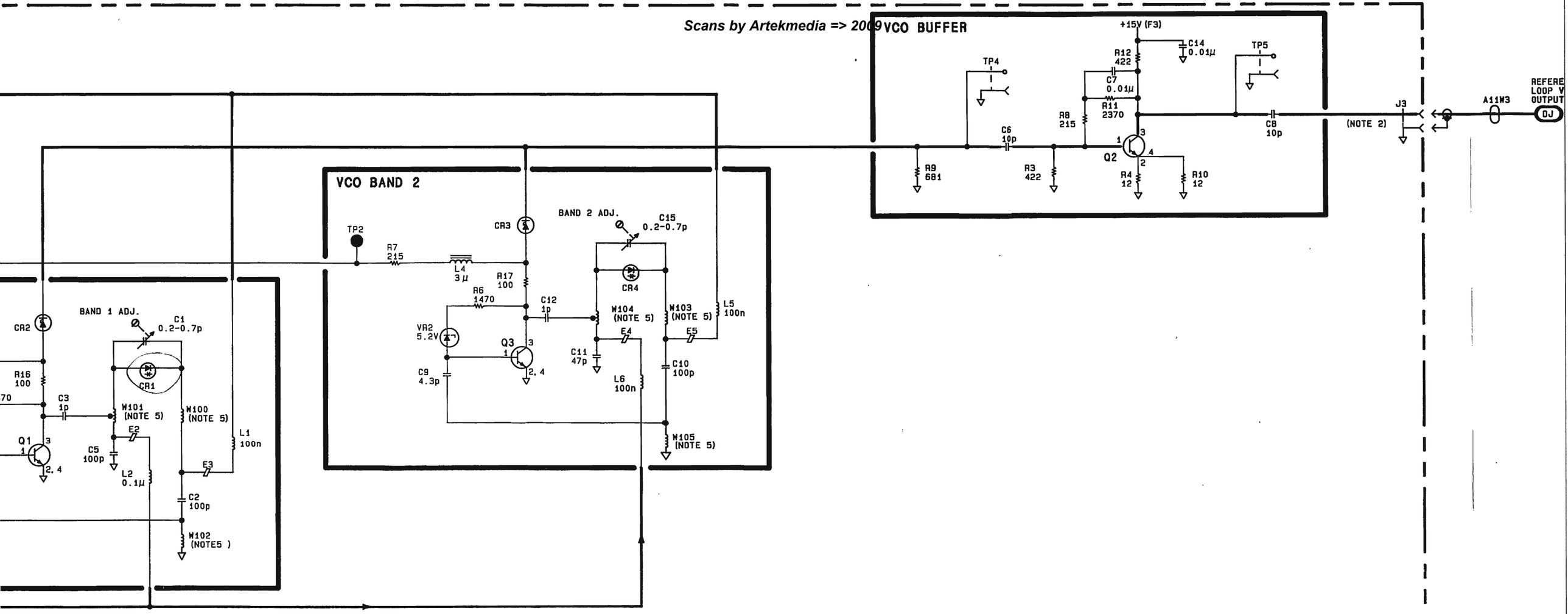
W104 (NOTE 5) — E4 — C11 47p

W103 (NOTE — E5 — C10 100p

L6 100n

W105 (NOTE

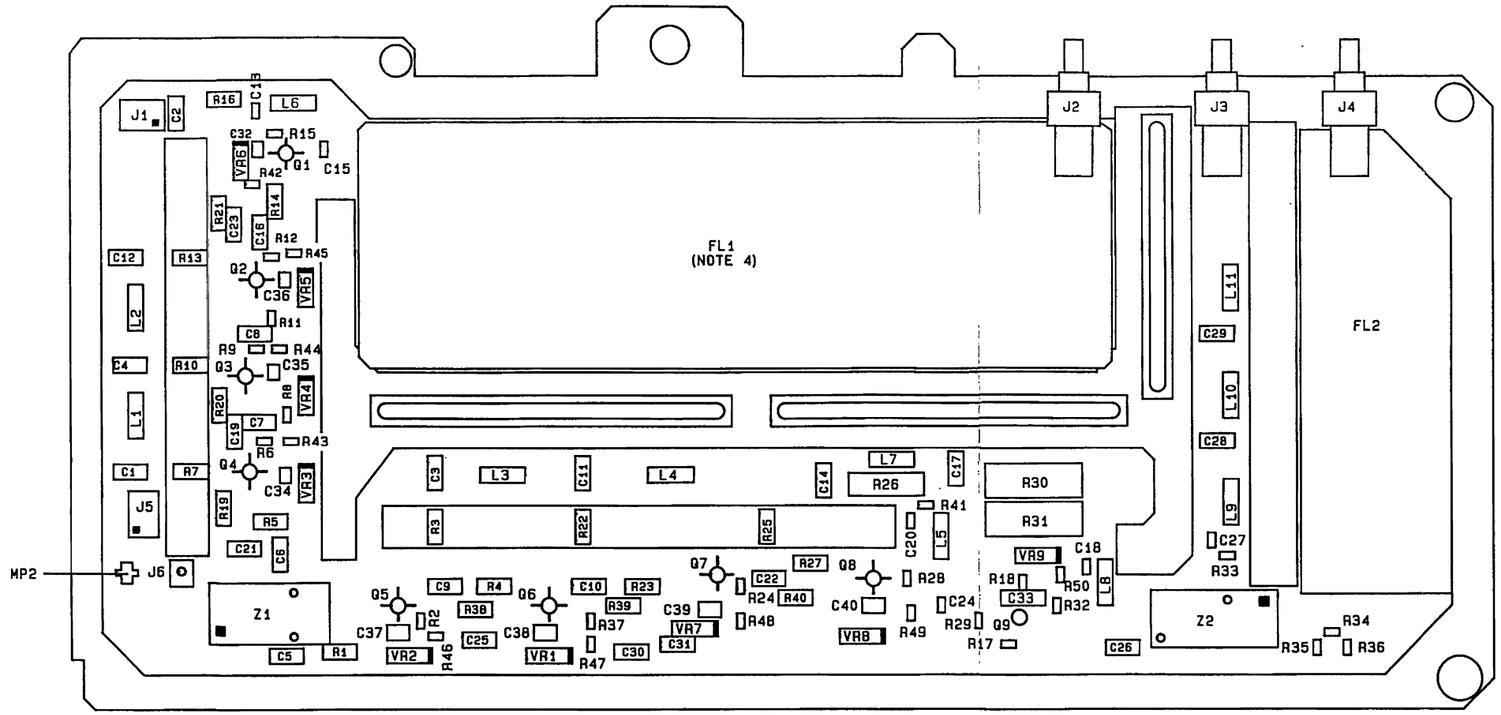
SERIAL PREFIX: 2427A



ATTENTION
Static Sensitive
Devices

SS34

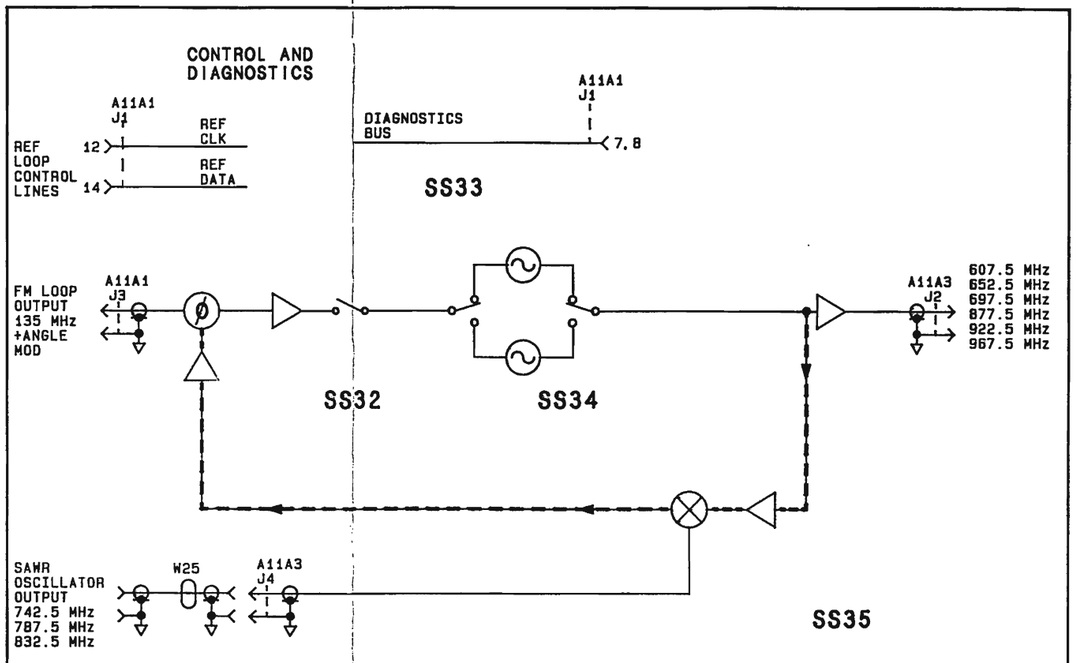
Figure 8N-107
8N-107



A11A3

Figure 8N-108. SERVICE SHEET 35 INFORMATION

Component Locator



Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	A, 2	C38	B, 3	R1	A, 3	R38	B, 3										
C2	A, 1	C39	B, 3	R2	A, 3	R39	B, 3										
C3	B, 2	C40	C, 3	R3	B, 3	R40	C, 3										
C4	A, 2			R4	B, 3	R41	C, 3										
C5	A, 3	FL1	B, 1	R5	A, 3	R42	A, 1										
C6	A, 3	FL2	D, 2	R6	A, 2	R43	A, 2										
C7	A, 2			R7	A, 2	R44	A, 2										
C8	A, 2	J1	A, 1	R8	A, 2	R45	A, 1										
C9	B, 3	J2	C, 1	R10	A, 2	R46	B, 3										
C10	B, 3	J3	D, 1	R10	A, 2	R47	B, 3										
C11	B, 2	J4	D, 1	R11	A, 2	R48	B, 3										
C12	A, 1	J5	A, 3	R12	A, 1	R49	C, 3										
C13	A, 1	J6	A, 3	R13	A, 1	R50	C, 3										
C14	C, 3			R14	A, 1												
C15	A, 1	L1	A, 2	R15	A, 1	VR1	B, 3										
C16	A, 1	L2	A, 2	R16	A, 1	VR2	A, 3										
C17	C, 2	L3	B, 2	R17	C, 3	VR3	A, 3										
C18	C, 3	L4	B, 2	R18	C, 3	VR4	A, 2										
C19	A, 2	L5	C, 3	R19	A, 3	VR5	A, 2										
C20	C, 3	L6	A, 1	R20	A, 2	VR6	A, 1										
C21	A, 3	L7	C, 2	R21	A, 1	VR7	B, 3										
C22	B, 3	L8	C, 3	R22	B, 3	VR8	C, 3										
C23	A, 1	L9	D, 3	R23	B, 3	VR9	C, 3										
C24	C, 3	L10	D, 2	R24	B, 3												
C25	B, 3	L11	D, 2	R25	B, 3	Z1	A, 3										
C26	C, 3			R26	C, 3	Z2	D, 3										
C27	D, 3	MP2	A, 3	R27	C, 3												
C28	D, 2			R28	C, 3												
C29	D, 2	Q1	A, 1	R29	C, 3												
C30	B, 3	Q2	A, 2	R30	C, 3												
C31	B, 3	Q3	A, 2	R31	C, 3												
C32	A, 1	Q4	A, 2	R32	C, 3												
C33	C, 3	Q5	A, 3	R33	D, 3												
C34	A, 2	Q6	B, 3	R34	D, 3												
C35	A, 2	Q7	B, 3	R35	D, 3												
C36	A, 2	Q8	C, 3	R36	D, 3												
C37	A, 3	Q9	C, 3	R37	B, 3												

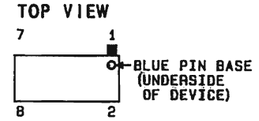
A11A2 REFERENCE LOOP V.C.O. ASSEMBLY **SS34**

SEE REVERSE SIDE

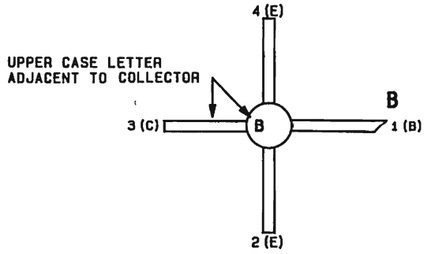
Notes:

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. L12-L18 are printed circuit trace inductors.
3. A11A3 J6 consists of a clip and single connector.
4. FL1 has polyiron shielding bordering the filter image (PC trace). It must be positioned so that none of the image area is covered by the polyiron. If the polyiron moves, recalibration may be necessary.
5. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

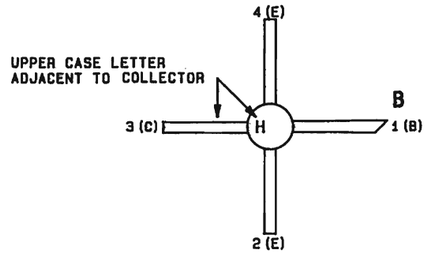
A11A3
Z1,Z2
TOP VIEW



A11A3
Q1-Q8



A11A3
Q9



Schematic General Information

CHANGES

2529A and above

In Schematic General Information:

- Revise Note 4 to include FL2.

On the schematic:

- In **860 MHz RF FILTER**, add "NOTE 4" next to FL2.

2535A and above

On the schematic:

- A11A3 L8 - In **LO LIMITER/AMPLIFIER** change the value of L8 to 36n Henries.

OUTPUT LEVEL CONTROL
33 DD → P/O J1 1

REFERENCE LOOP VCO OUTPUT A11W3
34 DJ → (NOTE 3) J6

SAWR OSCILLATOR OUTPUT W25
26 BJ → 937 → J4

+15V (F2) SUPPLY
33 DI → J5 1

OUTPUT LIMITER/AMPLIFIER

+15V (F2) R7 681
R43 1470, R6 220, VR3 5.2V, C34 0.1µ
Q4 (1 B, 3, 2, 4)
R5 51.1
C7 2.2p, R8 50
L13 20n (NOTE 2), R19 51.1, C21 100p

+15V (F4) R10 562
R44 1470, R9 220, VR4 5.2V, C35 0.1µ
Q3 (1 B, 3, 2, 4)
C8 2.2p, R11 50
L15 20n (NOTE 2), R20 51.1, C19 100p

+15V (F5) R13 464
R45 1470, R12 220, VR5 5.2V, C36 0.1µ
Q2 (1 B, 3, 2, 4)
C2 0.01µ, R16 147, C13 1000p, L6 24n, R15 220
VR6 5.2V, C32 1µ
C16 5.6p, R14 51.1, R42 1470
L17 20n (NOTE 2), R21 51.1, C23 100p
Q1 (1 B, 3, 2, 4)
C15 10p
FL1 (NOTE 4) — OUTPUT FILTER

POWER SPLITTER

C6 4.7p
Z1 (1, 2, 3, 4, 7, 8, 5, 6)
FEEDBACK PATH
C5 10p

LO LIMITER/AMPLIFIER

+15V (F3) R3 681
R46 1470, R2 220, VR2 5.2V, C37 0.1µ
Q5 (1 B, 3, 2, 4)
R1 51.1
C9 2.2p, R4 51.1
L14 20n (NOTE 2), R38 51.1, C25 100p

+15V (F6) R22 562
R47 1470, R37 220, VR1 5.2V, C38 0.1µ
Q6 (1 B, 3, 2, 4)
C10 2.2p, R23 51.1
L16 25n (NOTE 2), R39 51.1, C30 100p

+15V (F7) R25 464
R48 1470, R24 220, VR7 5.2V, C39 0.1µ
Q7 (1 B, 3, 2, 4)
C22 30p, R27 51.1
L18 40n (NOTE 2), R40 51.1, C31 100p

+15V (F8) R26 261
R49 510, R28 220, VR8 5.1V, C40 0.1µ
L5 24n, R41 50, C20 1000p
Q8 (1 B, 3, 2, 4)
C24 22p, R29 510
R50 220, R32 220, VR9 4.7V, C33 1µ
R30 237

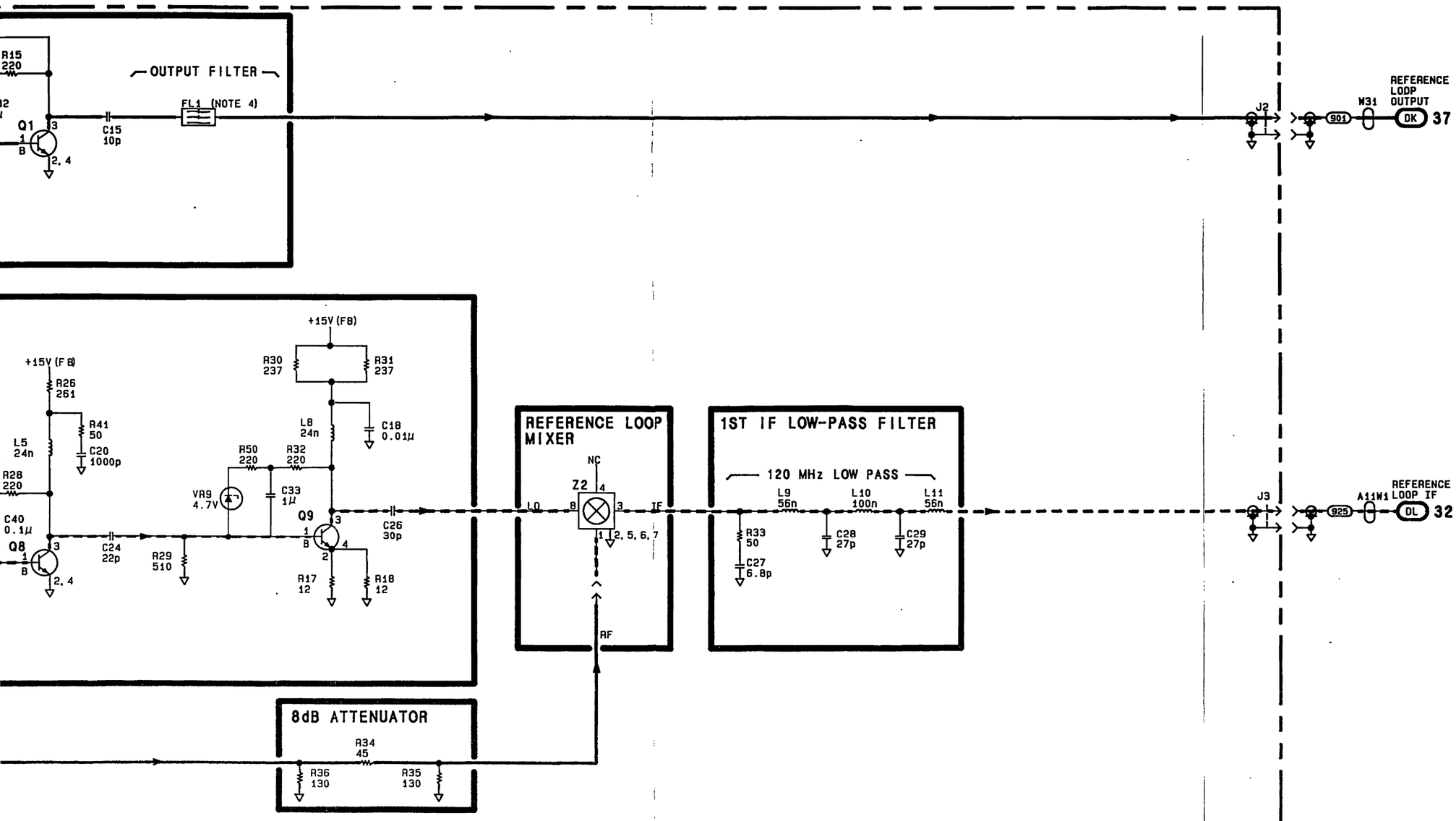
860 MHz RF FILTER

J4 — FL2

POWER SUPPLIES AND GND

J5 1
C1 0.01µ, L1 1µ → +15V (F2)
C4 0.01µ, L2 1µ → +15V (F4)
C12 0.01µ → +15V (F5)
L12 50n (NOTE 2) → +15V (F3)
L3 1µ → +15V (F6)
C3 0.01µ, L4 1µ → +15V (F7)
C11 0.01µ, C14 0.01µ, L7 1µ → +15V (F8)
C17 0.01µ

SERIAL PREFIX: 2427A



SS35
Figure 8N-109
8N-109