3048 MS

HP 8663A
SYNTHESIZED SIGNAL GENERATOR
(Including Options 001, 002, & 003)

Service Manual

Volume 2

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed:

2234A to 2927A and all *MAJOR* changes that apply to your instrument.

rev.01JUL91

For additional important information about serial numbers, refer to "INSTRUMENTS COVERED BY THIS MANUAL" in Section 1.

Third Edition

Service Manual (Volume 1, 2, 3, 4) HP Part 08663-90071

Other Documents Available:
Operation and Calibration Manual HP Part 08663-90069
Microfiche Service Manual HP Part 08663-90072
Microfiche Operation and Calibration Manual HP Part 08663-90070

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PRINCIPLES OF OPERATION

The basic frequency generating circuitry is composed of the Reference Section, phase lock loops and Output Section (in the upper-left, center and right hand portions of the block diagram respectively). All of the reference frequencies used within the instrument are obtained from the Reference Section. A total of seven phase lock loops work together to produce the fundamental frequency band of 320 to 640 MHz with a step resolution of 0.1 Hz. This fundamental (or basic) band is sent to the Output Section where it is doubled, passed straight through or down-converted to produce the entire frequency range at the RF output (.1 to 2560 MHz).

The Digital Control Unit (DCU) controls the operation of the unit. It accepts keyboard or remote inputs and generates internal data and control signals to control the signal at the RF output. Power for the instrument is supplied by a switching-regulated power supply.

Reference Section

All of the reference frequencies used within the instrument are obtained from the Reference Section. This block is composed of doublers, dividers, and mixers, all of which are driven by a single temperature-stabilized 10 MHz crystal oscillator. Outputs from the Reference Section are 10, 20, 120, 520, and 320-640 MHz (in 20 MHz steps). Signal levels vary depending on which section they are being sent to.

Phase Lock Loops

The Generator uses the indirect synthesis method for generating output frequencies. Phase lock loop (PLL) circuits are locked to signals from the Reference Section and generate signals which are combined to give the desired output frequency. All output frequencies retain the same accuracy and stability as the 10 MHz reference signal. PLL's are found in the High Frequency, Low Frequency, Fractional-N, and Modulation Sections.

High Frequency Loops

The Reference Sum Loop and the Output Sum Loop are two nearly identical circuits. The Reference Sum Loop starts with 320-640 MHz and 10 or 20 MHz signals from the Reference Section. Together, these signals are related to digits D9 and D8 in the FREQUENCY readout (in the basic band only). These signals are combined in the Output Sum Loop with the low frequency loops output that has a 0.1 Hz resolution.

Low Frequency Loops

The Low Frequency section consolidates several signals and produces an output signal having the characteristics of all of the inputs. This section has three phase lock loops: the N-Loop, the Low Frequency Sum Loop, and the FM Sum Loop.

The N-Loop generates a signal related to the D7 and D6 digits of the FREQUENCY readout (in the basic band). The other two loops combine this signal with outputs from the Fractional-N Loop. A 20 MHz signal is frequency modulated at the level needed to provide the desired amount of deviation at the front panel RF output.

Fractional-N-Loop

The Fractional-N-Loop uses the 10 MHz reference signal to produce an output that is related to digits D5, D4, D3, D2, D1, and D0 of the FREQUENCY readout (in the 320-640 MHz "basic band"). The phase lock loop is called "Fractional-N" because the divider in the feedback circuit can divide by both integer and fractional values. This is accomplished by using digital dividers that by themselves only divide by integer values, but with extra control circuitry can switch the "divide-by" integer (N) between two values so that the average value of N contains a fractional part.

For example, to divide by 1300.455, the divider would divide by 1301 for 455 cycles and by 1300 for 545 cycles. Over 1000 cycles, the effective division is by 1300.455. The Fractional-N-Loop provides high resolution, fast switching, and low noise.

Modulation Section and FM Loop

The Modulation Section has a Variable Modulation Oscillator (VMO) that produces modulation source signals at rates from 10.0 Hz to 99.9 kHz with 3 digit resolution. External modulating signals can be applied to the front panel AM IN, FM IN, and PM IN connectors. Simultaneous modulation is possible.

The FM Loop produces one of the reference signals for the FM Sum Loop. The signal is 20 MHz with FM. The phase lock loop is unlocked when a dc-coupled signal from the front panel's FM INPUT is selected. Thus, the 140 MHz Oscillator operates in a free run condition without any correction.

Phase Modulation Section (Option 002 Only)

The Phase Modulation section provides phase modulation at up to 10 MHz rates from an external source. BPSK at RF output frequencies of 640 MHz and above are generated in this section.

Output Section

The output section converts the basic band (320 to 640 MHz) from the High Frequency Section to all other frequencies by multiplying it, passing it through, or dividing it. This section also controls the RF level of the signal. It does this with a group of electromechanical attenuators. These attenuators reduce the amplitude in 5 dB increments from 5 dB through 140 dB. Electronic leveling keeps the output level constant and provides finer output step resolution.

Pulse modulation, AM, and BPSK (RF output frequencies < 640 MHz) are generated in the output section.

Digital Control Unit

The Digital Control Unit (DCU) is a microprocessor based controller that is responsible for directing the operation of the instrument. It takes information from the keyboard, HP-IB interface or AUX connector. It stores data, calculates the required oscillator frequencies, determines internal switch settings, and exercises general control over the instrument. Although not shown on this block diagram, the DCU is a transfer point for digital data to all the sections.

Power Supply

This instrument uses a switching-regulated power supply that provides high efficiency and low heat dissipation.

TROUBLESHOOTING

Introduction

Troubleshooting is structured into three levels:

1. Instrument (to identify a defective section)
2. Section (to identify a defective assembly)
3. Assembly (to identify a defective component)

The general procedure is to begin at the instrument level to isolate the problem to a section (Block Diagram BD1), then to an assembly within the section (Block Diagrams BD2-BD10), and finally to a component on the assembly (detailed schematics). There is troubleshooting information on the block diagrams which can be used

by someone who understands the theory of operation to isolate the problem to the next lower level. There is a troubleshooting procedure with each block diagram . These procedures are the recommended troubleshooting approach for someone who is inexperienced with servicing the Generator. To effectively use these procedures you need a basic understanding of the principles of operation. Read the theory before using the procedure so the procedure becomes a guide. Many short cuts are possible as more experience is gained.

WARNING

When working on the power supply, remember that high voltage is present at all times when the line cord is plugged in (that is, plus and minus 160 Vdc and line voltage). Unplug the line cord before doing anything to the power supply. The line switch has no effect on the high voltage.

When working near the rear panel, be careful to keep long hair from being drawn into the fan. This could cause personal injury.

CAUTION

DO NOT plug in or unplug any board assembly with the instrument line switch turned on. Always turn the line switch to STANDBY when removing or inserting a board. There are some components that could be damaged by transients generated this way.

The "LINE" fuse should not be replaced until the cause of its failure is determined Replacing this fuse in a damaged Generator might cause additional damage. A qualified service person should first determine the cause of its failure, specifically with resistance checks in the power supply (see Service Sheet 65); repair the failure and then replace the fuse.

When measuring frequency, connect a cable from the Generator's 10 MHz Reference output (rear panel) to the counter's reference input and set the counter Reference switch to EXT. Since minor differences exist between time bases, using the 8663A's as a common reference will ensure that all correct frequency readings will be off only by the resolution error of the counter.

When measuring frequency or power level at an output connector, disconnect any cable that is normally connected so the measuring instrument is the only load on the output. If the cable must remain connected to make a valid measurement, this will be specifically stated.

All power level values given are as measured on a spectrum analyzer. Measurements made with a power meter might give a slightly higher reading. ECL signals will read approximately 2 dB higher with a

power meter because the harmonics are high and add to the power meter reading.

Instrument Level Troubleshooting Procedure

The followeing procedure can be used to isolate an instrument malfunction to one of the sections.

1. Check power supply voltages. Remove the top cover of the instrument. The power supply is in the left-rear corner. Test points used to check each of the voltages are accessible through openings in the power supply top cover. Silkscreening on the cover identifies the test points. Measure each of the voltages and compare to the tolerances in Table 8-201.

Table 8-201. Power Supply Voltages

Supply Voltage	Tolerance
+5.2V	±.02V
+20V	±0.1V
-10V	±.04V
-40V	±0.2V

If a voltage is out of tolerance, adjust it. The voltage should be adjustable above and below the nominal value within the tolerance limits. If a voltage cannot be adjusted to within limits, there is a problem with the power supply. Continue troubleshooting on Service Sheet BD10.

If the Generator fails to turn on, check the power supply voltages first. If they are incorrect, continue on Service Sheet BD10. If the power supply voltages are correct, continue on Service Sheet BD9 (the Digital Control Unit).

2. STATUS light flashes. All sections contain self-check circuitry which can detect some malfunctions. When a malfunction is detected, the STATUS light flashes. Press the STATUS key and hold it down and the status code will be displayed in the frequency display (on the right). If 99 is displayed, press the Blue Key and then the STATUS key. The actual status code will be displayed. Table 8-203 defines the malfunction status codes and where to continue troubleshooting if one occurs.

There are many errors which cannot be detected by the self-check circuitry and it's also possible for the self-check circuitry to

malfunction. Therefore, use the status code only as a guide. Confirm that the problem indicated by the status code really exists.

NOTE

Under certain conditions, it is possible for Status Code 76, "Amplitude out of specification", to turn on when no amplitude error exists. This can happen during fast repetitive sweeps (for example, Auto Sweep or Remote Stepped Sweep, with the time/step less than 1 ms). Corrective action is not required unless code 76 persists under conditions other than those outlined above.

If no status code is present, continue with Step 3.

3. All malfunctions can be divided into eight general classifications as follows:

   a) Front Panel, HP-IB and AUX malfunctions. This includes all improper operation of keys, display and indicators. Begin troubleshooting with Service Sheet BD9.

   b) RF output frequency not correct. Begin troubleshooting with Step 4.

   c) RF output power level not correct. Begin troubleshooting with Step 5.

   d) AM and FM problems. Begin troubleshooting with Service Sheet BD7.

   e) Phase modulation problems. Begin troubleshooting with Service Sheet BD8.

   f) Pulse modulation and BPSK problems. Begin troubleshooting with Service Sheet BD6.

   g) High spurs or phase noise. Begin troubleshooting with Step 6, below.

   h) Problems associated with front and rear panel connectors (except RF output). Table 8-202, shows where to start troubleshooting when the signal from an output connector is not normal or the signal applied to an input connector does not produce the desired effect.

Table 8-202. Failures Associated With External Connectors

CONNECTOR	TROUBLESHOOT ASSEMBLY (SERVICE SHEET)
AM IN, FM IN, PM IN	A11A5 (41 and 42) A11A3 (44)
Rear Panel Connectors	
AUX	A2A1 (61 and 62)
SWP	A2A2 (56 and 57)
AM MKR	A2A2 (56 and 57)
Z/AXIS BLK/MKR	A2A2 (56 and 57)
PLS BPSK	A4A1 (37)
VMO OUT	A11A1 (39 and 40)
AUX FM IM	A11A2 (43)
(10 MHz Reference) OUTPUT	A8A4 (1)
(5 or 10 MHz Reference) INPUT	A8A4 (1)

4. RF Output Frequency Not Correct.

   a) Measure the RF output frequency with a counter. Run a cable from the Generator's 10 MHz reference output to the counter external time base input and set the counter time base switch to external.

   b) If the frequency is not stable (that is, it varies more than ±1 count), there is a phase lock loop unlocked. Measure the output of each section containing phase lock loops shown on the block diagram until the bad section is found. Start at the bottom of the block diagram and move up. Then continue troubleshooting on the Service Sheet for the bad section.

   c) If the frequency is stable, measure the High Frequency Loops Section output frequency. If this frequency is normal, the problem is in the Output Section. Otherwise, measure the output of each section starting at the bottom of the block diagram until the bad section is found. Then continue troubleshooting on the service sheet for the bad section.

5. RF Power Level Not Correct. Measure the power level of the output signal from the High Frequency Loops Section. If this power level is not within the limits given on the block diagram, there is a problem in the High Frequency Loops Section so continue troubleshooting on Service Sheet BD3. If this power level is normal, the problem is in the Output Section, so continue troubleshooting on Service Sheet BD8.

6. High Sprus or Phase Noise. This is the most difficult type of problem to troubleshoot. Some troubleshooting experience and a thorough understanding of the theory of operation of the instrument are needed to be successful. The general procedure to follow is:

   a) Locate the section of the instrument in which the problem is originating.

   b) Search for the cause. In the case of high phase noise it is now a matter of trying different approaches to narrow the range of possible causes. This is where experience helps. If the problem is spurs, identify the source of the spur. The location of the spur and how it moves in relation to the center frequency can provide a lot of information when the theory of operation of the Generator is understood. Removing cables or substituting signals from an external source are also useful techniques.

   c) Once the source of the spur is known look for the coupling mechanism.

TABLE 8-203. HARDWARE MALFUNCTION STATUS CODE DESCRIPTION

STATUS CODE	DESCRIPTION	CONTINUE TROUBLESHOOTING ON SERVICE SHEET
00	No malfunction	---
01	Low reference oscillator signal level. (Check INT-EXT switches on rear panel).	1
02	Fractional-N Loop out on lock.	BD4
03	Low Frequency N Loop out of lock.	BD5
04	Low Frequency Sum Loop out of lock.	BD5
05	Low Frequency FM Sum Loop out of lock.	BD5
06	High Frequency Reference Sum Loop out of lock.	BD3
07	High Frequency Sum Loop out of lock.	BD3
08	FM Loop out of lock.	BD7
61	Variable Modulation Oscillator Loop out of lock.	BD7
76	RF Output amplitude not leveled.	BD8
95	ROM Malfunction.	BD9
96	RAM Malfunction.	BD9
98*	Memory Malfunction.	
99*	Hardware Malfunction.	

* This is the general code for instrument malfunction. Press the BLUE KEY and then STATUS to obtain one of the other codes in the table which is the actual malfunction.

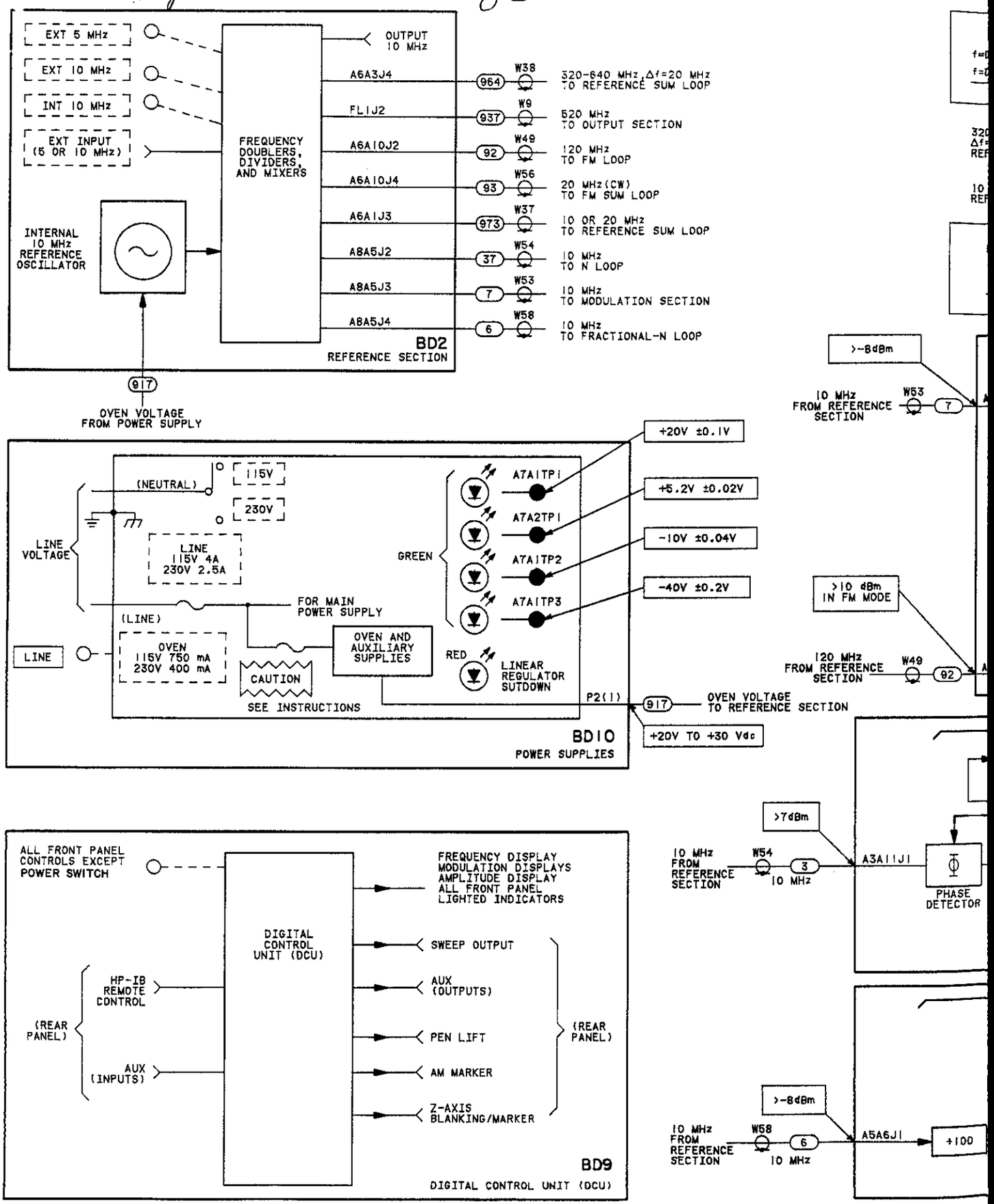
NOTE

Errors 101-119, below, are generated by self-check circuitry in the Digital Control Unit (DCU). The Frequency, level and modulation data that is sent to other sections is also read back from the DCU output. Thus, when an error occurs, it could be that the data is bad, something could be pulling the signal line up or down, or the read-back circuitry is bad. The description of the code gives the reference designator of the latch where the bad data is stored.

TABLE 8-203. HARDWARE MALFUNCTION STATUS CODE DESCRIPTION (continued)

STATUS CODE	DESCRIPTION	CONTINUE TROUBLESHOOTING ON SERVICE SHEET
101	AM/FM Control (A2A4U15)	55
102	AM Control (A2A4U16)	55
103	VMO Rate (A2A4U17)	55
104	VMO Rate (A2A4U14)	55
105	FM Level (A2A4U13)	55
106	AM LEVEL (A2A4U12)	55
107	AM/FM Level (A2A4U11)	55
108	PM Level (A2A10U13)	54
109	PM Level (A2A10U14)	54
110	RF Off Control (A2A10U15)	54
111	RF Level (A2A10U12)	54
112	RF Level (A2A10U11)	54
113	Not used	
114	Frequency Range Control (A2A5U24)	52,53
115	Frequency DF0-DF1 (A2A5U23)	52,53
116	Frequency DF2-DF3 (A2A5U26)	52,53
117	Frequency DF4-DF5 (A2A5U25)	52,53
118	Frequency DF6-DF9 (A2A5U21,U22)	52,53
119	Frequency DFB7-DFB8 (A2A5U19,U20)	52,53

/21917A Fig 8-201 Sht 1 of 5



SERIAL PREFIX: 2234A

Fig 8-201 Sht 2 of 5

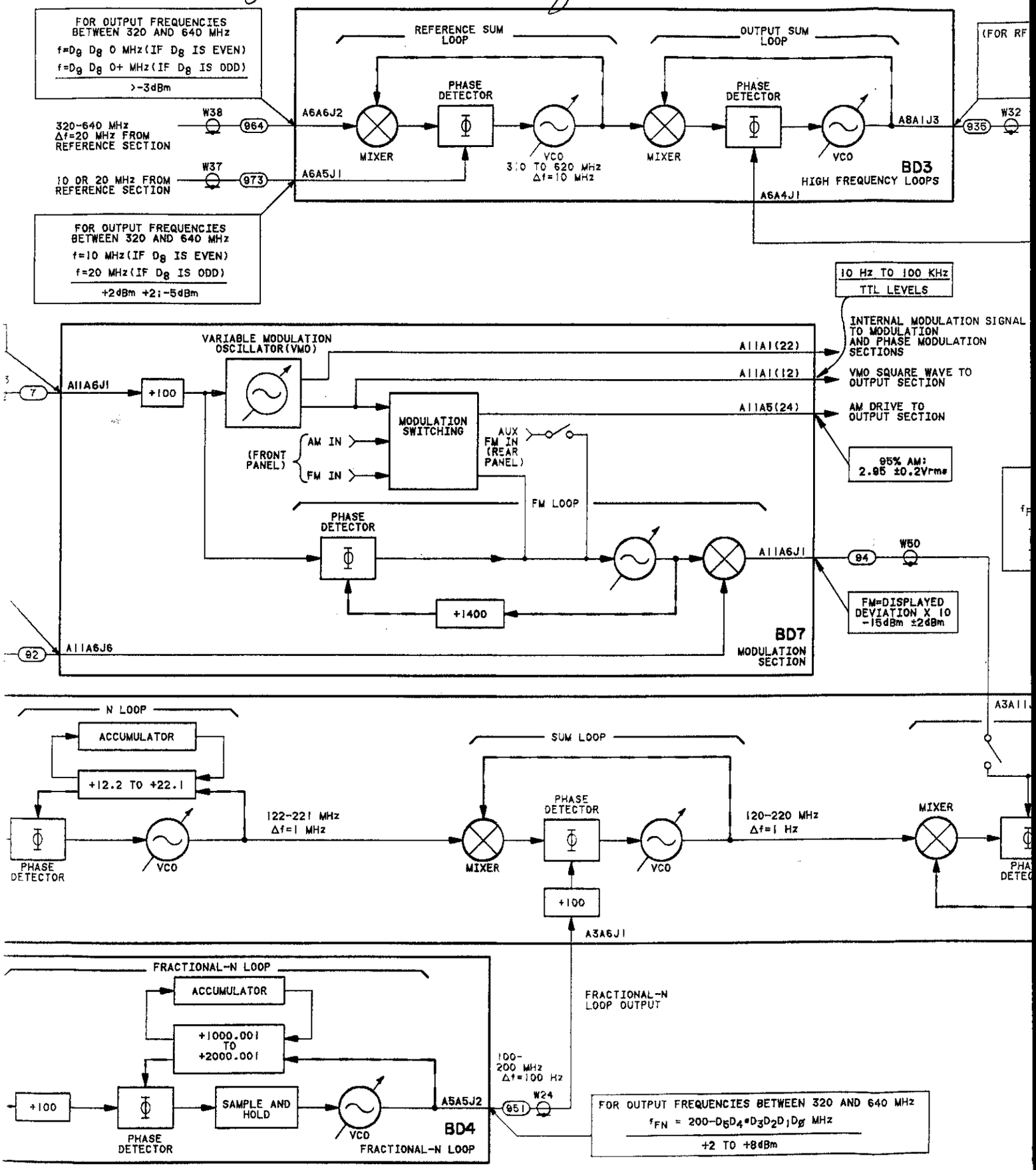


Fig 8-201 Sht 3 of 5

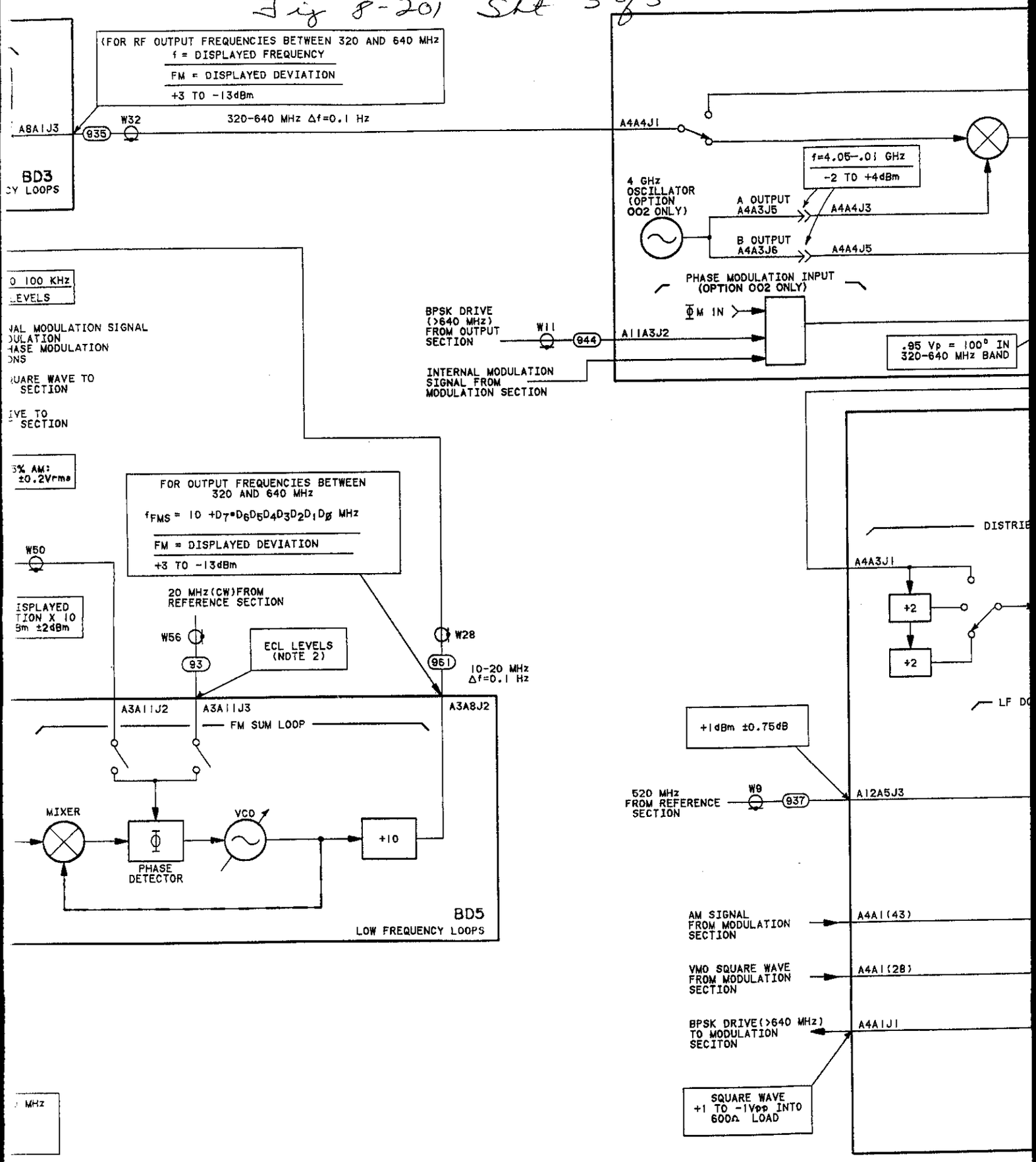


Fig 8-201 Sht 4 of 5

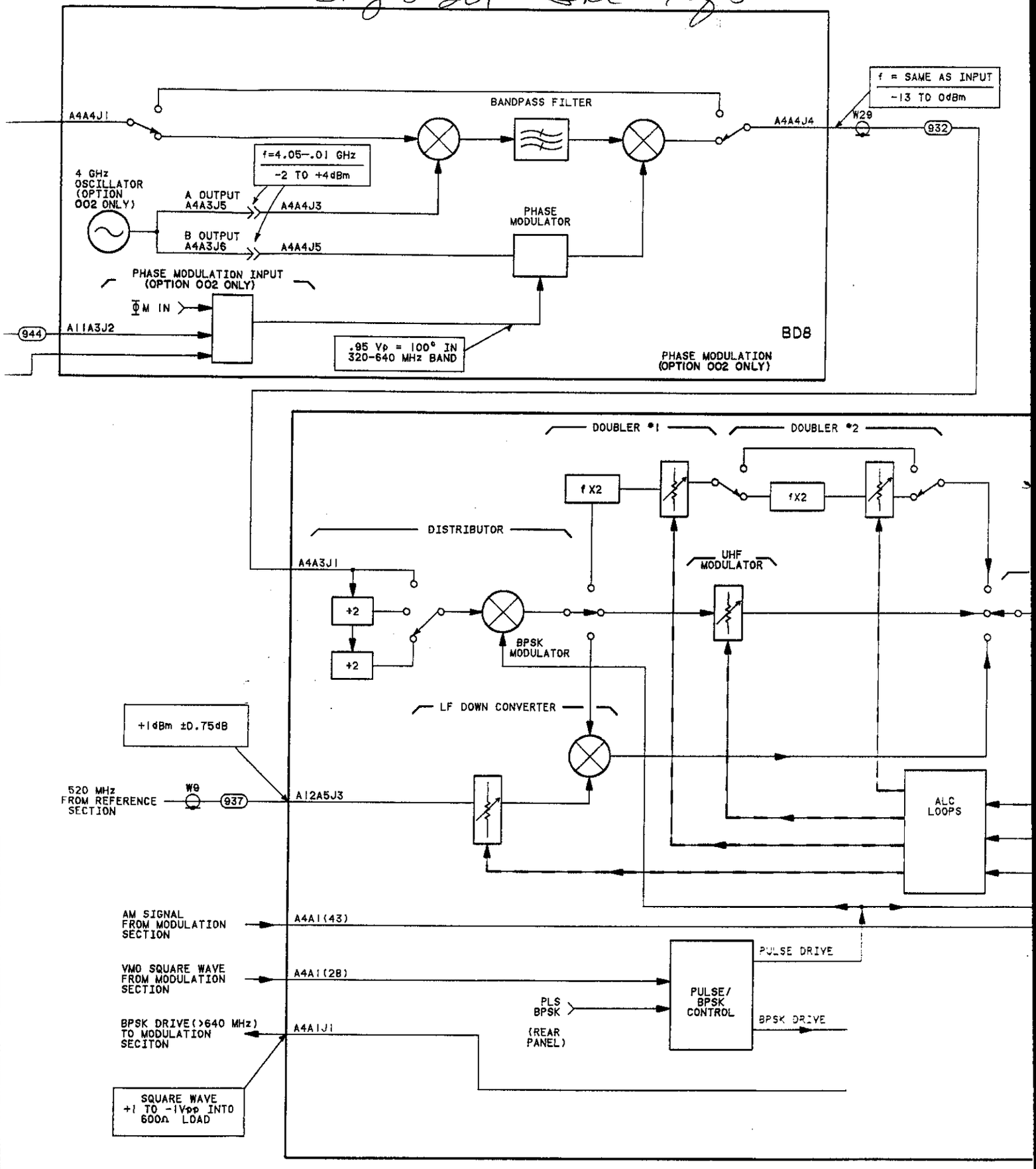
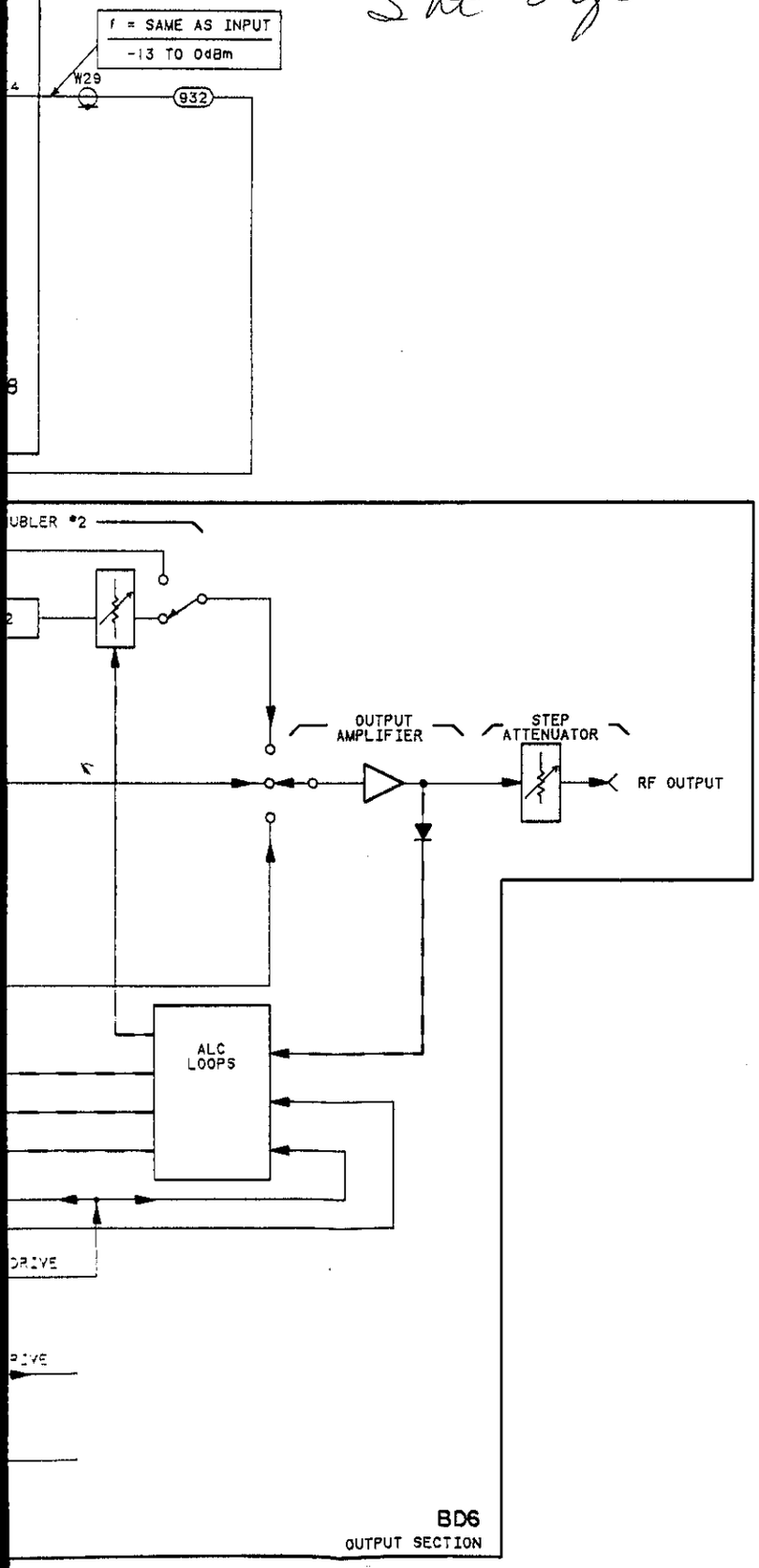


Fig 8-201
Sht 5 of 5



NOTES

1. INTERCONNECTIONS BETWEEN THE DCU AND THE OTHER SECTIONS ARE NOT SHOWN ON THIS BLOCK DIAGRAM. REFER TO THE APPROPRIATE SECTION BLOCK DIAGRAM (BD2-BD10) OR SCHEMATIC FOR THIS INFORMATION.

2. ECL LOGIC LEVELS IN THIS INSTRUMENT ARE NON-STANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS $\geq$ +4.0V; A LOW LEVEL IS $\leq$ +3.5V.

3. FREQUENCY FORMULAS GIVEN FOR BLOCK DIAGRAMS BD3, BD4 AND BD5, APPLY ONLY WHEN THE FRONT PANEL FREQUENCY SETTING IS BETWEEN 320 AND 640 MHz (THAT IS, THE BASIC BAND). THE FORMULAS DO NOT APPLY IF A FREQUENCY FAILURE OCCURS OUTSIDE THE BASIC BAND. FREQUENCY FAILURES OUTSIDE THE BASIC BAND ARE PROBABLY IN THE OUTPUT SECTION (REFER TO BD6 TO BEGIN TROUBLESHOOTING).

   THE FORMULAS RELATE TO THE FRONT PANEL FREQUENCY DISPLAY. THE DISPLAY DIGITS ARE DESIGNATED D_{10} THROUGH D_0 AS FOLLOWS:

FREQUENCY DISPLAY

D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
8	8	8	8	8	8	8	8	8	8	8

   ENTER THE VALUE OF EACH DIGIT INTO THE FORMULAS AND USE THE DECIMAL POINT SHOWN IN THE FORMULA INSTEAD OF THE DISPLAYED DECIMAL POINT.

   FOR EXAMPLE IF THE DISPLAYED FREQUENCY IS 532.876 401 9 MHz

   - THE OUTPUT OF BD3 WOULD BE: 532.876 401 9 MHz
   - THE OUTPUT OF BD4 WOULD BE: 200-76.401 9 MHz OR 123.598| MHz
   - THE OUTPUT OF BD5 WOULD BE: 10 + 2.876 401 9 MHz OR 12.876 401 9 MHz

CAUTION

IF THE LINE FUSE BURNS OUT DO, NOT REPLACE IT UNTIL THE CAUSE OF THE FAILURE HAS BEEN DETERMINED AND REPAIRED BY A QUALIFIED SERVICE PERSON AND, SPECIFICALLY, WITH RESISTANCE CHECKS IN THE POWER SUPPLY. REFER TO SERVICE SHEET 65. REPLACING THIS FUSE IN A DAMAGED SIGNAL GENERATOR CAN RESULT IN ADDITIONAL DAMAGE

BD1

Figure 8-201. Overall Block Diagram

SERVICE SHEET BD2
REFERENCE SECTION BLOCK DIAGRAM

REFERENCE BD1
Simplified Operation (Section III)
Operator's Checks (Section III)
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

The Reference Section provides the following output signals:

FM Loop 10 MHz Reference Signal
Fract. N 10 MHz Reference Signal
N Loop Phase Detector Reference (10 MHz)
RS Loop Phase Detector Reference (10 or 20 MHz)
FMS Loop Phase Detector Reference (20 MHz CW)
Down Converter Band Mixer RF (520 MHz)
RS Loop Mixer RF (320-640 MHz, delta f = 20 MHz)
FM Loop Mixer LO (120 MHz)

These signals are distributed to other sections of the instrument. All of the Reference Section outputs are derived from either a 10 MHz internal source (temperature controlled quartz oscillator) or an external frequency standard of 5 MHz or 10 Mhz. The accuracy and stability of all signals generated in the Generator are traceable to the outputs fron the Reference Section. The various output signals are generated by employing several frequency translation techniques (multiplying, dividing and heterodyning).

TROUBLESHOOTING

There are five signals generated in the Reference Section (besides three 10 MHz signals) and sent to other sections of the instrument:

1) 320-640 MHz in 20 MHz steps (A6A3J4)
2) 520 MHz reference signal (A6A3J1
3) 120 MHz reference signal (A6A10J2)
4) 10/20 MHz signal (A6A1J3)
5) 20 MHz reference signal when the instrument is in FM mode (A6A10J4)

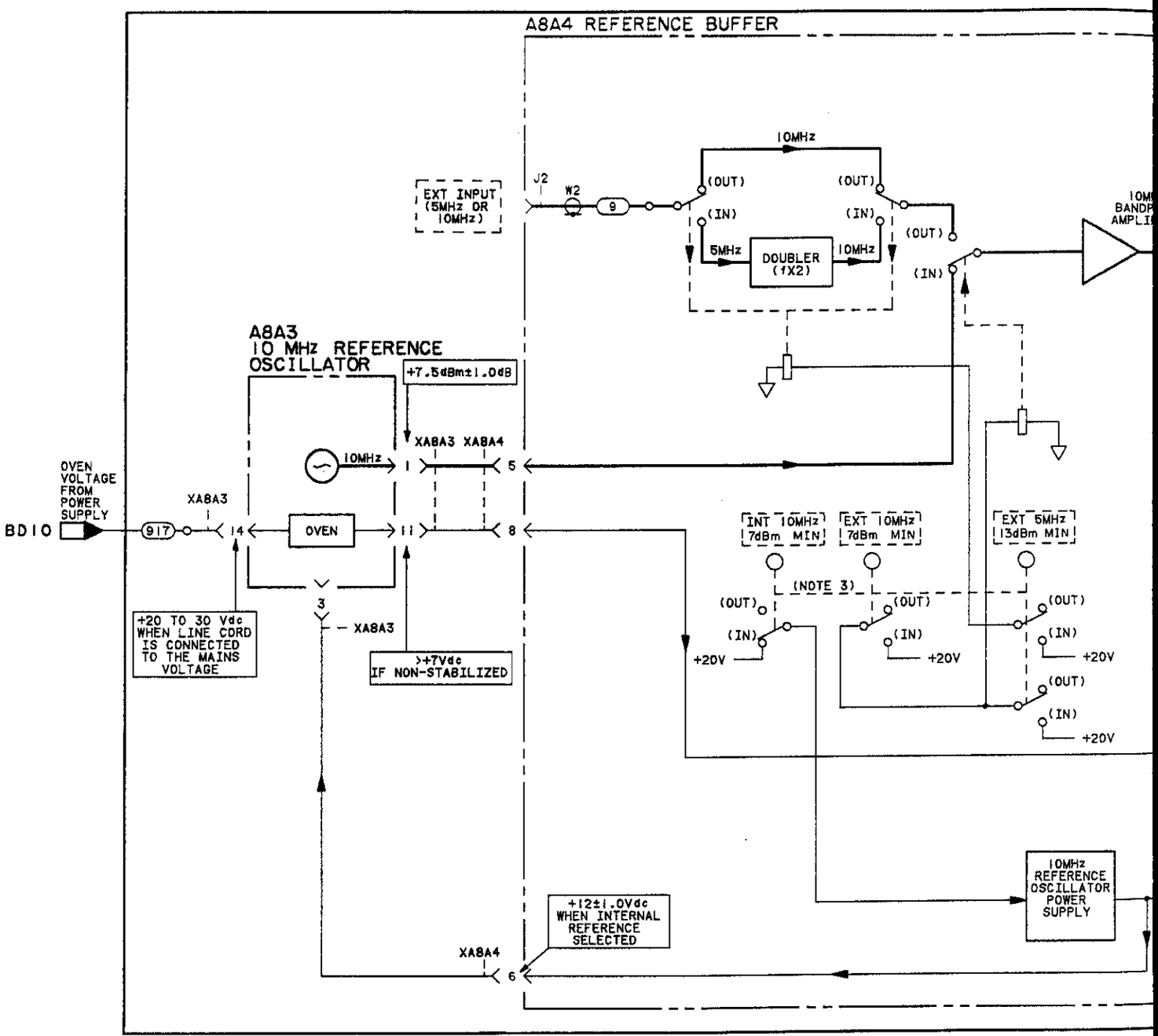
When the frequency or level of one of these signals is not the value shown on the block diagram, the problem is in the Reference Section. Table 8-205 shows at what frequencies the variable frequency signals are for output frequencies in the basic band (that is, 320 to 640 MHz). Troubleshoot the Reference Section by backtracking until the bad assembly is found. Then continue troubleshooting with the service sheet for the defective assembly.

Table 8-205. Reference Section Variable Frequency Signals

Output Frequency (MHz)		Reference Section Variable Signals (MHz)		
≥	<	A6A3J4 (320-640)	A6A1J3 (10/20)	A6A2J2[1] (60-140)
320.0	330.0	320.0	10.0	DC
330.0	340.0	340.0	20.0	140.0
340.0	350.0	340.0	10.0	140.0
350.0	360.0	360.0	20.0	120.0
360.0	370.0	360.0	10.0	120.0
370.0	380.0	380.0	20.0	60.0
380.0	390.0	380.0	10.0	60.0
390.0	400.0	400.0	20.0	80.0
400.0	410.0	400.0	10.0	80.0
410.0	420.0	420.0	20.0	60.0
420.0	430.0	420.0	10.0	60.0
430.0	440.0	440.0	20.0	120.0
440.0	450.0	440.0	10.0	120.0
450.0	460.0	460.0	20.0	140.0
460.0	470.0	460.0	10.0	140.0
470.0	480.0	480.0	20.0	DC
480.0	490.0	480.0	10.0	DC
490.0	500.0	500.0	20.0	140.0
500.0	510.0	500.0	10.0	140.0
510.0	520.0	520.0	20.0	120.0
520.0	530.0	520.0	10.0	120.0
530.0	540.0	540.0	20.0	60.0
540.0	550.0	540.0	10.0	60.0
550.0	560.0	560.0	20.0	80.0
560.0	570.0	560.0	10.0	80.0
570.0	580.0	580.0	20.0	60.0
580.0	590.0	580.0	10.0	60.0
590.0	600.0	600.0	20.0	120.0
600.0	610.0	600.0	10.0	120.0
610.0	620.0	620.0	20.0	140.0
620.0	630.0	620.0	10.0	140.0
630.0	640.0	640.0	20.0	DC

[1] The variable signal at A6A2J2 is used only within the Reference Section.

Fig 8-202
Sht 1 of 5



SERIAL PREFIX: 2234A

Fig 8-202
Sht 2 of 5

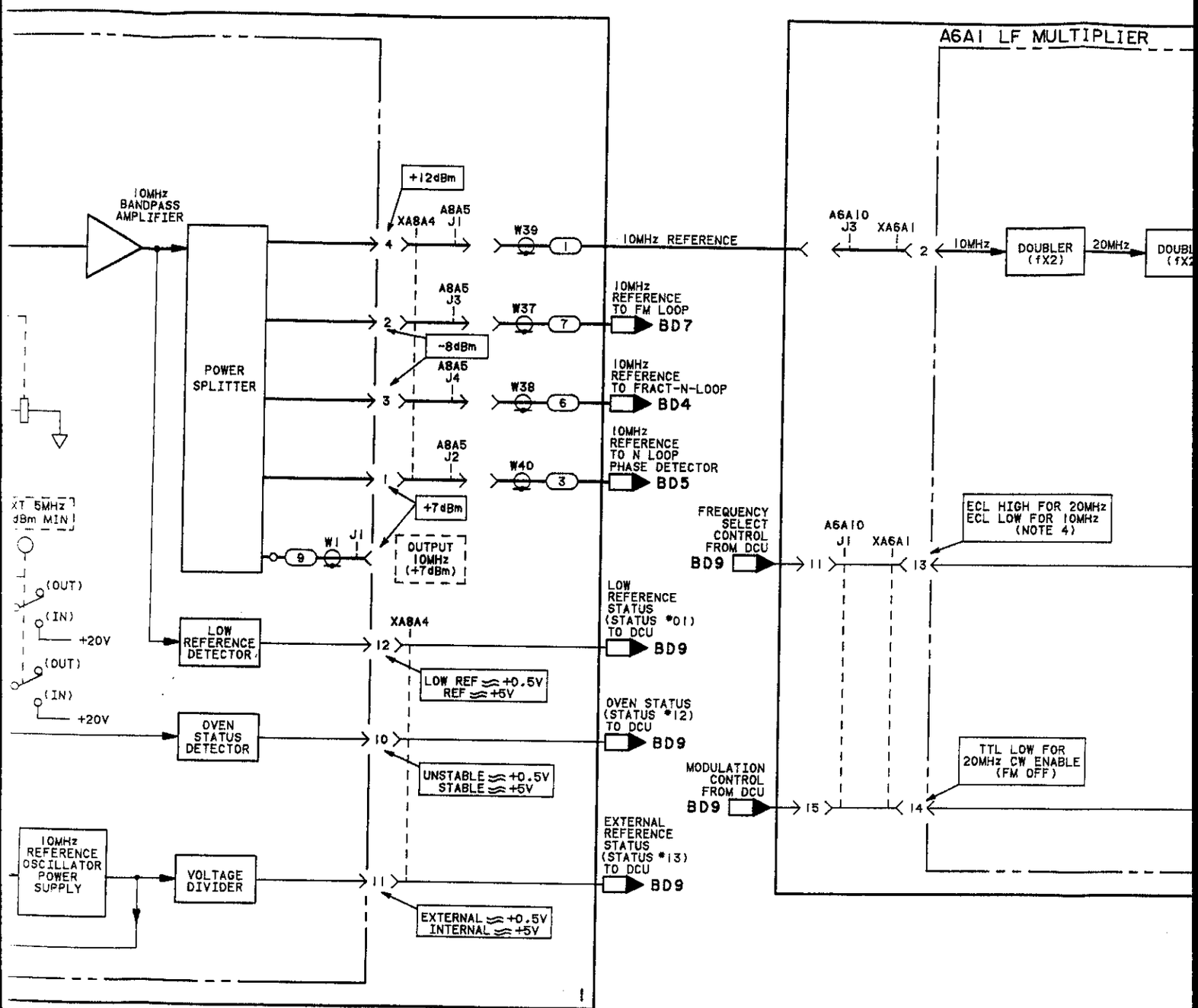


Fig 8-202
Sht 3 of 5

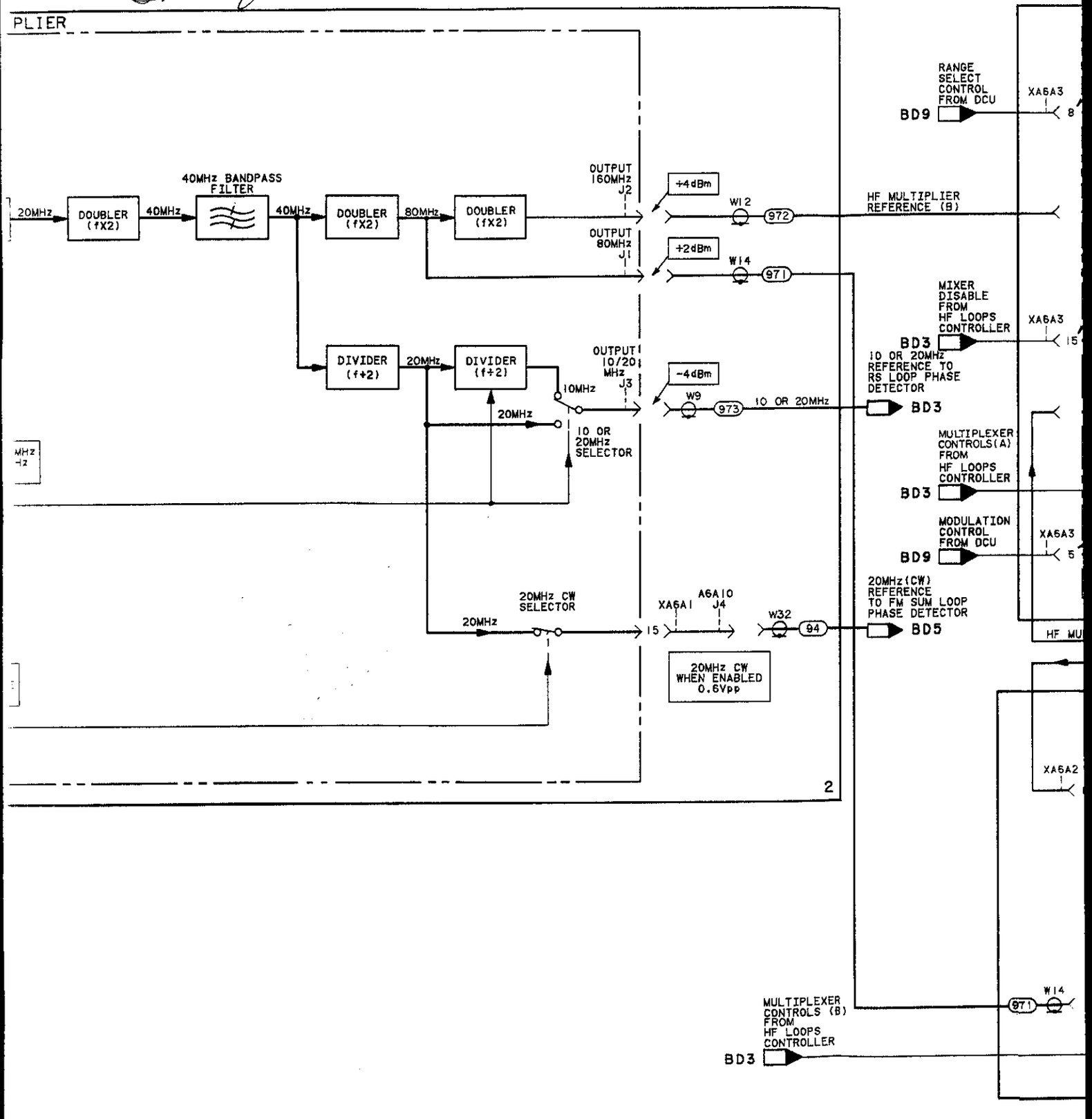


Fig 8-202
Sht 4 of 5

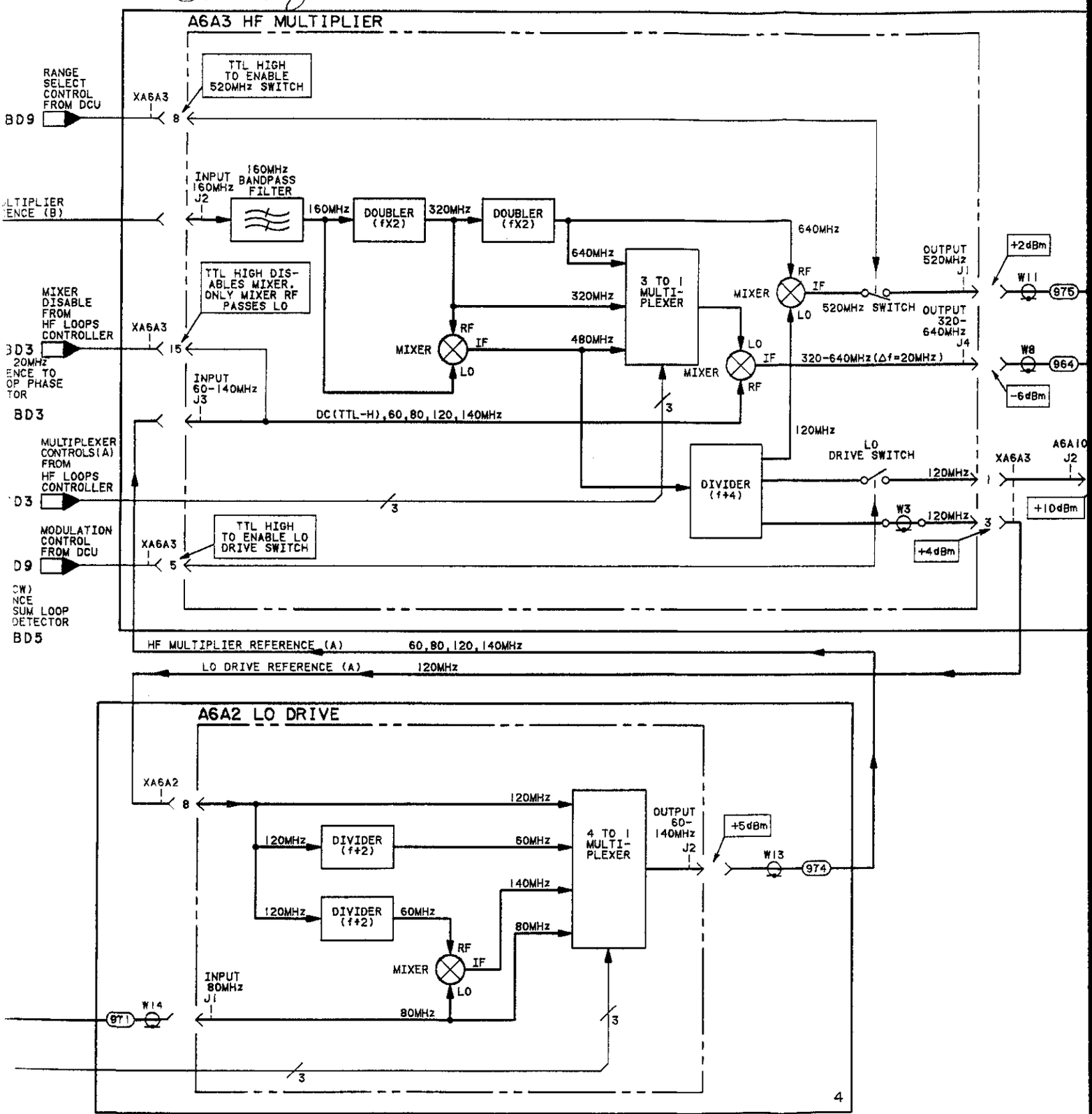
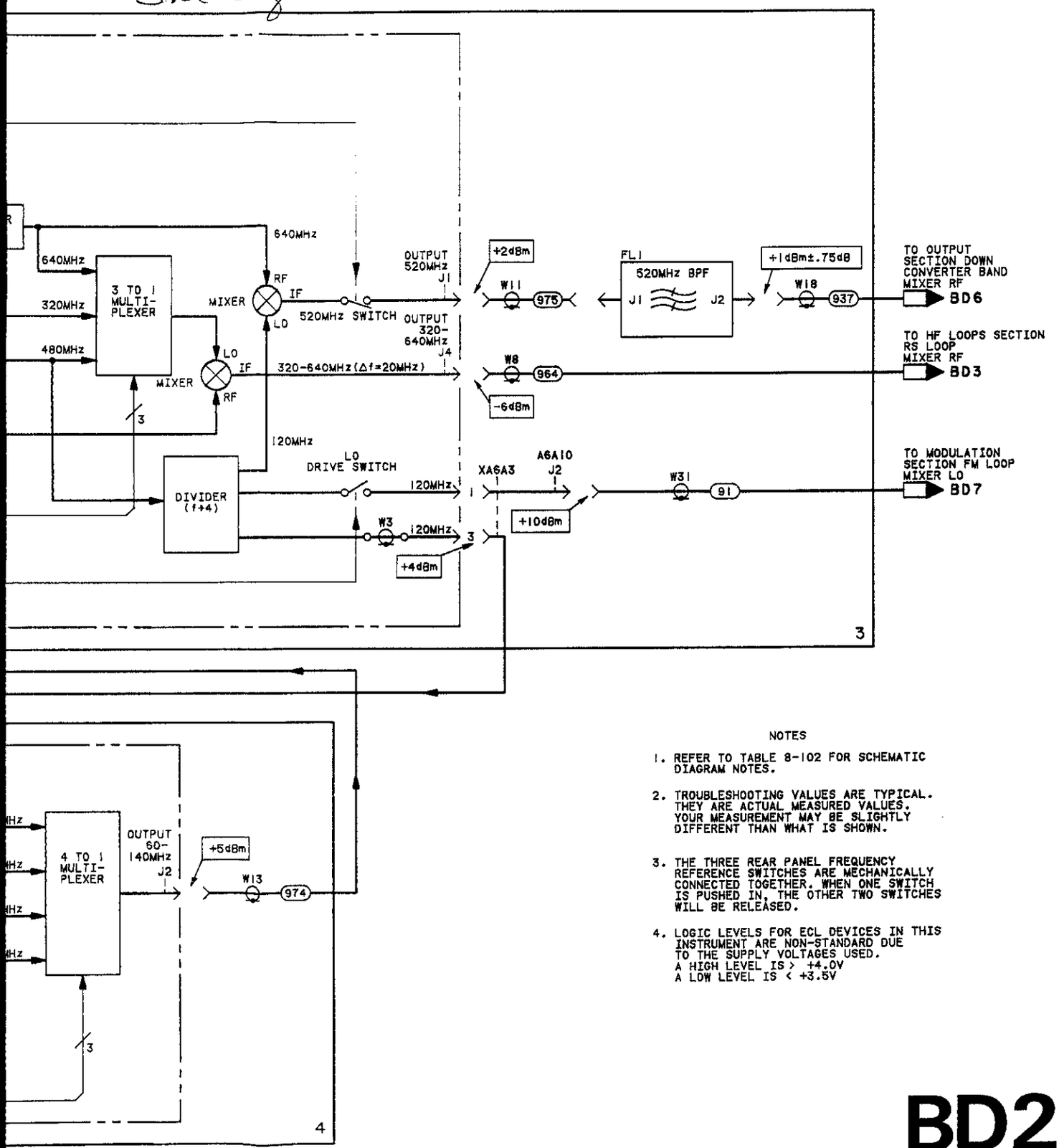


Fig 8-202
Sht 5 of 5



NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENT MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. THE THREE REAR PANEL FREQUENCY REFERENCE SWITCHES ARE MECHANICALLY CONNECTED TOGETHER. WHEN ONE SWITCH IS PUSHED IN, THE OTHER TWO SWITCHES WILL BE RELEASED.
4. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NON-STANDARD DUE TO THE SUPPLY VOLTAGES USED.
   A HIGH LEVEL IS > +4.0V
   A LOW LEVEL IS < +3.5V

BD2

Figure 8-202. Reference Section Block Diagram

SERVICE SHEET BD3
HIGH FREQUENCY LOOPS BLOCK DIAGRAM

REFERENCE BD1
Simplified Operation (Section III)
Operator's Checks (Section III)
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

The High Frequency Section generates the basic (fundamental) band which is sent to the Output section (Service Sheet BD6). This section employs two phase lock loops to generate the basic band. The 320 to 640 MHz and 10/20 MHz signals from the Reference Section are first mixed in the Reference Sum Loop to produce a 310 to 620 MHz, 10 MHz step resolution signal. This signal is then mixed in the Output Sum Loop with the 10 or 20 MHz, 0.1 Hz step resolution, signal from the Low Frequency Loops Section to produce the 320 MHz to 640 MHz , 0.1 Hz step resolution, basic band signal at the A8A1J3 output. Figure 8-203 is a block diagram of the basic high frequency loop. The only difference between the Reference Sum (RS) Loop and the Output Sum (OS) Loop is that, in the case of the RS Loop, the VCO output frequency is always less than the high frequency reference input at the mixer, whereas the opposite is true for the OS Loop. Coarse tuning and speedup is regulated by the Controller Board (Service Sheet 5) in the High Frequency Loops Section.

The frequency error circuits (Service Sheets 8 and 12) contain the frequency comparator and VCO correction circuitry. Under normal operating conditions, when the VCOs are locked, these lock acquisition circuits remain inactive. When the loop is un-locked, a beat note exists which is the difference between the loop IF down converted frequency and the reference frequency. If this beat note is within 200 kHz of the loop bandwidth (which is between 250 kHz and 500 kHz) the loop will acquire lock by itself. If the beat note is greater than the loop bandwidth by more than 200 kHz, the lock acquisition circuitry will be activated, coarsely tuning the VCO to within 200 kHz of the desired frequency. At this point, the phase lock loop will take over and complete the lock cycle.

TROUBLESHOOTING

When a problem has been traced to the High Frequency Loop section, this procedure can be used to isolate the problem to an assembly. The Reference Sum (RS) Loop must be locked before the Output Sum (OS) Loop will lock, therefore, work on the RS Loop first if both are unlocked.

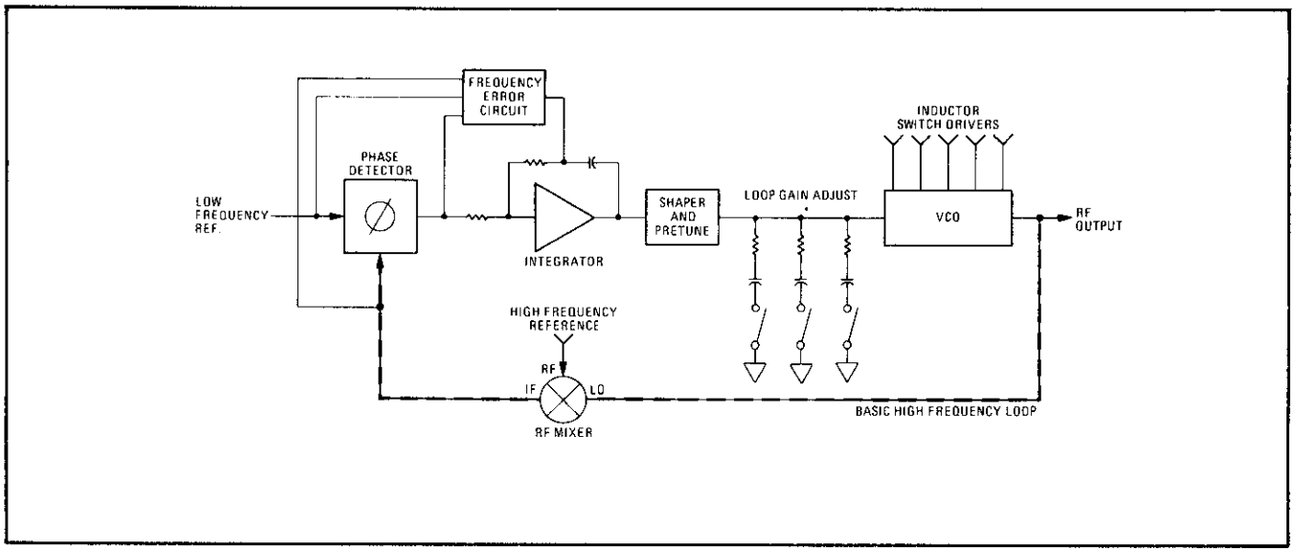


Figure 8-203. Basic High Frequency Loop Block Diagram

Procedure:

1. Set the front panel frequency to a value in the basic band (320.0 to 640.0 MHz). If the problem doesn't occur in this band, the fault is most likely in the Output Section (Service Sheet BD6) rather than the HF Loops Section.

2. Measure the input signals to the loop being tested. These input signals are described in Table 8-206. If any of the input signals are not normal, look for the problem at the source of the input signal.

3. Pull out the A6A4 (OS Loop) or A6A5 (RS Loop) assembly and move the slide switch to the TEST position. This opens the loop so the VCO can be checked. Use Table 8-207 or Table 8-208 depending on the loop being checked, and check the VCO output for the front panel frequency settings given in the table. If the VCO functions normally, continue troubleshooting with step 4. If the VCO output is not normal, check the two input signals to the VCO.

   a) The tuning voltage should be the value given in the table. If the voltage is not normal, there is most likely a problem in the pretuning circuitry on A6A4 or A6A5 (whichever drives the VCO where the problem exists).

   b) The inductor switch signals. The table states which inductor should be turned on. Sevice Sheet 5 shows the pin numbers where the switch signals can be measured and what the normal levels are. If the switch signals are not normal, the problem is most likely on A6A9.

   If the input signals are normal and the VCO output is bad, then the VCO is defective. The VCOs are not field-repairable. Exchange assemblies are available.

Table 8-206. HF Loops Input Signals

Loop	Signal	Where to Measure	Frequency	Level
Reference Sum	HF Reference	W38 (964) to A6A6J2	Table 8-209	-3 dBm
	10/20 Reference	W37 (973) to A6A5J1	Table 8-209	-4 dBm
Output Sum	FM Sum Loop Output	W28 (961) to A6A4J1	10-20 MHz	-3 dBm
	RS Loop Output	W43 (965) to A6A7J1	Table 8-209	+3 to -13 dBm

Table 8-207 Output Sum Loop VCO Pretuning Check (A8A1)

Front Panel Frequency Setting (MHz)	VCO Frequency * (± 3 MHz)	Bit On	Tuning Voltage (±1.0 Vdc) A6A4J2	Inductor On
524.0	527.5	None	-36.10	E
523.0	526.0	P1	-33.40	E
521.0	524.5	P2	-30.70	E
517.0	520.5	P4	-26.20	E
511.0	514.5	P8	-19.70	E
452.0	456.0	All	-13.00	D&C
330.0	334.0	None	-36.10	A
344.0	347.0	None	-36.10	B
370.0	375.0	None	-36.10	C
421.0	426.0	None	-36.10	D
524.0	527.5	None	-36.10	C

*Measure at W32 (935) at A4A3J1 (STD or OPTION 001), W29 (932) at A4A3J1 (OPTION 002 ONLY) or W46 (967) at A6A8J1.

Table 8-208. Reference Sum Loop VCO Pretuning Check (A8A2)

Front Panel Frequency Setting (MHz)	VCO Frequency* (±3 MHz)	Bit On	Tuning Voltage (±1.0 Vdc) A6A4J2	Inductor On
340.0	336.5	None	-36.10	A
350.0	346.5	P4	-26.60	B
380.0	376.0	None	-36.10	C
430.0	425.5	P1	-33.40	D
520.0	516.0	P8	-19.70	E
530.0	525.5	P2	-30.70	E

*Measure at W46 (967) at A6A8J1 and W43 (965) at A6A7J1.

Table 8-209. Reference Sum Loop Variable Frequency Signals

Front Panel Frequency Setting (MHz)	Reference Sum Loop Output (MHz) W43 (965) to A6A7J1	10/20 MHz Reference W37 (973) to A6A5J1	HF Reference (MHz) W38 (964) to A6A6J2
32X.X	310.0	10.0	320.0
33X.X	320.0	20.0	340.0
34X.X	330.0	10.0	
35X.X	340.0	20.0	360.0
36X.X	350.0	10.0	
37X.X	360.0	20.0	380.0
38X.X	370.0	10.0	
39X.X	380.0	20.0	400.0
40X.X	390.0	10.0	
41X.X	400.0	20.0	420.0
42X.X	410.0	10.0	
43X.X	420.0	20.0	440.0
44X.X	430.0	10.0	
45X.X	440.0	20.0	460.0
46X.X	450.0	10.0	
47X.X	460.0	20.0	480.0
48X.X	470.0	10.0	
49X.X	480.0	20.0	500.0
50X.X	490.0	10.0	
51X.X	500.0	20.0	520.0
52X.X	510.0	10.0	
53X.X	520.0	20.0	540.0
54X.X	530.0	10.0	
55X.X	540.0	20.0	560.0
56X.X	550.0	10.0	
57X.X	560.0	20.0	580.0
58X.X	570.0	10.0	
59X.X	580.0	20.0	600.0
60X.X	590.0	10.0	
61X.X	600.0	20.0	620.0
62X.X	610.0	10.0	
63X.X	620.0	20.0	640.0

Fig 8-204
Sht 1 of 4

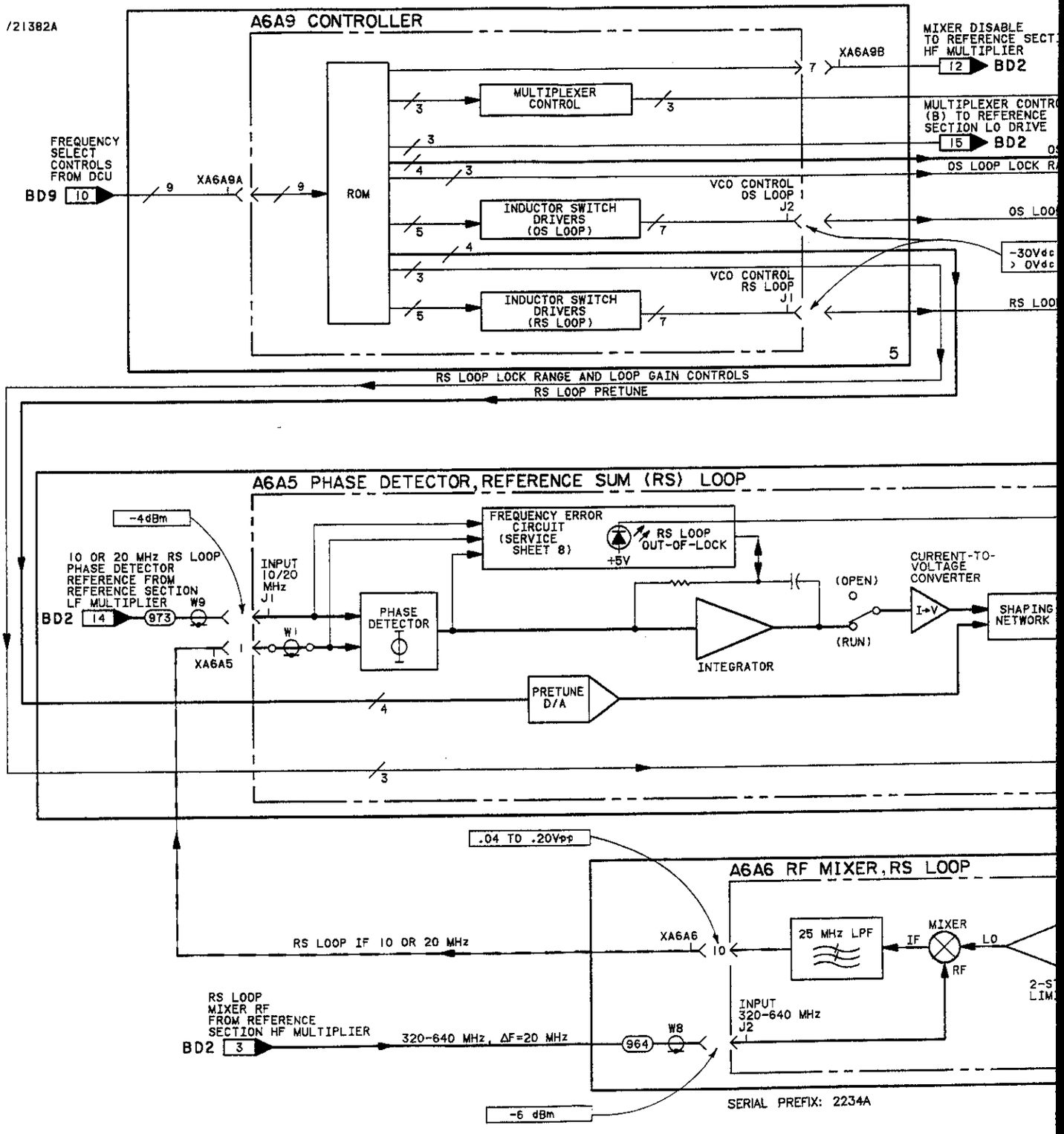


Fig 8-204
Sht 2 of 4

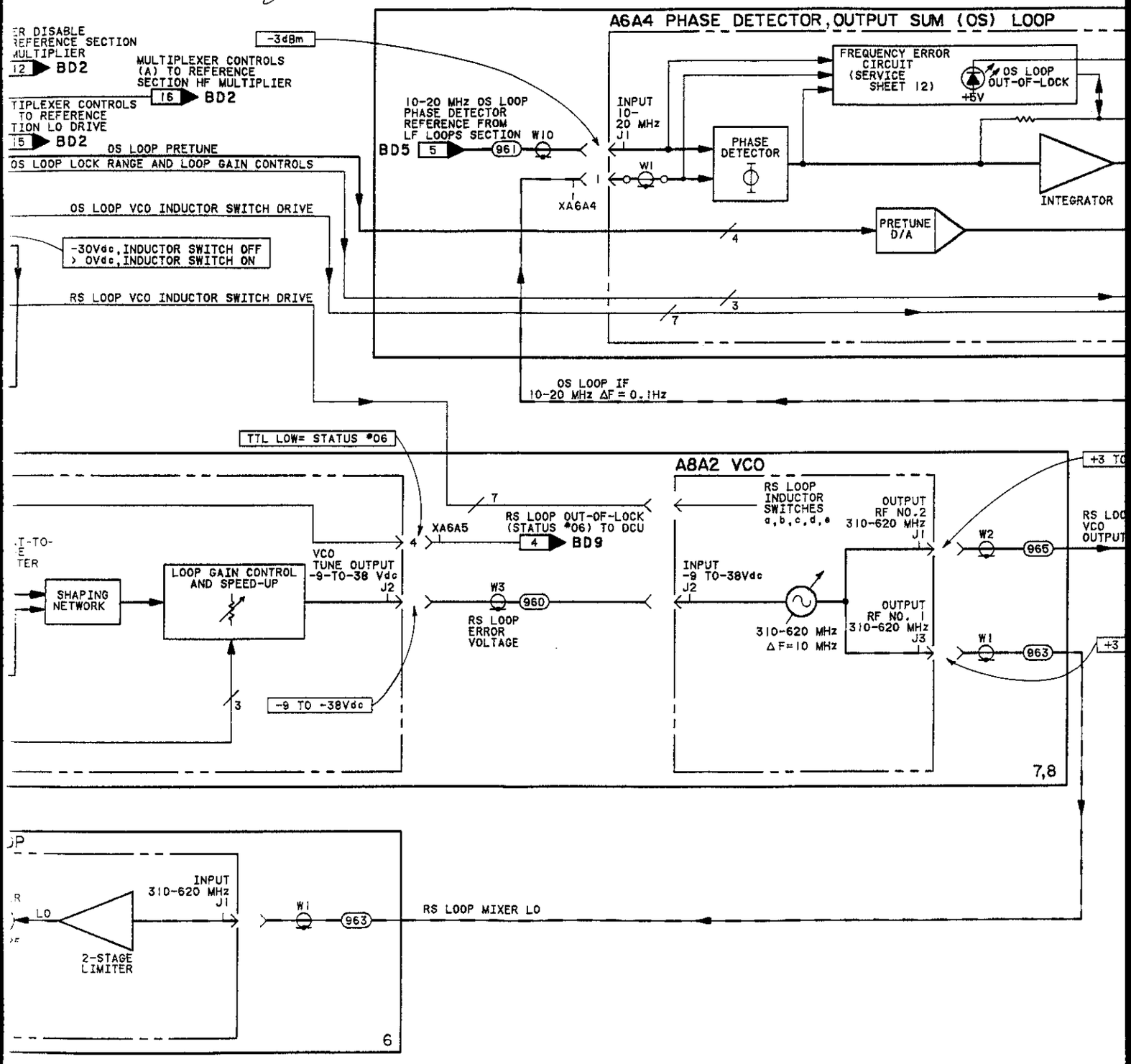


Fig 8-204
Sht 3 of 4

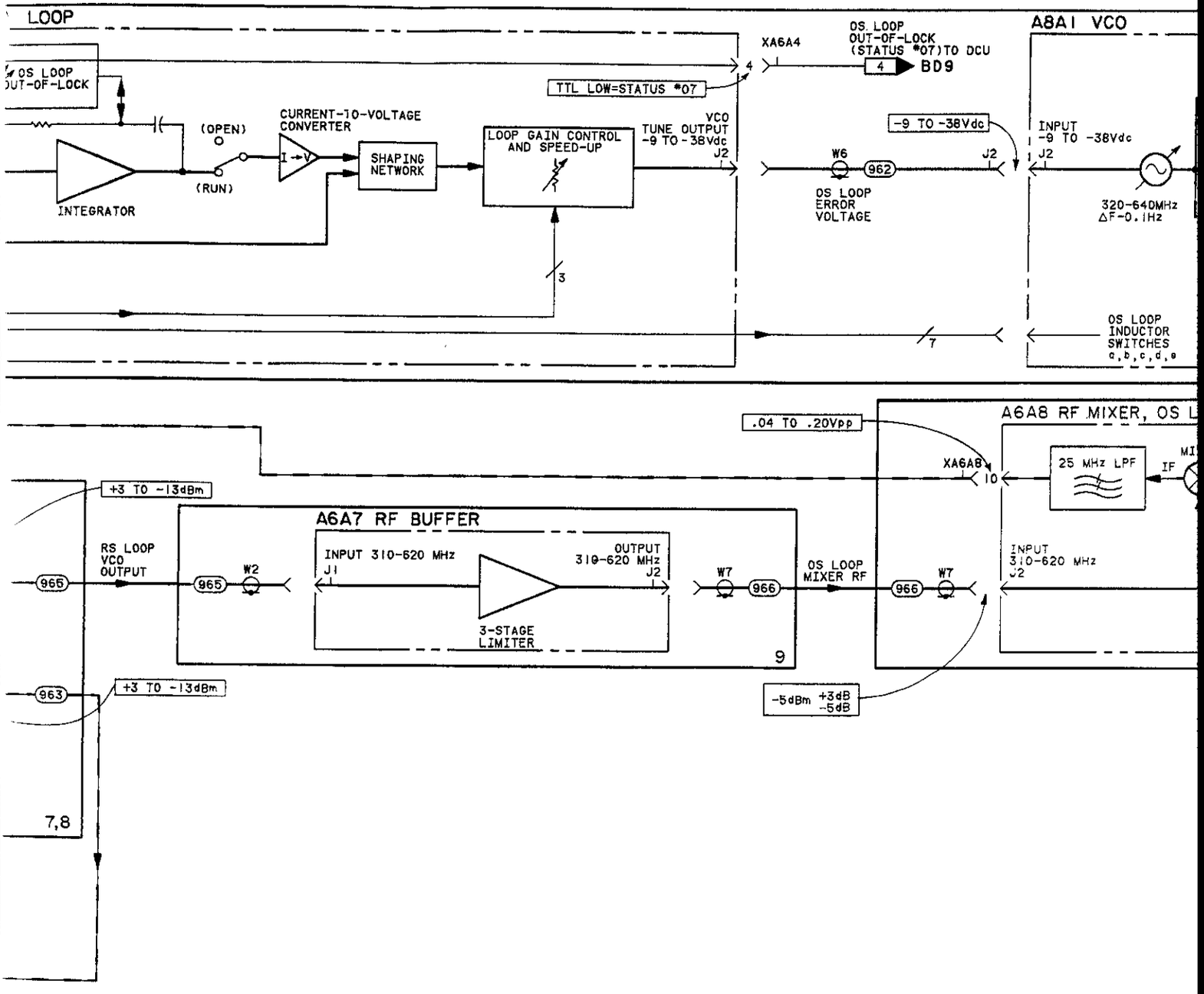
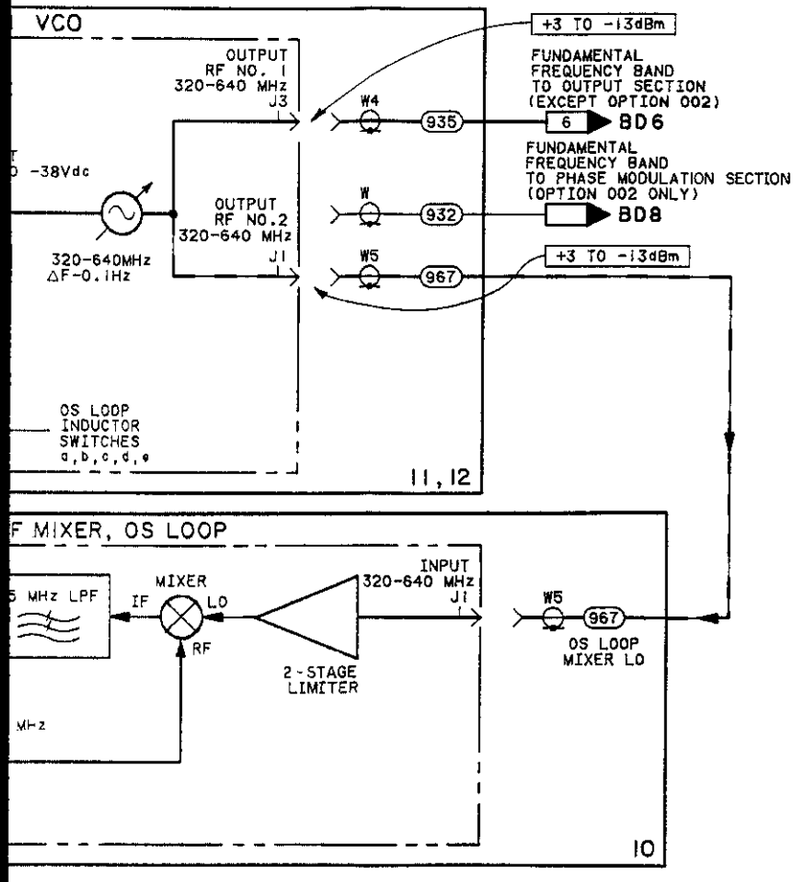


Fig 8-204
Sht 4 of 4



BD3

Figure 8-204. High Frequency Loops Block Diagram

SERVICE SHEET BD4
FRACTIONAL-N LOOP BLOCK DIAGRAM

REFERENCE BD1
Simplified Operation (Section III)
Operator's Checks (Section III)
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

The Fractional-N Loop (FN Loop) generates frequencies from 100 to 200 MHz in 100 Hz steps using a 100 kHz reference. The 100 kHz reference is derived by dividing the 10 MHz output signal from the Reference Section. The output frequency from this section is a function of front panel frequency digits D_5, D_4, D_3, D_2, D_1, and D_0 (that is, the six least significant digits) in the Generator's basic frequency band (that is, 320-640 MHz). The three least significant digits, D_2 - D_0, represent the fractional portion of the frequency while the next three digits (D_5 - D_3) contain the integer portion of the frequency. To determine the FN Loop VCO frequency from the front panel frequency display (RF OUTPUT frequency) use the following formula:

$$\text{FN VCO Freq.} = (200 - \underbrace{D_5\ D_4\ D_3}_{\text{Integer Portion}}\ \underbrace{D_2\ D_1\ D_0}_{\text{Fractional Portion}})\ \text{MHz}$$

The Fractional-N Loop uses a frequency synthesis technique known as Fractional N. With only one phase lock loop the FN Loop can produce signals with far greater frequency resolution than the traditional N Loop. In an N Loop, the VCO is restricted to only work at frequencies N times the reference frequency. Therefore, it can only generate signals that are integer multiples of the reference frequency (VCO Freq. = N x Ref Freq.).

The FN Loop is very similar to the N Loop. It contains all the basic elements of the N Loop with the addition of several new elements. In fact, if the selected frequency does not have a fractional part (that is, when D_2 - D_0 are zeros), the FN Loop works like the N Loop.

Figure 8-205 is a simplified block diagram of a Fractional-N phase lock loop with the shaded area containing the Fractional-N elements.

The major difference between the FN Loop and the N Loop is that the FN Loop VCO is not restricted to operating at only N times the reference frequency, but can also operate at frequencies that are fractional multiples of the reference frequency. The frequency resolution of the FN Loop is 100 Hz which means the FN VCO is capable of operating at a fractional multiple of 0.001 of the reference signal (0.001 of 100 kHz = 100 Hz).

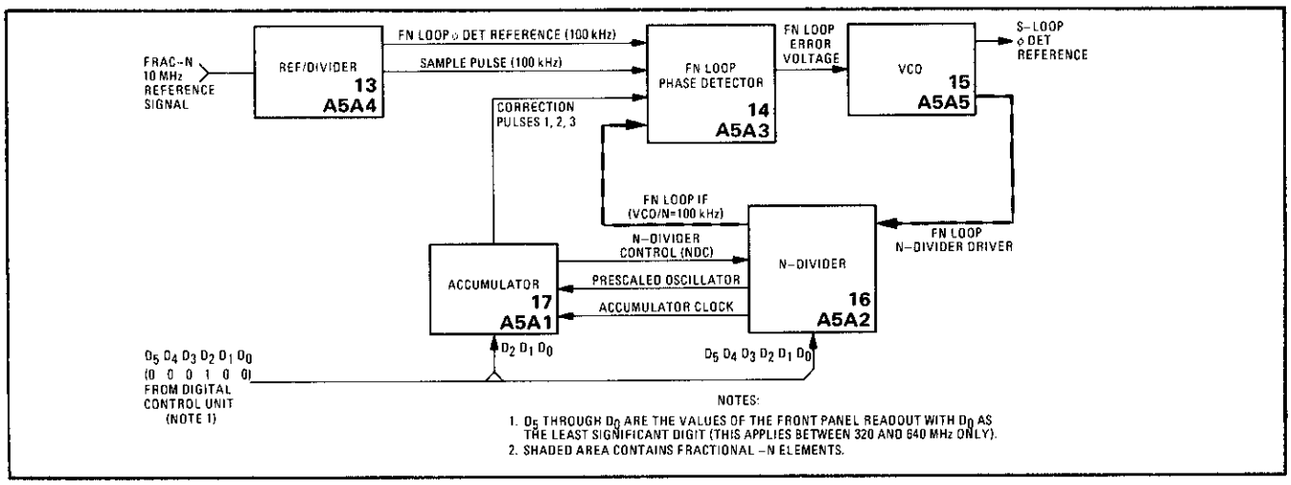


Figure 8-205. Simplified Block Diagram of Fractional-N Loop

Assume that the VCO frequency desired is 199.9900 MHz. In a traditional N Loop it would be impossible to phase lock the loop, since the desired VCO frequency, 199.9900 MHz, is a fractional multiple (1999.9) of the reference frequency. In order to phase lock the loop, the VCO frequency divided by N (VCO/N) must equal the 100 kHz reference signal. This would require an N that had a fractional component (N = 1999.9).

In the FN Loop, division by a fractional component is possible. The N Divider (A5A2) cannot divide by a fractional component directly but it is capable of changing from an N to an N-1 divider. Fractional division is accomplished by dividing by an integer (N) for the number of times and one less than the integer (N-1) for a number of times. The fractional N is then the average of N and N-1. For example, if an N of 1999.9 is required, the N Divider divides by 2000 (N) nine times and by 1999 (N-1) one time. This dividing between N and N-1 results in an average N of 1999.9.

A method of determining when to divide by N or N-1 is required. This is the purpose of the Accumulator (A5A1). When the FN Loop is operating with a fractional part, the VCO/N signal no longer equals the reference frequency, hence the phase difference between the two signals starts to increase. When analyzing the phase relationship between the reference and VCO/N signals, it is better to view it in terms of reference periods. A reference period is defined as the time required for the reference signal to complete one cycle (10 us). The Accumulator does not actually measure the phase difference but it computes what the phase difference should be after each reference period.

Since the phase difference is continuously increasing each reference period, the output from the phase detector is continuously increasing. In an N Loop the error voltage from the phase detector is used to tune the VCO frequency in a direction to reduce the phase difference or error. However, in the FN Loop, the phase difference is allowed to increase until the total or accumulated phase difference reaches or exceeds one full VCO cycle (360 degrees) of phase. Prior to the reference period that the phase difference

reaches or exceeds one full cycle, the Accumulator generates an N Divider Control (NDC) signal causing the N Divider to divide by one less than the previous N.

Dividing the FN VCO frequency by N-1 instead of N causes the N Divider to reach its terminal count one VCO period sooner. This effectively advances the VCO/N signal one VCO period which counteracts or cancels the previous phase advancement.

When the N Divider divides by a number N, the VCO/N signal starts to lag the reference signal. When the phase difference between the reference signal and the VCO/N signal reaches or exceeds one cycle of phase, the N Divider is programmed to divide by N-1 which now causes the VCO/N signal to lead the reference signal. The resulting averaged VCO/N signal equals the reference frequency and the loop can be phase-locked even though the instantaneous VCO frequency is not an integer-multiple of the reference.

In the example in Figure 8-206, the FN VCO is operating at 199.9900 MHz. That would require that the N Divider divide by an N equal to 1999.900. The N Divider is not capable of dividing by 1999.900 but it can divide by 2000 or 1999. The N Divider starts out dividing by 2000. Since the VCO operates at 199.9900 MHz and N = 2000, the VCO/N signal to the phase detector would be 99.9950 kHz. Note, the phase of the VCO/N signal starts to lag the 100 kHz reference frequency which causes the phase detector to output an ever increasing dc level.

As the reference signal goes through one cycle, the VCO (operating 1999.9 times faster) goes through 1999.9 cycles. For comparison, an N Loop circuit is also examined.

In an N Loop, if N = 2000 and reference = 100 kHz, the VCO frequency must equal 200.0 MHz to maintain phase lock. This means the N Loop goes through 2000.0 cycles for each reference period. Note the phase difference between the FN and N Loop VCO's after one reference period. The FN Loop lags the N Loop by 0.1 cycle which represents the fractional part of the frequency. To put it another way, the FN Loop VCO decreases by one tenth of a cycle relative to its integer part (N Loop) for every reference period. After the passage of two reference periods the FN VCO will have gone through 3999.8 cycles and the phase difference will have increased to 0.2 cycles. After each reference period the phase difference will increase by another 0.1 cycle. Table 8-210 illustrates this point.

After ten reference periods, the phase difference between the VCO/N and reference signals will have increased exactly one VCO cycle. Prior to the reference period that the phase difference reaches one

VCO cycle, the N Divider receives an NDC command from the Accumulator. This causes the N Divider to divide by 1999 (one integer less than 2000). This has the effect of cancelling the previous phase difference, hence the VCO/N frequency averaged over ten reference periods now equals the 100 kHz reference and therfore the loop can be phase locked.

Table 8-210. Phase Difference Versus Reference Periods

Number of Reference Periods	Cycles Per Reference Period		Phase Difference (Cycles of Phase)
	N-Loop = 200 MHz	FN Loop = 199.99 MHz (Fraction N = 0.1)	
1	2000	1999.9	0.1
2	4000	3999.8	0.2
3	6000	5999.7	0.3
4	8000	7999.6	0.4
5	10000	9999.5	0.5
6	12000	11999.4	0.6
7	14000	13999.3	0.7
8	16000	15999.2	0.8
9	18000	17999.1	0.9
10	20000	19999.0	1.0

This example uses a fractional N of 0.1. As another example, suppose the FN Loop VCO frequency was equal to 150.0050 MHz. This represents a fractional N of 0.95. For this example, the N Divider divides by N-1 (1500) nineteen out of twenty reference periods.

Continuously dividing by N and N-1 causes the phase detector to output a sawtooth waveform riding on a dc level. As shown in Figure 8-206, the output from the phase detector increases linearly (ramps) as the phase difference increases. The output continues to increase until the N Divider divides by N-1 which cancels the previous phase difference. This causes the output of the phase detector to return to its initial level.

The dc voltage level on which the sawtooth waveform is riding represents the proper tune voltage to phase-lock the VCO to the reference. Any ac components (sawtooth) on the dc tune voltage would prevent phase-lock and cause frequency modulation. To counteract this sawtooth waveform, an equal but opposite ac signal is generated by the Fractional-N Correction Pulse Width-to-Current Converters. This signal is then summed with the phase detector output to cancel the sawtooth components, leaving only the desired dc tuning voltage.

The fractional portion of the VCO frequency contains the information needed to develop the signal that counteracts the changing phase detector output. The fractional part of the frequency is presented to the Accumulator in BCD form. Once during each reference period the contents of the Accumulator are incremented by the fractional part. The number stored in the Accumulator corresponds to the difference in phase between the VCO/N and the reference signal.

Since the Accumulator is incremented each reference period, its contents represent an instantaneous fractional sum which grows until one VCO cycle of phase difference has occurred. The contents of the Accumulator as viewed with respect to time is shown in Figure 8-207. The contents of the Accumulator can be represented by a staircase ramp resetting each reference period when the N Divider divides by N-1. Note that the contents of the Accumulator when viewed graphically have the same characteristics as the sawtooth output from the phase detector.

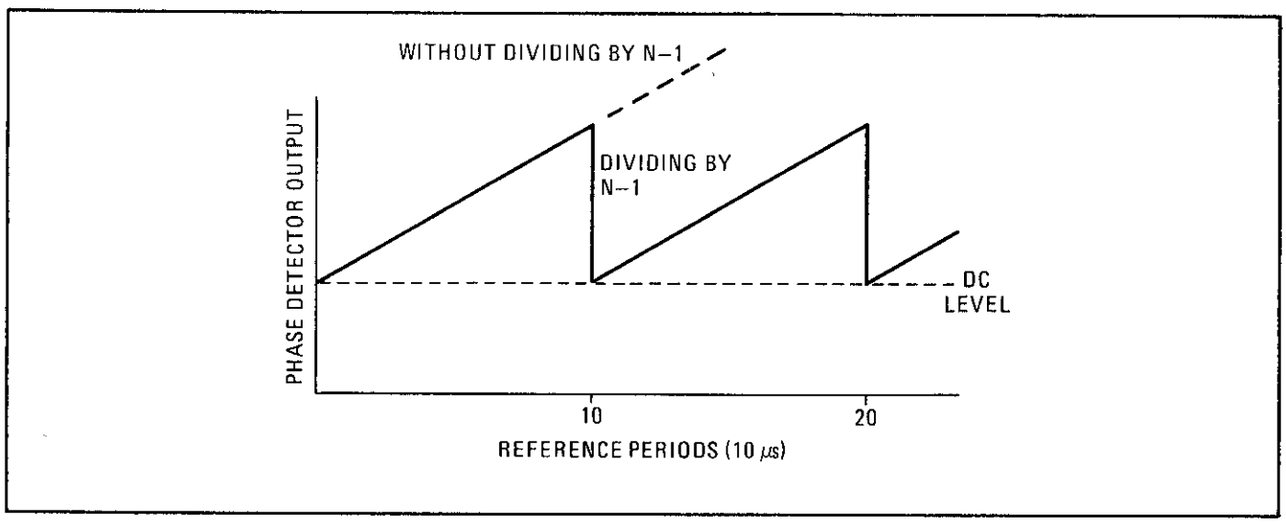


Figure 8-206. Phase Detector Output

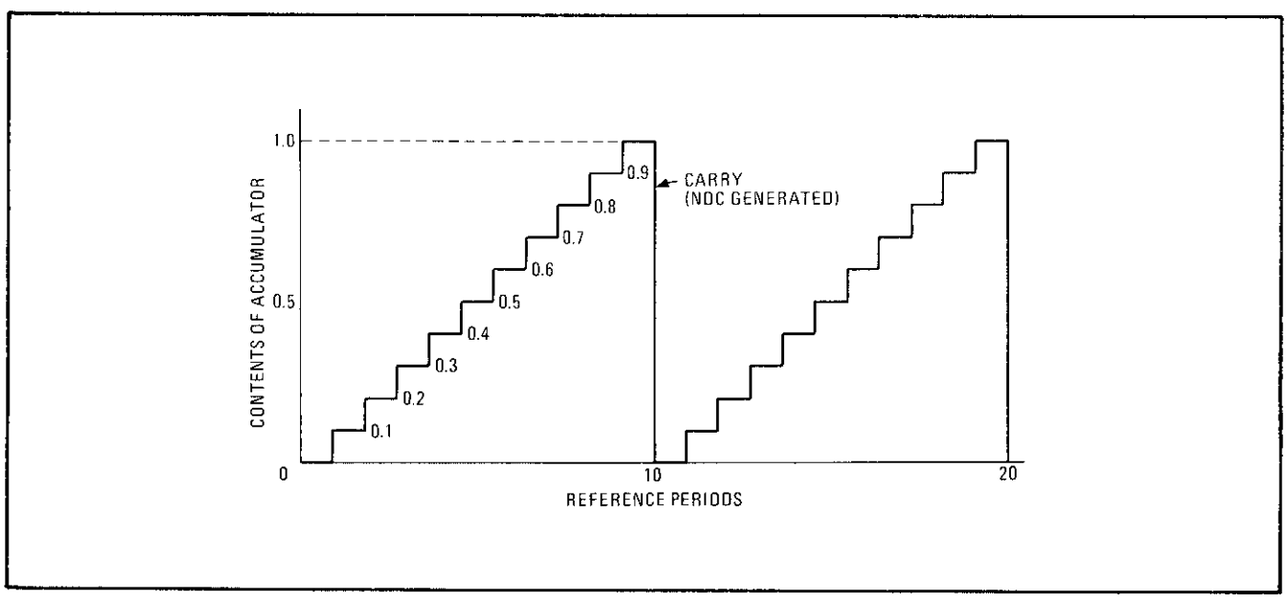


Figure 8-207. A Pictorial View of the Contents of the Accumulator

The numbers stored in the Accumulator are in BCD form. First the BCD information is inverted and then converted into signals with varying pulse widths. These signal lines are labeled Correction Pulse 1, 2, and 3. The Correction Pulses are then fed into the Pulse Width-to-Current Converter circuit which is located on the Fractional-N Loop Phase Detector Assembly (A5A3). The outputs from the Pulse Width-to-Current Converter circuit is then summed with the output from the phase detector. This cancels the sawtooth portion of the output fron the phase detector leaving only a clean dc tuning voltage for the VCO.

TROUBLESHOOTING

When a problem has been traced to the Fractional-N Loop or the instrument status code gives error 02, use the following procedure to isolate the problem to an assembly.

1. Check the 10 MHz reference signal at motherboard test point TP1. This signal should be the level shown on the block diagram.

2. Pull out the A5A1 Accumulator assembly. This removes the fractional part of the loop. Set the front panel frequency to 320.050 050 0 MHz. The loop should lock at a frequency of 149.0 MHz. Measure this frequency with a counter at A5A5J2. If the loop does lock, the Accumulator assembly is defective. If the loop doesn't lock, leave the Accumulator assembly out and continue with the next step.

3. Move the switch on the A5A3 Phase Detector Assembly to the TEST position. This opens the loop so that only the pretuning circuitry is driving the VCO. Set the Front panel frequency to the values in Table 8-211 and measure the VCO frequency at A5A5J2. This tests all the bits in the pretuning by turning on but one at a time.

Table 8-211. Fractional-N Loop Troubleshooting

Front Panel Frequency Setting (MHz)	Pretuning Bit On	A5A5 VCO Frequency Measured at A5A5J2 (MHz ±3 MHz)
320.011	All	102
320.080	D5-8	122
320.040	D5-4	162
320.020	D5-2	182
320.010	D5-1	192
320.008	D4-8	194
320.004	D4-4	198
320.0	None	202

If all these frequencies are within limits, the VCO and pretuning are good. This is most of the A5A5 assembly so proceed to the next step. If one or more frequencies are bad, the problem is on the A5A5 assembly.

4. Measure the PDV signal from the A5A2 N Divider Assembly at TP5 on the motherboard. The frequency of this signal should be 100 kHz ± 5 kHz. Use an oscilloscope to check that levels of this signal are valid TTL levels (high is greater than 2.4 Vdc and low is less than 0.8 Vdc). If this signal is correct, the A5A2 assembly is operating properly, otherwise, there is a problem on the A5A2.

5. Measure the PDR and SMP signals fron the A5A4 Reference Divider Assembly on the motherboard at TP3 (PDR) and TP2 (SMP). The frequency of both these signals should be 100.0 kHz. Look at the waveforms on an oscilloscope to check for valid TTL levels and the timing relationship between the waveforms as shown in Figure 8-208.

   If these signals are correct, the A5A4 is operating properly, otherwise, there is a problem on A5A4.

6. If all the previous checks do not show any problems, the A5A3 Phase Detector is the most likely cause of the problem.

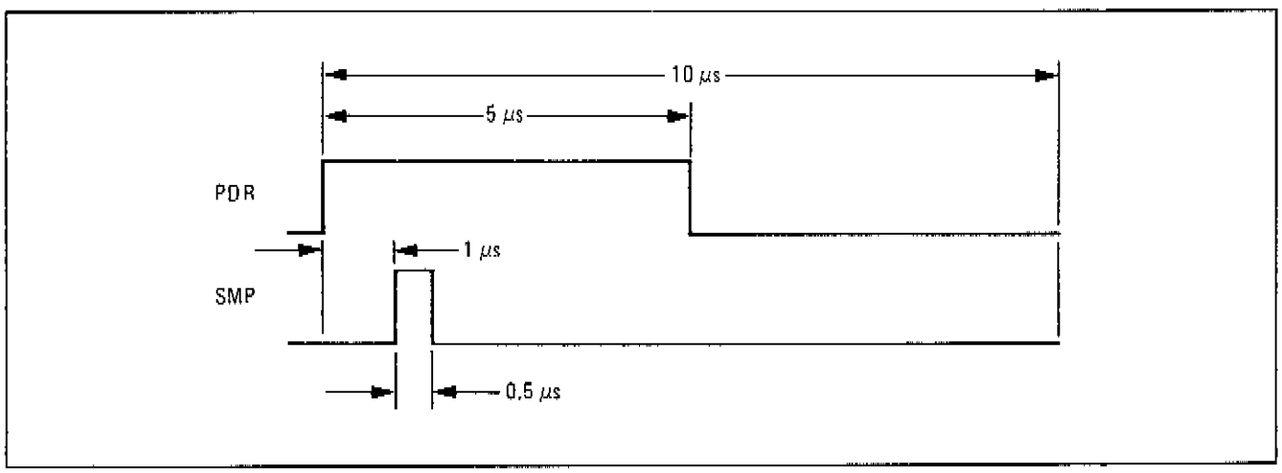


Figure 8-208. Timing Diagram for 100.0 kHz PDR and SMP Signals

Fig 8-209
Sht 1 of 4

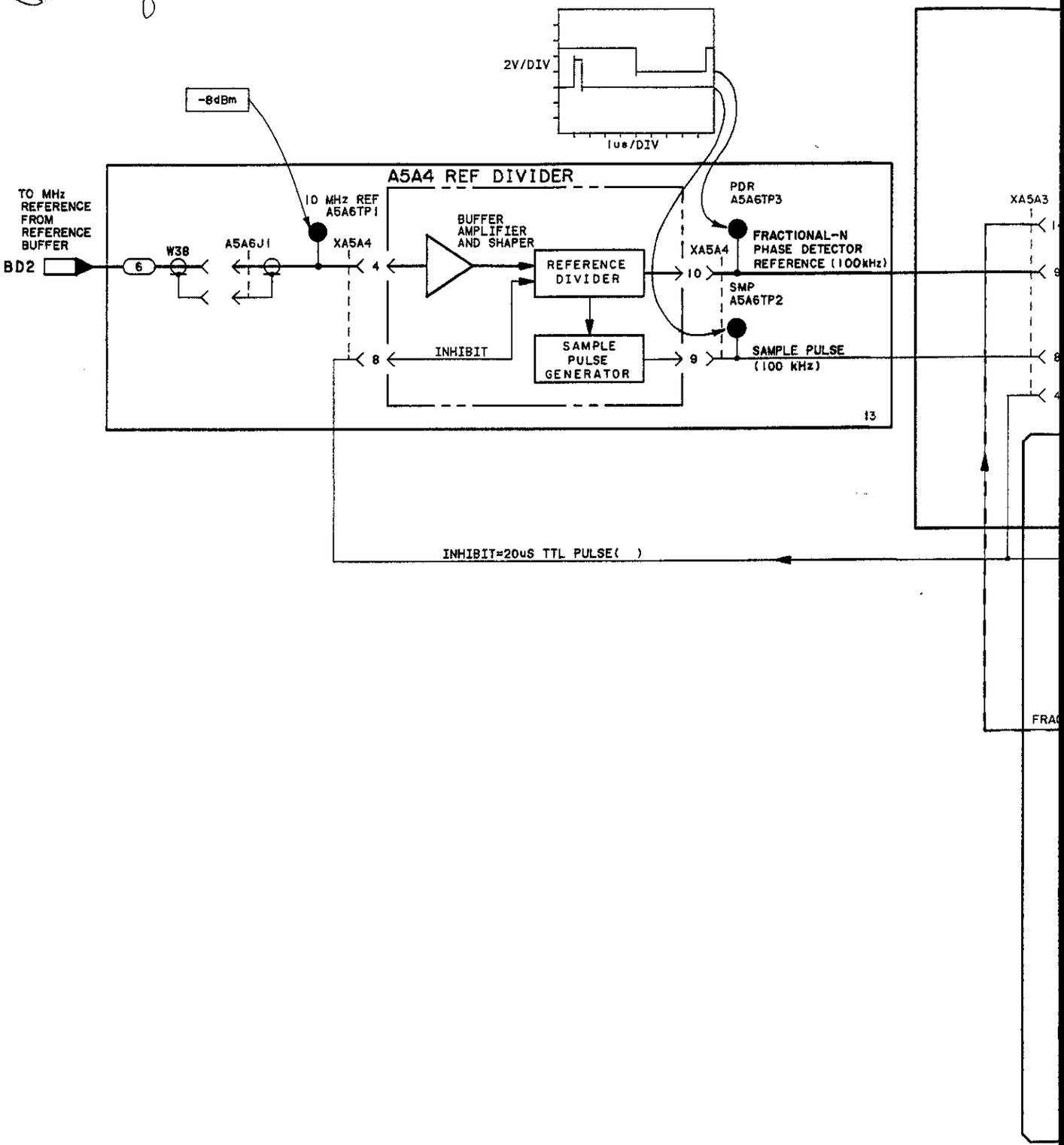


Fig 8-209
Sht 3 of 4

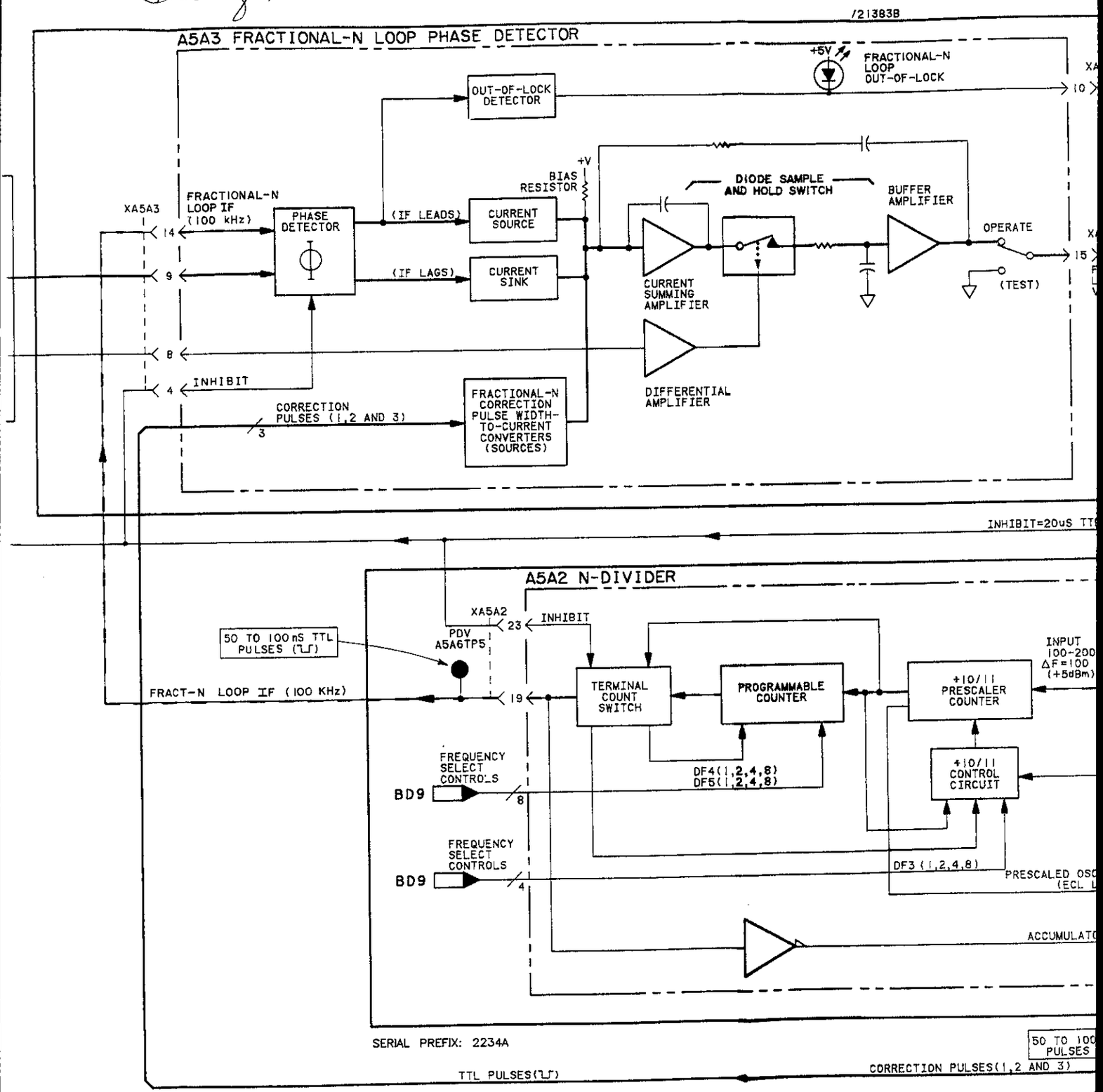


Fig 8-209
Sht 3 of 4

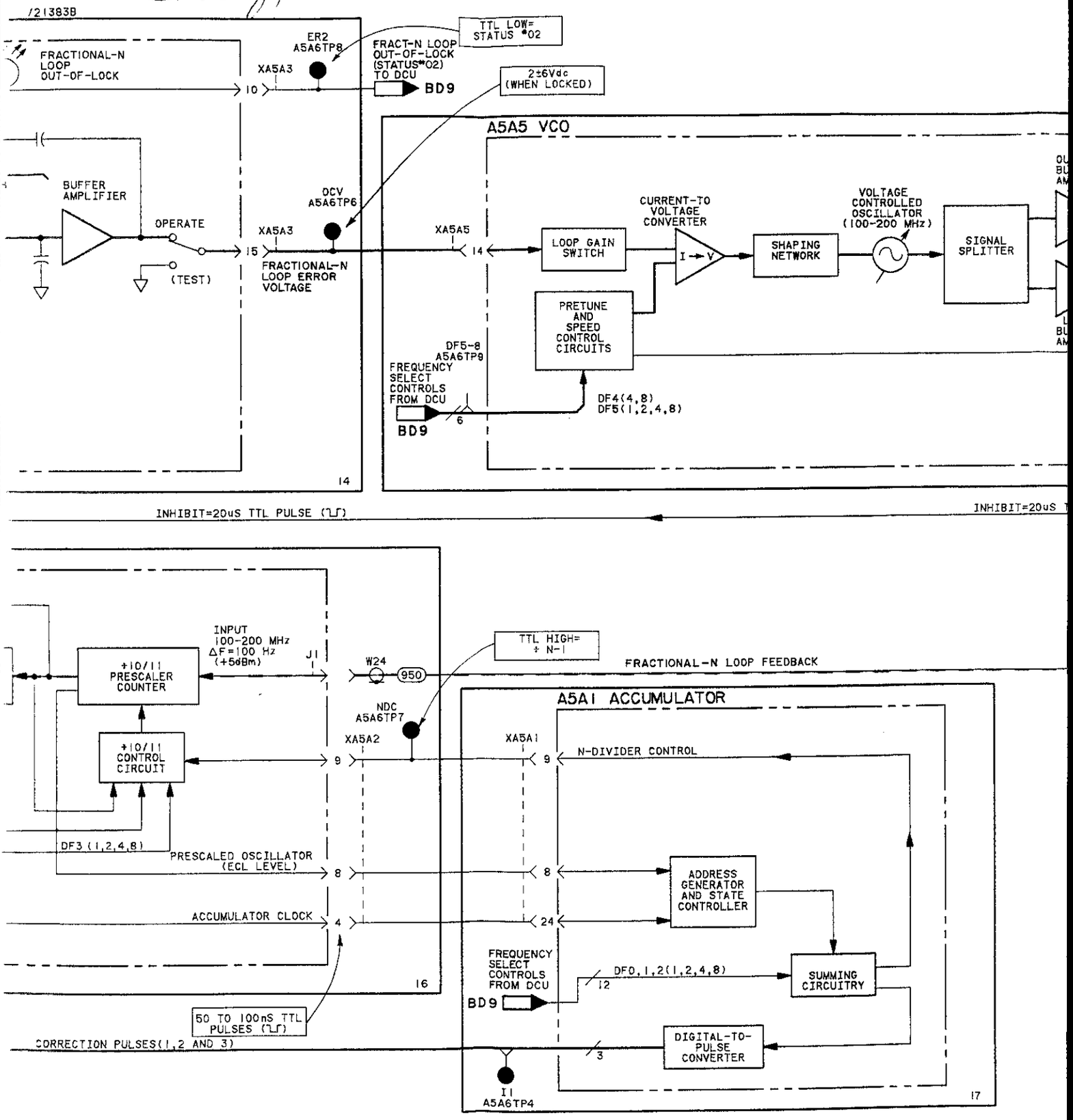
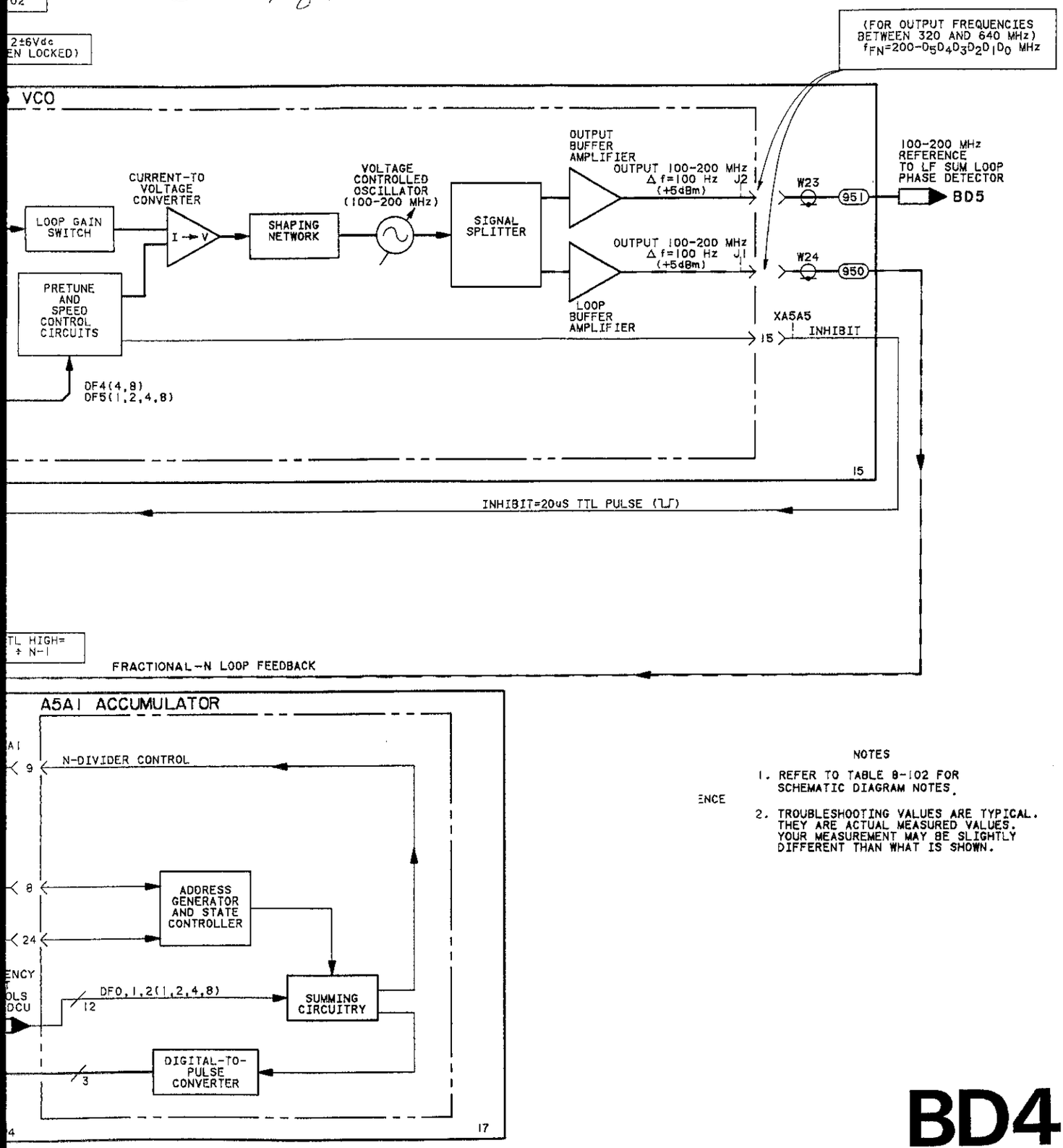


Fig 8-209
Sht 4 of 4



NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENT MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

BD4

Figure 8-209. Fractional-N Loops Block Diagram

SERVICE SHEET BD5
LOW FREQUENCY LOOPS BLOCK DIAGRAM

REFERENCE BD1
Simplified Operation (Section III)
Operator's Checks (Section III)
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

The Low Frequency Loops Section serves two functions. First, it produces the 10 MHz to 20 MHz reference signal which is sent to the input of the phase detector (in the Output Sum Loop of the High Frequency Loops Section) so that the 320 MHz to 640 MHz, 0.1 Hz step resolution, fundamental frequency band can be generated. Secondly, if FM is desired at the output, it is summed in at this point.

The Low Frequency Loops are composed of three principal sections: the N Loop, the Low Frequency Sum Loop, and the FM Sum Loop. Each is a discrete phase lock loop. The N Loop takes the 10 MHz reference signal (which must be greater than +7 dBm) and multiplies it, using fractional-N synthesis, to a frequency band of 122 MHz to 221 MHz (1 MHz step resolution). This frequency is related to the 1 MHz and 0.1 MHz digits of the front panel frequency display (D7 and D6 in the basic frequency band).

The signal from the N Loop is sent to the Low Frequency Sum Loop where it is locked to the signal from the Fractional-N Loop (Service Sheet BD4). This signal varies between 100 MHz and 200 MHz (100 Hz step resolution), but is divided by two decade counters (divide by 100) in the Low Frequency Sum Loop so that it varies between 1 MHz and 2 MHz (with 1 Hz resolution) at the input ot the phase detector. The output of the Low Frequency Sum Loop (120 MHz to 220 MHz, 1 Hz step resolution) is sent to the FM Sum Loop.

In the FM Sum Loop, the signal is summed with either a 20 MHz continuous wave (CW) signal from the Reference Section or a 20 MHz frequency modulated signal from the Modulation Section (Service Sheet BD7). The output of this loop is a 100 MHz to 200 MHz (1 Hz step resolution) signal which is passed through a decade divider before leaving the board. The output of the decade divider is a frequency band which extends from 10 MHz to 20 MHz in 0.1 Hz steps. This signal is sent to the phase detector in the Output Sum Loop of the High Frequency Loops Section at 0 dBm to +16 dBm.

TROUBLESHOOTING

General

There are three phase lock loops in this section. The hierarchy is:

- N Loop (Error code 03)
- Sum Loop (Error code 04)
- FM Sum Loop (Error code 05)

There is a separate troubleshooting procedure for each loop. If more than one of the loops is unlocked, always start with the highest order unlocked loop because it will cause the lower order loops to be unlocked. If the front panel status display gives a hardware malfunction code of 03, 04, or 05, then this code indicates at which loop to start troubleshooting.

N-Loop Troubleshooting

When it has been determined that there is a problem in the Low Frequency N Loop by troubleshooting on the Overall Block Diagram (Service Sheet BD1) or the out-of-lock indicator being lit, perform the following sequence to isolate the defective assembly:

1. Unplug the A3A3 assembly and remove it from the instrument. This opens the loop and leaves the A3A4 assembly being driven by only the pretune voltage from A3A6. Set the front panel frequency to the values in the first column of the table on the block diagram. Measure the VCO frequency at A3A4J2 and compare it to the normal values given in the table. Each frequency setting turns on one bit of the eight which drive the pretune circuitry. If the VCO frequencies are correct, the A3A4 VCO assembly is operating properly and the A3A3 divider/phase detector assembly is the likely cause of the problem. In this case, proceed to Service sheet 18 and troubleshoot the A3A3 assembly.

2. When the VCO frequencies are not correct, proceed with the Sum Loop troubleshooting.

Sum Loop Troubleshooting

When it has been determined that there is a problem in the Low Frequency Sum Loop by troubleshooting on the overall block diagram (Service Sheet BD1) or the out-of-lock indicator being lit, perform the following sequence to isolate the defective assembly:

1. Remove the two jumpers on the A3A7 VCO Assembly and plug the board back into its socket. Removing these jumpers opens the loop and the VCO is driven only by the pretuning voltage from the A3A6 assembly.

2. Set the front panel frequency to the values in the first column of the table on the block diagram. Measure the VCO frequency at A3A7J1 and compare to the normal values given in the table. Each frequency setting turns on one bit of the eight which drive the pretune circuitry. If the VCO frequencies are correct, the A3A7 VCO is operating properly so proceed to step 4 to continue troubleshooting.

3. When the VCO frequencies are not correct, try the following:

   a) Perform the open-loop pretune adjustment procedure on the block diagram. If these adjustments can be made, repeat step 2. Otherwise, continue below.

   b) Measure the pretune voltage (TP8 on the motherboard) for the front panel frequency settings given in the table on the block diagram. If these voltages are not normal, trace the problem starting with the pretune circuitry on A3A6.

   If the open-loop pretune adjustments cannot be made but the pretune voltages (TP8) are normal, the A3A7 VCO is faulty.

4. Set the front panel frequency to 320.0 MHz. Adjust the GAIN control on A3A7 to set the VCO output frequency at A3A7J2 to 120.0 $\pm$0.5 MHz. The W23 cable must be in place on A3A7J2.

   Check the following:

   a) a 2.0 $\pm$0.5 MHz signal at TP5 on the motherboard. Amplitude >3 Vp-p.

   b) A steady TTL low signal at TP7 on the motherboard. This is the frequency detector output.

   c) A steady TTL low signal at pin 11 of A3A5. This is the out-of-lock signal from A3A6 which should be active (low) when the loop is open.

5. Turn the A3A7 GAIN adjustment counter-clockwise (CCW) while monitoring the frequency of the mixer output at TP5 on the motherboard. Turning the GAIN adjustment CCW increases the VCO frequency. The N Loop output is at 122 MHz so the mixer output (TP5) should decrease in frequency, reach zero and begin increasing. When the frequency reaches zero and begins to increase, check TP7 on the motherboard for positive going TTL pulses. This is the output of the frequency detector and pulses indicate that the VCO is higher than the N Loop output.

   If any of these checks gives abnormal results, the problem is likely on the A3A5 assembly, otherwise, the A3A6 Phase Detector assembly is the likely cause of the problem.

FM Sum Loop Troubleshooting

When it has been determined that there is a problem in the FM Sum Loop by troubleshooting on the overall block diagram (Service Sheet BD1) or the out-of-lock indicator being lit, perform the following sequence to isolate the defective assembly:

1. Pull the A3A9 Mixer assembly up far enough so that the bottom edge connector is completely out of the motherboard connector, but leave all the RF cables connected to the top of the assembly. This opens the loop by disconnecting the phase detector drive circuitry but leaves the mixer connected. In this condition, the VCO is only driven by the pretune voltage from A3A6. Set the front panel frequency to the values in the first column of the table in the block diagram. measure the A3A8 VCO frequency at A3A8J3 and compare it to the normal values given in the table. Each frequency setting turns on one bit of the eight which drive the pretune circuitry.

2. If the VCO frequencies are correct, the A3A8 VCO is operating properly. Check that the outputs at A3A8J1 and A3A8J2 are the proper level as stated on the block diagram. Notice that the frequency at A3A8J2 is one-tenth that of the other outputs. Proceed to step 3 to continue troubleshooting. When the VCO frequencies are not correct, try the following:

   a) Perform the open-loop pretune adjustment procedure on the block diagram. If these adjusments can be made, repeat the VCO check. Otherwise, continue below.

   b) Measure the pretune voltage (TP8 on the motherboard) for the front panel frequency settings given in the table on the block diagram. If these voltages are not normal, trace the problem starting with the pretune circuitry on A3A6.

   If the open-loop pretune adjustments cannot be made but the pretune voltages (TP8) are normal, the A3A8 VCO is faulty.

3. Measure the output of the mixer at A3A9J2. Set the front panel frequency to the values in the first column of the table on the block diagram. The loop should still be opened by having A3A9 out of the motherboard socket. The frequency output of the mixer should be 20 MHz $\pm$ 4 MHz for all front panel frequency settings, and the level should be as stated on the block diagram. If correct, the mixer portion of A3A9 is good. Connect cable W27 to A3A9J2 but leave A3A9 out of the cottom connector.

4. The phase detector on A3A10 is a double balanced mixer so the frequency of the output will be the difference between a 20 MHz reference signal and the nominal 20 MHz IF signal from the mixer on A3A9. Using any front panel frequency setting, vary the GAIN adjustment on the top of A3A8 VCO assembly to vary the frequency of the IF signal. Turning the GAIN adjustment clockwise increases the frequency of the IF signal. The normal cable must be connected to A3A9J2 but the IF signal can be monitored there with the <u>high</u> <u>impedance</u> of a counter by using a T adaptor. Vary

the input IF frequency above and below 20 MHz and look for the difference signal at A3A10 pin 14.

5. Monitor the frequency detector output at A3A10 pin 12. Vary the IF signal frequency using the A3A8 GAIN adjustment and check the frequency detector output with the values shown in Table 8-212.

   The GAIN adjustment is coarse so the IF signal frequency cannot be controlled precisely. The IF signal frequency limits in the table should be considered approximations. It is important to verify that three different output states of the frequency detector exist but not that they occur at precise values of IF frequency.

Table 8-212. IF Signal vs Frequency Detector Output

IF Signal	Frequency Detector Output (A3A10 pin 12)
>21 MHz	dc level > +1.5 Vdc
<19 MHz	dc level < -3.0 Vdc
20 ±1 MHz	pulses high-low levels change as IF goes above and below 20 MHz

6. If both the phase detector and the frequency detector operate normally as described previously, the A3A10 assembly is probably normal. Therefore, the problem is most likely with the active circuitry on the A3A9 assembly.

Fig 8-210
Sht 1 of 5

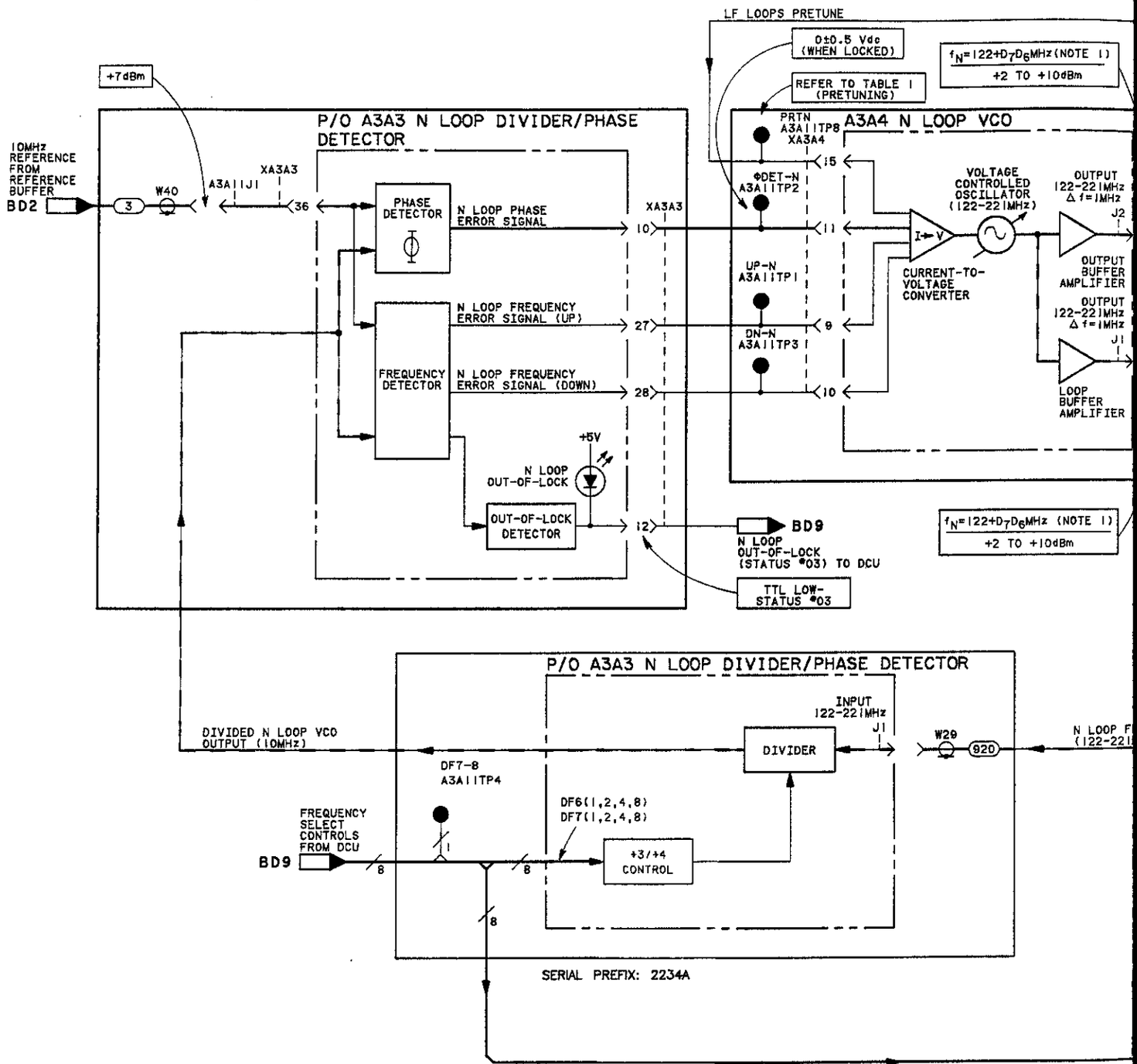


Fig 8-210
Sht 2 of 5

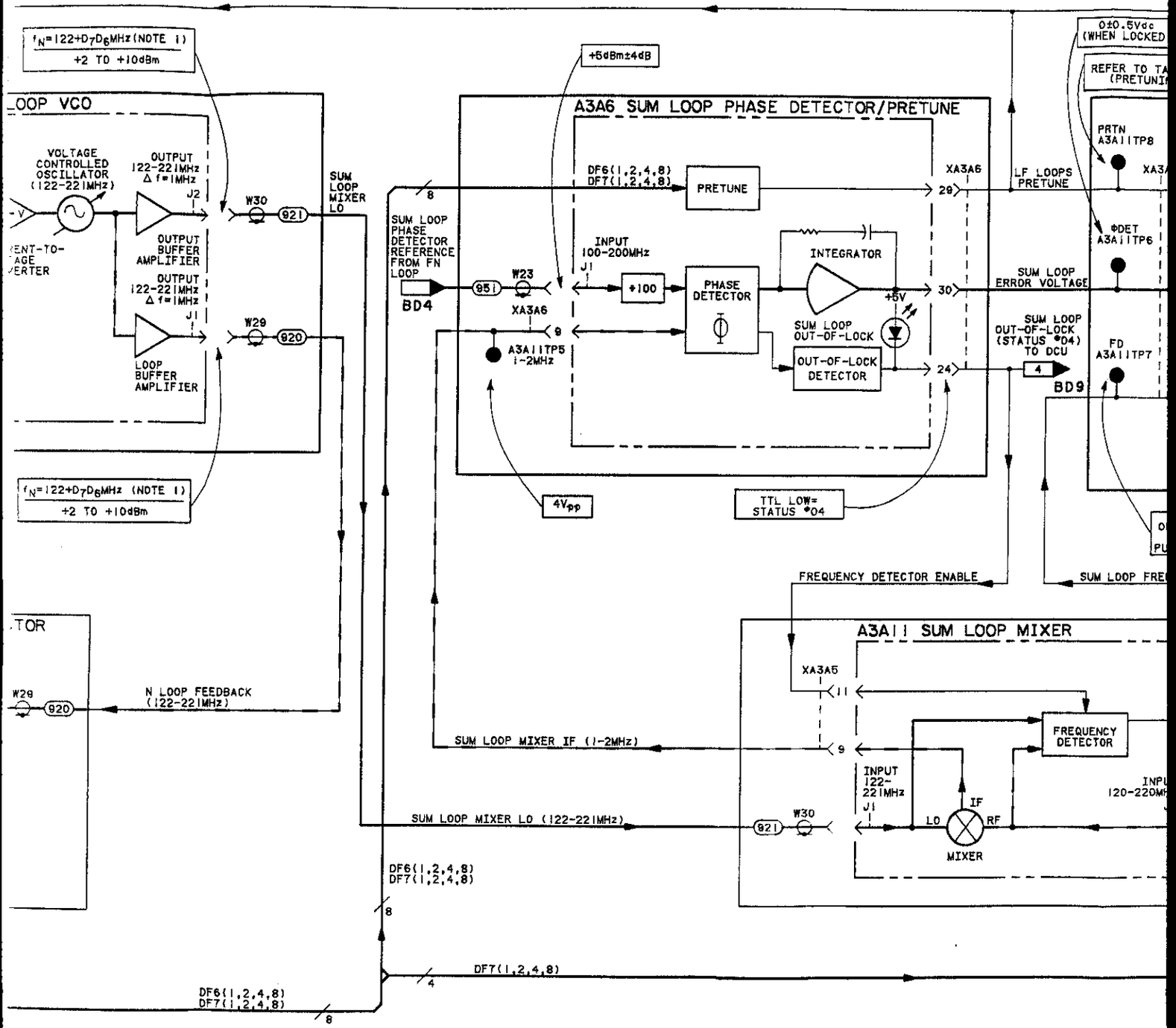


Fig 8-210
Sh 3 of 5

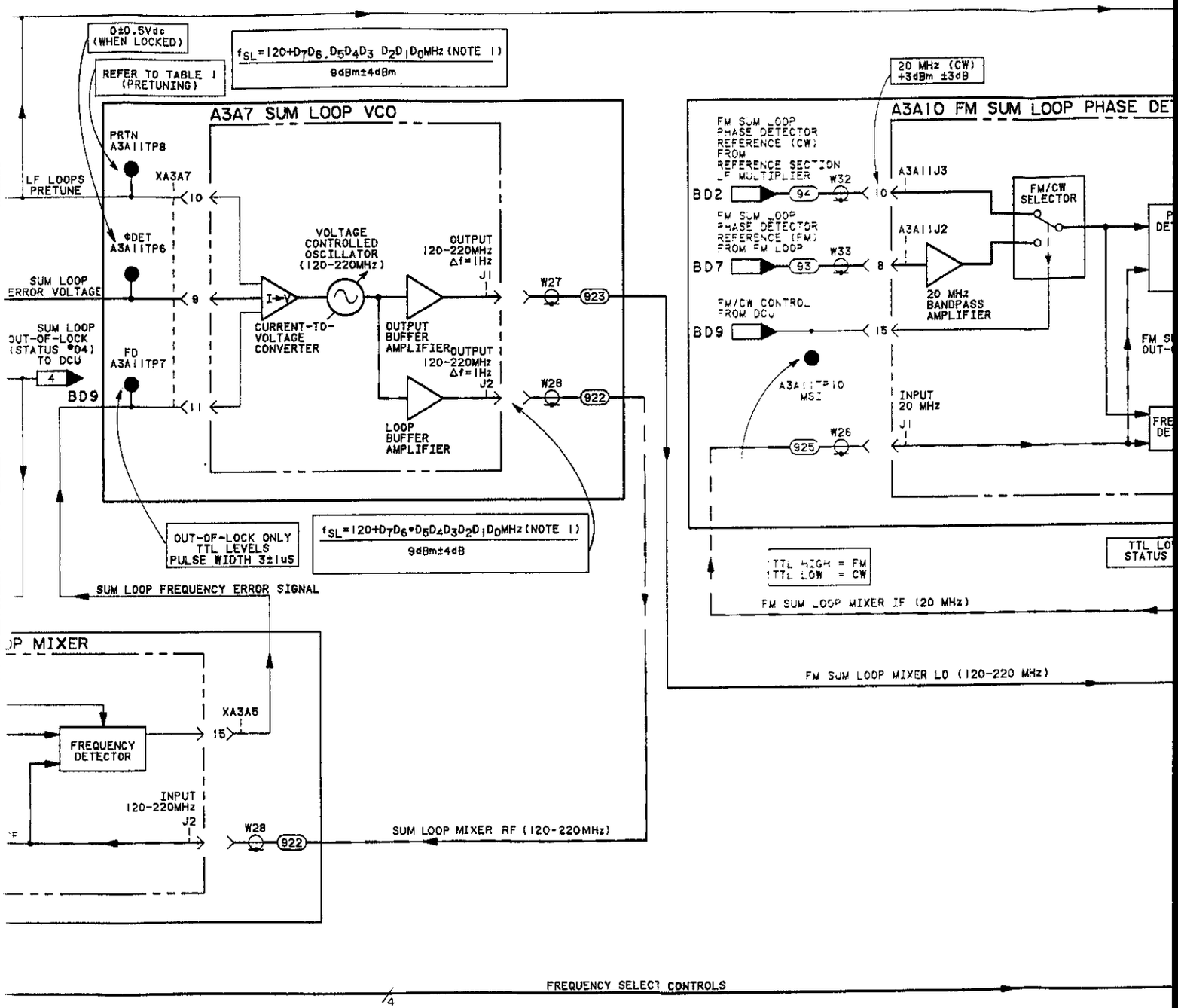
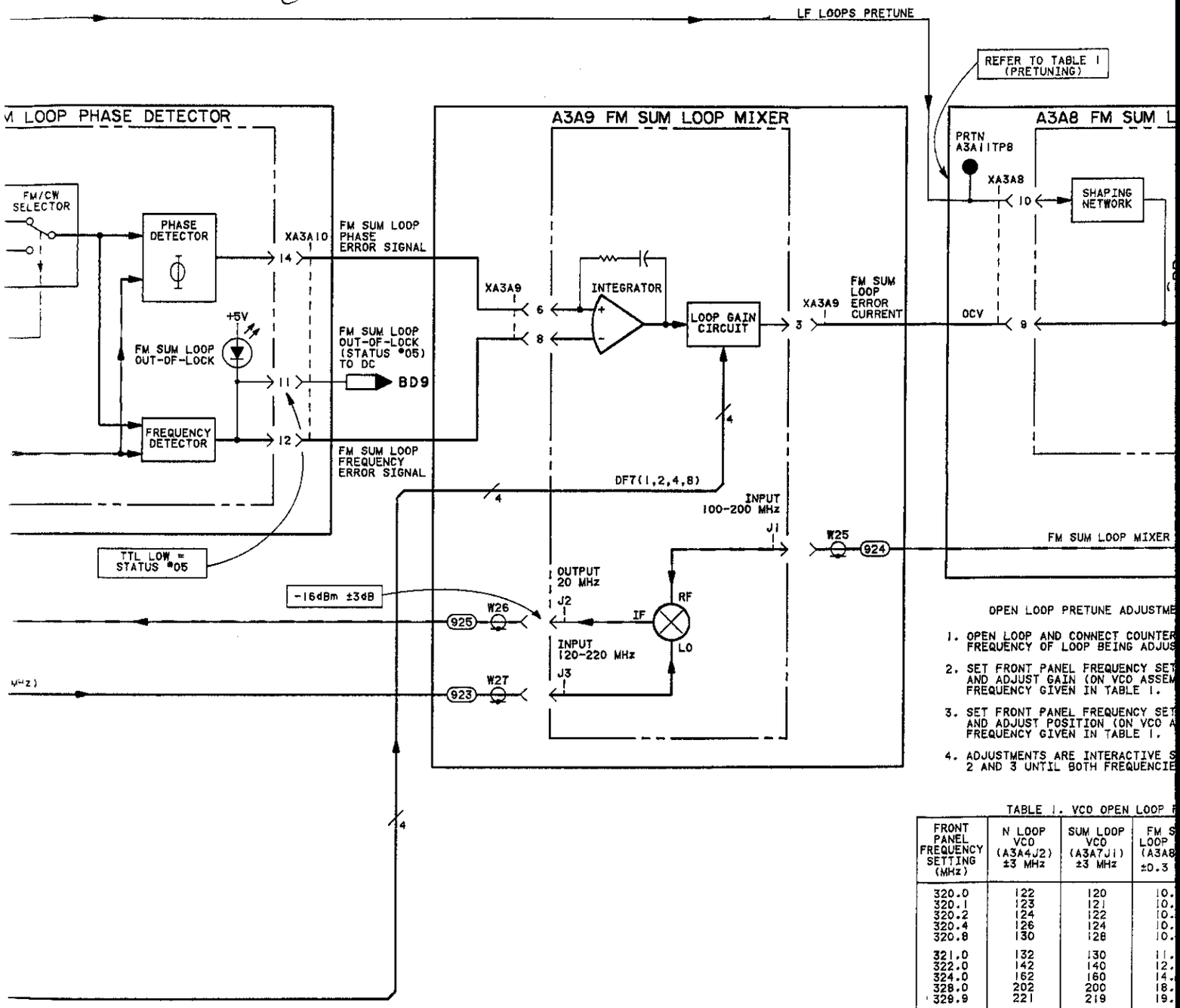


Fig 8-210
Sht 4 of 5



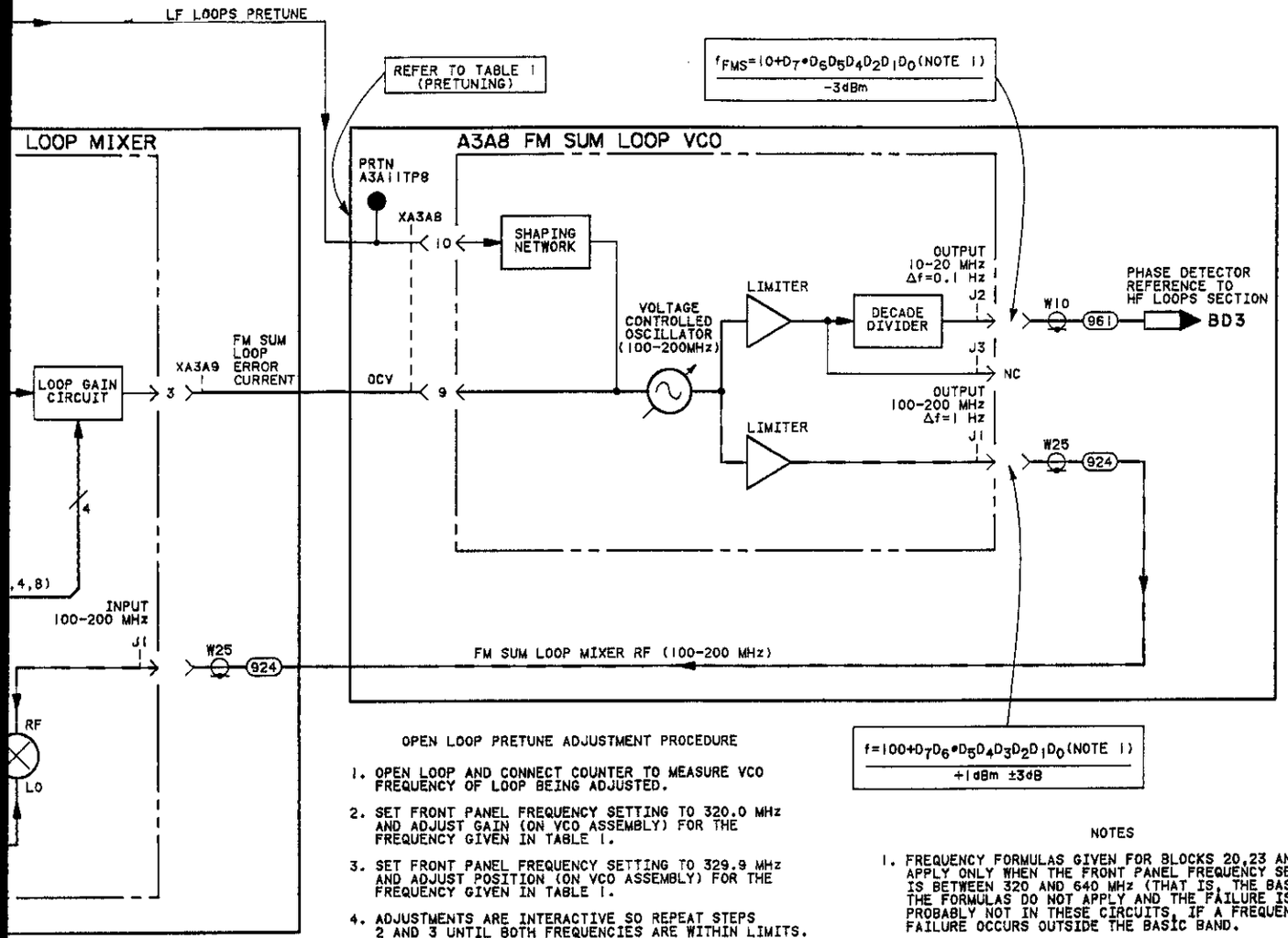
OPEN LOOP PRETUNE ADJUSTME

1. OPEN LOOP AND CONNECT COUNTER FREQUENCY OF LOOP BEING ADJUS
2. SET FRONT PANEL FREQUENCY SET AND ADJUST GAIN (ON VCO ASSEM FREQUENCY GIVEN IN TABLE I.
3. SET FRONT PANEL FREQUENCY SET AND ADJUST POSITION (ON VCO A FREQUENCY GIVEN IN TABLE I.
4. ADJUSTMENTS ARE INTERACTIVE S 2 AND 3 UNTIL BOTH FREQUENCIE

TABLE I. VCO OPEN LOOP F

FRONT PANEL FREQUENCY SETTING (MHz)	N LOOP VCO (A3A4J2) ±3 MHz	SUM LOOP VCO (A3A7J1) ±3 MHz	FM S LOOP (A3A8 ±0.3
320.0	122	120	10.
320.1	123	121	10.
320.2	124	122	10.
320.4	126	124	10.
320.8	130	128	10.
321.0	132	130	11.
322.0	142	140	12.
324.0	162	160	14.
328.0	202	200	18.
329.9	221	219	19.

Fig 8-210
Sht 5 of 5



OPEN LOOP PRETUNE ADJUSTMENT PROCEDURE

1. OPEN LOOP AND CONNECT COUNTER TO MEASURE VCO FREQUENCY OF LOOP BEING ADJUSTED.
2. SET FRONT PANEL FREQUENCY SETTING TO 320.0 MHz AND ADJUST GAIN (ON VCO ASSEMBLY) FOR THE FREQUENCY GIVEN IN TABLE 1.
3. SET FRONT PANEL FREQUENCY SETTING TO 329.9 MHz AND ADJUST POSITION (ON VCO ASSEMBLY) FOR THE FREQUENCY GIVEN IN TABLE 1.
4. ADJUSTMENTS ARE INTERACTIVE SO REPEAT STEPS 2 AND 3 UNTIL BOTH FREQUENCIES ARE WITHIN LIMITS.

TABLE 1. VCO OPEN LOOP FREQUENCIES

FRONT PANEL FREQUENCY SETTING (MHz)	N LOOP VCO (A3A4J2) ±3 MHz	SUM LOOP VCO (A3A7J1) ±3 MHz	FM SUM LOOP VCO (A3A8J2) ±0.3 MHz	PRETUNING	
				VOLTAGE (A3A11TP8) ±0.5Vdc	BIT ON
320.0	122	120	10.0	7.34	NONE
320.1	123	121	10.1	7.28	DF6-1
320.2	124	122	10.2	7.22	DF6-2
320.4	126	124	10.4	7.08	DF6-4
320.8	130	128	10.8	6.84	DF6-8
321.0	132	130	11.0	6.74	DF7-1
322.0	142	140	12.0	6.12	DF7-2
324.0	162	160	14.0	4.89	DF7-4
328.0	202	200	18.0	2.44	DF7-8
329.9	221	219	19.9	1.27	ALL

NOTES

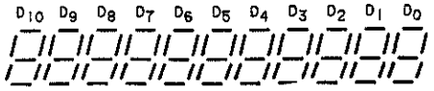
1. FREQUENCY FORMULAS GIVEN FOR BLOCKS 20,23 AND 26 APPLY ONLY WHEN THE FRONT PANEL FREQUENCY SETTING IS BETWEEN 320 AND 640 MHz (THAT IS, THE BASIC BAND). THE FORMULAS DO NOT APPLY AND THE FAILURE IS PROBABLY NOT IN THESE CIRCUITS, IF A FREQUENCY FAILURE OCCURS OUTSIDE THE BASIC BAND.

   DIGITS IN THE FREQUENCY DISPLAY ARE NUMBERED IN THE MANNER SHOWN BELOW. ENTER THE VALUE OF EACH DIGIT INTO THE FORMULAS AND USE THE DECIMAL POINT SHOWN IN THE FORMULA INSTEAD OF THE DISPLAYED DECIMAL POINT.

   FOR EXAMPLE, IF THE DISPLAYED FREQUENCY IS 532.8764019 MHz,

   - THE OUTPUTS OF BLOCK 20 WOULD BE:
     122 + 28 MHz OR 150 MHz.
   - THE OUTPUTS OF BLOCK 23 WOULD BE:
     120 + 28.764019 MHz OR 148.764019 MHz.
   - THE OUTPUTS OF BLOCK 26 WOULD BE:
     10 + 2.8764019 MHz OR 12.87640198 MHz AT A3A8J2, AND
     100 + 28.764019 MHz OR 128.764019 MHz AT A3A8J1 AND J3.

FREQUENCY DISPLAY



BD5

Figure 8-210. Low Frequency Loops Block Diagram

SERVICE SHEET BD6
OUTPUT SECTION BLOCK DIAGRAM

REFERENCE BD1
Simplified Operation (SectionIII)
Operator's Checks (Section III)
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

The Output Section translates the basic frequency band, 320-640 MHz which is generated by the phase lock loops, to the Signal Generator's complete output range, 0.1 - 2560 MHz. Table 8-213 lists the frequency bands. This section controls the amplitude of the RF output signal. Amplitude is controlled with an electromechanical step attenuator which can change in 5 dB steps and electronic leveling which can change the amplitude in 0.1 dB steps. Electronic leveling also keeps the amplitude constant. AM, pulse modulation, and BPSK (when RF output frequency is below 640 MHz) are generated within this section. The modulation signal sources come from other parts of the instrument.

Table 8-213. Output Section Frequency Bands.

BAND	FREQUENCY RANGE (MHz)
Down-Converter	0.1 - 119.9999999
Divide-by 4	120.0 - 159.9999999
Divide-by 2	160.0 - 319.9999999
Basic	320.0 - 639.9999999
Doubler #1	640.0 - 1279.9999998
Doubler #2	1280.0 - 2559.9999996

TROUBLESHOOTING

This procedure covers the following Output Section problems:

1. RF output amplitude not correct (includes front panel STATUS code 76).
2. Harmonics too high.
3. Amplitude modulation (AM) problems.
4. Pulse modulation problems.
5. BPSK problems.

Each of these problems has a separate procedure. Use the procedure that best describes the problem.

RF OUTPUT AMPLITUDE NOT CORRECT (Front Panel STATUS code 76)

1. Check the following input signals to the output section:

Signal	Measure at	Frequency	Level
320 to 640 MHz Fundamental Band Signal	Cable going to A4A3J1	Same as front panel frequency setting between 320.0 and 639.9999999 MHz	+3 to -13 dBm (varies with frequency)
520 MHz Reference	Cable W18(white/ orange/violet) going to A12A5J3	520.0 MHz	0 dBm +/- 1 dB (when front panel setting <120 MHz)

If these signals are normal, then the problem is in the output section. Continue troubleshooting with the steps below.

2. Enable special function 85 (amplitude correction off). Set the front panel AMPLITUDE setting to the values in the first column of Table 2-214, below. Measure the output level at A12A1J1 and compare measured values to the values in the table.

Table 8-214. Output Section Pre-Attenuated Levels

AMPLITUDE setting (dBm)	A12A1J1 output level (dBm)
+19.9	+19.9
+10.0	+10.0
+5.1	+5.1
+5.0	+10.0
0.0	+10.0
-10.0	+10.0
-30.0	+10.0
-70.0	+10.0

If the measured values are correct (± 2 dB), then the problem is with the mechanical step attenuator. Continue troubleshooting with service sheet 34. If the measured values are not correct, there is a problem somewhere else in the output section. Continue troubleshooting with step 3.

3. Check the operation of the A4A3 Distributor assembly by setting the front panel frequency to the values in the first column of Table 8-215, below, and measuring at the output connector listed in the second column of the table. The signal should be the frequency given in the last column of the table and the level should be greater than 0 dBm.

Table 8-215. A4A3 Distributor Output Levels

FREQUENCY Setting (MHz)	Measure at A4A3	Frequency (MHz)
80.0	J3	600.0
150.0	J4	150.0
200.0	J4	200.0
300.0	J4	300.0
400.0	J4	400.0
600.0	J4	600.0
800.0	J2	400.0
1000.0	J2	500.0
2000.0	J2	500.0

If all the signals are normal, the problem is not on the A4A3 assembly. Continue troubleshooting with step 4, below. If any of the signals are not normal, troubleshoot the A4A3 assembly using Service Sheets 27 and 28.

4. Check to see if the problem occurs in all bands by setting the frequency to each band and checking the front panel RF output. Table 8-216, below, gives the frequency range of each band.

Table 8-216. Frequency Bands/Assemblies

FREQUENCY RANGE (MHz)	BAND	A12A1 INPUT
0.1 - 119.9999999	Down Converter	J2
120.0 - 639.9999999	Mid (UHF)	J3
640.0 - 1279.9999998	Doubler #1	J4
1280.0 - 2559.9999996	Doubler #2	J4

If the problem occurs in only one band, continue troubleshooting with step 5. Otherwise, substitute a signal from another signal generator into the A12A1 assembly. Table 8-216, above, shows which connector to use to check the different bands. Set the level of the signal which is substituted to 0 dBm. Set the 8663A being tested to a frequency in the band to be checked and set Amplitude to +10.0 dBm which will set the mechanical step attenuator to 0dB attenuation. The output level at the front panel should be +19 dBm or greater. If

this level is not obtained, there is a problem on the A12A1 assembly. Continue troubleshooting with service sheet 34 and 35. If the output level is normal, vary the amplitude of the substituted signal to produce the output levels in the first column of Table 8-217, below. Measure the detector voltage on the A12A6 motherboard at TP1 (remove the bottom cover of the instrument to reach this test point).

Table 8-217. A12A1 RF Detector Output Levels

OUTPUT LEVEL (dBm)	DETECTOR OUTPUT (A12A6TP1) (Vdc)
+ 5.0	0.920
+10.0	1.637
+15.0	2.912
+19.0	4.610

If these voltage readings are not normal, there is a problem with the A12A1 assembly. Continue troubleshooting with service sheets 34 and 35. If the voltage readings are normal, the A12A1 assembly is good. Continue troubleshooting with step 5, below.

5. Remove the A4A1 ALC assembly from the instrument. Each of the bands has a modulator which controls the level. With the ALC assembly out of the instrument there is no drive signal to the modulators. Each modulator has two test points which can be shorted together to turn the modulator fully on. These test points are given in Table 8-218, below. To check the modulator for each band mount the assembly which contains the modulator on an extender board and short the test points listed in the table. Set the 8663A frequency to a setting in the band being checked. Use extender cables to connect all the normal cable connections to the assembly on the extender board.

Table 8-218. Output Modulator Test Points

BAND	FREQUENCY RANGE (MHz)	EXTEND ASSEMBLY	SHORT TEST POINTS
Down Converter	0.1 - 119.9999999	A12A5	TP9 and TP10
Mid (UHF)	120.0 - 639.9999999	A12A2	TP3 and TP4
Doubler #1	640.0 - 1279.9999998	A12A4	TP6 and TP9
Doubler #2	1280.0 - 2559.9999996	A4A2	TP5 and TP13

The amplitude of the signal at the front panel RF output connector should be +19 dBm or greater. If the signal level is normal, then the problem is in the ALC assembly. Remove the short on the test points, reinstall the A4A1 ALC assembly in the instrument, and continue troubleshooting with Service Sheets 36 and 37. If the output level is too low, trace back from the A12A1 Output Amplifier assembly to find where the signal level is lost and continue troubleshooting on the schematic diagram for that assembly.

HARMONICS TOO HIGH.

1. Check for excessive harmonic levels in all bands. If the harmonics are too high in the Down Converter and/or all other bands, the problem is most likely in the A12A1 Multiplexer and Power Amp Assembly. To test this, drive the A12A1 with an external signal source known to be low in harmonics. If harmonic levels at the output are still too high, then the A12A1 Assembly is the source of the problem. Continue troubleshooting with Service Sheet 34. The bias adjustment of the amplifiers should be checked first, as this is a primary cause of high harmonics.

2. If harmonics are too high in only one band, then the problem is most likely on one of the other assemblies in the output section. Look at the outputs of the A4A3 Distributor assembly.

   If the outputs of A4A3 are good, then trace the signal through the other assemblies to find where the harmonics become too high. Use a T adapter to look at the outputs of the other assemblies and keep the normal cable connected and the AMPLITUDE setting less than +13 dBm because there will be a 3 dB loss due to using the T adapter. Check the bias settings of amplifiers when the bad assembly is located.

AMPLITUDE MODULATION (AM) PROBLEMS.

1. Check distortion and level of the AM modulating signal from the Modulation Section. Measure the signal at A4A5TP1 which is on the motherboard and is accessable with the instrument bottom cover removed. Level should be as specified on the block diagram (BD7) and distortion should be less than 0.4%.

2. Check that the Amplitude of the instrument will range from +5.1 to +19.0 dBm in .1 dB steps. Use a power meter to check this. Set special function 85 (amplitude correction off). If there are any problems, troubleshoot using the procedure, "RF Amplitude Not Correct", above. If amplitude is correct, then the problem must be on the A4A1 ALC assembly. Continue troubleshooting with Service Sheets 36 and 37.

PULSE MODULATION PROBLEMS.

1. Check the pulse drive signal at A12A6TP2 (motherboard test point is accessed by removing the bottom cover of the instrument). This should be a TTL digital signal at the internal modulation rate or the external rate depending on which source is being used. If this signal is not normal, then the problem is on the A4A1 ALC assembly. Continue troubleshooting with Service Sheets 36 and 37.

2. Check the signal out of the A4A3 Distributor assembly. The signal should be pulse modulated. If it is not, then the problem is on the A4A3 assembly. In the Mid Band (120.0 - 639.9999999 MHz) the A12A2 UHF Modulator also pulse modulates the signal so check the signal out of the A12A2 assembly in that band.

3. The A12A1 Multiplexer and Power Amp assembly has circuitry to sample the level of the signal when the pulse is on to generate the detector signal. Thus, if the pulse level is not correct, troubleshoot the A12A1 assembly using Service Sheets 34 and 35.

Fig 8-21
Sht 1 of 5

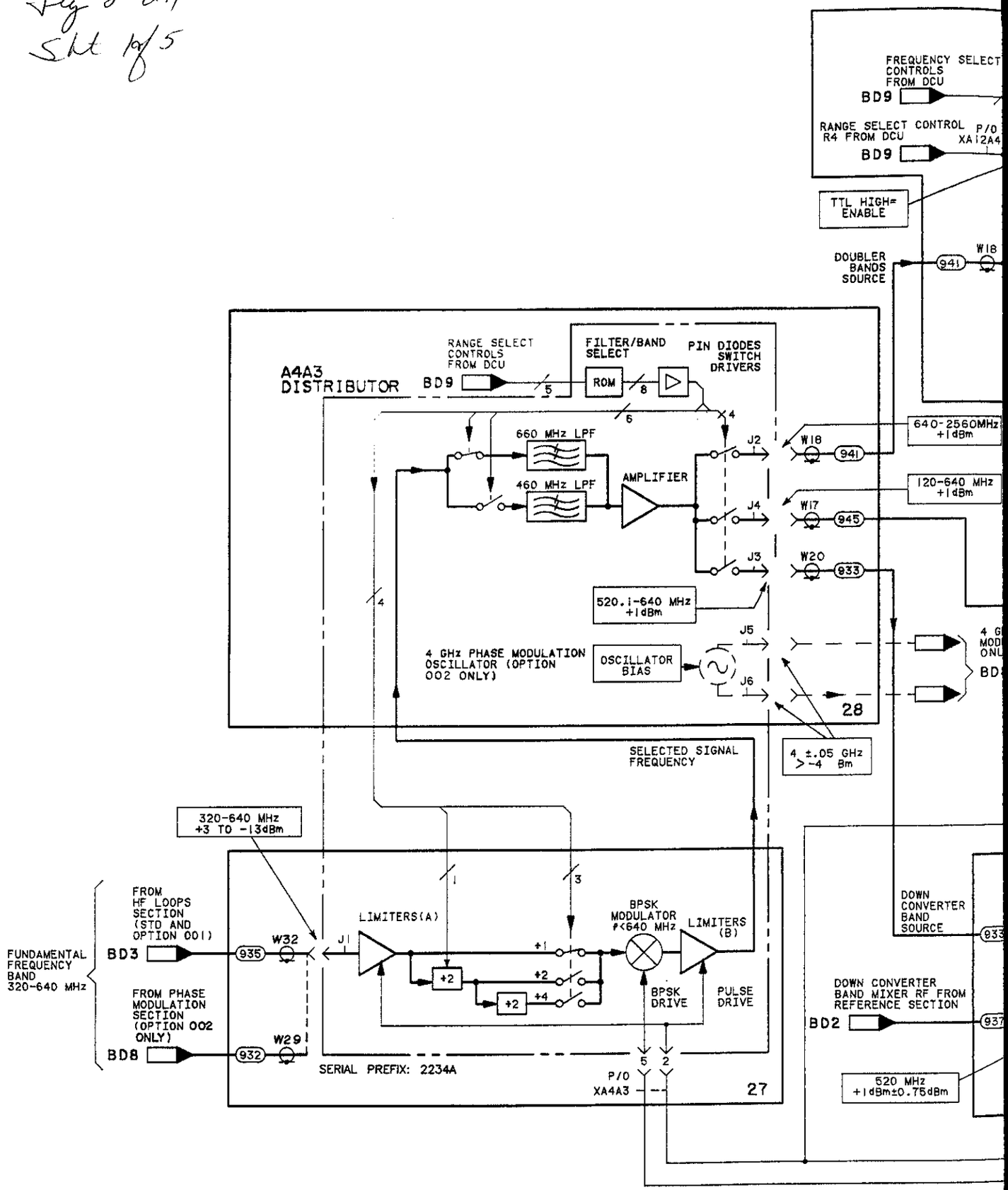


Fig 8-211
Sht 2 of 5

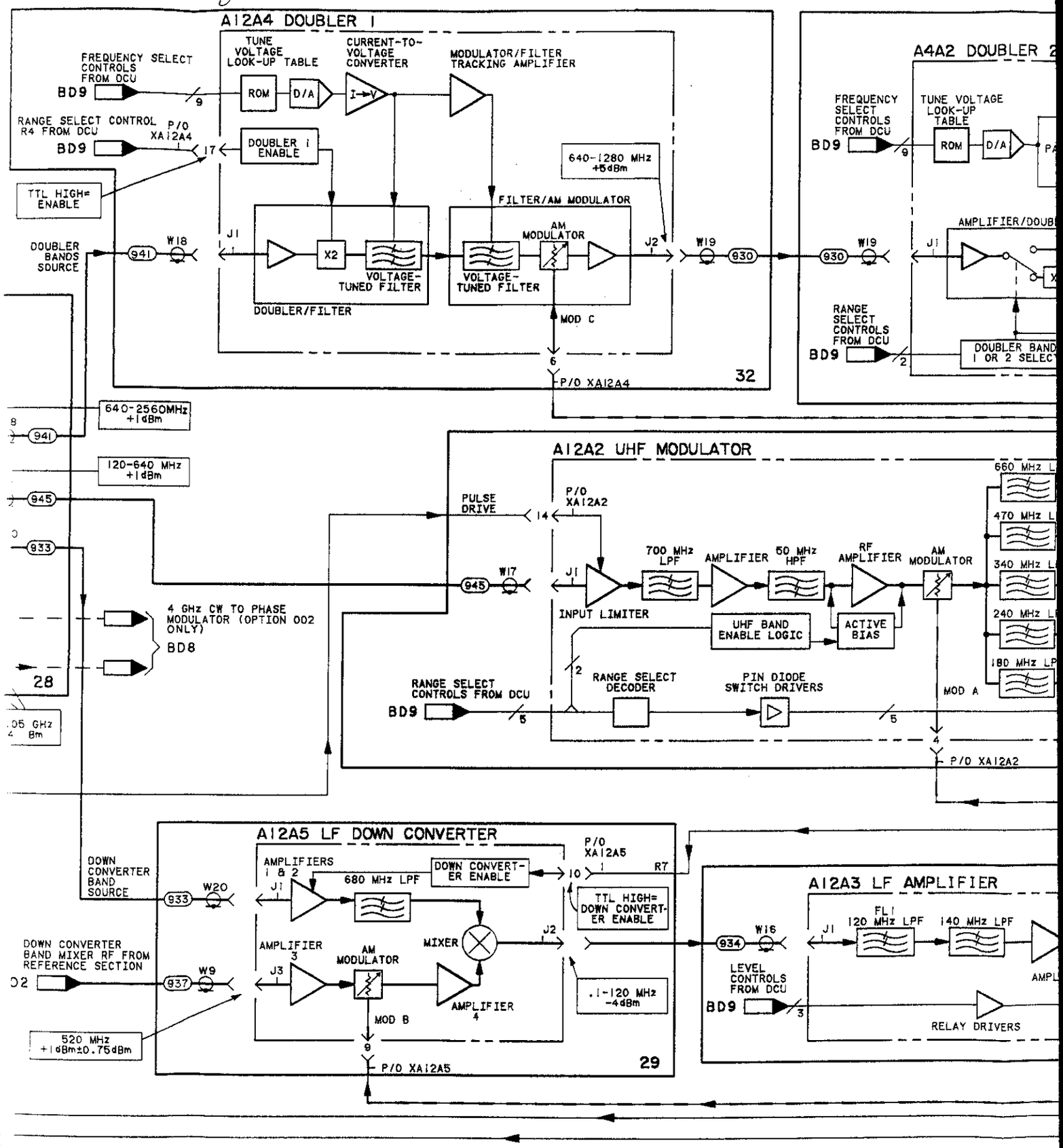


Fig 8-211 Sht 3 of 5

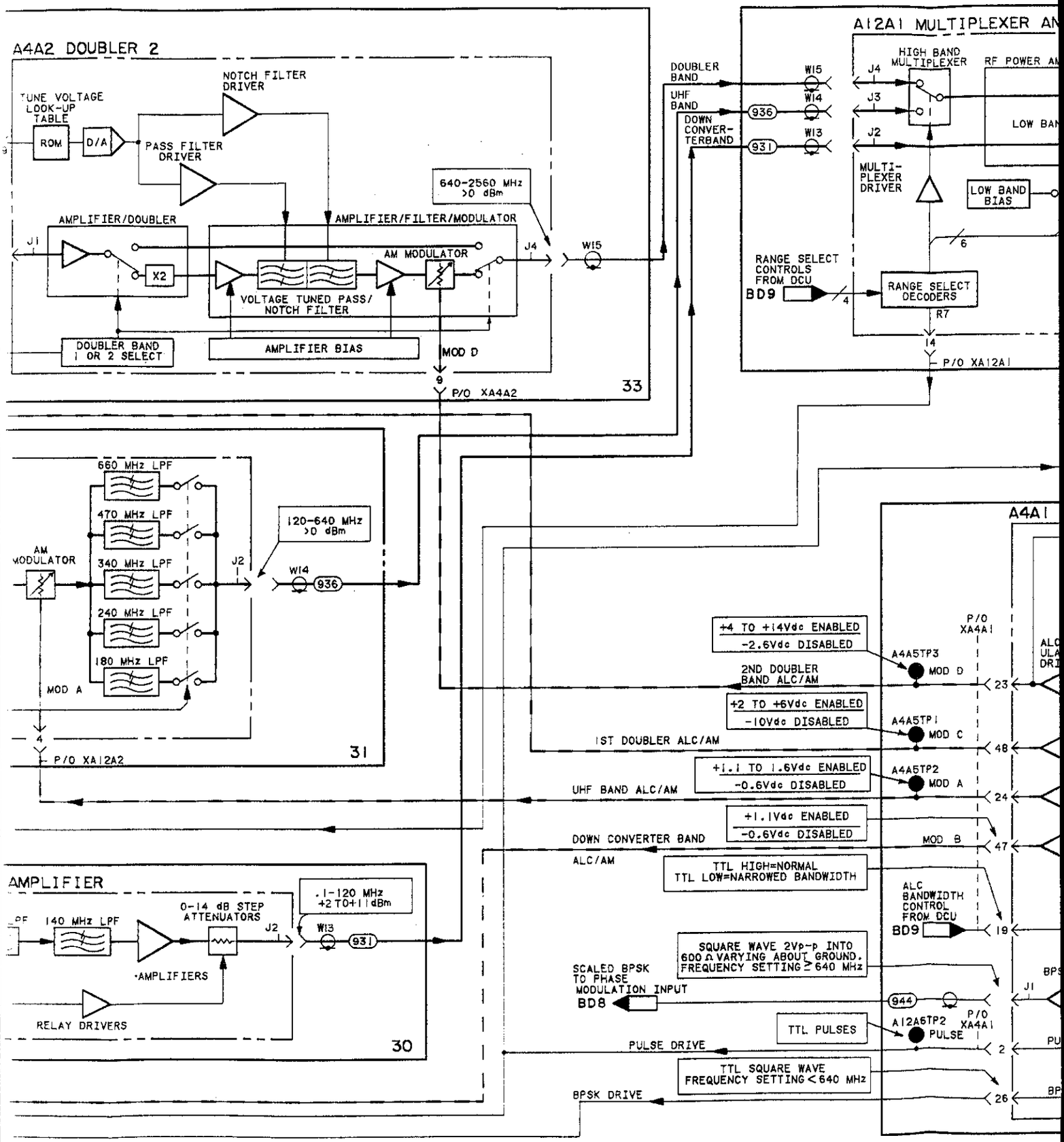
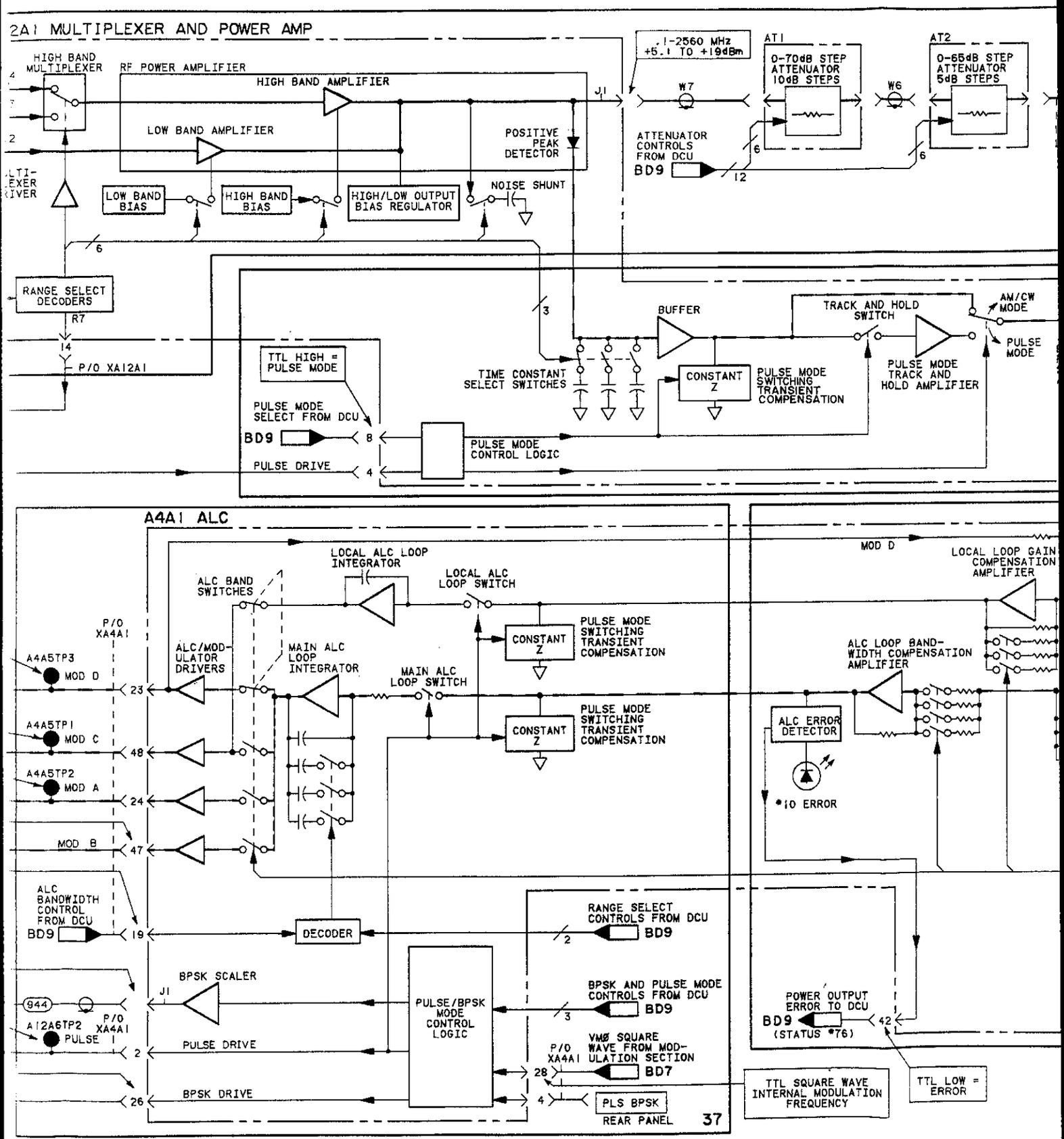


Fig 8-211 Sht 4 of 5



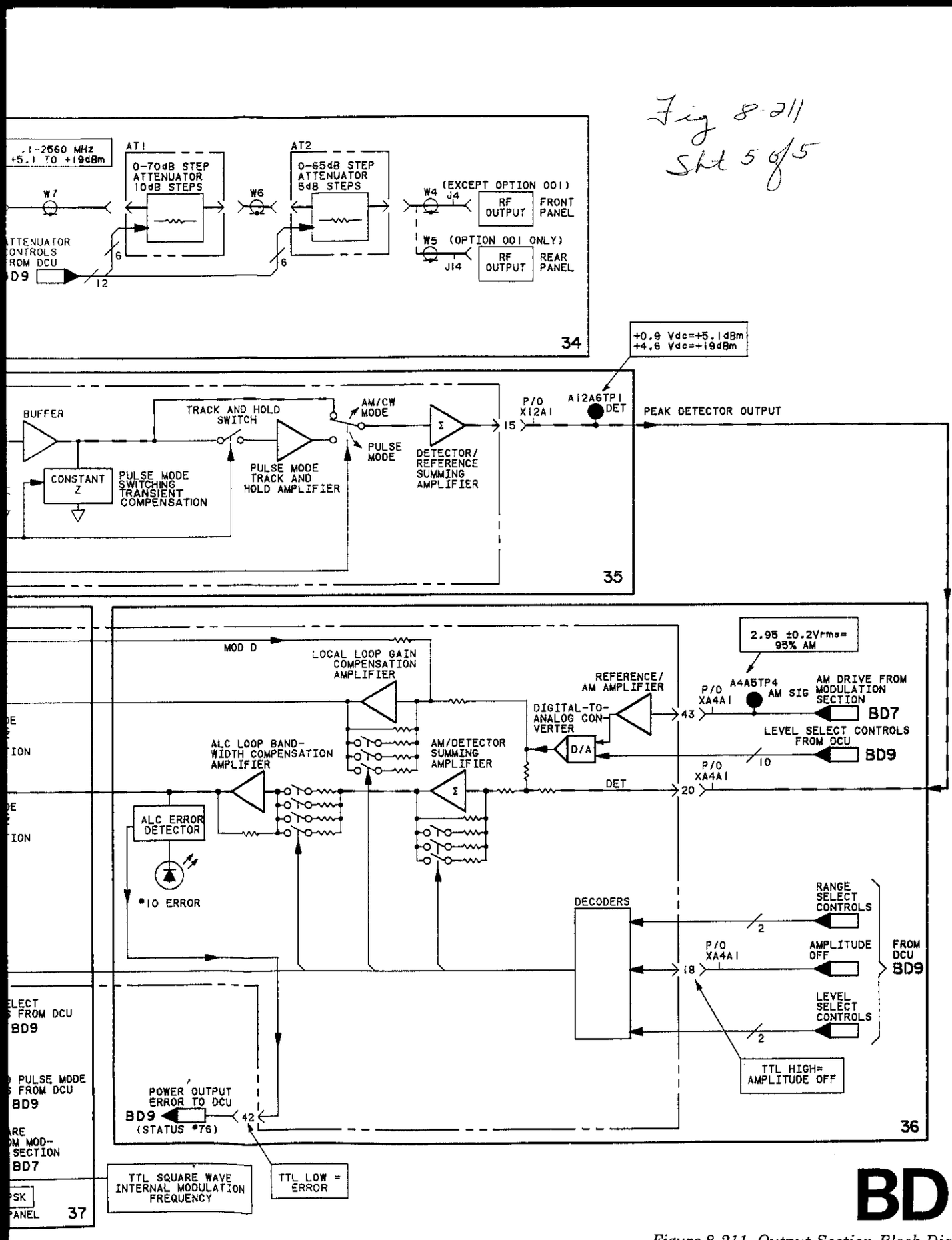


Figure 8-211. Output Section Block Diagram

SERVICE SHEET BD7
MODULATION SECTION BLOCK DIAGRAM

REFERENCE BD1
Simplified Operation (Section III)
Operator's Checks (Section III)
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

The Modulation Section controls the amplitude and frequency modulation modes of the Signal Generator. The two primary output signals from this section are the AM modulating signal (AM signal) and the FM modulating signal (FMS LOOP PH DET REFERENCE). In the AM mode, the modulating signal is routed to the Output Section where the actual amplitude modulation of the RF signal takes place. In the FM mode, a 20 MHz modulated signal is routed to the Low Frequency Loops Section where it is combined with other signals.

The Signal Generator can be amplitude and frequency modulated using internal or external modulating signals. The internal modulating signals are generated by a phase lock loop which is part of the A11A1 Variable Modulation Oscillator (VMO) in this section. The VMO produces modulating signals from 10.0 Hz to 99.9 kHz which are phase locked to the reference oscillator. External modulating signals are coupled into the Modulation Section from the front panel AM IN and FM IN connectors and the AUX FM IN connector on the rear panel. Simultaneous AM and FM operation is possible.

The frequency modulated 20 MHz signal is generated by applying the modulating signal to the varactor diode that forms part of the A11A2 FM VCO's tank circuit. The result is that the 140 MHz VCO output is frequency modulated. The 140 MHz FM VCO output is then heterodyned with the stable 120 MHz signal to produce the frequency modulated 20 MHz signal.

Phase-locked FM is possible down to a rate of 20 Hz with some limitations on peak deviation at modulation rates below 200 Hz. In EXTERNAL DC mode, phase-locked FM is not possible because this mode disables the FM Loop.

TROUBLESHOOTING

General

There are four types of Modulation Section problems covered by this procedure:

1. FM loop unlocked and/or 20 MHz output (A11A6J5) level wrong.

2. Variable Modulation Oscillator (VMO) unlocked or output level incorrect.

3. Incorrect AM or FM depth, deviation or function.

4. AM or FM distortion too high.

There is a separate troubleshooting procedure for each of these problem types. If the problem symptoms fit more than one type, start troubleshooting with the symptom highest on the list.

FM Loop Unlocked And/Or 20 MHz Output (A11A6J5) Level Wrong

When the front panel STATUS light flashes and the error code is 08, it indicates the FM loop is unlocked. The LED on top of the A11A2 assembly should light when this occurs.

1. Remove the A11A4 Phase Detector and A11A5 Modulation Drive Assemblies from the instrument. This leaves the FM VCO (A11A2) free-running. Check for the following:

   a) Signal at A11A2J1 (top of A11A2 assembly) is 140.0 ± 0.1 MHz at greater than -5 dBm.

   b) Signal at A11A6J5 (20 MHz OUT on motherboard) should be 20.0 ± 0.1 MHz. Level should be greater than -20 dBm when in FM mode and less than -50 dBm when not in FM mode.

   c) The LED on top of A11A2 should not be lit.

   If any of these conditions are not met, there is a problem on the A11A2 assembly. In this case, continue troubleshooting with Service Sheet 43.

2. Plug the Phase Detector Assembly (A11A4) into its connector in the instrument and connect the cable between A11A2 and A11A4. This closes the loop but no modulation is applied because the Modulation Drive (A11A5) is not installed. Check the following:

   a) The LED on top of A11A2 should not be lit.

   b) The signal at A11A4J2 (top of A11A4 assembly) should be 14.0 MHz ± 1 count.

   If these conditions are met, the loop is locked and the A11A2 and A11A4 assemblies are probably good. The problem is most likely caused by the A11A5 assembly.

   If the frequency at A11A4 is wrong, the loop is unlocked so continue troubleshooting with step 3. If the frequency at A11A4 is correct but the LED is lit, the loop is locked but the phase

lock detector on A11A2 is probably malfunctioning. Continue troubleshooting with Service Sheet 43.

3. Disconnect the white/yellow/black cable from A11A4J1. This removes the VCO signal from the phase detector. Check for:

   a) Voltages at A11A4 pin 10 (motherboard TP2) >+7.5 Vdc.

   b) signal at A11A6J5 >20.5 MHz.

   If both conditions are met, continue troubleshooting with step 4. If condition (a) is not met, A11A4 is bad or the 10 MHz reference signal is not reaching A11A4. Continue troubleshooting with Service Sheet 38.

4. Reconnect the cable to A11A4J1. Disconnect the violet cable from A11A6J1 (10 MHz input on motherboard). This removes the 10 MHz reference signal from the phase detector. Check for:

   a) Voltages at A11A4 pin 10 (motherboard TP2) more negative than -6.5 Vdc.

   b) Signal at A11A6J5 <19.5 MHz. Measure with the cable connected using a T adapter. Use the high impedance input of the counter.

   If condition (a) is not met, the A11A4 assembly is bad. If condition (a) is met but condition (b) is not, the A11A2 assembly is bad.

   If both conditions are met, this procedure has failed to isolate the problem. In this case, continue troubleshooting the FM VCO with Service Sheet 43.

Variable Modulation Oscillator (VMO) Unlocked or Output Level Incorrect

When the front panel STATUS light flashes and the error code is 61, it indicates that the VMO is out of lock. When this error occurs, continue troubleshooting with Service Sheet 39.

To verify proper VMO operation, use the following procedure:

1. Connect a cable from the rear panel VMO OUT connector to the high impedance input of a frequency counter and an oscilloscope or DVM capable of measuring AC voltage up to 100 kHz.

2. Set MOD FREQ from the front panel to the following values:

99 Hz
999 Hz
9.9 kHz
31.9 kHz
99.9 kHz

For each setting check that:

* The frequency is the exact value.

* The level is approximately 1.4 Vrms or 2.0 Vp. The exact value depends on the LEVEL adjustment setting on the A11A1 assembly.

3. If any of the readings are not correct, there is a problem on the A11A1 VMO assembly. Continue troubleshooting with Service Sheet 39. If all readings are normal, then the problem is probably not on the A11A1 assembly.

Incorrect AM or FM Depth, Deviation or Function

1. Check the outputs of A11A5 Modulation Drive Assembly:

AM = A11A5 pin 24
FM = A11A5 pin 25

2. These signals should be the levels specified on the block diagram (Service Sheet BD7) and the frequency of the modulation source being used. If either signal is not normal, troubleshoot the A11A5 assembly (Service Sheets 41 and 42). If these signals are normal, the problem must be with the A11A2 FM VCO (FM) or the output section (AM). Continue troubleshooting with Service Sheet 43 (FM) or BD6 (AM).

AM or FM Distortion Too High

1. Check to see if distortion is out of specifications at the output of the A11A5 assembly. Check distortion at:

AM = A11A1 pin 24
FM = A11A1 pin 25

Distortion should be less than 0.4% at these points.

2. If distortion is within specification at these points, the problem must be in the A11A2 FM VCO (FM) or the output

section (AM). Continue troubleshooting with Service Sheet 43 (FM) or BD6 (AM).

If distortion is too high at only one of these points, the problem must be on the A11A5 assembly. Continue troubleshooting with Service Sheets 41 and 42. If distortion is too high at both points the problem could be the A11A5 assembly or the modulation source. Measure the distortion of the internal Variable Modulation Oscillator (VMO) at the rear panel VMO OUT connector. If distortion is above 0.4%, there is a problem with the VMO so continue troubleshooting with Service Sheets 39 and 40. If VMO distortion is normal, the problem must be on the A11A5 so continue troubleshooting with Service Sheets 41 and 42.

Fig 8-212
Sht 1 of 5

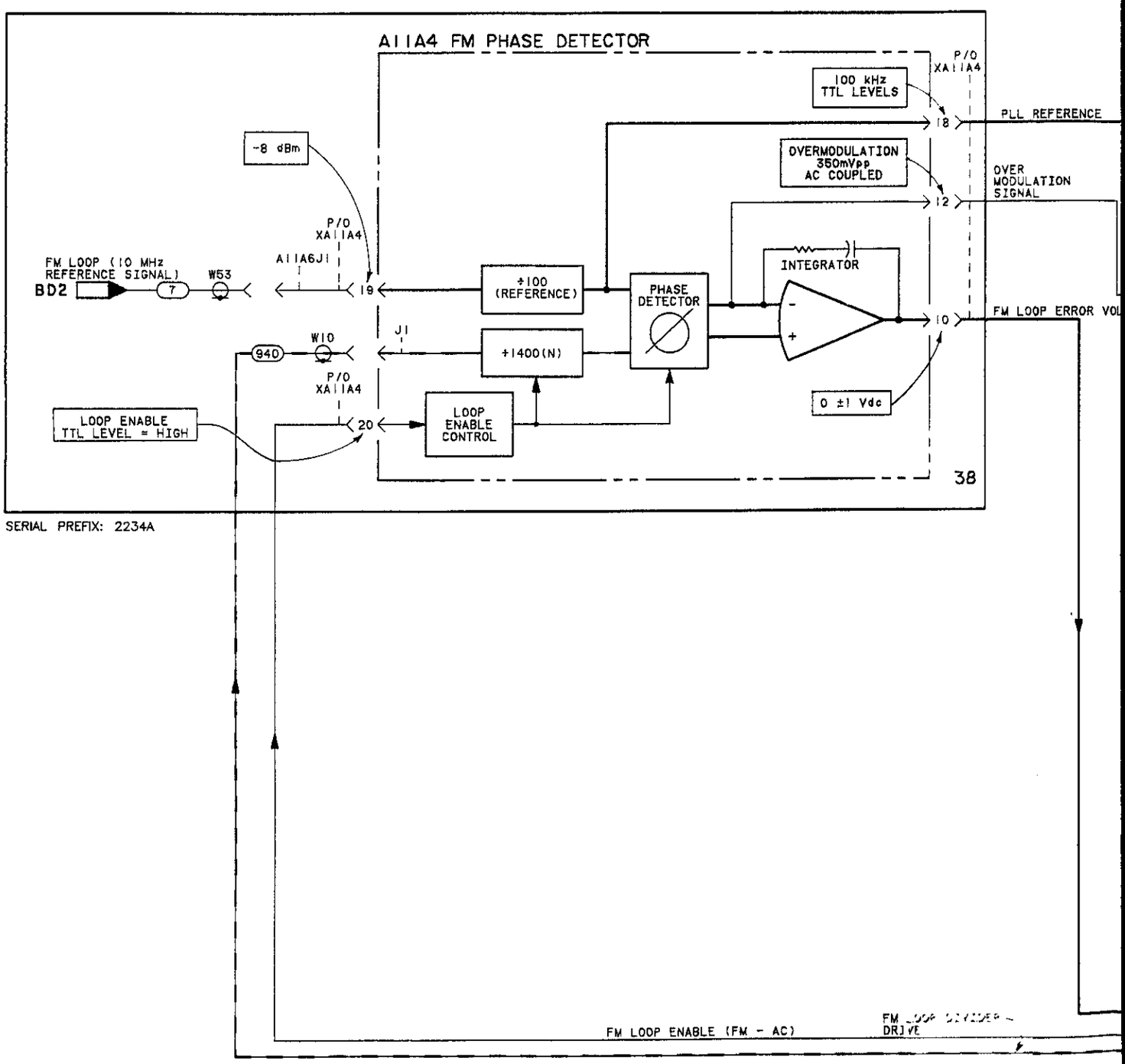


Fig 8-22
Sht 2 of 5

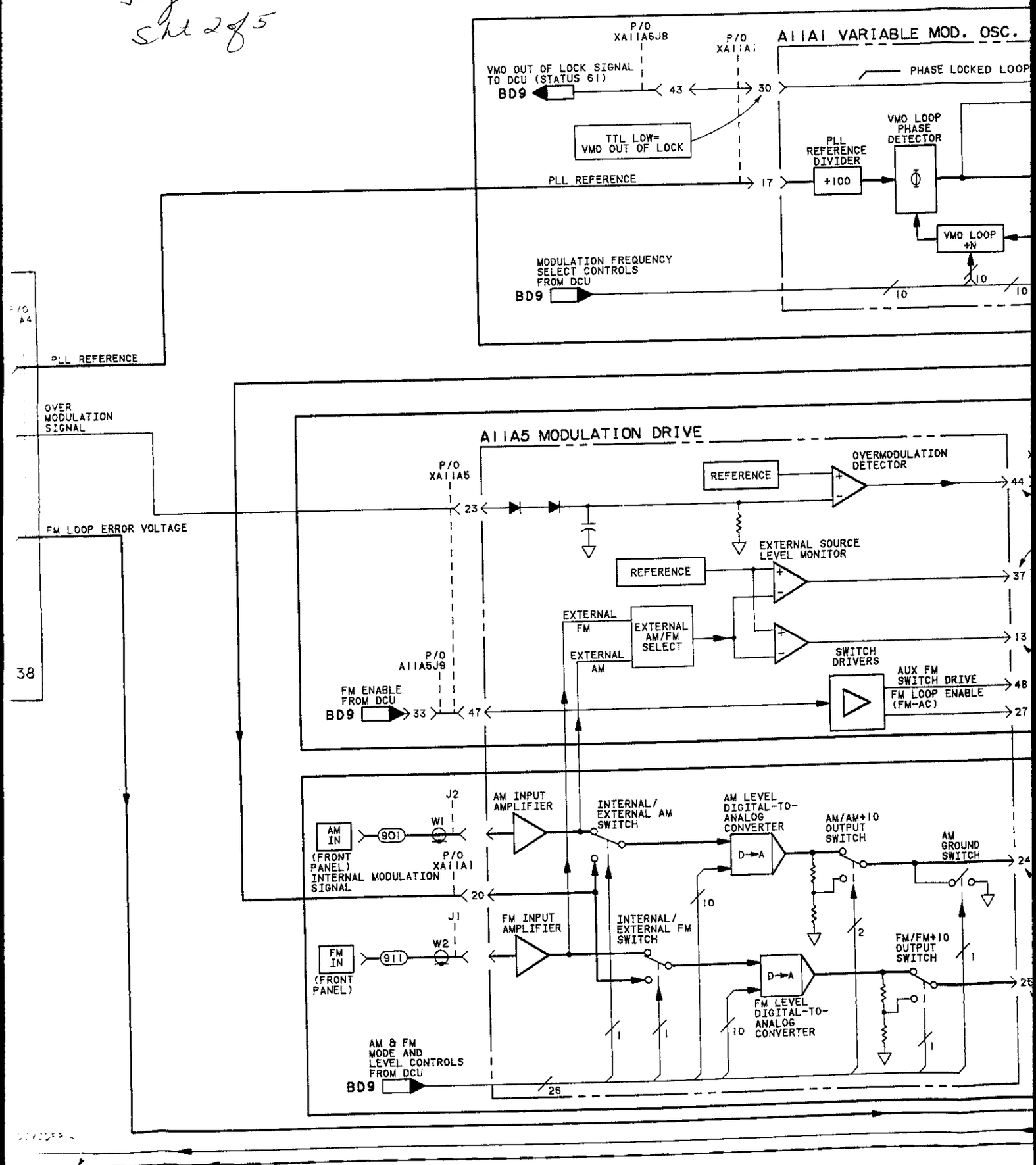


Fig 8-212 Sht 3 of 5

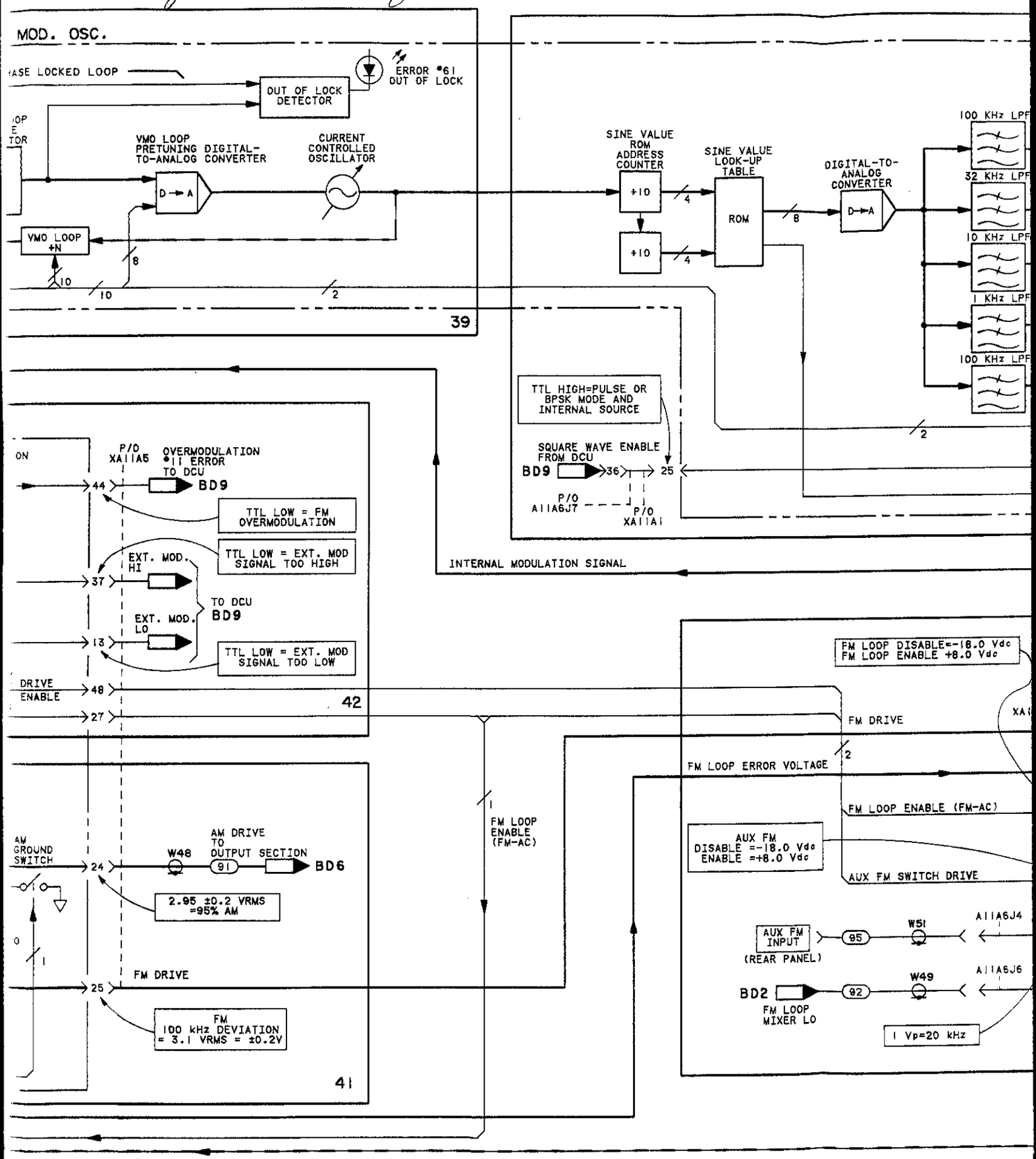
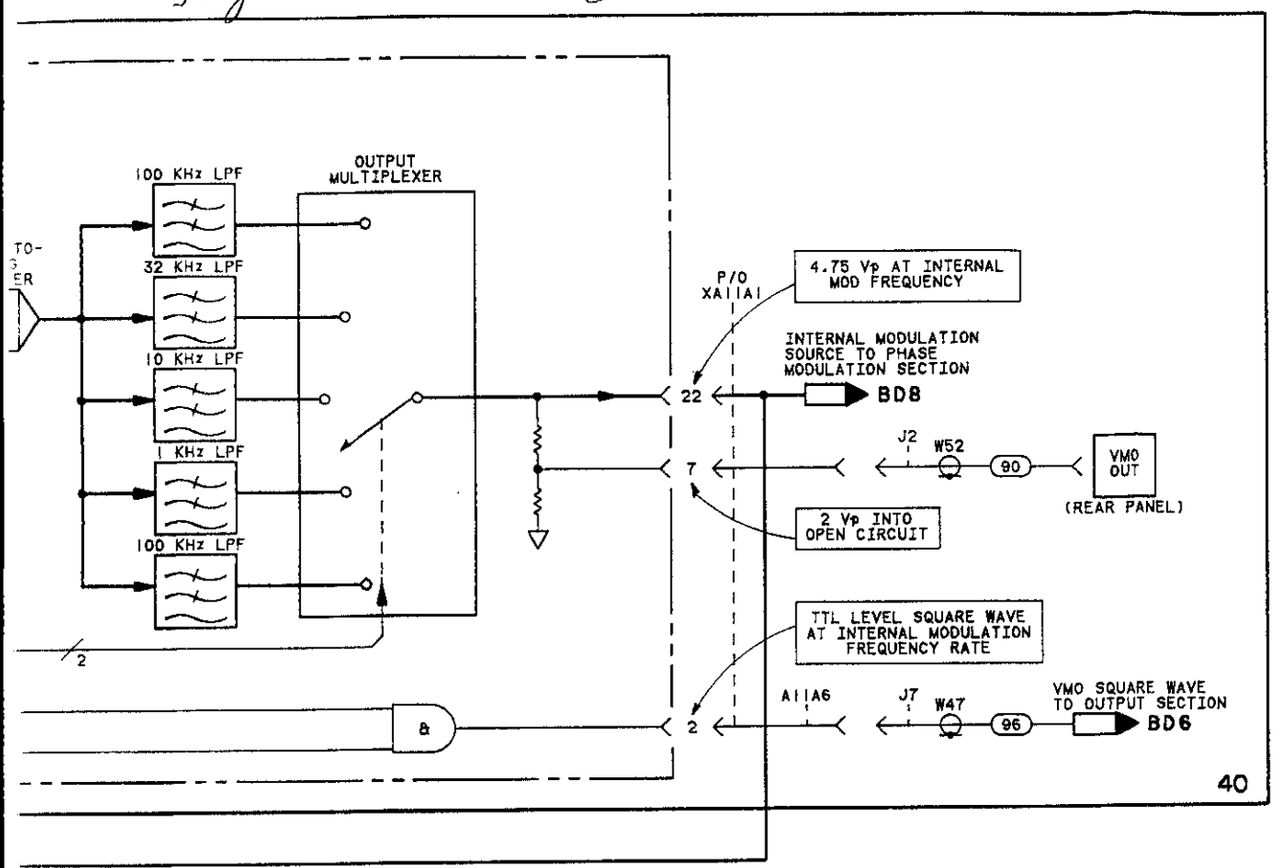


Fig 8-212 Sht 4 of 5



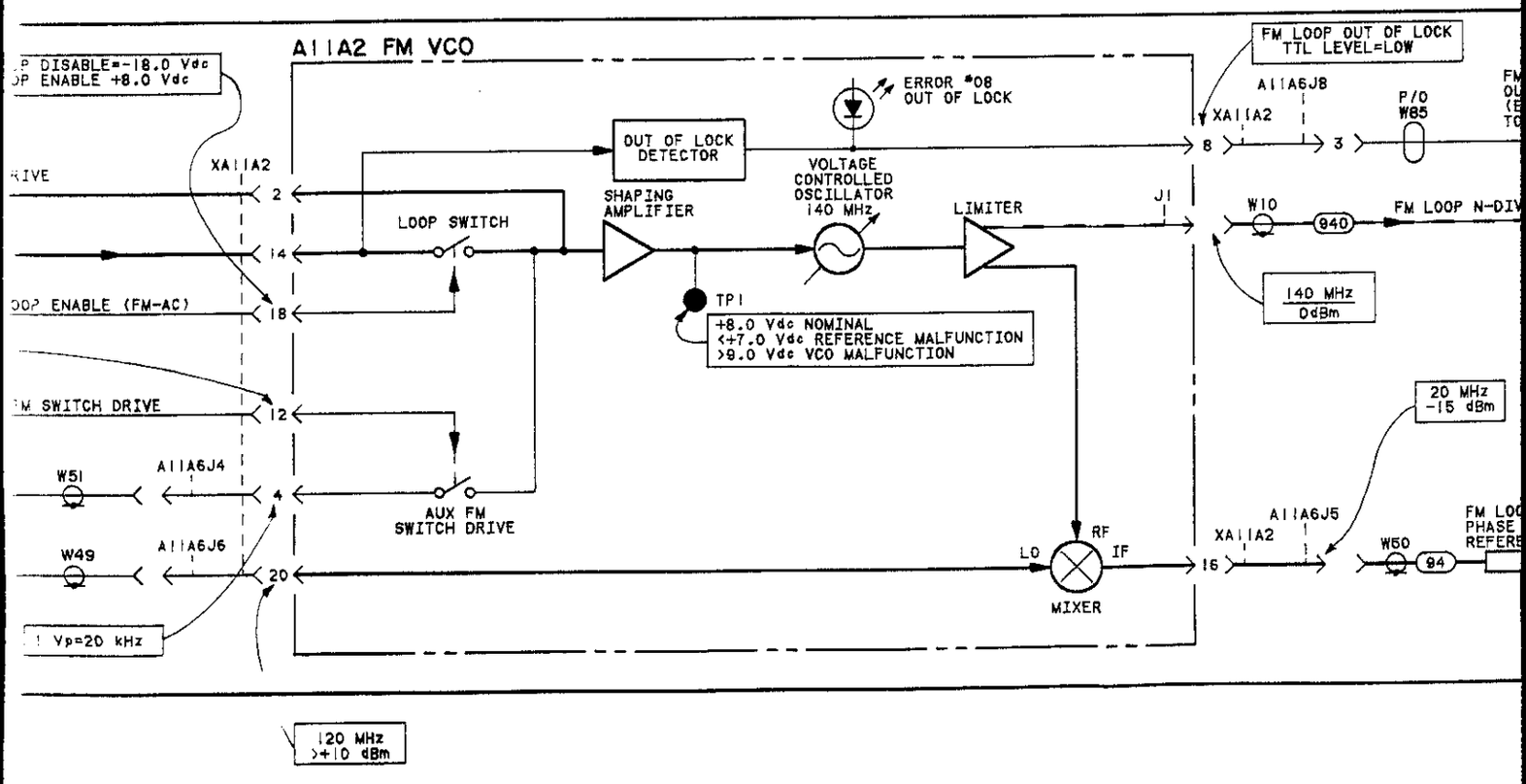
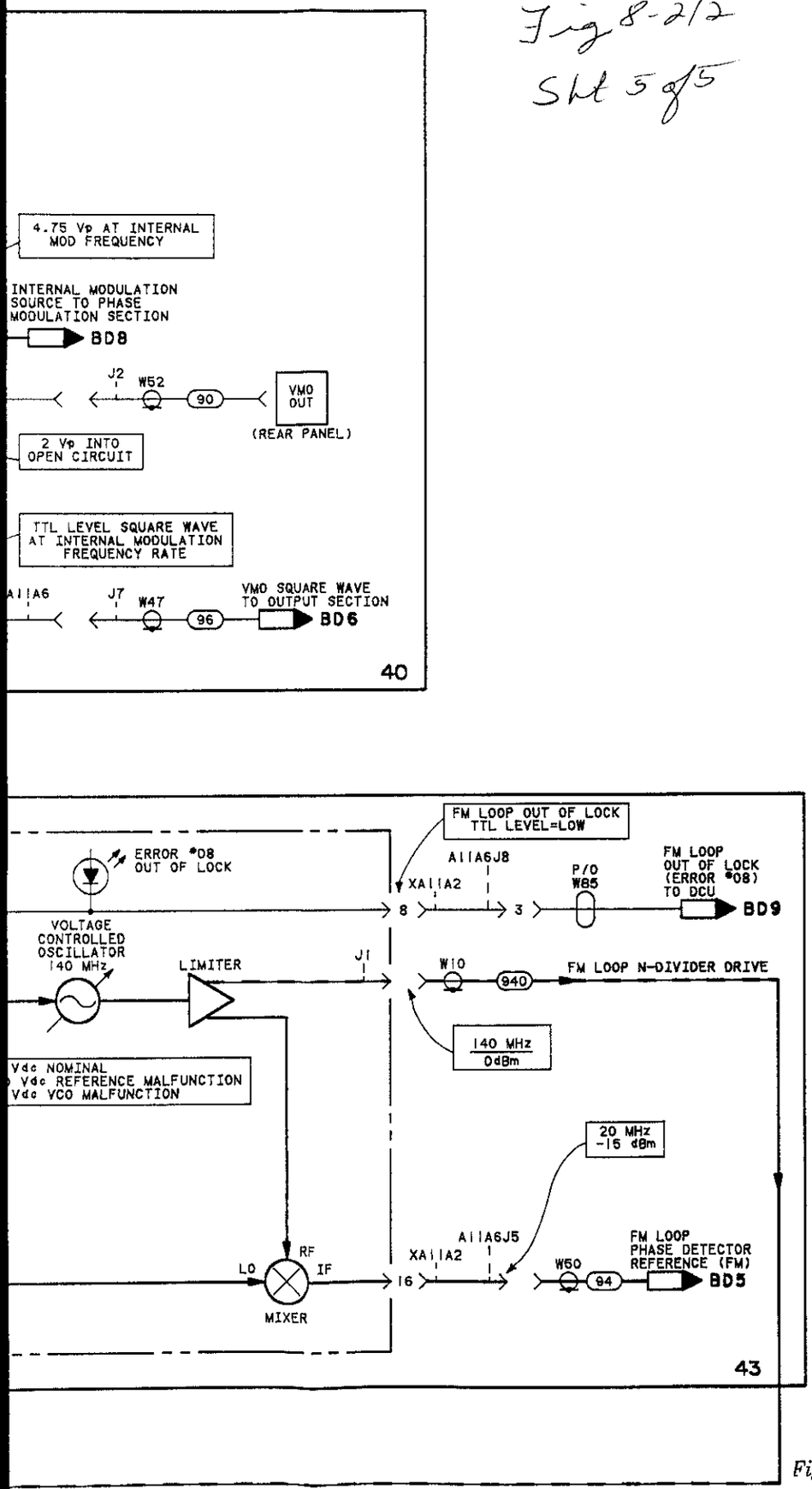


Fig 8-212
Sht 5 of 5



BD7

Figure 8-212. Modulation Section Block Diagram

SERVICE SHEET BD8
PHASE MODULATION SECTION BLOCK DIAGRAM

REFERENCE BD1
Simplified Operation (Section III)
Operator's Checks (Section III)
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

The Phase Modulation Section is only present in the instrument if Option 002 was ordered. The 320-640 MHz signal from the phase lock loops enters the Phase Modulation Section and is mixed with a 4 GHz signal from the A4A3 Assembly. The up-converted signal is then mixed with a phase modulated 4 GHz signal which down-converts the signal back to the original frequency and transfers the phase modulation to the signal. The 4 GHz signal is phase modulated by passing it through a circulator that has a phase modulator attached to its intermediate ports. The phase modulator consists of varactor diodes which terminate the coax lines from the circulator. This causes the signal to be reflected back to the circulator shifted in phase. The amount of the phase shift depends on the capacitance of the varactors which is in turn determined by the bias on the diodes. This bias is the modulating signal, so that the amount of phase shift is proportional to the amplitude of the modulating signal. This is phase modulation.

If phase modulation is not enabled,the signal from the phase lock loops bypasses the circuitry described, above, and is passed through a coax cable inside the A4A4 assembly.

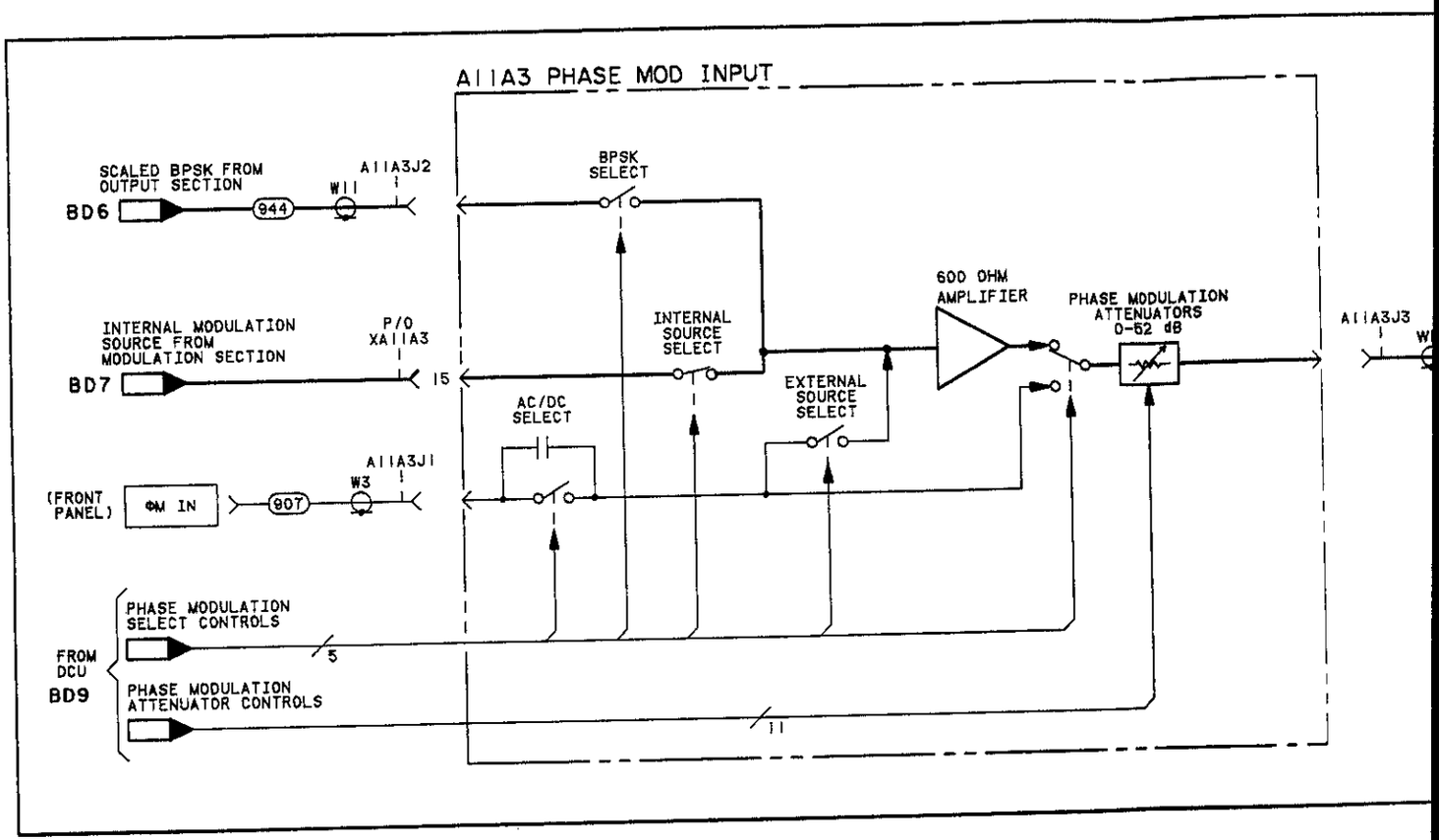
TROUBLESHOOTING

1. Check that the RF output level at A4A4J4 is normal. To do thi set the front panel frequency to any setting in the basic band (320.0 to 639.9999999 MHz). Enable phase modulation with EXT AC source but do not connect a signal to the PM IN connector. Measure the signal level A4A4J4. It should be the value specified on Block Diagram BD8. If the signal level is normal, continue with Step 3, otherwise, continue with Step 2.

2. If the output level is not normal, measure the level of the input signal at the cable which goes to A4A4J1. It should be the value specified on Block Diagram BD8. If this signal level is not normal, then there is a problem in some other section. If the input is normal, measure the 4 GHz signal levels from the A4A3 Assembly. If these signal levels are not the values specified on the block diagram, then there is a problem on the A4A3 Assembly. If the 4 GHz signals and the input signal are normal and the output signal level is not normal, then there is a problem in the Phase Modulation Section. Continue troubleshooting with Service Sheet 45.

3. If the output signal level is normal and phase modulation is not correct, then the problem is with the phase modulator. Check the modulating signal at the coax cable that connects to A4A4J6. It should be the frequency of the source being used at the level shown on Block Diagram BD8. If the signal is not correct, then there is a problem with the A11A3 Phase Mod Input Assembly. Continue troubleshooting with Service Sheet 44. Otherwise, the problem is in the A4A4 Phase Modulation Assembly and troubleshooting should continue with Service Sheet 45.

Fig 8-213
Sht 1 of 4



SERIAL PREFIX: 2234A

Fig 8-213
Sht 2 of 4

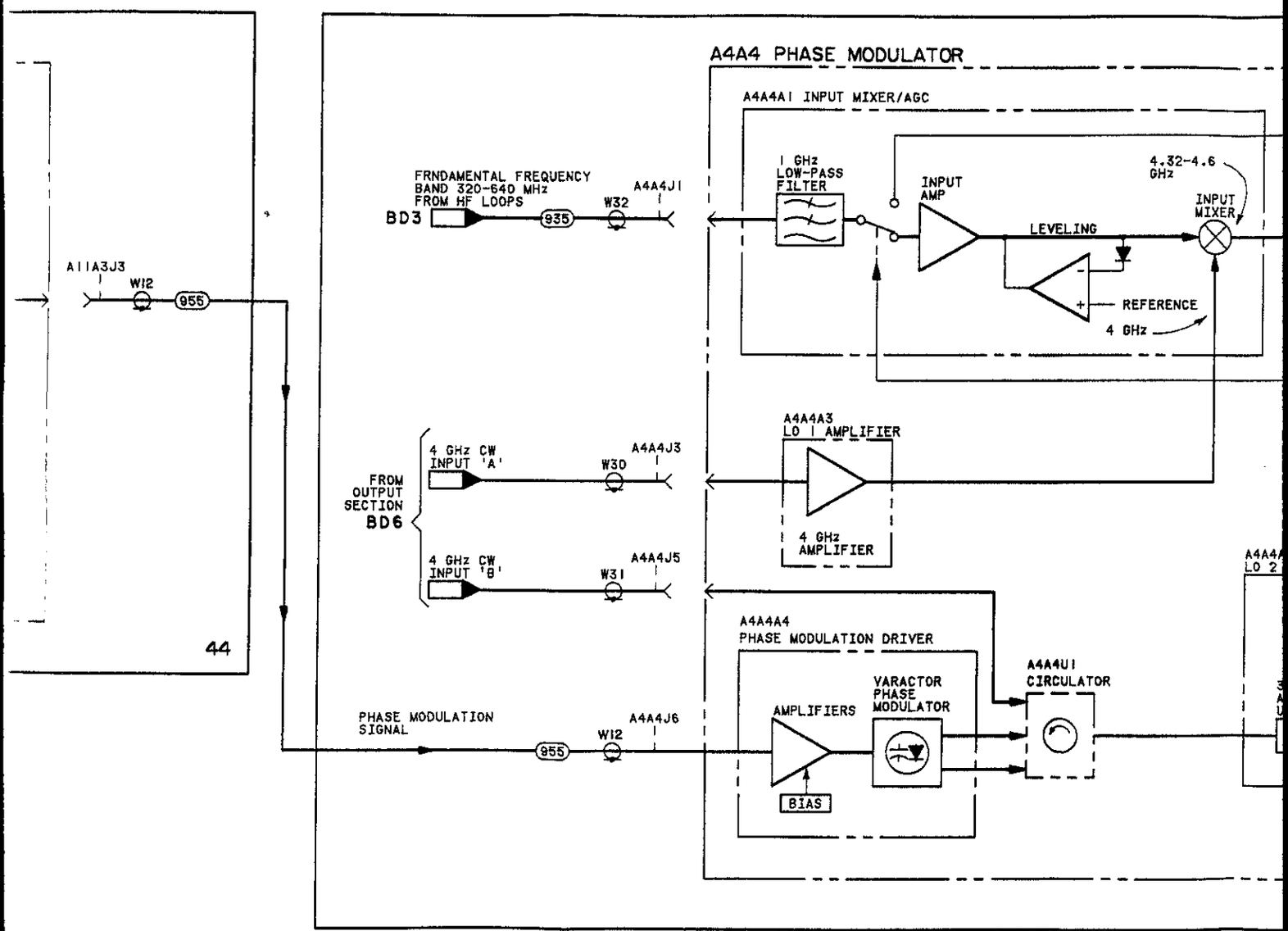


Fig 8-213
Sh 3 of 4

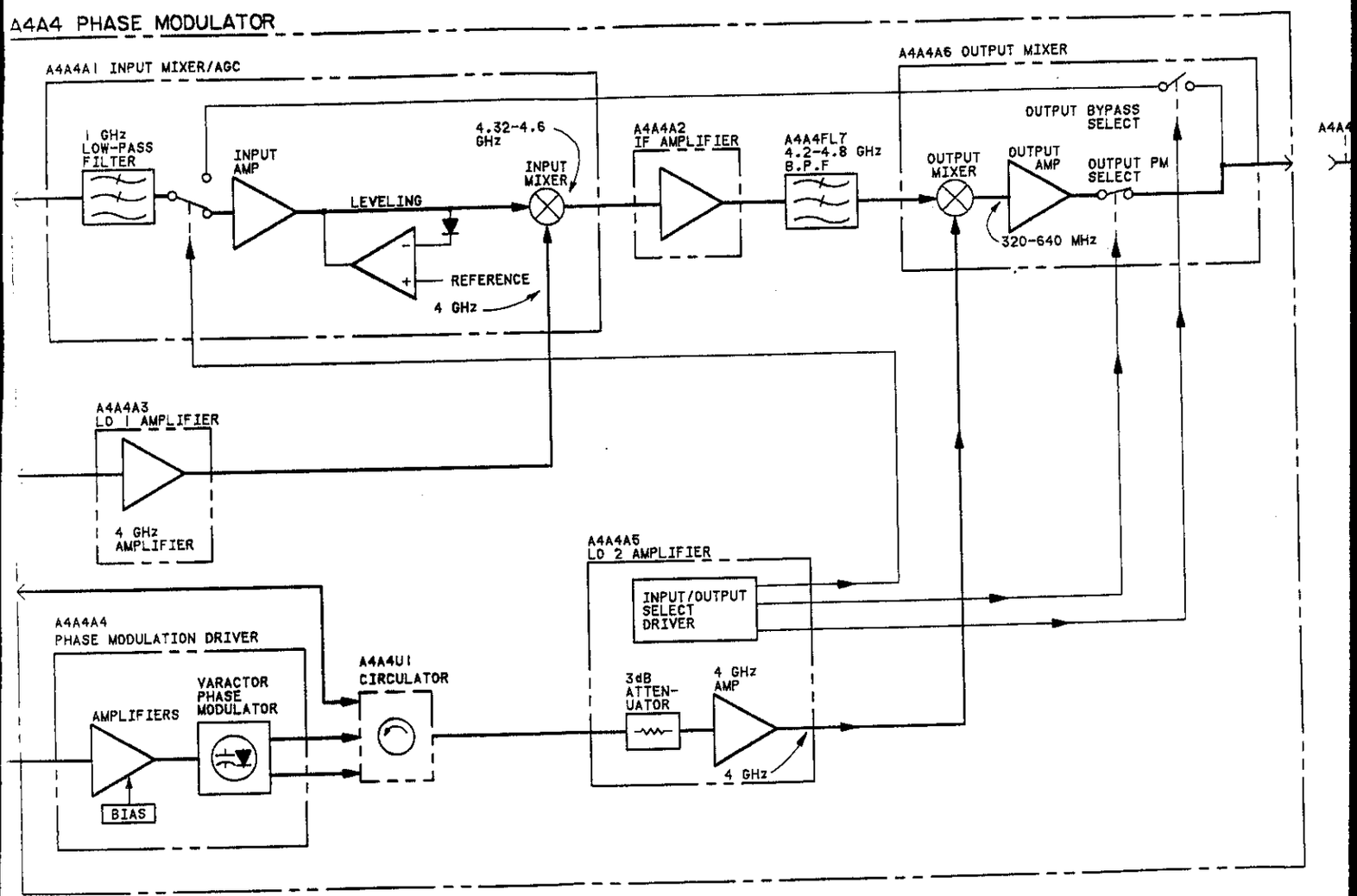
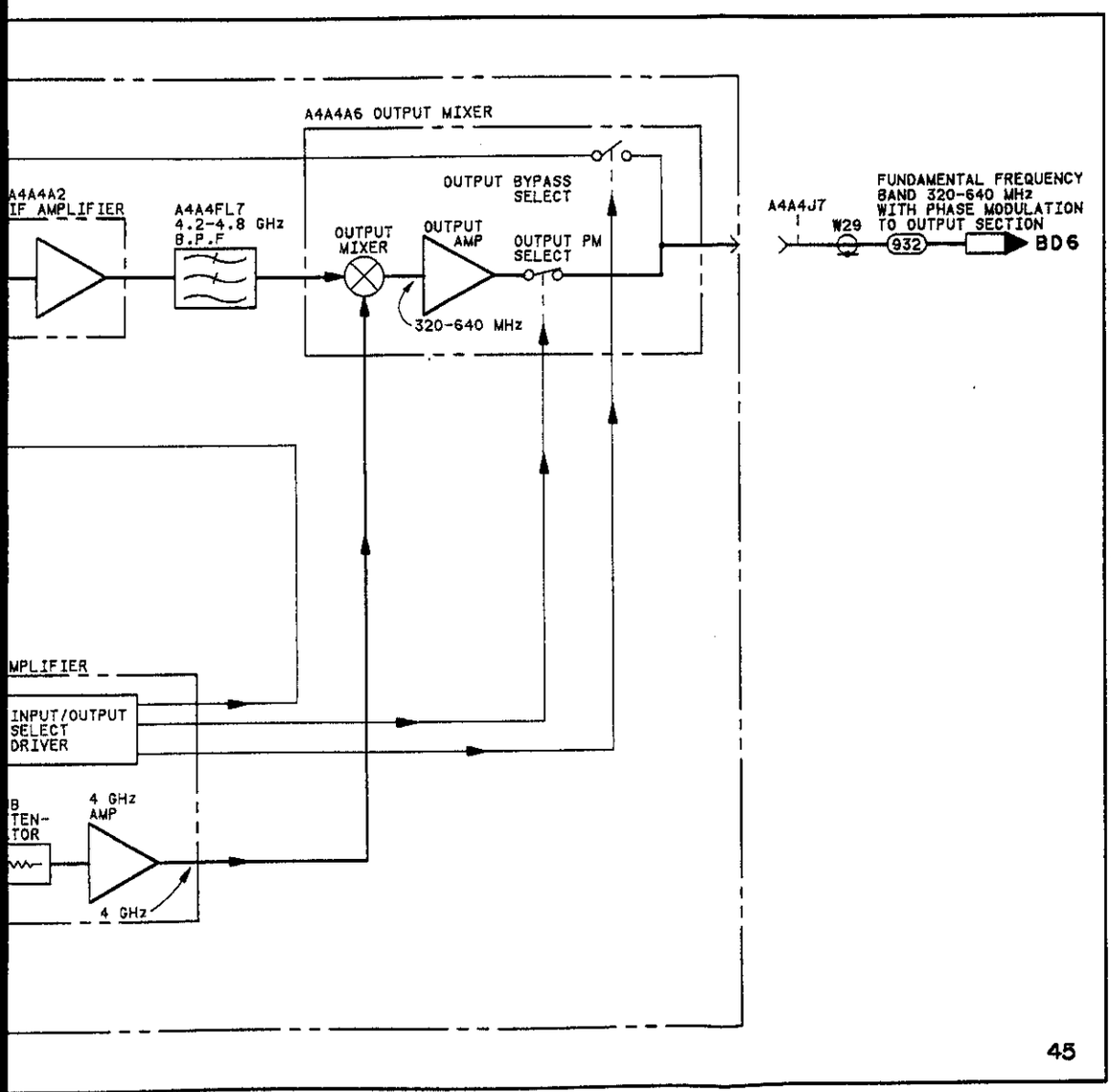


Fig 8-213
Sht 4 of 4



BD8

Figure 8-213. Phase Modulation Section Block Diagram

SERVICE SHEET BD9
DIGITAL CONTROL UNIT (DCU) BLOCK DIAGRAM

REFERENCE BD1
HP-IB Address Selection (Section II)
HP-IB Connector (Section II)
Memory Check (Section III)
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The function of the DCU is to control the operation of the Signal Generator in response to data and instructions received from the front panel keyboard, rear panel AUX connector, and the Hewlett-Packard Interface Bus (HP-IB).

The Microprocessor assembly maintains control of the system by implementing a master program stored permanently in read only memory (ROM). Temporary storage of data is located in random access memory (RAM) on the RAM/ROM assembly. Storage of front panel data is located on the Peripheral RAM assembly which has battery backup to keep stored data intact during power-down conditions.

The HP-IB assembly functions as the instrument interface to the IEEE488 interface bus which enables the instrument to be remotely controlled by an automated controller.

The DCU employs an eight-bit bi-directional data bus for the transfer of data between the Microprocessor assembly and the peripheral assemblies. The Frequency Control, Level Control, Modulation Control, Sweep Control, and Display assemblies receive and latch the data on the data bus from the Microprocessor. The outputs of the latches drive the analog portions of the Signal Generator. The Frequency Control, Level Control, and Modulation Control assemblies have read-back circuitry which can, under Microprocessor control, send the latched data back to the Microprocessor via the data bus. This read-back of data is a diagnostic feature which is used to verify normal operation.

The Keyboards are of the matrix type where pushing a key grounds one row and one column in the matrix. The Keycode asembly receives row and column information from the keyboards and encodes it to form a unique code for each key pressed. The Keycode assembly interrupts the Microprocessor which reads the code via the data bus and takes whatever action is required. Likewise, when a character is sent to the Signal Generator on the HP-IB, the HP-IB assembly interrupts the Microprocessor, which reads the character via the data bus. The Microprocessor then interprets the character and determines what action is required.

TROUBLESHOOTING

There are two methods of troubleshooting the DCU:

1. Use internal diagnostic programs.

2. Use signature analysis which also requires use of the internal diagnostic programs to exercise the appropriate portions of the hardware.

Table 8-220, below, contains a list of all the diagnostic programs available in the 8663A.

Table 8-219. DCU Diagnostic Programs

TEST NUMBER	TITLE
0	System self check. Performs tests 1,3,5 and 8.
1	Single pass RAM test.
2	Continuous run RAM test.
3	Single pass ROM test.
4	Continuous run ROM test.
5	Peripheral RAM test.
6	Signature analysis stimulus of I/O circuitry.
7	Same as test #6 with delayed signature analysis clock.
8	Test of internal I/O circuitry.
9	Not used.
10	Allows direct control of RF output step attenuator from keyboard.
11	HP-IB signature analysis stimulus and output test.
12	Keyboard LED visual stimulus and signature analysis stimulus of Sweep assembly.
13	Readout visual stimulus and signature analysis stimulus.
14	Keycode assembly signature analysis stimulus.
15	Manual keyboard test.

General DCU Troubleshooting Information

A complete description of each test is provided in the following pages. Since these tests are the tools that are available to troubleshoot the DCU, it is important to read this material carefully in order to gain an understanding of of what each test actually does. Then, based on the problem symptoms observed, one or more of the tests can be run to determine the source of the problem.

Test 0 should normally be run first if there is any type of DCU problem. Then, if no failures are found, other tests can be run based on the problem symptoms.

DCU Test Configurations

There are a minimum number of assemblies required in the DCU for each test. These assemblies are listed under REQUIRED ASSEMBLIES in each test description. The tests will run with all assemblies in the DCU. It is possible, however, for one of the assemblies not used in the test to affect a backplane line and cause a test to fail. Therefore, if a test fails, it is good practice to remove all the unused assemblies and run the test again. Then, if the test passes, add the other assemblies one at a time to determine which assembly causes the failure.

SYSTEM SELF TEST

Test Number: 0

Required Assemblies: All DCU Assemblies.

Description: This test allows continuous execution of tests numbers 1, 3, 5, and 8. This sequence of tests will run until an error is found in one of the tests. Refer to the descriptions for each individual test for more details.

Procedure:

1. Remove instrument top cover and DCU Covers.
2. Set the test number switch on A2A7 to 0.
3. Install the shorting connector on the top edge connector of A2A7 (at A2A7J1).
4. Connect a jumper between TP4 and TP10 on the A2A7 assembly.
5. Momentarily short TP3 to TP10 on the A2A7 assembly to reset the microprocessor.
6. Remove the jumper between TP4 and TP10.
7. The test will now begin to run. The test number will be displayed in the left side of the FREQUENCY display in the format, " -XX- ". The pass number (the number of times the entire sequence has run) is displayed in the AMPLITUDE display. This is a two digit number which increments with each failure-free test sequence. The count will reset to 00 when incremented from a count of 99. If a failure occurs, the program will stop and display an error code in the right side of the frequency display. Refer to the operating instructions (Section III) for the test number being run and an explanation of the error code.

RAM DIAGNOSTIC

Test Number: 1 (Single pass)
2 (Continuous run)

Required Assemblies: A2A7, A2A8.

Description: This test checks the A2A8 RAM/ROM assembly. Three types of data checks are performed:

1. All possible data patterns are written to all locations except one byte. The one byte that is not written to would cause the attenuator to switch, if exercised.

2. The address of each location is written into that location. Then the data is read back and checked. This checks for overwrite errors.

3. Data is written into all locations and, after a 30 second pause, the data is read back and checked. This checks for fade.

If test number 1 is selected, the test will run once and pause. If test number 2 is selected, the test will continuously repeat until an error is found or the test number is changed.

Procedure:

1. Remove instrument top cover and DCU covers.

2. Set the test number switch on A2A7 to 1 or 2.

3. Install the shorting connector on the top edge connector of A2A7 (at A2A7J1).

4. Connect a jumper between TP4 and TP10 on the A2A7 assembly.

5. Momentarily short TP3 to TP10 on the A2A7 assembly to reset the Microprocessor.

6. Remove the jumper between TP4 and TP10.

7. The test first checks that a small block of RAM is available for use by the test. If an error is detected in this block of RAM, the test halts with " -1 " displayed in the left side of the FREQUENCY display. The test cannot run until the source of the problem is found. Use signature analysis to troubleshoot the A2A8 RAM/ROM assembly if this happens. Use the troubleshooting procedure with the schematic for A2A8.

   If everything is normal, the test will begin to run and " -01- " or " -02- " (the test number) will be displayed on the left side of the FREQUENCY display. During the first part of the test, keyboard LEDs will randomly flash and you will hear relays clicking. Then the relay clicking will stop and the LEDs will remain lit. Finally the LEDs will all be off during

the final portion of the test. If test number 2 was selected, the AMPLITUDE display will contain the number of times that the test has run. This is a two digit number and after 99 the number will reset to 00. If test number 1 is selected, the AMPLITUDE display will be blank.

NOTE

If test number 2 (continuous run) is to be run for a long period of time, the A2A10 assembly should be removed from the DCU. This will prevent the relays from being exercised excessively.

8. The run time for the test is 1 minute, 10 seconds. If no failures are found, " 00 " will be displayed in the right side of the FREQUENCY display. If test number 1 was selected, the program will halt in this condition. If test number 2 was selected, " 00 " will not be displayed. The pass number will be incremented and the test will begin to run again.

9. If a failure is found, the test will halt with a two digit error code in the right side of the FREQUENCY display. Table 8-221, below, specifies which RAM IC is likely bad for each possible error code. The error code is generated when the data read back from a memory location is bad. The RAM IC is not the only possible source of the error. Frequency address decoding circuitry could also cause a failure. Thus, this diagnostic can narrow down the source of a problem, but further troubleshooting may be required to find the faulty component.

When the program halts because of an error, the actual and expected data is placed in the MODULATION display. The expected data is in the MOD FREQ display and the actual data is in the MOD LEVEL display.

Table 8-220. A2A8 RAM/ROM Diagnostic Test Failure Codes

ERROR CODE	LIKELY DEFECTIVE RAM IC
00	No Failure
X0	A2A8 U10
X1	U11
X2	U12
X3	U13
Where: X is 1,2 or 3 which designates the data check during which the error was found. The data checks are defined in DESCRIPTION, above.	

Test Number: 3 (single pass)
4 (continuous run)

Required Assemblies: A2A7, A2A8, A2A9.

Description: This test checks the ROMs on the A2A8 and A2A9 assemblies. Each ROM has a checksum which is a unique number in the range of 1 - 18. The test program reads the data from each ROM and calculates the checksum. If the checksum is not correct, the program stops and indicates an error.

Procedure:

1. Remove the instrument top cover and DCU covers.
2. Set the test number switch on A2A7 to 3 or 4.
3. Install the shorting connector on the top edge connector of A2A7 (at A2A7J1).
4. Connect a jumper between TP4 and TP10 on the A2A7 assembly.
5. Momentarily short TP3 to TP10 on the A2A7 assembly to reset the Microprocessor.
6. Remove the jumper between TP4 and TP10.
7. The test will begin to run. The test number " -03- " or " -04- " will be displayed in the left side of the FREQUENCY display. The test takes approximately one second to run. If no failures are found, test 3 will stop with " 00 " displayed in the right side of the FREQUENCY display. Test 4 displays a two digit pass number in the AMPLITUDE display. Each time the test is run without a failure, the pass number is incremented. When the count reaches 99, the next increment will cause it to reset to 00. If a failure is found, test 4 will stop with an error code displayed in the right side of the FREQUENCY display. Table 8-222, below, shows the ROM from which incorrect data was read for each error code. The actual and expected data is placed in the MODULATION display. The expected data is in the MOD FREQ display and the actual data is in the MOD LEVEL display. Test 3 will display the same information if an error is found, but will not halt. The information will be displayed for approximately 3 seconds and then the test will continue and look for other errors. All errors that are found will be displayed for approximately 3 seconds. When the test is complete, the program will halt with " 99 " displayed in the right side of the FREQUENCY display.

Test 3 should normally be used so that all errors are reported. Test 4 is useful for finding intermittent problems. Test 4 can be left running indefinitely and the test will stop when an error is detected with the error code displayed.

It is important to note that when a failure occurs, it is because the data that was read is not correct. The error code specifies from which ROM data was being read when the error was detected. Any bad component that could alter the data would cause an error code to be generated. So the ROM itself is not necessarily the source of the problem. Address decoding circuitry failures would also cause an error code to be generated. Thus, this diagnostic can narrow down the source of a problem, but additional troubleshooting may be required to find the bad component.

Table 8-221. A2A9 ROM Diagnostic Test Failure Codes

ERROR CODE	LIKELY DEFECTIVE ROM IC
01	A2A8 U1
02	U2
03	U3
04	U4
05	U5
06	U6
07	A2A9 U5
08	U11
09	U6
10	U12
11	U9
12	U3
13	U4
14	U10
15	U8
16	U2
18	U7

PERIPHERAL RAM DIAGNOSTIC

Test Number: 5

Required Assemblies: A2A7, A2A8, A2A3.

Description: This test checks the A2A3 Peripheral RAM Assembly. A data check is performed on the RAM and the entire assembly is stimulated for Signature Analysis (SA) testing. Only the data check is documented here. The SA capability of the test is documented in the troubleshooting procedure for the A2A3 assembly. Refer to Service Sheets 50 and 51.

Procedure:

1. Remove the instrument top cover and DCU covers.

2. Set the test number switch on A2A7 to 5.

3. Install the shorting connector on the top edge connector of A2A7 (at A2A7J1).

4. Connect a jumper between TP4 and TP10 on the A2A7 assembly.

5. Momentarily short TP3 and TP10 on the A2A7 assembly to reset the Microprocessor.

6. Remove the jumper between TP4 and TP10.

7. The test will begin to run. The test number, " -05- ", will be displayed in the left side of the FREQUENCY display. The test takes approximately two seconds to execute and runs continuously until an error is found or the test number switch is changed. The pass number (number of times the test has run) is displayed in the AMPLITUDE display. This is a two digit number that is incremented every time the test is run. When this number reaches 99, the next increment will reset the count to 00.

   The test will stop when an error is detected. An error code will be displayed in the right side of the FREQUENCY display. Table 8-223, below, specifies which RAM is likely bad for each possible error code. The actual and expected data is placed in the MODULATION display. The expected data is in the MOD FREQ display and the actual data is in the MOD LEVEL display. It is important to note that when a failure occurs, it is because the data that was read is not correct. The error code specifies from which RAM data was being read when the error was detected. Any bad component which could alter the data would cause an error code to be generated. The RAM, therefore, is not always the source of the problem. Thus, this diagnostic can narrow down the source of a problem, but additional troubleshooting may be necessary to identify the defective component.

Table 8-222. A2A3 Peripheral RAM Diagnostic Test Failure Codes

ERROR CODE	LIKELY DEFECTIVE RAM IC
X0	A2A3 U6
X1	U8
X2	U7
X3	U9
30	
31	
Where: X is 1 or 2.	

SIGNATURE ANALYSIS I/O DIAGNOSTIC

Test Number: 6 (Normal)
7 (Delayed Clock)

Required Assemblies: A2A7, A2A8, A2A4, A2A5, A2A10.

Required Test Equipment: HP 5005A Signature Analyzer

Description: This test exercises the A2A4, A2A5 and A2A10 assemblies for signature analysis (SA) testing. A signature analyzer is required to use this diagnostic. The two test numbers perform exactly the same test. The SA clock is delayed in test number 7 to allow for the longer settling time when making measurements on the outputs of these assemblies. The longer settling time is caused by cables on the outputs.

This procedure specifies how to make measurements of the outputs of these assemblies to determine if the assembly is operating correctly. To use these diagnostics to troubleshoot an assembly, refer to the troubleshooting procedure included with the schematic diagram for the assembly.

Procedure:

1. Remove instrument top and bottom covers and DCU covers.

2. Set the HP 5005A Signature Analyzer as follows:

   SIGNATURE: NORM
   CLOCK: FALLING
   START: RISING
   STOP: FALLING
   THRESHOLD: TTL DATA

3. Carefully position the 8663A on its side, exposing the A2A11 DCU Motherboard. This facilitates measurement at the underside of the instrument.

4. Connect the signature analyzer to the 8663A as follows:

SIGNATURE ANALYZER	CONNECTION TO A2A7 AT
CLOCK	TP8
START	TP7
STOP	TP7
GND	TP10

5. Set the test number switch on the 8663A A2A7 assembly to 7.

6. Install the shorting connector on the top edge connector of A2A7 (at A2A7J1).

7. Connect a jumper between TP4 and TP10 on the A2A7 assembly.

8. Momentarily short TP3 to TP10 on the A2A7 assembly to reset the Microprocessor.

9. Remove the jumper between TP4 and TP10.

10. The test should begin to run. The test number, " -07· ", should be displayed in the left side of the FREQUENCY display. Table 8-224 gives the output edge connector signatures for the assemblies stimulated by this diagnostic. These signatures are most easily read at the A2A11 DCU Motherboard on the underside of the instrument.

    To confirm that the signature analyzer is connected correctly and that the diagnostic program is running, touch the signature analyzer probe to +5V (available on the DCU motherboard). The signature analyzer should read " 035P ". If this signature is not obtained, check the signature analyzer settings and connections. If no problems are found, use the Free Run Mode Troubleshooting (Section VIII) to check the Microprocessor assembly and the diagnostic ROM.

Table 8-223. Signature Analysis I/O Diagnostic; Signatures.

	SIGNATURES					
Pin No.	XA2A4A	XA2A4B	XA2A5A	XA2A5B	XA2A10A	XA2A10B
1	035P	7838	035P	4U18	035P	37H1
2	9U1P	C437	2CC2	1HHA	035P	4F63
3	U1PH	0000	49H6	035P	035P	0000
4	069U	4378	71C8	0F29	035P	18HU
5	69U1	1HH6	3HCF	121C	035P	H929
6	P12A	HH68	0000	0000	9456	9298
7	12A3	F21H	PH1U	0000	4565	5AH9
8	U6P1	21HH	0000	0000	6H94	AH92
9	6P12	5698	54U1	0000	H945	008C
10	97AF	0000	FP97	0000	C5A8	0000
11	7AF6	0000	5P7H	0000	5A86	0000
12	5197	6984	4591	0208	C2C5	08C5
13	197A	C569	F459	FU13	2C5A	A008
14	1FP5	035P	7UC0	035P	5P65	035P
15	FP56	0000	1164	0000	P654	0000
16	631F	0000	F459	0000	435P	0000
17	31FP	0000	U116	0000	35P6	0000
18	HPOP	0000	0000	0000	8HU4	0000
19	035P	POP2	035P	HCP4	035P	HU44
20	7F7C	H0HP	956F	44HH	----	318H
21	F7C7	0000	5848	0000	----	0000
22	1A7F	0HP0	06C7	2H17	----	F637
23	A7F7	775A	3772	68P6	----	64A6
24	84A8	75A1	H5AC	0000	5159	4A63
25	4A8F	0877	C480	0000	1595	6C64
26	HC84	8775	8813	0000	C651	C64A
27	C84A	5A61	U01A	0000	6515	022H
28	5PC1	0000	91C5	0000	H6A1	0000
29	PC18	035P	9AC8	035P	6A1A	035P
30	465P	A610	1647	4C29	FAH6	22H6
31	65PC	H5A6	1164	7411	AH6A	8022
32	7395	0000	CF07	0000	7995	0000
33	395A	0000	8C25	0000	9950	0000
34	8F73	0000	0000	0000	0H79	0000
35	F739	0000	UF45	0000	H799	0000
36	3783	0000	0000	0000	637H	0000

I/O SELF TEST DIAGNOSTIC

Test Number: 8

Required Assemblies: A2A7, A2A8, A2A4, A2A5, A2A10.

Description: This test checks the A2A4, A2A5 and A2A10 assemblies by writing data to the outputs of these assemblies and using the internal read-back capability to check that the data at the outputs is the same data that was sent.

Procedure:

1. Remove instrument top cover and DCU covers.
2. Set the test number switch on A2A7 to 8.
3. Install the shorting connector on the top edge connector of A2A7 (at A2A7J1).
4. Connect a jumper between TP4 and TP10 on the A2A7 assembly.
5. Momentarily short TP3 to TP10 on the A2A7 assembly to reset the Microprocessor.
6. Remove the jumper between TP4 and TP10.
7. The test will begin to run. The test takes approximately four seconds to run and it will run continuously until an error is found or the test number switch is changed. The test number " -08- " will be displayed in the left side of the FREQUENCY display. A two digit pass number will be displayed in the AMPLITUDE display. This number is incremented each time the test runs. When it reaches 99, it will reset to 00 with the next increment.

   When an error is detected, a two digit error code is displayed in the right side of the FREQUENCY display and the test stops. The actual and expected data is displayed in the MODULATION displays. The expected data is in the MOD FREQ display and the actual data is in the MOD LEVEL display. Table 8-225, below, shows which output pins are being checked for each error code. To determine the output assembly edge connector pin where the error was detected, do the following:

A. Examine the actual and expected data and determine which bit(s) is bad.

B. Table 8-225 gives the Error Code, Assembly, and edge connector pin number associated with the detected bit error.

Use the troubleshooting procedure with the schematic diagram for the defective assembly to find the source of the problem.

Table 8-224. I/O Self-Test Diagnostic; Bit Error/Pin Number Locations.

ERROR CODE	ASSEMBLY	EDGE CONNECTOR PIN NUMBERS /---------- DATA BIT ----------\ 7	6	5	4	3	2	1	0
10	A2A4	B2	B20	B4	B22	A36	A18	B1	B19
11	A2A4	B7	B25	B8	B26	B5	B23	B6	B24
12	A2A4	--	---	B13	B31	B9	B27	B12	B30
13	A2A4	A16	A34	A17	A35	A14	A32	A15	A33
14	A2A4	A12	A30	A13	A31	A10	A28	A11	A29
15	A2A4	A8	A26	A9	A27	A6	A24	A7	A25
16	A2A4	A4	A22	A5	A23	A2	A20	A3	A21
20	A2A10	B2	B20	B22	B4	A36	A18	B1	B19
21	A2A10	B7	B25	B8	B26	B5	B23	B6	B24
22	A2A10	--	--	B13	B31	B9	B27	B12	B30
23	A2A10	A16	A34	A17	A35	A14	A32	A15	A33
24	A2A10	A12	A13		A32	A10	A28	A11	A29
25	A2A10	A8	A26	A9	A27	A6	A24	A7	A25
32	A2A5	B9	B27	B26	B8	B24	B7	B25	B6
33	A2A5	A9	A29	A11	A28	A10	A32	A14	A27
34	A2A5	B31	B30	B13	B12	A35	A17	A16	A15
35	A2A5	B1	B19	B2	B23	B5	B20	B4	B22
36	A2A5	--	--	A25	A7	A13	A31	A12	A30
37	A2A5	--	A5	A4	A3	A2A	A21	A20	A33

ATTENUATOR TEST DIAGNOSTIC

Test Number: 10 (Test Number Switch Setting = A)

Required Assemblies: All DCU Assemblies.

Required Test Equipment: HP 436A Power Meter
HP 8482A Power Sensor

Description: The RF output of the 8663A is set to 50 Mhz at a level of +16dBm. The keyboard entries allow specific attenuator sections within the programable output step attenuators to be individually selected one at a time.

Procedure:

1. Remove instrument top cover and DCU covers.
2. Set the test number switch on the A2A7 to A, the hexadecimal equivalent of decimal 10.
3. Install the shorting connector on the top edge connector of A2A7 (at A2A7J1).
4. Connect a jumper between TP4 and TP10 on the A2A7 assembly.
5. Momentarily short TP3 to TP10 on the A2A7 assembly to reset the Microprocessor.
6. Remove the jumper between TP4 and TP10.
7. Connect the 436A Power Meter to the 8663A RF output connector via the 8482A Power Sensor.
8. The test number, " -10- ", will be displayed in the left side of the FREQUENCY display. " 0 " will be displayed in the MOD FREQ display. Keyboard data keys 0-6 are used to control the mechanical step attenuators as indicated in Table 8-225, below.

   Pushing one of these keys switches in the attenuator section controlled by that key. Pushing another key switches out the section that is in and switches in a new one. Only one section at a time can be in during the running of this test. The last key pressed is displayed in the MOD FREQ display.
9. Use the 436A (or a spectrum analyzer) to measure the change in level as attenuator sections are switched in and out.

Table 8-225. Output Attenuator Sections Controlled by Data Entry Keys.

	70dB OUTPUT ATTENUATOR AT1			65dB OUTPUT ATTENUATOR AT2		
KEY	10dB	20dB	40dB	5dB	20dB	40dB
0		(none)			(none)	
1	X					
2		X				
3			X			
4				X		
5					X	
6						X
Where: X indicates attenuator section in.						

HP-IB STIMULUS DIAGNOSTIC

Test Number: 11 (Test Switch Number B)

Required Assemblies: A2A7, A2A8, A2A6.

Required Test Equipment: HP IB Controlling Computer (HP 85, 9825, or similar).

Description: This test performs the following tests of the A2A6 HP-IB assembly:

1. Displays the HP-IB address switch setting in the front panel FREQUENCY display.

2. Stimulates the A2A6 assembly for signature analysis testing. The procedure for using this capability will be included in the troubleshooting procedure for the A2A6 assembly with the schematic diagram .

3. Sends a fixed sequence of data bytes via HP-IB. An HP-IB controller can read these bytes. This confirms the 8663A talker capability.

Procedure:

1. Remove instrument top cover and DCU covers.

2. Set the test number switch on the A2A7 to B, the hexadecimal equivalent of decimal 11.

3. Install the shorting connector on the top edge connector of A2A7 (at A2A7J1).

4. Connect a jumper between TP4 and TP10 on the A2A7 assembly.

5. Momentarily short TP3 to TP10 on the A2A7 assembly to reset the Microprocessor.

6. Remove the jumper between TP4 and TP10.

7. The test number, " -11- ", should be displayed in the left side of the FREQUENCY display. The HP-IB address switch (on A2A6) setting should be displayed in the right side of the FREQUENCY display. If the HP-IB address switch is changed the display should change. This checks the capability of the Microprocessor to read the address switch setting. If " -- " is displayed instead of the address switch setting, it means that the Microprocessor is not receiving a valid address switch reading. This would occur if the HP-IB assembly is not in its socket.

   If an HP-IB controller is connected to the 8663A, there will be a delay (approximately 15 seconds) from the time the address switch setting is changed to the time the display changes.

NOTE

Signature analysis testing cannot be performed with a controller connected to the HP-IB interface connector.

8. This test outputs a continuous sequence of data bytes. The sequence starts at 00 (binary all zeroes) and each byte is incremented until the value reaches 255 (binary all ones). The sequence then repeats, starting at 00. A controller can read this data and check for the correct sequence. This confirms that the talker capability of the 8663A is functioning correctly. A sample program to read and check the data is given in figure 8-214, below. This program is written for the HP-85 computer. Note that the 8663A is functioning as a talker. All that the controller must do therefore, is read from any address on the HP-IB and the data will be received. The first data byte read will depend on where the 8663A is in the sequence when the controller performs the read operation. The 8663A is free running and is not synchronized with the controller read operation.

```
 10 OPTION BASE 1
 20 DIM A$[300],A(257)
 30 IOBUFFER A$
 40 TRANSFER 719 TO A$ FHS
 50 FOR I=1 TO 257
 60 ENTER A$ USING "#,B" ; A(I)
 70 NEXT I
 80 FOR J=1 TO 256
 90 IF A(J+1)=0 THEN 110
100 IF A(J)+1#A(J+1) THEN 150
110 NEXT J
120 BEEP
130 DISP "    PASSED ! "
140 GOTO 240
150 ! ERROR FOUND
160 BEEP
170 DISP
180 IF J<=10 THEN J1=J ELSE J1=J-10
190 FOR K=J1 TO J1+12
200 S$=DTB$(A(K))
210 DISP TAB(5);S$[9];A(K)
220 IF K=J+1 THEN DISP "< ERROR!" ELSE DISP
230 NEXT K
240 END
```

Figure 8-214. Sample Controller Program

SWEEP CONTROL/KEYBOARD LED DIAGNOSTIC

Test Number: 12 (Test Switch Number C)

Required Assemblies: A2A7, A2A8, A2A2.

Required Test Equipment: HP 1740A Oscilloscope (or similar).

Description: This test checks the A2A2 Sweep Control Assembly as follows:

1. Stimulates the circuitry for signature analysis testing. Operating instructions will be included with the troubleshooting procedure for the A2A2 assembly and are not included here.

2. Turns all keyboard LEDs on and off at a slow rate so they can be visually checked.

3. Generates output waveforms on the rear panel Z/AXIS BLKG/MKR and SWP outputs.

Procedure:

1. Remove instrument top cover and DCU covers.

2. Set the test number switch to C, the hexadecimal equivalent of decimal 12.

3. Install the shorting connector on the top edge connector of A2A7 (at A2A7J1).

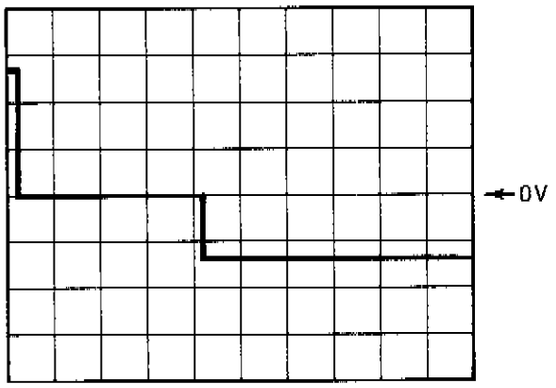
4. Connect a jumper between TP4 and TP10 on the A2A7 assembly.

5. Momentarily short TP3 to TP10 on the A2A7 assembly to reset the Microprocessor.

6. Remove the jumper between TP4 and TP10.

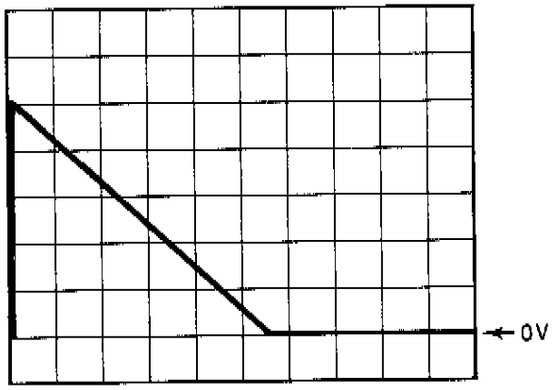
7. The test number, " -12- ", will be displayed in the left side of the FREQUENCY display. All the LEDs on the keyboard will blink at a slow rate.

8. Use an oscilloscope to view the outputs of the rear panel Z/AXIS BLKG/MKR and SWP connectors. Waveforms should be similar to those represented in figures 8-215 and 8-216, below.



Vertical: 2 V/division
Horizontal: 2 ms/division

Figure 8-215. Z/AXIS BLKG/MKR Output; DCU Diagnostic Test 12



Vertical: 2 V/division
Horizontal: 2 ms/division

Figure 8-216. Sweep Output; DCU Diagnostic Test 12

FRONT PANEL DISPLAY DIAGNOSTIC

Test Number: 13 (Test Number Switch D)

Required Assemblies: A2A7, A2A8, A1A1.

Description: This test checks the A1A1 Display Assembly by stimulating the circuitry for signature analysis testing and changing the display at a slow rate for visual testing. Signature analysis testing is covered in the troubleshooting procedure for the A1A1 assembly.

Procedure:

1. Remove instrument top cover and DCU covers.
2. Set the test number switch to D, the hexadecimal equivalent of decimal 13.
3. Install the shorting connector on the top edge connector of A2A7 (at A2A7J1).
4. Connect a jumper between TP4 and TP10 on the A2A7 assembly.
5. Momentarily short TP3 to TP10 on the A2A7 assembly to reset the Microprocessor.
6. Remove the jumper between TP4 and TP10.
7. The test will begin to run. The test number, " -13- ", will be displayed in the left side of the FREQUENCY display for approximately one second. The display will then change and go through a long sequence (55 seconds) during which all digits and annunciators are exercised.

   This sequence is easily interpreted through observation of the front panel for one or two test sequences. It can then be readily determined if any annunciators or displays are malfunctioning.

KEYCODE STIMULUS DIAGNOSTIC

Test Number: 14 (Test Switch Number E)

Required Assemblies: A2A7, A2A8, A2A1, A2A2.

Description: This test stimulates the A2A1 Keycode Assembly for signature analysis testing. Refer to Service Sheets 61 and 62 troubleshooting information for procedures and the use of this Diagnostic.

MAIN AND SWEEP KEYBOARDS MANUAL TEST DIAGNOSTIC

Test Number: 15 (Test Number Switch F)

Required Assemblies: A2A7, A2A8, A2A1, A2A2.

Description: This test displays the keycode as Main or Sweep Keyboard keys are pressed. Thus, the keyboards and much of the A2A1 Keycode assembly is checked.

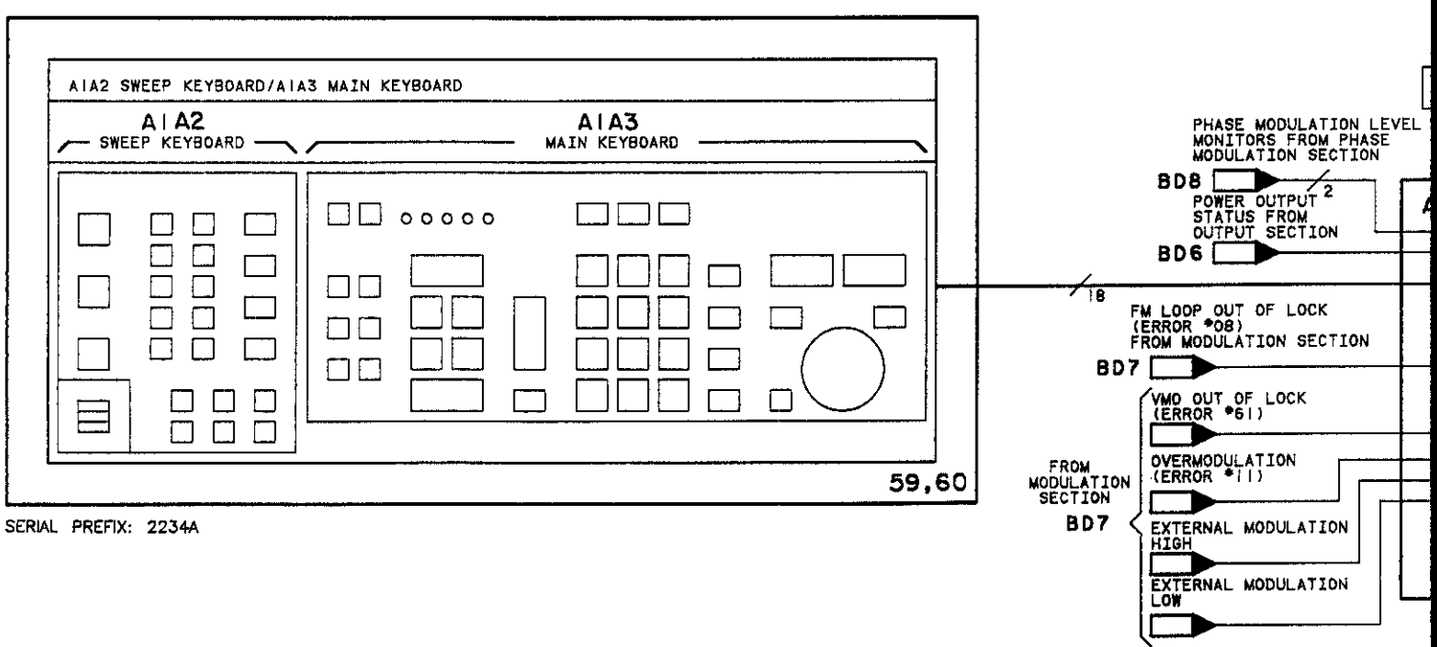
Procedure:

1. Remove instrument top cover and DCU covers.
2. Set the test number switch to F, the hexadecimal equivalent of decimal 15.
3. Install the shorting connector on the top edge connector of A2A7 (at A2A7J1).
4. Connect a jumper between TP4 and TP10 on the A2A7 assembly.
5. Momentarily short TP3 to TP10 on the A2A7 assembly to reset the Microprocessor.
6. Remove the jumper between TP4 and TP10.
7. The test number," -15- ", will be displayed in the left side of the FREQUENCY display. The MOD FREQ display will contain " 000 " until a key is pressed. The display will then be the keycode of the key that was pressed. Keycodes are given in Table 8-226, below.

Table 8-226. Main and Sweep Keyboard Keycodes.

KEY	KEY-CODE	KEY	KEY-CODE	KEY	KEY CODE
NONE	000	AMPLITUDE	105	STORE	134
0	060	MOD FREQ	106	PULSE	135
1	061	BPSK	107	RECALL	136
2	062	START FREQ	110	SEQ	137
3	063	STOP FREQ	111	MODE OFF	140
4	064	MARKER 1	112	AUTO MODE	141
5	065	MARKER 2	113	MANUAL MODE	142
6	066	MARKER 3	114	SINGLE MODE	143
7	067	MARKER 4	115	0.5 ms	144
8	070	MARKER 5	116	1 ms	145
9	071	MARKER OFF	117	2 ms	146
FREQUENCY	072	" . "	120	10 ms	147
INCR SET	073	BACK SPACE	121	100 ms	150
UP ARROW	074	GHz	122	LIN 100	151
DOWN ARROW	075	MHz	123	LIN 1000	152
RESOLUTION		kHz	124	SET SIZE	153
OFF	076	Hz	125	LOG 10%	154
FCTN OFF	077	INT 400	126	LOG 1%	155
/10	100	INT 1K	127	SPAN FREQ	156
X10	101	EXT AC	130	KNOB CCW	160
AM	102	EXT DC	131	KNOB CW	161
FM	103	BLUE KEY	132		
PM	104	STATUS	133		

Fig 8-217
Sht 1 of 5



SERIAL PREFIX: 2234A

Fig 8-217
Sht 2 of 5

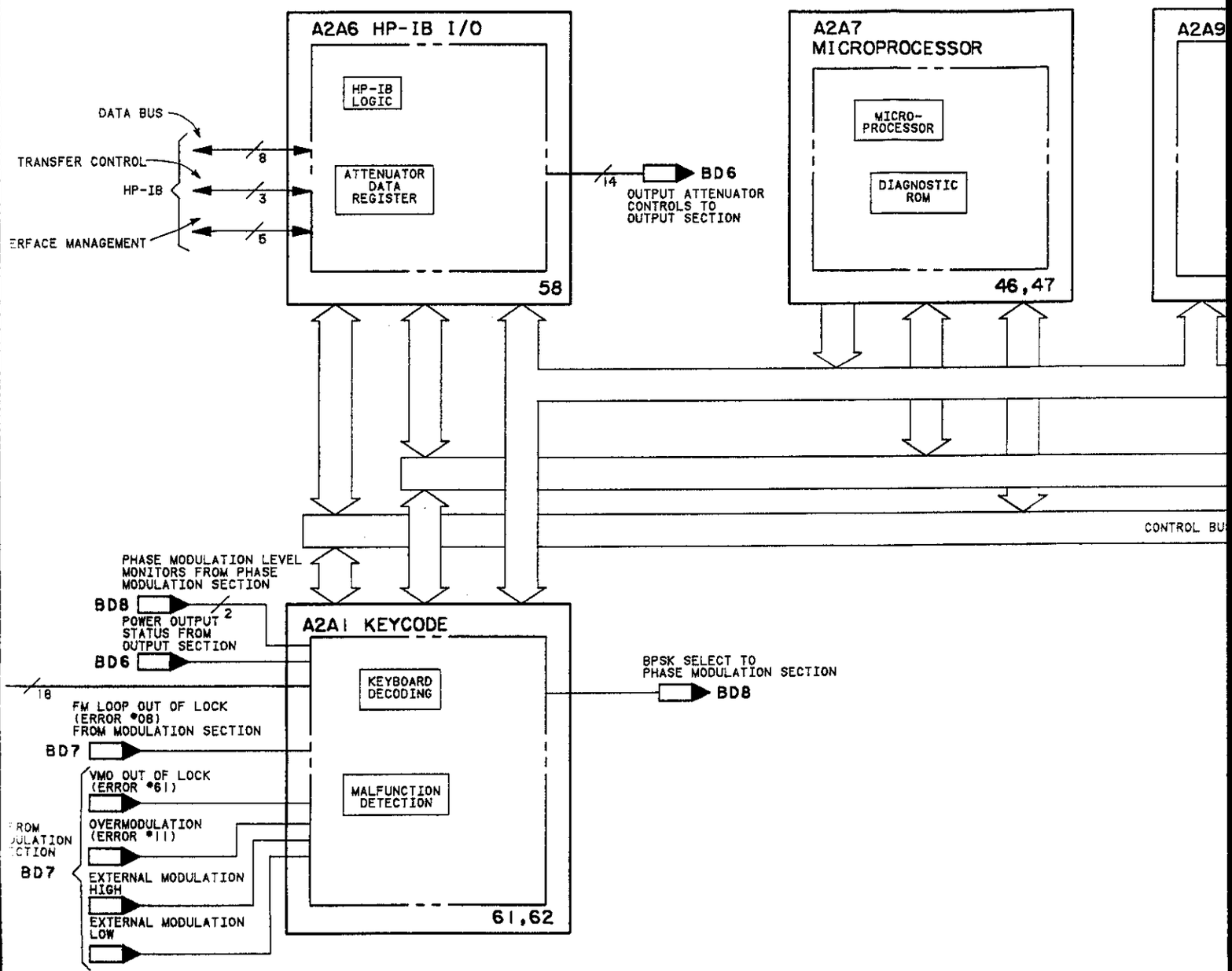


Fig 8-217
Sht 3 of 5

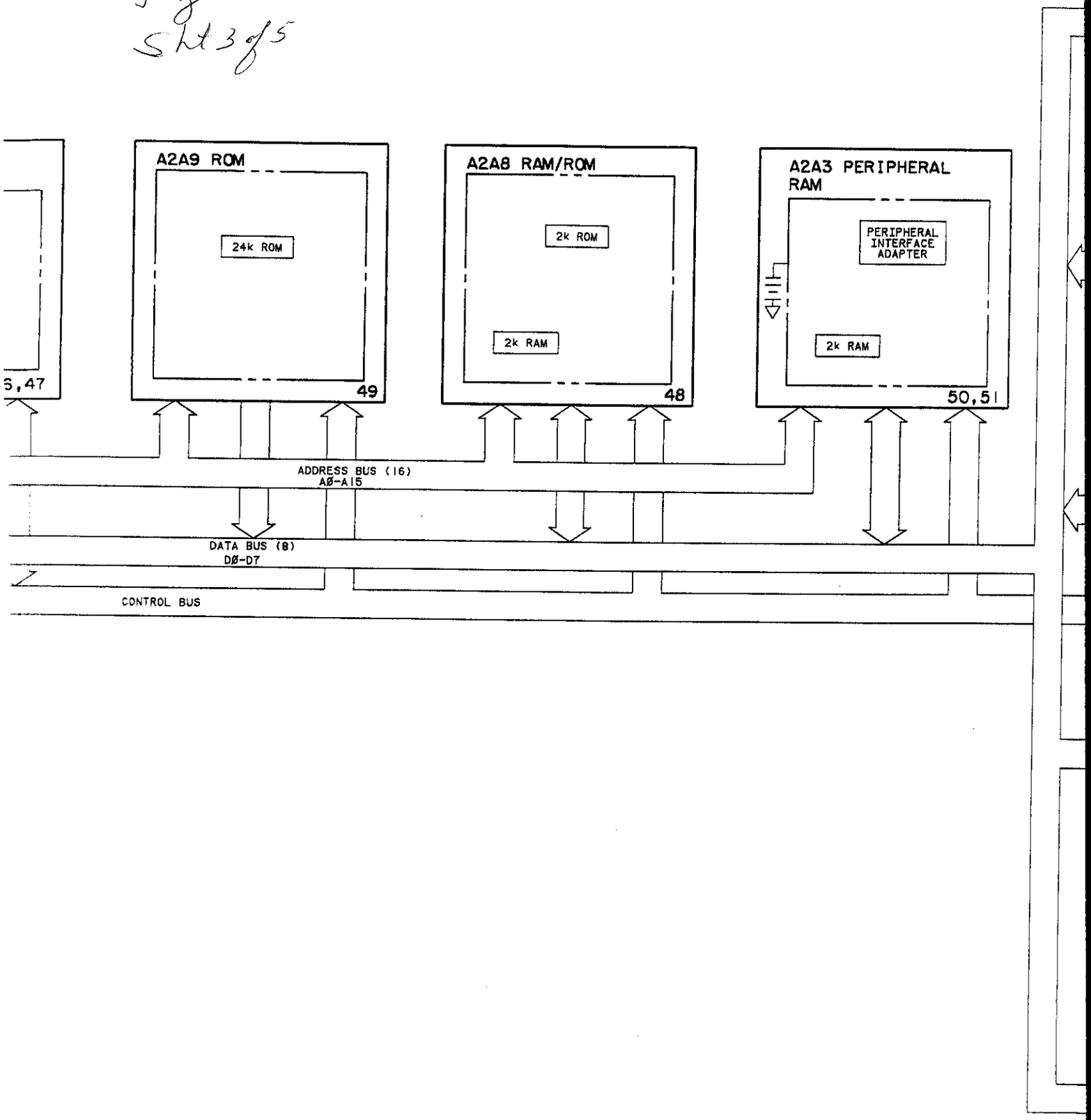
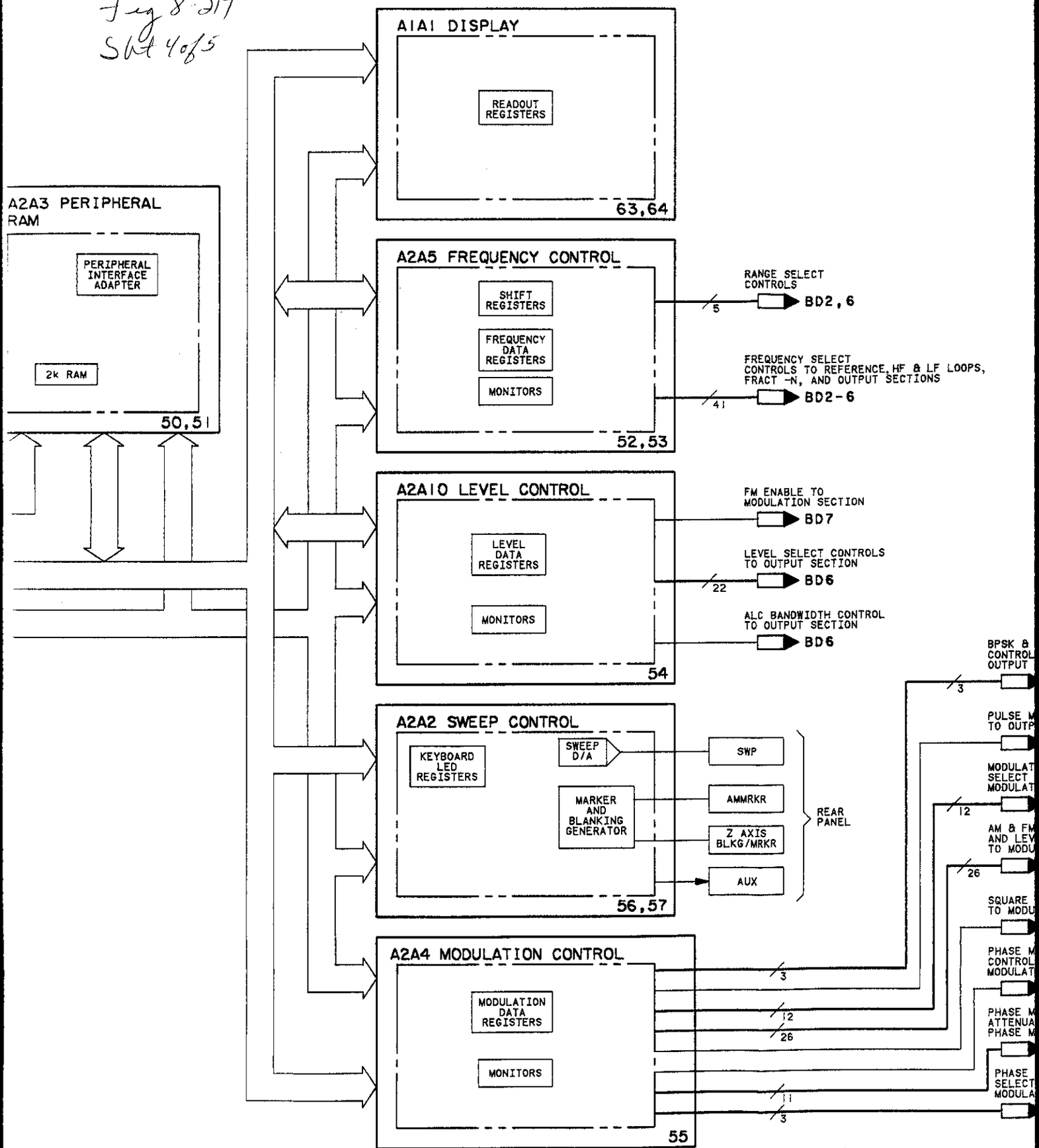
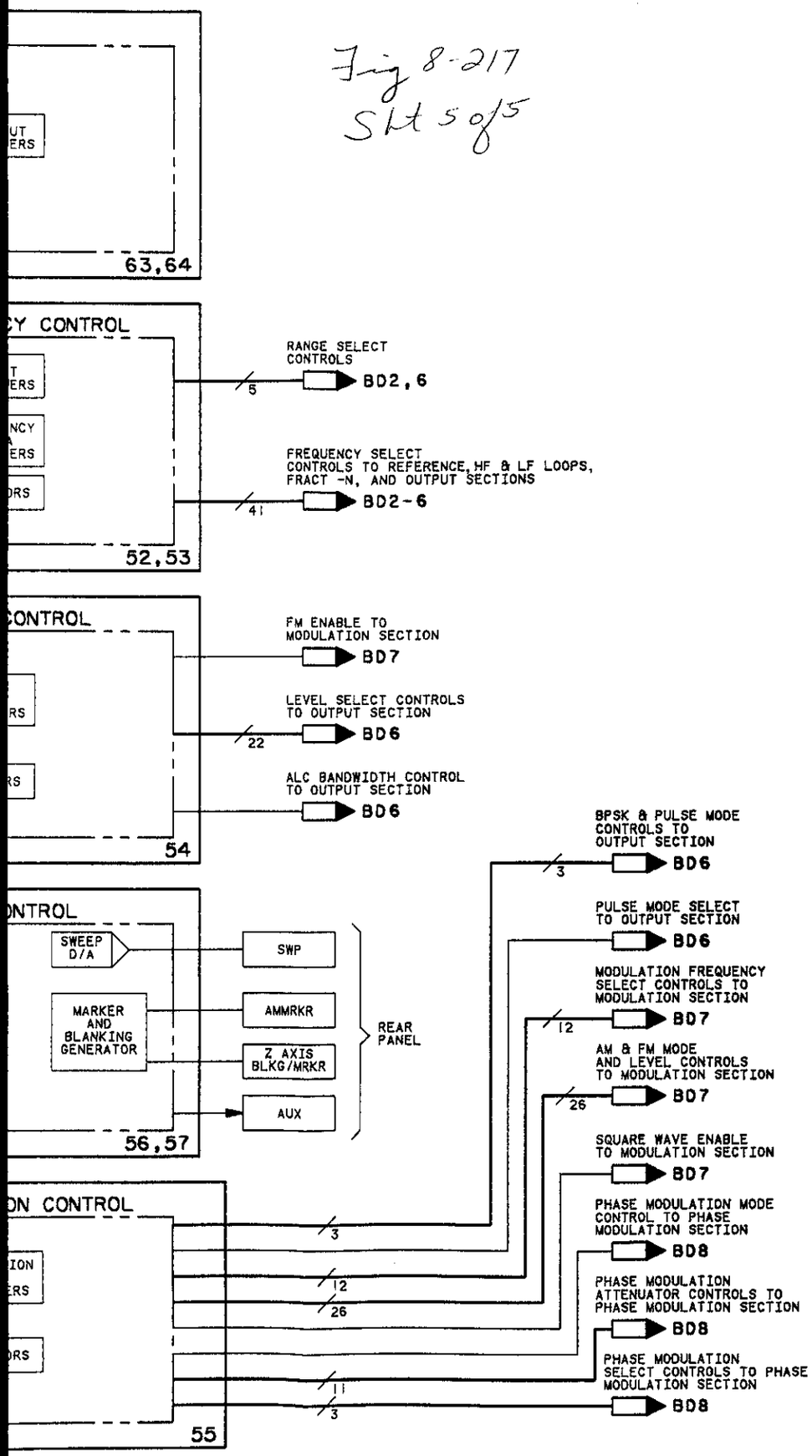


Fig 8-217
SM 4 of 5





BD9

Figure 8-217. Digital Control Unit (DCU) Block Diagram

SERVICE SHEET BD10
POWER SUPPLY SECTION

REFERENCE BD1
Simplified Operation (Section III)
Operator's Checks (Section III)
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

The Signal Generator utilizes a switching power supply for reduced size, weight, and heat dissipation. The supply is made up of five major elements: an input rectifier/filter, the regulator switching transistors, a step-down/isolation transformer, output rectifiers (and associated L-C filters and IC regulators), and a pulse-width-modulated regulation network. The circuitry is on four boards. These are the Power Supply Motherboard, Inverter Board, Control Board, and the Linear Regulator Board. Supplementary circuits include current limiters, overvoltage protection networks, and a reference voltage supply.

At the power line receptacle, the instrument can be switched for use with 115 Vac or 220 Vac power. Following line filtering, the raw ac is rectified and coarsely filtered to produce plus and minus 160 Vdc. In the case of 115 Vac operation, voltage doubling occurs during rectification. The plus and minus 160 Vdc is then chopped at a 20 kHz rate to drive step-down/isolation transformer A7A3T3. Voltages at the tapped outputs of T3 are rectified and filtered. Sense lines from the +5.2 volt supply line are fed to the switching-regulator circuitry on the Control Board. The +5.2 volt line is the only line which is regulated by the switching action of the supply. The +20 Vdc, -10 Vdc, and -40 Vdc lines are maintained at constant voltage by linear regulators (Service Sheet 66)

The +5.2 volt line is regulated by a feedback network consisting of the constant voltage comparator, turn-on level comparator, 40 kHz oscillator, pulse-width modulator (duty-cycle control circuitry), and switch drivers. If the output voltage attempts to decrease, the feedback network senses the change and holds switching transistors A7A3Q3 and A7A3Q4 ON for longer periods of their switching cycles; an attempted increase is corrected by reducing the ON periods of the transistors. In this manner, the power delivered by the supply is matched to the requirements of the instrument, resulting in maximum operating efficiency.

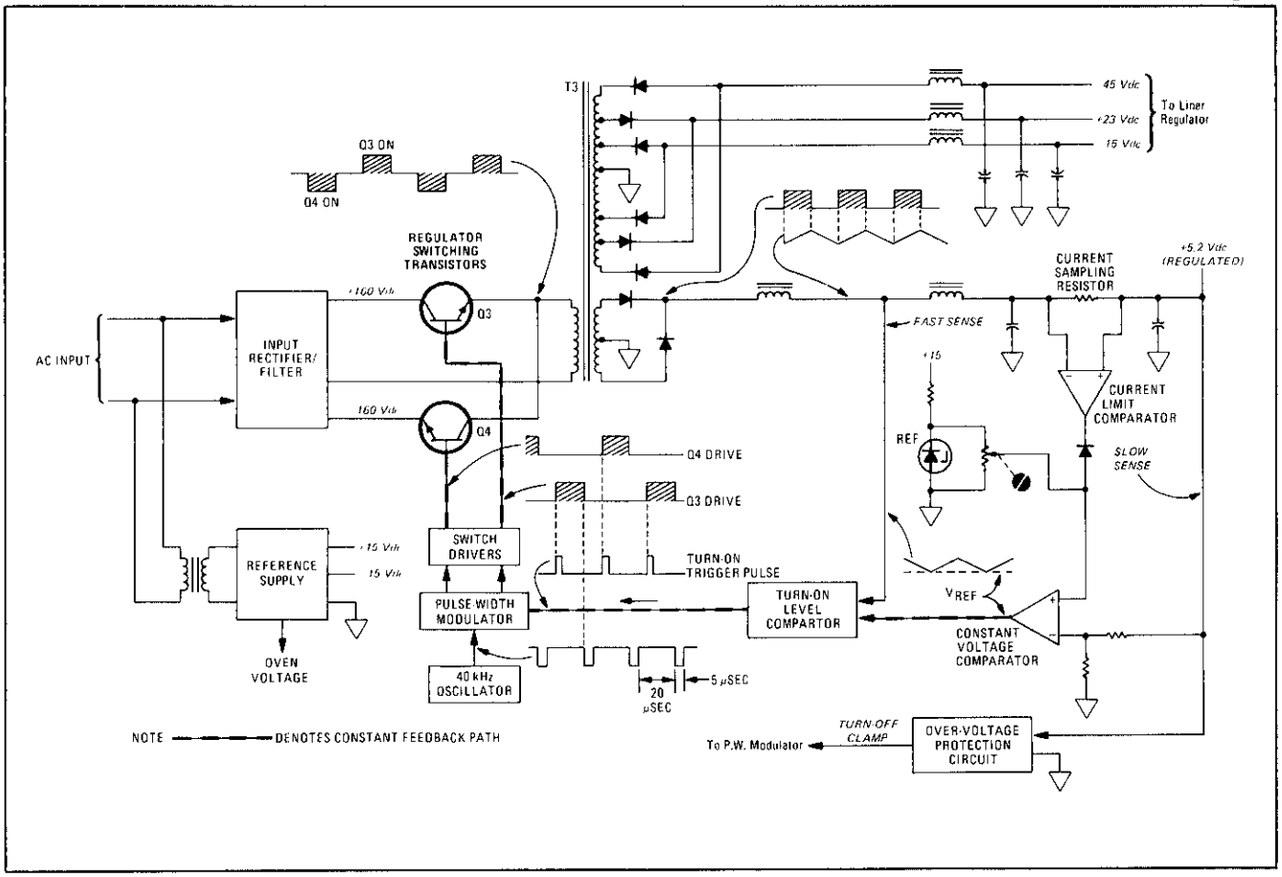


Figure 8-218. Simplified Power Supply Block Diagram

TROUBLESHOOTING

This procedure can be used to isolate a malfunction in the power supply. Once the problem is isolated to an assembly, continue troubleshooting on the service sheet for that assembly to find the bad component.

WARNING

Plus and minus 160 Vdc, and line voltage, are present whenever the power cable is plugged in. This high voltage exists on the red heatsink, on the other portions of the inverter board and on the motherboard. Be extremely careful when working in this area.

Before removing or inserting power supply plug-in boards, disconnect ac power cable and allow 30 seconds for filter capacitors to discharge.

Failure to observe these precautions may result in injury to personnel or damage to equipment.

CAUTION

If the line fuse burns out, do not replace it until the cause of the failure has been determined and repaired (by a qualified service person only and specifically with resistance checks in the power supply. (See Service Sheet 65). Replacing this fuse in a damaged generator can cause additional damage.

1. General

Measure the +5.2V test point with a DVM. If the reading is not 5.20 ± 0.02 Vdc and cannot be adjusted to bring the voltage within these limits, continue troubleshooting with the next step listed in Table 8-227, based on the DVM reading. The +5.2V supply should be operating normally before working on problems with the other supply voltages. If the +5.2V supply is normal and one of the other supply voltages is not, continue troubleshooting with step 5.

Table 8-227. +5.2V Test Point Conditions

DVM Reading	Condition	Next Step
V < 0.05	Shut down	2
0.05< V < 5.20	Low Voltage	5
5.18< V < 5.22	Normal	6
V > 5.22	High Voltage	7

2. Shut Down

Check the following:

a) The linear regulator overvoltage shut-down LED visible through an opening in the top of the power supply. If this LED is lit, the overvoltage shut-down has triggered so continue troubleshooting with step 3.

b) The fuses on the rear panel. If either fuse is blown, continue troubleshooting with Service Sheet 65.

c) Disconnect the line cord from the rear panel of the Generator.

d) Extend the A7A2 Control Board Assembly using the extender board from the service accessory kit. Connect the line cord and turn the Power switch to ON. Look at TP6 and TP7 on A7A2. These waveforms should be similar to those shown on the block diagramms pins 10 and 11). If these waveforms are not present (that is, only a dc level is present), the problem is most likely on A7A2 so continue troubleshooting on Service Sheet 67. If these waveforms are present, the problem is most likely on A7A3 so continue troubleshooting on Service Sheet 65.

3. **Linear Regulator Overvoltage Shutdown**

Turn the Power switch to STANDBY. Unplug the line cord from the rear panel. Remove the A7A1 Linear Regulator Assembly from the instrument. Mount the A7A2 Control Board Assembly on its extender board from the service kit. Connect a short jumper wire between TP5 and ground on A7A2. Connect the line cord and turn the Power switch to ON. Measure TP1 (5.2V supply) on A7A2.

If the voltage is 5.20 $\pm$ 0.02 Vdc or can be adjusted to within the range, the problem is on the A7A1 assembly so continue troubleshooting on Service Sheet 66. Otherwise, refer to Table 8-228, and continue troubleshooting with the next step listed in the table based on the actual voltage reading at TP1. The jumper from TP1 to ground must remain connected and A7A1 must remain out of the power supply. Once the +5.2V supply is normal, remove the jumper and install A7A1. Measure all supplies. If there are any abnormalities, restart with step 1 of this procedure.

4. **+5.2V Supply Low**

Turn the Power switch to STANDBY and unplug the line cord from the rear panel. Mount the A7A2 Control Board Assembly on its extender board. Connect the line cord and turn the line switch to ON. Use a DVM with floating inputs and measure the voltage between pins 17 and 18 on the edge connector of A7A2. This voltage is the drop across the current sensing resistor in series with the output. If this voltage is greater than 0.070V, the load is drawing too much current and the supply is in current limit. Look for the cause of the excess current draw in the other sections of the instrument. If the problem is not current limiting, look at TP6 and TP7 with an oscilloscope. The waveforms should be as shown on the block diagram. The pulse width of the positive part of the waveform should be 20us or more. If the pulse width is less, there is a problem on the A7A2 Control Board so continue troubleshooting on Service Sheet 67. If the pulse width is normal, the problem is most likely on the

A7A3 Inverter Board or the A7A4 motherboard so continue troubleshooting on Service Sheet 65.

5. +5.2V Supply Normal, Linear Regulator Problem

Table 8-228 gives the normal input and output voltages for the A7A1 Linear Regulator Board and the test points where these voltages can be measured.

Table 8-228. Linear Regulator Voltages

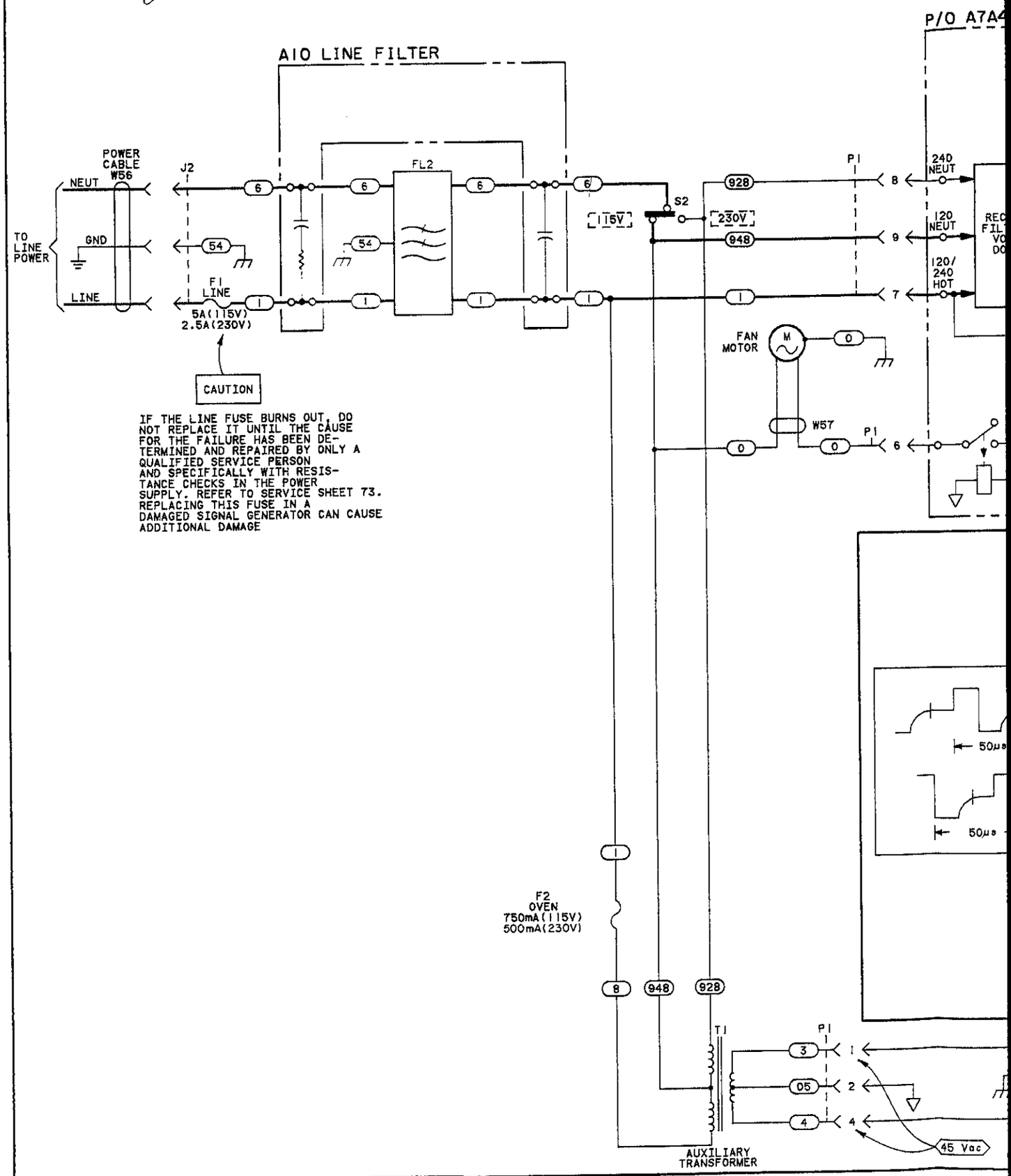
Normal Output (Vdc)	Output	Input	Normal Input (Vdc)
20.0 ±0.1	TP1	TP4	> +22.5
-10.0 ±0.04	TP2	TP5	> -12.5
-40.0 ±0.2	TP3	TP6	> -44.0

Measure the outputs and try to adjust any that are not within the normal range. If an output is too high, the problem is most likely on the A7A1 Linear Regulator. If an output voltage is low, measure the input. If the input is too low, the problem is likely to be on the A7A3 Inverter Assembly but if the input is normal, the A7A1 Linear Regulator is malfunctioning or the load is drawing too much current. Continue troubleshooting with the service sheet where the problem appears to be.

6. +5.2V Supply Higher Than Normal

This is most likely a problem with A7A2 Control Assembly. Continue troubleshooting on Service Sheet 67.

Fig 8-219 Sht 1 of 5



SERIAL PREFIX: 2234A

Fig 8-217 Sht 2 of 5

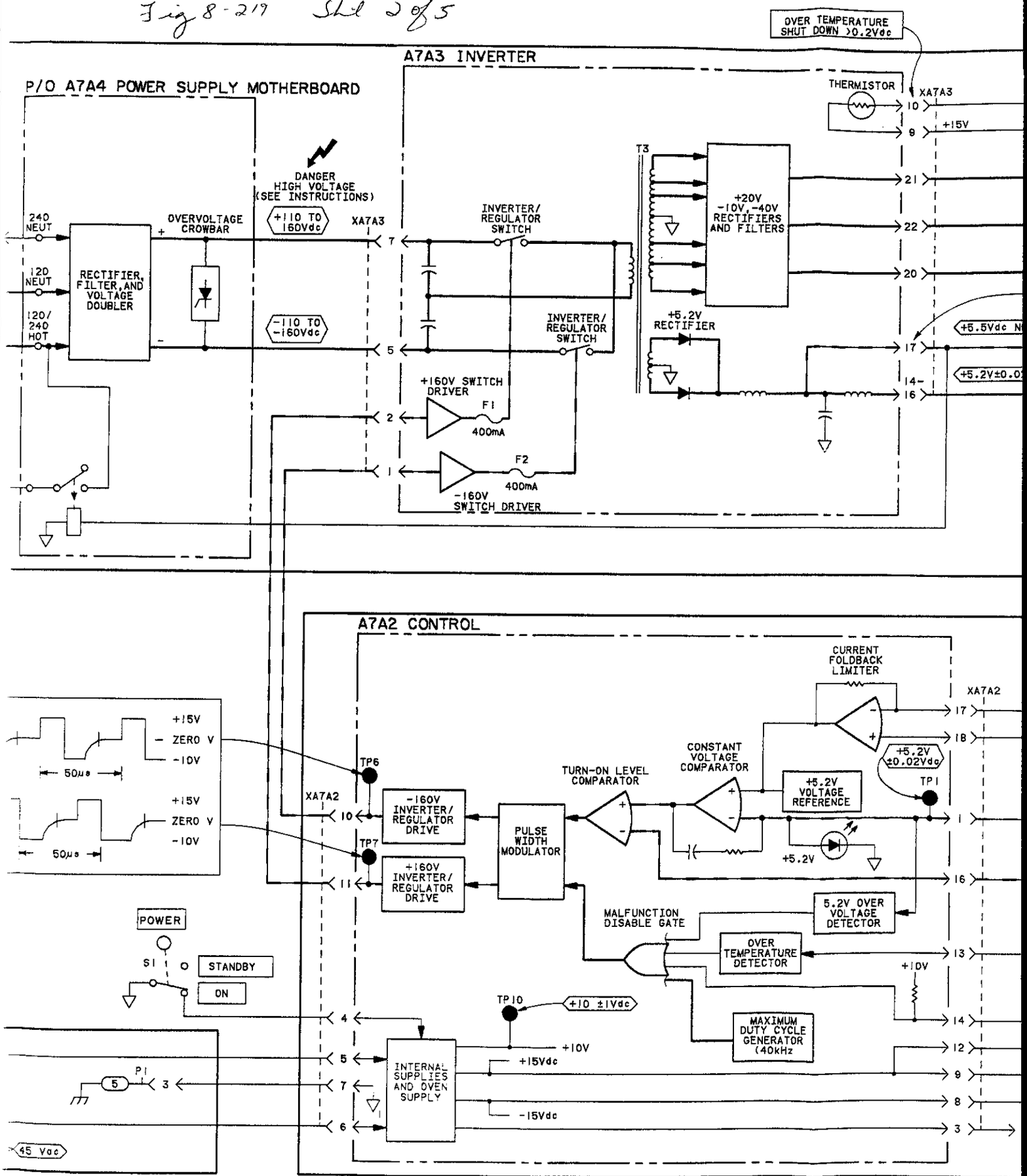


Fig 8-219
Sht 3 of 5

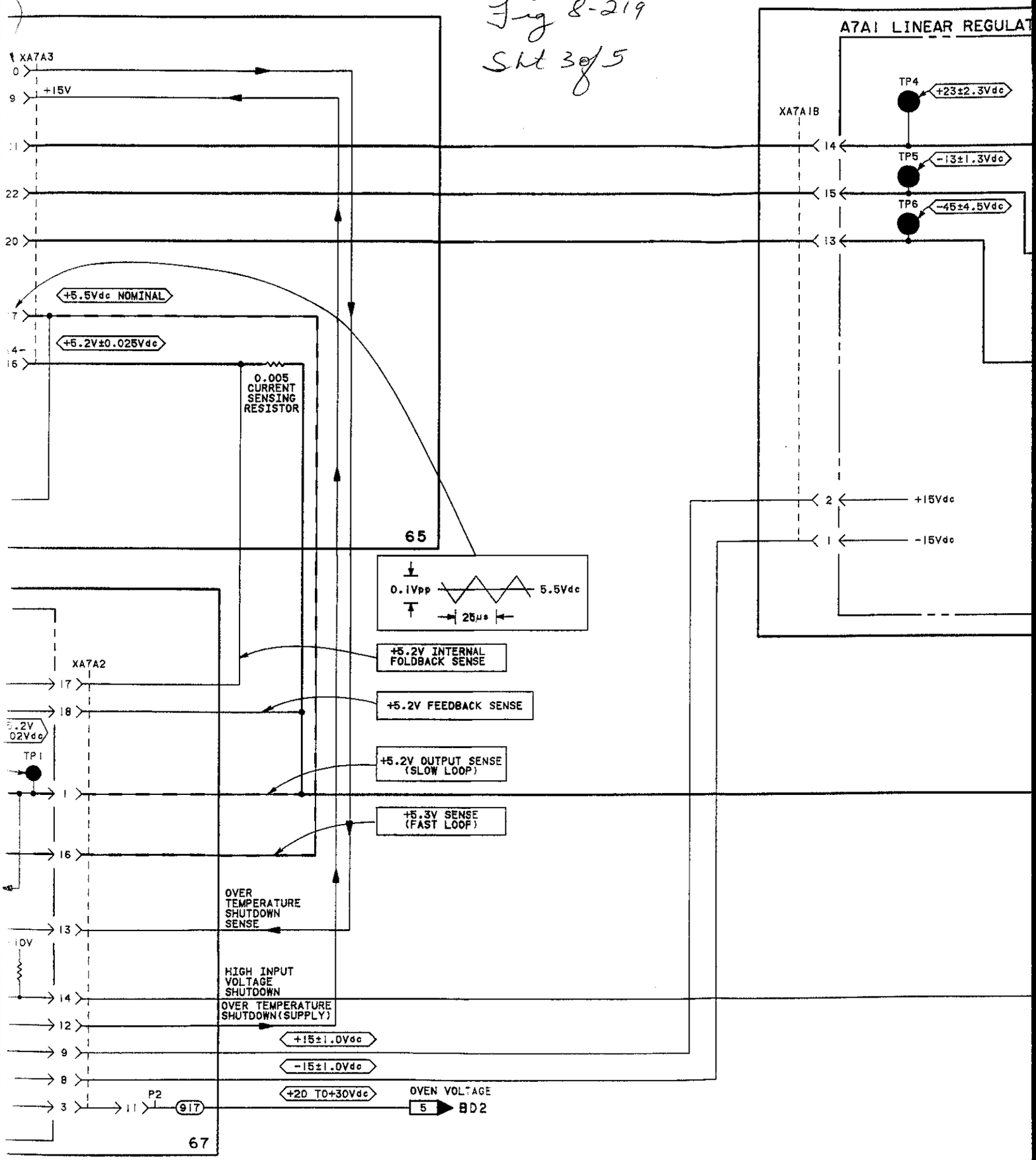
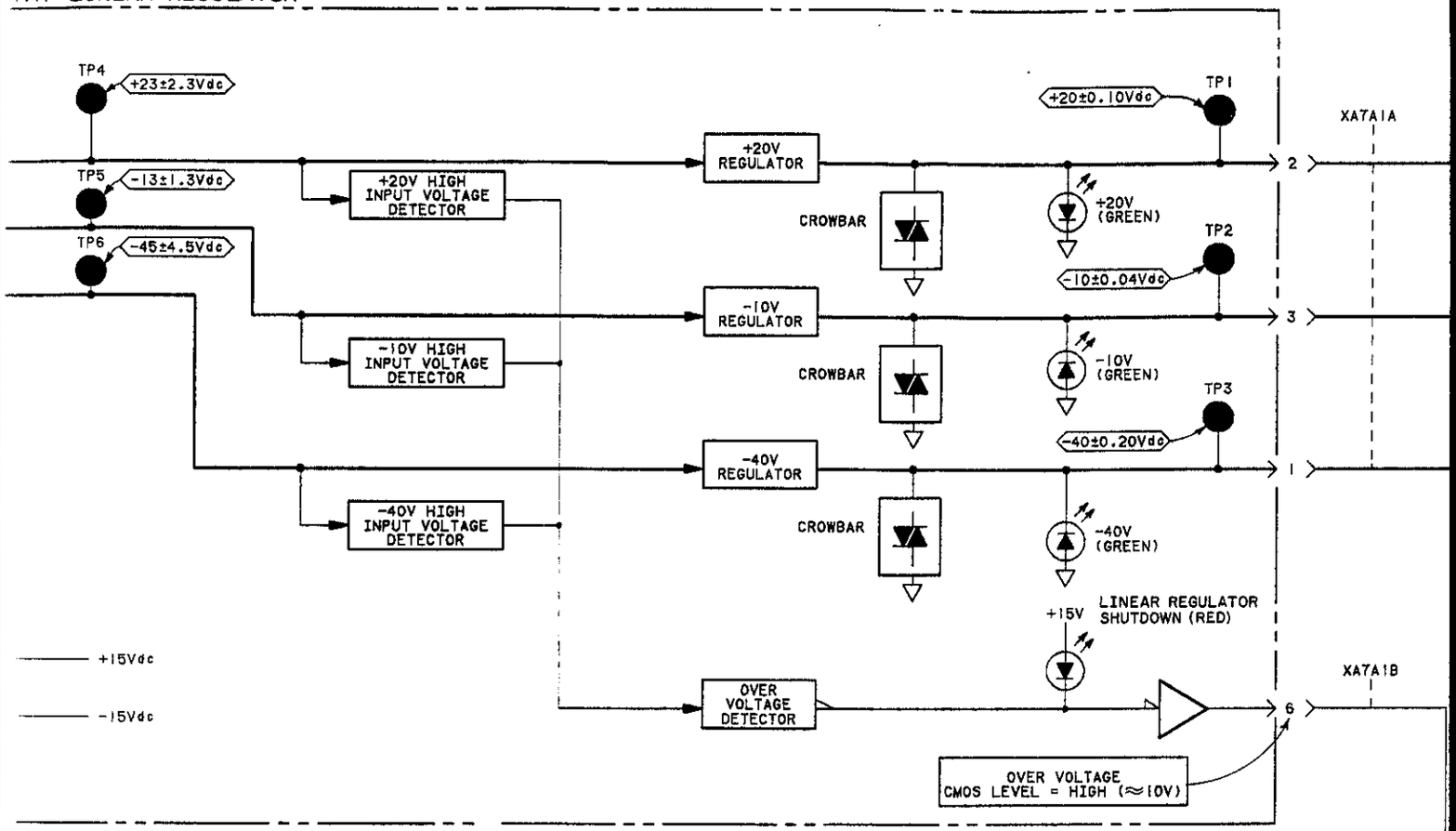


Fig 8-219 Sht 4 of 5

7A1 LINEAR REGULATOR

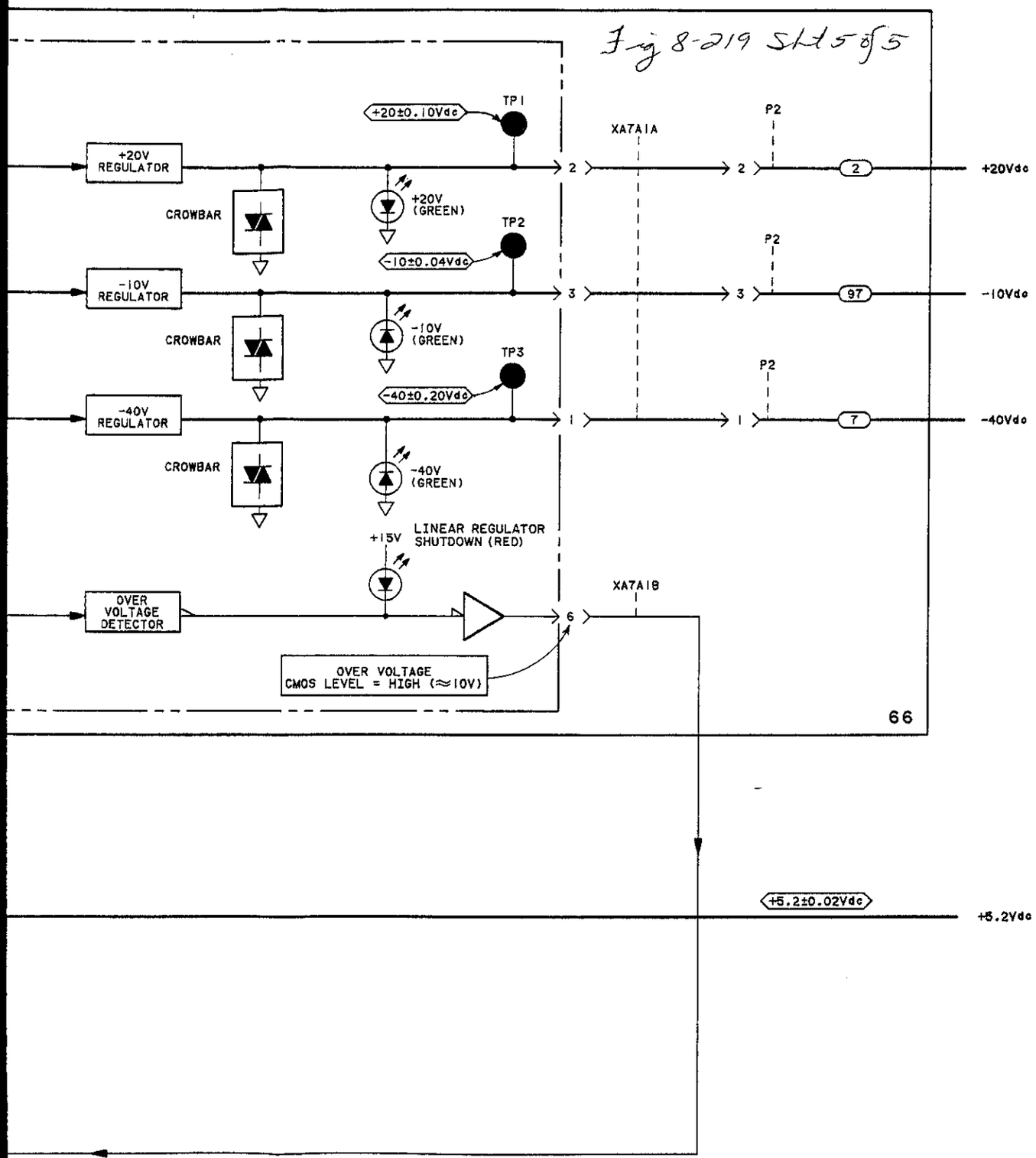


DANGER

PLUS AND MINUS 160VDC AND LINE VOLTAGE ARE PRESENT WHENEVER THE POWER CABLE IS PLUGGED IN. THIS HIGH VOLTAGE EXISTS ON THE RED HEAT SINK, ON THE OTHER PORTIONS OF THE INVERTER BOARD, AND ON THE MOTHERBOARD. BE EXTREMELY CAREFUL WHEN WORKING IN THESE AREAS.

BEFORE REMOVING OR INSERTING POWER SUPPLY PLUG-IN BOARDS, DISCONNECT THE AC POWER CABLE AND ALLOW 30 SECONDS FOR THE FILTER CAPACITORS TO DISCHARGE.

FAILURE TO OBSERVE THESE PRECAUTIONS MAY RESULT IN INJURY TO PERSONNEL OR DAMAGE TO THE EQUIPMENT.



DANGER

AND MINUS 160VDC AND LINE VOLTAGE ARE PRESENT WHENEVER THE POWER CABLE IS
GED IN. THIS HIGH VOLTAGE EXISTS ON THE RED HEAT SINK, ON THE OTHER PORTIONS OF THE
RTER BOARD, AND ON THE MOTHERBOARD. BE EXTREMELY CAREFUL WHEN WORKING IN
E AREAS.

RE REMOVING OR INSERTING POWER SUPPLY PLUG-IN BOARDS, DISCONNECT THE AC POWER
E AND ALLOW 30 SECONDS FOR THE FILTER CAPACITORS TO DISCHARGE.

URE TO OBSERVE THESE PRECAUTIONS MAY RESULT IN INJURY TO PERSONNEL OR DAMAGE
HE EQUIPMENT.

BD10

Figure 8-219. Power Supply Block Diagram

SERVICE SHEET 1
A8A3 AND A8A4-10 MHz REFERENCE OSCILLATOR AND REFERENCE BUFFER ASSEMBLY

REFERENCE BLOCK DIAGRAM 2
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Reference Buffer amplifies and distributes the reference source signal to the rest of the instrument. The reference source can be the internal 10 MHz Reference Oscillator (A8A3) or an external frequency standard of 5 or 10 MHz. The outputs from the Reference Buffer are always 10 MHz, even when an external frequency standard of 5 MHz is selected. The internal reference oscillator is a high stability, temperature controlled, 10 MHz quartz oscillator.

Doubler Circuit

When an external frequency standard of 5 MHz is used, the 5 MHz signal is passed through a frequency doubler circuit. The doubler circuit is a full-wave rectifier, consisting of a center-tapped transformer (T1) and two Schottky diodes (CR1 and CR2). Following the doubler circuit is a 10 MHz bandpass amplifier which minimizes the feed through of the fundamental frequency (5 MHz).

Power Splitters

Transformers T2 through T9 and associated circuitry form a five-way power splitter. The 10 MHz input signal is applied to the primary of transformer T2. The resistors across the secondary windings of T4, T7, T8, and T9 provide a 50 ohm impedance match and also increase isolation between the five output ports.

No Reference Detector

The No Reference Detector monitors the output of Q2 to check for the presence of the 10 MHz signal. As long as the 10 MHz reference signal is present, capacitor C17 remains charged. In the absence of the 10 MHz signal due to the loss of the reference source (at its inverting input) the comparator goes low, signaling the DCU that no signal is present at the output of Q2.

Oven Status Detector

The Oven Status Detector detects whether or not the internal oscillator's oven temperature has stabilized. From a cold start, that is, the instrument has not been plugged into the Main (line) voltage, the voltage at the oven monitor terminal (A8A3 pin 11) is high. This causes the comparator's output to go low, which signals the DCU that the oven temerature has not heat stabilized. As the oven temperature stabilizes the voltage at the oven monitor terminal drops. It takes approximately 15 minutes for the oven temperature to heat stabilize after the line cord has been plugged in. Power is still supplied to the oven (via A8A3 pin 14) when the LINE switch is in the STANDBY position. From a cold start, the oscillator should be within one hertz of its final value after 10 minutes.

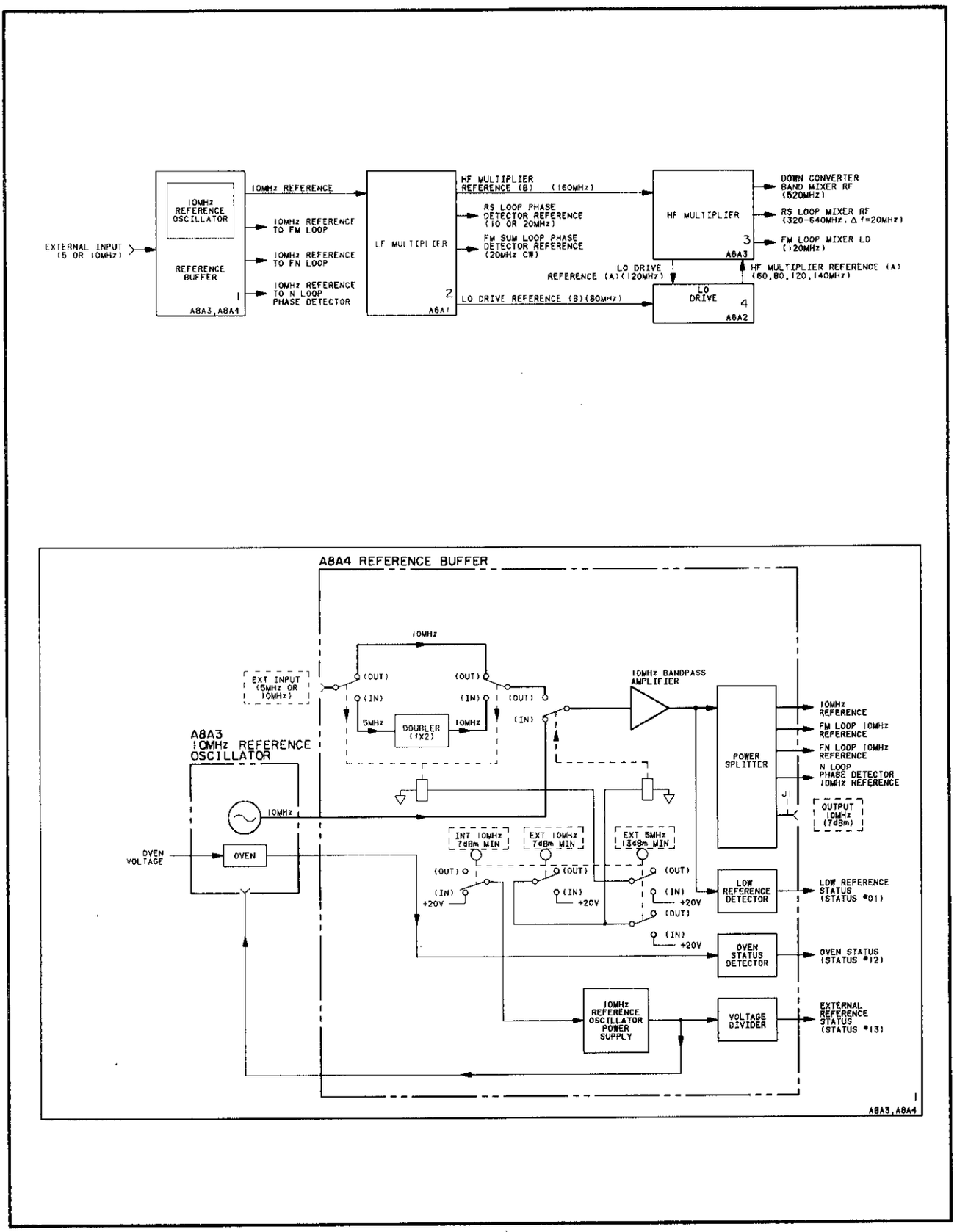
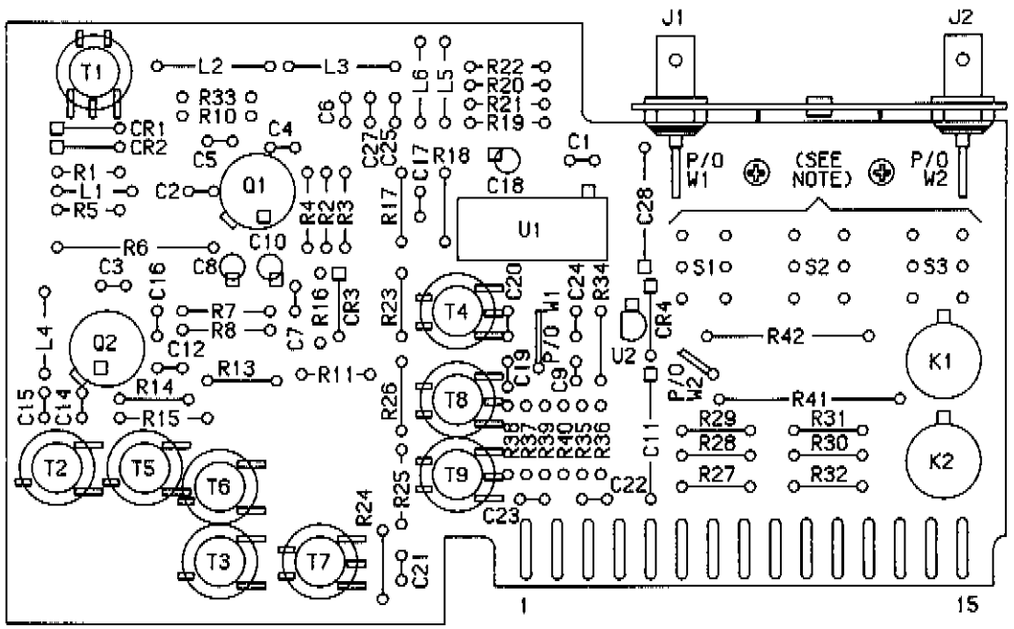


Figure 8-301. A8A3 and A8A4 10 MHz Reference Oscillator & Buffer Block Diagrams

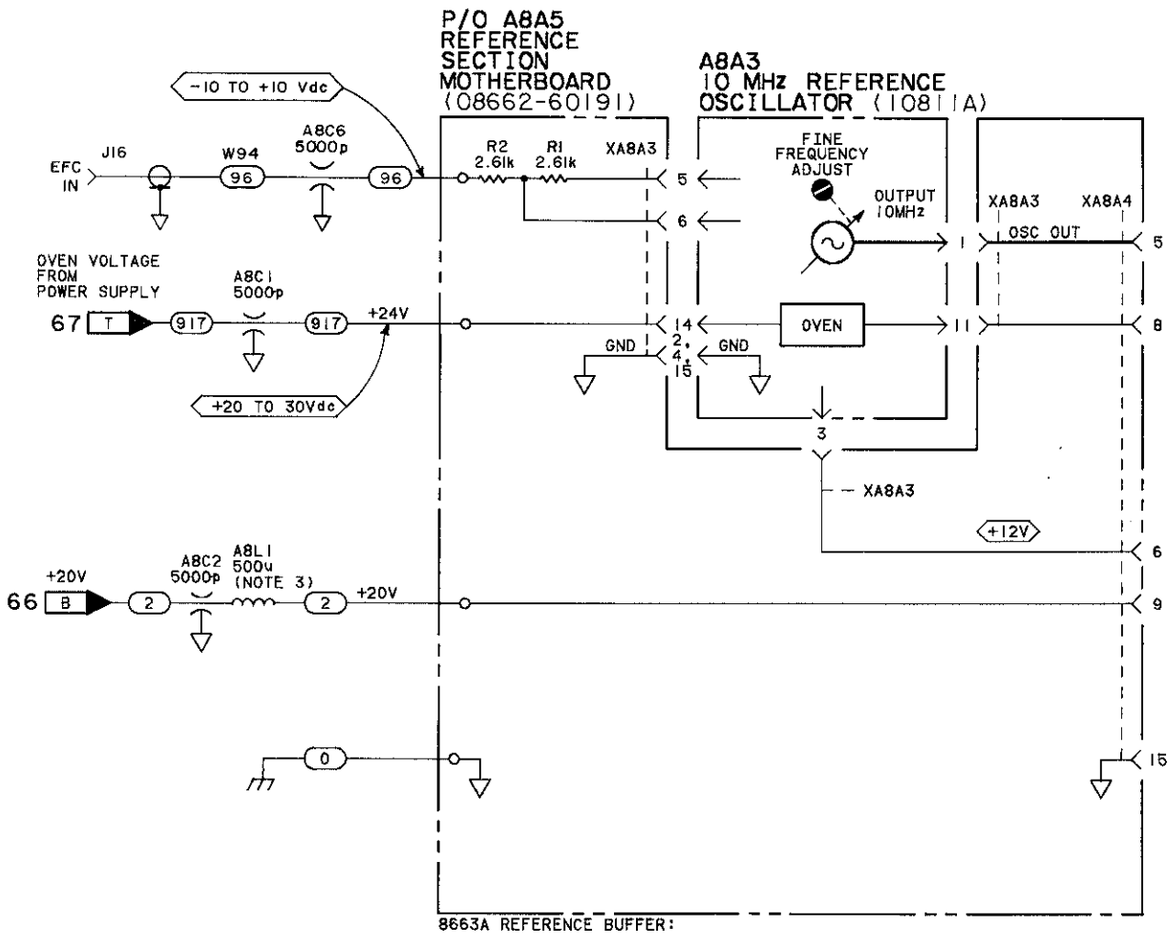


NOTE:
SWITCHES S1, S2, S3 ARE
MOUNTED ON CIRCUIT SIDE
OF BOARD

Figure 8-302. A8A4 Reference Buffer Component Locator

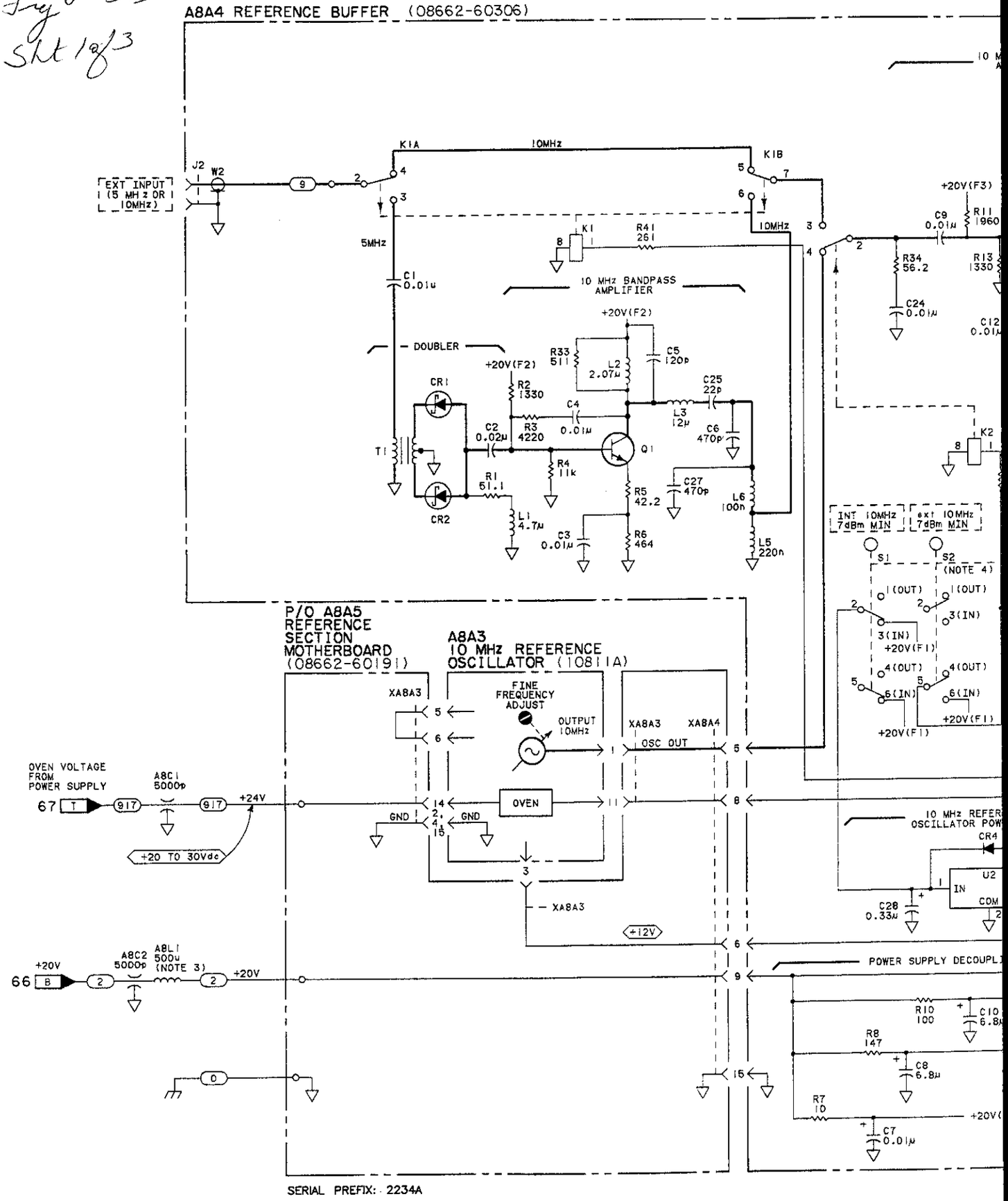
CHANGES

All serial prefixes	**On the A8A4 Component Locator:** • **U2** - Correct the position of U2 by turning it 180°'s.
2408A and above	**On the A8A3 schematic:** • **J16, W94, W96, A8C6, A8A5R1-R2** - Use the partial schematic on page 8-304.3.
2447A and above	**On the A8A3 schematic:** • **10811-60111** - Change the part number of the A8A3 10 MHz REFERENCE OSCILLATOR to 10811-60111.



P/O Figure 8-303. *A8A3 and A8A4 10 MHz Reference Oscillator and Buffer Schematic (2408A)*

Fig 8-303
Sht 1 of 3



SERIAL PREFIX: 2234A

Fig 8-303 Sht 2 of 3

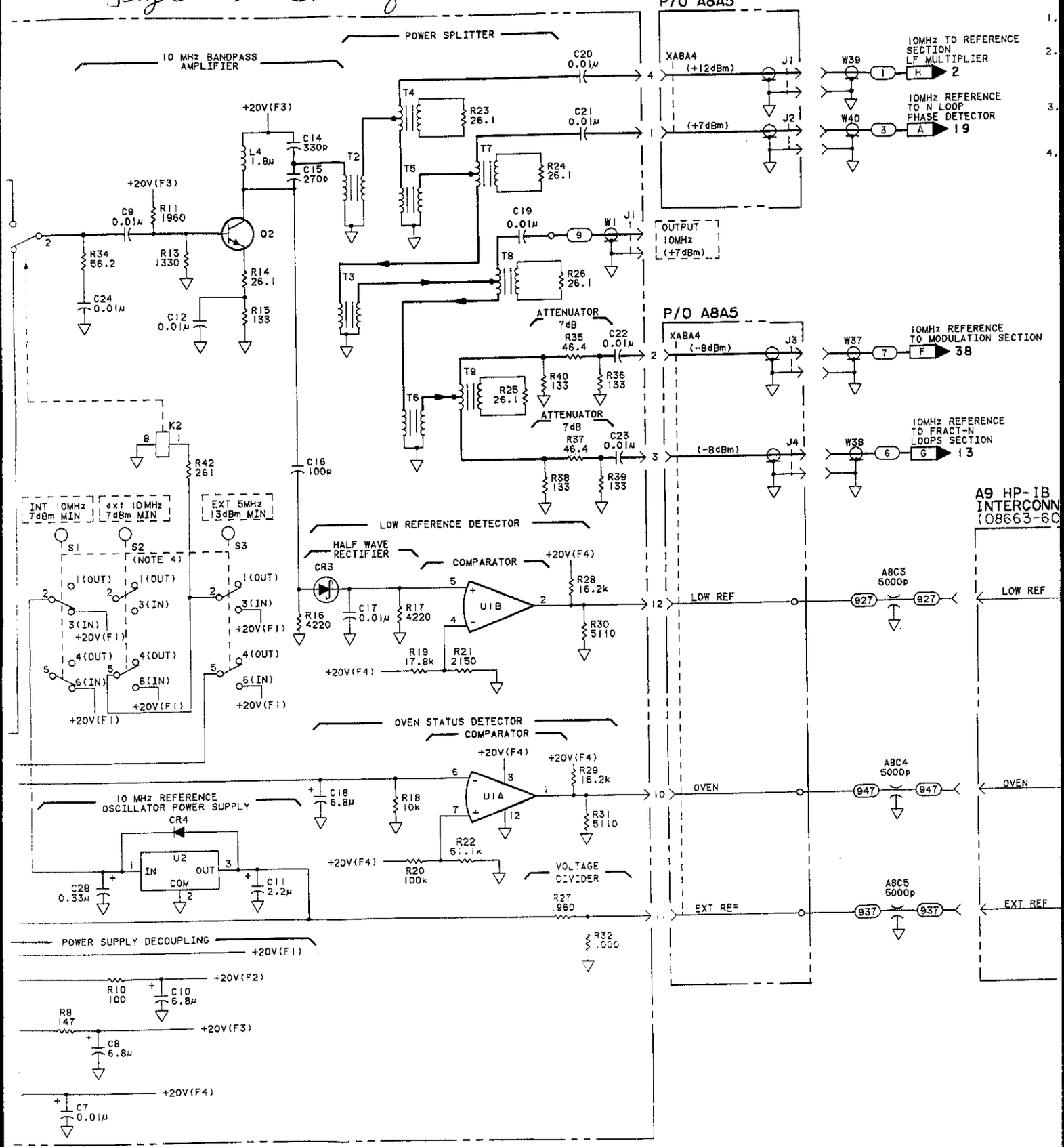


Fig 8-303
Sht 3 of 3

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENT MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. A8L1 IS FORMED BY WINDING ONE TURN OF THE +20V SUPPLY WIRE (COLOR CODE RED) AROUND A TOROID CORE.
4. THE THREE REAR PANEL FREQUENCY REFERENCE SWITCHES (A8A4S1,2,3) ARE MECHANICALLY CONNECTED TOGETHER. WHEN ONE SWITCH IS PUSHED IN, THE OTHER TWO SWITCHES WILL BE RELEASED.

z TO REFERENCE
ION
ULTIPLIER
▶ 2

z REFERENCE
LOOP
E DETECTOR
▶ 19

z REFERENCE
ODULATION SECTION
▶ 38

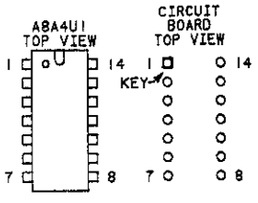
z REFERENCE
RACT-N
S SECTION
▶ 13

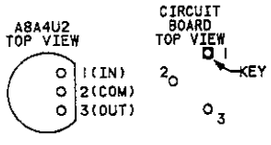
REFERENCE DESIGNATIONS

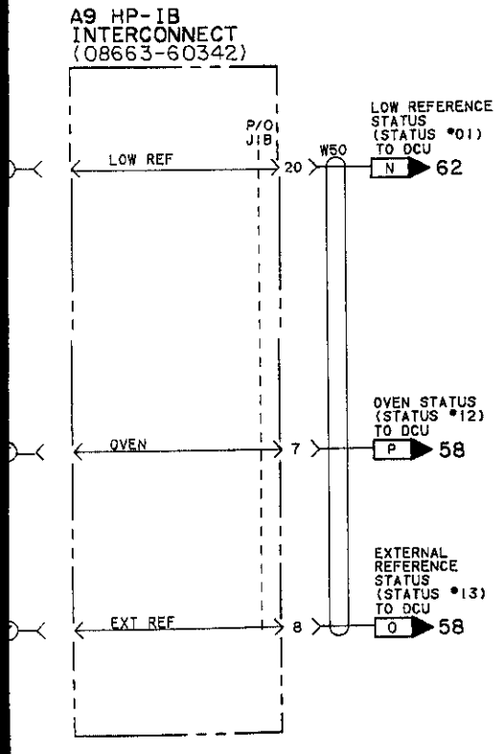
NO PREFIX	A8A4
W37-40,50	C1-12,14-25,27,28 CR1-4 J1,2 K1,2 L1-6 Q1,2 R1-8,10,11,13-42 S1-3 T1-9 U1,2 W1,2
A8	A8A5
	J1-4
C1-5 L1	XA8A3,4
	A9
	J1

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,2	1854-0247
U1	1826-0138
U2	1826-0275







SERVICE SHEET 1

A8A3, A8A4

Figure 8-303. A8A3 and A8A4 10 MHz Reference Oscillator & Buffer Schematic

SERVICE SHEET 2
A6A1 LF MULTIPLIER ASSEMBLY

REFERENCE BLOCK DIAGRAM 2
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The LF Multiplier (A6A1) provides output signals at 10 MHz, 20 MHz, 40 MHz, 80 MHz, and 160 MHz. The LF multiplier takes the 10 MHz signal from the reference buffer (A8A4) and by the use of frequency doubler and divider circuits it generates the other desired frequencies. Since all the output signals are derived from the 10 MHz Reference Buffer signals, they all retain the same accuracy and stability as the reference source signal.

Four frequency doubler circuits are cascaded in order to multiply the 10 MHz input up to 160 MHz. The other output signals are obtained by tapping various points in the doubler chain. The Doubler circuits are basically full-wave rectifier circuits, consisting of a center-tapped transformer and two Schottky diodes.

Following each Doubler circuit are Band-Pass Amplifiers which are tuned to the doubled frequency. This minimizes the feed through of the fundamental frequency and eliminates unwanted harmonics.

The 40 MHz Filter, FL1 is a narrrow band crystal filter. This filter contributes significantly to the Signal Generator's single-sideband phase noise performance.

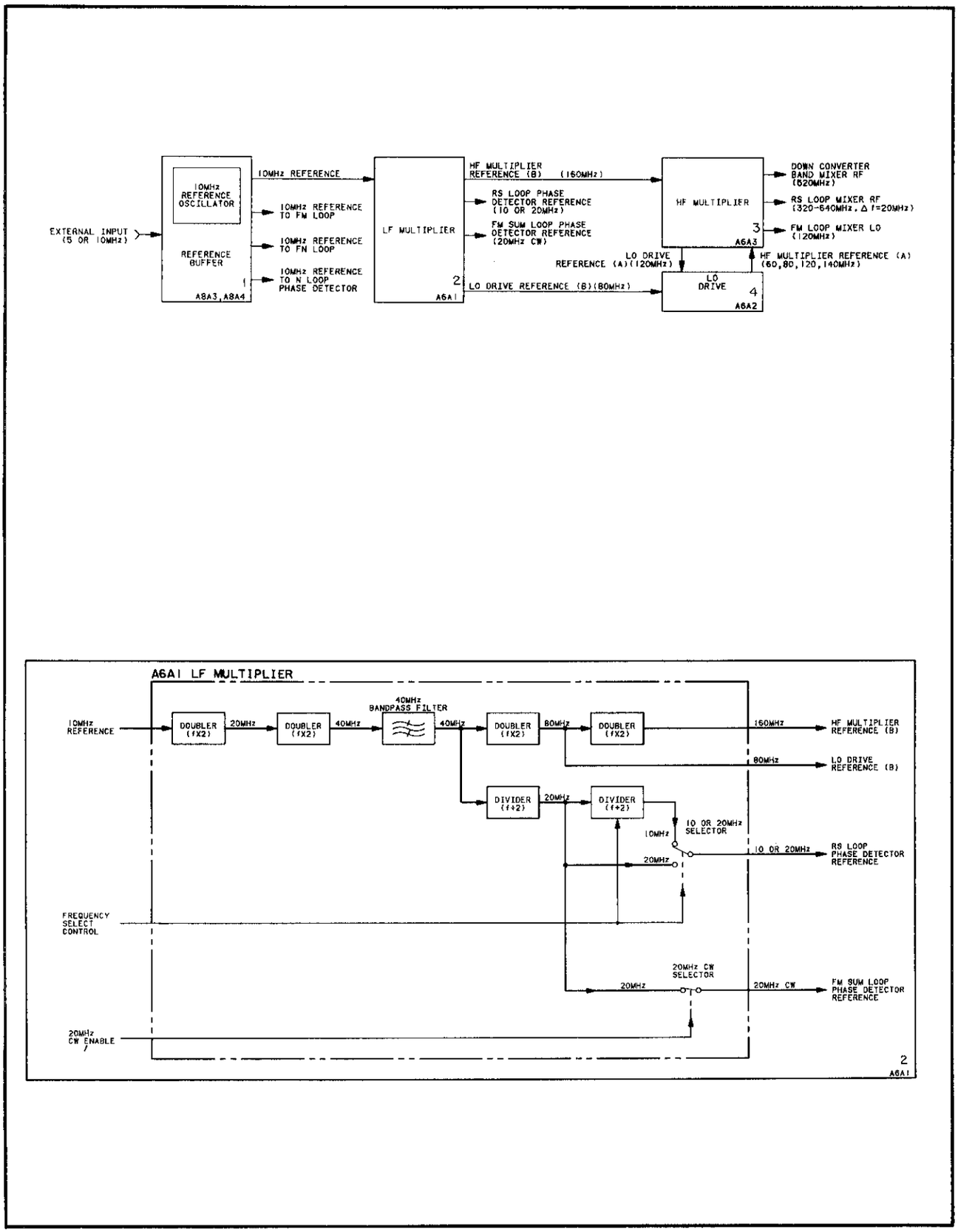


Figure 8-304. A6A1 Reference Section Low Frequency Multiplier Block Diagrams

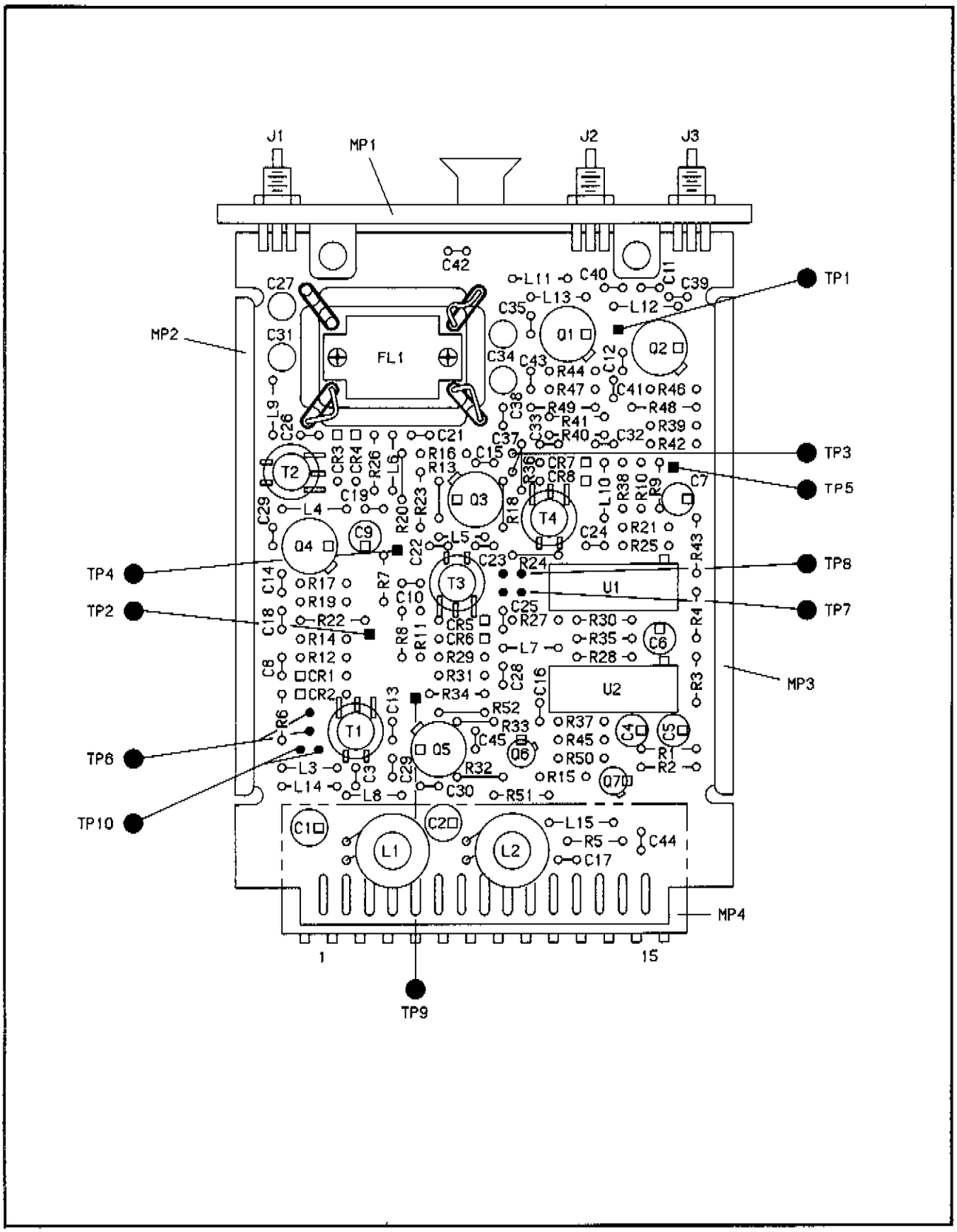
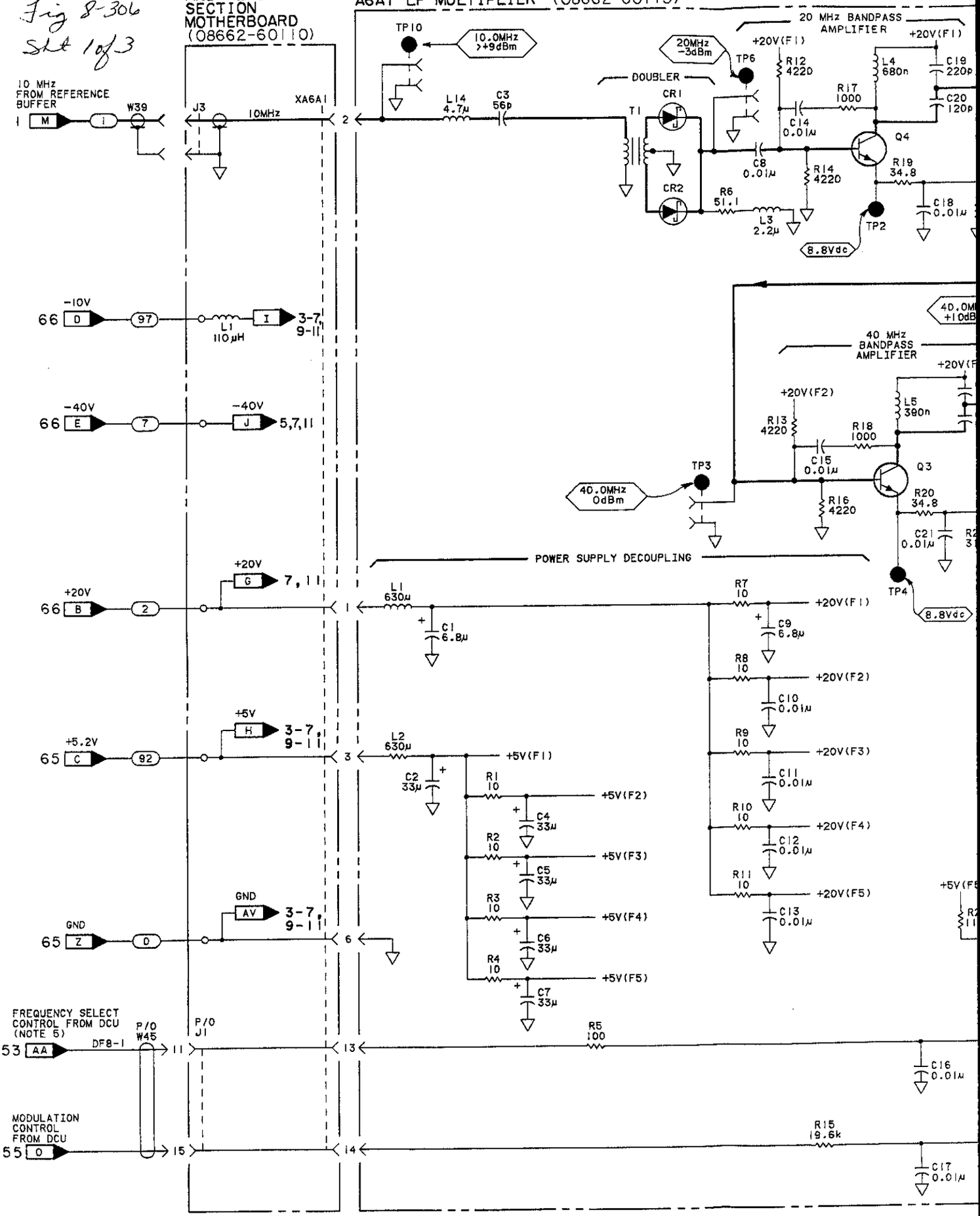


Figure 8-305. A6A1 Reference Section Low Frequency Multiplier Component Locator

Fig 8-306
Sht 1 of 3

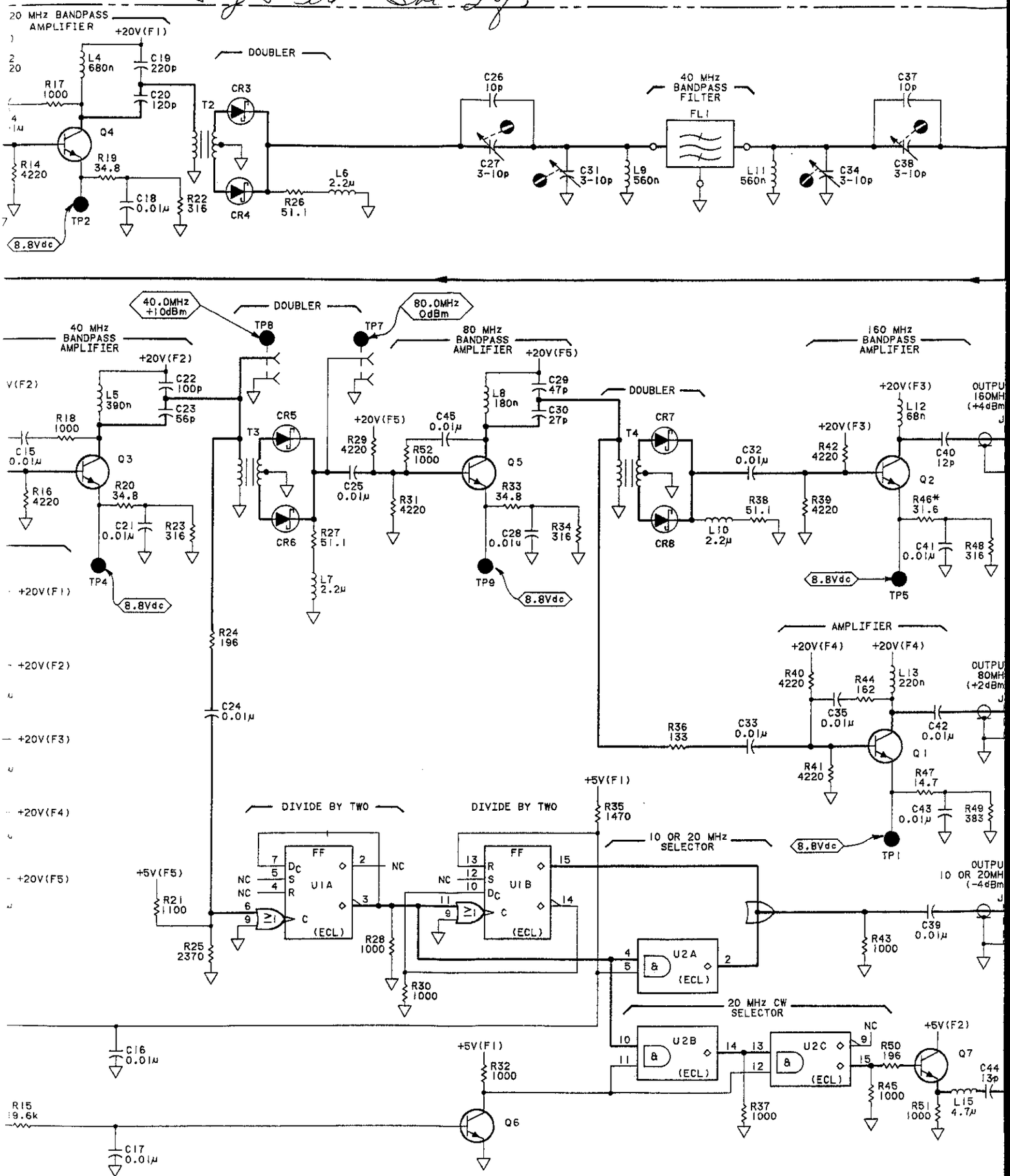
P/O A6A10
HF LOOPS
AND REFERENCE
SECTION
MOTHERBOARD
(08662-60110)

A6A1 LF MULTIPLIER (08662-60115)



SERIAL PREFIX: 2234A

Fig 8-304 Sht 2 of 3



NOTES:

1. REFER TO TABLE FOR 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENT MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. ASTERISK (*) INDICATES THAT THESE PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL ONLY. REFER TO SECTION V FOR PROCEDURE.
4. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NONSTANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS ≥ +4.0V; A LOW LEVEL IS ≤ 3.5V.
5. MNEMONIC DF8-1 REPRESENTS THE 8TH FREQUENCY DIGIT ON THE FRONT PANEL AND THE BCD WEIGHTING.

Fig 8-306
Sht 3 of 3

REFERENCE DESIGNATIONS

NO PREFIX	A6A10
W9,12,14 32,39,45	J1,3,4 XA6A1
A6A1	
C1-35,37-45 CR1-8 FL1 J1-3 L1-15 Q1-7 R1-52 T1-4 TP1-10 U1,2	

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1-5	1854-0247
Q6,7	1854-0071
U1	1820-0817
U2	1820-1400

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V(F5)-1 +5V(F4)-16 ▽ -8
U2	+5V(F3)-1 +5V(F2)-16 ▽ -8

A6A1U1,2 TOP VIEW

CIRCUIT BOARD TOP VIEW

LOGIC LEVELS

	ECL (NOTE 4)
HIGH	>+4.0V
LOW	<+3.5V
< IS MORE NEG. THAN	
> IS MORE POS. THAN	
OPEN	LOW
GROUND	LOW

OUTPUT 160MHz (+4dBm) J2
C40 12p
W12 972 N 3
HF MULTIPLIER REFERENCE(8) TO REFERENCE SECTION HF MULTIPLIER
R48 316

OUTPUT 80MHz (+2dBm) J1
C42 0.01µ
W14 971 F 4
LO DRIVE REFERENCE(8) TO REFERENCE SECTION LO DRIVE
R49 383

OUTPUT 10 OR 20MHz (-4dBm) J3
C39 .01µ
W9 973 A 7
10 OR 20 MHz REFERENCE TO RS LOOP PHASE DETECTOR

P/O A6A10
+5V(F2)
Q7
C44 13p
L15 4.7µ
XA6A1 15
20MHz CW (0.6Vpp)
20MHz OUTPUT J4
W32 94 K 25
20MHz(CW) REFERENCE TO FM SUM LOOP PHASE DETECTOR

SERVICE SHEET 2
A6A1

Figure 8-306. A6A1 Reference Section Low Frequency Multiplier Schematic

SERVICE SHEET 3
A6A3 HF MULTIPLIER ASSEMBLY

REFERENCE BLOCK DIAGRAM 2
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The HF Multiplier (A6A3) generates four separate signals from its two input signals. Three of the output signals are fixed in frequency, while the fourth output varies from 320 to 640 MHz in 20 MHz steps.

The two 120 MHz output signals, the LO Drive Reference A and the FM Loop Mixer LO, are generated by multiplying, heterodyning, and dividing the 160 MHz input signal, the HF Multiplier Reference (B). The 160 MHz input signal is first passed through a 160 MHz Band-Pass Filter. The 160 MHz filter, FL1, is a narrow band crystal filter. This filter contributes significantly to the Signal Generator's single sideband phase noise performance. After the 160 MHz Band-Pass Filter, the signal path splits into two paths. One signal path goes to the LO port of MIxer U10, and the other goes to the 160 MHz Band-Pass Amplifier and Doubler circuit. The Doubler is a full-wave rectifier circuit, consisting of a center-tapped transformer and two schottky diodes. The 320 MHz Band-Pass Amplifier amplifies the doubled frequency while attenuating the fundamental and the undesired higher harmonics. Limiter U7 provides a constant signal level to the RF port of Mixer U10. Mixer U10 heterodynes the 320 MHz signal with the 160 MHz input signal and the resulting sum, 480 MHz, is then amplified by the 480 MHz Band-Pass Amplifier. The 480 MHz Band-Pass Amplifier and the 480 MHz Band-Pass Filter attenuate the residual LO and RF signals and the undesired difference signal. The 480 MHz signal is divided by counter U9, to obtain the 120 MHz output signal. U9 is an ECL device and has complimentary outputs. The two 120 MHz output signals from U9 are then amplified by the 120 MHz Band-Pass Amplifiers which remove the unwanted harmonics from the 120 MHz square wave outputs.

The 520 MHz output signal is generated by doubling the 320 MHz signal from the collector of Q5 and heterodyning the doubled signal (640 MHz) with the 120 MHz signal from U9. Mixer U1 is a double balanced mixer. The 520 MHz Switch and Band-Pass Amplifier can be turned off by cutting off the emitter current to Q1. The amplifier is tuned to amplify the difference signal and filter the sum signal and the residual input signals (LO and RF).

The 320 to 640 MHz (delta [f]=20 MHz) output is generated by heterodyning various combinations of input signals. Mixer U4 is a double balanced mixer (same as U1 and U10) but instead of normally feeding the two input signals into the RF and LO ports, one input signal is applied to the mixer's IF port and the output is taken at the mixer's RF port, In this configuration the mixer acts as a current-controlled switch (normal mixing action is disabled) when a dc current is applied to the mixer's IF port. That is, if a dc control current is applied to the IF port, the signal at the LO port is allowed to pass straight through to the RF port. The input signals to the IF port come from the LO drive (60, 80, 120, and 140 MHz) and the Controller (which supplies the dc control current to disable the mixer). The input signals to the LO port are derived from the HP multiplier Reference (B)(320, 480, and 640 MHz). The 3 to 1 Multiplexer circuit, which is comprised of four limiters (U2, U3, U6, and U8), directs one of the three signals to the LO port. Limiters U2, U6, and U8 can be switched on and off by controlling the bias current flowing into the limiters (via pin 3 of the limiters). The voltage at pin 3 is about -10 Vdc when the limiters are enabled.

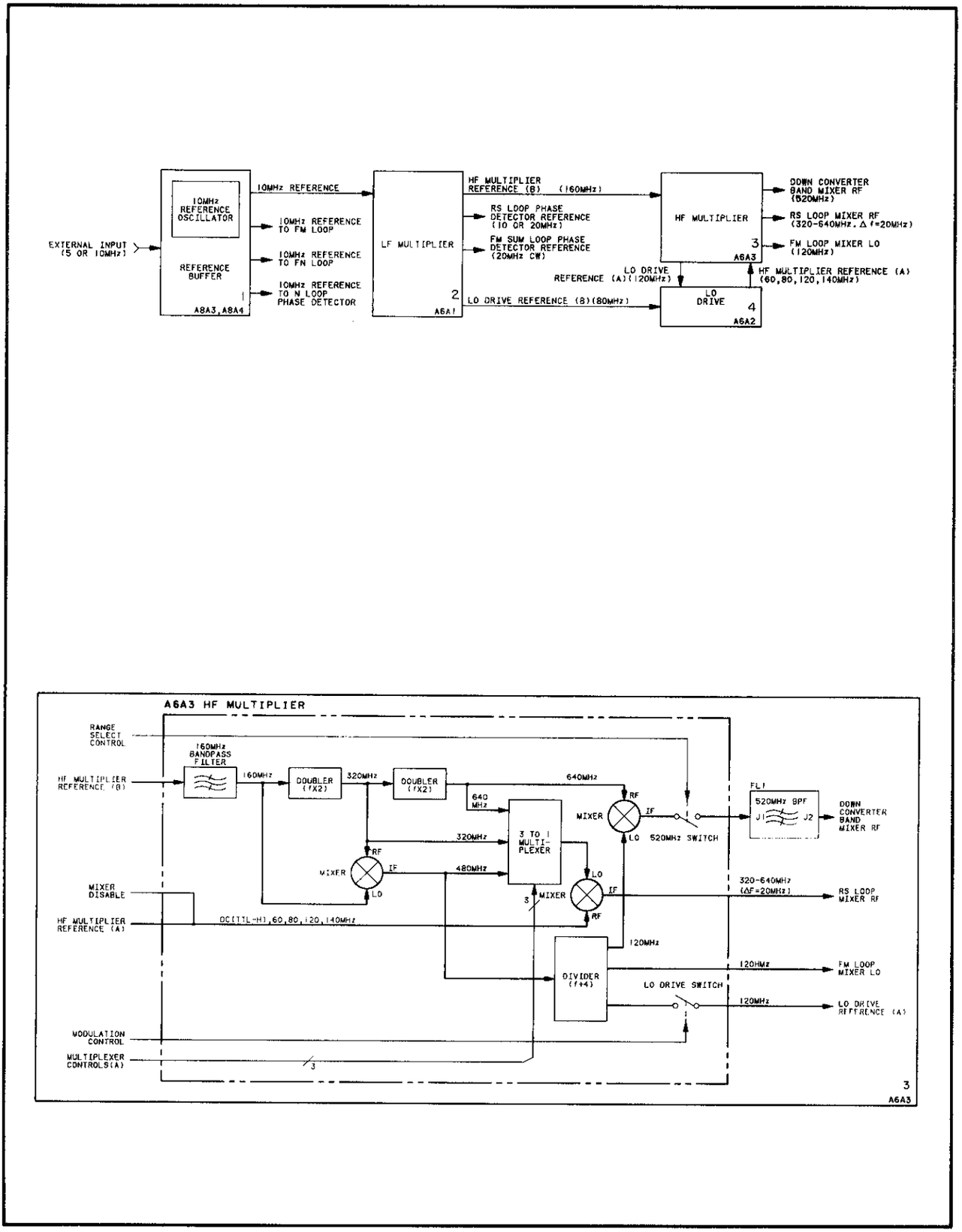


Figure 8-307. A6A3 Reference Section High Frequency Multiplier Block Diagrams

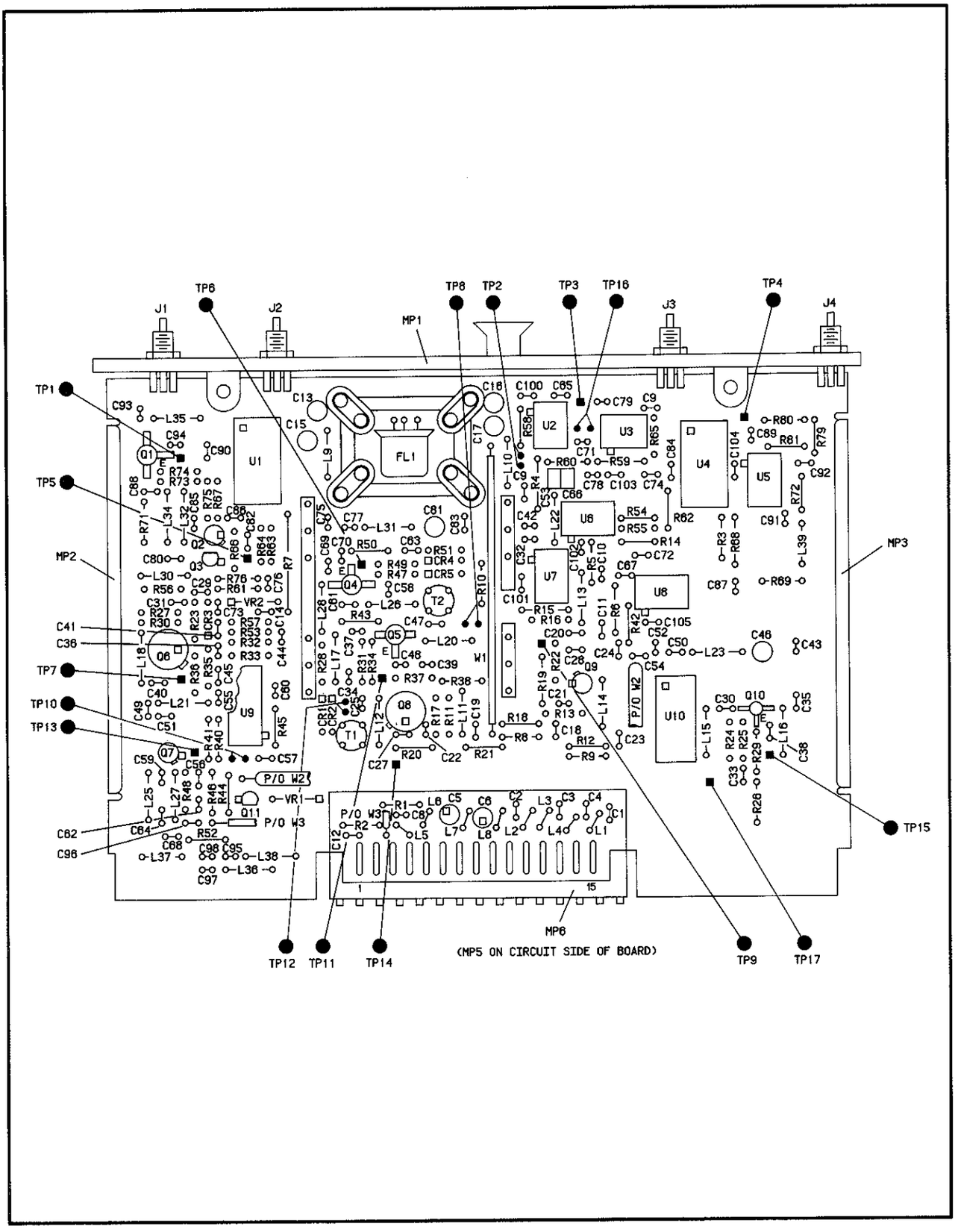


Figure 8-308. A6A3 Reference Section High Frequency Multiplier Component Locator

CHANGES

2333A and Above

On the A6A3 component locator:

- A6A3R81-R83, C99 - Modify the component locator as shown in the partial component locator "P/O Figure 8-308. A6A3 Reference Section High Frequency Multiplier Component Locator (2333A)" on page 8-316.3

On the A6A3 schematic:

- A6A3R81-R83, C99 - Modify the schematic as shown in the partial schematic "P/O Figure 8-309. A6A3 Reference Section HF Multiplier Schematic" on page 8-316.3
- A6A3C38 - Change the value of C38 to 100p.
- Down Converter Band Mixer RF to Output Section (+1 dBm ±.75 dB) Bullet "O" - On the right side of the page, find bullet "O". Change the label of this bullet to read, "Down Converter Band Mixer RF to Output Section (-1 dBm ±0.75 dB)"

2408A and Above

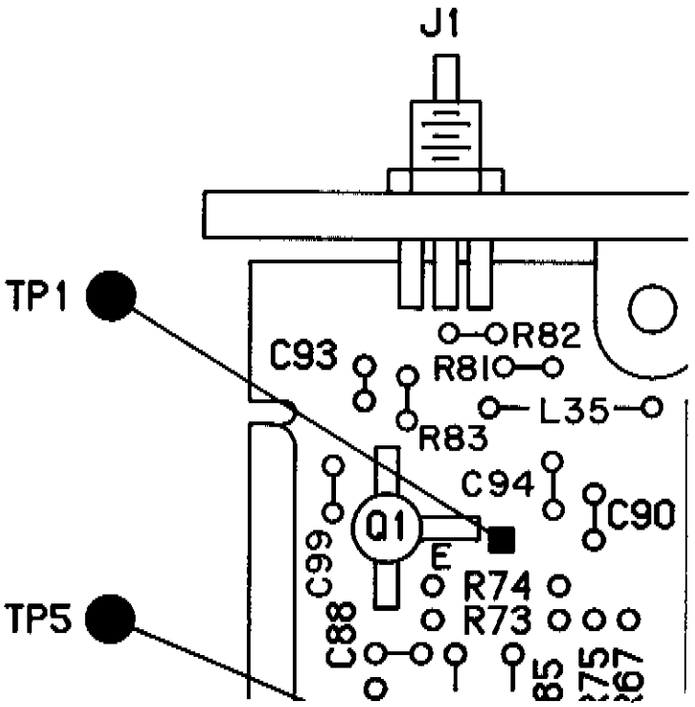
On the A6A3 schematic:

- AT2, J5, J15, TP2, W93, A6A3R84* - Modify the schematic as shown in the partial schematic "P/O Figure 8-309. A6A3 Reference Section High Frequency Multiplier Schematic (2408A)" on page 8-316.4

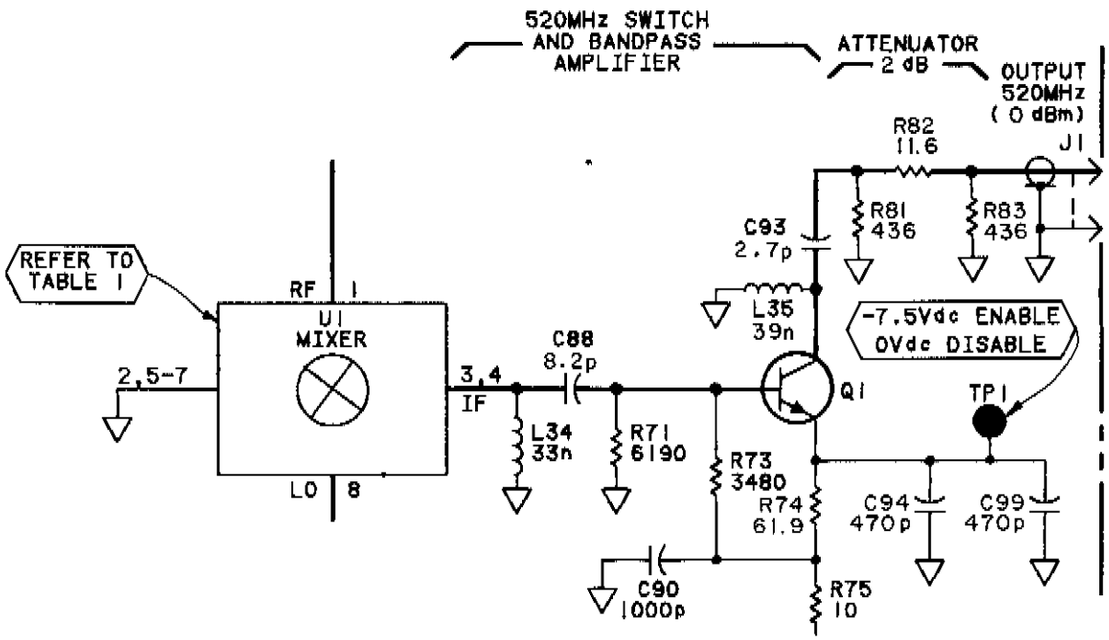
2449A and Above

On the schematic:

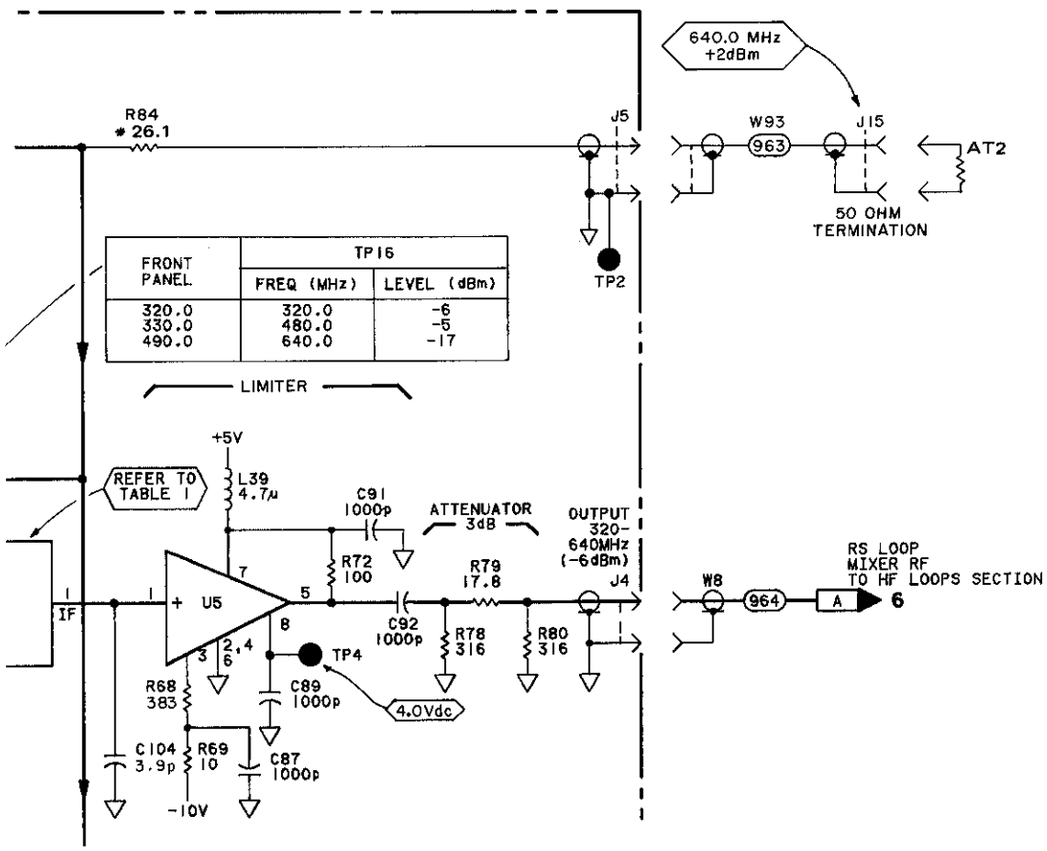
- W93 - W93 was added on serial prefix 2408A. Refer to the partial schematic "P/O Figure 8-309. A6A3 Reference Section High Frequency Multiplier Schematic (2408A)" on page 8-316.4. Change the color code of W93 to "3".



P/O Figure 8–308. *A6A3 Reference Section HF Multiplier Component Locations (2333A)*



P/O Figure 8–309. *A6A3 Reference Section HF Multiplier Schematic (2333A)*



P/O Figure 8–309. *A6A3 Reference Section High Frequency Multiplier Schematic (2408A)*

Fig 8-309
Sht 1 of 5

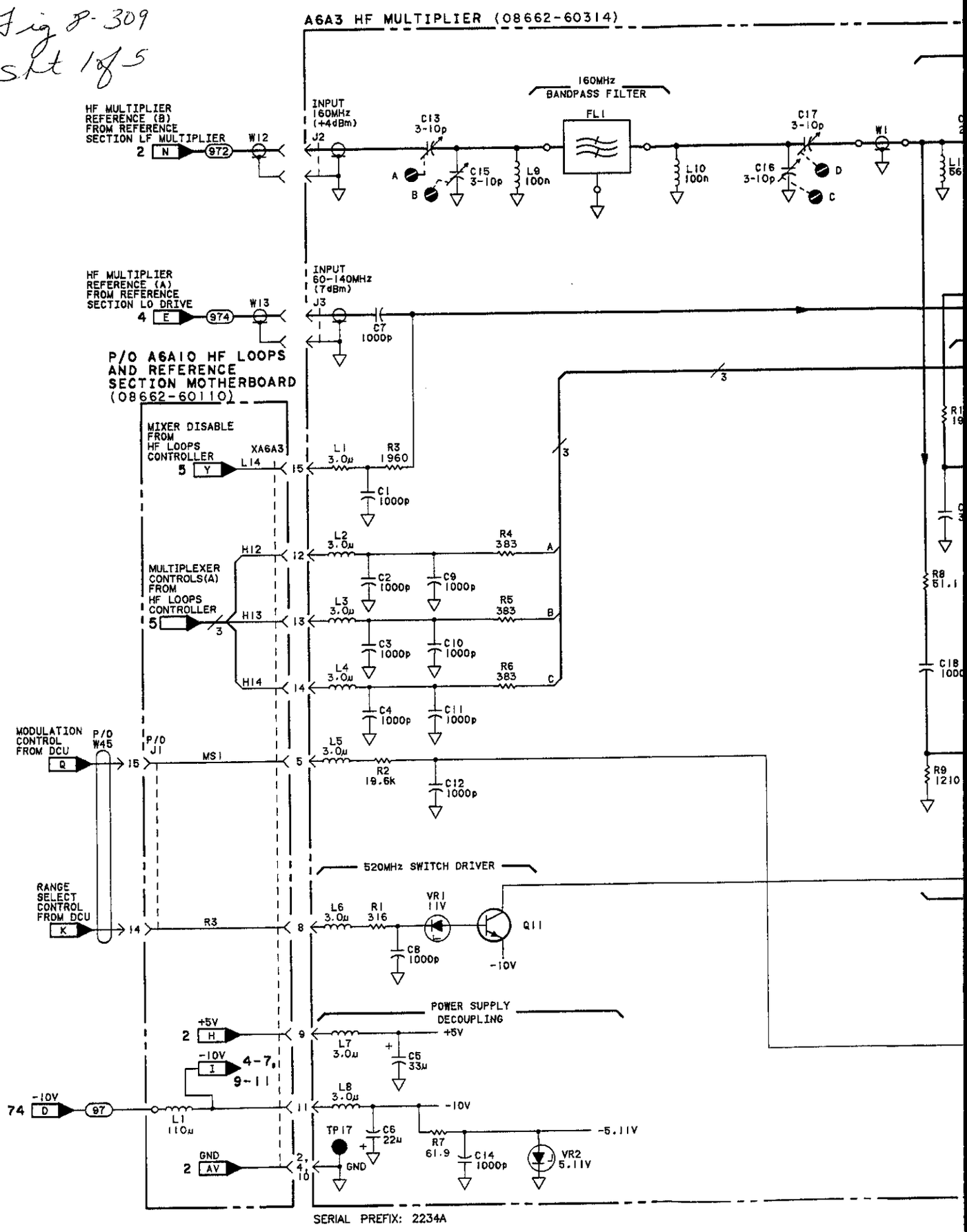


Fig 8-309 Sht 2 of 5

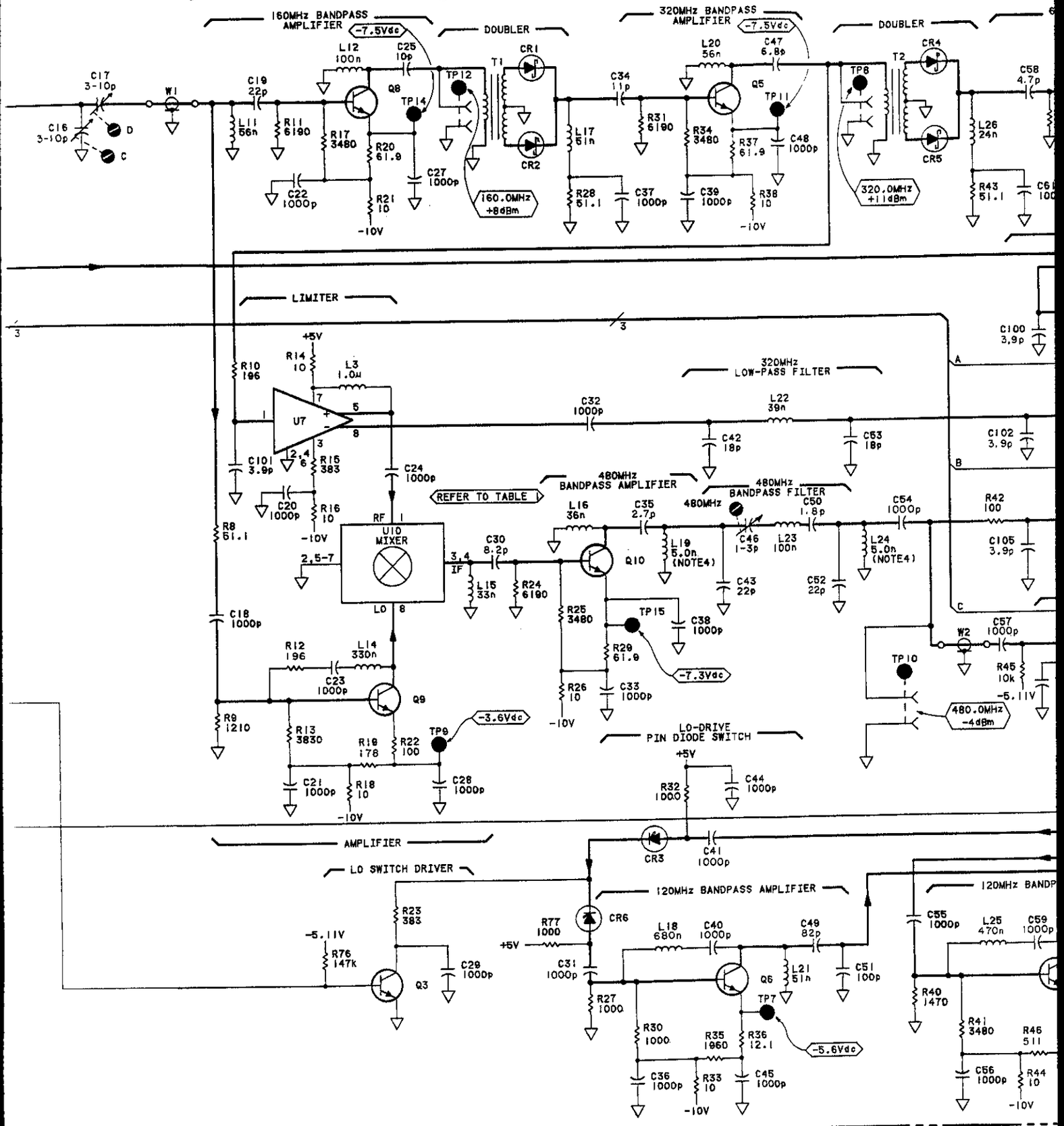


Fig 8-309 Sht 3 of 5

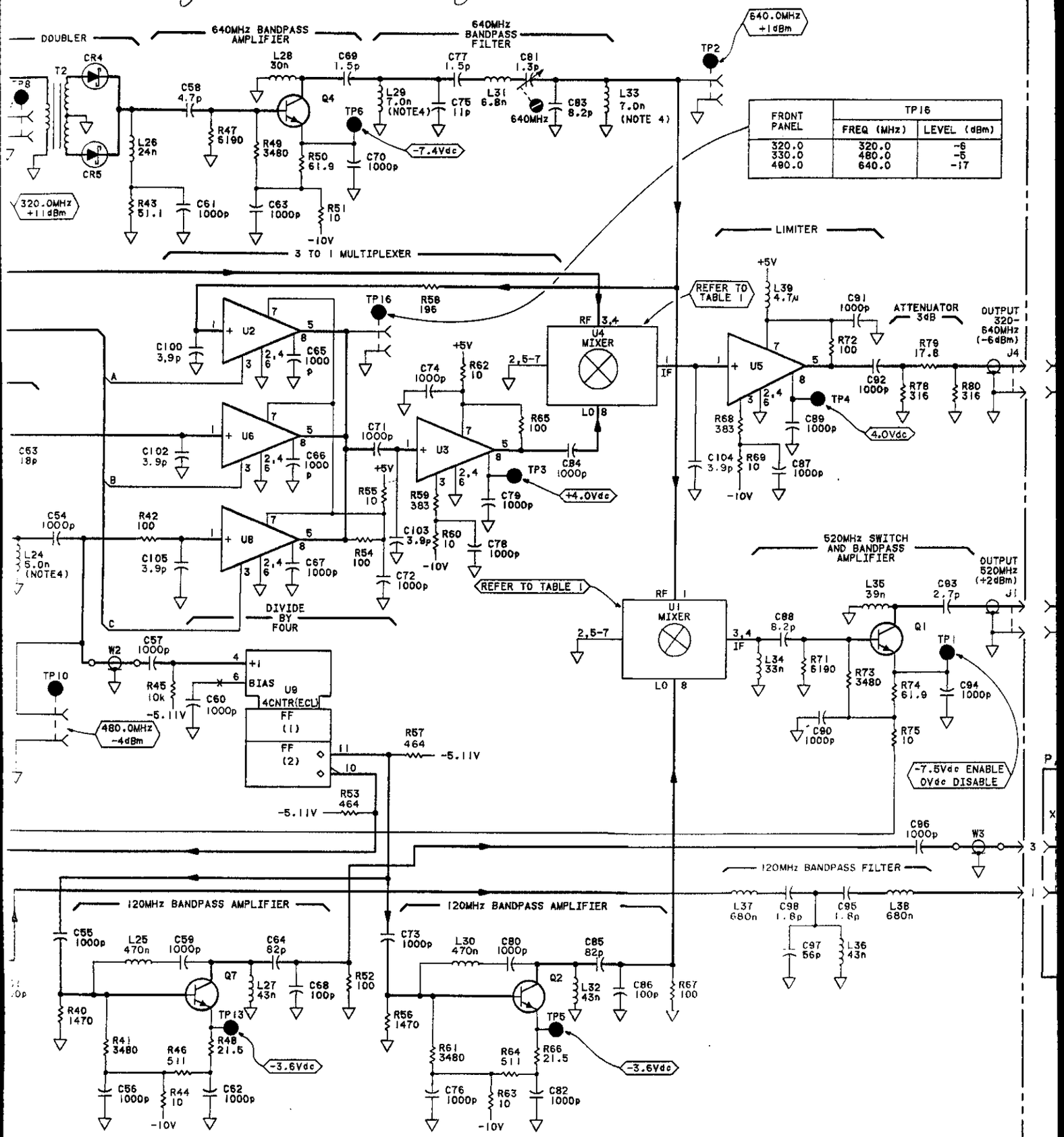


Fig 8-309
Sht 4 of 5

MIXER	ADAPTER[1]	
	TOP CONNECTOR	BOTTOM CONNECTOR
U1	640.0MHz @ +7dBm	120.0MHz @ -7dBm
U10	320.0MHz @ +4dBm	160.0MHz @ -4dBm
U4[2]	NOT USED	320.0(320.0) 480.0(330.0) 640.0(490.0) @ 0dBm

TABLE 1. MIXER CHECK

1. MIXER LEVELS WITH MIXER REMOVED AND 08662-60196 ADAPTER INSTALLED.
2. FREQUENCY DEPENDS ON FRONT PANEL FREQUENCY SETTING. SETTINGS IN PARENTHESIS WILL PRODUCE ALL THREE POSSIBLE OUTPUT FREQUENCIES.

CAUTION

RF TESTPOINTS (PC BOARD CUP CONNECTORS)MUST BE AC COUPLED TO TEST EQUIPMENT. OTHERWISE DAMAGE MAY OCCUR TO THE TEST EQUIPMENT OR THE CIRCUIT UNDER TEST. USE THE SPECIAL CAPACITOR-COUPLED CABLE ADAPTOR FOUND IN THE SERVICE KIT.

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENT MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NON-STANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS ≥ +4.0V; A LOW LEVEL IS ≤ +3.5V.
4. INDUCTORS L19,24,29 AND 33 ARE ETCHED TRACE INDUCTORS.

	TP16	
ONT NEL	FREQ (MHz)	LEVEL (dBm)
20.0	320.0	-6
30.0	480.0	-5
30.0	640.0	-17

REFERENCE DESIGNATIONS

NO PREFIX	A6A3 CONT
FL1 W8,11-13, 18,31,45	C1-11 R1-38,40- 69,71-80 T1,2 TP1-17 U1-10 VR1,2 W1-3
A6A3	
C1-25,27- 98,100-105 CR1-6 FL1 J1-4 L1-39	A6A10 J1,2 L1 XA6A3

LOGIC LEVELS

	ECL (NOTE 3)
HIGH	>+4.0V
LOW	<+3.5V
<IS MORE NEG. THAN	
>IS MORE POS. THAN	
OPEN	LOW
GROUND	HIGH

A6A3U2,3,5 TOP VIEW

A6A3U9 TOP VIEW

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U9	-5.11V -7 -14 NC-1,2,3, 5,8,9, 12,13

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,4,5,10	1854-0720
Q2,7,9	1854-0610
Q3,11	1854-0071
Q6,8	1854-0247
U1,4	0955-0096
U2,3,5-8	1826-0372
U9	1820-2140
U10	0955-0095

A6A3Q1,4,5,10 TOP VIEW

A6A3U2,3,5-8

A6A3U1,4,10 MIXER BOTTOM VIEW

BLUE BEAD

IMITER

C91 1000p ATTENUATOR 3dB OUTPUT 320-640MHz (-6dBm) J4
R72 100 R79 17.8
C92 1000p R78 316 R80 316
TP4 4.0Vdc
C89 1000p
C87 1000p

W8 964 A 6 RS LOOP MIXER RF TO HF LOOPS SECTION

520MHz SWITCH AND BANDPASS AMPLIFIER
OUTPUT 520MHz (+2dBm) J1
L35 39n C93 2.7p
Q1
TP1
R71 6190 R73 3480 R74 61.8 C94 1000p
C90 1000p R75 10
-7.5Vdc ENABLE 0Vdc DISABLE

W11 975

FL1 520MHz BPF
A B C D J1 J2

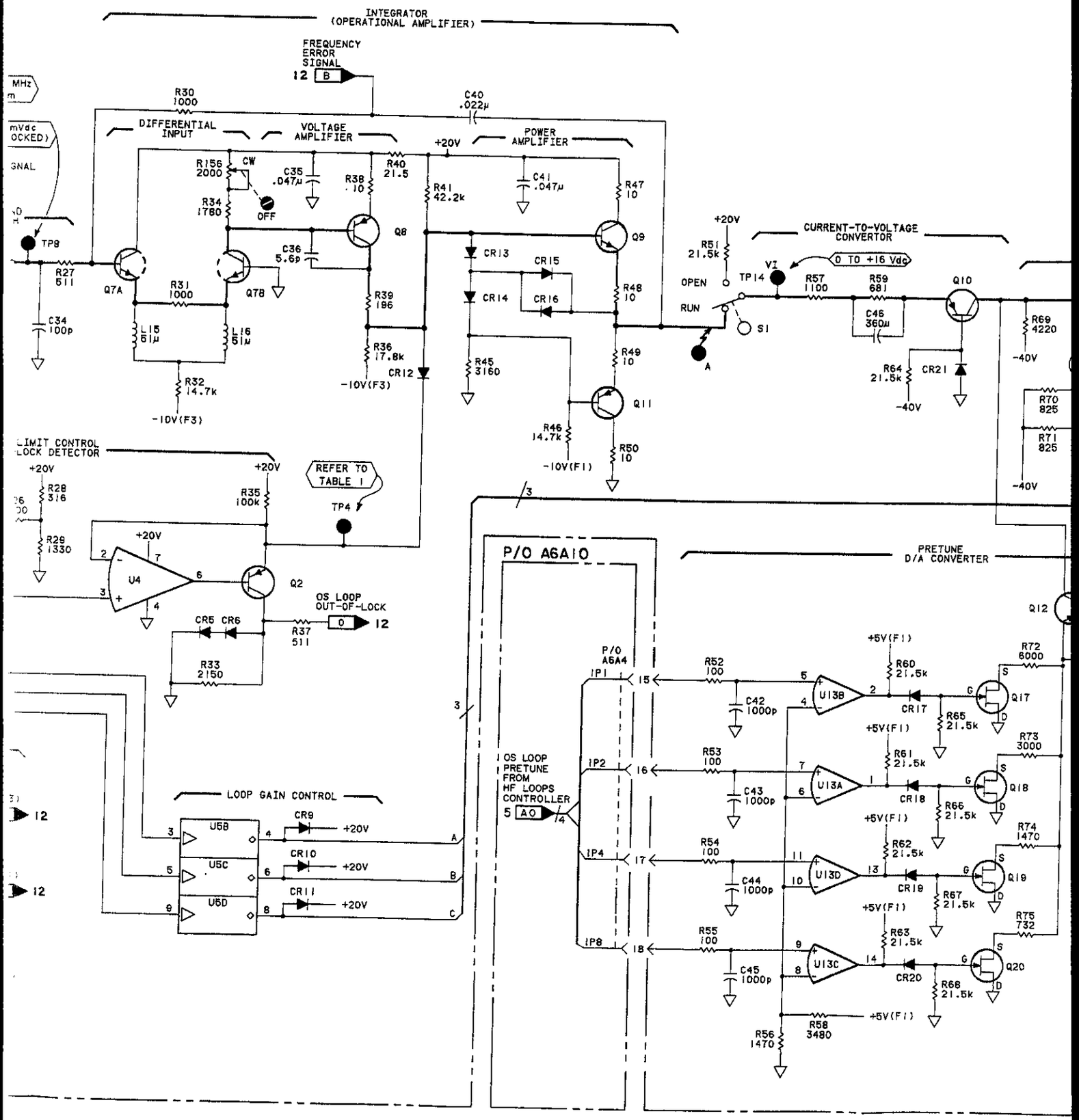
W18 937 0 29 DOWN CONVERTER BAND MIXER RF TO OUTPUT SECTION (+10dBm±.75dB)

P/O A6A10
XA6A3
120MHz (+4dBm) B 4 LO DRIVE REFERENCE (A) TO REFERENCE SECTION LO DRIVE
120MHz (+10dBm) J2

C96 1000p W3
BANDPASS FILTER
C95 1.8p L38 680n
C97 56p L36 43n

W31 91 C FM LOOP MIXER LO TO MODULATION SECTION

Fig 8-333 Sht 2 of 5



SERVICE SHEET 4
A6A2 LO DRIVE ASSEMBLY

REFERENCE BLOCK DIAGRAM 4
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The LO Drive (A6A2) provides an output signal at either 60 MHz, 80 MHz, 120 MHz, or 140 MHz to the HF Multiplier (A6A3). A 4 to 1 multiplexer circuit is used to select one of the four frequencies. The primary inputs are the 80 MHz signal (LO Drive Reference (B)), and the 120 MHz signal (LO Drive Reference (A)). When either the 80 MHz or 120 MHz output frequency is selected the corresponding input signal is routed to the output jack, J2. The 60 MHz output is derived by dividing the 120 MHz input by two. For an output of 140 MHz, the 60 MHz signal and 80 MHz signal are mixed together.

Mixer

Mixer U3 is a double balanced type which suppresses the input signals. The Mixer heterodynes the 60 MHz signals and 80 MHz signals to produce the 140 MHz signal (sum product). The difference signal and the residual input signal are attenuated by the 140 MHz Band-Pass Filter, leaving only the desired 140 MHz signal.

4 to 1 Multiplexer

The 4 to 1 Multiplexer consists of PIN diodes CR1 through CR8. PIN diodes act as current conrolled resistors at RF frequencies. The Multiplexer Control, U2, supplies the control bias for the PIN diodes. The control bias is either switched on or off, hence, the PIN diodes act as RF switches. When the PIN diodes are forward biased the RF resistance is reduced, allowing the RF signal to pass. When the PIN diodes are reverse biased they offer high resistance to the RF signal.

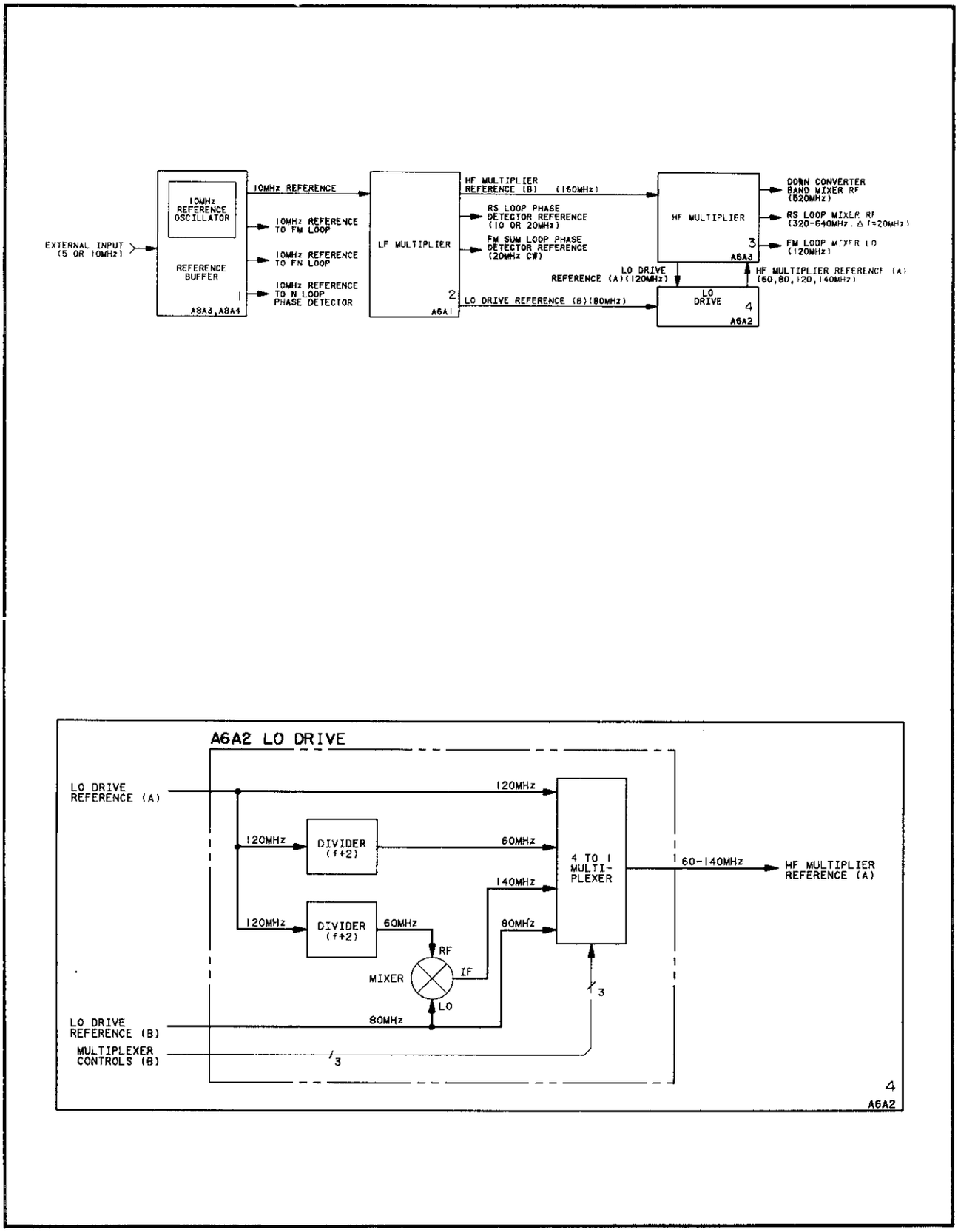


Figure 8-310. A6A2 Reference Section LO Drive Block Diagrams

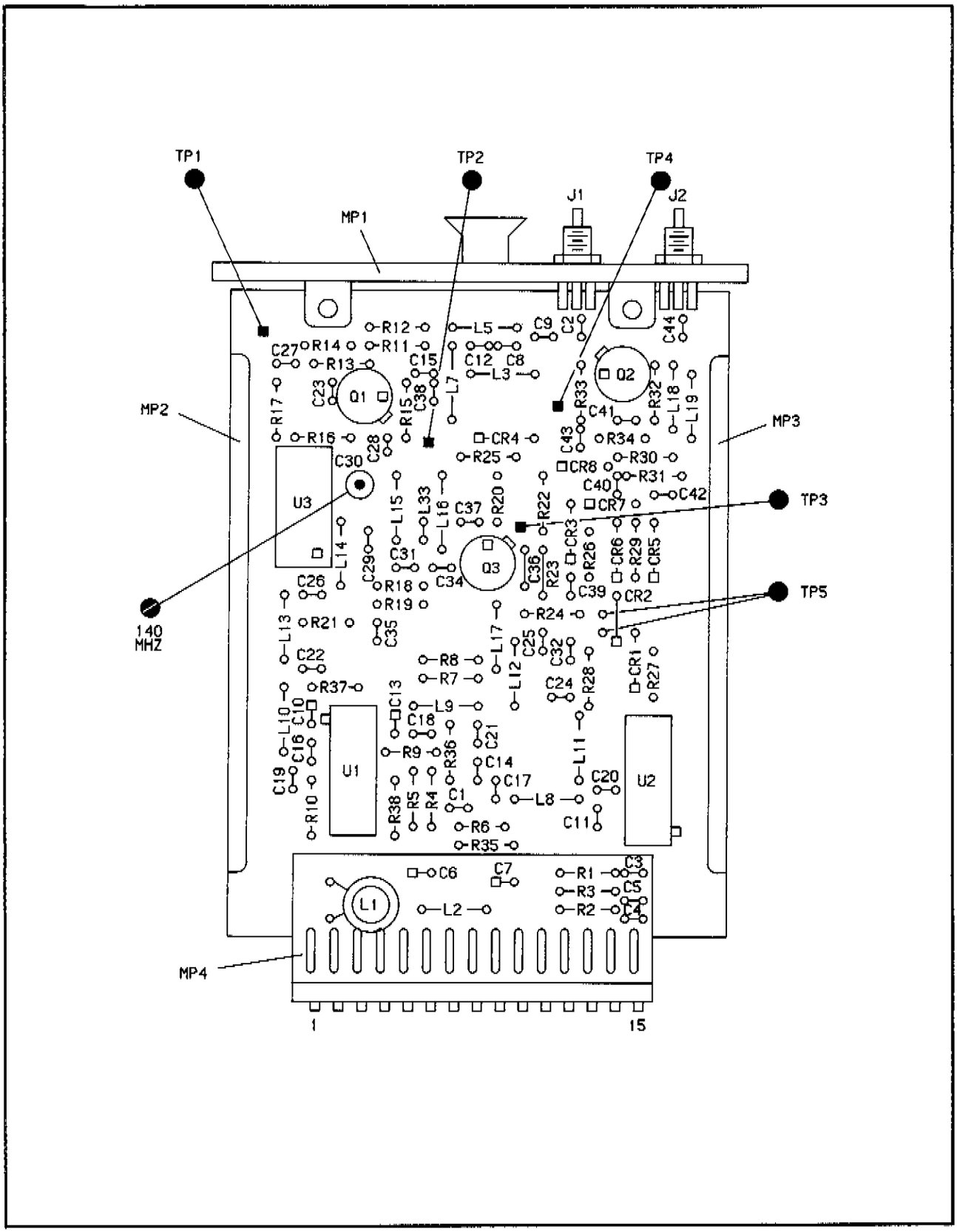


Figure 8-311. A6A2 Reference Section LO Drive Component Locator

Fig 8-312 Sht 1 of 4

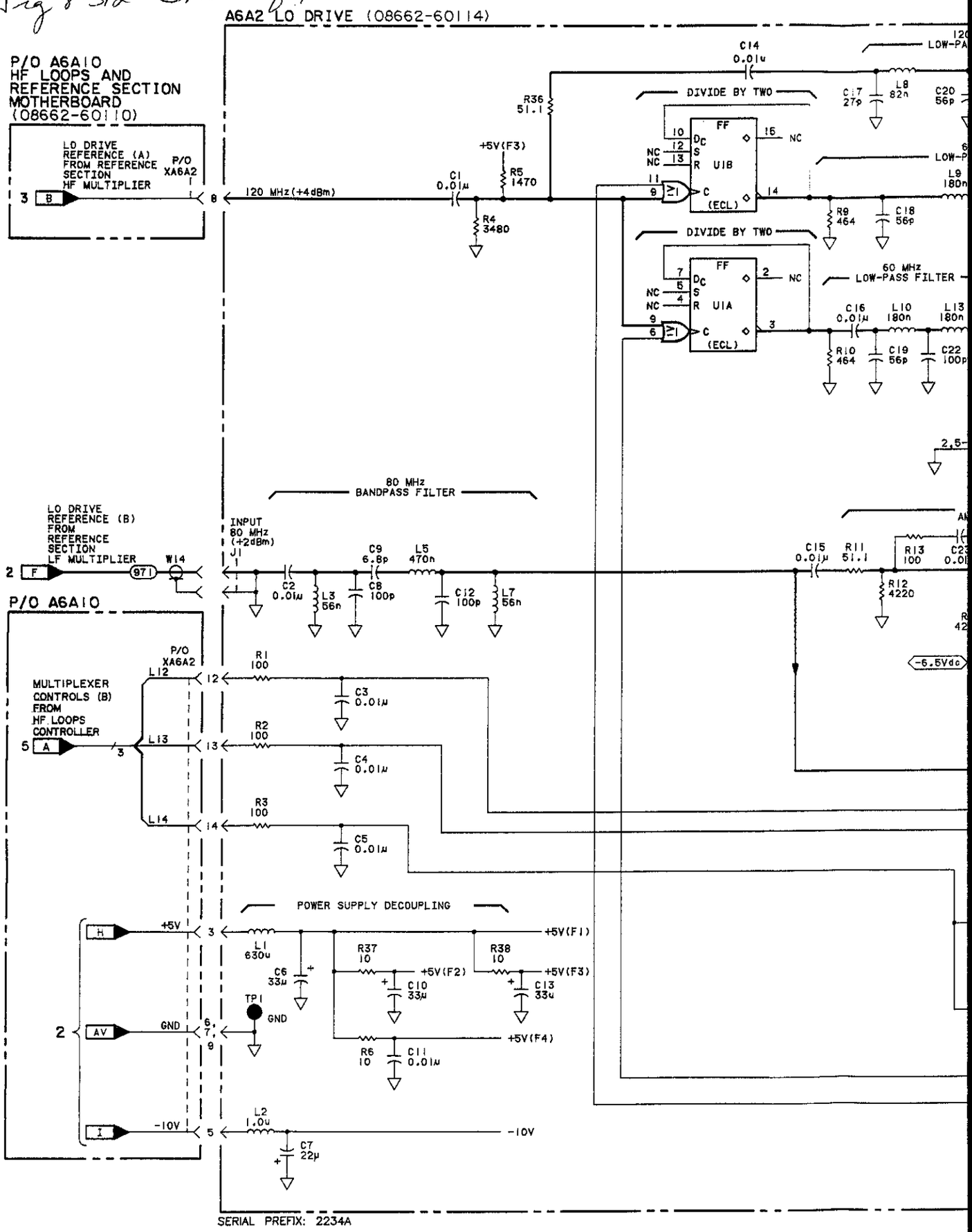


Fig 8-312 Sht 2 of 4

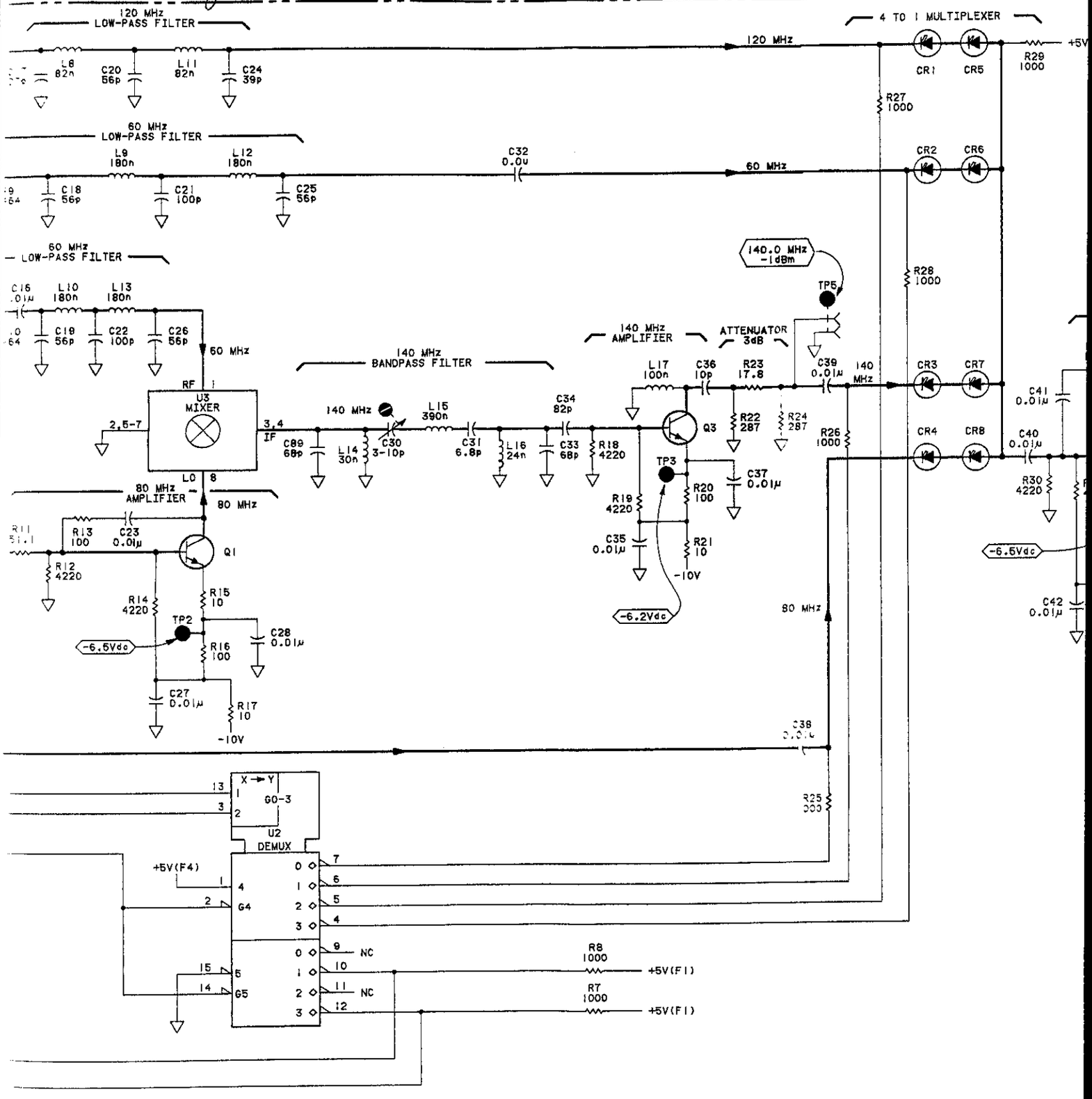
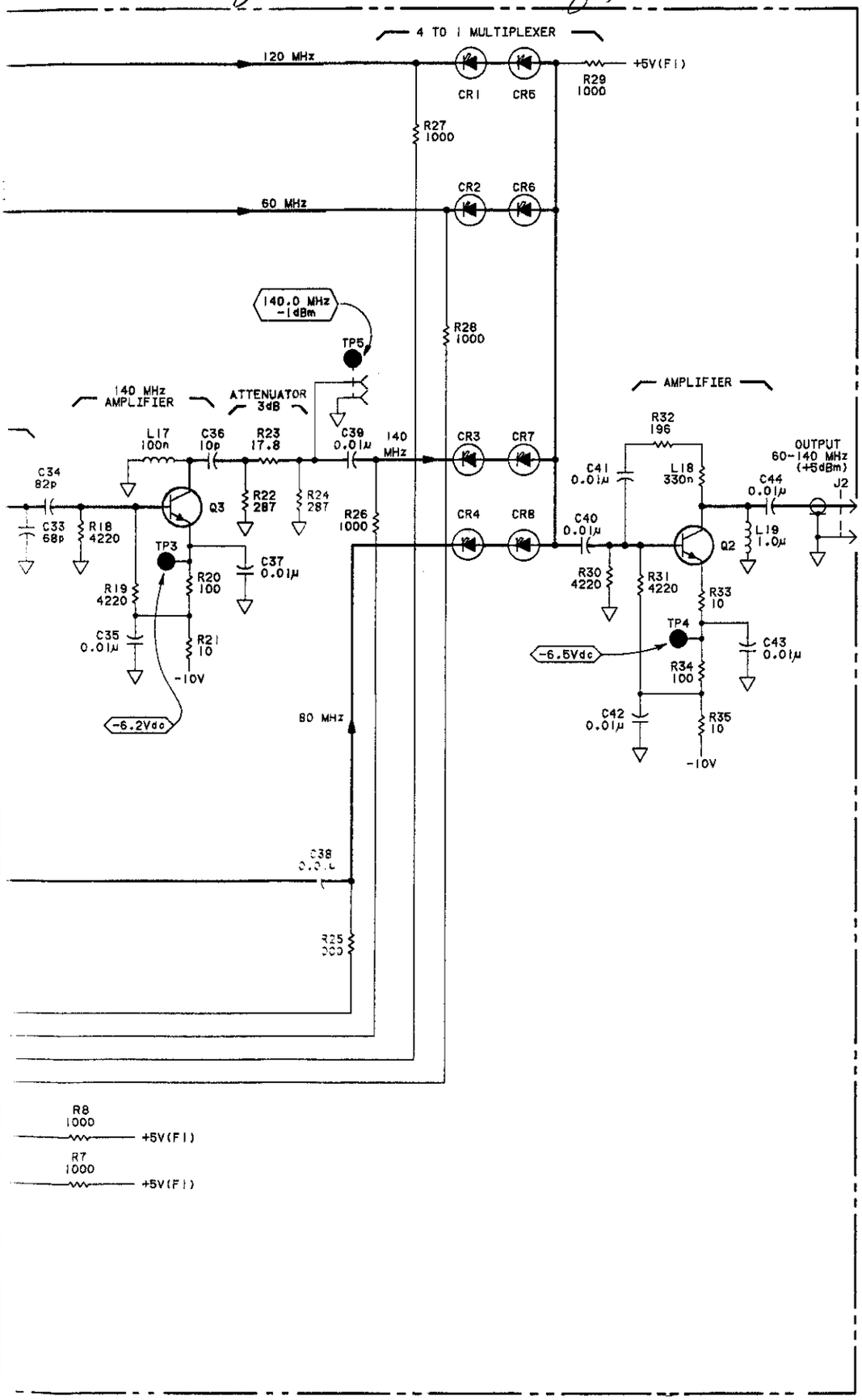


Fig 8-312 sht 3 of 4



CAUTION

RF TEST POINTS (PC BOARD CUP CONNECTORS) MUS
AC COUPLED TO TEST EQUIPMENT. OTHERWISE DAMA
OCCUR TO THE TEST EQUIPMENT OR THE CIRCUIT U
TEST. USE THE SPECIAL CAPACITOR-COUPLED CABL
ADAPTER FOUND IN THE SERVICE KIT.

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRA
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY
ACTUAL MEASURED VALUES. YOUR MEASUREMENT
BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. LOGIC LEVELS FOR ECL DEVICES IN THIS INST
"NONSTANDARD" DUE TO THE SUPPLY VOLTAGE US
LEVEL IS ≥+4.0V; A LOW LEVEL IS ≤+3.5V.

REFERENCE DESIGNATI

NO PREFIX	A6A
W13,14	XA6A2
A6A2	
C1-44	
CR1-8	
J1,2	
L1-3,5,7-10	
Q1-3	
R1-38	
TP1-5	
U1-3	

HF MULTIPLIER REFERENCE (A) TO REFERENCE SECTION HF MULTIPLIER

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

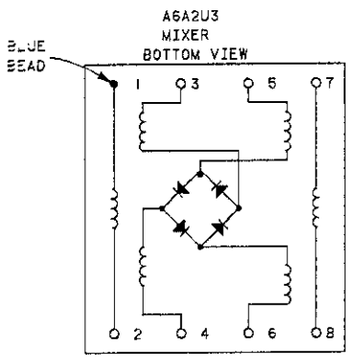
REFERENCE DESIGNATIONS	PART NUMBERS
Q1-3	1854-0247
U1	1820-0817
U2	1820-1046
U3	0955-0096

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V(F2)-1
	+5V(F3)-16
	▽ -8
U2	+5V(F4)-16
	▽ -8

LOGIC LEVELS

	TTL	ECL (NOTE 3)
HIGH	>+2V	>+4.0V
LOW	<+0.8V	<+3.5V
< IS MORE NEG. THAN		
> IS MORE POS. THAN		
OPEN	HIGH	LOW
GROUND	LOW	LOW



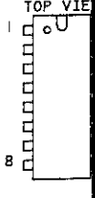


Fig 8-312
Sht 4 of 4

CAUTION

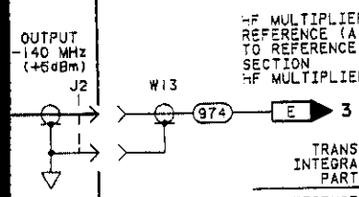
RF TEST POINTS (PC BOARD CUP CONNECTORS) MUST BE AC COUPLED TO TEST EQUIPMENT. OTHERWISE DAMAGE MAY OCCUR TO THE TEST EQUIPMENT OR THE CIRCUIT UNDER TEST. USE THE SPECIAL CAPACITOR-COUPLED CABLE ADAPTER FOUND IN THE SERVICE KIT.

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE MAY ACTUAL MEASURED VALUES. YOUR MEASUREMENT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE "NONSTANDARD" DUE TO THE SUPPLY VOLTAGE USED, A HIGH LEVEL IS ≥+4.0V; A LOW LEVEL IS ≤+3.5V.

REFERENCE DESIGNATIONS

NO PREFIX	A6A10
W13,14	XA6A2
A6A2	
C1-44	
CR1-8	
J1,2	
L1-3,5,7-10	
Q1-3	
R1-38	
TP1-5	
U1-3	



TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

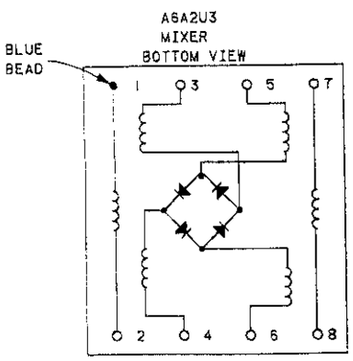
REFERENCE DESIGNATIONS	PART NUMBERS
Q1-3	1854-0247
U1	1820-0817
U2	1820-1046
U3	0955-0096

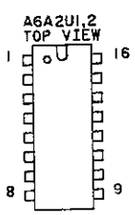
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

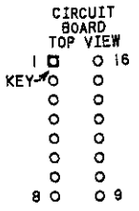
REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V(F2)-1 +5V(F3)-16 ▽ -8
U2	+5V(F4)-16 ▽ -8

LOGIC LEVELS

	TTL	ECL (NOTE 3)
HIGH	>+2V	>+4.0V
LOW	<+0.8V	<+3.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	LOW
GROUND	LOW	LOW







SERVICE SHEET 4

A6A2

Figure 8-312. A6A2 Reference Section LO Drive Schematic

SERVICE SHEET 5
A6A9 HF LOOPS AND REFERENCE SECTION CONTROLLER ASSEMBLY

REFERENCE BLOCK DIAGRAM 3
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The ROMs on this board contain factory generated pre-tune and fine-tune information that provides precise control over loop gain, loop lock limits, high frequency switching, and VCO frequency in the high frequency section. BCD lines carrying information which corresponds to front panel digits DF7, DF8, and DF9 provide addressing for the ROMs on this board.

Reference Sum (RS) and Output Sum (OS) Loop Inductor Switch Drivers

When a pair of inductor switch drivers is stimulated by a HI output from its respective ROM, the first transistor (for example, Q1) is turned OFF, turning Q2 ON to pull the inductor line to -30 volts. this shuts OFF the inductor being controlled. When the ROM output goes LO, Q1 is turned ON. This turns Q2 OFF. When Q2 turns OFF, current flows through the PIN diode in the VCO, turning the inductor ON.

All of the inductor driver circuits work in the same manner, except that different transistors are used for different current drive capabilities. The currents are: a, 15mA; b, 30mA; c, 30mA; d, 60mA; and e,120mA.

TROUBLESHOOTING

The output of the ROMs (U1, U2, and U3) can be checked using Signature Analysis. Service sheet B1 contains operating instructions. The frequency data inputs (DB7-1 through DF9-2) are related to the front panel frequency display as explained in Note 1 on the schematic.

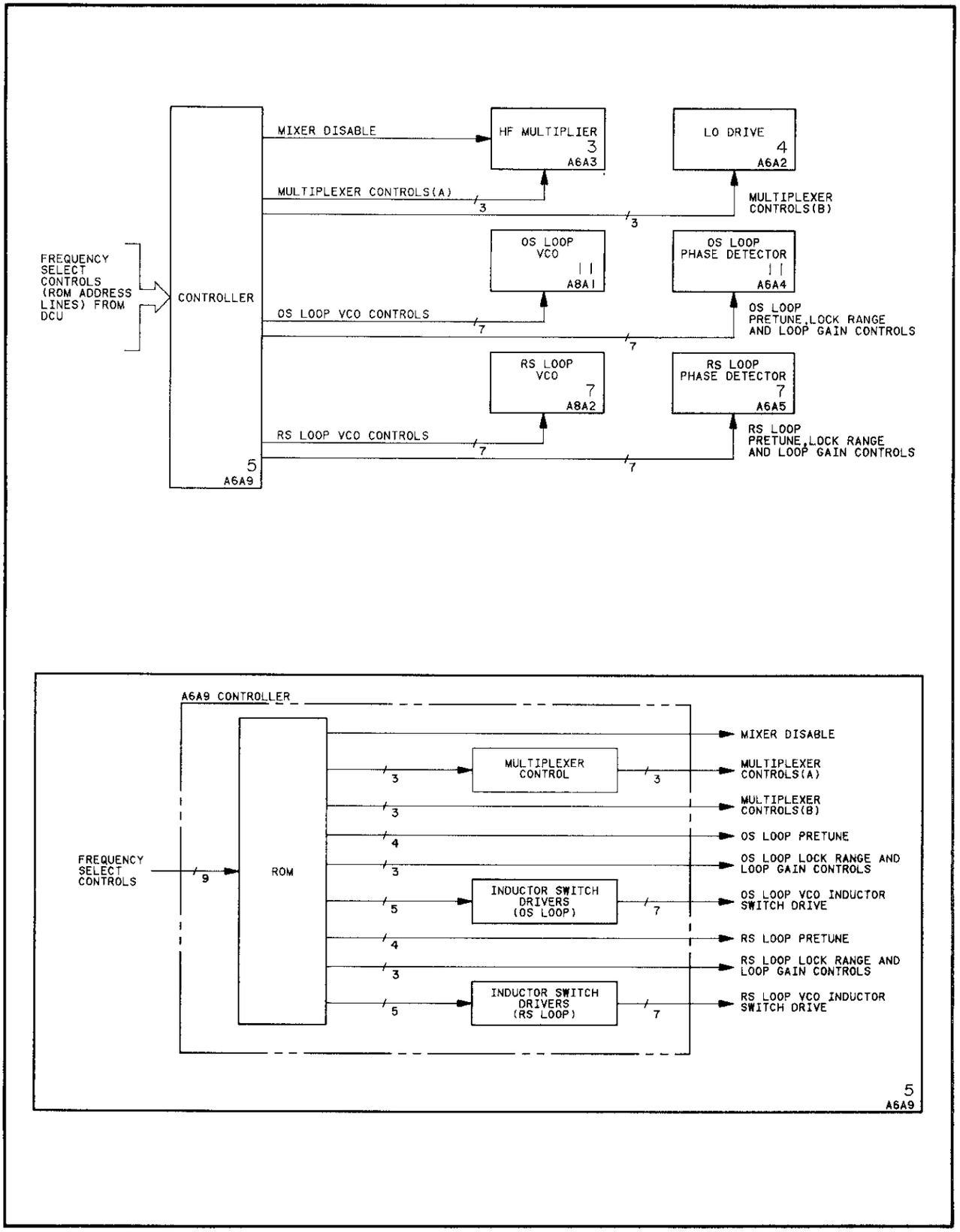


Figure 8-313. A6A9 Reference and High Frequency Loops Sections Controller Block Diagrams

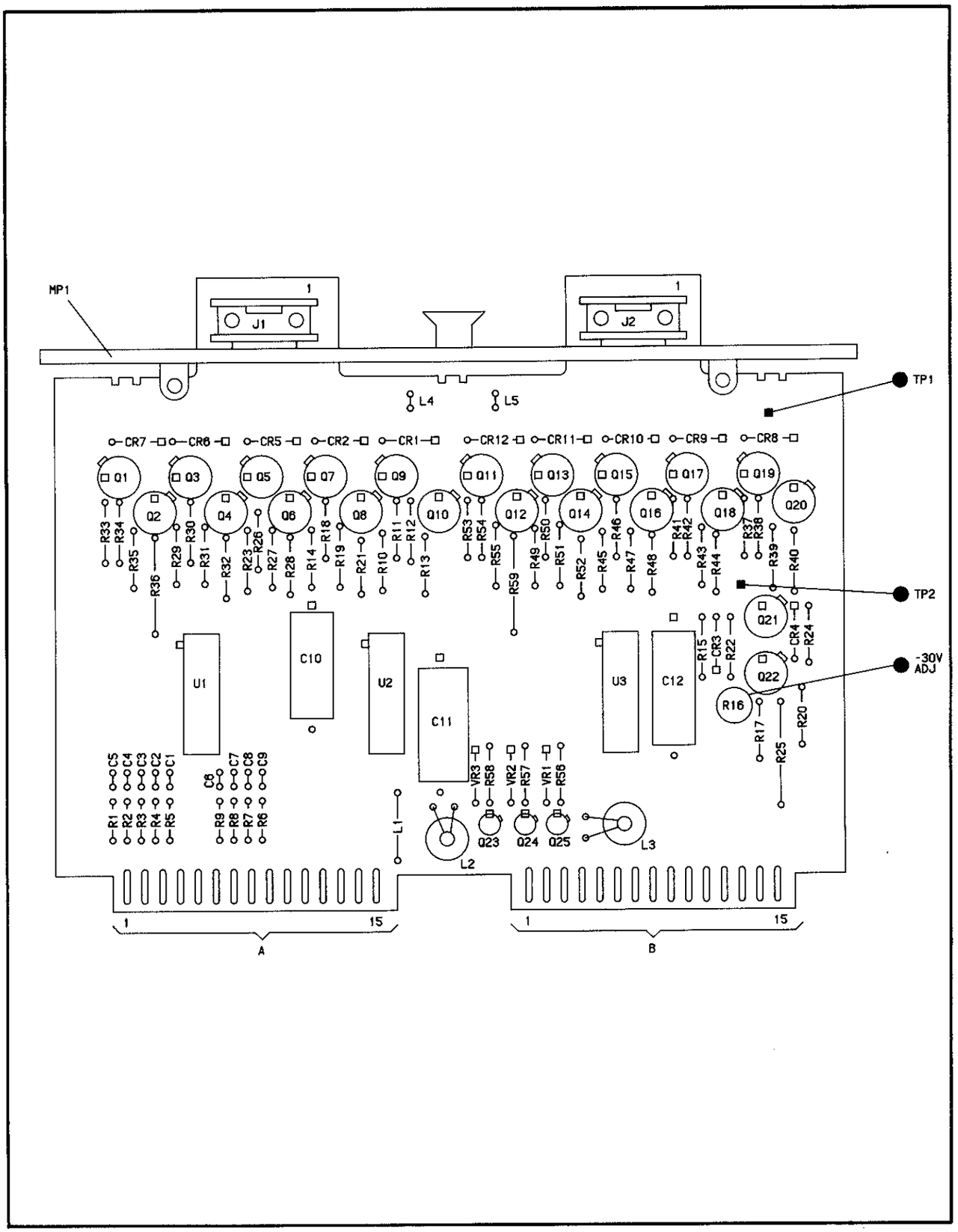


Figure 8-314. A6A9 Reference and High Frequency Loops Sections Controller Component Locator

CHANGES

All serial prefixes

On the A6A9 schematic:

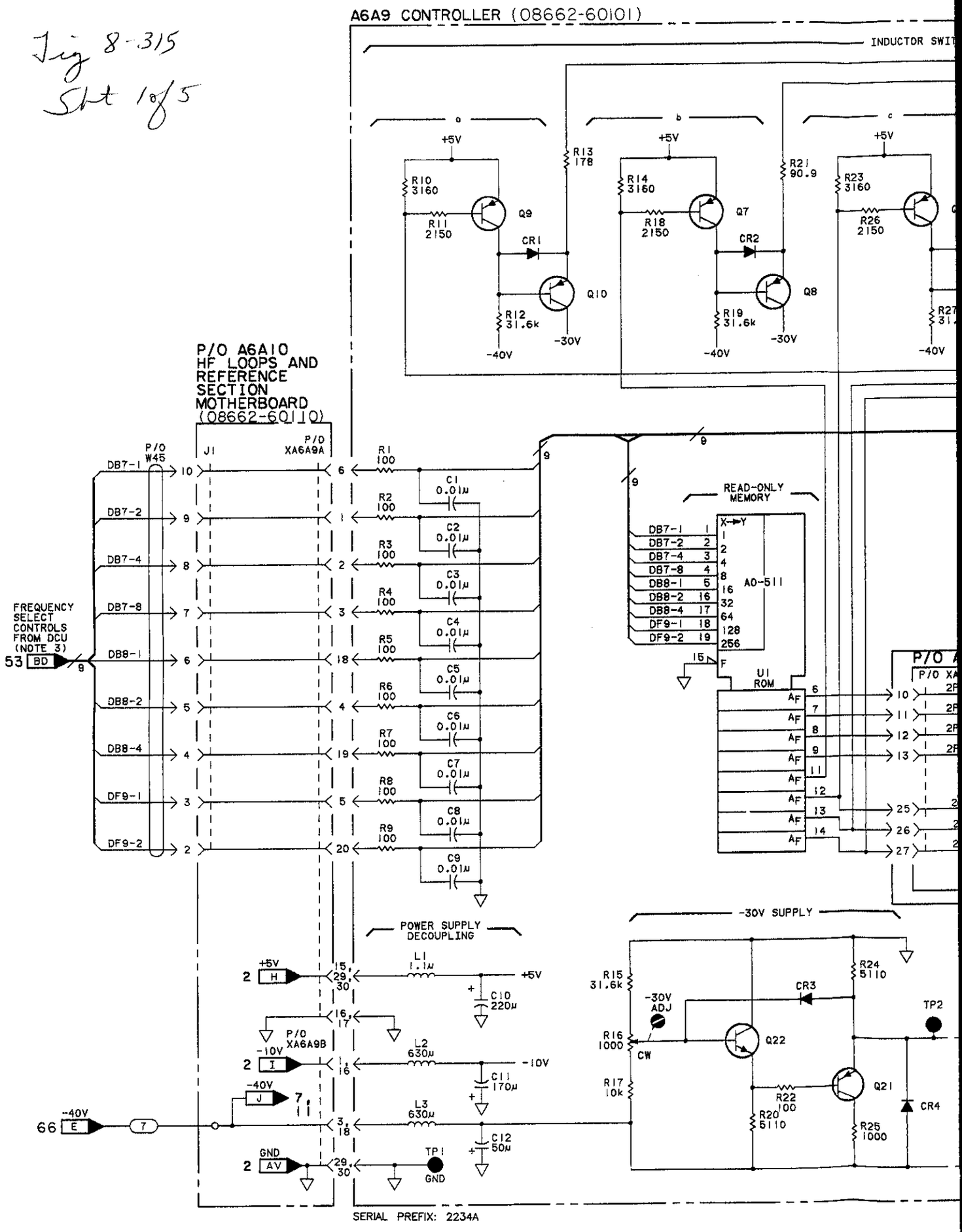
- A6A9R8, R9 - Change the value of R8 and R9 to 196 ohms.

2552A and Above

On the A6A9 schematic:

- A6A9 - Change the part number of the A6A9 CONTROLLER to 08662-60326.

Fig 8-315
Sht 1 of 5



SERIAL PREFIX: 2234A

Fig 8-315 Sht 2 of 5

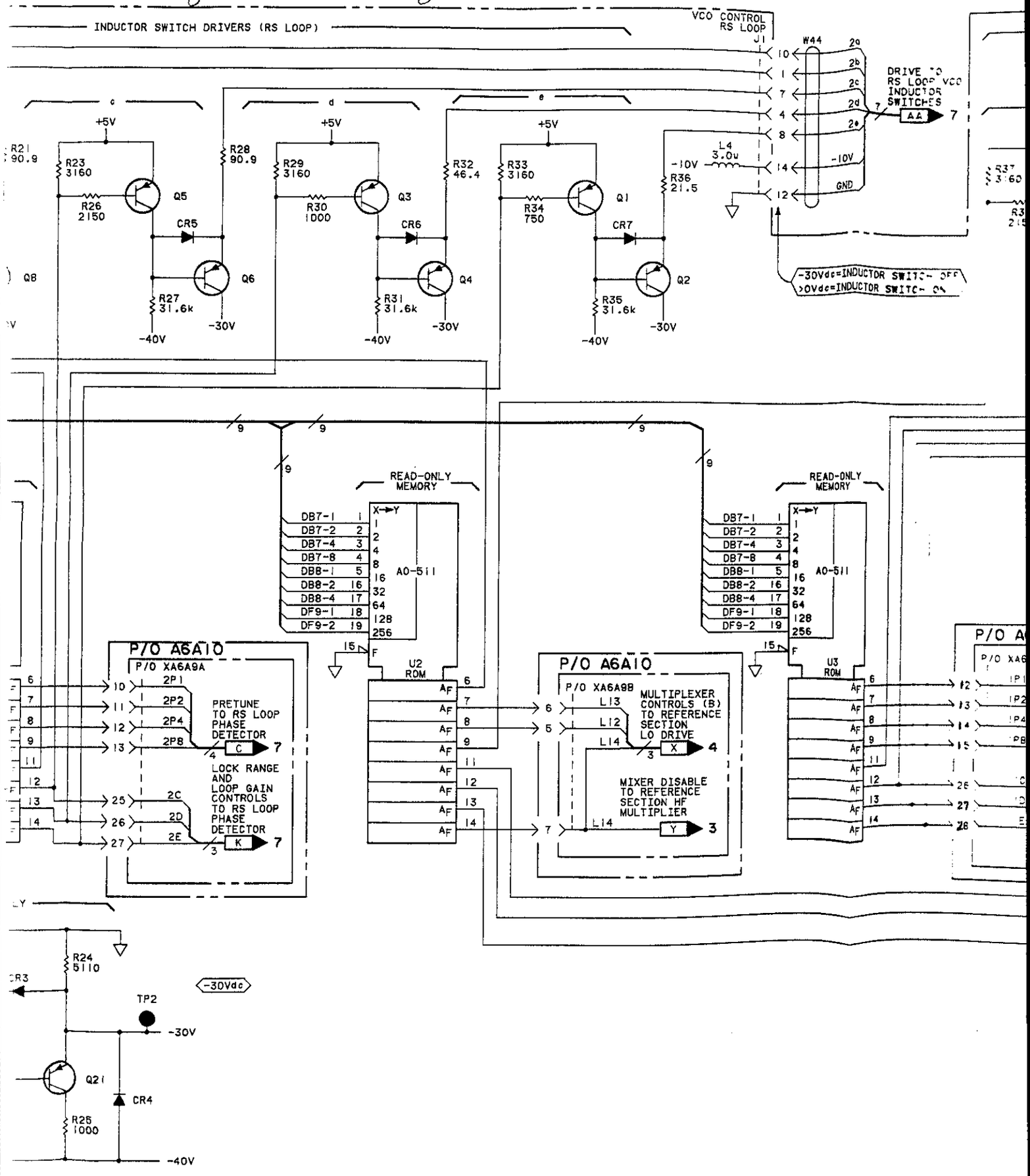


Fig 8-315 Sht 3 of 5

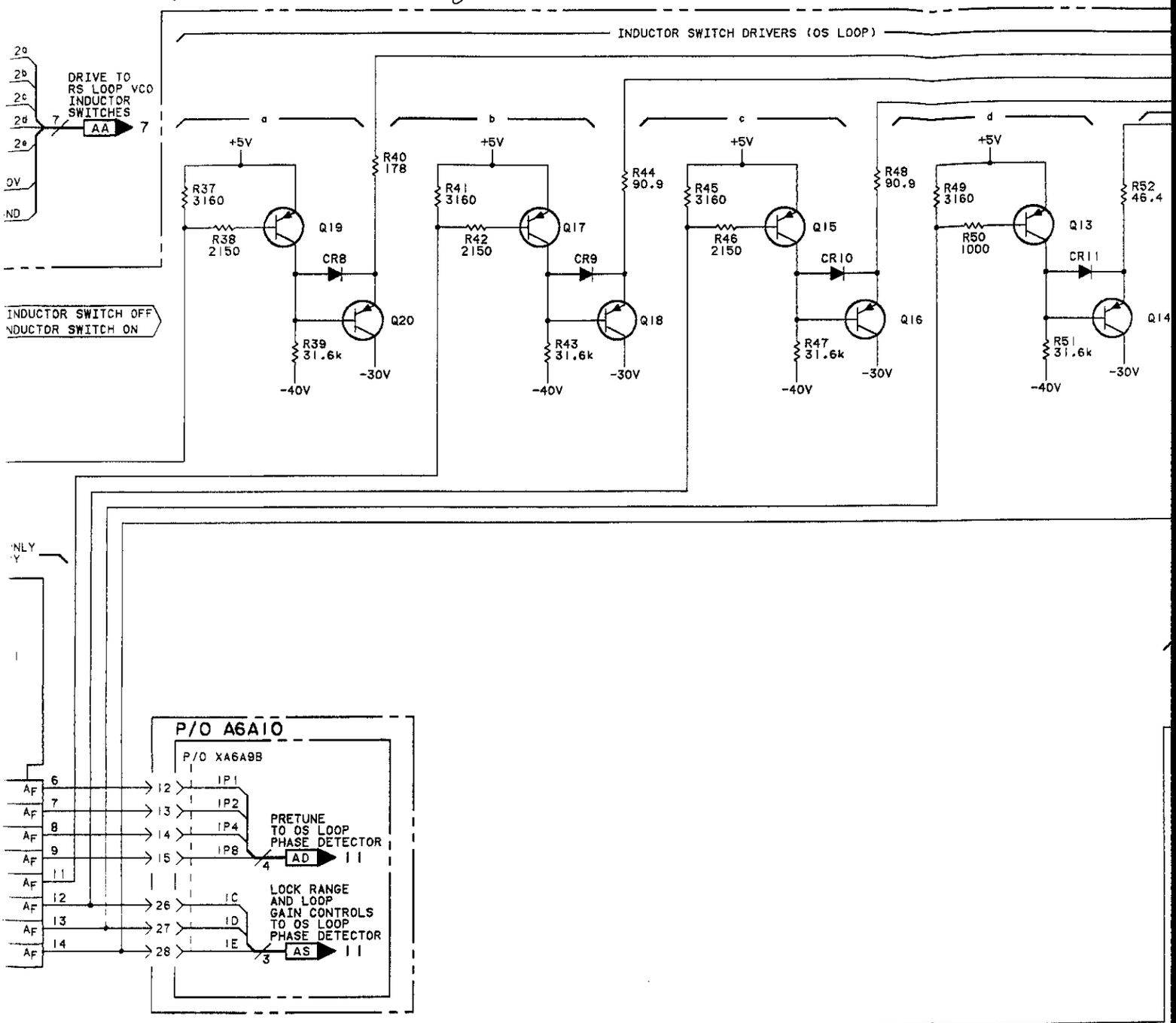
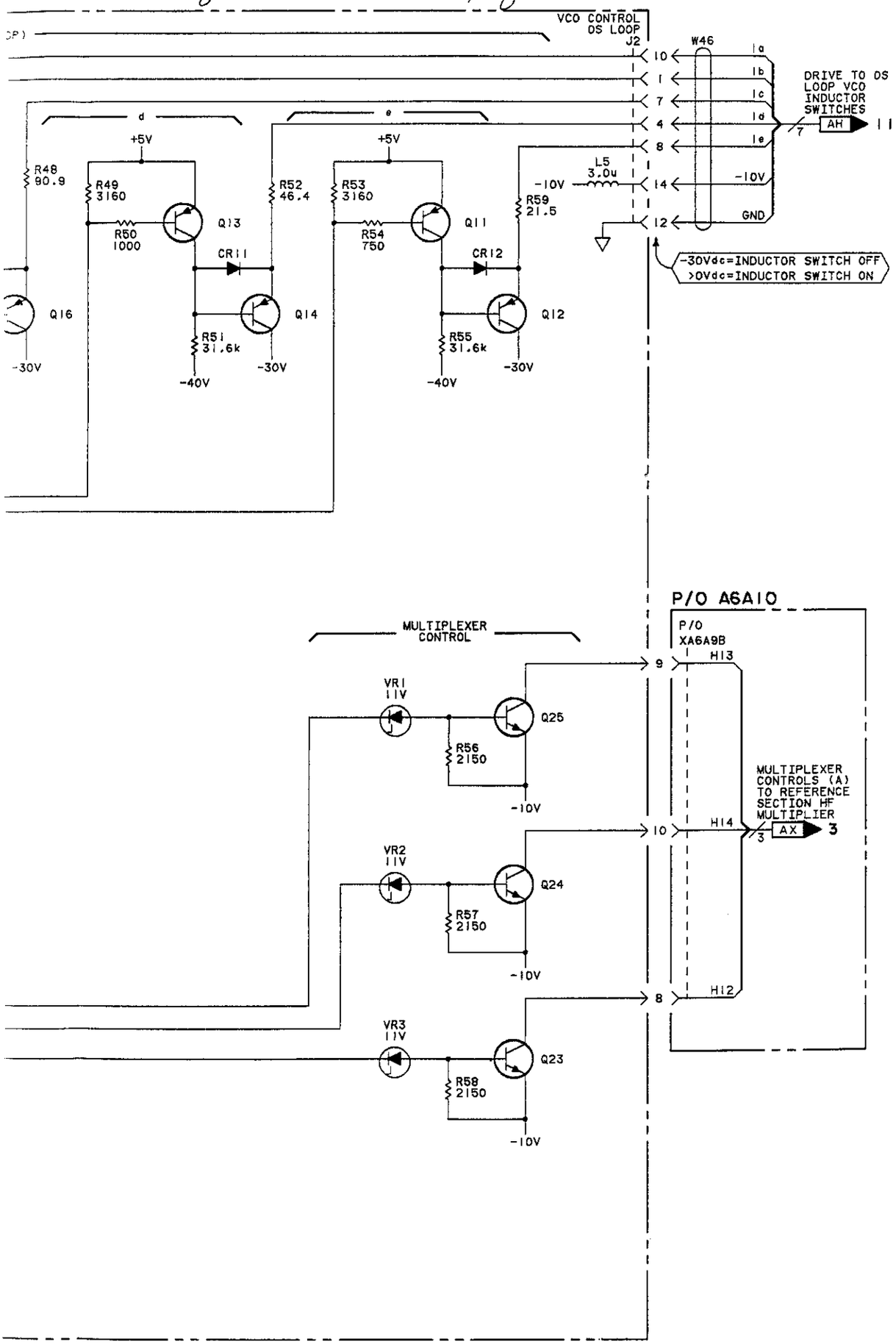


Fig 8-315 Sht 4 of 5



1. REFER TO TABL
DIAGRAM NOTES

2. TROUBLESHOOTI
THEY ARE ACTU
YOUR MEASUREM
DIFFERENT THA

3. THIS DIGITAL
FRONT PANEL FR
FOLLOWS. FOR
BETWEEN 320 A
a. DB7-1 THR
BINARY WE
TO THE D8
PANEL FRE
b. DF0-1 AND

D9(100MHz)D OF FREQUE DISPLAY
3
4
5
6

REFERE
NO PRE
W44-46
A6A8
C1-12
CR1-12
J1,2
L1-5
Q1-25
R1-59

LOGI
HIGH
LOW
< IS MO
> IS MO
OPEN
GROUND

TR
INTE
P

REFERE DESIGNAT
Q1-2
Q22.
Q23-2
U1
U2
U3

INTE
V
GROU

REFERE DESIGNAT
U1-3

A6A9 U1
TOP VIE

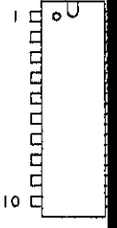
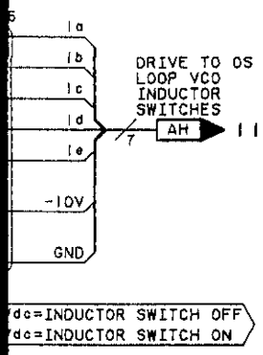


Fig 8-315
Sh 5 of 5

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. THIS DIGITAL DATA IS RELATED TO THE FRONT PANEL FREQUENCY DISPLAYS AS FOLLOWS. FOR A FREQUENCY SELECTION BETWEEN 320 AND 640MHz:
   a. DB7-1 THROUGH DB8-4 FORM A 7 BIT BINARY WEIGHTED VALUE EQUIVALENT TO THE D8 D7 DIGITS OF THE FRONT PANEL FREQUENCY DISPLAY.
   b. DF9-1 AND DF9-2 ARE SPECIAL CODES.

D9(100MHz)DIGIT OF FREQUENCY DISPLAY	DF9-1	DF9-2
3	1	1
4	0	0
5	1	0
6	0	1

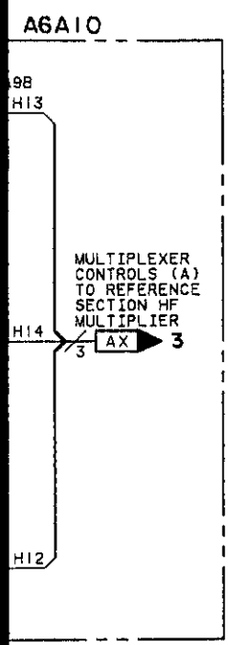


REFERENCE DESIGNATIONS

NO PREFIX	A6A9 CON'T
W44-46	TP1,2
A6A9	U1-3 VR1-3
C1-12 CR1-12 J1,2 L1-5 Q1-25 R1-59	A6A10
	J1 XA6A9A,B

LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW

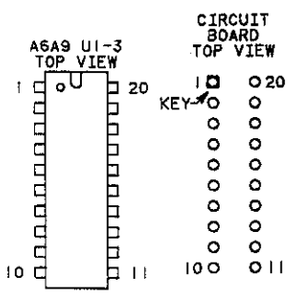


TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1-21	1853-0012
Q22	1854-0263
Q23-25	1854-0071
U1	08662-80005
U2	08662-80006
U3	08662-80007

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1-3	+5V - 20 ⏚ - 10



SERVICE SHEET 5
A6A9

Figure 8-315. A6A9 Reference and High Frequency Loops Sections Controller Schematic

SERVICE SHEET 6
A6A6 RF MIXER ASSEMBLY

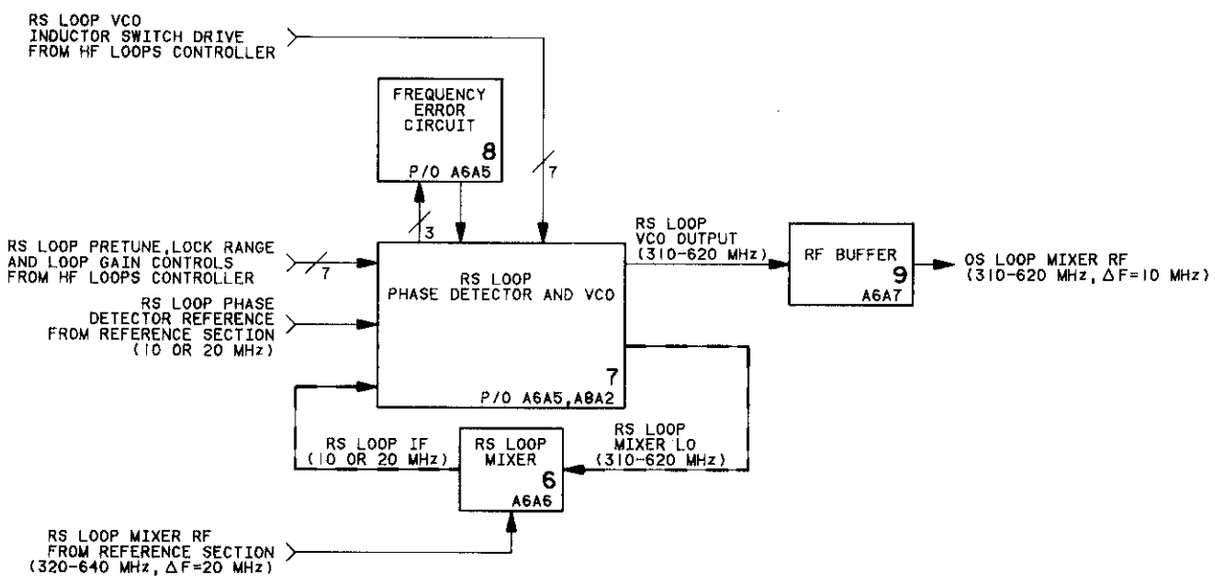
REFERENCE BLOCK DIAGRAM 3
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Refernce Sum Loop RF Mixer Board contains circuitry that combines the 310 MHz to 620 MHz and 320 MHz to 640 MHz inputs to produce the 10 MHz or 20 MHz loop IF output. The two limiter stages serve as buffers and also provide a constant output level to the linear amplifier. Each limiter stage has a gain of about 10 dB and limits at approximately +1 dBm.

The output of limiter U2 is fed to the single stage common emitter amplifier (Q1), which has a gain of about 8 dB. The mixer is a double balanced type (that is, both inputs are suppressed at the output). The output of the mixer contains the sum and difference frequencies of the two input signals at a power level of approximatiely -16 dBm. The sum signal is filtered by the 25 MHz low-pass filter, leaving only the desired difference signal at the output.



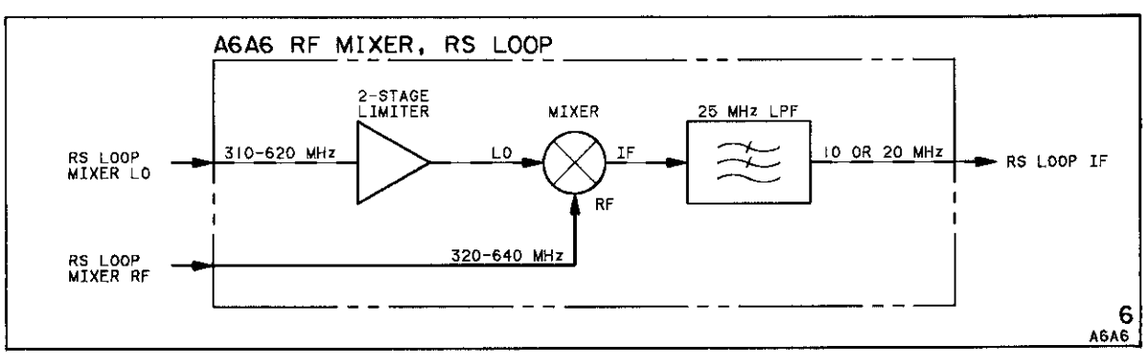


Figure 8-316. A6A6 Reference Sum Loop RF Mixer Block Diagrams

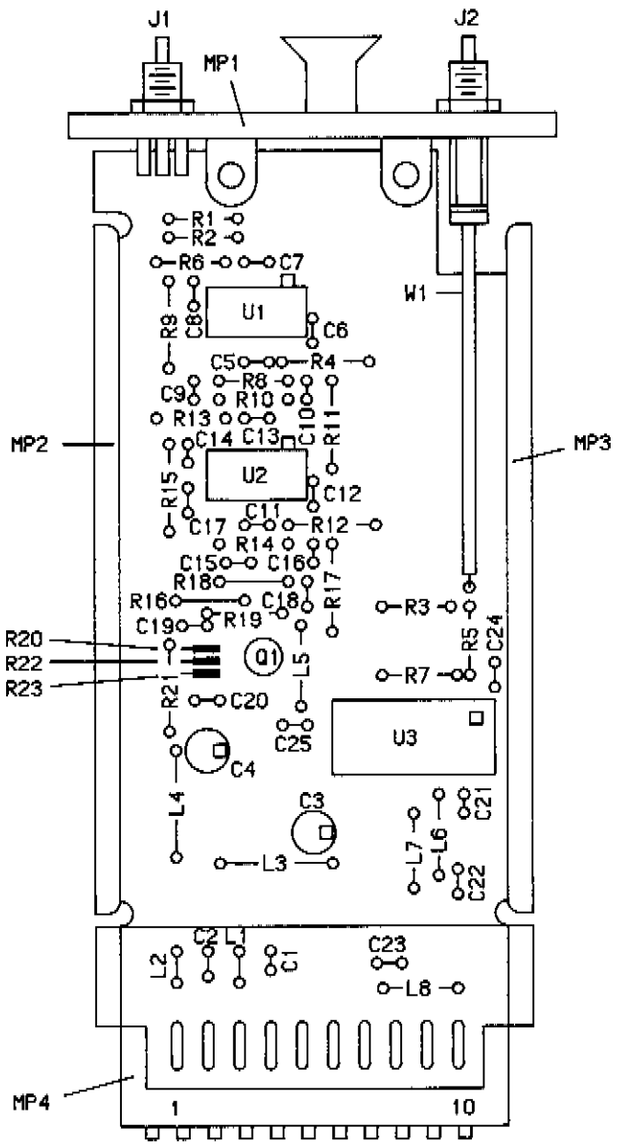
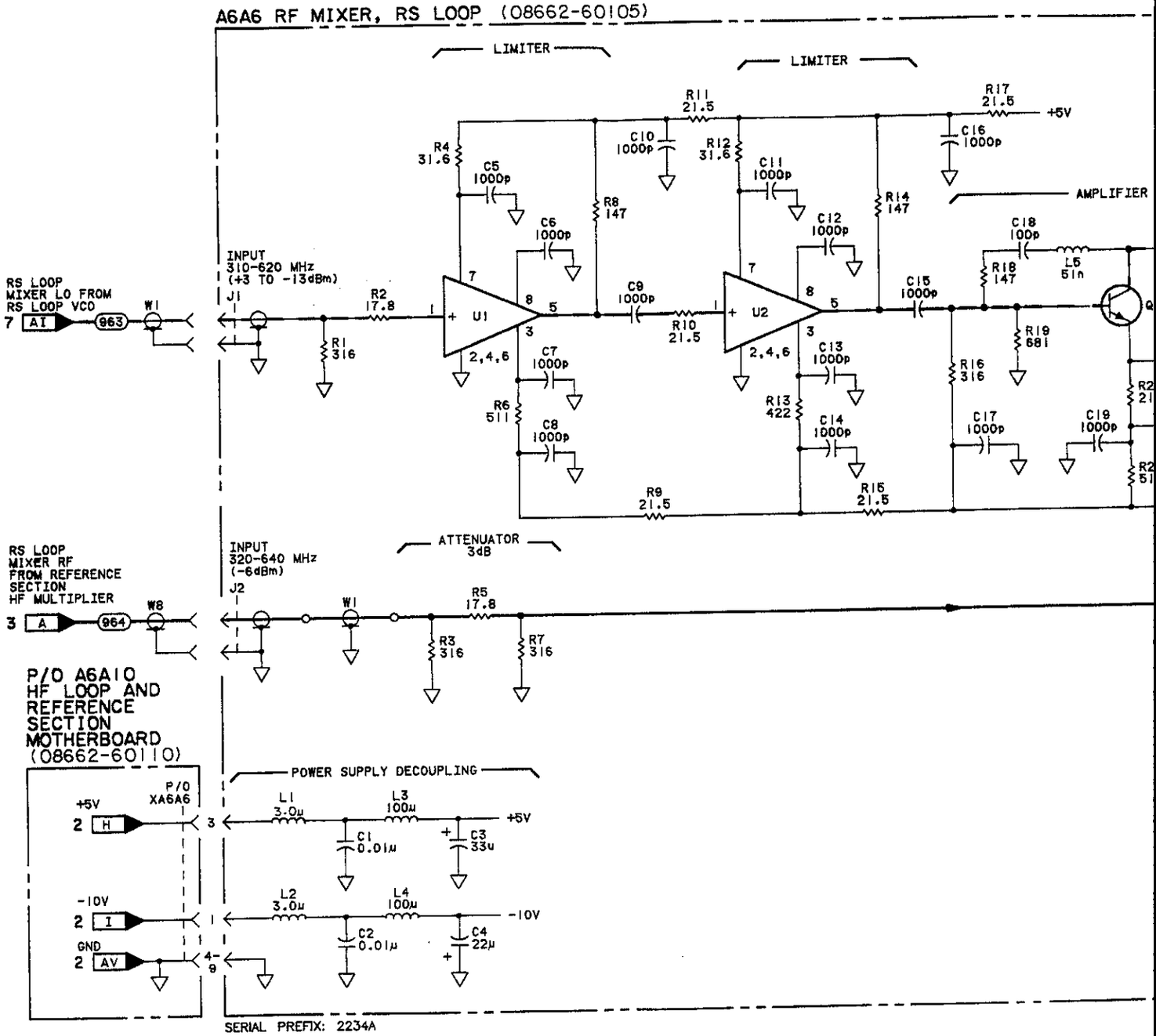


Figure 8-317. A6A6 Reference Sum Loop RF Mixer Component Locator

CHANGES

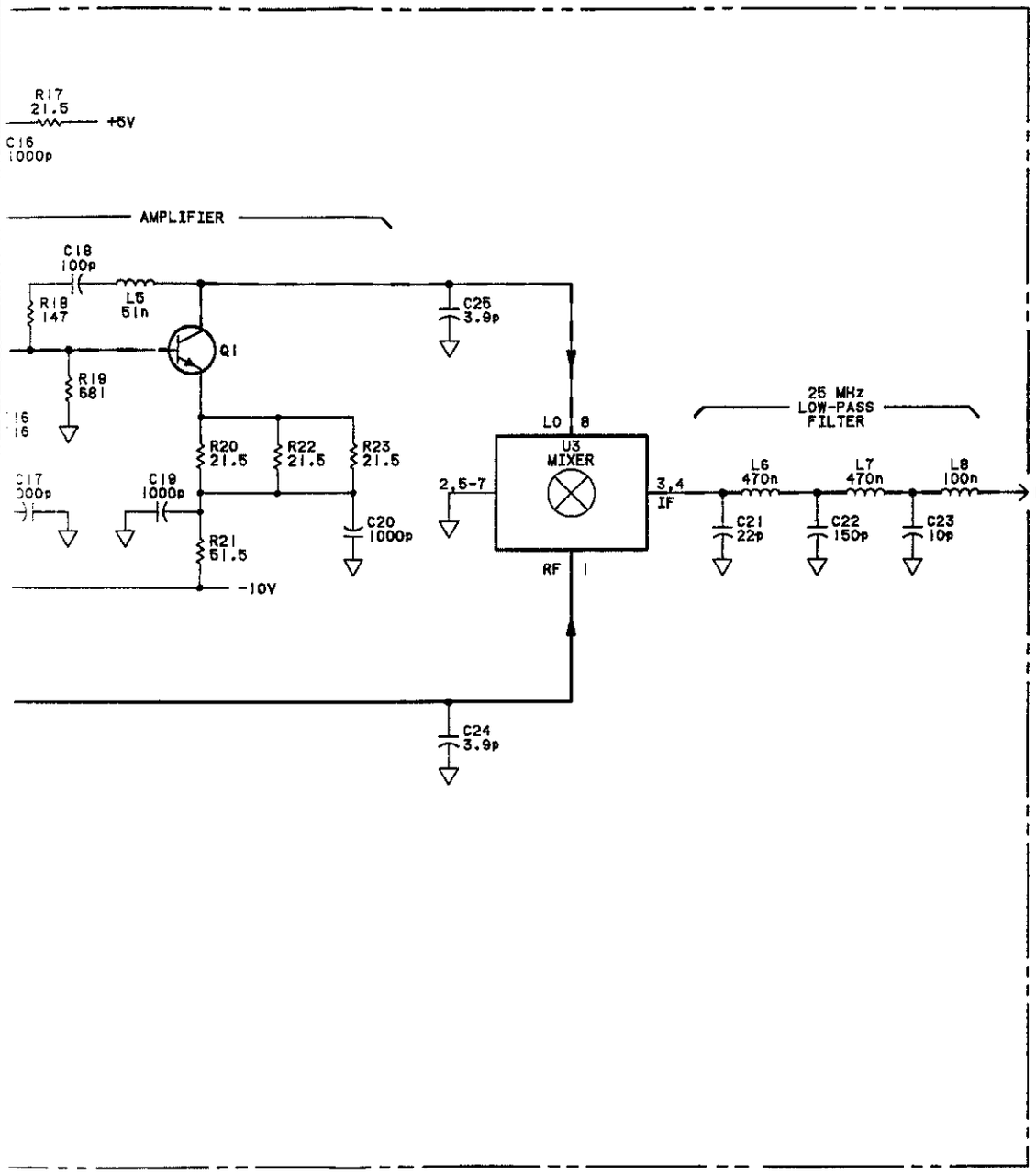
2837A and above	On the A6A6 schematic: • C1, C2 - Under **POWER SUPPLY DECOUPLING** change the value of C1 and C2 to 1000pF.

Fig 8-318
Sht 1 of 3



SERIAL PREFIX: 2234A

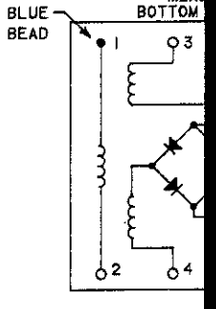
Fig 8-318
Sht 2 of 3

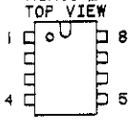


1. REFER
DIAGRA
2. TROUBL
THEY A
YOUR M
DIFFER

REFEREN
NO PREF
W1,8
A6A6
C1-25 J1,2 L1-8 Q1 R1-23 U1-3 W1

A6A6
MIXE
BOTTOM





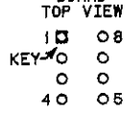


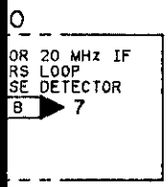
Fig 8-318
Sht 3 of 3

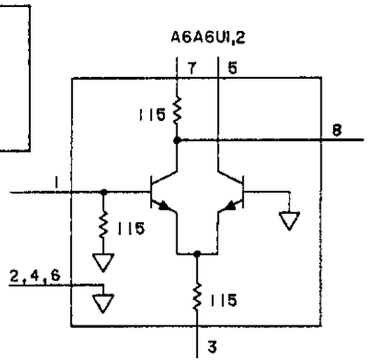
NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

REFERENCE DESIGNATIONS

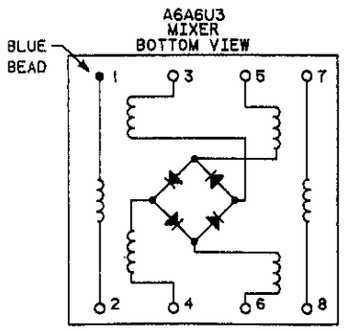
NO PREFIX	A6A10
W1,8	XA6A6
A6A6	
C1-25 J1,2 L1-8 Q1 R1-23 U1-3 W1	

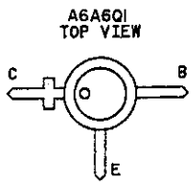


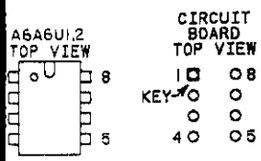


TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1	1854-0720
U1,2	1826-0372
U3	0955-0096







SERVICE SHEET 6

A6A6

Figure 8-318. A6A6 Reference Sum Loop RF Mixer Schematic

SERVICE SHEET 7
P/O A6A5, A8A2 REFERENCE SUM LOOP PHASE DETECTOR AND VOLTAGE CONTROLLED OSCILLATOR ASSEMBLY

REFERENCE BLOCK DIAGRAM 3
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The 10/20 MHz loop phase detector reference signal (at J1) and the 10/20 MHz loop IF signal (at board pin 1) are attenuated and amplified, respectively, and are sent to the phase detector formed by CR1, CR2, CR3, and CR4. The phase detector combines the two signals and outputs a difference signal which is filtered by a 5 MHz low-pas filter and a 19 MHz broadband notch filter before entering the integrator formed by Q7, Q8, and Q9.

The integrator output current is converted to voltage by Q10. This voltage is summed with a four-bit ROM-controlled BCD pretune current in the resistor-diode shaper. The resulting voltage is then filtered, buffered, and used to drive the VCO so that it produces linear tuning with constant loop gain.

The frequency range of the integrator voltage is automatically adjusted to maintain a constant lock range for the loop. The long time constants associated with switching the RC loop gain adjust are accelerated by the speed-up circuit during switching.

Loop Reference and IF Limiters

Before the 10/20 MHz loop IF (from the RF mixer) is compared against the 10/20 MHz loop phase detector reference frequency within the double balanced phase detector, the two signals are passed through identical limiters. Prior to entering the limiters, the reference signal is attenuated by 3 db and the IF signal is amplified by 8 dB so that the two signals have amplitudes of about -3 dBm to -5 dBm. The limiters have adequate gain at this input level to produce sharp limiting action over the 10 MHz to 20 MHz frequency range. The outputs of the limiters are connected to the inputs of center-tapped transformers T1 and T2. These transformers, together with four PN junction diodes, form the high level mixer/phase detector.

Phase Detector

A high level mixer is used as the phase detector on this board. Switching both sides of the phase detector hard generates a very linear slope. IF signals are suppressed by double balanced action so that the main components at the output are dc phase and two times the IF signal. the two signals from the limiters and the phase detector output signal operate the lock acquisition circuitry.

Integrator

The phase detector's output signal passes through the 5 MHz low-pass filter and a 19 MHz notch filter. The signal which enters the integrator is either an ac difference frequency or a dc voltage (for signals of the same frequency). In this latter case, the dc varies between +-0.6 volts. The integrator has a large dc gain with a zero located at about 7 kHz. The loop locks at a 90° phase difference when the dc voltage reaches 0 volts. The integrator has only one driving input when the difference frequency is less than 200 kHz. This input comes from the 5 MHz low-pass filter. If the difference signal is greater than 200 kHz, an additional drive current (the primary driver at this point) is supplied by the out-of-lock circuitry.

The integrator's output is proportional to the charge across its feedback capacitor. The output level will be between 0 volts and some positive level determined by the lock range limit control and limit detector (set by the controller).

The integrator is actually a discrete component op-amp. It produces output voltages in 8 ranges. These 8 ranges accommodate the widely differing voltage-frequency sensitivity of the VCO caused as various combinations of inductors are switched into the VCO. Gain of the integrator is maximum at dc, but reaches unity between 250 kHz and 500 kHz. The high gain for close-in signals suppresses VCO noise.

Lock Range Limit Control and Out-Of-Lock Detector

As inductors in the VCO are switched ON in parallel, the VCOs sensitivity increases. As the VCO frequency is increased from 310 MHz to 640 MHz by progressively switching in inductors A, B, C, D, and E, the oscillators' gain increases by a factor of four (12dB). To maintain constant lock range, the positive voltage swing of the integrator is limited by a 3-bit D/A converter controlled by the signals that switch inductors C, D, and E, the most significant frequency bits. The output of the D/A resistive ladder drives the out-of-lock circuitry.

The out-of-lock detector (U4) compares the D/A output against the positive swing of the integrator. If the output becomes too positive, an out-of-lock signal is generated. Loss of signal or oscillator-drift, causing the integrator to reach its positive voltage limit, triggers this circuit and causes four things to happen. It lights the out-of-lock LED, sends TTL LO signals back through the motherboard to the microprocessor, enables the first dual CMOS switch and the two TTL trigger circuits, and enables the digital discriminator to clock the mixer beat note, producing a pulse-width modulated discriminator signal.

Resistor Diode Shaping Network

The VCO is controlled by varying the reverse bias on a group of varactor diodes which form part of the oscillator's tank circuit. An increase in reverse bias causes a reduction in junction capacitance, which increases the frequency. However, the frequency characteristic of the tuning circuit is not a linear function of input voltage.

A shaping circuit on the Phase Detector Board is used to linearize the signal. The shaping circuit consists of a ladder of diodes which are reverse biased at successively higher voltages. As the signal level increases, the diodes become progressively forward biased, presenting a lower impedance to the drive source. The tuning curve of the VCO is thus approximated by the shaping circuits in a piecewise linear manner.

4-Bit BCD Pretune

The beat note of the difference of the loop IF down-converted frequency and the reference frequency passes through a 7 MHz low-pass filter to remove the RF sum frequency and leave only the difference frequency. The pretune ensures that this difference frequency will be less than 7 MHz by pretuning within 7 MHz of its locked frequency. The pretune D/A converter is formed by quad comparator U13, JFET switches Q17-Q20, and associated circuitry. The Reference Sum Loop pretune inputs accept TTL signals from the Controller Assembly (service sheet 5) to control the pretuning. The pretunes are weighted BCD currents of 0.63mA, 1.25mA, 2.50mA, and 5.00mA. R85 allows the pretune currents to be scaled up or down by 7% and allows for minimization of dc offset. The collector of Q12 injects the pretune current into the resistor-diode shaper.

Loop Gain Adjust and Pretune (Speed-Up) Circuitry

The loop gain adjust circuit works on the same principle as the lock range circuit. VCO inductor lines C, D, and E control gates that activate the RC attenuator sections in the loop gain adjust circuit, ensuring that no phase shift occurs at the loop gain crossover frequency. Because of the low frequency and large capacitors, diodes CR29, CR30, CR31, and CR32 are used to speed up charging of these capacitors during switching. R95 and C49 keep loop gain as constant as possible with any combination of inductors A, B, C, D, and E switched on.

VCO (A8A2)

The VCO in the high frequency loops section is a non-field-repairable assembly; it is sealed and can only be repaired at the factory. The VCO is coarsely tuned by a 5-bit code which switches inductors A, B,,C, D, and E inside the VCO. A control voltage of -9 Vdc to -38 Vdc fine tunes the VCO to lock the loop. The output frequency of the VCO extends from 310 MHz to 620 MHz, at +3 dBm to -13 dBm (level depends on frequency).

TROUBLESHOOTING

When a high frequency loops problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

1. Mount the A6A5 assembly on an extender board. Move the slide switch to the TEST position (up). This opens the loop.

2. Set the front panel frequency setting to 510.0 MHz. Connect a counter or spectrum analyzer to the A8A2 VCO output [disconnect cable W43 (965) from A6A7J1 and measure the signal at the end of the cable]. Connect the output of an adjustable power supply to A6A5TP14 (+) and A6A5TP1 (-).

3. Set the power supply output voltage to approximately 4 volts. The counter should read close to 510 MHz. Slowly decrease the power supply output to zero, and then increase the voltage to +8V. Check that the frequency changes as shown, but the amount and direction of change should be similar to these values.

Voltage to TP14 (Vdc)	TP2 (Vdc)	VCO Frequency (MHz)
0.0	-14.3	504
4.0	-11.8	498
8.0	-9.9	492

If these readings are correct, continue troubleshooting with step 4. Otherwise, there is a problem from TP14 to TP2. Troubleshoot to find the cause.

4. Monitor TP8 with the high impedance input of a counter. The counter should read the difference signal from the phase detector. Vary the adustable power supply so the VCO frequency varies above and below 500 MHz. The counter should read the absolute frequency error.

   If operation of this circuit is normal, continue troubleshooting with step 5. Otherwise, there is a problem with the phase detector circuitry.

5. Monitor TP7 (service sheet 8) with an oscilloscope or TTL logic probe. Vary the adjustable power supply so the VCO varies above and below 500 MHz. TP7 should be a TTL logic high (>2.4 Vdc) when the VCO is within 200 kHz of 500 MHz. At more than 500.2 and less than 499.2 MHz, TP7 should become a TTL logic low (<0.8 Vdc).

   If operation of this circuit is normal, continue troubleshooting with step 6. Otherwise, there is a problem with the out-of-lock discriminator circuitry (bottom half of service sheet 8). Troubleshoot this circuitry to find the cause.

6. Monitor U3 pin 7 (service sheet 8) with a scope. Vary the adjustable power supply so the VCO is less than 499.7 MHz. The output of U3 should be less than 0.5 Vdc.

   Increase the VCO frequency to more than 500.3 MHz. The output of U3 should be more than 3.5 Vdc.

   If operation of this circuit is normal, continue troubleshooting with step 7. Otherwise, there is a problem with the frequency detector circuitry (top half of service sheet 8). Troubleshoot this circuitry to find the cause.

7. Monitor TP3 (service sheet 8) with an oscilloscope. Vary the adjustable power supply to increase the frequency of the VCO to more than 501.0 MHz. The signal at TP3 should be a dc level more negative than -3.0 Vdc. This level will become more negative as the RF output frequency increases.

   Decrease the frequency of the VCO to less than 499.0 MHz. The signal at TP3 should be a series of pulses with slow rise and fall times at about a +4 Vdc level. The level increases and the pulses get smaller as the RF output frequency decreases.

   If operation of this circuit is normal, continue troubleshooting with step 8. Otherwise, there is a problem with the CMOS switch (U7) or the circuitry that drives it. Troubleshoot this circuitry to find the cause.

8. Monitor TPA (output of integrator) with an oscilloscope. Vary the adjustable power supply to make the frequency of the VCO signal greater than 501.0 MHz. The waveform at TPA should be a dc level greater than +7.0 Vdc. Decrease the VCO frequency to less tan 499.9 MHz. The waveform at TPA should be a dc level near ground. Pulse like those seen on TP3 may be visible on either of these levels.

   If these waveforms are not normal, there is a problem with the integrator circuitry.

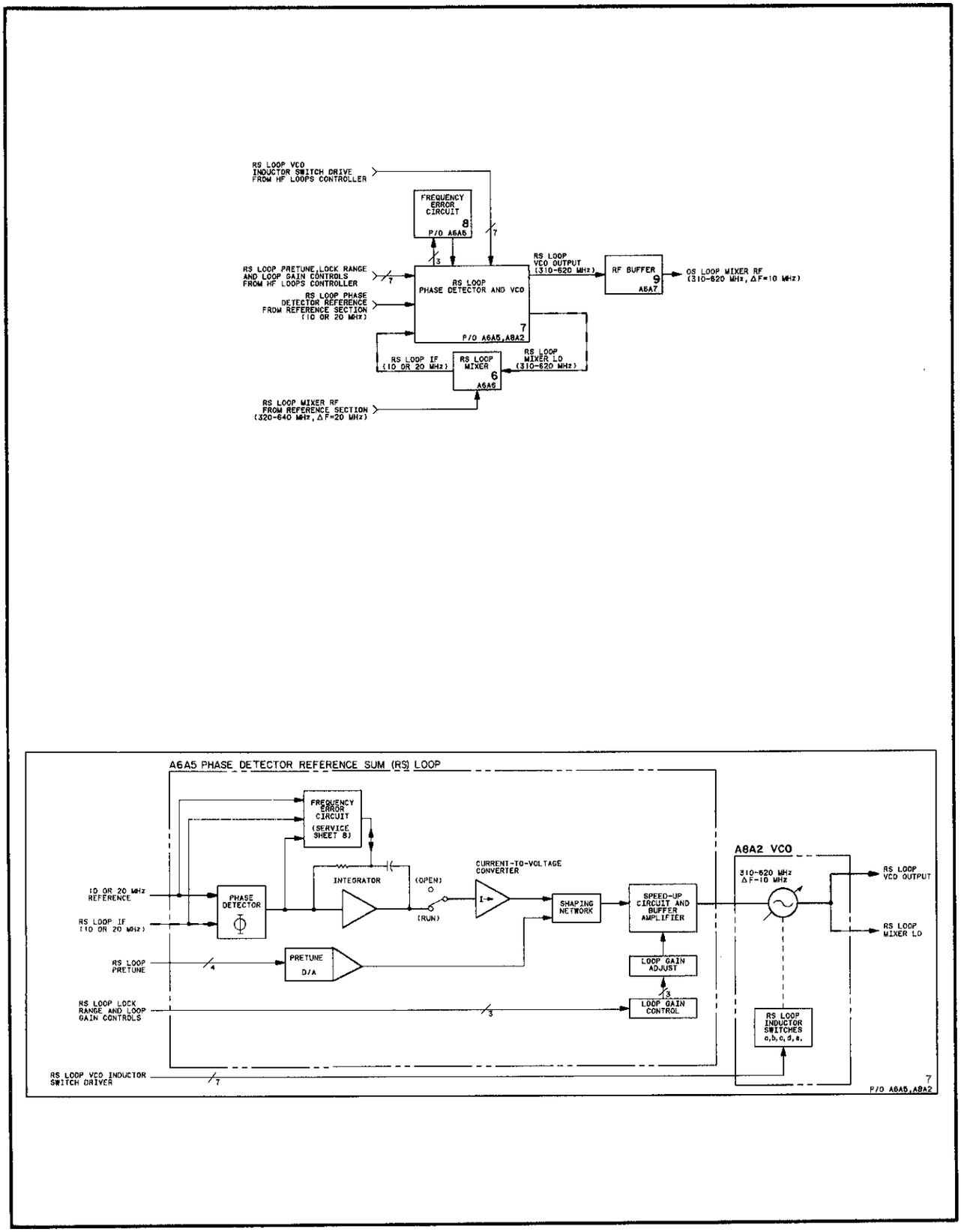


Figure 8-319. P/O A6A5 Reference Sum Loop Phase Detector Block Diagrams

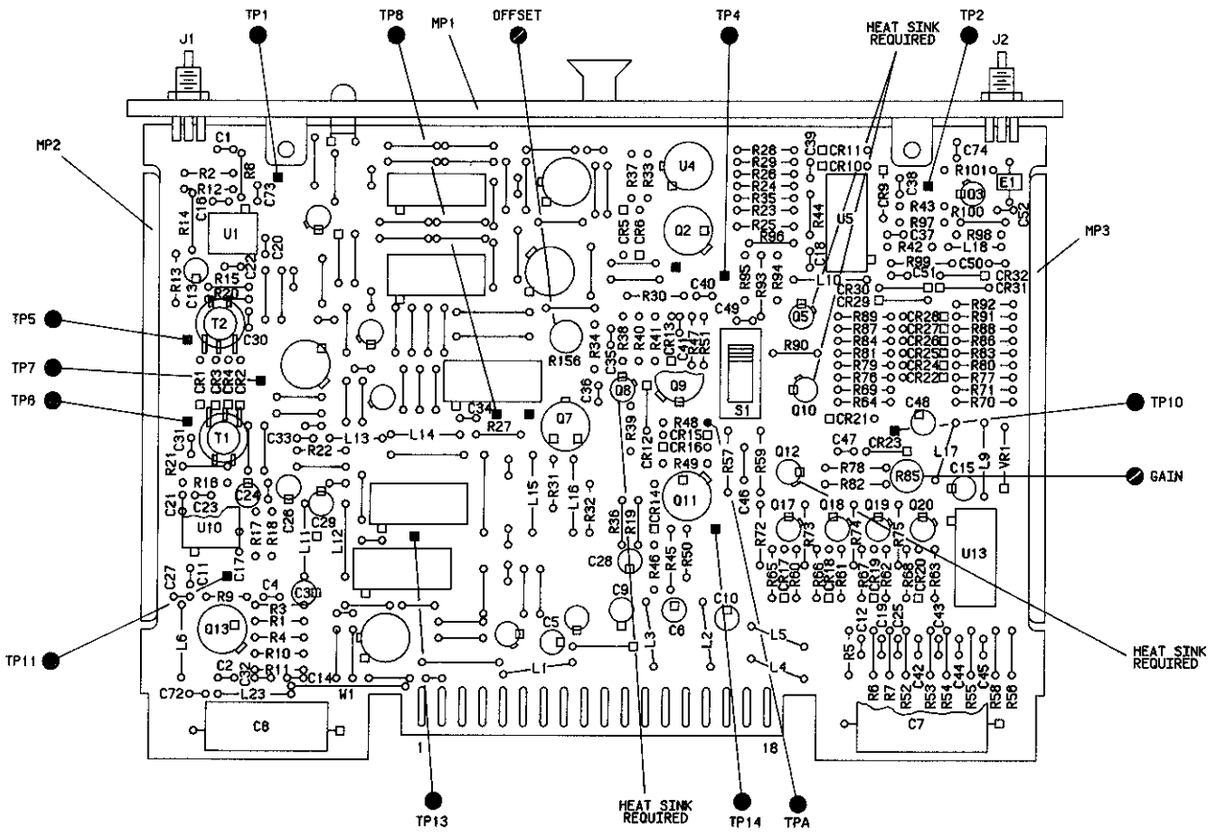


Figure 8-320. P/O A6A5 Reference Sum Loop Phase Detector Component Locator

CHANGES

2319A and above	On the A8A2 schematic: • A8A2 - Change the part number of the A8A2 Assembly to 08662-60317.
2601A and above	On the schematic: • A6A5Q7 - In the "Table of Transistor and Integrated Circuit Part Numbers", change the part number of Q7 to 1854-1046.
2706A and above	On the A6A5 schematic: • A6A5 - Change the part number of the A6A5 Assembly to 08662-60357.
2823A and above	On the A8A2 schematic: • A8A2 - Change the part number of the A8A2 Assembly to 08662-60417.
2837A and above	On the A6A5 Component Locator: • R2, R8, R12 - In the upper left hand corner of the component locator change R2 to C75, R8 to L24, and, delete R12. On the A6A5 schematic: • R2, R8, R12 - In the upper left hand corner of the schematic change **ATTENUATOR 3dB** to **25 MHz LOW PASS FILTER**. Delete R2, R8, and, R12. Add C75 100p to ground in place of R2 and add L24 560nH in place of R8.

Fig 8-321
Sht 1 of 5

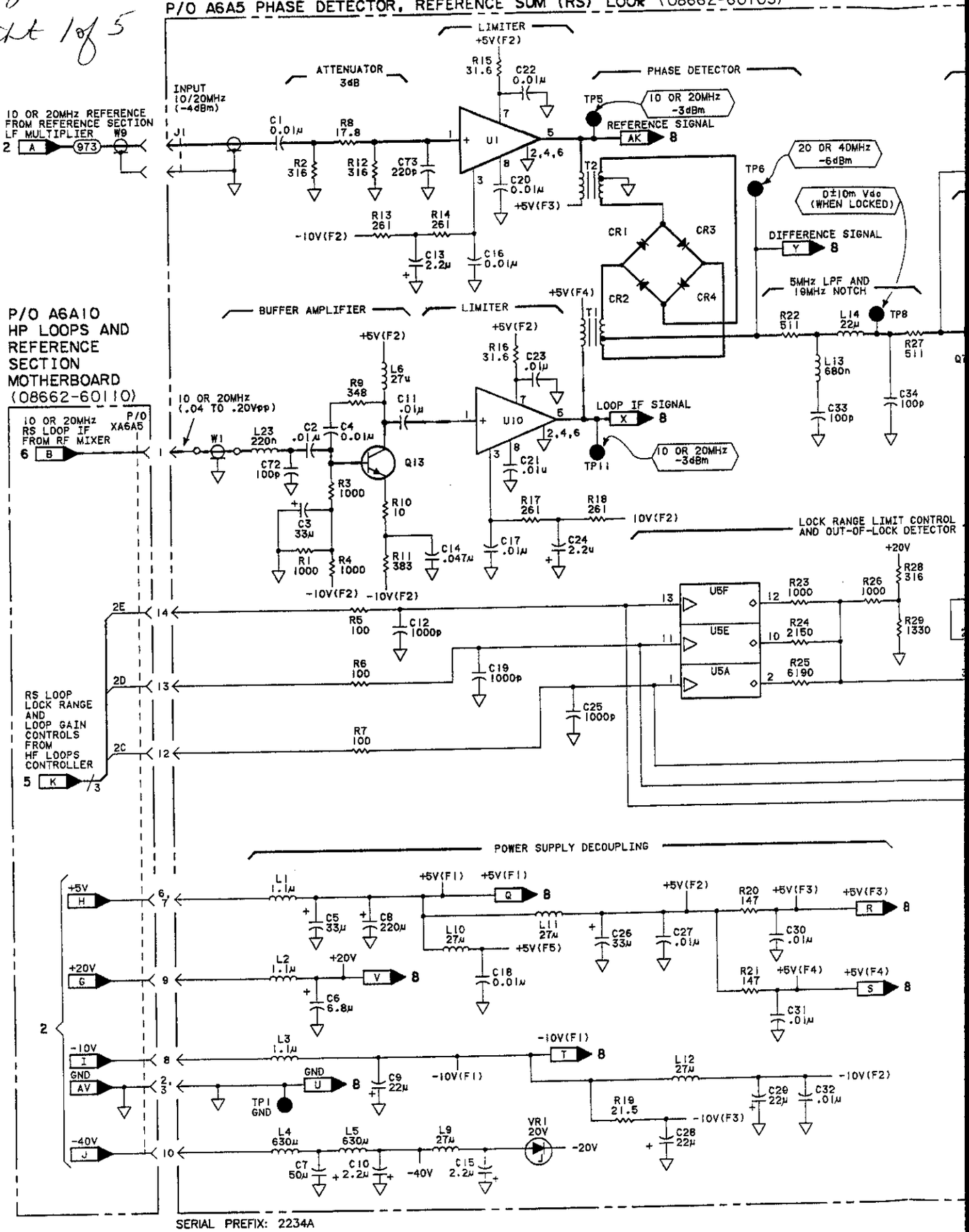


Fig 8-321 sht 2 of 5

2103)

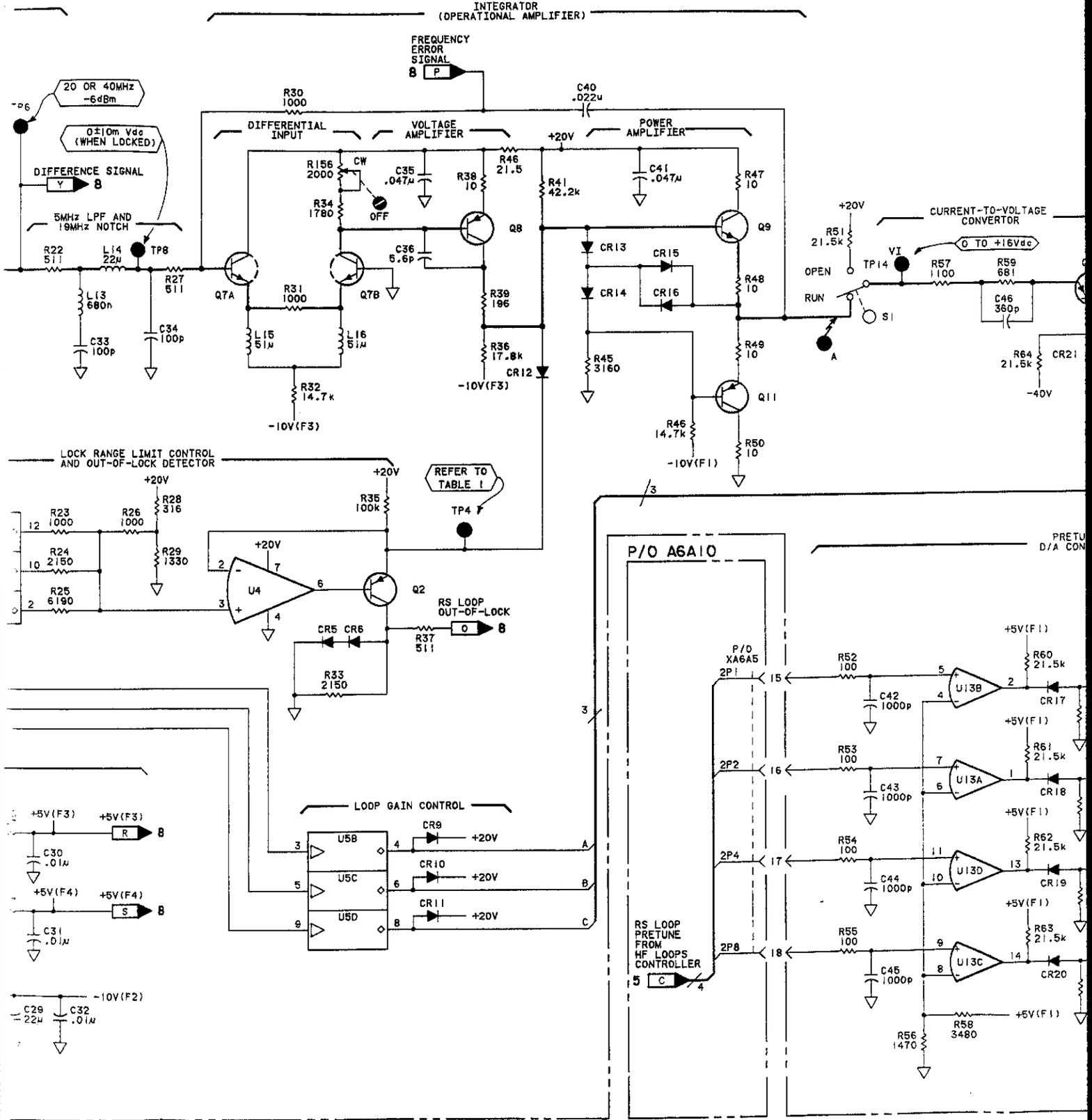
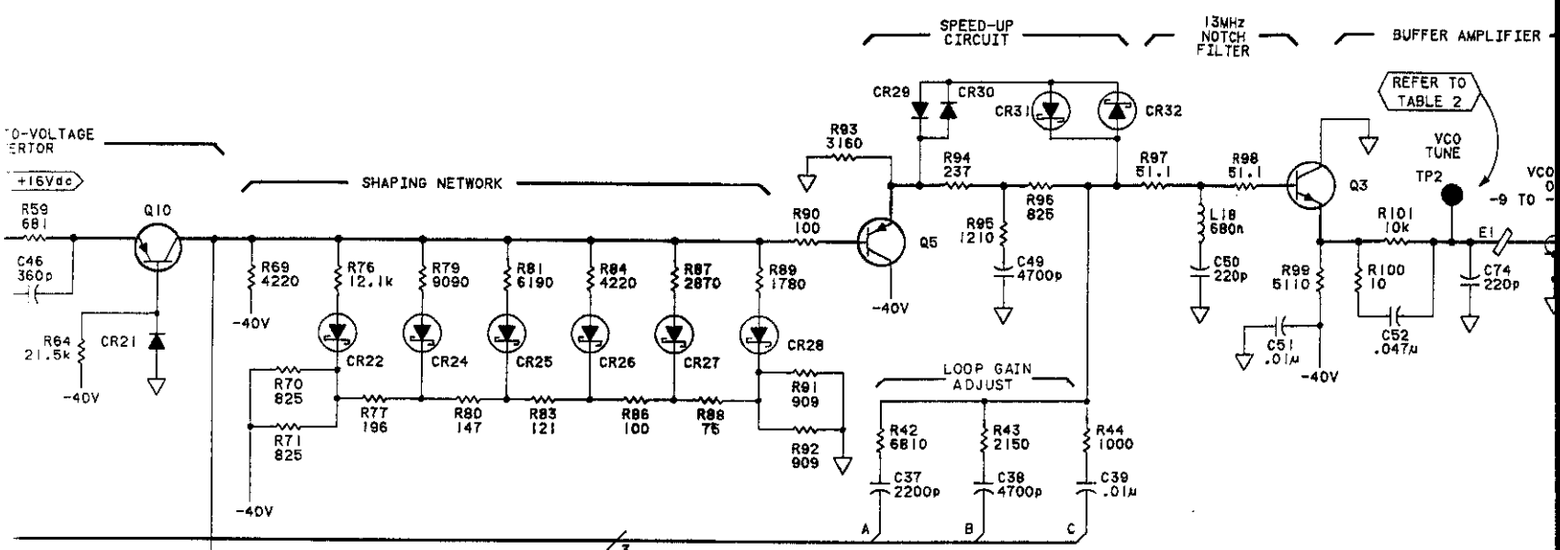


Fig 8-321 Sht 3 of 5



NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. THE A8A2 VOLTAGE CONTROLLED OSCILLATOR HAS SEVERAL ADJUSTMENTS WHICH ARE NOT RECOMMENDED FOR FIELD ADJUSTMENT. THESE ADJUSTMENTS SHOULD ONLY BE PERFORMED AT THE FACTORY

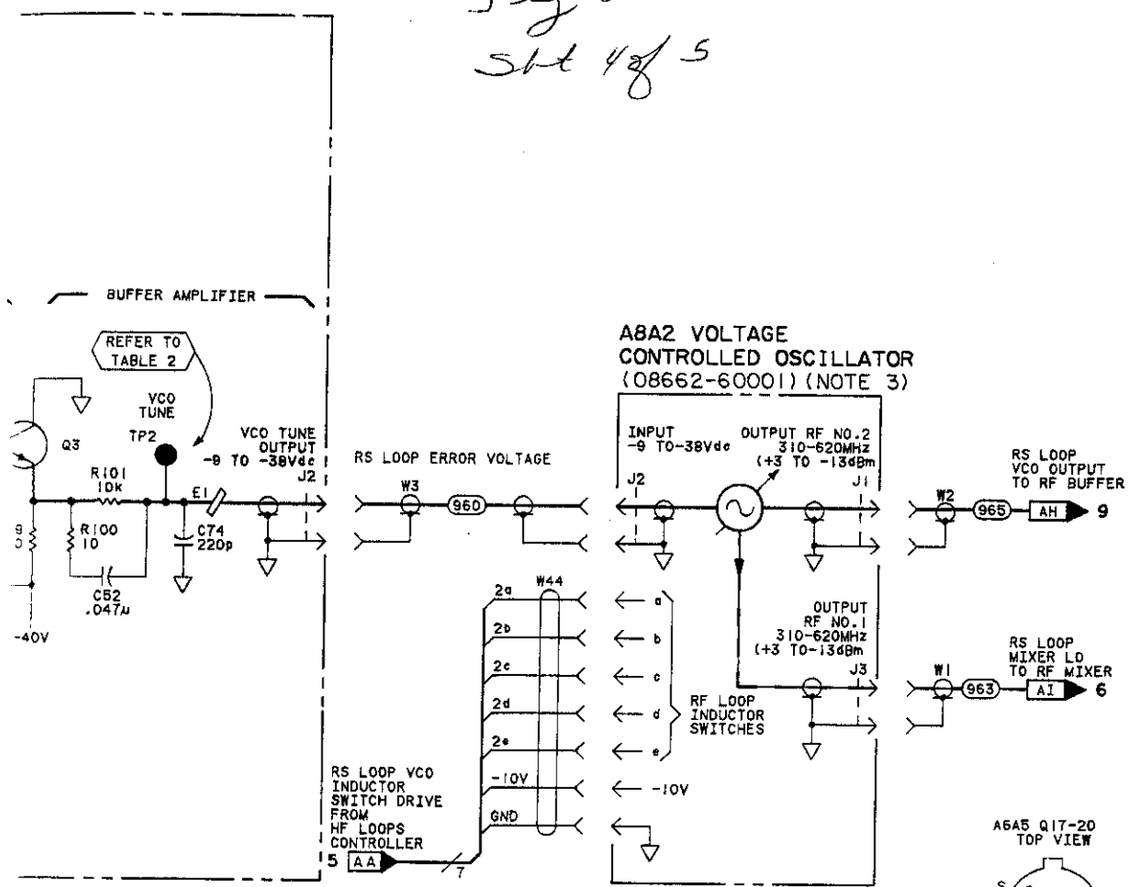
LOGIC LEVELS

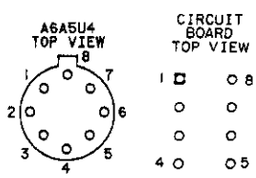
	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

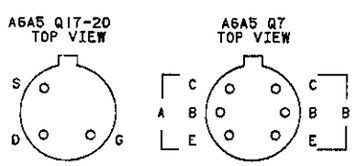
REFERENCE DESIGNATIONS

NO PREFIX	A6A10
W1-3,9,44	XA6A5
A6A5	A8A2
C1-52,72-74 CR1-6,9-32 E1 J1,2 L1-6,9-18,23 Q2,3,5,7-13,17-20 R1-101,156 S1 T1,2 TP1,2,4-6,8,10,11,14 U1,4,5,10,13 VR1 W1	J1-3

Fig 8-321
Sht 4 of 5







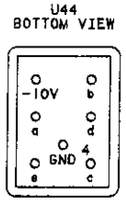
OGIC LEVELS	
	TTL
GH	>+2V
OW	<+0.8V
MORE	NEG.THAN
MORE	POS.THAN
EN	HIGH
UND	LOW

TABLE 1.
LOCK RANGE LIMIT CONTROL CHECK

FRONT PANEL FREQUENCY SETTING (MHz)	ACTIVE INPUTS	TP4 (Vdc)
330	NONE	16.1
370	2C	13.4
420	2D	10.2
520	2E	7.2
620	ALL	5.4

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U5	+5V(F5)-14
	- 7
U13	+5V(F1)- 3
	-20V -12



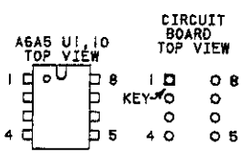
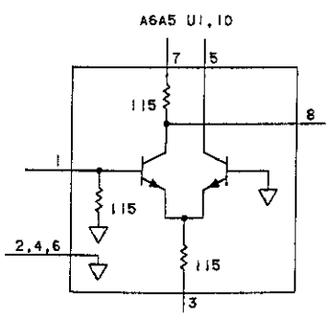
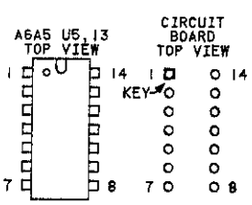


TABLE 2. PRETUNE CHECK

FRONT PANEL FREQUENCY SETTING (MHz)	PRETUNE BIT ON	TP10 (Vdc)	TP2* (Vdc)
340	NONE	-4.05	-36.1
430	2P1	-3.85	-33.5
530	2P2	-3.83	-30.8
350	2P4	-3.80	-26.3
520	2P8	-3.77	-19.9
510	ALL	-3.71	-13.1

*SET SWITCH S1 IN TEST POSITION TO MEASURE VOLTAGES AT TP2

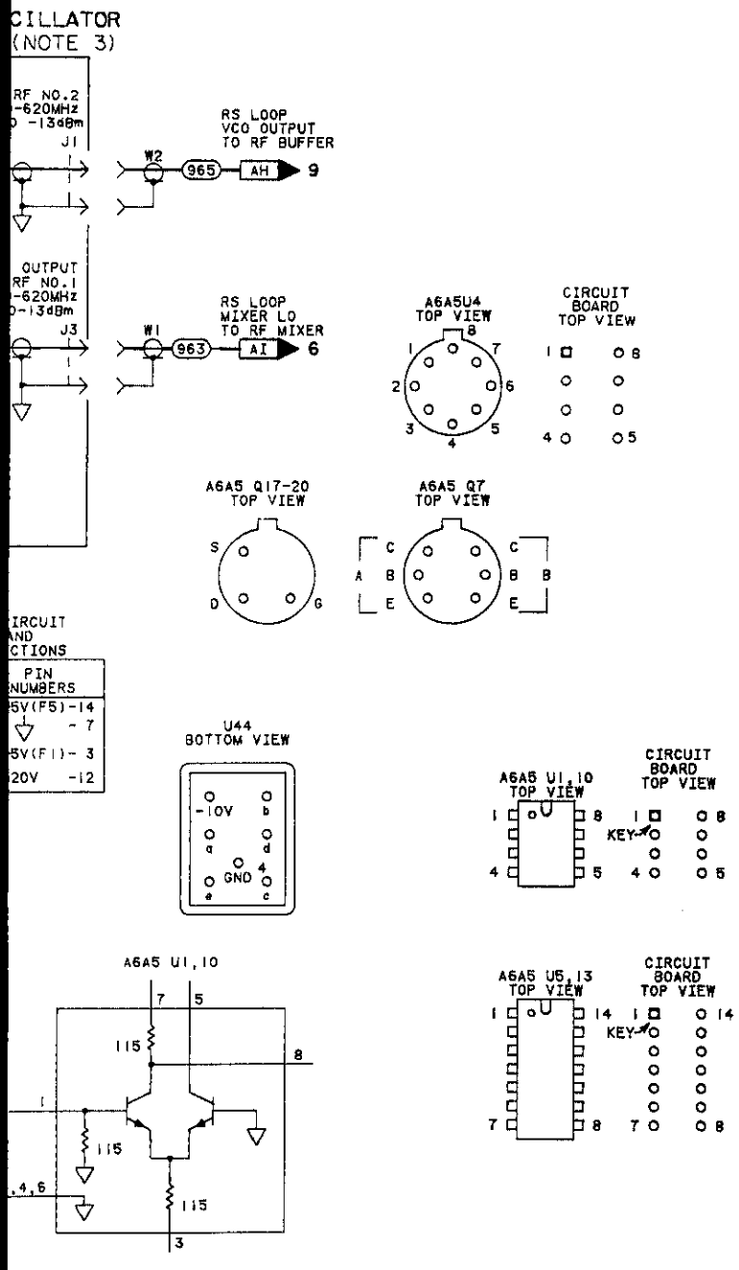




TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q2	1853-0012
Q3	1854-0409
Q5,8,10,12	1853-0451
Q7	1854-0475
Q9	1854-0404
Q11	1853-0007
Q13	1854-0247
Q17,20	1855-0020
U1,10	1826-0372
U4	1826-0013
U5	1820-0668
U13	1826-0138

Fig 8-321
Sht 5 of 5



SERVICE SHEET 7

A6A5, A8A2

Figure 8-321. P/O A6A5 Reference Sum Loop Phase Detector Schematic

SERVICE SHEET 8
P/O A6A5 REFERENCE SUM LOOP PHASE DETECOR ASSEMBLY

REFERENCE BLOCK DIAGRAM 3
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The frequency error-correction circuitry on this board aids the phase lock loop (PLL) in acquiring lock. The first dual CMOS switch (U8) connects the outputs of the limiters to the trigger circuits. The trigger circuits produce TTL signals which are used by the ECL frequency detector when the loop is unlocked. These signals clock the frequency detector, which senses the direction of the frequency offset to determine whether the VCO (service sheet 7) should be driven up or down. The comparator produces a TTL logic level that controls the direction of the VCO frequency change.

The out-of-lock discriminator signal (pin 5 of U11) enables the digital discriminator to clock the mixer difference signal, producing a pulse-width modulated discriminator signal at the output of U12B. This signal is modulated at a frequency which varies from 200 kHz to 2.5 MHz. A resultant signal is generated, and one of the second dual CMOS switches (U7) is activated depending on the direction of the frequency offset.

If the loop is out of lock by more than 2.5 MHz, the correction current stays on continuously. From an offset of 2.5 MHz down to 200 kHz, the correction signals are not necessary and the lock acquisition circuitry is disabled.

Dual CMOS Switch No. 1 (U8)

This dual CMOS switch connects the reference and loop IF signal inputs to the TTL trigger circuits. The switch itself is controlled by the out-of-lock discriminator. It is disabled when the loops are locked, preventing the TTL trigger circuits from being clocked and reducing spurious loop mixer signals.

ECL Frequency Detector

The two output signals from dual CMOS switch No. 1 clock the ECL frequency detector (U2) producing a HI at either pin 4 or pin 11 of the device. A HI at one of the input pins 6 or 9 will produce a HI at the respective output pin. The output pin will remain HI until reset by a HI on the opposite input pin. The output pin will remain HI until reset by a HI on the opposite input pin. It will again go HI with a HI input at its respective input and will reset the opposite output. Therefore, one of the output pins will be mostly HI (with some glitches) while the other will be LO (with some glitches). The output that is HI will depend upon which of the two frequencies is greater (that is, the direction of the frequency offset). The glitches are removed by the differential low-pass filter. When locked, the ECL frequency detector inputs are gated off by U9C and U9D and the two outputs end up in either a LO-HI,HI-LO or LO-LO state.

Comparator

Comparator U3 converts the filtered ECL frequency signal to a clean TTL logic level. This TTL level in turn controls whether the VCO (service sheet 7) is driven up or down. R141 provides a small amount of positive feedback around the comparator. This serves to suppress oscillation by producing a dead zone and latches the comparator when the loop is locked.

Programmable Inverter

The TTL frequency-direction logic level from the comparator is sent through an exclusive-OR gate which acts as a programmable inverter. The RS loop requires a logic inversion here to drive the loop into lock if the VCO frequency is below that required. The OS loop requires no inversion for the feedback level to lock the loop when the frequency is above that of the reference. This is the only difference between the two loops. The state of the programmable inverter is set at pin 5 of the RS and OS loop boards. Pin 5 is allowed to float HI for the Reference Sum Loop assembly (service sheet 8) and is tied LO for the Output Sum Loop assembly (service sheet 12).

7 MHz Low-Pass Filter

When the loop is out of lock, a beat note appears at the output of the mixer (service sheet 7). The 7 MHz low-pass filter removes the sum signal and other mixing products and only allows a beat note below 7 MHz to pass.

150 kHz Active High-Pass Filter

This circuit along with the dead zone in the TTL trigger circuit is used to prevent FM from triggering the out-of-lock circuitry.

Out-Of-Lock Discriminator

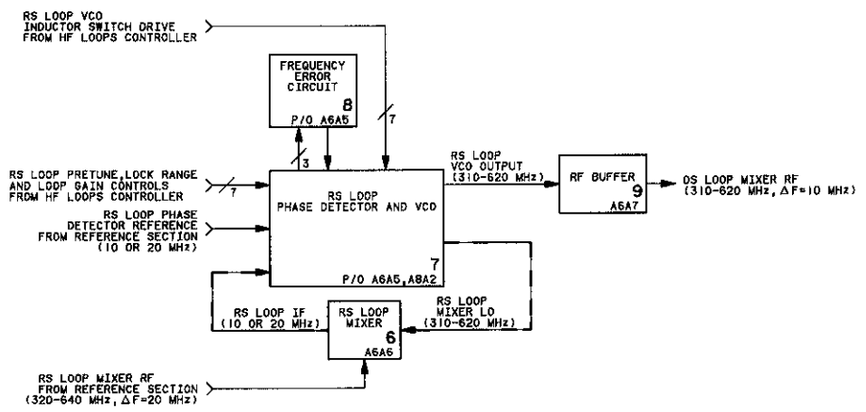
The out-of-lock signal (pin 5 of U11) enables the final stage of the digital discriminator and clocks the difference signal from the mixer. If the difference signal is greater than 200 kHz (<5 us) pin 5 of U11 will always be high, enabling one-shot U12B.

If the loop is out of lock by more than 2.5 MHz (<400 ns) pin 12 of one-shot U12B will always be low enabling the dual-OR gates and current will be on continuously until the offset decreases to 2.5 MHz (400 ns). Between 2.5 MHz and 200 kHz U12B produces 400 ns pulses to modulate the correction current pumped into or out of the RC feedback node. As the offset decreases toward 200 kHz the pulse rate decreases.

When an offset of 200 kHz (5 us) is reached, one-shot U12A and flip flop U11 disable one-shot U12B and the inputs to the ECL frequency detector. At this point the difference signal from the mixer is within the loop bandwidth and the loop will acquire lock by itself.

Dual CMOS Switch No. 2 (U7)

This circuit has one channel activated, depending on the out-of-lock direction of the VCO, by one of the two AND circuits being modulated by the discriminator signal. Thus, current is pumped into or out of the RC feedback node of the op-amp integrator (service sheet 7). This forces the output of the op-amp to ramp up or down in the correct direction toward lock.



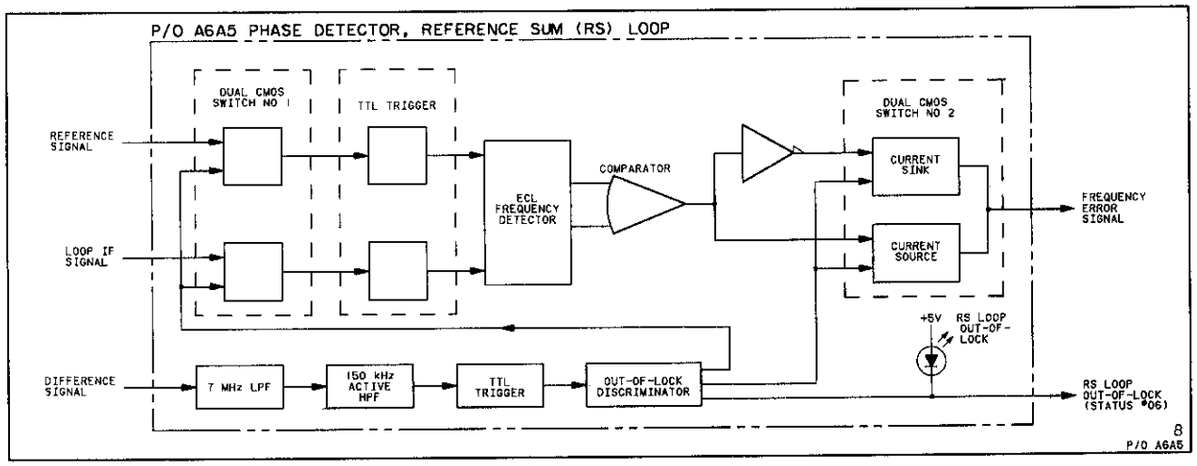


Figure 8-322. P/O A6A5 Reference Sum Loop Phase Detector Block Diagrams

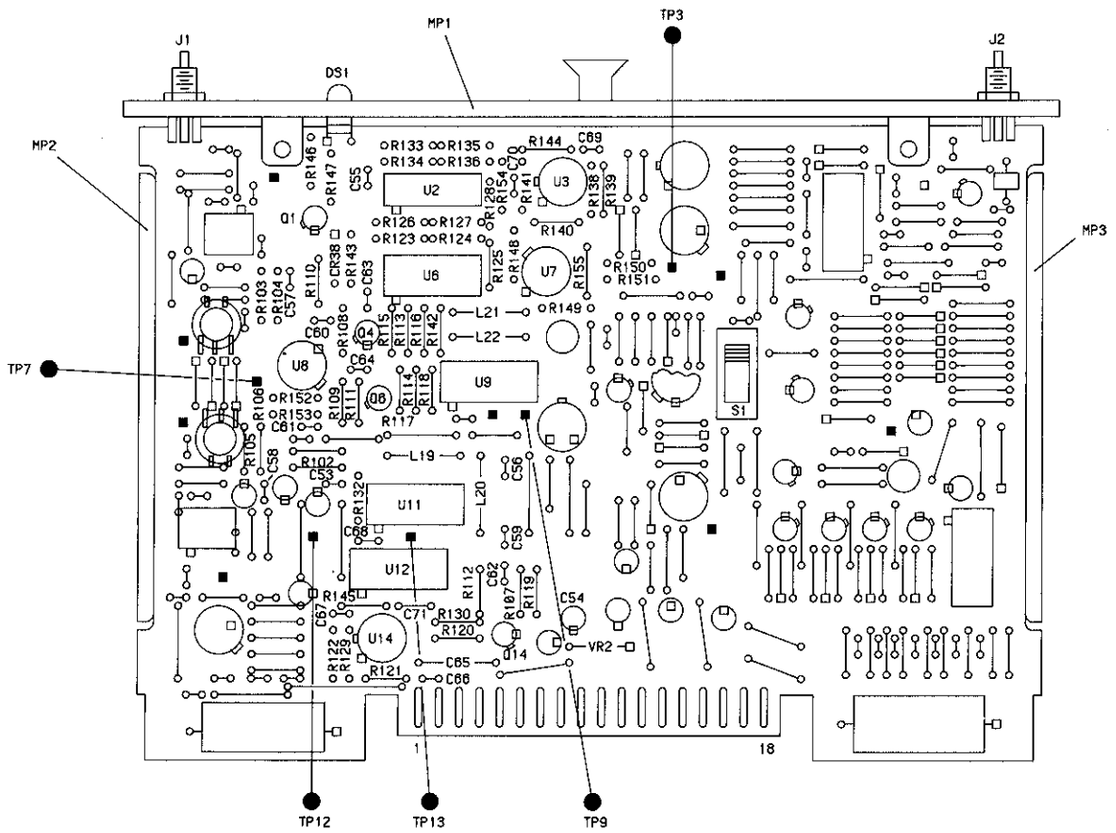


Figure 8-323. P/O A6A5 Reference Sum Loop Phase Detector Component Locator

CHANGES

2516A and Above

On the A6A5 schematic:

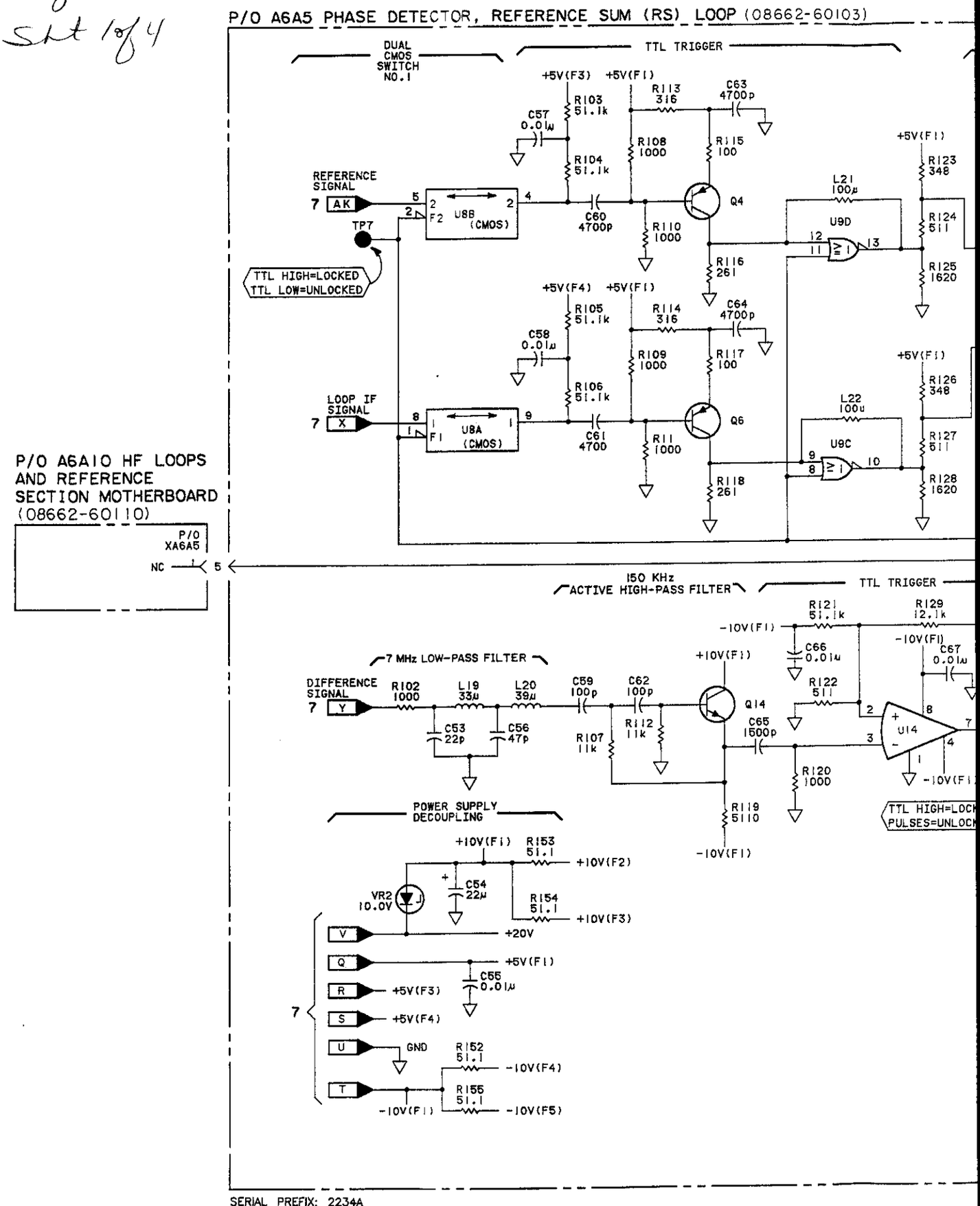
- A6A5R148 - Change the value of R148 to 1.33k.
- A6A5VR2 - Change the value of VR2 to 7.5V.

2706A and Above

On the A6A5 schematic:

- A6A5 - Change the part number of the A6A5 schematic to 08662-60357.

Fig 8-324
Sht 1 of 4



SERIAL PREFIX: 2234A

Fig 8-324 sht 2 of 4

0103)

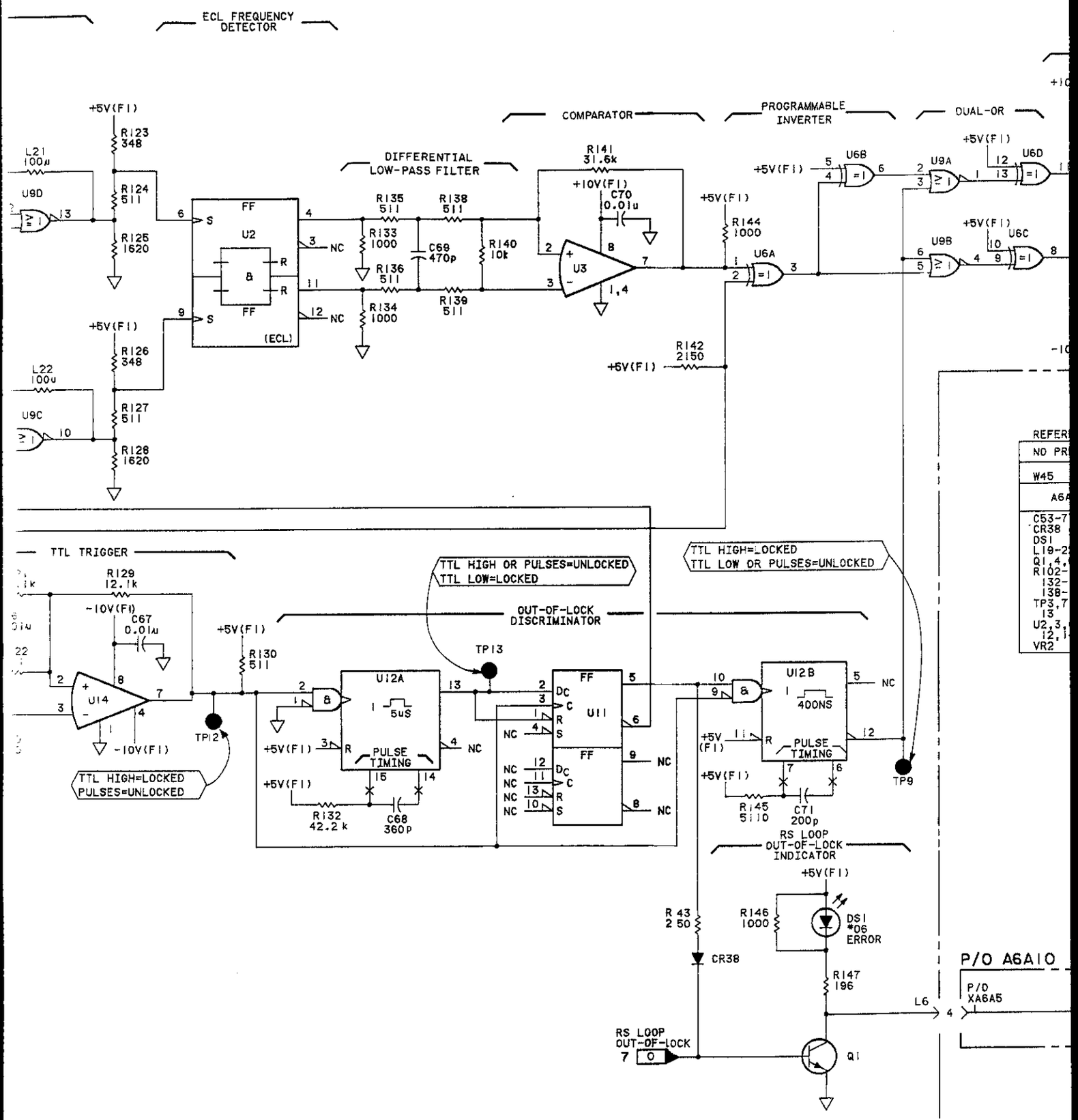
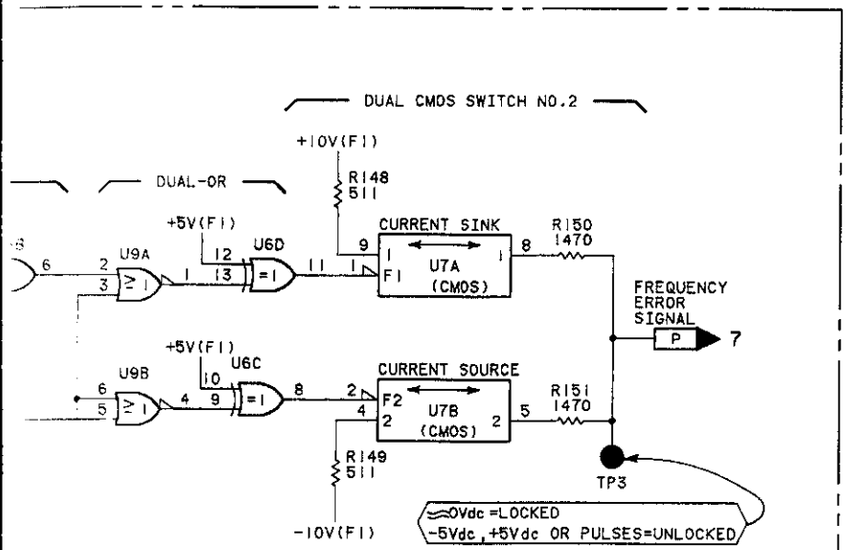


Fig 8-324 Sht 3 of 4



NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NON-STANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS ≥ +4.0V; A LOW LEVEL IS ≤ +3.5V.

REFERENCE DESIGNATIONS

NO PREFIX	A6A10
W45	J1
A6A5	XA6A5
C53-71 CR38 DS1 L19-22 Q1,4,6,14 R102-130, 132-136 138-155 TP3,7,9,12, 13 U2,3,6-9,11 12,14 VR2	

LOGIC LEVELS

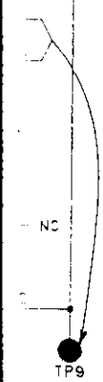
	TTL	ECL (NOTE 3)	CMOS
HIGH	>+2V	>+4.0V	≈VDD
LOW	<+0.8V	<+3.5V	<+0.1V
< IS MORE NEG. THAN > IS MORE POS. THAN			
OPEN	HIGH	LOW	UNDEF.
GROUND	LOW	LOW	LOW

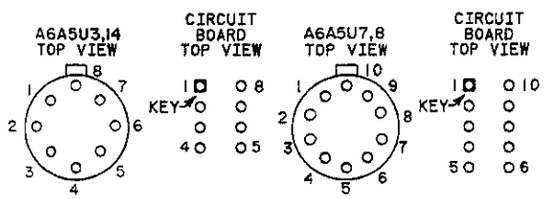
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

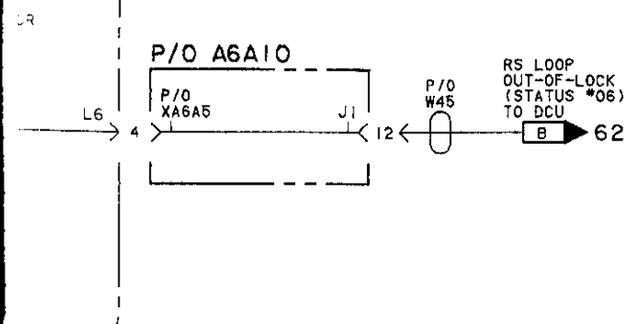
REFERENCE DESIGNATIONS	PART NUMBERS
Q1,14	1854-0404
Q4,6	1853-0007
U2	1820-1344
U3	1826-0026
U6	1820-1211
U7,8	1820-1781
U9	1820-1322
U11	1820-1112
U12	1820-0579
U14	1820-0475

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U2	+5V(F1)-1,14 ▽ - 7 NC-2,5,8, 10,13
U6,9,11	+5V(F1)-14 ▽ - 7
U7	+10V(F3)-10 -10V(F5)-6 ▽ - 3
U8	+10V(F2)-10 -10V(F4) -6 ▽ - 3
U12	+5V(F1) -16 ▽ - 8







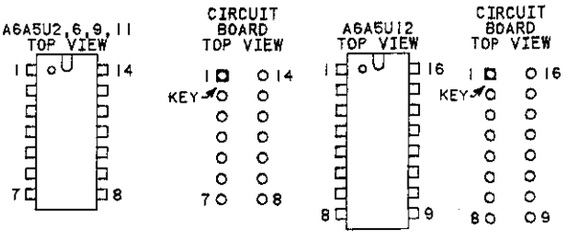
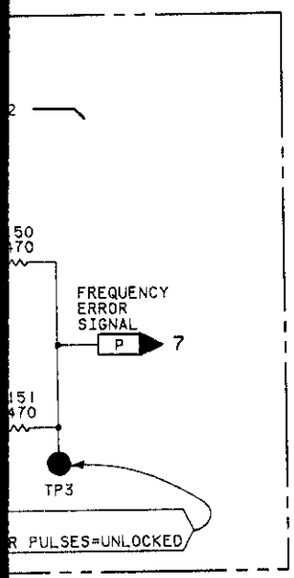


Figure 8-3

Fig 8-324
Sh 4 of 4



NOTES

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LOGIC LEVELS

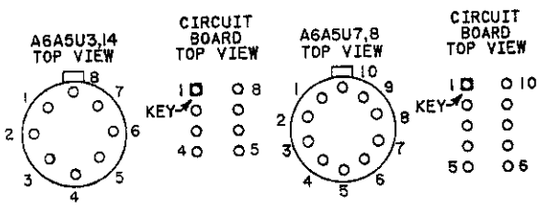
	TTL	ECL (NOTE 3)	CMOS
HIGH	>+2V	>+4.0V	≈VDD
LOW	<+0.8V	<+3.5V	<+0.1V
< IS MORE NEG. THAN > IS MORE POS. THAN			
OPEN	HIGH	LOW	UNDEF.
GROUND	LOW	LOW	LOW

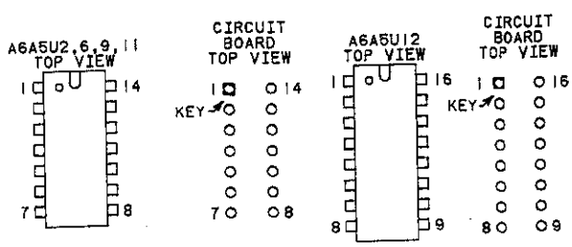
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,14	1854-0404
Q4,6	1853-0007
U2	1820-1344
U3	1826-0026
U6	1820-1211
U7,8	1820-1781
U9	1820-1322
U11	1820-1112
U12	1820-0579
U14	1820-0475

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U2	+5V(F1)-1,14 ⏚ - 7 NC-2,5,8,10,13
U6,9,11	+5V(F1)-14 ⏚ - 7
U7	+10V(F3)-10 -10V(F6)-6 ⏚ - 3
U8	+10V(F2)-10 -10V(F4) -6 ⏚ - 3
U12	+5V(F1) -16 ⏚ - 8





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SERVICE SHEET 8

P/O A6A5

Figure 8-324. P/O A6A5 Reference Sum Loop Phase Detector Schematic

SERVICE SHEET 9
A6A7 RF BUFFER ASSEMBLY

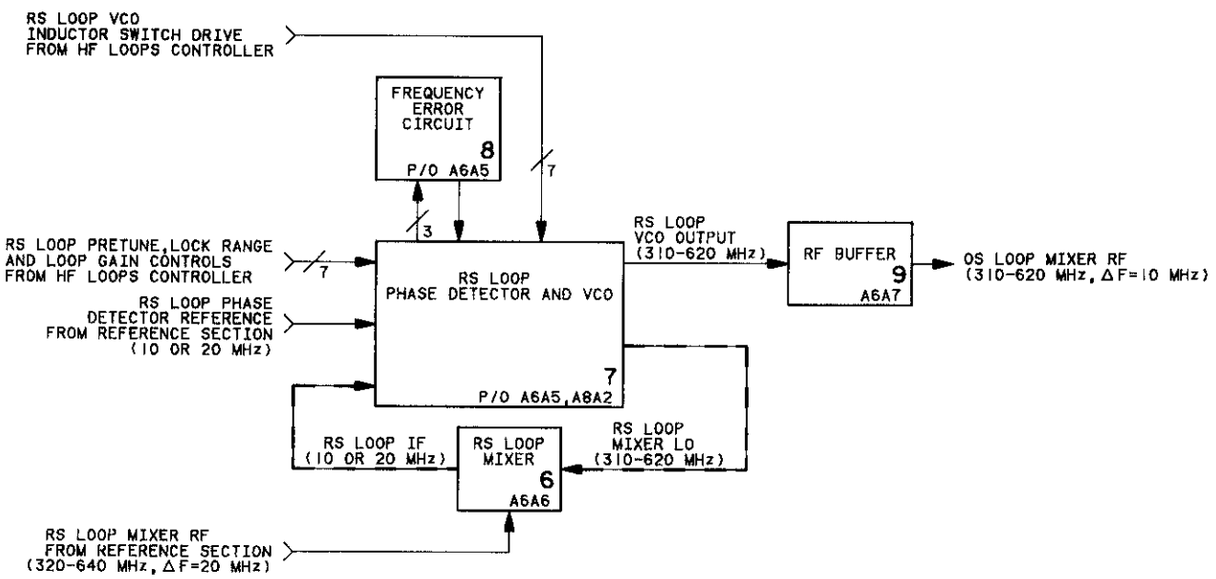
REFERENCE BLOCK DIAGRAM 3
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The RF Buffer Assembly amplifies the 310 MHz to 620 MHz input signal before it is sent to the mixer in the Output Sum Loop. The RF Buffer consists of three limiter stages which provide gain and 75 dB of isolation. Each limiter stage has a gain of about 10 dB and limits at +1 dBm.

The output signal from limiter U3 is sent through a 700 MHz low-pass filter to minimize spurious signals. The level of the output signals from the RF buffer circuit varies from about -2 dBm to -5 dBm. This is due to the high frequency roll-off characteristic of the limiters and the insertion loss of the low-pass filter at higher frequencies.



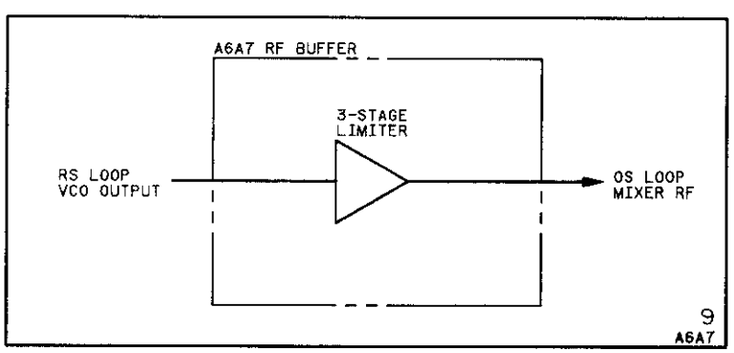


Figure 8-325. A6A7 RF Buffer Block Diagrams

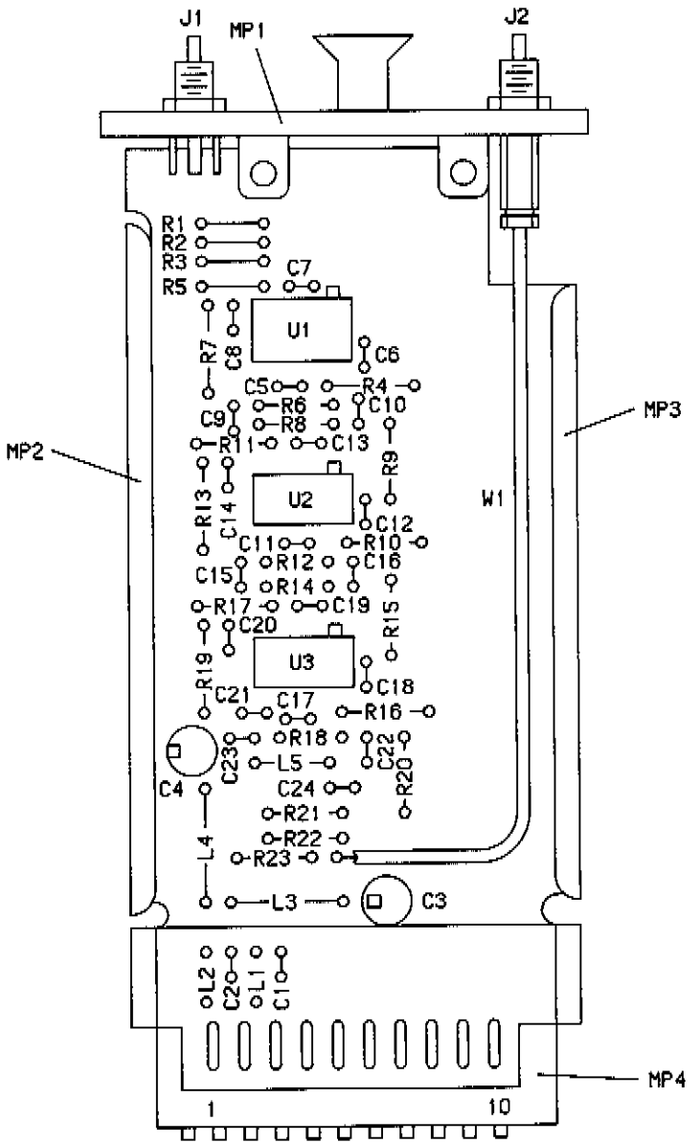
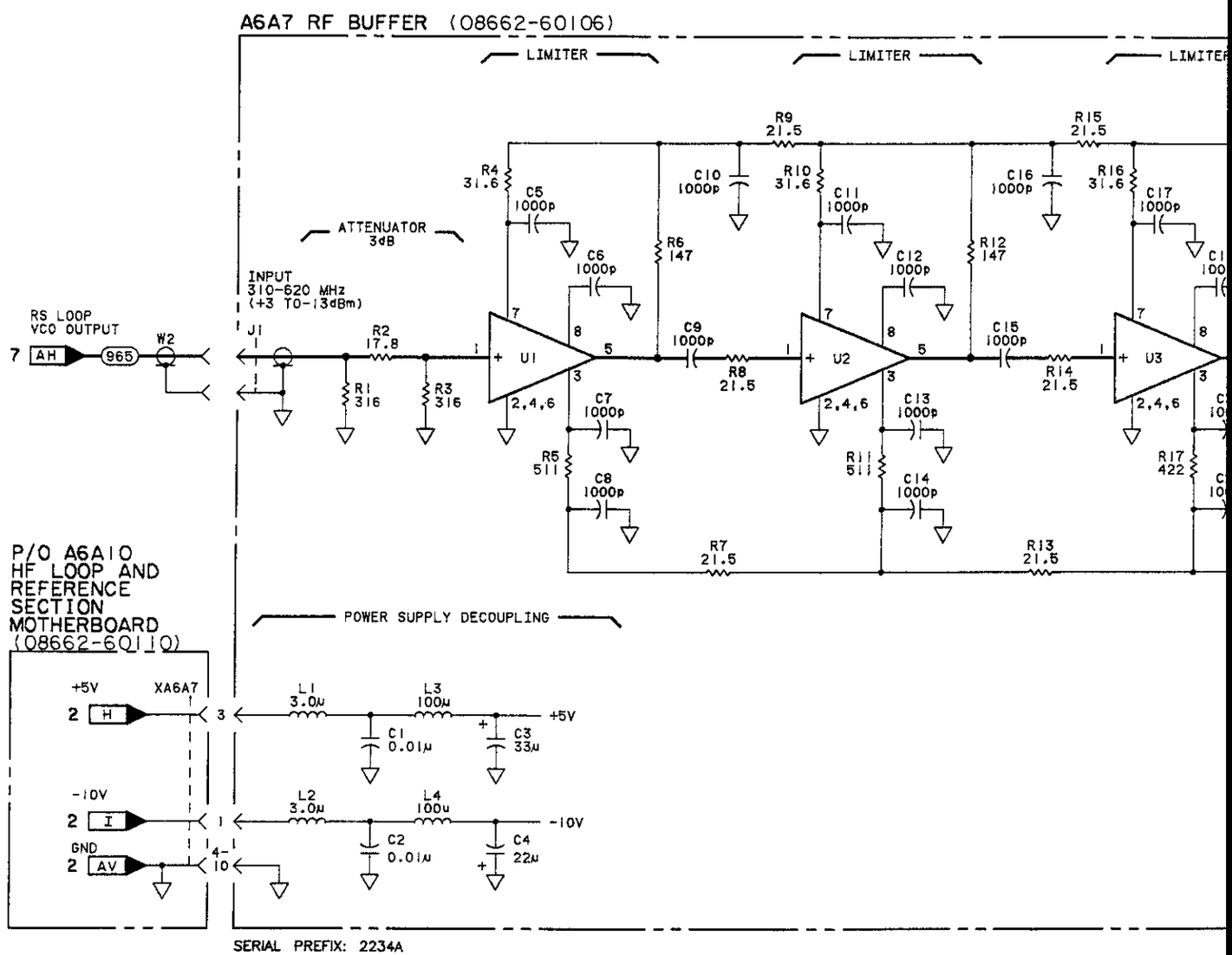


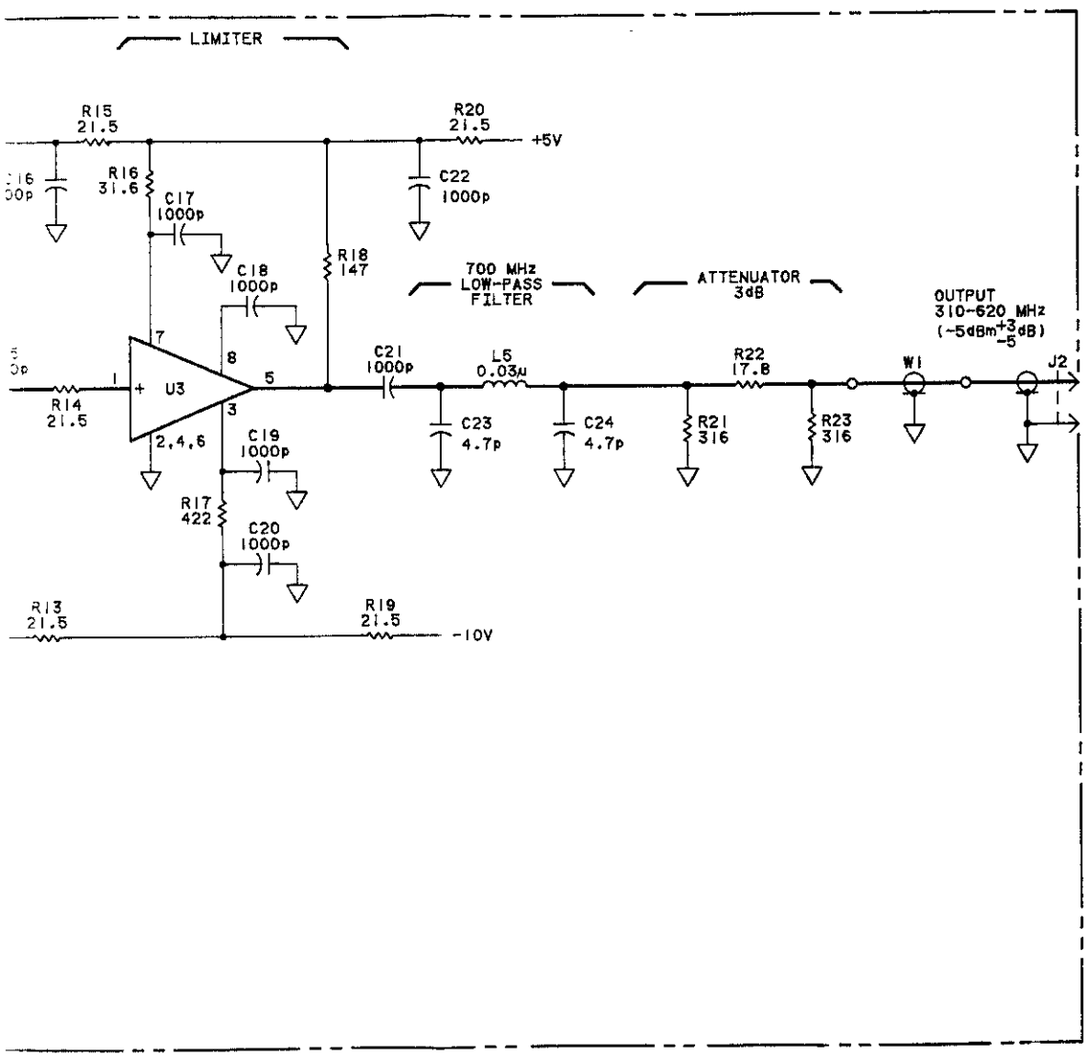
Figure 8-326. A6A7 RF Buffer Component Locator

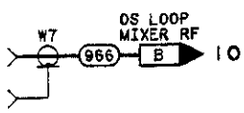
Fig 8-327
Sht 1 of 3



SERIAL PREFIX: 2234A

Fig 8-327
Sht 2 of 3



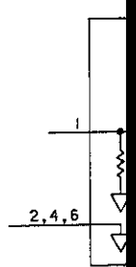


REFERENCE DESIGNATIONS

NO PREFIX	A6A10
W3,7	XA6A7
A6A7	
C1-24 J1-2 L1-5 R1-23 U1-3 W1	

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U1-3	1826-0372



1. R
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2. T
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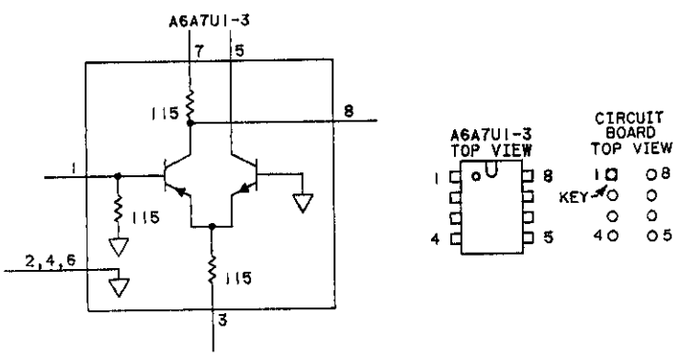
Fig 8-327
Sht 3 of 3

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.



SERVICE SHEET 9

A6A7

Figure 8-327. A6A7 RF Buffer Schematic

SERVICE SHEET 10
A6A8 RF MIXER ASSEMBLY

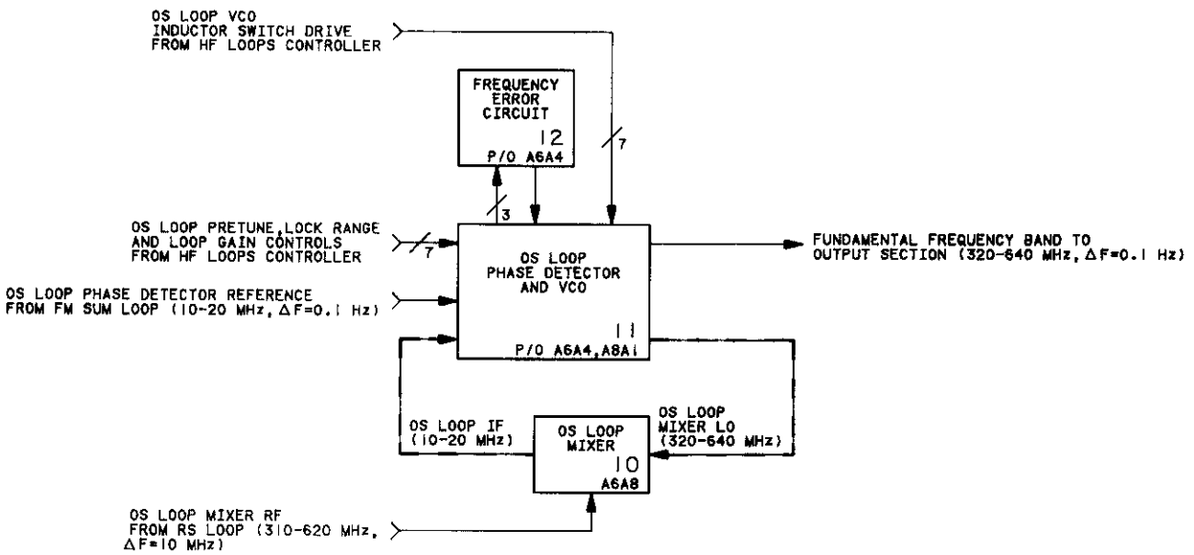
REFERENCE BLOCK DIAGRAM 3
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The RF Mixer combines the 310 MHz to 620 MHz and the 320 MHz to 640 MHz inputs to produce the 10 MHz to 20 MHz loop IF output signal. The two limiter stages serve as buffers and provide a constant level output to amplifier Q1. Each of the limiter stages has a gain of 10 dB and limits at +1 dBm.

The output of limiter U2 is amplified by the single stage common-emitter amplifier, which has an approximate gain of 8 dB. The mixer is a double balanced type (that is, both input signals are suppressed at the output). The output of the mixer contains the sum and difference frequencies of the two input signals at a power level of approximately -16 dBm. The sum signal is filtered by the 25 MHz low-pass filter, leaving only the desired difference signal.



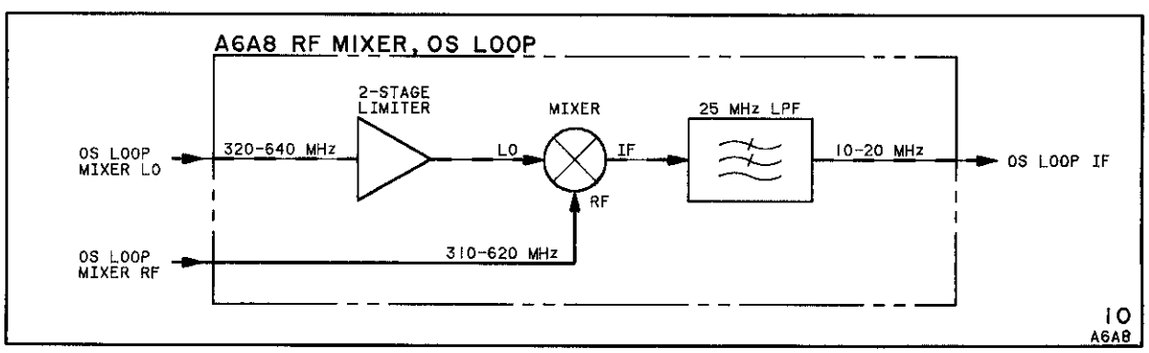


Figure 8-328. A6A8 RF Mixer Block Diagrams

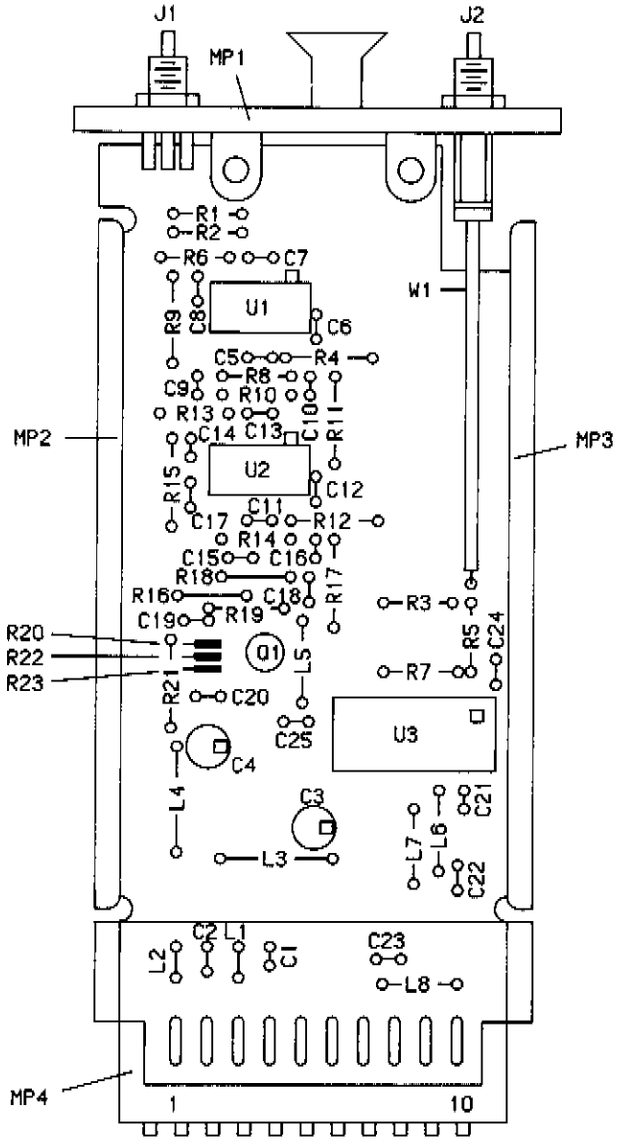
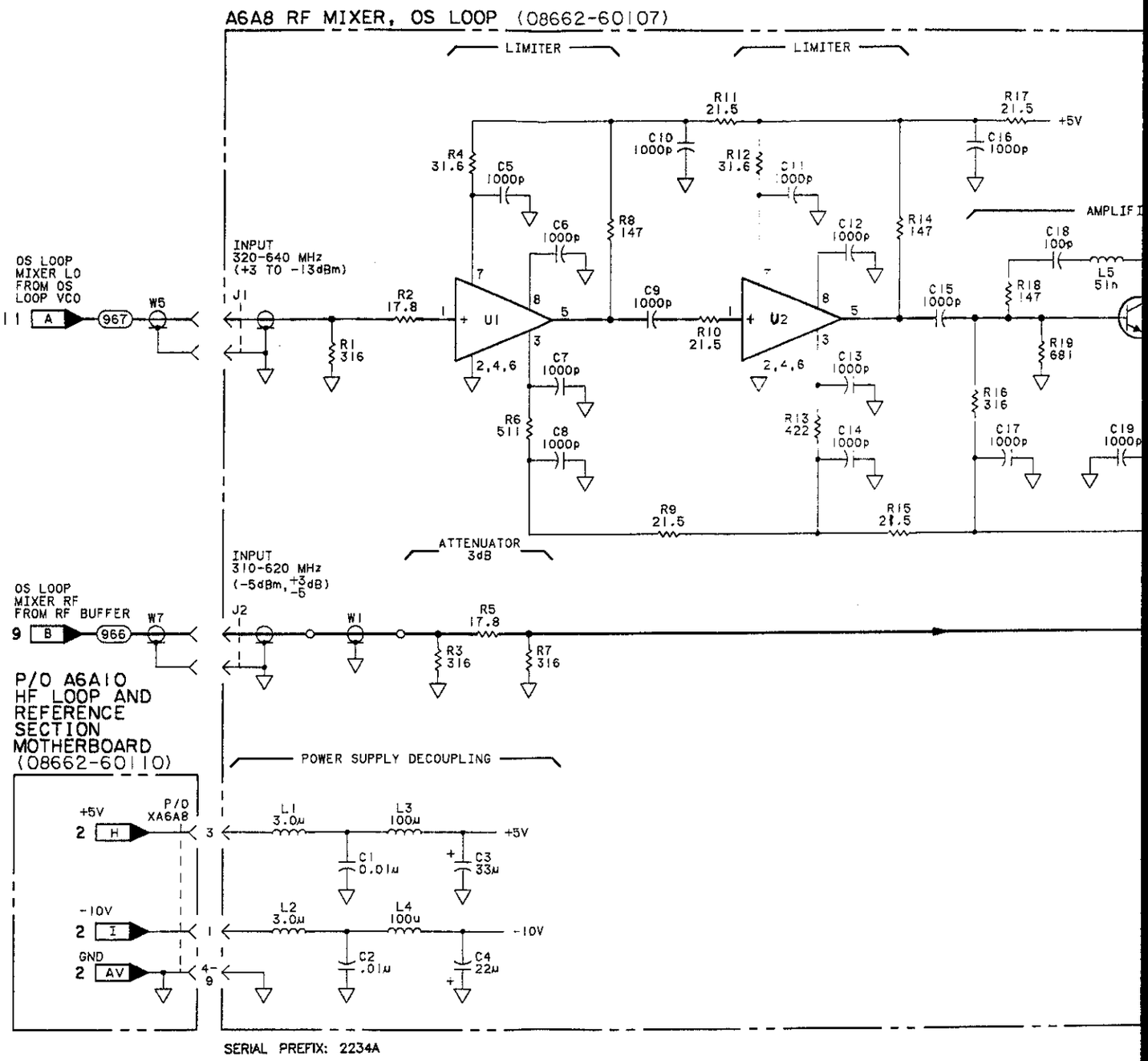


Figure 8-329. A6A8 RF Mixer Component Locator

CHANGES

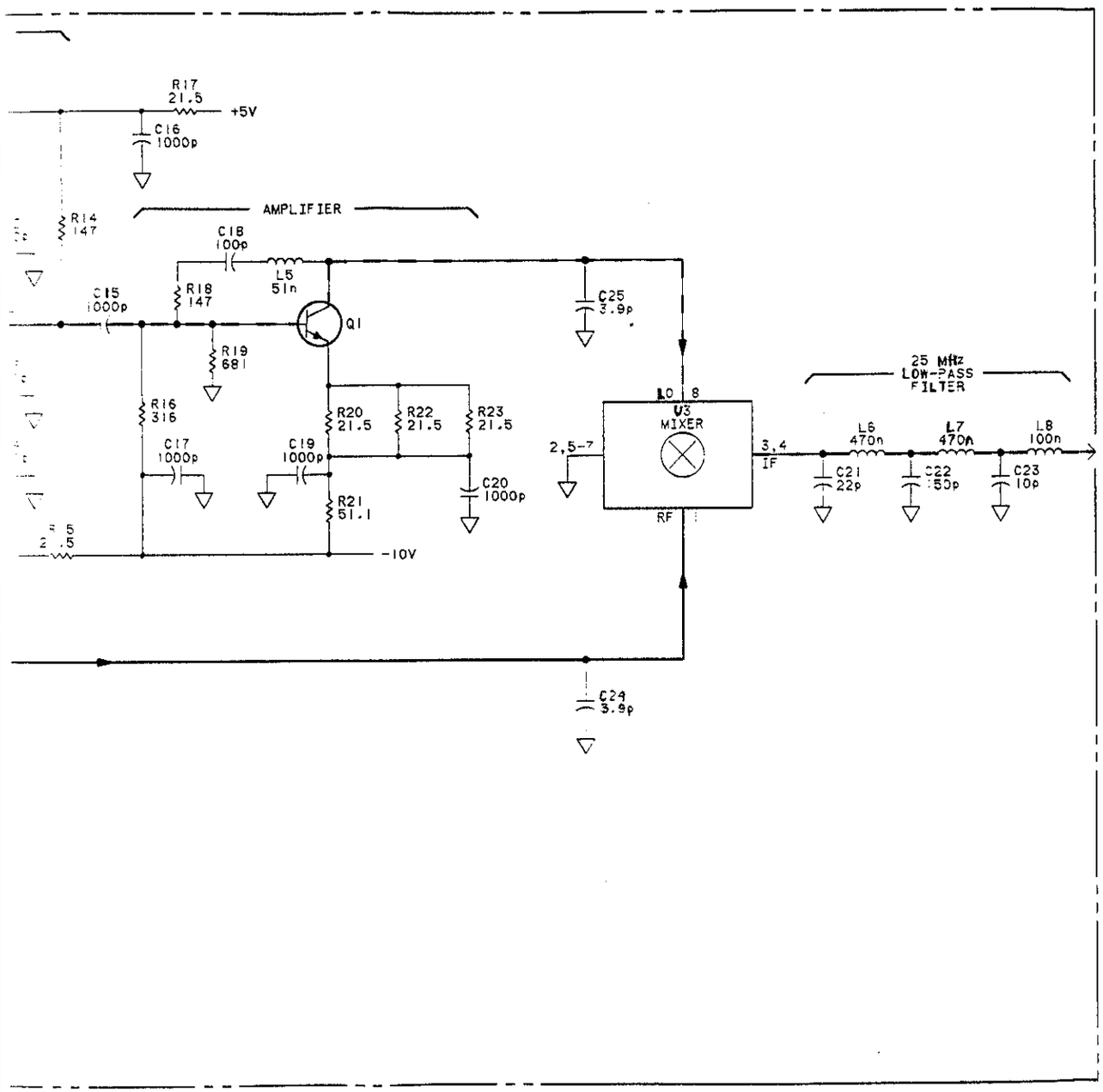
2748A to 2823A	On the A6A8 schematic: • C26 - Add C26 4.7p to ground between R10 and U2.
2837A and above	On the schematic: • C1, C2 - Under **POWER SUPPLY DECOUPLING** change C1 and C2 to 1000pF. • C26, C27 - Under **LIMITER** change the value of C26 to 8.2pF and add C27 8.2pF from ground to the junction of U1 and R2.

Fig 8-330
Sht 1 of 3

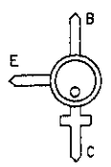


SERIAL PREFIX: 2234A

Fig 8-330
Sht 2 of 3



A6A8Q1
TOP VIEW



NOTE

1. REFER TO TABLE 8-
DIAGRAM NOTES.

2. TROUBLESHOOTING V
THEY ARE ACTUAL M
YOUR MEASUREMENTS
DIFFERENT THAN WH

REFERENCE DESIGNAT

NO PREFIX	A6A
W5,7	XA6A8
A6A8	
C1-25 J1,2 L1-8 Q1 R1-23 U1-3 W1	

Fig 8-330
Sht 3 of 3

NOTES

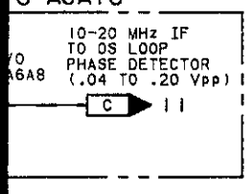
1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

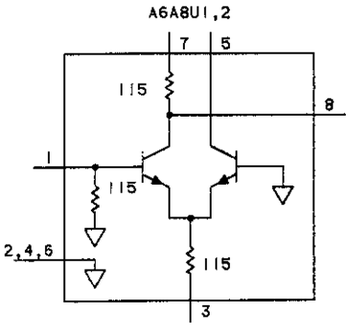
REFERENCE DESIGNATIONS

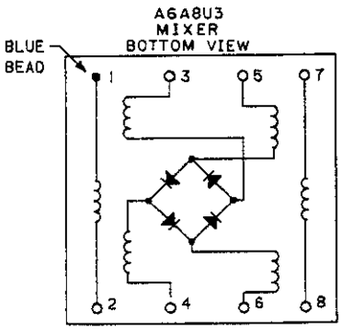
NO PREFIX	A6A10
W5,7	XA6A8
A6A8	
C1-25 J1,2 L1-8 Q1 R1-23 U1-3 W1	

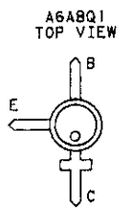
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

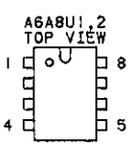
REFERENCE DESIGNATIONS	PART NUMBERS
Q1	1854-0720
U1,2	1826-0372
U3	0955-0096

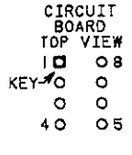












SERVICE SHEET 10

A6A8

Figure 8-330. A6A8 RF Mixer Schematic

SERVICE SHEET 11
P/O A6A4, A8A1 OUTPUT SUM LOOP PHASE DETECTOR AND
VOLTAGE CONTROLLED OSCILLATOR ASSEMBLY

REFERENCE BLOCK DIAGRAM 3
Table 4-1. Recommended Performance Tests
After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The 10/20 MHz loop phase detector reference signal (at J1) and the 10/20 MHz loop IF signal (at board pin 1) are attenuated and amplified, respectively, and are sent to the phase detector formed by CR1, CR2, CR3, and CR4. The phase detector combines the two signals and outputs a difference signal which is filtered by a 5 MHz low-pass filter and a 19 MHz broadband notch filter before entering the integrator formed by Q7, Q8, and Q9.

The integrator output current is converted to voltage by Q10. This voltage is summed with a four-bit ROM-controlled BCD pretune current in the resistor-diode shaper. The resulting voltage is then filtered, buffered, and used to drive the VCO so that it produces linear tuning with constant loop gain.

The frequency range of the integrator voltage is automatically adjusted to maintain a constant lock range for the loop. The long time constants associated with switching the RC loop gain adjust are accelerated by the speed-up circuit during switching.

Loop Reference and IF Limiters

Before the 10/20 MHz loop IF (from the RF mixer) is compared against the 10/20 MHz loop phase detector reference frequency within the double balanced phase detector, the two signals are passed through identical limiters. Prior to entering the limiters, the reference signal is attenuaated by 3 dB and the IF signal is amplified by 8 dB so that the two signals have amplitudes of about -3dBm to -5 dBm. The limiters have adequate gain at this input level to produce sharp limiting action over the 10 MHz to 20 MHz frequency range. The outputs of the limiters are connected to the inputs of center-tapped transformers, together with four PN junction diodes, form the high level mixer/phase detector.

Phase Detector

A high level mixer is used as the phase detector on this board. Switching both sides of the phase detector hard generates a very linear slope. IF signals are suppressed by double balanced action so that the main components at the output are dc phase and two times the IF signal. The two signals from the limiters and the phase detector output signal operate the lock acquisition circuitry.

Integrator

The phase detector's output signal passes through the 5 MHz low-pass filter and a 19 MHz notch filter. The signal which enters the integrator is either an ac difference frequency or a dc voltage (for signals of the same frequency). In this latter case, the dc varies between +-0.6 volts. The integrator has a large dc gain with a zero located at about 7 kHz. The loop locks at a 90° phase difference when the dc voltage reaches 0 volts. The integrator has only one driving input when the difference frequency is less than 200 kHz. This input comes from the 5 MHz low-pass filter. If the difference signal is greater than 200 kHz, an additional drive current (the primary driver at this point) is supplied by the out-of-lock circuitry.

The integrator's output is proportional to the charge across its feedback capacitor. The output level will be between 0 volts and some positive level determined by the lock range limit control and limit detector (set by the controller).

The integrator is actually a discrete component op-amp. It produces output voltages in 8 ranges. These 8 ranges accommodate the widely differing volatge-frequency sensitivity of the VCO caused as various combinations of inductors are switched into the VCO. Gain of the integrator is maximum at dc, but reaches unity between 250 kHz and 500 kHz. The high gain for close-in signals suppresses VCO noise.

Lock Range Limit Control and Out-Of-Lock Detector

As inductors in the VCO are switched ON in parallel, the VCOs sensitivity increases. As the VCO frequency is increased from 310 MHz to 640 MHz by progressively switching in inductors A, B, C, D, and E, the oscillators' gain increases by a factor of four (12dB). To maintain constant lock range, the positive voltage swing of the integrator is limited by a 3-bit D/A converter controlled by the signals that switch inductors C, D, and E, the most significant frequency bits. The output of the D/A resistive ladder drives the out-of-lock circuitry.

The out-of-lock detector (U4) compares the D/A output against the positive swing of the integrator. If the output becomes too positive, an out-of-lock signal is generated. Loss of signal or oscillator-drift, causing the integrator to reach its positive voltage limit, triggers this circuit and causes four things to happen. It lights the out-of-lock LED, sends TTL LO signals back through the motherboard to the microprocessor, enables the first dual CMOS switch and the two TTL trigger circuits, and enables the digital discriminator to clock the mixer beat note, producing a pulse-width modulated discriminator signal.

Resistor Diode Shaping Network

The VCO is controlled by varying the reverse bias on a group of varactor diodes which form part of the oscillator's tank circuit. An increase in reverse bias causes a reduction in junction capacitance, which increases the frequency. However, the frequency characteristic of the tuning circuit is not a linear function of input voltage.

A shaping circuit on the Phase Detector Board is used to linearize the signal. The shaping circuit consists of a ladder of diodes which are reverse biased at successively higher voltages. As the signal level increases, the diodes become progressively forward biased, presenting a lower impedance to the drive source. The tuning curve of the VCO is thus approximated by the shaping circuits in a piecewise linear manner.

4-Bit BCD Pretune

The beat note of the difference of the loop IF down-converted frequency and the reference frequency passes through a 7 MHz low-pass filter to remove the RF sum frequency and leave only the difference frequency. The pretune ensures that this difference frequency will be less than 7 MHz by pretuning within 7 MHz of its locked frequency. The pretune D/A converter is formed by quad comparator U13, JFET switches Q17-Q20, and associated circuitry. The RS loop pretune inputs accept TTL signals from the Controller Assembly (service sheet 5) to control the pretuning. The pretunes are weighted BCD currents of 0.63mA, 1.25mA, 2.50mA, and 5.00mA. R85 allows the pretune currents to be scaled up or down by 7% and allows for minimization of dc offset. The collector of Q12 injects the pretune current into the resistor-diode shaper.

Loop Gain Adjust and Pretune (Speed-Up) Circuitry

The loop gain adjust circuit works on the same principle as the lock range circuit. VCO inductor lines C, D, and E control gates that activate the RC attenuator sections in the loop gain adjust circuit, ensuring that no phase shift occurs at the loop gain crossover frequency. Because of the low frequency and large capacitors, diodes CR29, CR30, CR31, and CR32 are used to speed up charging of these capacitors during switching. R95 and C49 keep loop gain as constant as possible with any combination of inductors A, B, C, D, and E switched on.

VCO (A8A2)

The VCO in the high frequency loop sections is a non-field-repairable assembly; it is sealed and can only be repaired at the factory. The VCO is coarsely tuned by a 5-bit code which switches inductors A, B,,C, D, and E inside the VCO. A control voltage of -9 Vdc to -38 Vdc fine tunes the VCO to lock the loop. The output frequency of the VCO extends from 310 MHz to 620 MHz, at +3 dBm to -13 dBm (level depends on frequency).

TROUBLESHOOTING

When a high frequency loops problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

1. Mount the A6A5 assembly on an extender board. Move the slide switch to the TEST position (up). This opens the loop.

2. Set the front panel frequency setting to 510.0 MHz. Connect a counter to the front panel RF output of the generator Connect the output of an adjustable power supply to A6A4:
   + terminal to TP14
   - terminal to TP1 (ground).

3. Set the power supply output voltage to approximately 4 volts. The counter should read close to 510 MHz. Slowly decrease the poser supply output to zero, and then increase the voltage to +8V. Check that the frequency changes as shown in the table, below. Voltage and frequency readings may not be exactly as shown, but the amount and direction of change should be similar to these values.

Voltage to TP14 (Vdc)	TP2 (Vdc)	VCO Frequency (MHz)
0.0	-21.7	516.0
4.0	-17.1	509.6
8.0	-13.8	503.5

If these readings are correct, continue troubleshooting with step 4. Otherwise, there is a problem from TP14 to TP2. Troubleshoot to find the cause.

4. Monitor TP8 with the high impedance input of a counter. The counter should read the difference signal from the phase detector. Vary the adustable power supply so the RF output frequency varies above and below 510 MHz. The counter should read the absolute frequency error.

   If operation of this circuit is normal, continue troubleshooting with step 5. Otherwise, there is a problem with the phase detector circuitry.

5. Monitor TP7 (service sheet 12) with an oscilloscope or TTL logic probe. Vary the adjustable power supply so the RF output varies above and below 510 MHz. TP7 should be a TTL logic high (>2.4 Vdc) when the RF output is within 200 kHz of 510 MHz. At more than 510.2 and less than 509.8 MHz, TP7 should become a TTL logic low (<0.8 Vdc).

   If operation of this circuit is normal, continue troubleshooting with step 6. Otherwise, there is a problem with the out-of-lock discriminator circuitry (bottom half of service sheet 12). Troubleshoot this circuitry to find the cause.

6. Monitor U3 pin 7 (service sheet 12) with a scope. Vary the adjustable power supply so the RF output is less than 510.3 MHz. The output of U3 should be less than 0.5 Vdc.

   Increase the RF output frequency to more than 509.7 MHz. The output of U3 should be more than 3.5 Vdc.

   If operation of this circuit is normal, continue troubleshooting with step 7. Otherwise, there is a problem with the frequency detector circuitry (top half of service sheet 12). Troubleshoot this circuitry to find the cause.

7. Monitor TP3 (service sheet 12) with an oscilloscope. Vary the adjustable power supply to increase the frequency of the RF output to more than 511.0 MHz. The signal at TP3 should be a dc level more negative than -3.0 Vdc. This level will become more negative as the RF output frequency increases.

Decrease the frequency of the VCO to less than 509.0 MHz. The signal at TP3 should be a series of pulses with slow rise and fall times at about a +4 Vdc level. The level increases and the pulses get smaller as the RF output frequency decreases.

If operation of this circuit is normal, continue troubleshooting with step 8. Otherwise, there is a problem with the CMOS switch (U7) or the circuitry that drives it. Troubleshoot this circuitry to find the cause.

8. Monitor TPA (output of integrator) with an oscilloscope. Vary the adjustable power supply to make the frequency of the VCO signal greater than 511.0 MHz. The waveform at TPA should be a dc level greater than +7.0 Vdc. Decrease the VCO frequency to less tan 499.9 MHz. The waveform at TPA should be a dc level near ground. Pulse like those seen on TP3 may be visible on either of these levels.

   If these waveforms are not normal, there is a problem with the integrator circuitry.

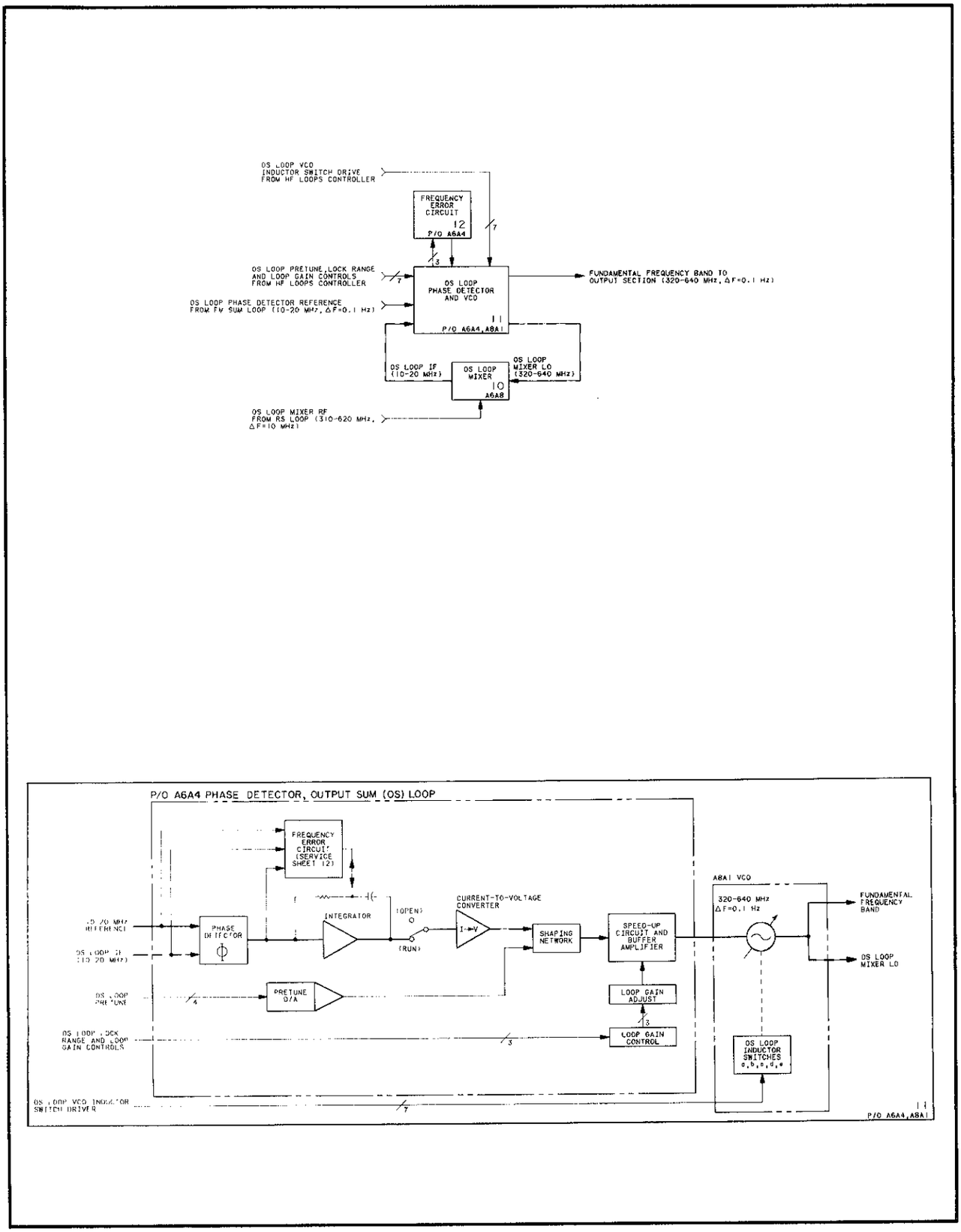


Figure 8-331. P/O A6A4, A8A1 Output Sum Loop Phase Detector & Voltage Controlled Oscillator Block Diagrams

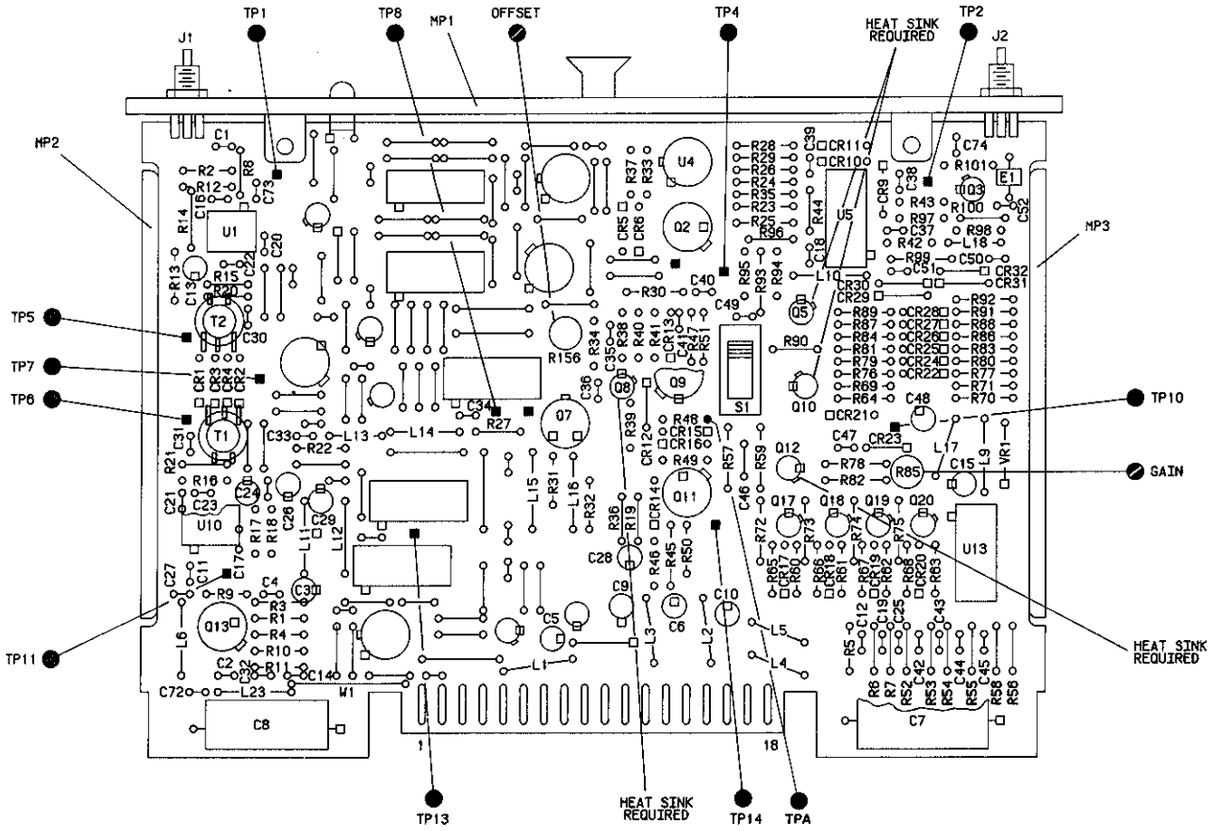


Figure 8-332. P/O A6A4, A8A1 Output Sum Loop Phase Detector & Voltage Controlled Oscillator Component Locator

CHANGES

2601A and above	On the A6A4 schematic: • A6A4Q7 - In the "Table of Transistor and Integrated Circuit Part Numbers", change the part number of Q7 to 1854-1046.
2706A and above	On the A6A4 schematic: • A6A4 - Change the part number of the A6A4 schematic to 08662-60358.
2823A and above	On the A8A1 schematic: • A8A1 - Change the part number of the A8A1 schematic to 08662-60401.
2837A and above	On the A6A4 Component Locator: • R2, R8, R12 - In the left hand corner of the component locator change R2 to C75, R8 to L24, and, delete R12. On the A6A4 schematic: • R2, R8, R12 - In the upper left hand corner of the schematic change **ATTENUATOR 3dB to 25 MHz LOW PASS FILTER.** Delete R2, R8, and, R12. Add C75 100p to ground in place of R2 and add L24 560 nH in place of R8.

Fig 8-333
Sht 1 of 5

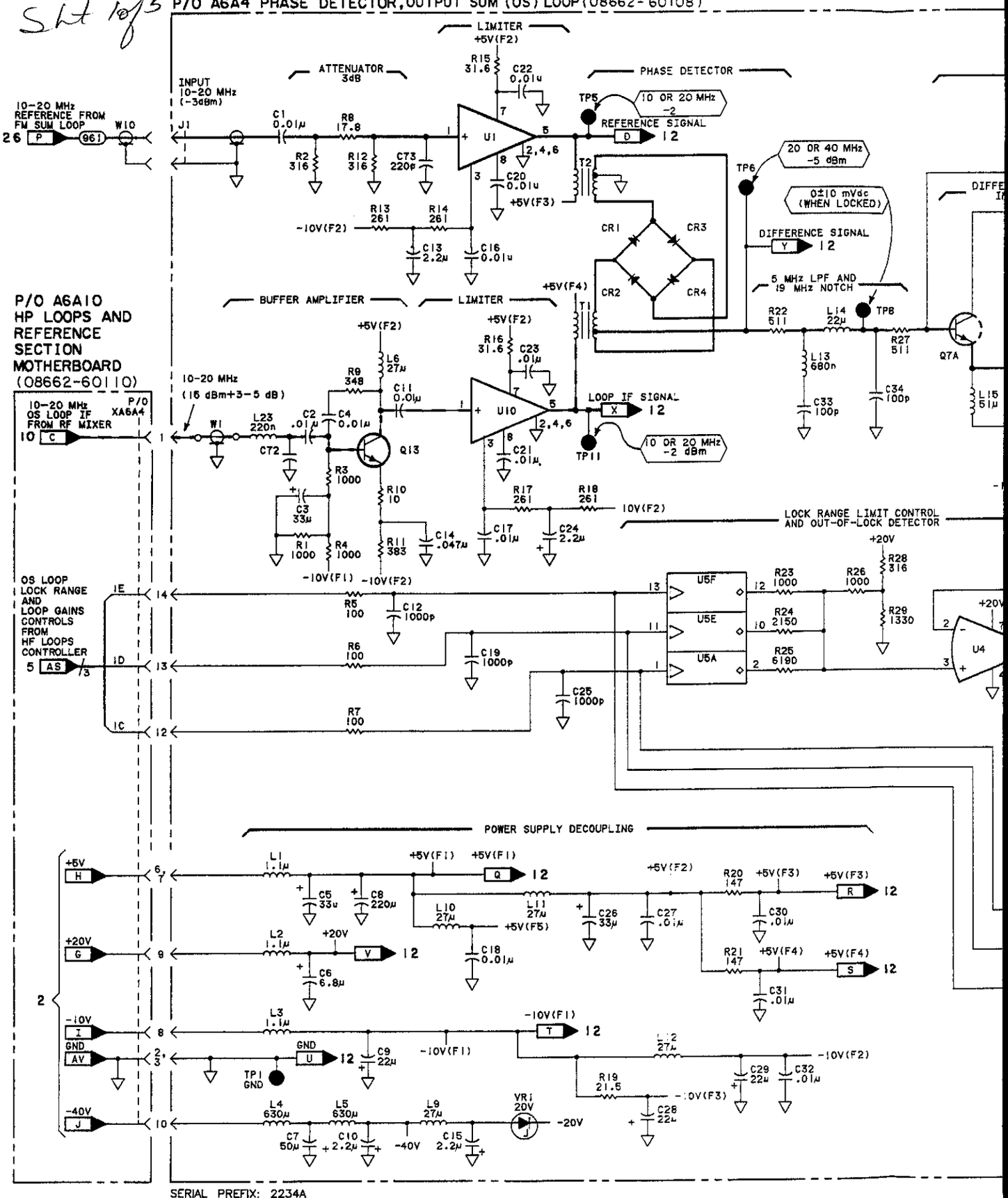


Fig 8-333 Sht 2 of 5

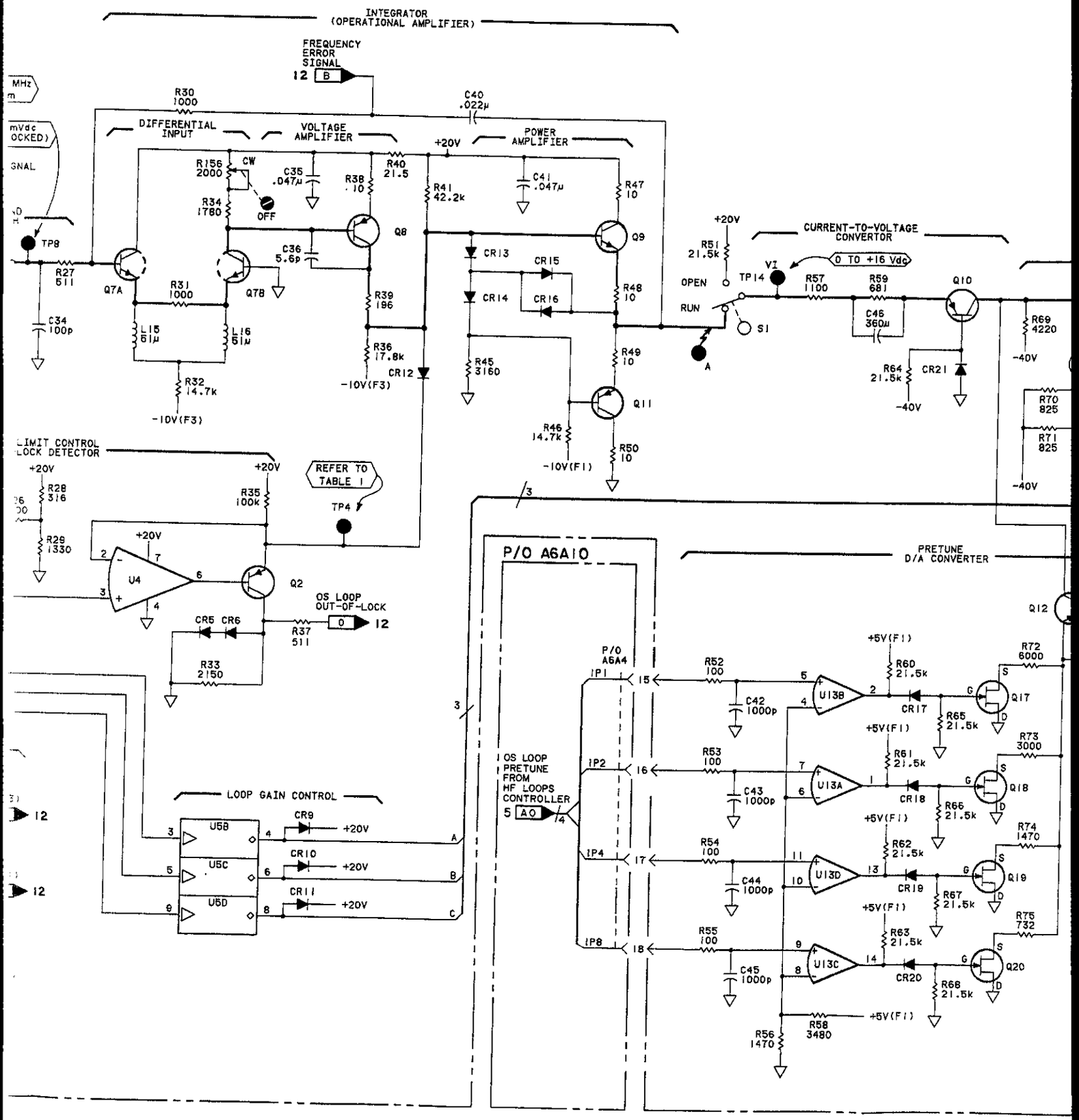
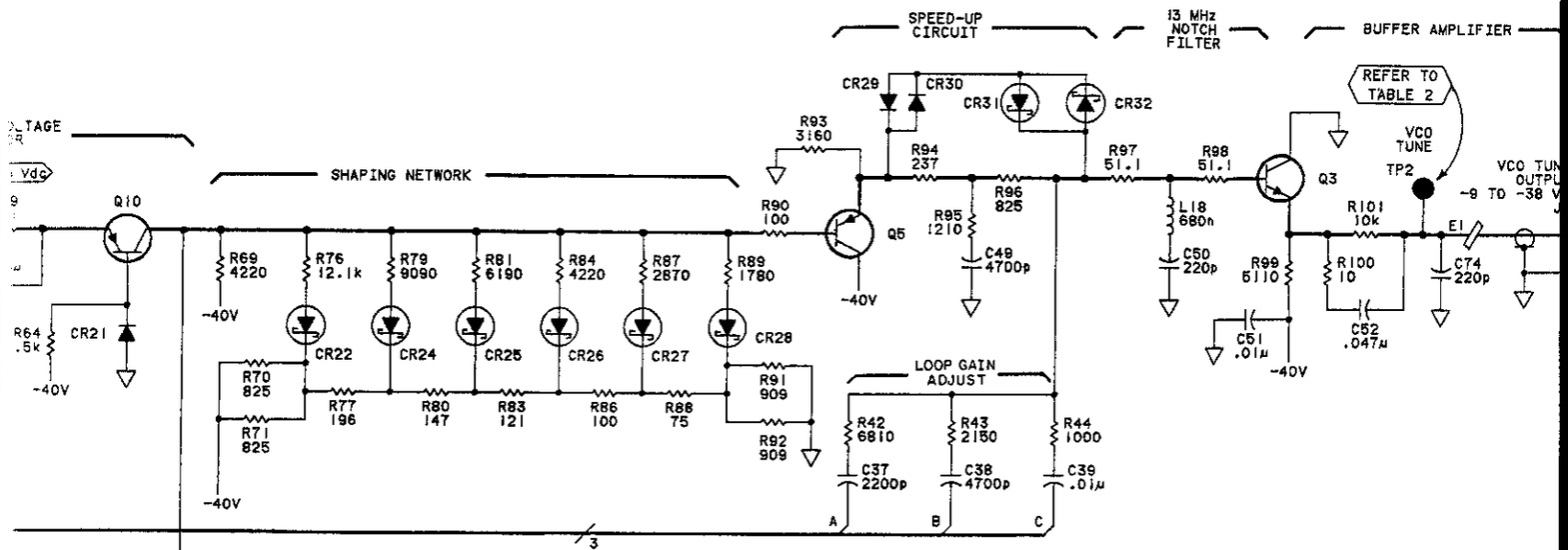
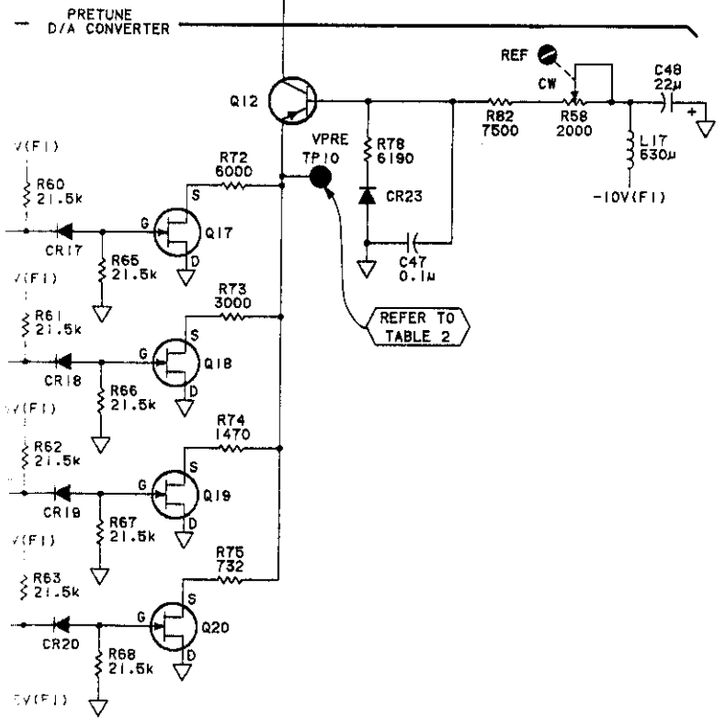


Fig 8-333 Sht 3 of 5





NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. THE A8A1 VOLTAGE CONTROLLED OSCILLATOR HAS SEVERAL ADJUSTMENTS WHICH ARE NOT RECOMMENDED FOR FIELD ADJUSTMENT. THESE ADJUSTMENTS SHOULD ONLY BE PERFORMED AT THE FACTORY

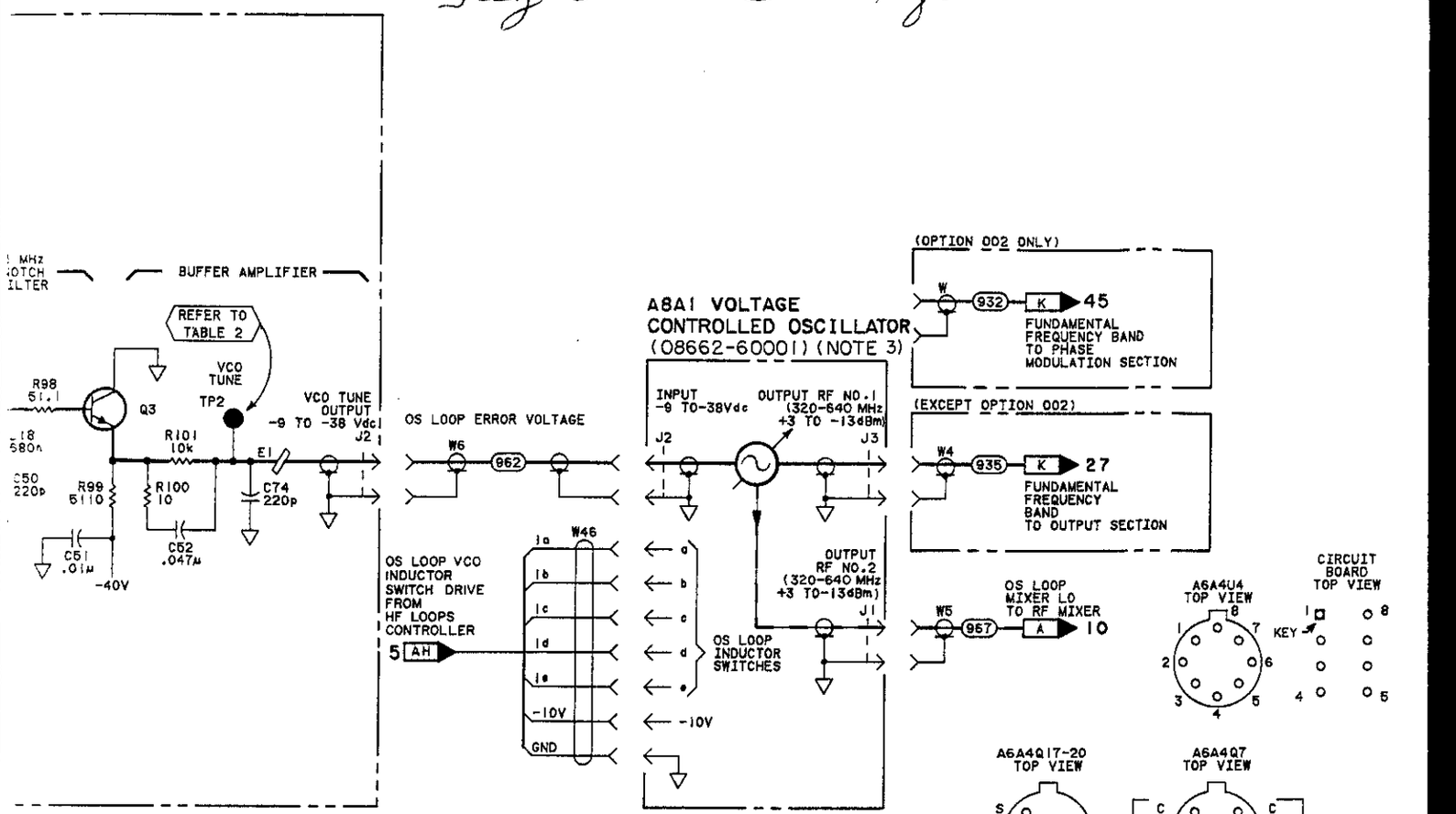
LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

REFERENCE DESIGNATIONS

NO PREFIX	A6A10
W4-6,10,46	XA6A4
A6A4	A8A1
C1-52,72-74 CR1-6,9-32 E1 J1,2 L1-6,9-18,23 Q2,3,5,7-13,17-20 R1-101,156 S1 T1,2 TP1,2,4-6,8,10,11,14 U1,4,5,10,13 VR1 W1	J1-3

Fig 8-333 Sht 4 of 5



LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW

TABLE 1.
LOCK RANGE LIMIT CONTROL CHECK

FRONT PANEL FREQUENCY SETTING (MHz)	ACTIVE INPUTS	TP4 (Vdc)
320	NONE	16.1
360	IC	13.4
410	ID	10.2
510	IE	7.2
612	ALL	5.4

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U5	+5V(F5)-14 ▽ - 7
U13	+5V(F1)- 3 -20V -12

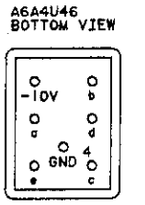
TABLE 2. PRETUNE CHECK

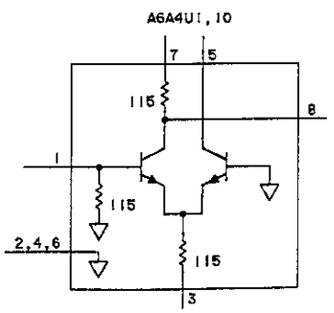
FRONT PANEL FREQUENCY SETTING (MHz)	PRETUNE BIT ON	TP10 (Vdc)	TP2* (Vdc)
524	NONE	-4.09	-36.1
523	IP1	-3.88	-33.4
521	IP2	-3.87	-30.8
517	IP4	-3.84	-26.3
511	IP8	-3.81	-19.8
452	ALL	-3.74	-13.0

*SET SWITCH S1 IN TEST POSITION TO MEASURE VOLTAGE AT TP2

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q2	1853-0012
Q3	1854-0408
Q5,8,10,12	1853-0451
Q7	1854-0475
Q9	1854-0404
Q11	1853-0007
Q13	1854-0247
Q17-20	1855-0020
U1,10	1826-0372
U4	1826-0013
U5	1820-0668
U13	1826-0138





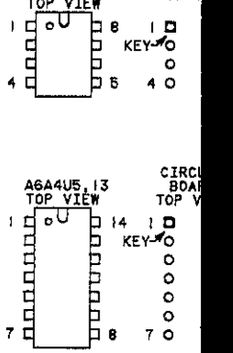
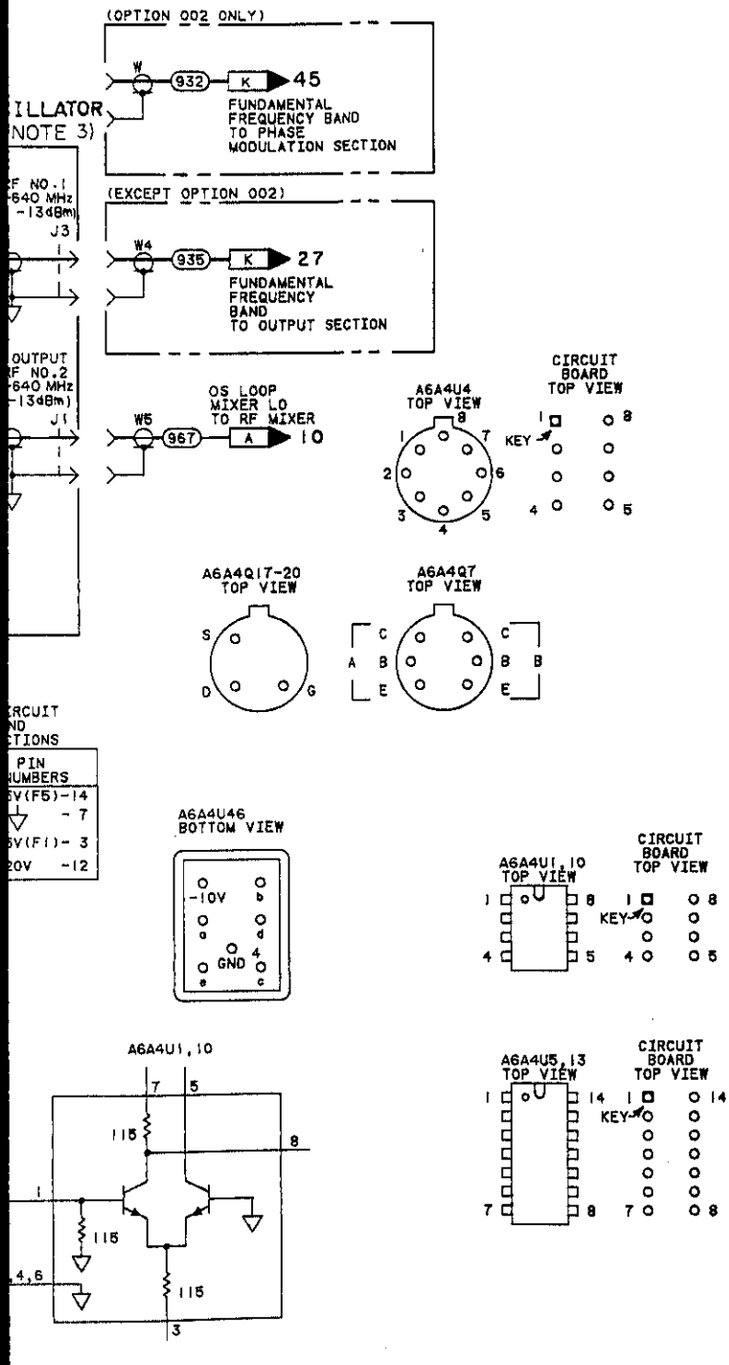


Fig 8-333
Sht 5 of 5



SERVICE SHEET 11

P/O A6A4, A8A1

Figure 8-333. P/O A6A4, A8A1 Output Sum Loop Phase Detector & Voltage Controlled Oscillator Schematic

SERVICE SHEET 12
P/O A6A4 OUTPUT SUM LOOP PHASE DETECTOR ASSEMBLY

REFERENCE BLOCK DIAGRAM 3
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The frequency error-correction circuitry on this board adis the phase lock loop (PLL) in acquiring lock. The first dual CMOS switch (U8) connects the outputs of the limiters to the trigger circuits. The trigger circuits produce TTL signals which are used by the ECL frequency detector when the loop is unlocked. These signals clock the frequency detector, which senses the direction of the frequency offset to determine whether the VCO (service sheet 11) should be driven up or down. The comparator produces a TTL logic level that controls the direction of the VCO frequency change.

The out-of-lock discriminator signal (pin 5 of U11) enables the digital discriminator to clock the mixer difference signal, producing a pulse-width modulated discriminator signal at the output of U12B. This signal is modulated at a frequency which varies from 200 kHz to 2.5 MHz. A resultant signal is generated, and one of the second dual CMOS switches (U7) is activated depending on the direction of the frequency offset.

If the loop is out of lock by more than 2.5 MHz (400 ns), the correction current stays on continuously. From an offset of 2.5 MHz down to 200 kHz, the discriminator modulates the correction current. This speeds up switching time by a factor of two or three. Under 200 kHz (5 us) the correction signals are not necessary and the lock acquisition circuitry is disabled.

Dual CMOS Switch No. 1 (U8)

This dual CMOS switch connects the reference and loop IF signal inputs to the TTL trigger circuits. The switch itself is controlled by the out-of-lock discriminator. It is disabled when the loops are locked, preventing the TTL trigger circuits from being clocked and reducing spurious loop mixer signals.

ECL Frequency Detector

The two output signals from dual CMOS switch No. 1 clock the ECL frequency detector (U2) producing a HI at either pin 4 or pin 11 of the device. A HI at one of the input pins 6 or 9 will produce a HI at the respective output pin. The output pin will remain HI until reset by a HI on the opposite input pin. It will again go HI with a HI input at its respective input and will reset the opposite output. Therefore, one of the output pins will be mostly HI (with some glitches) while the other will be LO (with some glitches). The output that is HI will depend upon which of the two frequencies is greater (that is, the direction of the frequency offset). The glitches are removed by the differential low-pass filter. When locked, the ECL frequency detector inputs are gated off by U9C and U9D and the two outputs end up in either a LO-HI,HI-LO or LO-LO state.

Comparator

Comparator U3 converts the filtered ECL frequency signal to a clean TTL logic level. This TTL level in turn controls whether the VCO (service sheet 11) is driven up or down. R141 provides a small amount of positive feedback around the comparator. This serves to suppress oscillation by producing a dead zone and latches the comparator when the loop is locked.

Programmable Inverter

The TTL frequency-direction logic level from the comparator is sent through an exclusive-or gate which acts as a programmable inverter. The RS loop requires a logic inversion here to drive the loop into lock if the VCO frequency is below that required. The OS loop requires no inversion for the feedback level to lock the loop when the frequency is above that of the reference. This is the only difference between the two loops. The state of the programmable inverter is set at pin 5 of the RS and OS loop boards. Pin 5 is allowed to float HI for the Reference Sum Loop assembly (service sheet 8) and is tied LO for the Output Sum Loop assembly (service sheet 12).

7 MHz Low-Pass Filter

When the loop is out of lock, a beat note appears at the output of the mixer (service sheet 11). The 7 MHz low-pass filter removes the sum signal and other mixing products and only allows a beat note below 7 MHz to pass.

150 kHz Active High-Pass Filter

This circuit along with the dead zone in the TTL trigger circuit is used to prevent FM from triggering the out-of-lock circuitry.

Out-Of-Lock Discriminator

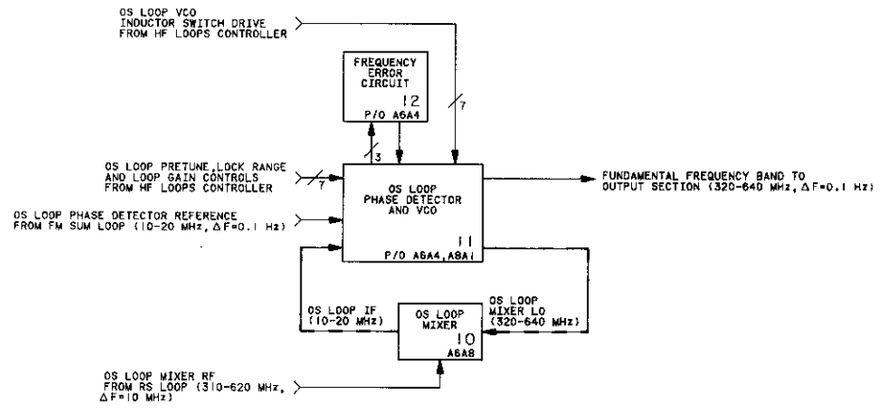
The out-of-lock signal (pin 5 of U11) enables the final stage of the digital discriminator and clocks the difference signal from the mixer. If the difference signal is greater than 200 kHz (<5 us) pin 5 of U11 will always be high, enabling one-shot U12B.

If the loop is out of lock by more than 2.5 MHz (<400 ns) pin 12 of one-shot U12B will always be low enabling the dual-OR gates and current will be on continuously until the offset decreases to 2.5 MHz (400 ns). Between 2.5 MHz and 200 kHz U12B produces 400 ns pulses to modulate the correction current pumped into or out of the RC feedback node. As the offset decreases toward 200 kHz the pulse rate decreases.

When an offset of 200 kHz (5 us) is reached, one-shot U12A and flip flop U11 disable one-shot U12B and the inputs to the ECL frequency detector. At this point the difference signal from the mixer is within the loop bandwidth and the loop will acquire lock by itself.

Dual CMOS Switch No. 2 (U7)

This circuit has one channel activated, depending on the out-of-lock direction of the VCO, by one of the two AND circuits being modulated by the discriminator signal. Thus, current is pumped into or out of the RC feedback node of the op-amp integrator (service sheet 11).This forces the output of the op-amp to ramp up or down in the correct direction toward lock.



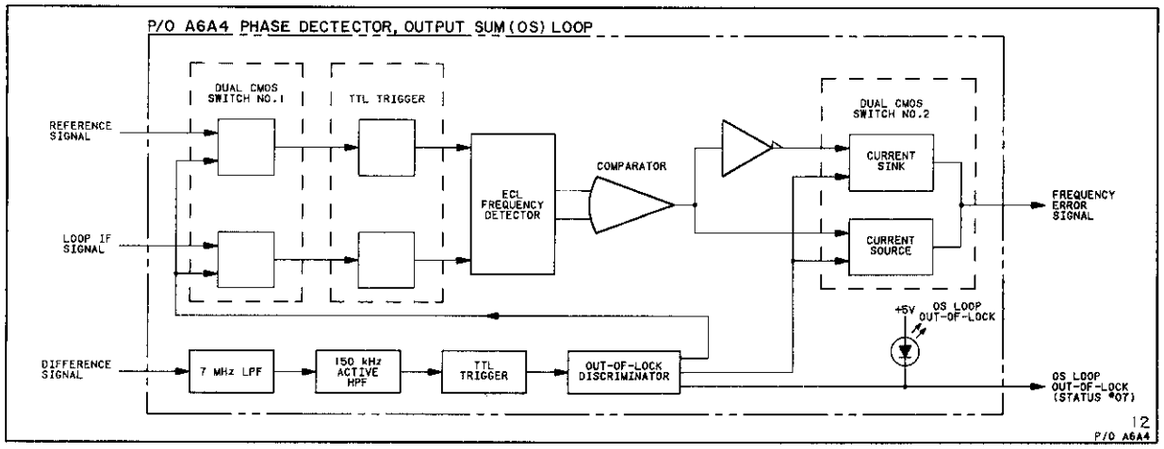


Figure 8-334. P/O A6A4 Output Sum Loop Phase Detector Block Diagrams

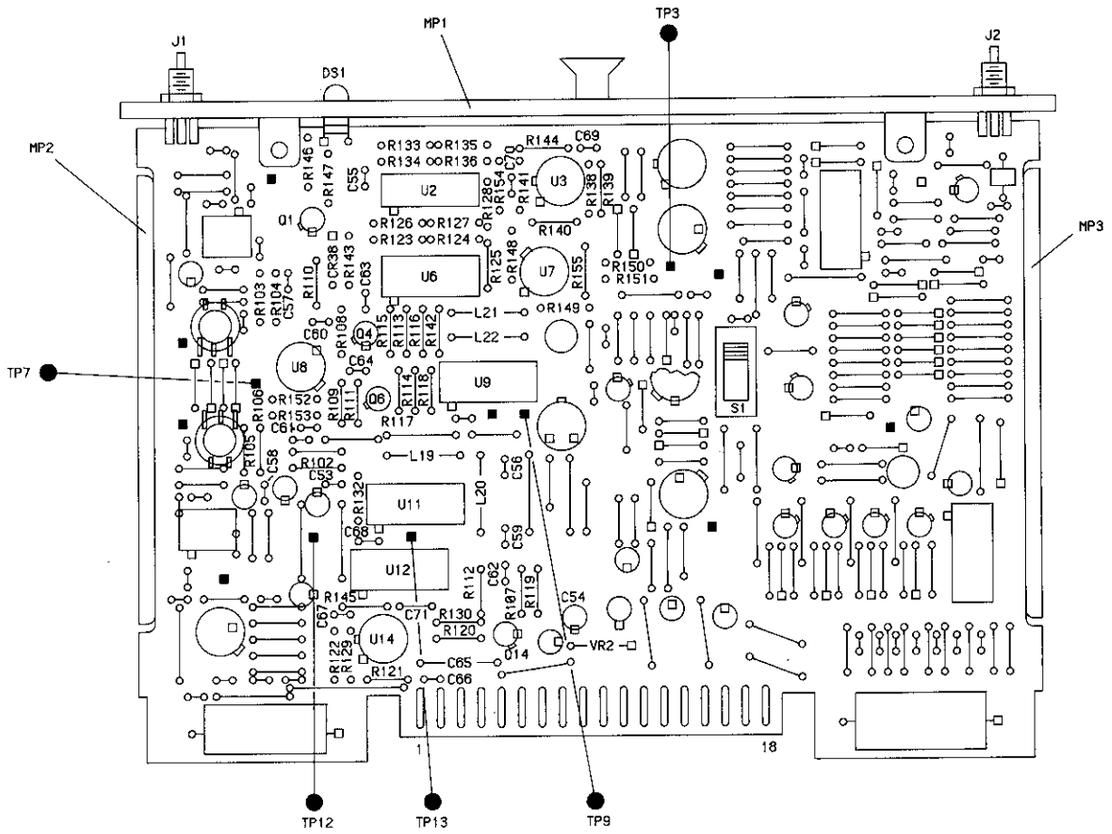


Figure 8-335. P/O A6A4 Output Sum Loop Phase Detector Component Locator

CHANGES

2516A and Above

On the A6A4 schematic:

- A6A4R148 - Change the value of R148 to 1.33k.
- A6A4VR2 - Change the value of VR2 to 7.5V.

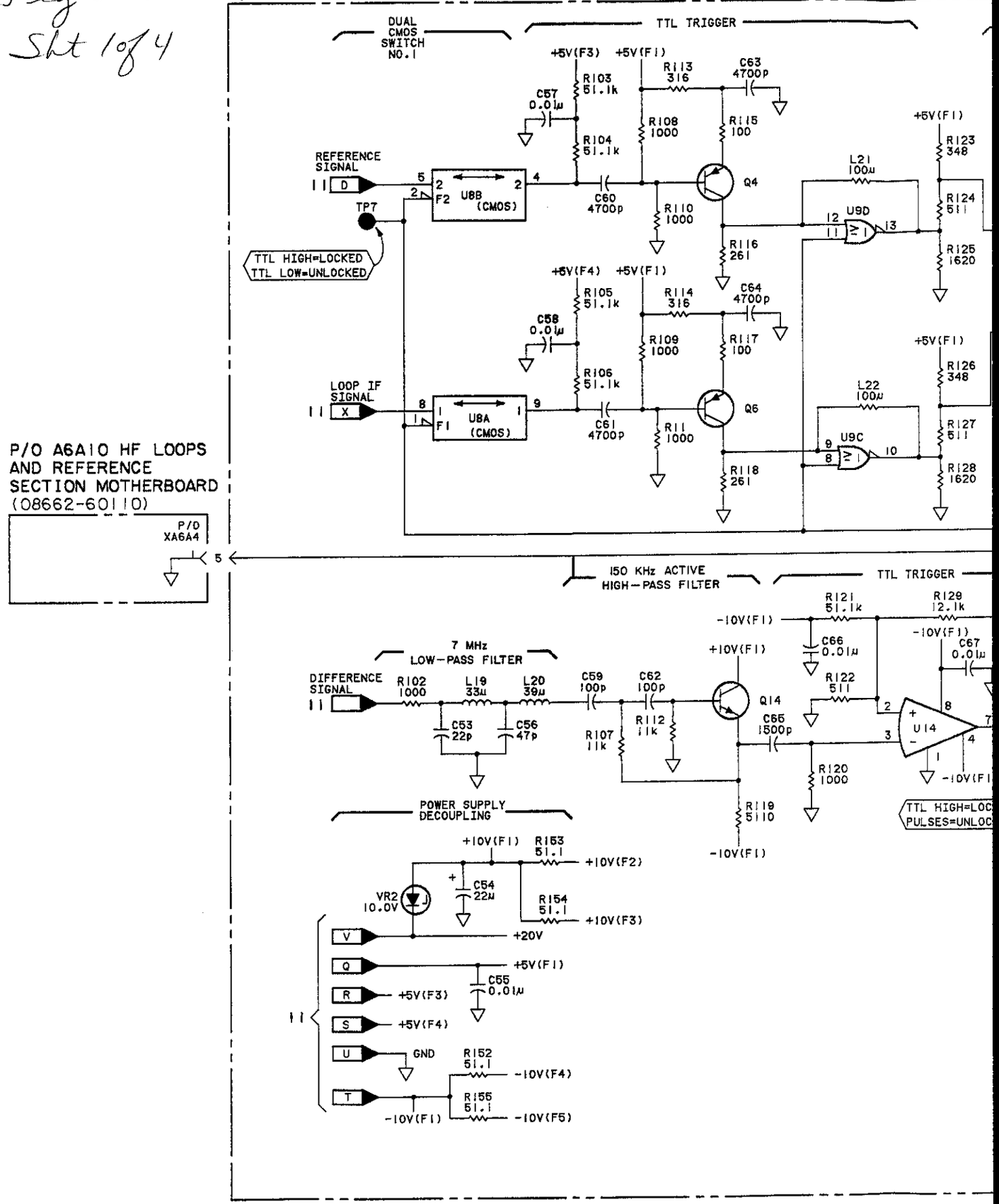
2706A and above

On the A6A4 schematic:

- A6A4 - Change the part number of the A6A4 schematic to 08662-60358.

Fig 8-336
Sht 1 of 4

P/O A6A4 PHASE DETECTOR, OUTPUT SUM (OS) LOOP (08662-60108)



SERIAL PREFIX: 2234A

Fig 8-336 Sht 2 of 4

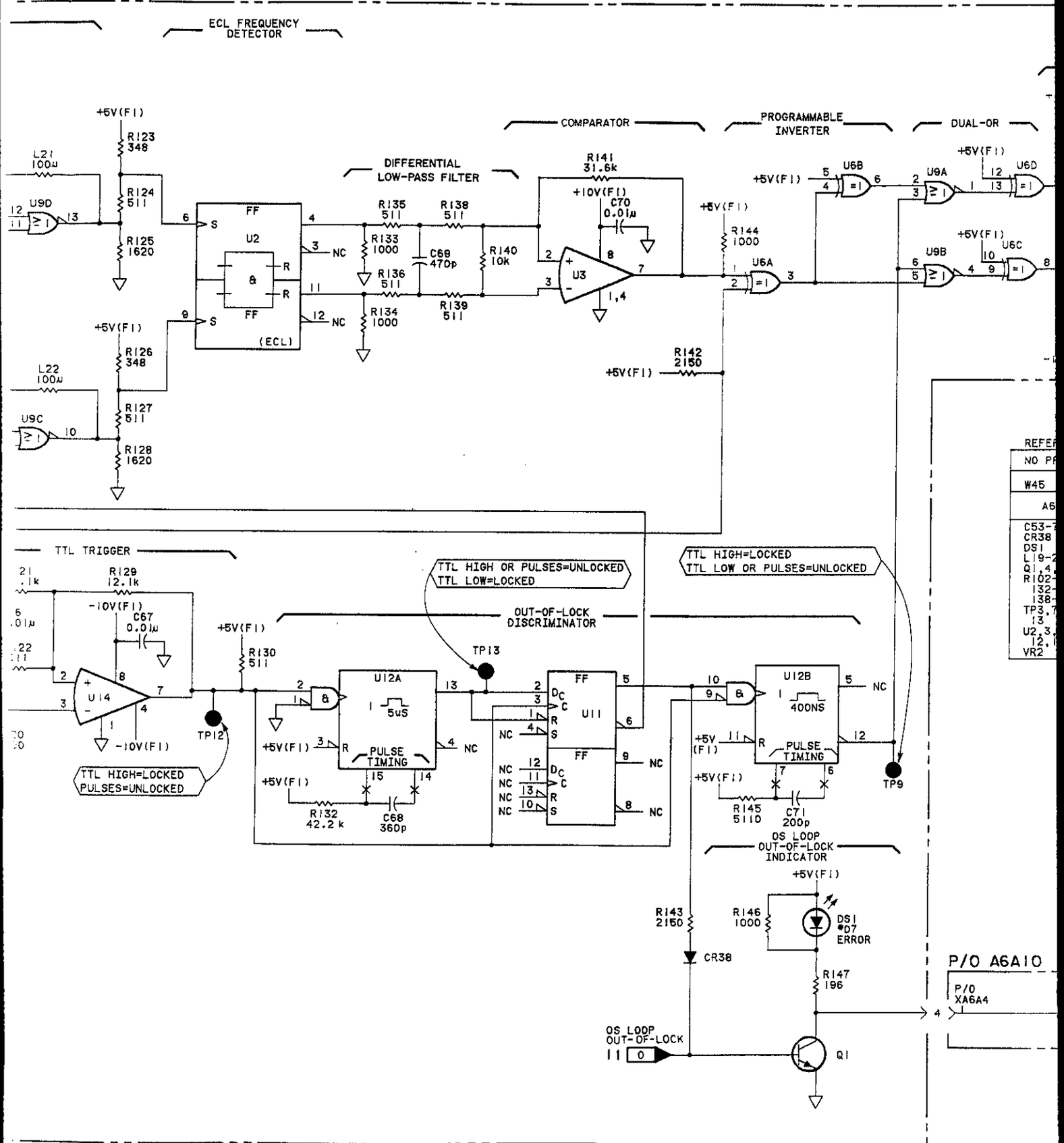
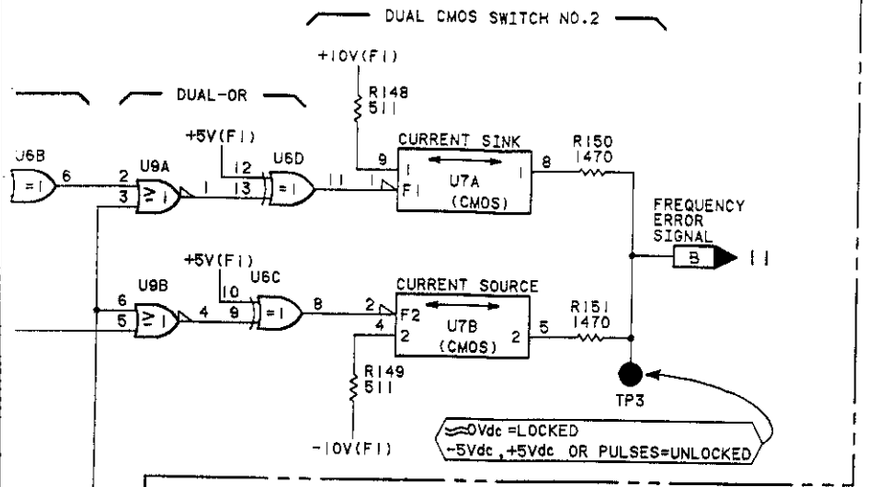


Fig 8-336 Sht 3 of 4



NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NON-STANDARD DUE TO SUPPLY VOLTAGE USED. A HIGH LEVEL IS ≥ +4.0V; A LOW LEVEL IS ≤ +3.5V.

REFERENCE DESIGNATIONS

NO PREFIX	A6A10
W45	J1
A6A4	XA6A4
C53-71 CR38 DS1 L19-22 Q1,4,6,14 R102-130, 132-136 138-155 TP3,7,9,12, 13 U2,3,6-9,11 12,14 VR2	

LOGIC LEVELS

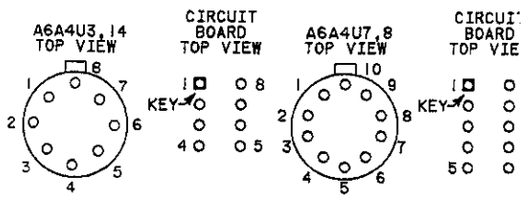
	TTL	ECL (NOTE 4)	CMOS
HIGH	>+2V	>+4.0V	≈VDD
LOW	<+0.8V	<+3.5V	<+0.1V
< IS MORE NEG. THAN > IS MORE POS. THAN			
OPEN	HIGH	LOW	UNDEF.
GROUND	LOW	LOW	LOW

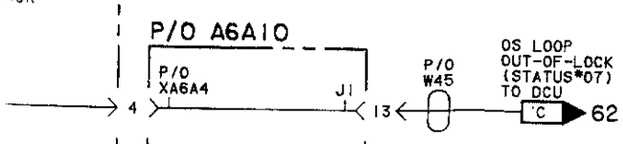
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,14	1854-0404
Q4,6	1853-0007
U2	1820-1344
U3	1826-0026
U6	1820-1211
U7,8	1820-1781
U9	1820-1322
U11	1820-1112
U12	1820-0579
U14	1820-0475

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U2	+5V(F1)-1,14 ▽ - 7 NC-2,5,8,10,13
U6,9,11	+5V(F1)-14 ▽ - 7
U7	+10V(F3)-10 -10V(F5)-6 ▽ - 3
U8	+10V(F2)-10 -10V(F4) -6 ▽ - 3
U12	+5V(F1) -16 ▽ - 8





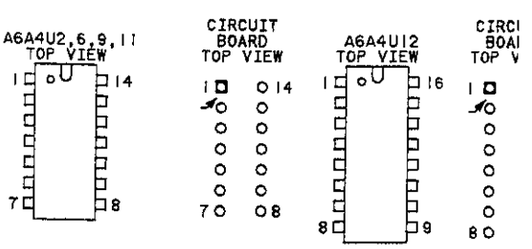
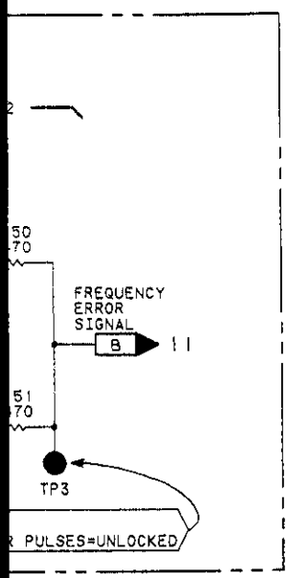


Fig 8-336
Sht 4 of 4



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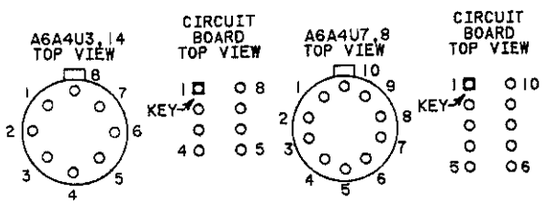

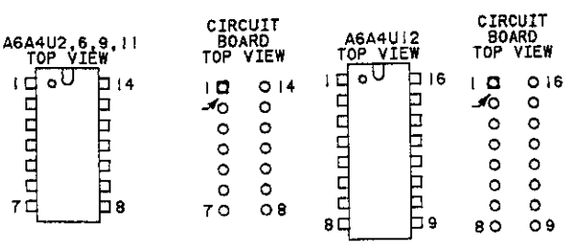

SERVICE SHEET 12

P/O A6A4

Figure 8-336. P/O A6A4 Output Sum Loop Phase Detector Schematic