3048 MS

HP 8663A
SYNTHESIZED SIGNAL GENERATOR
(Including Options 001, 002, & 003)

Service Manual

Volume 3

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed:

2234A to 2927A and all *MAJOR* changes that apply to your instrument.

rev.01JUL91

For additional important information about serial numbers, refer to "INSTRUMENTS COVERED BY THIS MANUAL" in Section 1.

Third Edition

Service Manual (Volume 1, 2, 3, 4) HP Part 08663-90071

Other Documents Available:
Operation and Calibration Manual HP Part 08663-90069
Microfiche Service Manual HP Part 08663-90072
Microfiche Operation and Calibration Manual HP Part 08663-90070

Printed in U.S.A. : November 1990

HEWLETT PACKARD

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A5A4 FRACTIONAL-N LOOP

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Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Reference Divider divides the 10 MHz reference signal down to 100 kHz which is used as the reference signal to the phase detector. This assembly also generates the sample pulse signal that clocks the sample-hold circuit at the proper time.

Shaper

The shaper network consists of a diode clamping network and a differential amplifier. It provides the analog-to-TTL conversion.

Reference Divider

U1 and U4 form the divide-by-100 circuit which divides the 10 MHz input signal to produce the 100 kHz phase detector reference signal.

Sample Pulse Generator

The function of the sample pulse generator is to produce a 500 ns pulse that is delayed by 1 microsecond from the leading edge of the phase detector reference signal. This is accomplished by detecting a state in the divide-by-100 circuit which corresponds to the desired delay time.

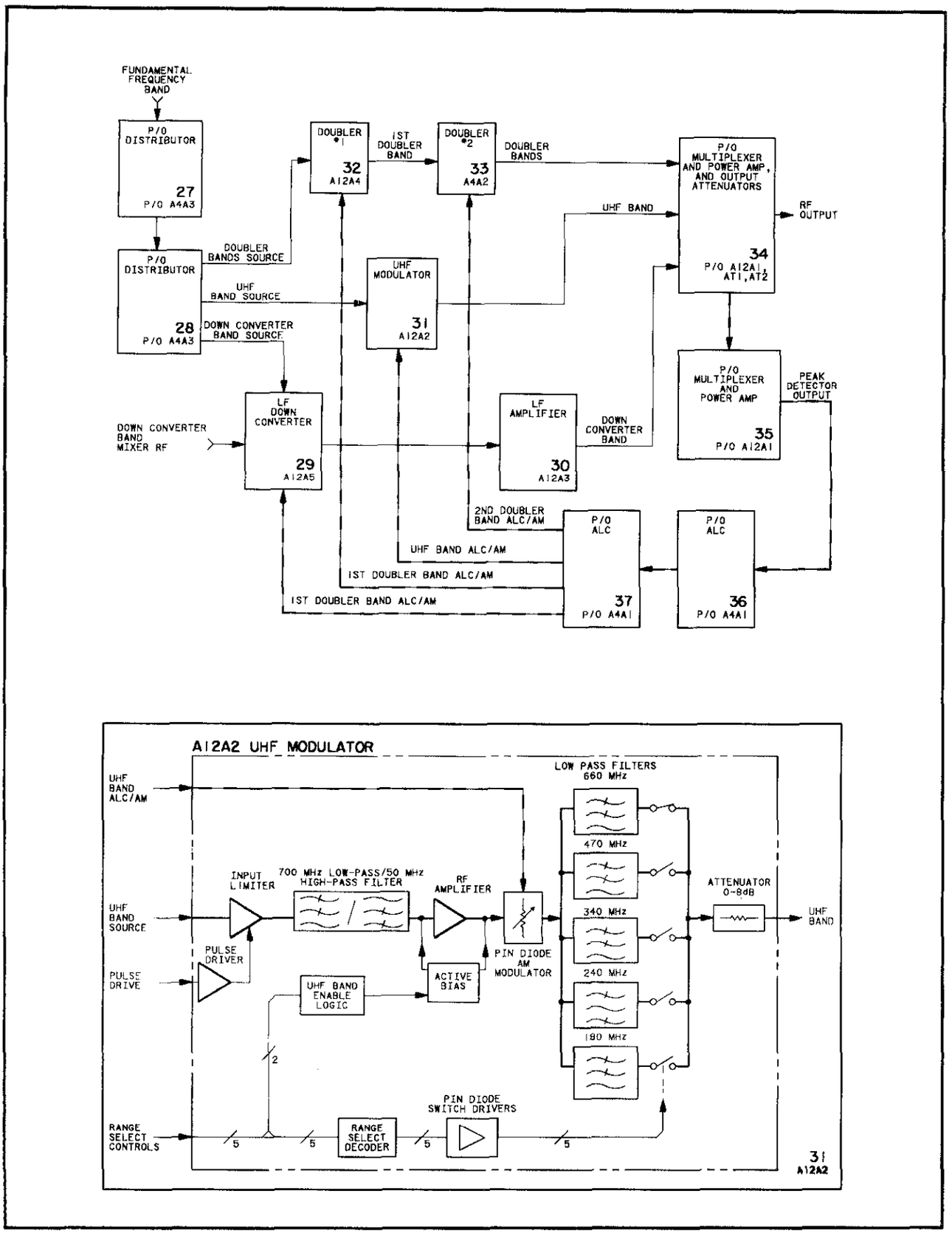


Figure 8-513. A12A2 UHF Modulator Block Diagrams

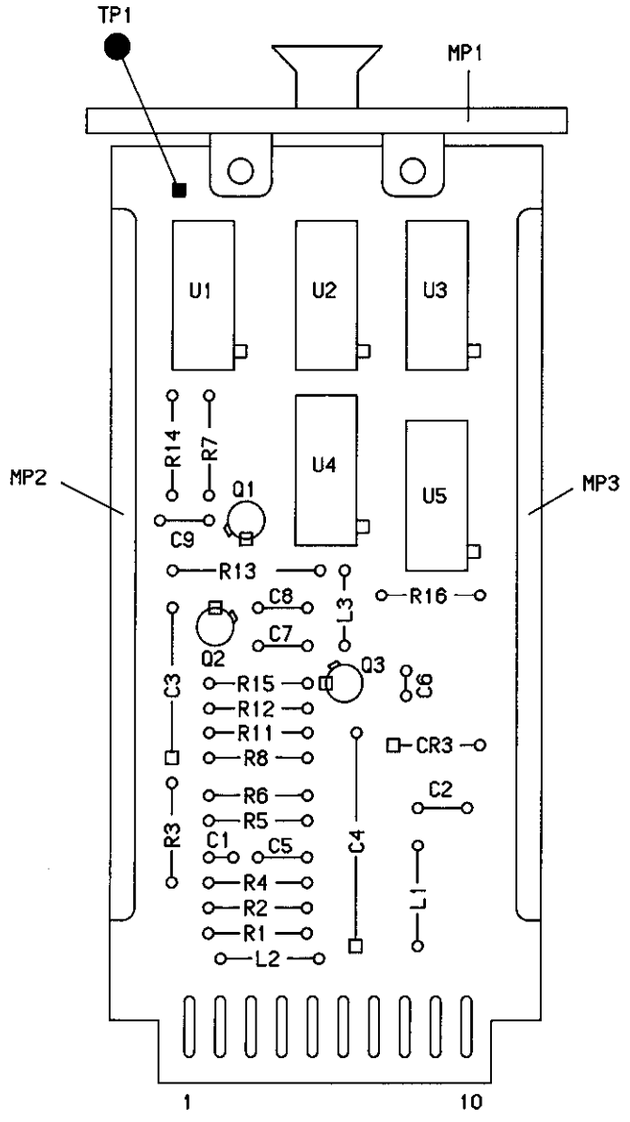


Figure 8-402. A5A4Fractional-N Loop Reference Divider Component Locator

Fig 8-403
Sht 1 of 4

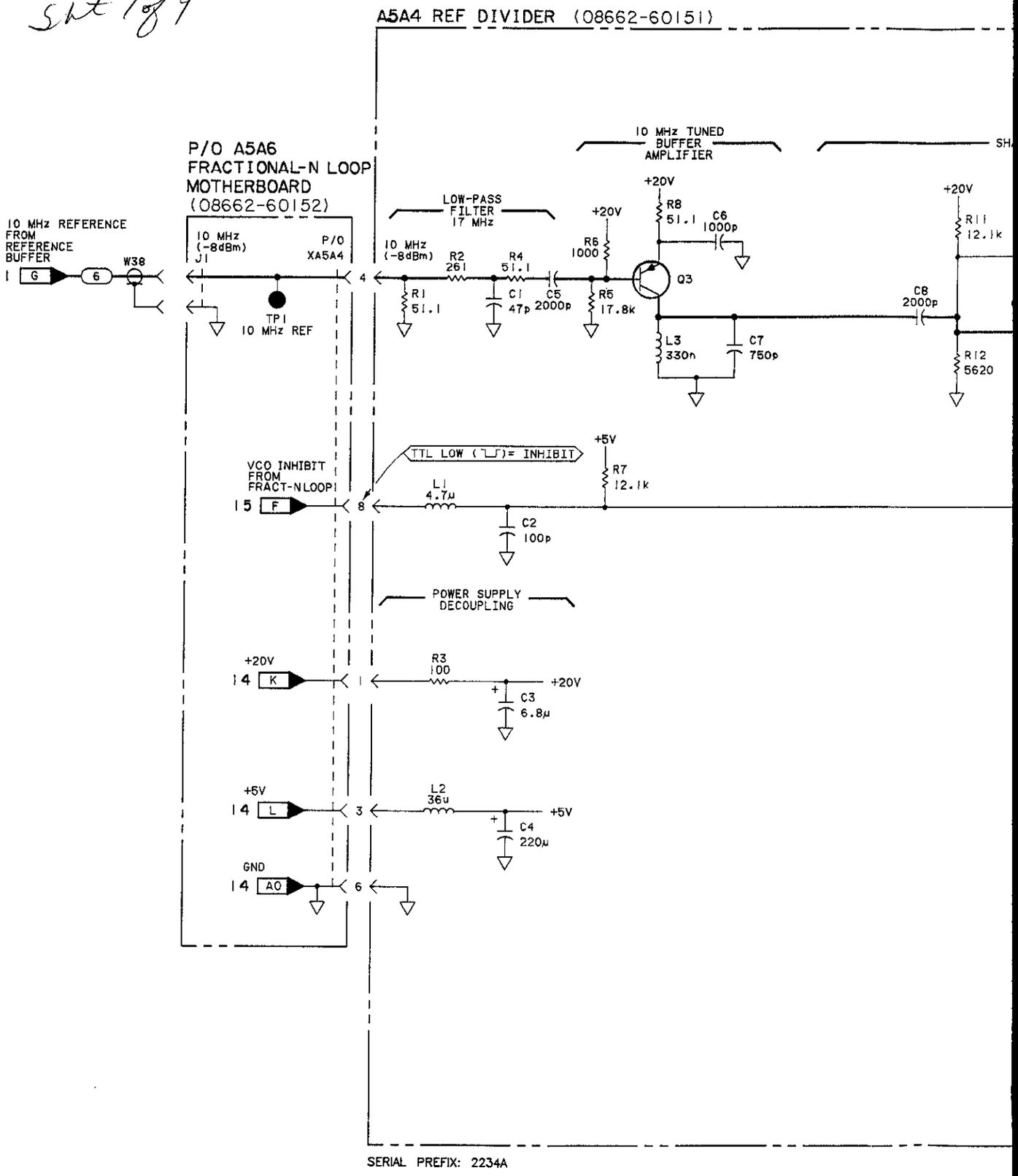


Fig 8-403
Sht 2 of 4

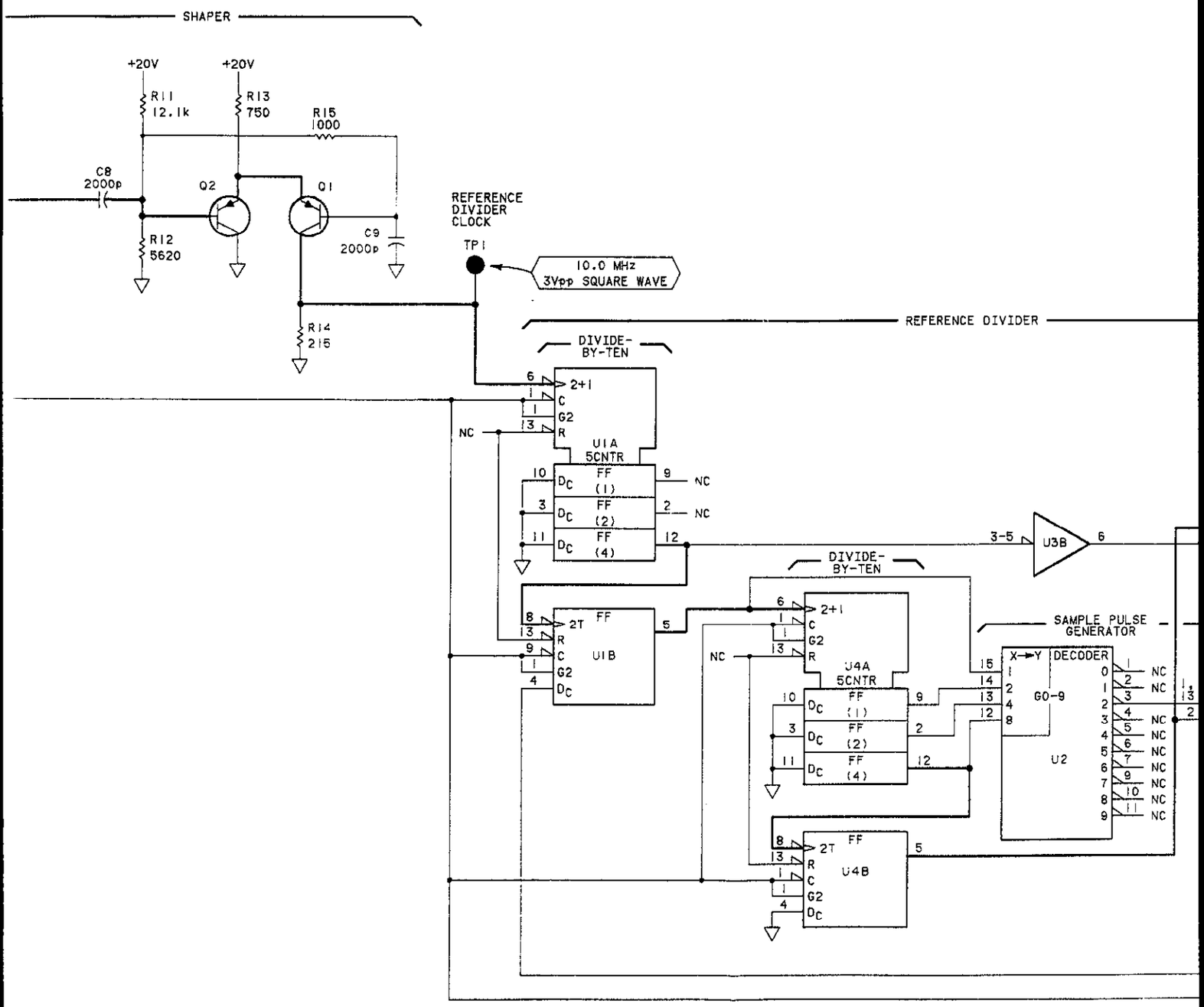


Fig 8-403
Sht 3 of 4

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

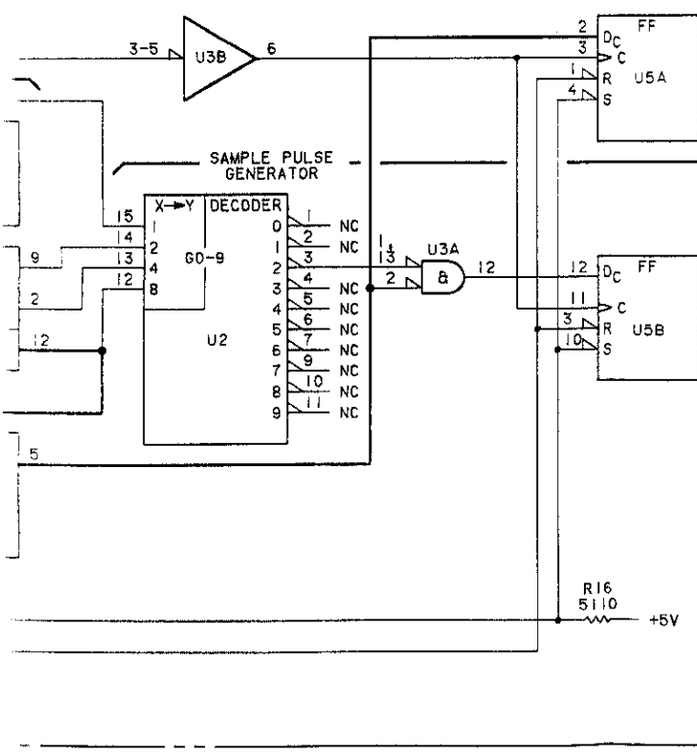
REFERENCE DESIGNATIONS

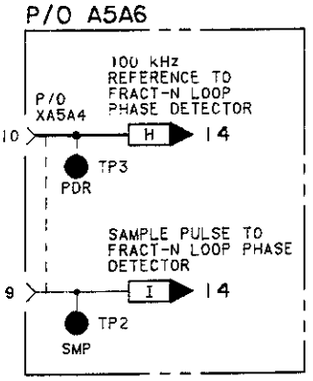
NO PREFIX	A5A6
W38	J1
A5A4	TP1-3 XA5A4
C1-9 CR3 L1-3 Q1-3 R1-8,11-16 TP1 U1-5	

LOGIC LEVEL

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

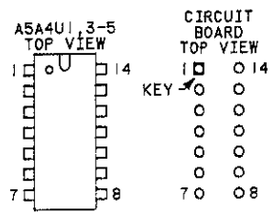
REFERENCE DIVIDER





INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1,3-5	+5V ▽ — 14 — 7
U2	+5V ▽ — 16 — 8



TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1-3	1853-0034
U1,4	1820-1251
U2	1820-1418
U3	1820-1206
U5	1820-0693

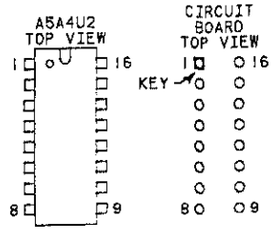


Fig 8-403
Sht 4 of 4

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

REFERENCE DESIGNATIONS

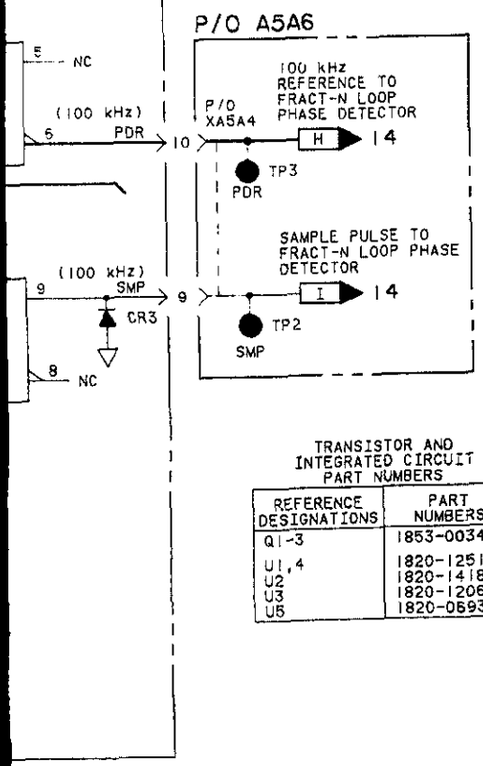
NO PREFIX	A5A6
W38	J1
A5A4	TP1-3
	XA5A4
C1-9	
CR3	
L1-3	
Q1-3	
R1-8, 11-16	
TP1	
U1-5	

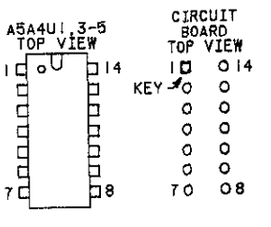
LOGIC LEVEL

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1,3-5	+5V - 14 ▽ - 7
U2	+5V - 16 ▽ - 8





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Q1-3	1853-0034
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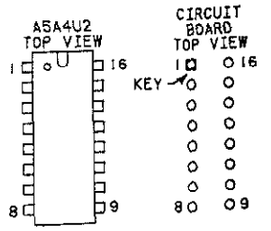
U2	1820-1418
U3	1820-1206
U5	1820-0693



SERVICE SHEET A5A4 13

Figure 8-403. A5A4 Fractional-N Loop Reference Divider Schematic

SERVICE SHEET 14
A5A3 FRACTIONAL-N LOOP PHASE DETECTOR

REFERENCE BLOCK DIAGRAM 4
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The purpose of the Fractional-N Loop Phase Detector (A5A3) is to develop the FN Loop Error Voltage which is used to tune the VCO. This FN Loop Error Voltage (tuning voltage) is developed by integrating currents from the Phase Detector circuit, the Fractional-N Correction Pulse Width to Current Converters, and the Bias Sink circuit. These currents are integrated together by the Current Summing Amplifier to develop a voltage. The Sample and Hold circuit samples the voltage output from the Current Summing Amplifier once each reference period and at the same time during each reference period. The sampled voltage becomes the FN Loop Error Voltage.

When the Fractional-N Loop (FN Loop) is phase-locked, the tune voltage must be a constant dc value. This means the voltage output from the Current Summing Amplifier must be the same at every sample period. In order to meet this condition the total of the currents being integrated must be the same each reference period. To look at it another way, the currents entering the summing node must equal the currents leaving the summing node in order for the tune voltage to remain constant. This concept, that when the FN Loop is phase-locked, the currents entering the summing node equal the currents leaving the node is true for all conditions, that is, for the condition when the loop runs without a fractional part and for the condition when it has a fractional part. The difference is that when the loop operates with no fractional part the output from the Phase Detector circuit remains constant. However, when the loop operates with a fractional part, the output from the Phase Detector circuit no longer remains constant but varies from reference period to reference period. To compensate for the changing phase detector output the outputs from the Fractional-N Correction Pulse Width to Current Converters must also change. For example, if the Phase Detector circuit supplies less current to the summing node, the Fractional-N Correction Pulse Width to Current Converters must supply more current so that the current entering the summing node is always a constant value.

Phase Detector

The Phase Detector consists of a pair of flip-flops, U5A and B, and gates U4D and U8C. The purpose of the Phase Detector is to generate a pulse width proportional to the phase difference between its two input signals, the FN Loop IF (VCO/N) and the FN Loop PM Det

Reference (reference). Normally the FN Loop operates with a slight phase offset when the loop is phase-locked. This phase offset is due to the constant current being drawn from the summing node by the Bias Sink circuit. Figure 8-404 shows the phase relationship between the VCO/N signal and the reference signal when the loop is phase-locked and has no fractional part. Note that the two signals are equal in Frequency but are out of phase. This phase offset is normally about 250 ns.

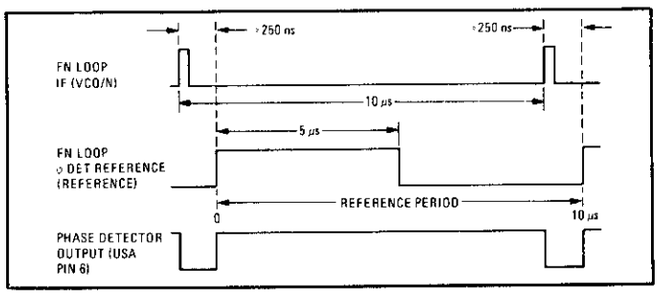


Figure 8-404. Fractional-N Loop Phase Detector Input and Output Waveforms (Phase Locked and No Fractional Part)

This phase offset causes the Phase Detector (U5A) to generate a 250 ns negative-going pulse every reference period (See Figure x-xx). The other Phase Detector output (U5B) is normally only a glitch (which is filtered out) when the loop is phase-locked. U5B should only generate a pulse output during the acquisition of lock.

In a phase-locked condition the amount of current drawn from the summing node is equal to current driven into the node. When the FN Loop operates without a fractional part, the phase detector generates a constant pulse width every reference period. This results in a constant amount of current being driven into the summing node from the phase detector current source (I_{DET}) each reference period. Currents from the Fractional-N Correction circuit (I_1, I_2, and I_3,) also remain constant, therefore, the total current entering into the summing node is always a constant value each reference period.

Now when the loop operates with a Fractional part, the VCO/N signal and reference signal no longer equal each other, hence the phase detector no longer generates a constant pulse width each reference period.

NOTE

If the N-Divider (A5A2) is in the divide-by-N mode, the VCO/N signal starts to lag the reference frequency,which results in a series of decreasing pulse width signals from the phase detector. Conversely, if the N-Divider is dividing by N-1, the pulse width from the phase detector starts to increase.

For example, if the N-Divider is in the divide by N mode, the output pulses from the phase detector start to decrease in duration each reference period. This causes the phase detector current source, I_{DET}, to be connected to the summing node for shorter periods each reference period. At the same time correction current from the Fractional-N Correction circuit is increasing (Correction Pulses duration increasing). The net result is that the decreasing phase detector current is compensated by the increasing correction currents so that the total current contributions from the Phase Detector and the Fractional-N Correction circuits to the summing node are always a constant value.

Level Translators, Diode Switches and Current Sources

Following the Phase Detector are Level Translators, and Diode Switches and Current Sources. These circuits convert the digital outputs from the Phase Detector into currents. There are two types of Level Translators and Current Sources used. One type uses an active current source and a differential amplifier arrangement to switch the Diode Switch on and off. Q4 and U3 form an active current source while CR17 and CR19 form the Diode Switch. Q1, Q2 and Q3 make up the differential amplifier that translates the TTL levels to the appropriate levels required to drive the Diode Switch on and off. When the output from the Phase Detector goes LOW, CR17 is reverse-biased and CR19 is forward-biased, connecting the Current Source to the summing node. In the opposite state when the output is HIGH, CR17 is forward-biased and CR19 becomes reverse-biased, disconnecting the Current Source from the summing node.

The Levels Translator, Diode Switch and Current Source which follow the output of U5B word in a similar manner, as described previously. The major difference is that the active current source is replaced simply by a resistor, and that the level shifting is done with a diode string instead of a differential amplifier.

Out-of-Lock Detector

The Out-of-Lock Detector monitors the two outputs from the Phase Detector to determine if the loop is unlocked. The Out-of-Lock Detector detects two unlock conditions. One condition is when the pulse width from U5A exceeds about 700 ns. The other condition is when the output from U5B exceeds 100 ns. Note that the Loop should never be in a phase-locked condition when U5B generates a pulse. Monostable U7 stretches either the 100 ns or 700 ns pulse to give a contiuous indication that an unlocked condition exists.

Fractional-N Correction Pulse Width To Current Converters (Fractional-N Correction)

The purpose of the Fractional-N Correction circuit is to develop the signals that counteract the changing phase detector output when the loop is operating with a fractional part. The Fractional-N Correction circuit is comprised of Level Translators, Diode Switches and Current Sources. These circuits convert the Correction Pulses (TTL levels) from the Accumulator (A4A1) into currents. The Level Translators, Diode Switches and Current Sources are the same types which follow the Phase Detector circuit. For discussion of these circuits, refer to the Section titled Level Translators, Diode Switches and Current Sources.

Each one of the Correction Current Sources I_1, I_2, and I_3, is connected to the summing node once during each reference period. The sequence of these currents are as follows: Correction current I_3, Correction current I_2, and Correction current I_1. How long each of the Current Sources remains connected to the summing node depends on the negative pulse duration of its corresponding Correction Pulse.

Current Summing Amplifier

The Current Summing Amplifier is an integrator circuit. C34 is the integrating capacitor. When the loop is phase-locked the currents being integrated are: I_{DET}; I_3; I_2; I_1 and currents from the feedback network C32 and R54.

Due to the different magnitudes of the various current sources and the different times the current sources are connected to the summing node, the output from the Current Summing Amplifier is continuously ramping up and down. Figure 8-405 illustrates the integrator waveform showing the contribution of the different currents.

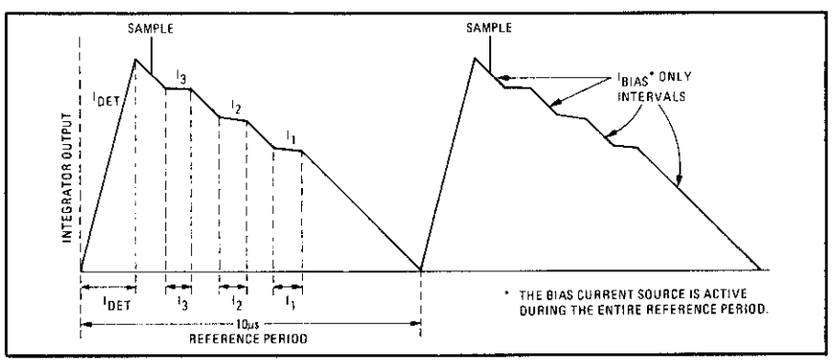


Figure 8-405. Current Summing Amplifier Output Waveform showing the contributions of the different currents

Sample and Hold

The circuits which make up the Sample and Hold circuit are the Diode Switch, Differential Amplifier, Guard Voltage Network, and the Buffer Amplifier. During each reference period, the four diodes which comprise the Diode Switch are all forward-biased and the output of the Current Summing Amplifier is sampled. This sample voltage (VS) is stored in hold capacitor C47. During the hold period the Diode Switch is reversed-biased and the hold capacitor remains stored. The Buffer Amplifier, U1, which follows the hold capacitor, provides isolation and a low output impedance.

The Buffer Amplifier is a unity-gain, noninverting amplifier. Feedback from this output is fed back to the summing node through C32 and R54 for loop stabilizations.

Switching of the Diode Switch is controlled by the Differential Amplifier. During the sample period, the Sample Pulse line goes high, causing the Differential Amplifier to supply current to the Diode Switch. The Differential Amplifier also provides current to the Guard Voltage Network during the hold period.

The purpose of the Guard Voltage Network is to ensure that the voltage to be sampled does not itself forward-bias the Diode Switch during the hold period. The guard voltages (the collector voltages of Q7 and Q11) are balanced and centered around the last sample voltage. About 2 ma of current flows through the Guard Voltage network during the hold of current flows through the Guard Voltage network during the hold period. This causes a voltage drop of 4V (guard voltages) across CR28 and R82 and across CR27 and R81 the guard voltages equal +6V and -2V for a sample voltage of +2 Vdc (guard voltages = Vs $\pm$ 4 Vdc).

TROUBLESHOOTING

When a Fractional-N Loop problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

1. Mount the A5A3 assembly on an extender board from the service kit. Move the slide switch on A5A3 to the TEST position (up) which opens the loop.

2. Monitor TP3 with an oscilloscope. The waveform should be a dclevel with small spikes. Measure the frequency of the signal at pin 14 of the edge connector.

   Turn the PRETUNE-GAIN adjustment on the top of the A5A5 VCO assembly while monitoring the frequency at pin 14. Move the frequency above and below 100 kHz and check that the voltage at TP3 goes to the values shown in the following table. If the voltages at TP3 are normal, continue troubleshooting with step 3. Otherwise, there is a problem with the basic phase detector circuitry so continue troubleshooting with step 4.

Edge Connector Pin 14 Frequency (kHz)	A5A3 TP3 (Vdc)	A5A3 TP2 (Vdc)	A5A3 TP1 (Vdc)
>100 kHz	+18	+16	+15
<100 kHz	-7	-7	-7

3. Repeat the measurement made in step 2 while monitoring TP2 and then TP1. Compare the measured values to the normal values in the table above.

   If the voltage at TP2 is not normal, the differential amplifier or diode switch is bad. Shorting TP5 and TP5A together holds the amplifier and diode switch in the ON condition for troubleshooting.

   If the voltage at TP1 is not normal but the voltage at TP2 is normal, the problem is in U1 or associated circuitry.

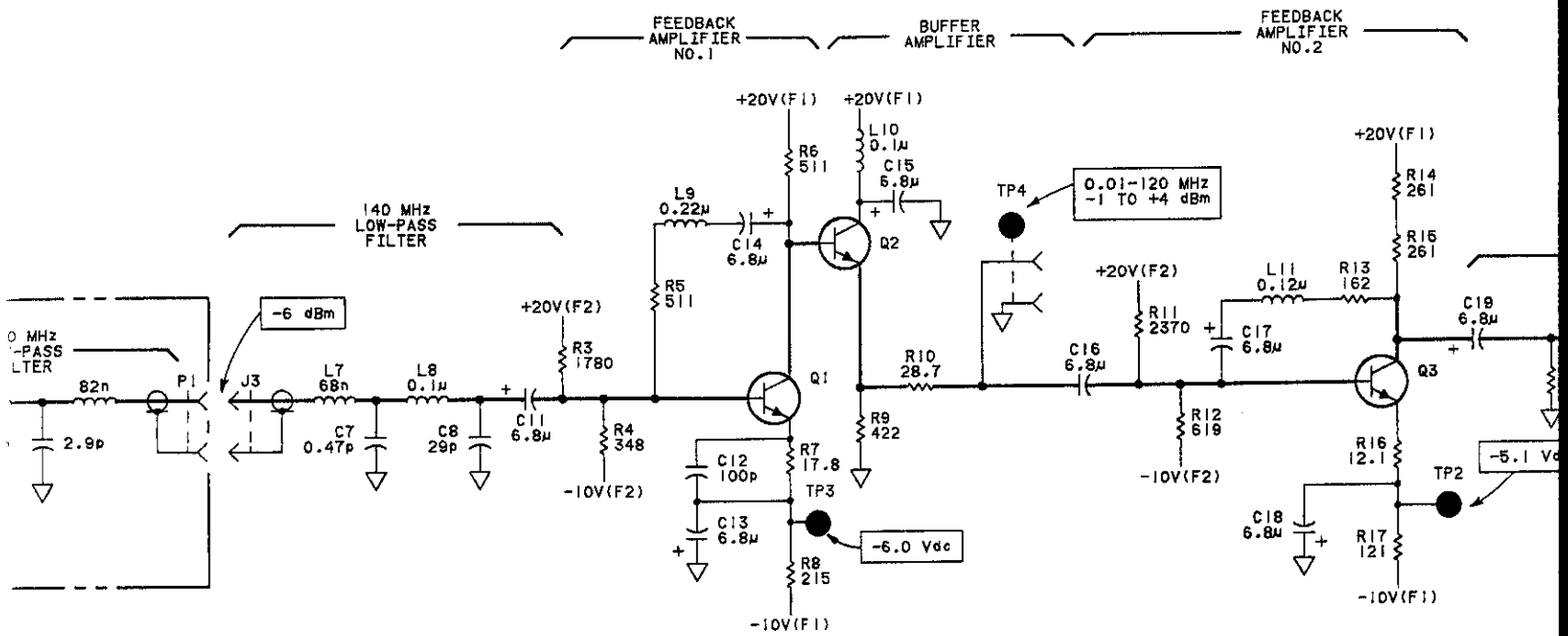
4. Turn the PRETUNE-GAIN adjustment on A5A5 so the frequency at pin 14 of the A5A3 edge connector is greater than 100 kHz. Check that there are pulses on A5A3 TP4.

   Change the frequency at pin 14 to less than 100 kHz. Check that there are pulses on A5A3 TP8.

5. If pulses are not present at one of the test points, troubleshoot from U5 to find the cause of the problem. If both pulses are present, the problem is with U2 or associated components.

Fig 8-512
Sht 2 of 4

345)



+20V(F1)

+20V(F2)

C9
6.8μ

GND

-10V(1)

-10V(1)

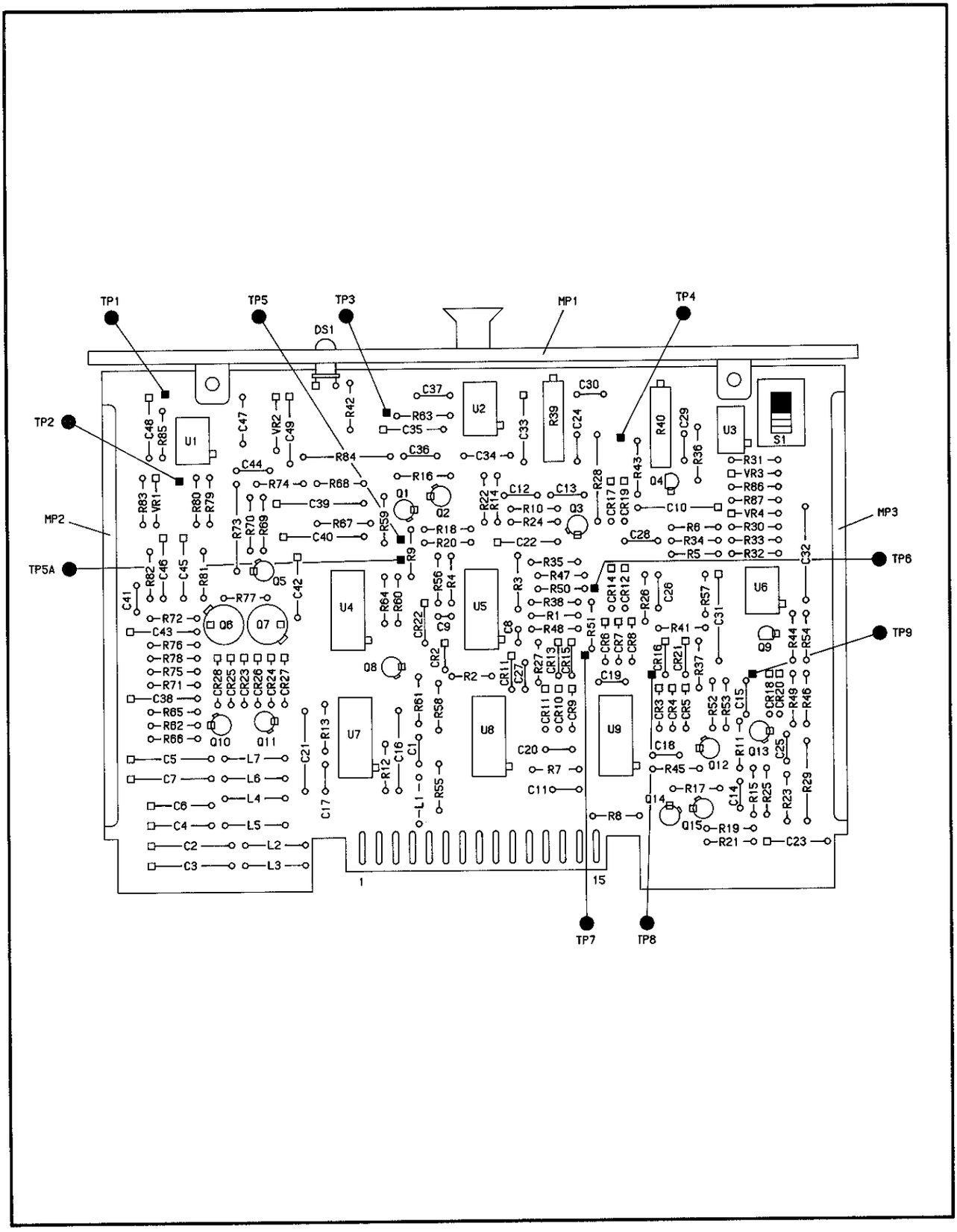
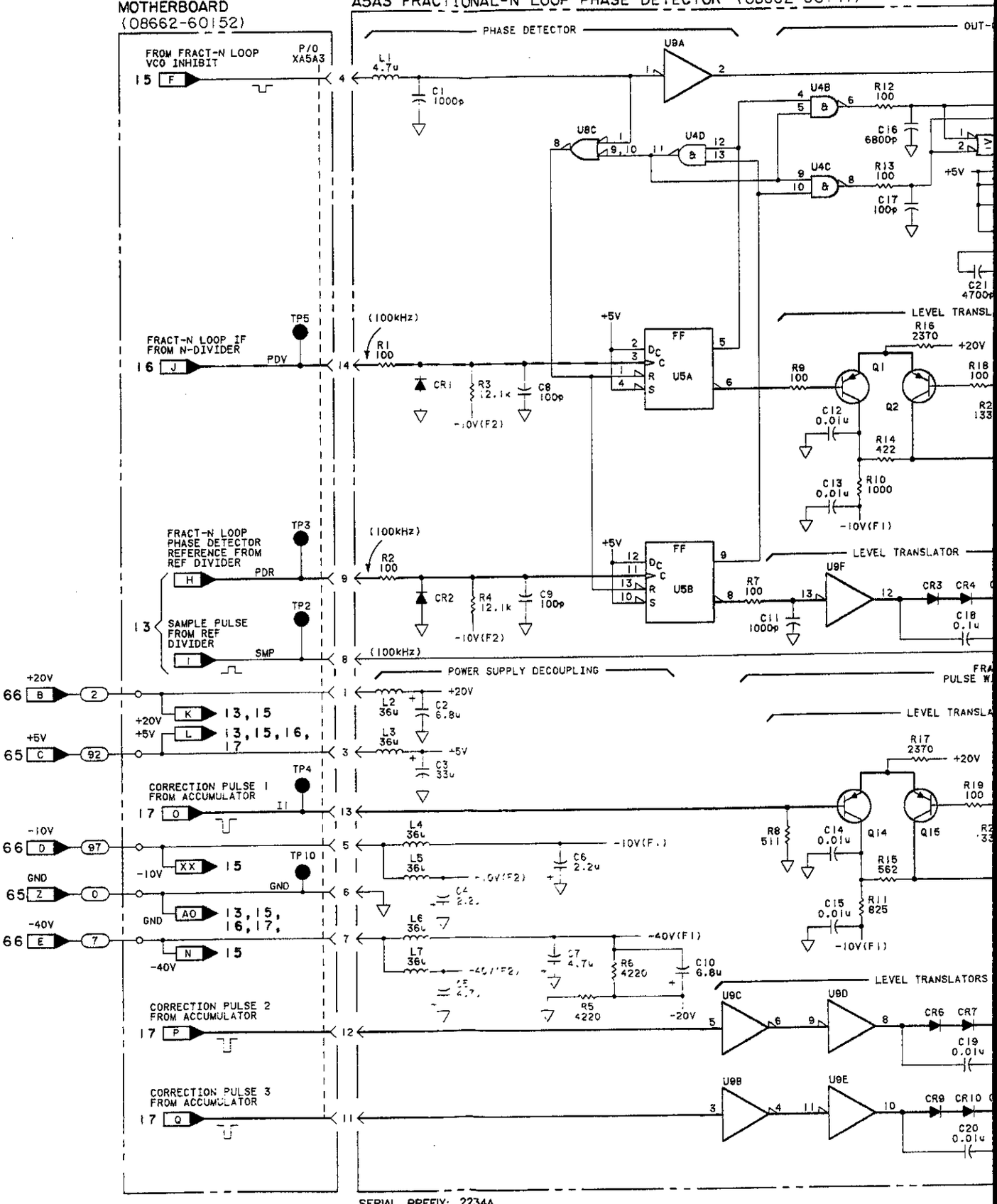


Figure 8-407. A5A3 Fractional-N Loop Phase Detector Component Locator

Fig 8-408
Sht 1 of 4

P/O A5A6
FRACTIONAL-N LOOP
MOTHERBOARD
(08662-60152)



SERIAL PREFIX: 2234A

Fig 8-408
Sht 2 of 4

(08662-60147)

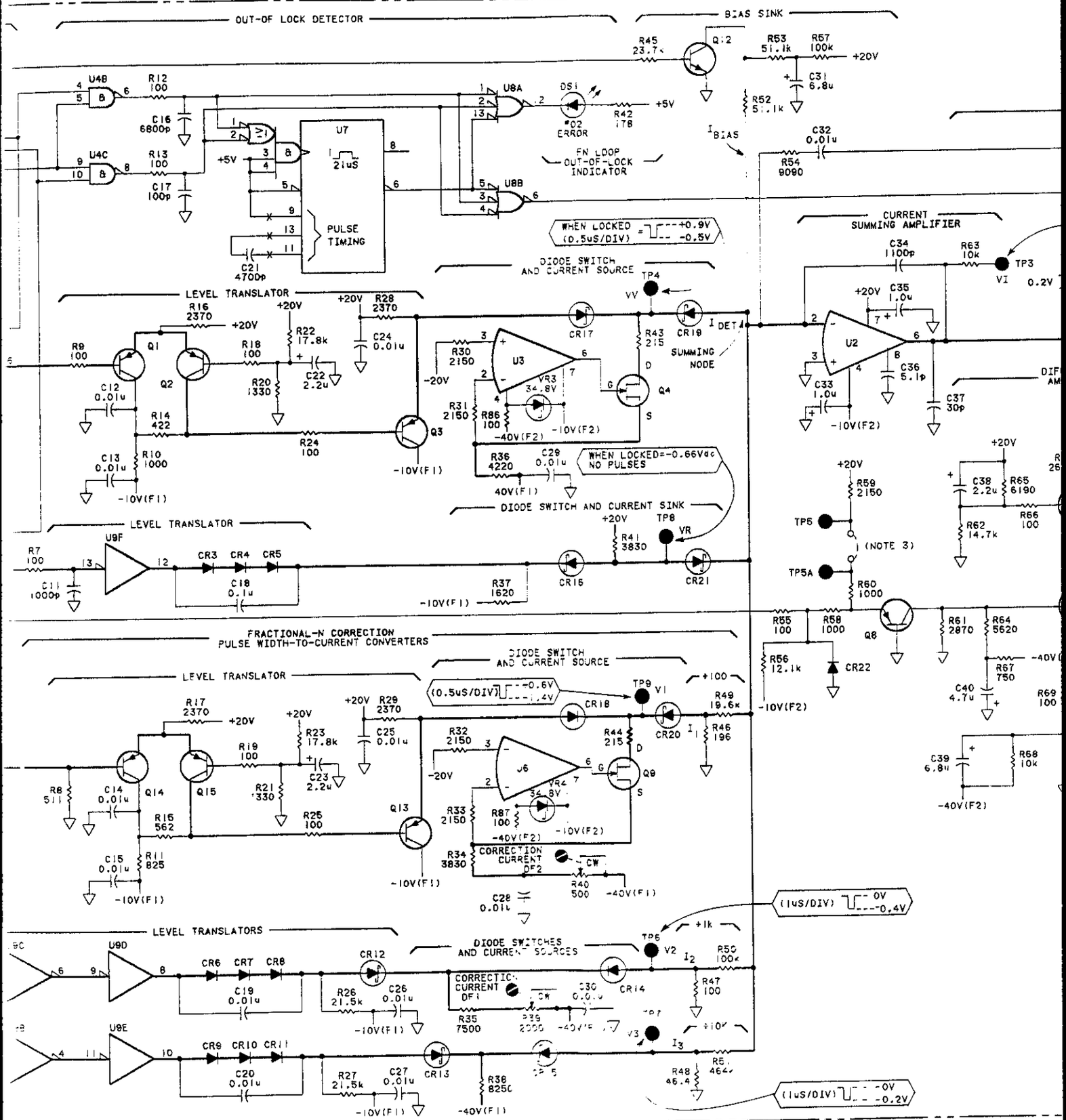


Fig 8-408
Sht 3 of 4

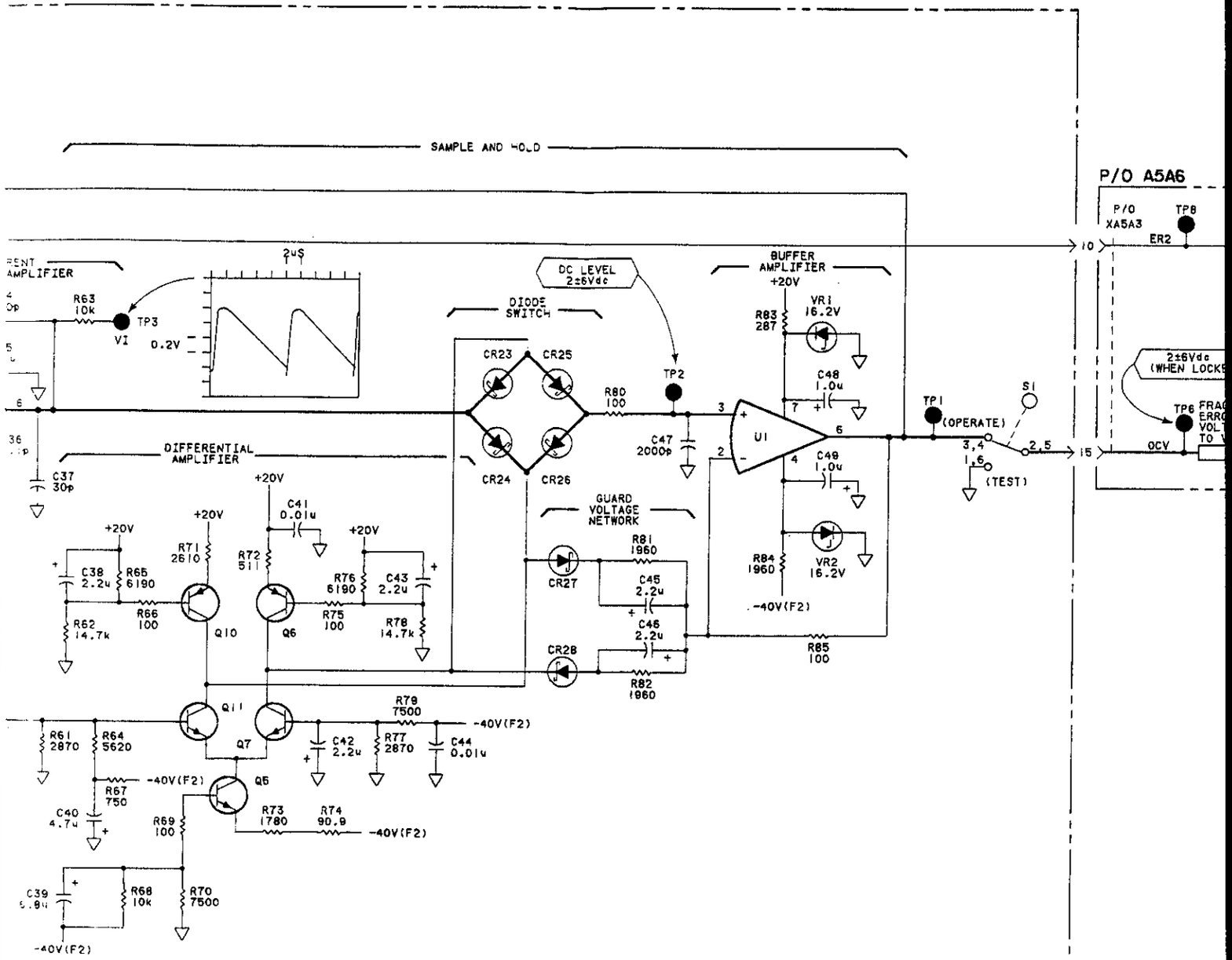
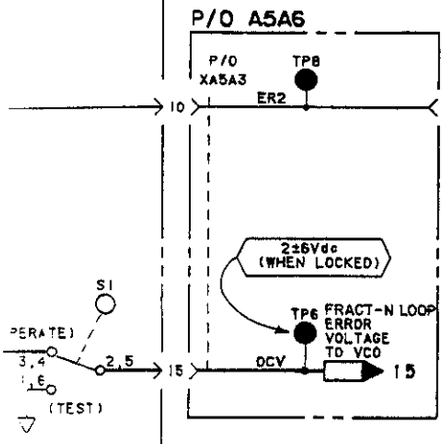
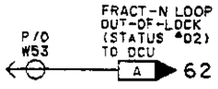


Fig 8-408
Sht 4 of 4





NOTES

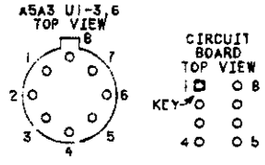
1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. SHORTING TP5 TO TP5A KEEPS THE DIODE SWITCH CLOSED SO THE OUTPUT OF U2 IS ALWAYS CONNECTED TO THE INPUT OF U1. IN THIS CONDITION, THE WAVEFORM AT TP3 SHOULD APPEAR AT TP2.

REFERENCE DESIGNATIONS

NO PREFIX	A5A6
W53	TP2-6,8,10 XA5A3
A5A3	
C1-49 CR1-28 DS1 L1-7 Q1-15 R1-87 S1 TP1-9 U1-9 VR1-4	

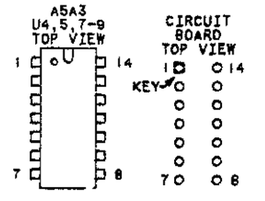
LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW



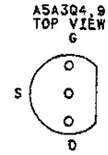
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1-3,8,10, 13-15	1853-0007
Q4,9	1855-0081
Q5,11	1854-0210
Q6	1853-0012
Q7	1854-0013
Q12	1854-0023
U1	1826-0371
U2	1826-0089
U3,6	1826-0013
U4	1820-0681
U5	1820-0693
U7	1820-1422
U8	1820-0686
U9	1820-0683



INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U4,5,7-9	+5V - 14 ⏚ - 7



SERVICE SHEET 14

A5A3

Figure 8-408. A5A3 Fractional-N Loop Phase Detector Schematic

SERVICE SHEET 15
A5A5 FRACTIONAL-N LOOP VCO

REFERENCE BLOCK DIAGRAM 4
Table 4-1. Recommended Performance Tests After Adjustments or Repair
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The purpose of the VCO (A4A4) is to generate an output frequency between 100 MHz and 200 MHz. The primary inputs are the pretune information, Digit Frequency DF4 and DF5, and the FN Loop Error Voltage. The output from the Pretune D/A Converter is used to tune the VCO close to the desired frequency and then the FN Loop Error Voltage is used to phase lock the loop.

Voltage-Controlled Hartley Oscillator (VCO)

Varactors CR10, CR11, and CR12, transistor Q11, and associated components comprise a voltage-controlled Hartley oscillator. Three varactors are used in parallel to provide the wide capacitance range required to tune the VCO. Feedback is obtained by tapping the inductive branch (L7) of the Tank Circuit. C32 and R84 couple the feedback signal back to the emitter of Q11 to sustain oscillation.

The VCO is both pretuned and phase locked by controlling the reverse bias voltage on the varactor diodes. An increase in the reverse bias voltage causes a reduction in the junction capacitance of the varactor diodes. This reduction increases the resonant frequency of the Tank Circuit, causing the VCO to oscillate at a higher frequency.

Signal Splitter and Buffer Amplifiers

The signal developed across the resonant Tank Circuit is coupled to Q6 by tapping inductor L7. Q6 amplifies the signal and applies the signal to the center tap winding of T1. T1 splits the power and adds isolation between the buffer amplifiers. The output from the Loop Buffer Amplifier is used to phase lock the loop. The output from the Output Buffer Amplifier goes to the Low Frequency Loop Section where it is combined with other signals.

Shaping Network

Due to the nonlinear tuning characteristics of the varactor diodes a Shaping Network is required. The Shaping Network conditions the pretune and error signals applied to the varactor in order to ensure that the frequency change is linear with the applied tuning voltage.

The Shaping Network consists of a ladder of diodes that are reverse-biased at successively higher voltage. As the voltage at the collector of Q12 increases, the diodes turn on consecutively and present a lower impedance to the tuning signal.

Current to Voltage Converter

Common-base amplifier Q12 sums the output of the Pretune D/A Converter, current from the +20V source (R53) and the FN Loop Error Voltage from the phase detector. The voltage at the emitter (summing point) is always near zero volts since the base of Q12 is biased one diode drop below ground.

Pretune D/A Converter

The output from the Pretune D/A Converter roughly tunes the VCO to a frequency within the capture range of the phase lock loop. The Pretune D/A Converter cannot, by itself, set the VCO precisely.

Op amp, U1, is connected in the inverting amplifier configuration. Its output voltage is programmed by Frequency Digits DF4 and DF5. Figure 8-409 is a simplified schematic of the Pretune D/A Converter Circuit.

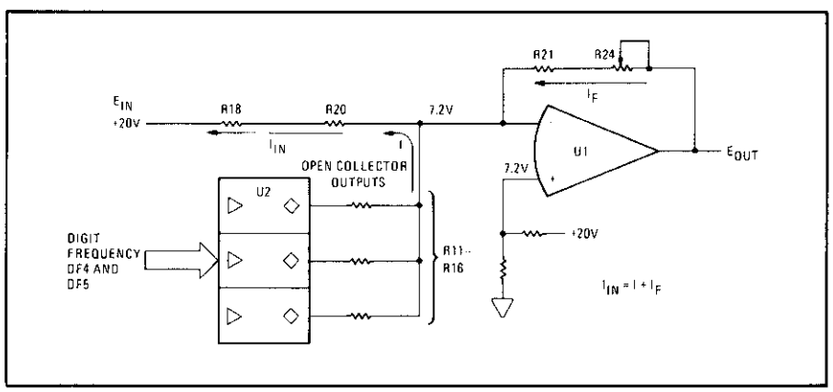


Figure 8-409. Simplified Pretune D/A Converter Circuit

To better analyze how this circuit works, assume that the op amp (U1) is ideal. That is, its gain and bandwidth are both infinity, the input currents and offset are both zero, and there is zero potential difference between the two input terminals. The output voltage, E_{OUT}, is dependent on the feedback current, I_F, that flows through R21 and R24. In the ideal inverting amplifier configuration the feedback current must equal the input current ($I_{IN} = I_F$). The magnitude of the input current I_{IN} is dependent on the potential across R18 and R20. In this circuit the magnitude of I_{IN} remains constant at all times.

If the outputs of U2 are all HIGH (open), there is no current flowing through the pull-up resistors, R11-R16. Hence, the input and feedback currents equal each other. Now, when any of the outputs of U2 goes LOW, current starts flowing into the (-) input node through the pull-up resistors. I_{IN} is no longer equal to I_F, I_{IN} now

equaling I_F + I. Since the value of I_{IN} has to remain constant, the feedback current has to decrease so equilibrium is maintained. A decrease in I_F causes the output voltage, E_{OUT}, to decrease in magnitude.

Speed Control Circuit

The Speed Control Circuit monitors the output from the Pretune D/A Converter circuit. When a change in the pretune voltage is detected, the Speed Control Circuit drives the J-FET switch (Q9) ON. U4B and U4D are comparators. U4B detects a negative going transition while U4D detects a positive going transition. When either transition is detected, the monostable U3 is triggered. This causes comparator U4A to go HIGH which then turns ON J-FET switch Q9.

Speed-Up Switch and Low-Pass Filter

J-FET Q9 is connected in parallel with R42, so when Q9 is turned ON C27 is allowed to charge or discharge at a faster rate. Hence, voltage stored on the capacitor tracks the pretune voltage at a faster rate. Q13 and Q14 form a buffer amplifier that couples the pretune voltage to the emitter of Q12.

To maintain the J-FET switch in the ON state, the gate is biased with a positive voltage. To turn the J-FET switch OFF, the gate is biased with a negative voltage.

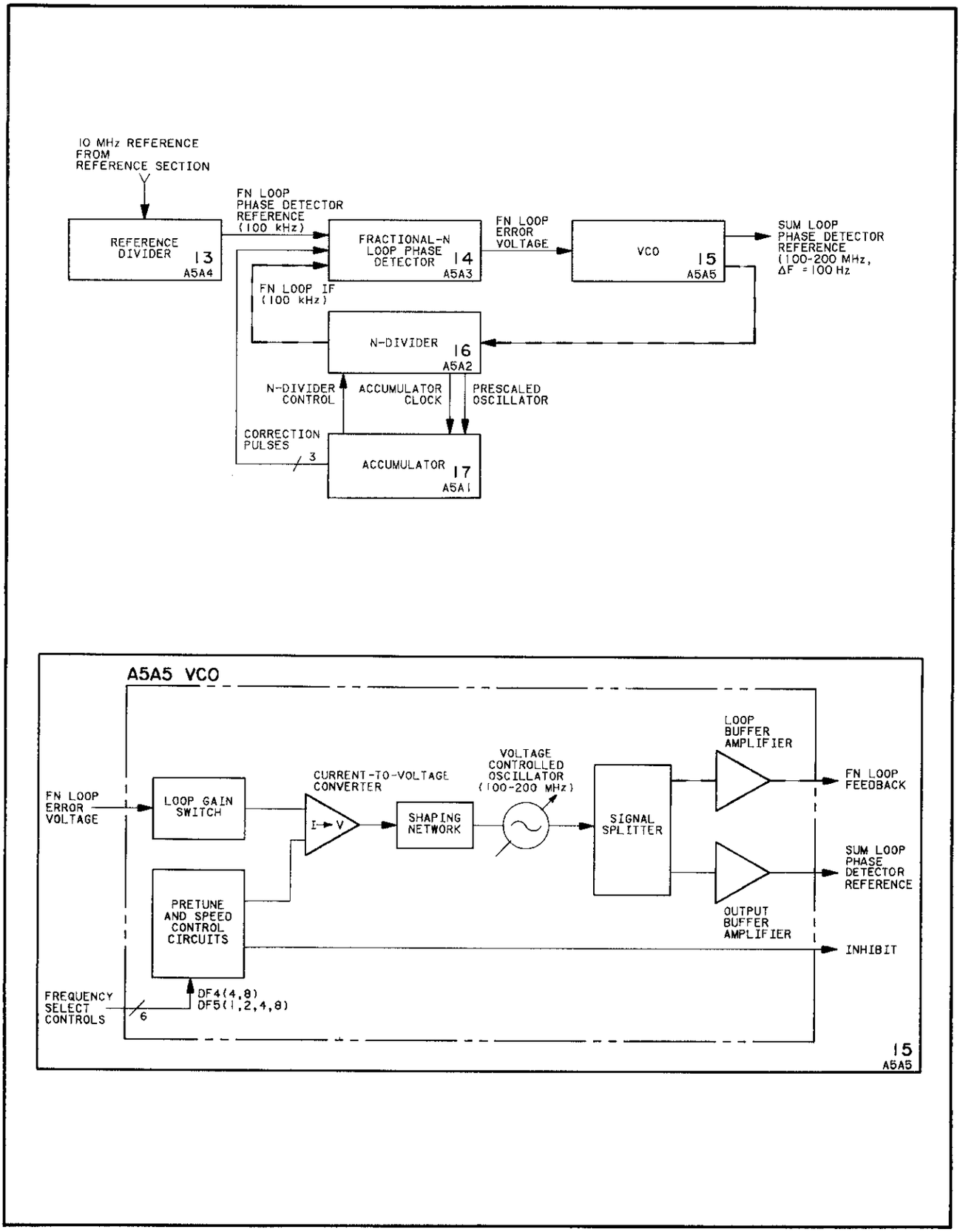


Figure 8-410. A5A5 Fractional-N Loop Voltage Controlled Oscillator Block Diagrams

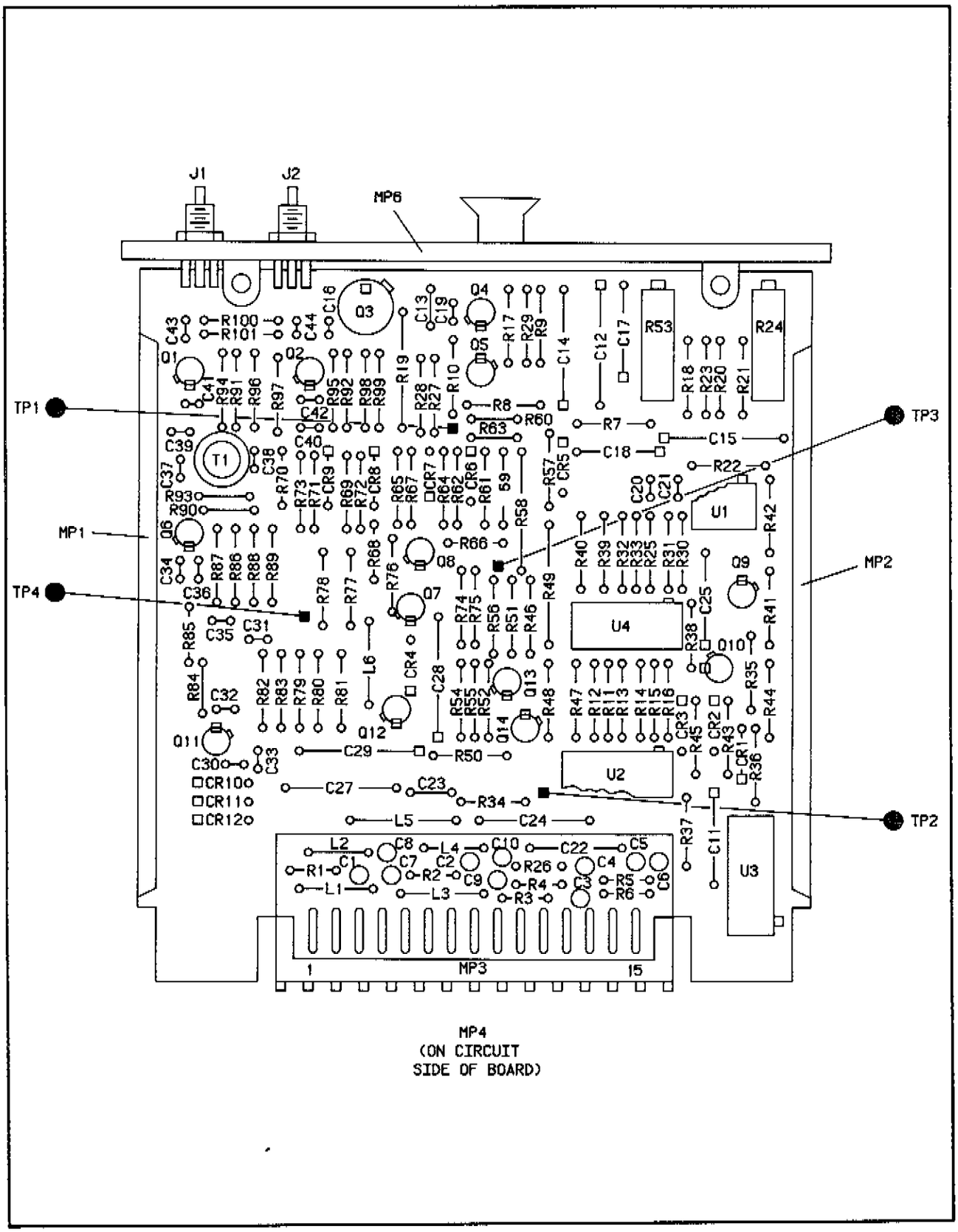


Figure 8-411. A5A5 Fractional-N Loop Voltage Controlled Oscillator Component Locator

CHANGES

All serial prefixes

2604A and Above

On the A5A5 schematic:

- A5A5R1-R6 - Change the value of R1-R6 to 178 ohms.

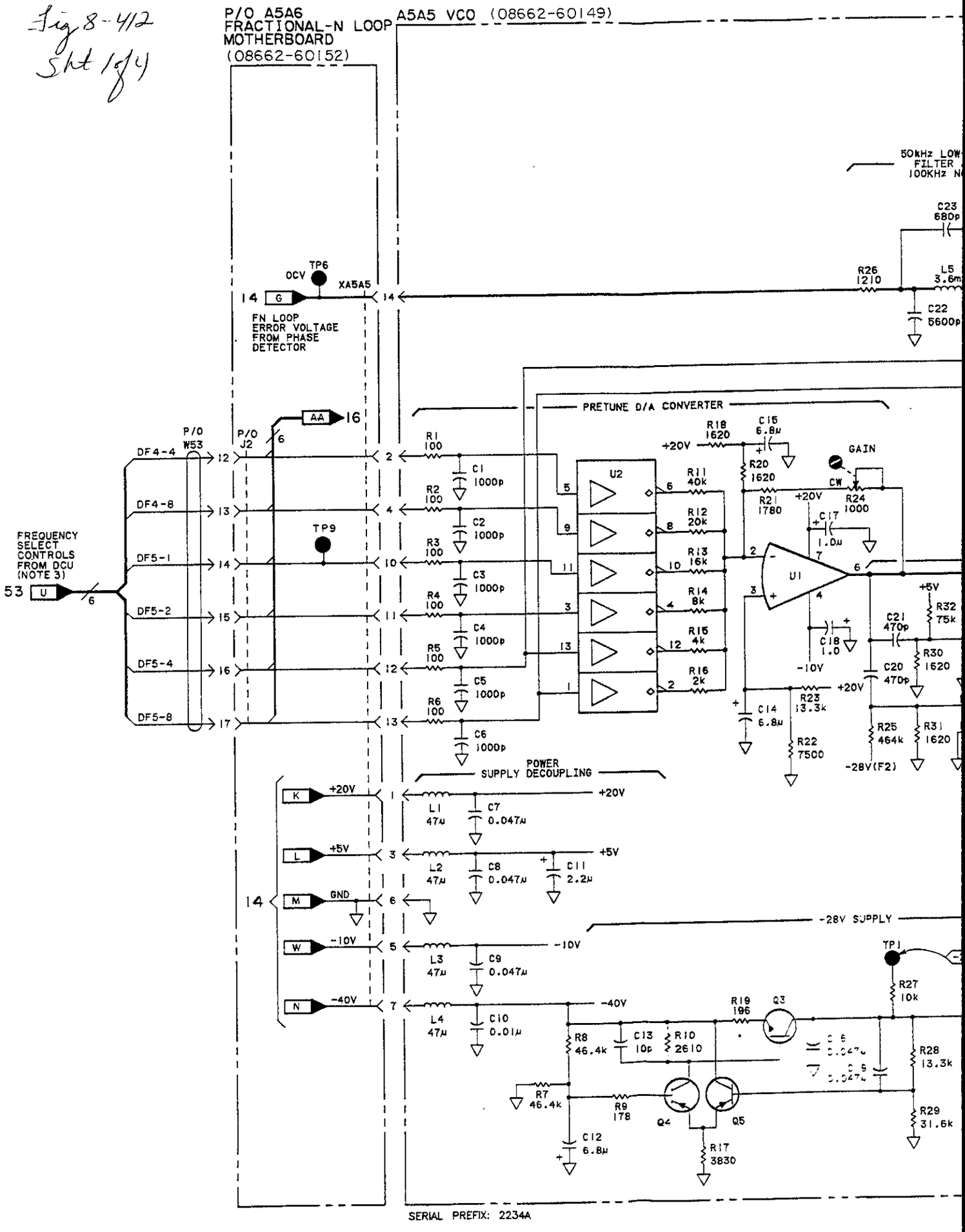
On the A5A5 schematic:

- A5A5CR6-CR9 - Delete CR6-CR9.
- A5A5R53, R54, R58-R61 - Change the values of these resistors to those shown below:

R53	3k
R54	100 ohms
R58	3.83k
R59	56.2k
R60	348 ohms
R61	5.62k

- A5A5R62-R73 - Delete R62-R73.

Fig 8-4/2
Sht 1 of 4



SERIAL PREFIX: 2234A

Fig 8-412 Sht 2 of 4

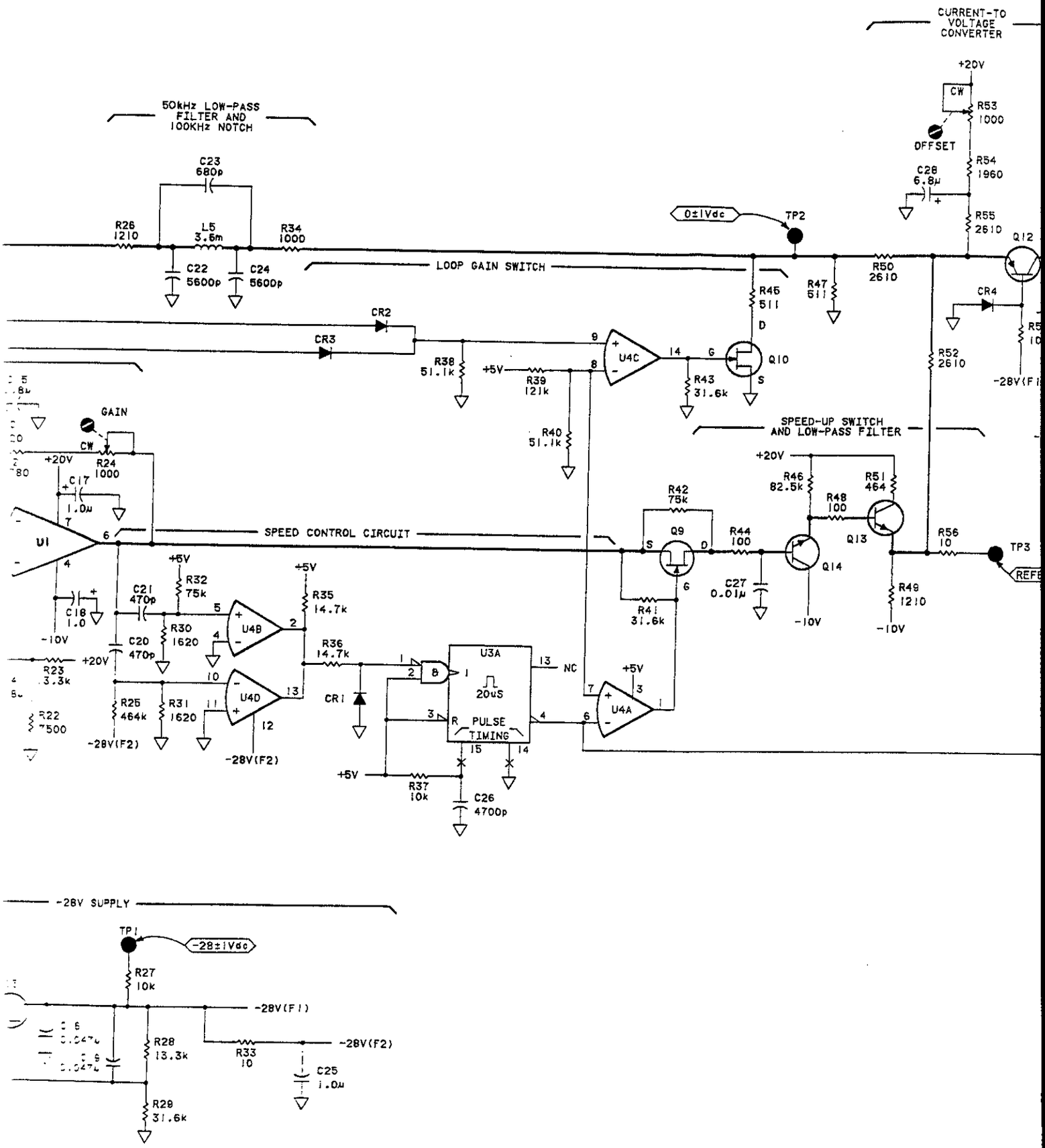
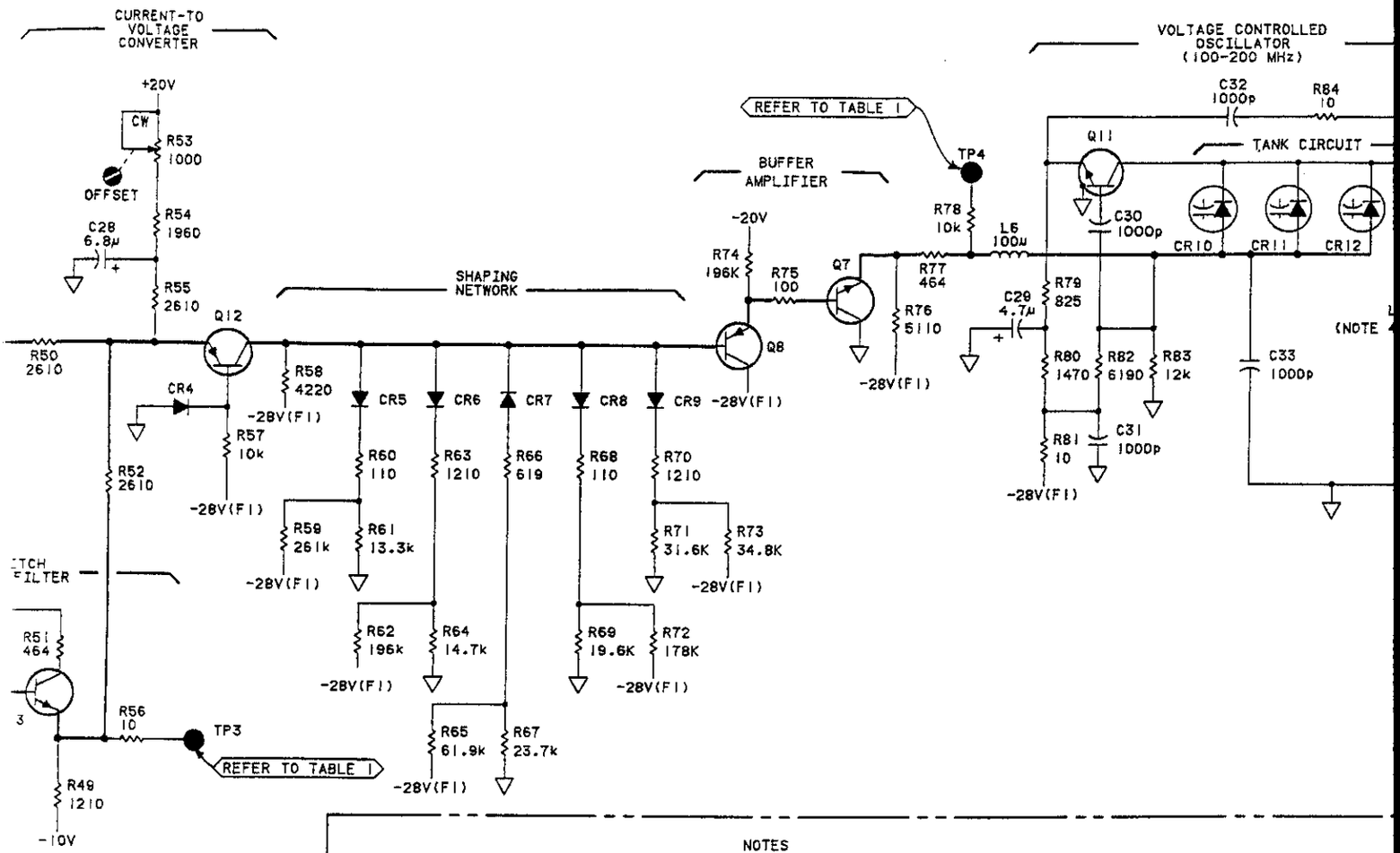


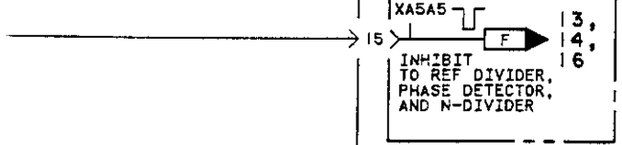
Fig 8-412 Sht 3 of 4



NOTES

1. REFER TO TABLE 8-1D2 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. MNEMONICS DF4-4 TO DF5-8 REPRESENT THE FREQUENCY DIGITS ON THE FRONT PANEL AND THE BCD WEIGHTING
4. INDUCTOR L7 IS A PC TRACE INDUCTOR

P/O A5A6



TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,2,6,11	1854-0540
Q3	1854-0039
Q4,5,8,12,14	1853-0461
Q7,13	1854-0404
Q9,10	1855-0020
U1	1826-0371
U2	1820-0577
U3	1820-1423
U4	1826-0138

REFERENCE DESIGNATIONS

NO PREFIX	A5A6
W23,24 53	J2 TP6,9 XA5A5
A5A5	
C1-44 CR1-12 J1,2 L1-7 Q1-14 R1-101 T1 TP1-4 U1-4	

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U2	+5V - 14 ▽ - 7
U3	+5V - 16 ▽ - 8

Fig 8-412 Sht 4 of 4

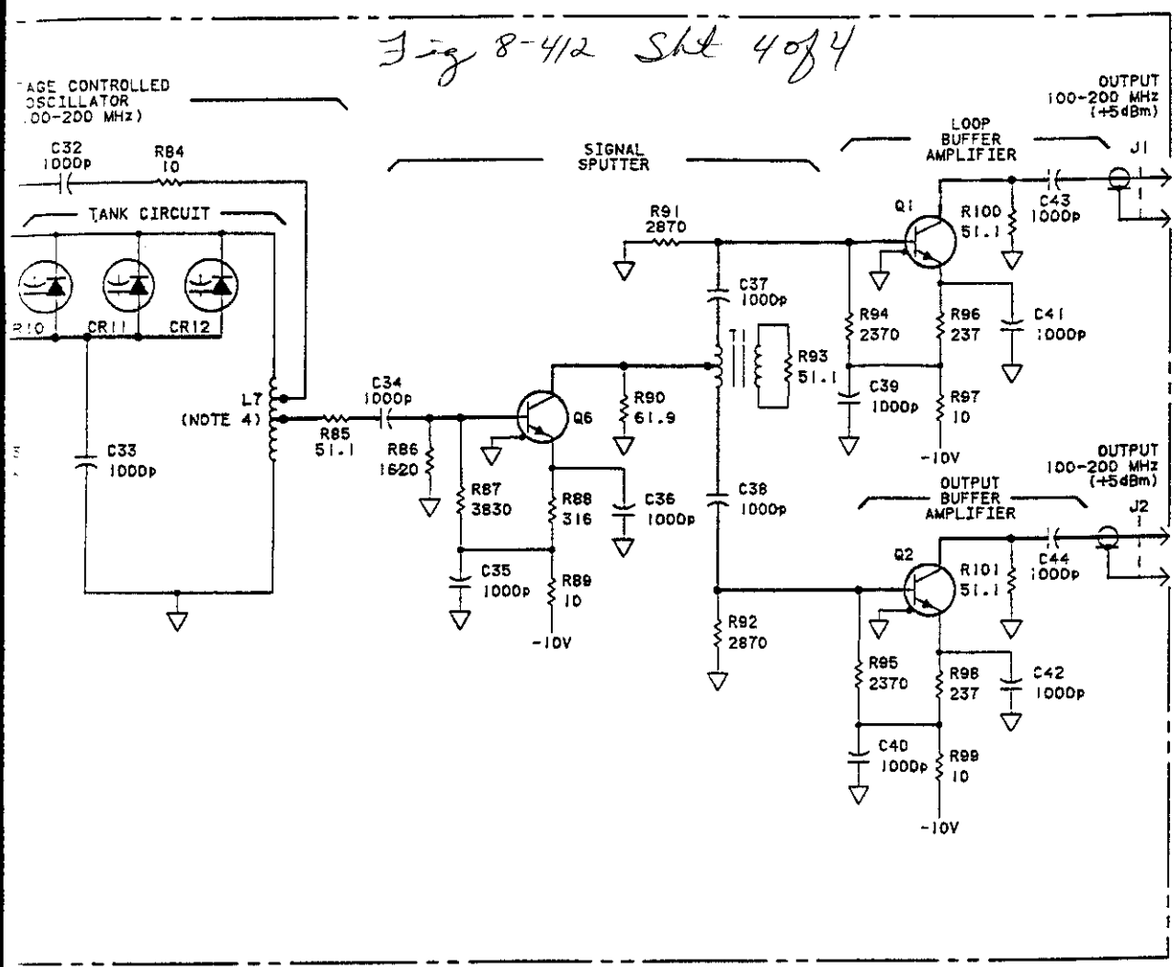


TABLE 1 TUNE VOLTAGE CHECK

FRONT PANEL FREQUENCY SETTING (MHz)	TP3 (Vdc)	TP4 (Vdc)	VCO FREQUENCY (MHz)
320.0	-2.1	-13.5	200.0
320.004	-1.7	-13.0	196.0
320.008	-1.3	-12.4	192.0
320.01	-1.1	-12.2	190.0
320.02	0.0	-11.0	180.0
320.04	+2.1	-8.9	160.0
320.08	+6.2	-3.8	120.0
320.099	+8.0	-1.5	101.0

ISTOR AND
ED CIRCUIT
UMBERS

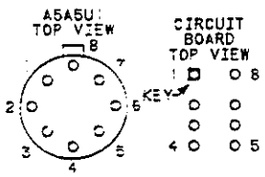
S	PART NUMBERS
	1854-0540
	1854-0039
4	1853-0451
	1854-0404
	1855-0020
	1826-0371
	1820-0577
	1820-1423
	1826-0138

LOGIC LEVEL

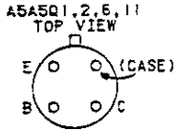
	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW

A5A5U1
TOP VIEW

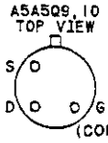
CIRCUIT
BOARD
TOP VIEW



A5A5Q1,2,6,11
TOP VIEW



A5A5Q9,10
TOP VIEW

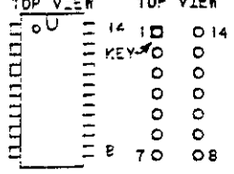


ED CIRCUIT
GE AND
ONNECTIONS

S	PIN NUMBERS
+5V ▽	- 14
	- 7
+5V ▽	- 16
	- 8

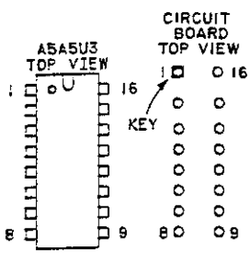
A5A5U2,4
TOP VIEW

CIRCUIT
BOARD
TOP VIEW



A5A5U3
TOP VIEW

CIRCUIT
BOARD
TOP VIEW



SERVICE SHEET 15

A5A5

Figure 8-412. A5A5 Fractional-N Loop Voltage Controlled Oscillator Schematic

SERVICE SHEET 16
A5A2 FRACTIONAL-N LOOP N-DIVIDER

REFERENCE BLOCK DIAGRAM 4
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The purpose of the N-Divider (A5A2) is to divide the Fractional N (FN) Loop VCO frequency (FN Loop N-Divider Drive) down to 100 kHz. The 100 kHz output signal, FN loop IF, is one input to the FN Loop's phase detector. The N-Divider consists of programmable digital dividers (counters) which divide down the VCO frequency. The N-Divider can divide by integers from 1001 through 2000. The frequency digits, DF3, DF4 and DF5, determine the divide-by-N number. In addition the divide by N number can be changed to N-1 by the N-Divider Control (NDC) signal from the Accumulator (A5A1).

Fractional division is accomplished by dividing by N for a number of times and then by N-1 for a number of times. The fractional N is then the average of N and N-1. The N-Divider can divide by a fractional part that has three significant places, for example, a fractional N of 1000.001.

Divide-by-10/11 Prescaler Counter

The divide-by-10/11 Prescaler Counter, U1, is an ECL device which can be programmed to divide by 11 or 10. At the beginning of each reference period the divide-by-10/11 Prescaler Counter divides by 11. It later starts dividing by 10 and remains in the divide-by-10 mode until the end of the reference period. How long it continues to divide by 11 is determined by the divide-by-10/11 Control Circuit. One output from the divide-by-10/11 Prescaler Counter, the Prescaled Oscillator signal (PSO), goes to the Accumulator (A5A1) where it is used as a clock. Note during the time when the Correction Pulses are generated this clock equals the VCO frequency divided by 10.

Divide-by-10/11 Control Circuit

The purpose of the divide-by-10/11 Control Circuit is to control the modulus (10 or 11) of U1. Frequency digit DF3 along with the NDC line determine how long U1 divides by 11 each reference period. Frequency digit DF3 presets the Programmable Decade Counter (U8) while the NDC line controls the terminal count of the Terminal Count Decoder (18). Normally the terminal count is 18 except when the NDC line goes high. When the NDC line goes high the terminal count changes from 18 to 17. Changing the terminal count of the Terminal Count Decoder (18) from 18 to 17 effectively causes the N-Divider to divide by N-1.

U8 starts to count up from its preset value to the terminal count. When counter U8 reaches the terminal count the Terminal Count Latch (U7B) is set and on the next clock the Terminal Count Latch output goes high. This causes counter U1 to start dividing by 10.

Programmable Counters

The Programmable Counter counts all the pulses out of the divide-by-10/11 Prescaler Counter. Frequency digits DF4 and DF5 preset the Programmable Decade Counters U6 and U9 respectively. These counters count from the preset count to the count of 196. The count of 196 is determined by the Terminal Count Decoder (196). When the count reaches 196 the Terminal Count Switch is set up to change state on the next pulse from U1. The output from the Terminal Count Switch (U3B) is fed back to reset both the Programmable Counter and the divide-by-10/11 Control Circuit.

When the loop is phase-locked the output from the Terminal Count Switch is a 50 to 100 ns pulse with an average pulse repetition rate of 100 kHz.

TROUBLESHOOTING

When a Fractional-N Loop problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

There are two types of procedures covered by this procedure.

1. No output pulses produced by A5A2 assembly. Begin troubleshooting with section I of the procedure.

2. Output pulses produced by A5A2 assembly are at the wrong frequency. Begin troubleshooting with section II of the procedure.

No output pulses.

1. Mount the A5A2 assembly on its extender board.

2. Use a logic probe and check for pulses at the outputs of U3B (pins 9 and 7). If pulses are present, the problem is between U3B and the edge connector. If no pulses are present, continue with step 3.

3. Check the output of U2A pin 12 (TP2). This signal should be a TTL pulse train. Check that the signal assumes valid high and low TTL logic levels. If this signal is not normal, the problem is in the prescaler (U1) or translator (U2A), or one of the counters (U6B, U8B, U3B) is pulling down the output of U2A. If this signal is normal, continue with step 4.

4. Connect a jumper between TP4 and TP4A which will allow counters U6 and U9 to free-run. Check that these counters are counting by touching a logic probe to the outputs. Flip-flop U3A should be set. The outputs of U5A (pin 12) and U5C (pin 8) should be normally low but go high when the counters reach the value they are decoding so a logic probe touched to these pins should blink.

   If the counter circuitry is normal, the problem is with the terminal counter switch.

Output pulses of wrong frequency.

1. Mount the A5A2 assembly on its extender board.

2. Connect an extender cable from the service kit between A5A2J1 and A3A4J2. This cable routes the output of the LF N-loop to the input of the A5A2 N-divider assembly.

3. Set the 8663A front panel frequency to 327.8 MHz. This sets the LF N-loop output to 200.0 MHz.

4. Short test points TP4 and TP4A together. This holds flip-flop U7B in the set condition (TP1 high) which keeps counter U1 in the divide-by-10 mode. Measure the frequency at TP2 with the high impedance input of a frequency counter. The frequency should be exactly 20.0 MHz. If it is not, the problem is with flip-flop U7B, counter U1 or associated components.

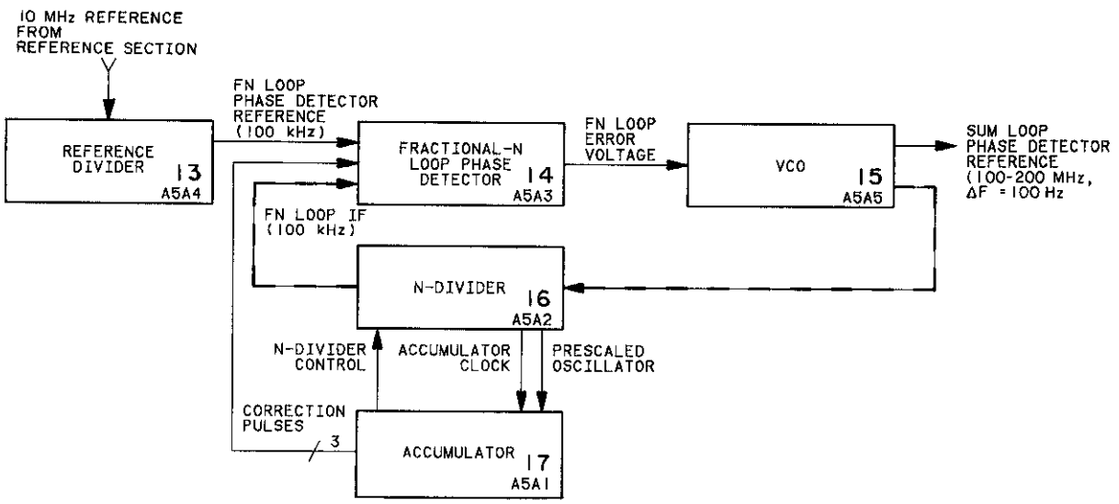
5. Remove the short between TP4 and TP4A. Connect a jumper between TP3 and ground. This holds flip-flop U7B in the clear condition (TP1 low) which keeps counter U1 in the divide-by-11 mode. Measure the frequency at TP2. The frequency should be 18.181818 MHz (200 divided by 11). If it is not, the problem is with flip-flop U7B, counter U1 or associated components.

6. Remove the jumper from TP3. View the signal at TP1 on an oscilloscope. The waveform should be a TTL negative-going pulse approximately 1.1 microsec wide. Set the frequency increment to 100 Hz. Pushing the INCREMENT (up) key should decrease the pulse width in 55 microsec steps.

   If there are no pulses on TP1, the problem could be the pulses coming from flip-flop U3B. Check TP3 for TTL negative going pulses (approximately 50 microseconds wide). The normal period

of these pulses is approximately 10 microseconds, but any period greater than 1.5 microseconds should allow the pulses on TP1, described above, to be produced. If the TP3 pulses are not normal, continue troubleshooting with step 7.

7. Remove the jumper from TP3. Short test points TP4 and TP4A together which makes the output of U2A (pin 12) exactly 20.0 MHz and puts counters U6 and U9 into a free-run mode. The output of U6 (pin 12) should be a 2.0 MHz signal and the output of U9 (pin 12) should be a 200.0 kHz signal.



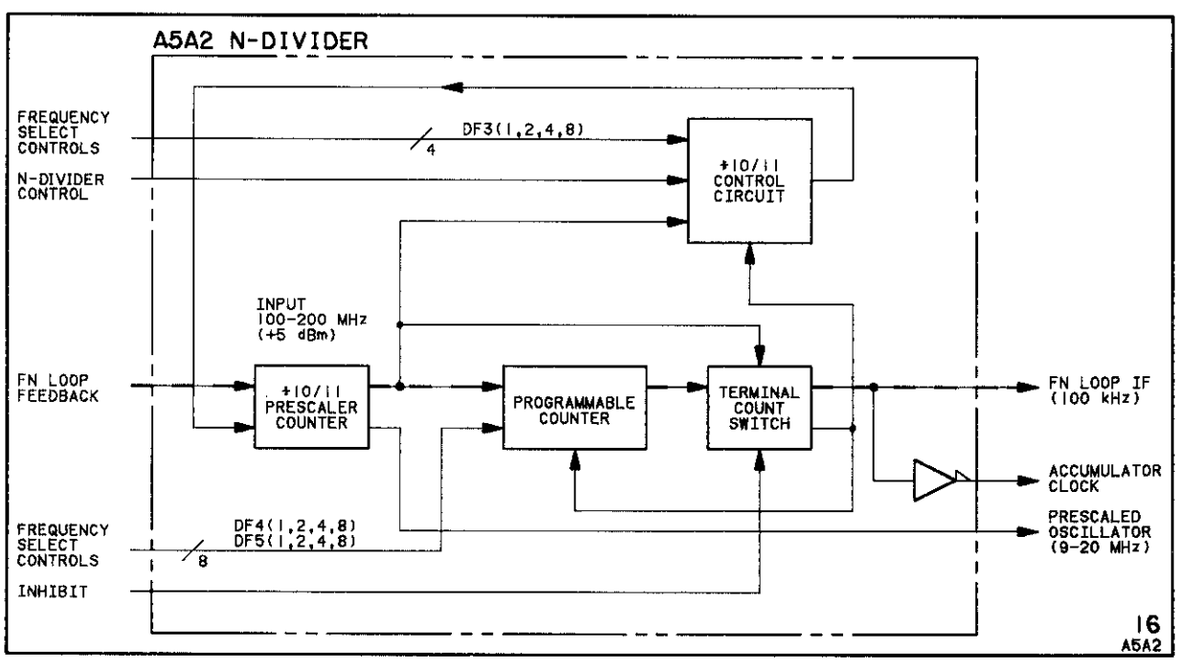


Figure 8-413. A5A2 Fractional-N Divider Block Diagrams

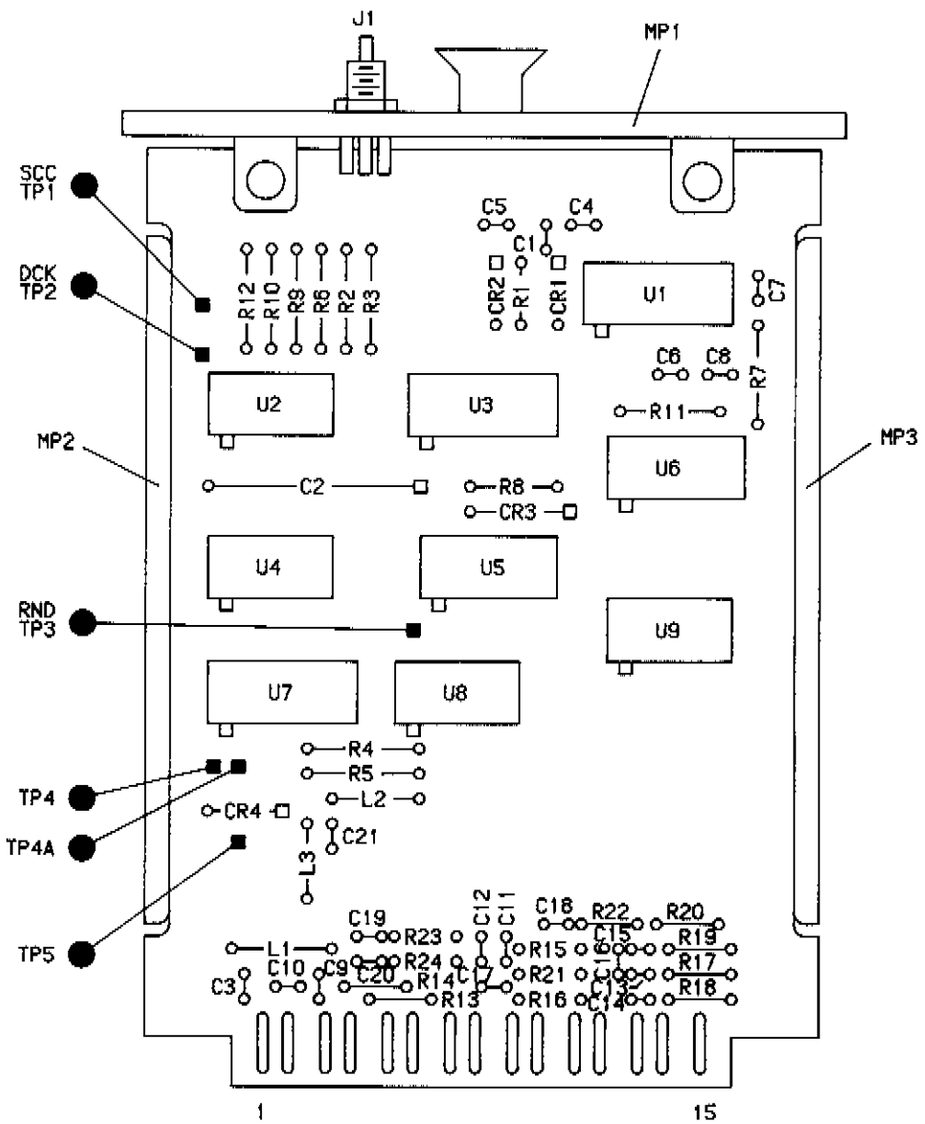
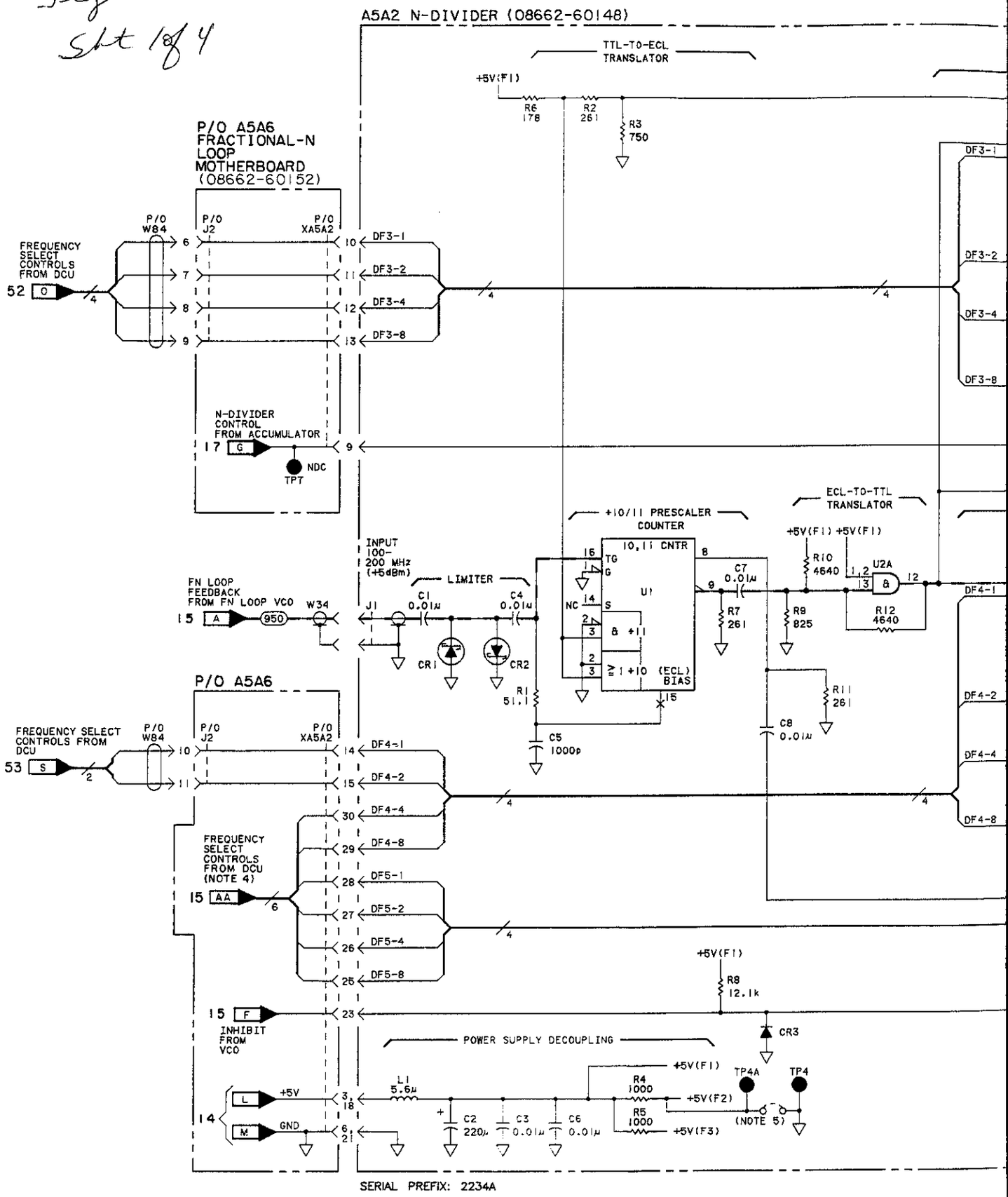


Figure 8-414. A5A2 Fractional-N Divider Component Locator

Fig 8-415
Sht 1 of 4



SERIAL PREFIX: 2234A

Fig 8-415 Sht 2 of 4

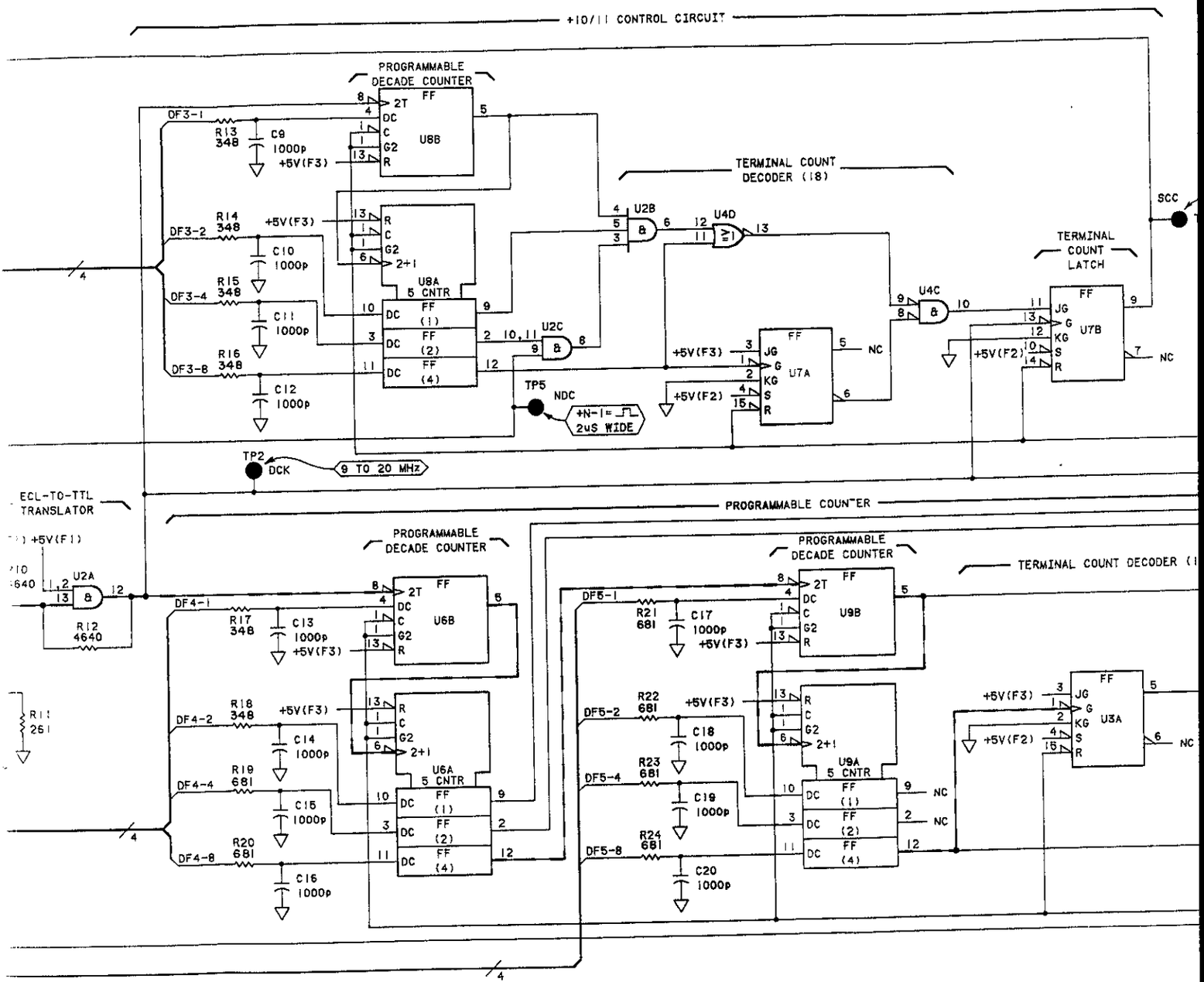
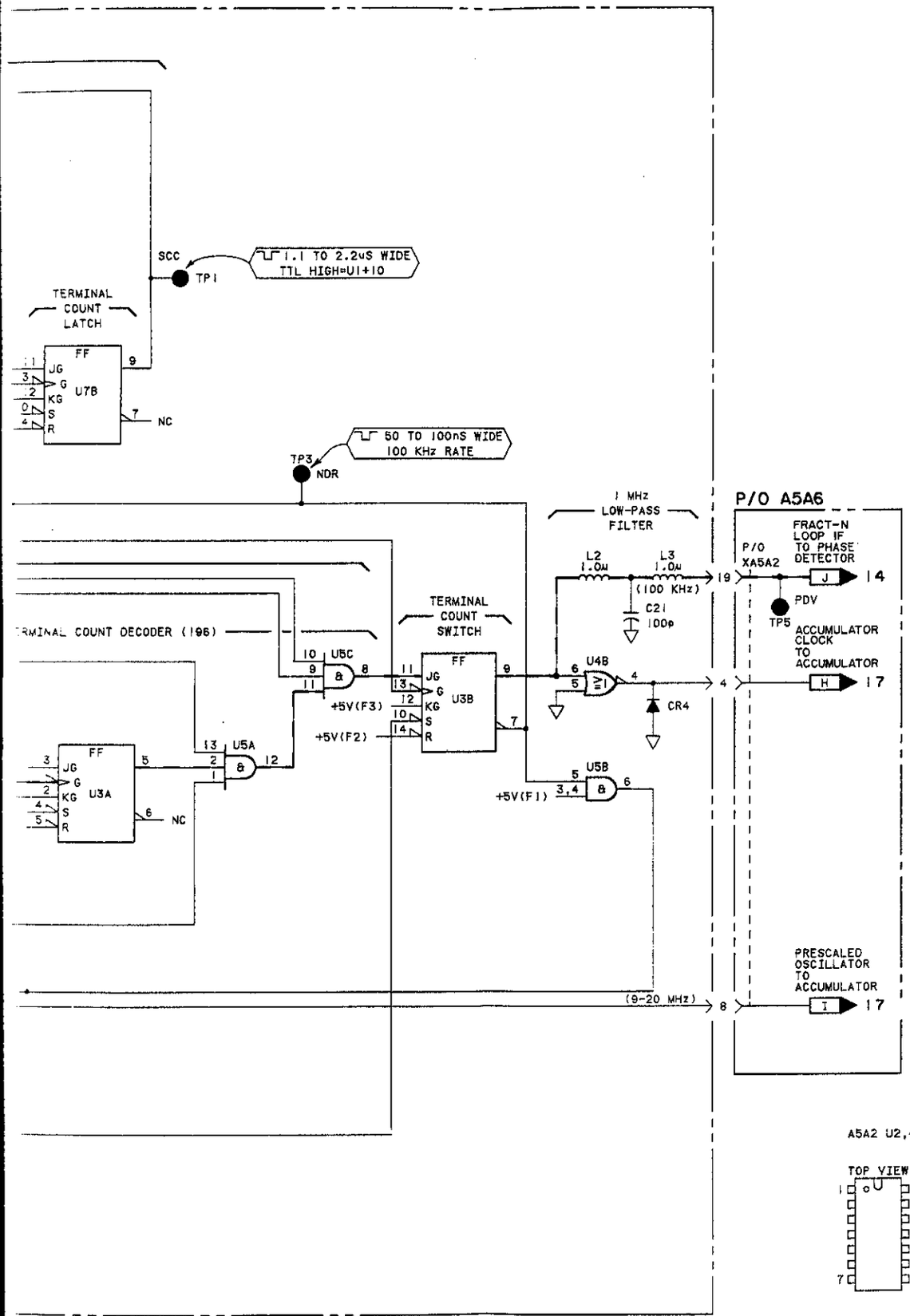


Fig 8-415 Sht 3 of 4



NOTES

1. REFER TO TABLE 8-102 FOR DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ... THEY ARE ACTUAL MEASURED ... YOUR MEASUREMENTS MAY BE ... DIFFERENT THAN WHAT IS ...
3. LOGIC LEVEL FOR ECL DEV... THIS INSTRUMENT ARE NON... DUE TO THE SUPPLY VOLTA... A HIGH LEVEL IS >+4.0; ... LEVEL IS <+3.5V.
4. MNEMONICS DF3-1 TO DF5-... REPRESENT THE FREQUENCY ... ON THE FRONT PANEL AND ... BCD WEIGHTING.
5. JUMPER IS INSTALLED FOR ... SHOOTING PURPOSES ONLY. ... JUMPER SETS FLIP-FLOPS ... AND U3B

REFERENCE DESIGNAT...

NO PREFIX	A5A
W24 53	J2 TP5, XA5A
A5A2	
C1-21 CR1-4 L1-3 R1-24 TP1-5 U1-9	

LOGIC LEVELS

	TTL	E (NO
HIGH	>+2V	>+
LOW	<+0.8V	<+
< IS MORE NEG. TH...		
> IS MORE POS. TH...		
OPEN	HIGH	
GROUND	LOW	H

TRANSISTOR ... AND INTEGRAT... CIRCUIT PART NU...

REFERENCE DESIGNATIONS	NU...
U1	1820
U2,5	1820
U3,7	1820
U4	1820
U6,8	1820
U9	1820

INTEGRATED CIR... VOLTAGE AN... GROUND CONNECT...

REFERENCE DESIGNATIONS	NU...
U1	+5V(▽
U2,4-6,8,9	+5V(▽
U3,7	+5V(▽

A5A2 U2,4-6,8,9 — CIRCUIT BOARD TOP VIEW — A5A2 U1,3

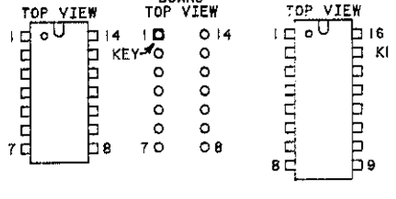


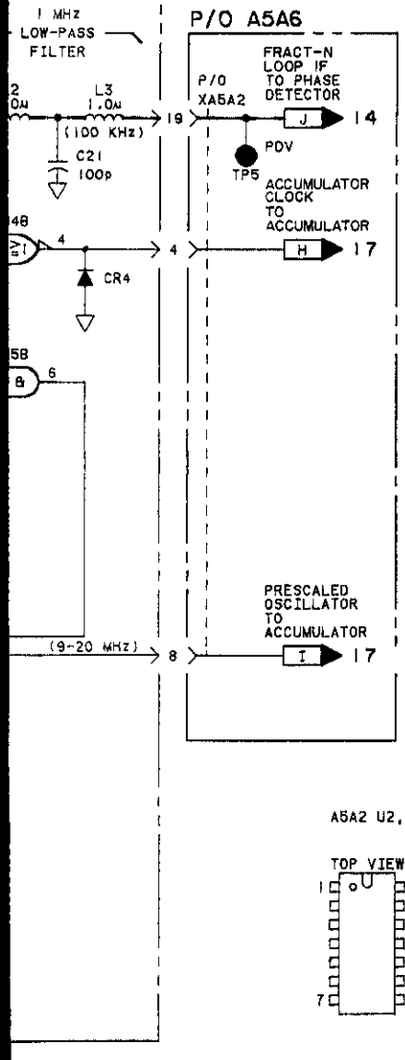
Fig 8-415
Sht 4 of 4

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. LOGIC LEVEL FOR ECL DEVICES IN THIS INSTRUMENT ARE NONSTANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS >+4.0; A LOW LEVEL IS <+3.5V.
4. MNEMONICS OF3-1 TO OF5-8 REPRESENT THE FREQUENCY DIGITS ON THE FRONT PANEL AND THE BCD WEIGHTING.
5. JUMPER IS INSTALLED FOR TROUBLE-SHOOTING PURPOSES ONLY. INSTALLING JUMPER SETS FLIP-FLOPS U7A,U7B,U3A AND U3B

REFERENCE DESIGNATIONS

NO PREFIX	A5A6
W24 53	J2 TP5,7 XA5A2
A5A2	
C1-21 CR1-4 L1-3 R1-24 TP1-5 U1-9	



LOGIC LEVELS

	TTL	ECL (NOTE 3)
HIGH	>+2V	>+4.0V
LOW	<+0.8V	<+3.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	LOW
GROUND	LOW	HIGH

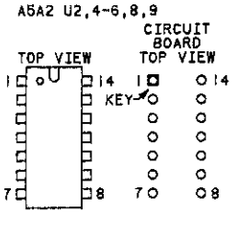
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U1	1820-1780
U2,5	1820-0686
U3,7	1820-0629
U4	1820-1322
U6,8	1820-2049
U9	1820-1251

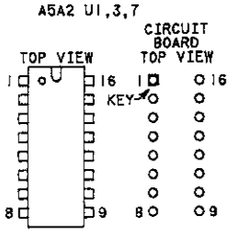
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V(F1)-4,5 ▽ - 12
U2,4-6,8,9	+5V(F1)- 14 ▽ - 7
U3,7	+5V(F1)- 16 ▽ - 8

A5A2 U2,4-6,8,9



A5A2 U1,3,7



SERVICE SHEET 16

A5A2

Figure 8-415. A5A2 Fractional-N Divider Schematic

SERVICE SHEET 17
A5A1 FRACTIONAL-N LOOP ACCUMULATOR

REFERENCE BLOCK DIAGRAM 4
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

General

The purpose of the Accumulator (A5A1) is to determine when to divide by N or divide by N-1. The Accumulator computes the phase difference between the VCO/N (FN Loop IF) and the 100 kHz reference (FN Loop Reference). This information is used to develop the N Divider Control signal (NDC) and the Correction Pulses. The Accumulator consists of three major sections which are the Algorithmic State Machine, Summing Circuitry, and the Digital to Pulse Converter.

Algorithmic State Machine

The Address Generator along with the State Controller form a small Algorithmic State Machine (ASM). The ASM generates a set of control signals or instructions which properly sequences the Summing Circuitry and the Digital to Pulse Converter. The control signals or instructions are determined by the program stored in ROM (U6).

The ASM generates a total of seventeen instructions. The seventeenth instruction is a halt command which resets and disables the Address Generator (U1 and U2). The ASM remains in the halt state until the end of a reference period. A clock pulse, labeled Accumulator Clock, is generated at the end of each reference period. This pulse restarts the Address Generator and the whole sequence is repeated again.

Summing Circuitry

The fractional portion of the VCO frequency contains the information needed to develop the N Divider Control (NDC) and the Correction pulses. The fractional portion of the VCO frequency is entered into the Accumulator in BCD form (DF0 through DF2). These BCD lines, DF0 through DF2, carry information which corresponds to the front panel frequency digits D0 through D2. The Summing Circuitry takes the BCD data, adds it to the previous sum, and stores it in the Accumulator Registers (U19, U7, and U5). Each reference period the content of the Accumulator Registers is incremented by the fractional portion. The number stored in the Accumulator Registers corresponds to the difference in phase between the VCO signal and the reference signal. When the accumulated total reaches or exceeds unity an NDC signal is generated.

To better understand the operation of the Summing Circuit, let's go through an example. When analyzing the operating of the Summing Circuitry it is better to view it in terms of reference periods. Let's assume that the Accumulator Registers initially contains the number zero and the fractional portion equals the number 207, that is, DF0=7, DF1=0, and DF2=2. At the beginning of the reference period the Input Multiplexer selects the four BCD lines which corresponds to the DF0 and steers the BCD data to the BCD Adder. The BCD Adder adds the DF0 number (7) to the number stored in U5. Since U5 contains the number zero, the resulting sum is just the number DF0. The sum is then latched into U10. At the same time the previous content stored in U10 is shifted into U7 while the previous content of U7 is shifted into U5 (shift right). This sequence is then repeated for both DF1 and DF2, respectively. Figure 8-416 shows the content of the Accumulator Registers after the end of one reference period. Note at the end of the reference period, DF0 is stored in U5, DF1 is stored in U7, and DF2 is stored in U10.

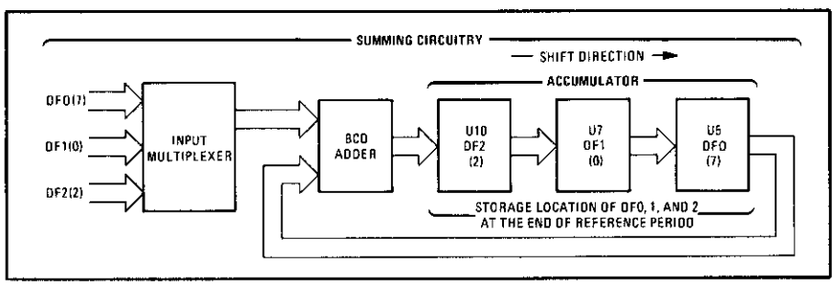
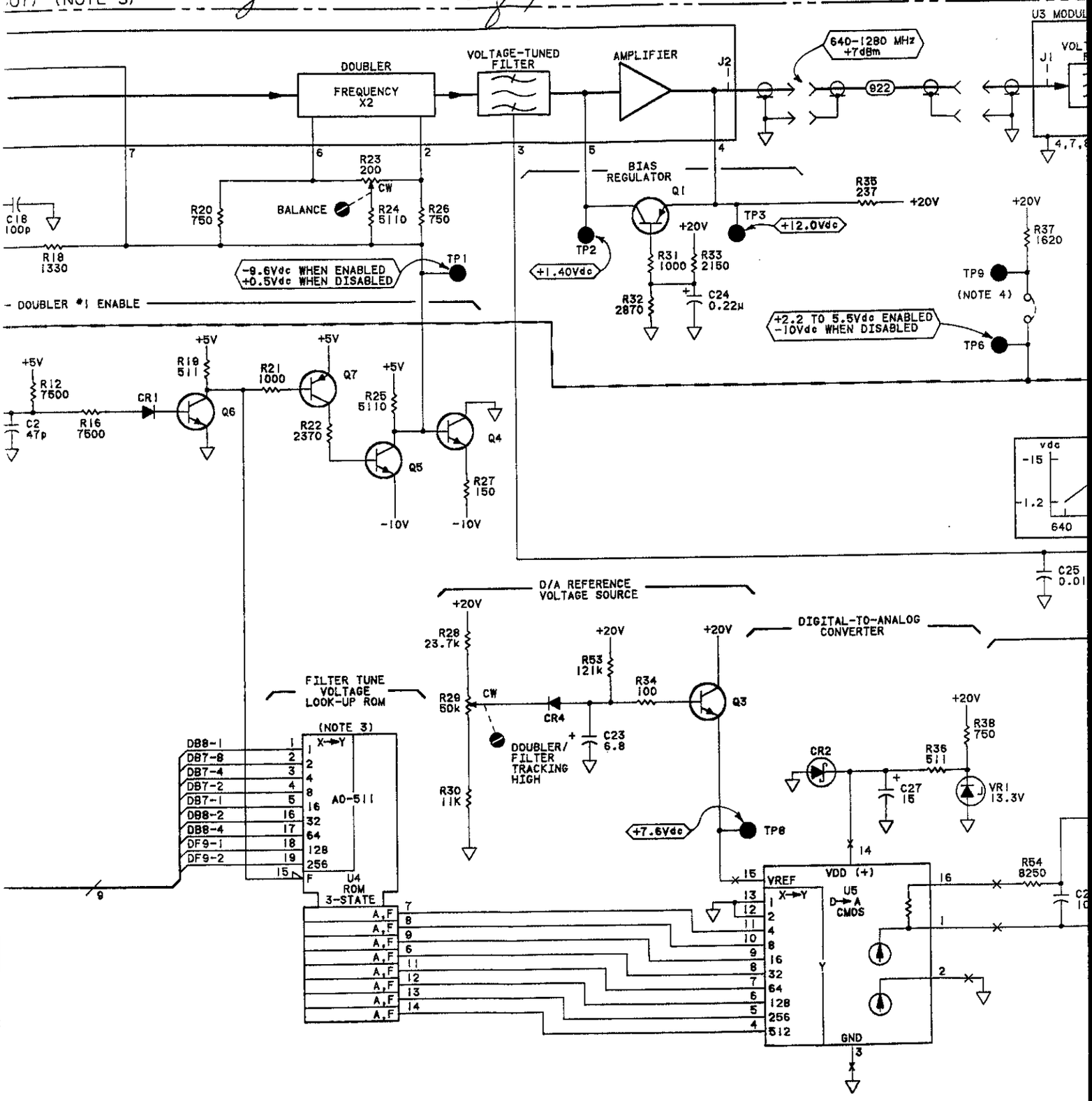


Figure 8-416. Summing Circuitry Simplified Block Diagram Showing the Content of the Accumulator after each Reference Period

At the beginning of the next reference period DF0 is again selected first and steered to the BCD Adder. DF0 is added to the content stored in U5 which now contains the result of the previous addition of DF0. Again this sequence is repeated for DF1 and DF2. The net result is that the content of the Accumulator Registers is incremented by the fractional portion every reference period. Table 8-401 illustrates this point.

.07) (NOTE 3) Fig 8-518 Sht 2 of 4



the three outputs. The order in which the pulses are outputed is Correction Pulse 3, Correction Pulse 2, and Correction Pulse 1.

The Programmable Counter along with the 15 Decoder determines the pulse width (negative going) of each Correction Pulse. The 15 Decoder circuit causes the counter to reset when it reaches the count of 15. The Programmable Counter is preset by the complemented of the BCD number stored in register U5. The Program Counter is clocked by the Prescaled Oscillator (PSO) signal. During the interval when the Correction Pulses are being developed, the PSO frequency equals the FN Loop VCO frequency divided by ten. The time it takes for the Program Counter to count from its preset value to 15 determines the pulse width. The pulse width can be calculated by the following formula:

Pulse Width = 10 x (number in U5 +1) x VCO Cycle Wide

For example if U5 contains the number 0, a 10 VCO cycle wide pulse is generated. If U5 contains the number 9, a 100 VCO cycle wide pulse is generated. Note if the FN Loop operates with no fractional part, the pulse width of the Correction Pulses remains constant from reference period to reference period. However, if the loop is operating with a fractional part, the Correction Pulses will vary in duration every reference period. Also note, the pulse duration will be the longest when the phase difference is at its maximum value.

TROUBLESHOOTING

When a Fractional-N Loop problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem. Signature analysis is used to troubleshoot this assembly. The normal operation of the A4A1 assembly provides the stimulus needed to drive the HP 5004A Signature Analyzer. Any special set-up requirements are listed under the signature tables.

Set-up

1. Mount the A5A1 assembly on an extender board from the service kit.

2. Set the Signature Analyzer switches as follows:

HP 5004A	Pushbuttons
START	_/‾ (OUT)
STOP	‾_ (IN)
CLOCK	_/‾ (OUT)
HOLD	(OUT)
SELF TEST	(OUT)

3. Connect the Signature Analyzer to the A5A1 assembly as follows:

HP 5004A	A5A1 Assembly
STOP	U11 pin 6
START	U11 pin 6
CLOCK	U2 pin 6
GND	TP4A

4. Run a cable from the Signal Generator rear panel 10 MHz reference output to the A5A2J1 connector.

Initialization

1. Set frequency to 320.0 MHz.
2. Short TP1 and TP1A. Remove any other jumpers connected to these test points.
3. Remove short and connect jumper from U11 pin 6 to TP1A.
4. Set frequency to test value.

Test Procedure

1. Touch the SA probe to +5V on the A5A1 assembly.

signature: OHA5

If this signature is correct, the set-up is correct so continue troubleshooting with step 2. Otherwise, there is a problem with the set-up or the state controller circuitry on A5A1. SA cannot be used until the +5V signature is correct. Troubleshoot the state controller using the information in the timing diagram (Figure 8-417).

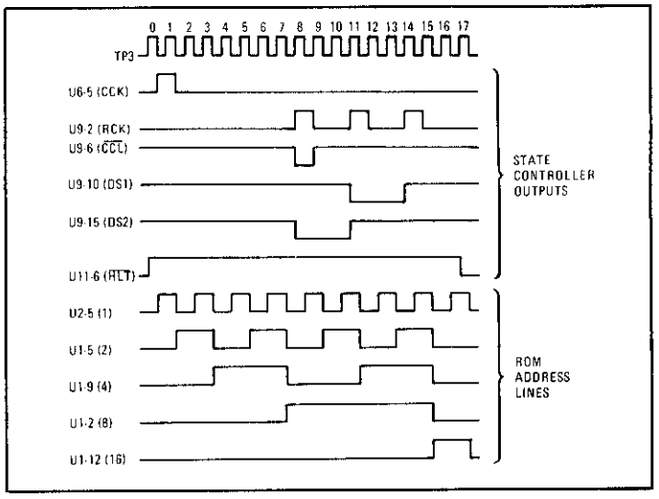


Figure 8-417. State Controller Timing Diagram

2. Check the state controller by verifying the signature at the output of U9. Correct signatures are shown in the signature tables.

   If these signatures are correct, continue troubleshooting with step 3. Otherwise, there is a problem in the state controller so check the signatures at U9 (input), U6 and U1 to isolate the cause of the problem.

3. Set the 8663A front panel frequency to 320.0999596 MHz. Short TP1 and TP1A together. Check the signatures at the output of U7 and U10. Correct signatures are shown in the signature tables.

   If these signatures are correct, continue troubleshooting with step 4. Otherwise, there is a problem in the summing circuitry so check the signatures at U14, U15 and U16 to isolate the cause of the problem.

4. Perform the initialization procedure for checking U5 specified in the signature table. Check signatures at frequency settings of 320.099960 and 320.099990 MHz. The initialization procedure must be performed each time the frequency setting is changed.

   If these signatures are not correct, U5 is the likely cause. Otherwise, the problem is in one of the circuit elements that cannot be checked by signature analysis. Those elements not checked by this procedure are:

U13A	U8A	U12A
U13B	U8B	U12B
U11B	U3A	U12C
	U3B	

5. Set the 8663A front panel frequency to 320.0999596 MHz. This causes all the circuitry on the A5A1 assembly to be active and a logic probe or oscilloscope can be used to check proper circuit operation.

Accumulator (A5A1) Signatures

U1- 1	----	
2	C2C5	
3	----	
4	----	
5	1182	
6	----	
7	----	
8	----	
9	3409	
10	----	
11	----	
12	01UF	
13	----	
14	----	
*U5- 1		
2	7U39	
3	729F	
4	C16H	
5	0000	
6	OHA5	
7	0000	
8	----	
9	2P86	
10	0000	
11	OHA5	
12	0000	
13	C16H	
14	729F	
15	7U39	
16	----	
**U5- 1	----	
2	0000	
3	OHA5	
4	0000	
5	C16H	
6	729F	
7	7U39	
8	----	

**U5- 9	2P86	
10	7U39	
11	729F	
12	C16H	
13	0000	
14	OHA5	
15	0000	
16	----	
U6- 1	P8C9	
2	A6H3	
3	1C79	
4	5CA9	
5	2C5F	
6	000U	
7	----	
8	----	
9	----	
10	21H4	
11	1182	
12	3409	
13	C2C5	
14	01UF	
U7- 1	----	
2	----	
3	----	
4	CFF8	
5	C16H	
6	540H	
7	59A8	
8	----	
9	----	
10	2P8C	
11	----	
12	P560	
13	P8F5	
14	59A8	
15	540H	
16	----	

U9- 1		
2	2P8C	
3		
4	P8C9	
5	A6H3	
6	77F8	
7	7A6H	
8		
9	----	
10	CFF8	
11	C16H	
12	1C79	
13	5CA9	
14	P560	
15	P8F5	
16	----	
U10- 1	----	
2	----	
3	----	
4	P8F5	
5	P560	
6	CFF8	
7	C16H	
8	----	
9	----	
10	2P8C	
11	----	
12	59A8	
13	540H	
14	C16H	
15	CFF8	
16	----	
U14- 1	0000	
2	0000	
3	0000	
4	C16H	
5	----	
6	0000	

U14- 7	CFF8	
8	----	
9	C16H	
10	P560	
11	P8F5	
12	0000	
13	P8F5	
14	P560	
15	CFF8	
16	----	
U15- 1	----	
2	P560	
3	----	
4	0000	
5	OHA5	
6	OHA5	
7	P8F5	
8	----	
9	P560	
10	0000	
11	0000	
12	OHA5	
13	----	
14	C16H	
U16- 1	----	
2	P560	
3	----	
4	OHA5	
5	0000	
6	OHA5	
7	CFF8	
8	----	
9	C16H	
10	0000	
11	OHA5	
12	0000	
13	----	
14	C16H	

* Test Frequency 320.09996 MHz
** Test Frequency 320.09999 MHz

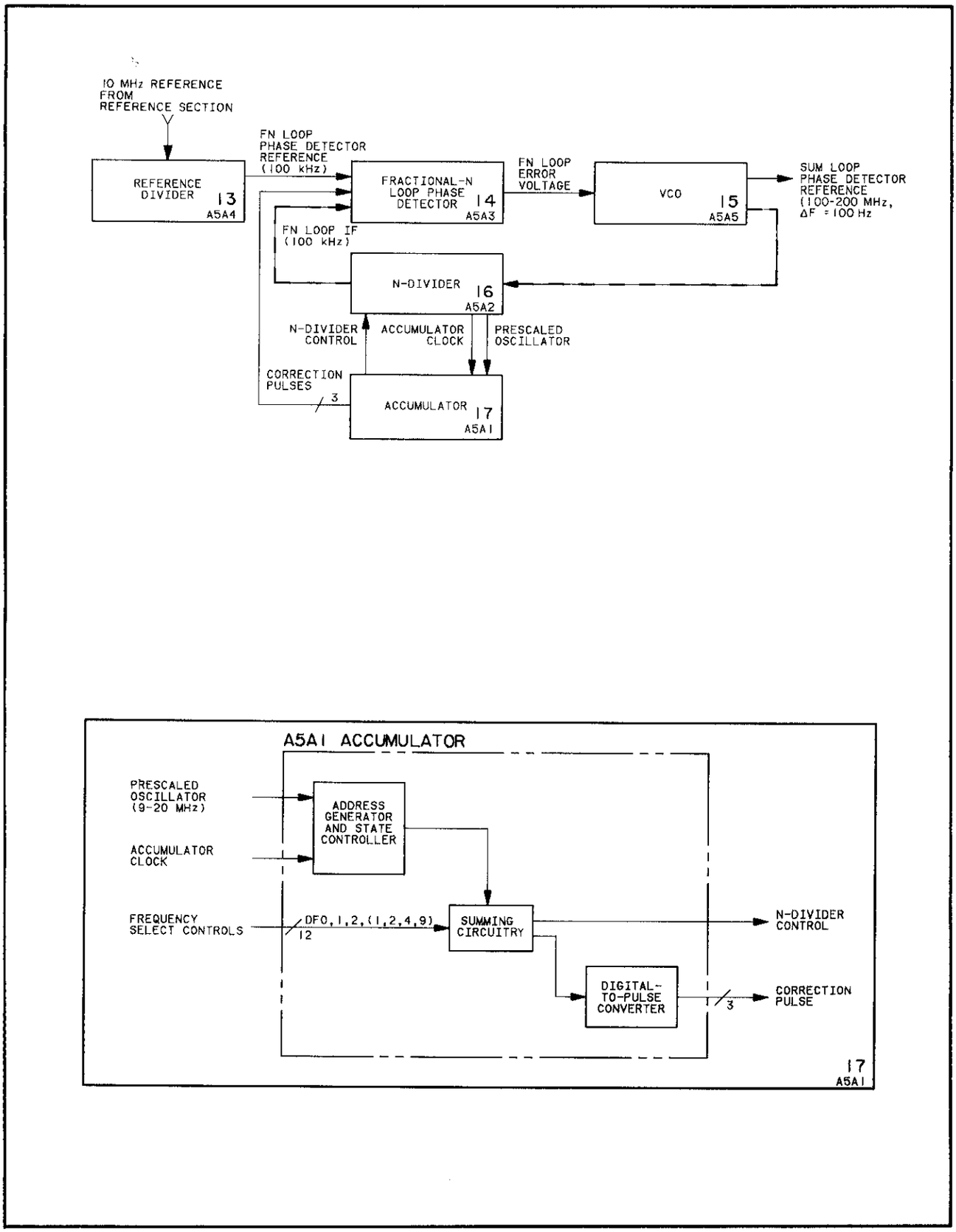


Figure 8-418. A5A1 Fractional-N Loop Accumulator Block Diagrams

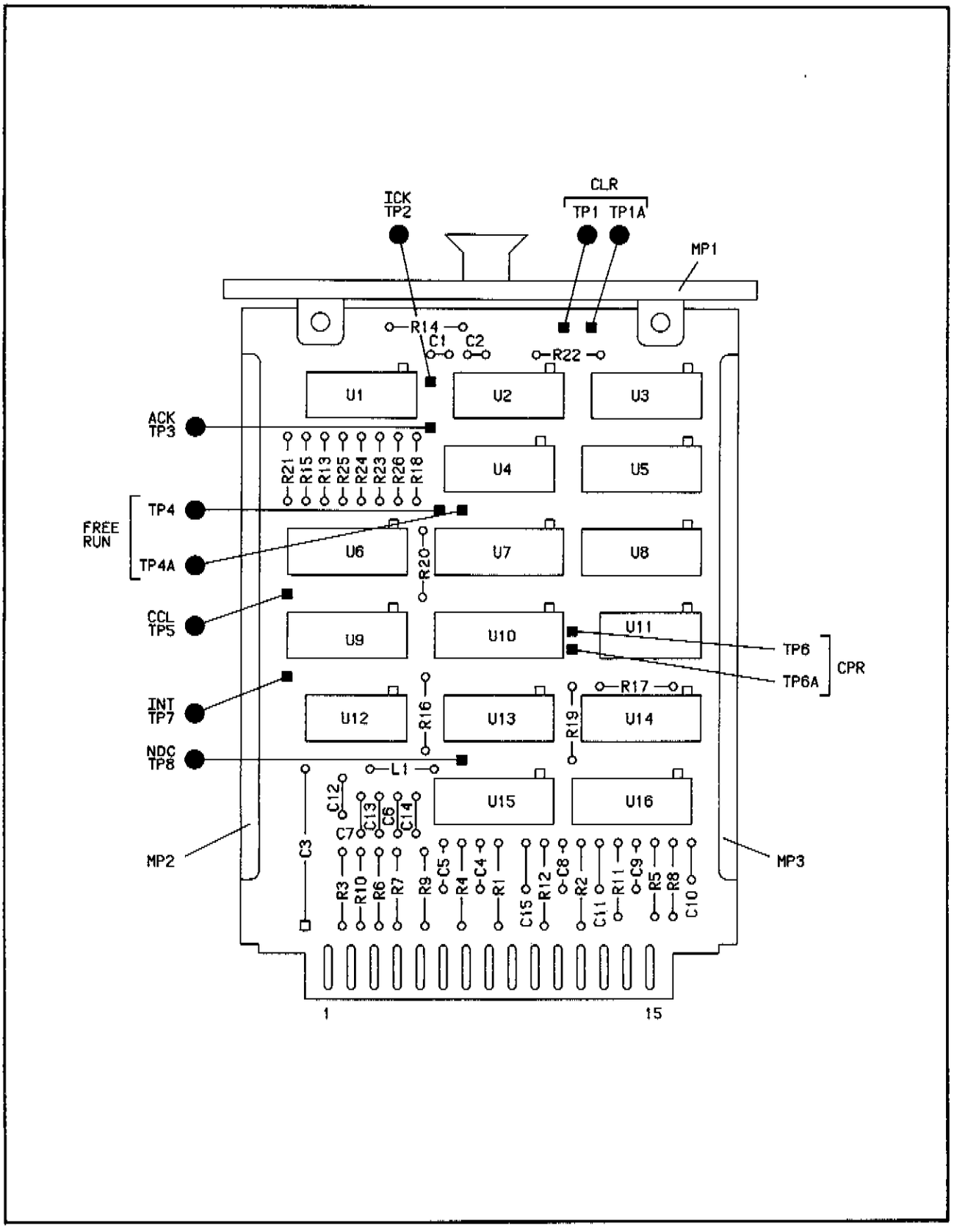
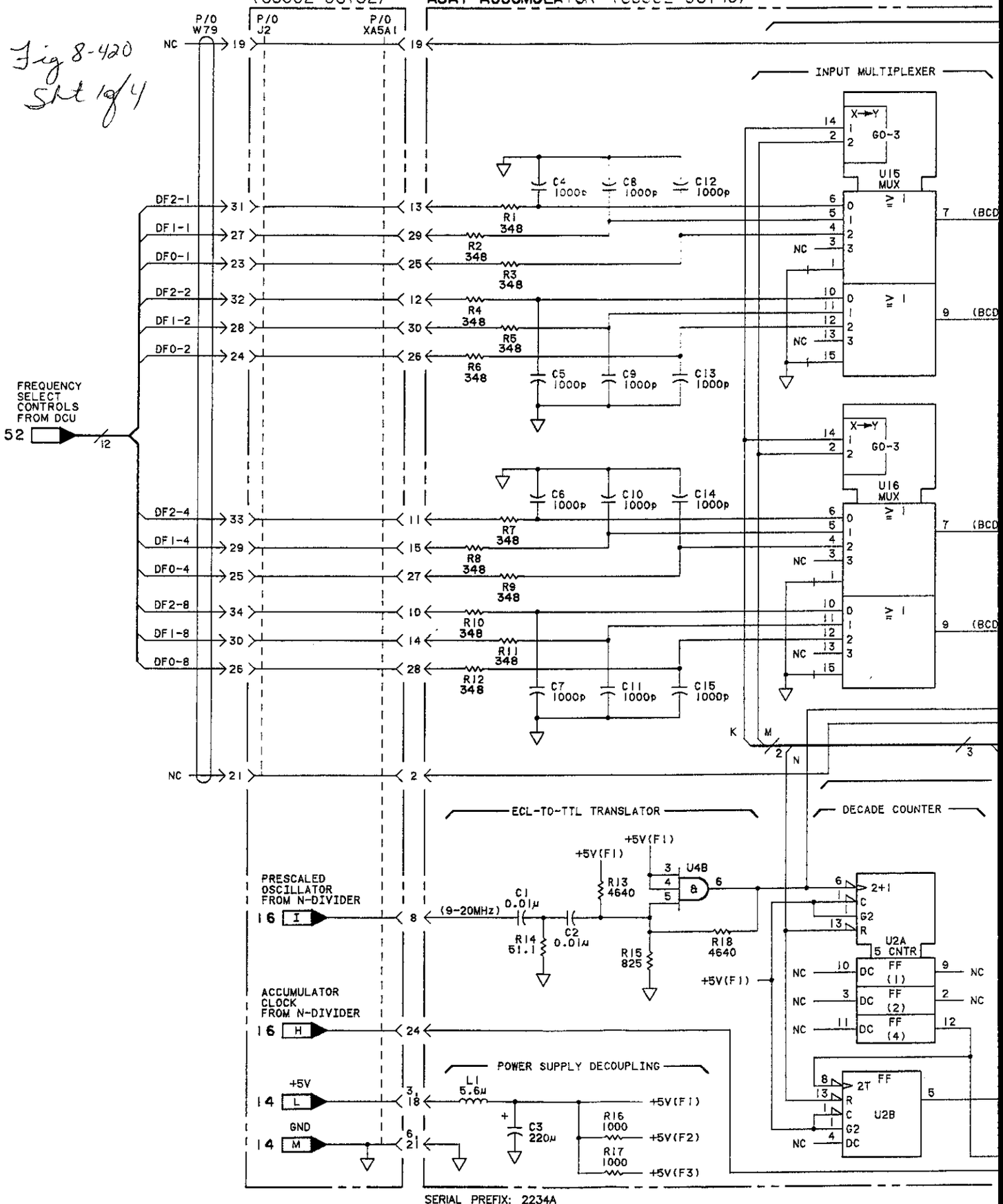


Figure 8-419. A5A1Fractional-N Loop Accumulator Component Locator

Fig 8-420
Sht 1 of 4

P/O A5A6
FRACTIONAL-N LOOP
MOTHERBOARD
(08662-60152)

A5A1 ACCUMULATOR (08662-60146)



SERIAL PREFIX: 2234A

Fig 8-420 Sht 2 of 4

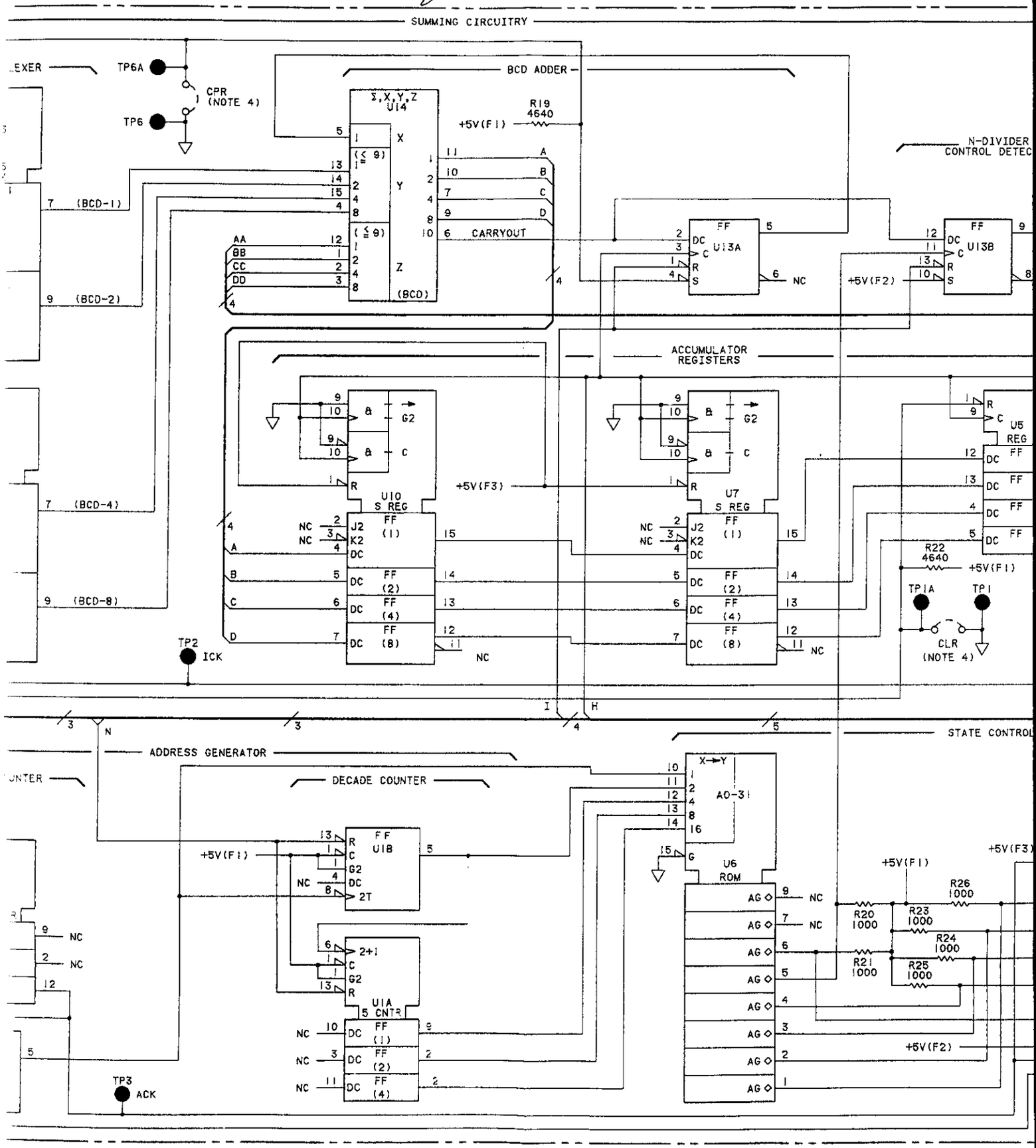
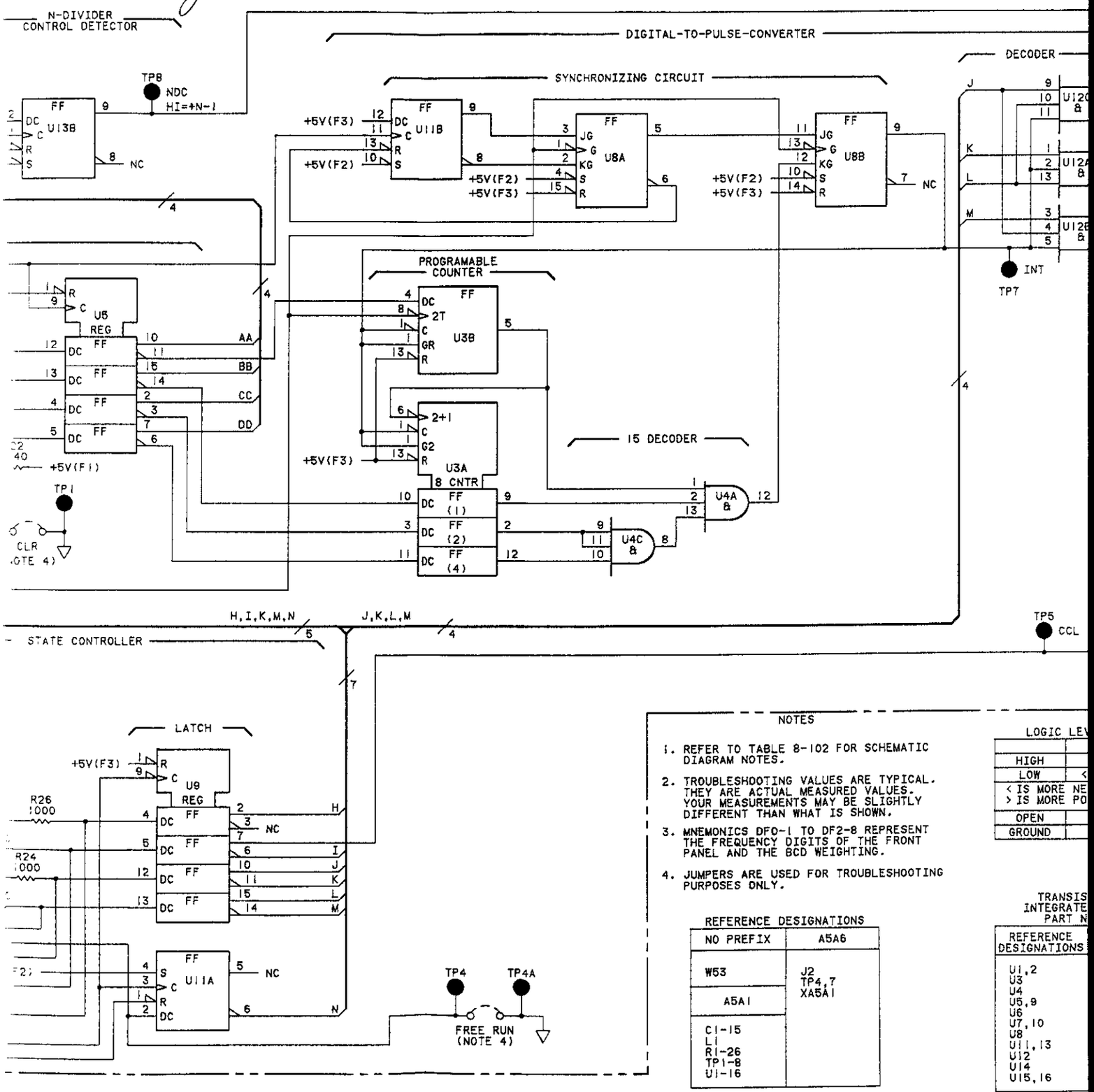


Fig 8-420 Sht 3 of 4



NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. MNEMONICS DF0-1 TO DF2-8 REPRESENT THE FREQUENCY DIGITS OF THE FRONT PANEL AND THE BCD WEIGHTING.
4. JUMPERS ARE USED FOR TROUBLESHOOTING PURPOSES ONLY.

REFERENCE DESIGNATIONS

NO PREFIX	A5A6
W53	J2 TP4,7 XA5A1
A5A1	
C1-15 L1 R1-26 TP1-8 U1-16	

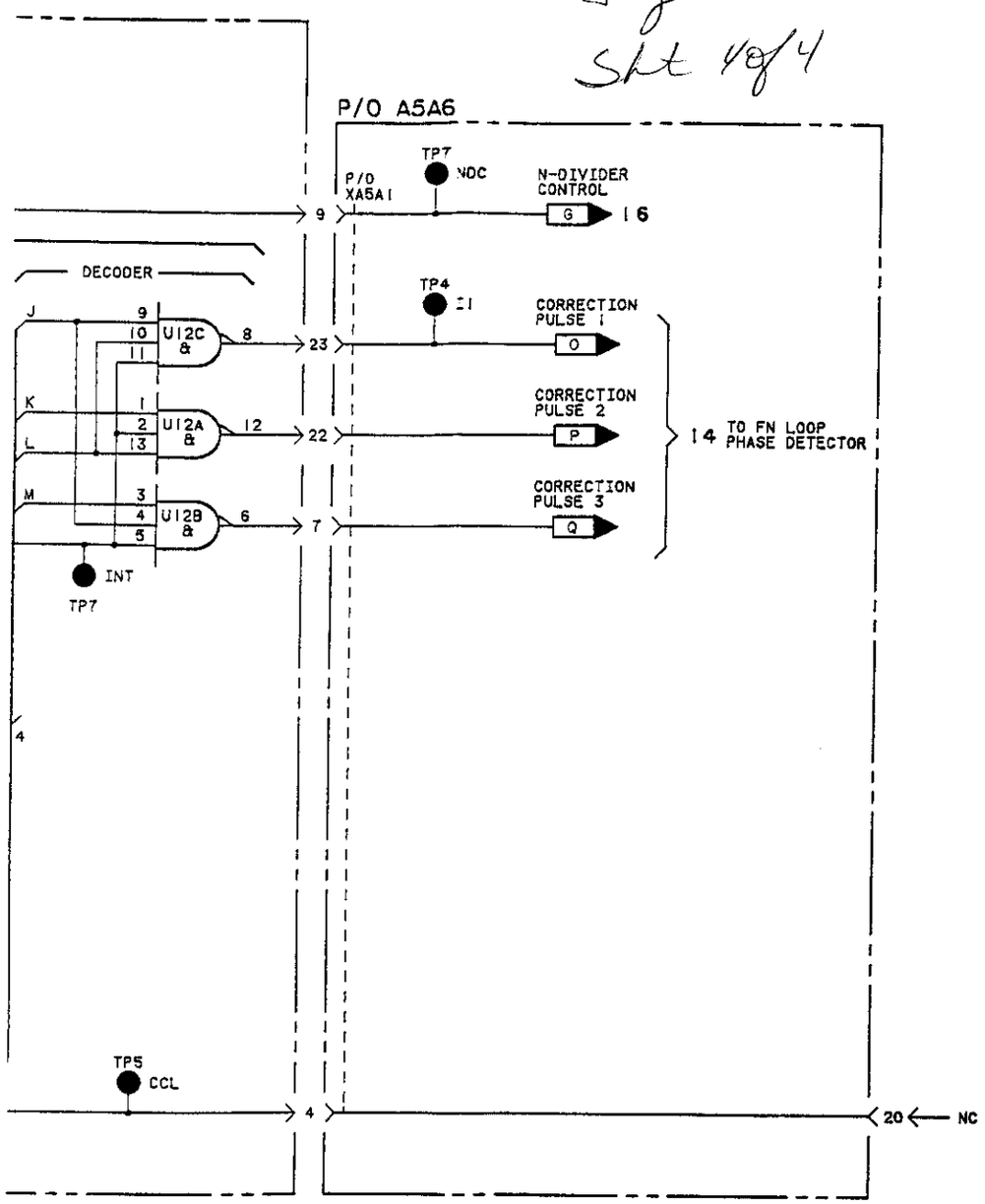
LOGIC LEV

HIGH	
LOW	<
< IS MORE NE > IS MORE PO	
OPEN	
GROUND	

TRANSIS INTEGRATE PART N

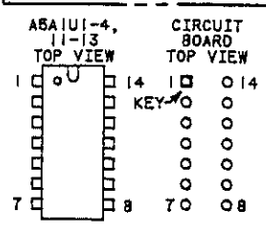
REFERENCE DESIGNATIONS
U1,2 U3 U4 U5,9 U6 U7,10 U8 U11,13 U12 U14 U15,16

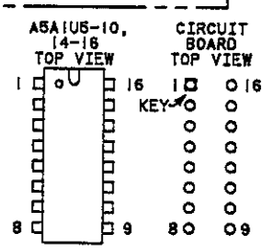
Fig 8-420
Sht 4 of 4



LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW





TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U1,2	1820-1251
U3	1820-1193
U4	1820-0686
U5,9	1820-1195
U6	08662-80002
U7,10	1820-1300
U8	1820-0629
U11,13	1820-1112
U12	1820-0685
U14	1820-1777
U15,16	1820-1244

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1-4,11-13	+5V(F1)- 14 ▽ - 7
U5-10,14-16	+5V(F1)- 16 ▽ - 8

SERVICE SHEET 17

A5A1

Figure 8-420. A5A1 Fractional-N Loop Accumulator Schematic

SERVICE SHEET 18
P/O A3A3 N LOOP DIVIDER/PHASE DETECTOR

REFERENCE BLOCK DIAGRAM 5
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Tabel 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

General

This portion of the N Loop Divider/Phase Detector Assembly contains the N loop programmable divider circuitry. The output (which goes to service sheet 19) is the 10 MHz phase detector variable (VCO frequency divided by N). The inputs consist of the N loop divider drive from the N Loop VCO Assembly (service sheet 20) and the frequency select controls from the Digital Control Unit.

The circuitry on this service sheet takes the 122 MHz to 221 MHz N loop divider drive from the VCO (service sheet 20) and divides it down to 10 MHz by means of the programmable N loop divider. In order to produce the 10 MHz output, the divider circuitry must be capable of dividing the 122 MHz to 221 MHz input by 12.1 to 22.1 in one-tenth of a unit steps.

In order to fractionally divide between 12 and 23, fractional-N circuitry is utilized. The fractional-N divider employs a unique method for generating fractional division. Control circuitry causes the input frequency to be divided by one number for a measured number of cycles and then by another number for a second period of cycles. These two count cycles, when averaged over a period of time, result in a fractional divide count.

Divider Circuitry

The divide by 12 to 23 circuitry is composed of U1-U8 and U12. U1, U2, and U3 make up a divide by 3, divide by 4 circuit. The control circuitry looks at the output of this section and switches back and forth between the two divide modes in order to produce divide values between 12 and 23. For example, suppose a divide value of 17 is desired. The circuit divides by four, two times, and then by three, three times. Thus, for every 17 input pulses, one pulse is produced at the output of U12A.

Control Circuitry (For Fractional-N)

U13, U16, U18, U19, and U20 are the fractional-N control circuits. U13-U19 vary the control signal (TP10) to U20 so that fractional division can be accomplished. U13 adds two to the input. U18 and U19 form the accumulator circuit (U18 is a latch; U19 is an adder). The adder's outputs are at pins 6, 7, 9, 10, and 11. Each time there

is an output from the divider (pin 8 of U21), the count sum is added to the least significant digit programmed. Whenever a carry occurs, the divider is triggered to divide by a number that is one greater. In other words, the control circuitry tells the divide by 12 to 23 section when to shift up by one divide number to achieve fractional division.

For example, to obtain a divide by 12.1 value, the divide by 12 to 23 circuit must divide by 12 for 9 divider output cycles and then by 13 for 1 divider output cycle. The U16A output at pin 5 goes to pin 13 of U20. This is the N/N+1 line. It tells the divider whether it should divide by N or N+1. When the line is HI, the circuit is dividing by N+1, when it is LO, the circuit is dividing by N. (See Fractional-N Loops Section for a more detailed description of howFractional-N works.)

Shift Register and Decoder Circuitry

The shift register and decoder circuitry in the divider section is composed of U6, U7, and U8. U6 generates the appropriate output to control the divide by 3, divide by 4 circuitry. When TP4 is HI, the 3/4 circuit divides by 4. The 12/23 divide number is changed through pin 12 of U7 and pin 6 and 9 of U8 by data from the control section decoder formed by U12. This decoder decodes information from pin 2 and 14 of U20. Signals from gate U4D and pins 2, 3, 14, and 15 of U11 control U7 and U8, the outputs of which are decoded by U6.

ECL to TTL Translator and Squaring Gates

Q3 and Q4 are buffers which convert the ECL output of U12A to TTL levls. The actual output of the divider passes through gates U4A, U4B, and U4C, which square up the output and change the 15% to 20% duty-cycle of the divider output signal to 50%.

TROUBLESHOOTING

When a Low Frequency N Loop problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

Procedure

1. Mount the A3A3 assembly on an extender board from the service kit. Use an extender cable in place of the short cable running to this assembly. Look at TP15 with an oscilloscope. The signal should be a 10.0 MHz TTL signal (high 80 ns, low 20 ns). Check that the signal at U4C pin 14 is a 10.0 MHz ECL signal.

   If the pulses are there and assume valid logic levels (even though the frequency may be wrong), continue with step 2, below. If there are no pulses (either point stuck high or low, or

doesn't assume valid logic levels), trace the signal back to find where the signal goes bad.

2. Set the front panel frequency to 323.3450 MHz. Connect a cable from A5A5J2 (disconnect the cable that is normally connected there) to A3A3J1. This connects the stable output of the fractional N loop to the input of the divider. Measure the frequency of the signal at TP15. The frequency should be 10.0 MHz (±1 count). If the frequency is correct, the divider is functioning normally so continue with step 6, below. Otherwise, there is a problem with the divider so continue troubleshooting with step 3.

3. Set the front panel frequency to 327.80 MHz. The frequency at TP15 should be 10.0 MHz. This frequency setting programs a divide number of 20.0 and input frequency (from fractional N loop) of 200.0 MHz. If the frequency at TP15 is correct, the problem is with the accumulator circuitry (U13, U19, U18 or U16). Otherwise, the problem is in the basic divider circuitry so continue troubleshooting with step 4.

4. Remove jumper W1 (to the left of U2). The frequency at TP5 should be 66.66667 MHz. The 34 counter is held in the divide-by-3 mode with the jumper removed.

   Connect a jumper from +5V to the top pad where the jumper was connected. The frequency at TP5 should be 50.0 MHz. The 3/4 counter is held in the divide-by-4 mode with +5V applied.

   If the counter operates normally, replace the jumper and continue troubleshooting with step 5. Otherwise, there is a problem with U1, U2, U3 or associated components.

5. Set the front panel frequency to 320.80 MHz. Set the frequency increment to 1 MHz. Press the INCREMENT (up) and INCREMENT (down) keys and check the frequency digit decoder outputs shown in the table below. If any outputs are wrong, troubleshoot to find the cause. Otherwise, the problem is in one of the shift registers (U7 or U8) or the U6 decoder.

FREQUENCY DIGIT DECODER OUTPUTS
(Front-panel frequency setting = 320.80 MHz)

1 MHz DIGIT	U11-15	U11-2	U11-3	U4-15	U12-13	U12-9	U12-3
0	H	L	H	L	L	H	L
1	L	H	L	L	L	H	L
2	H	H	L	H	L	H	L
3	L	L	H	L	H	H	L
4	H	L	H	L	H	H	L
5	L	H	L	L	H	H	L
6	H	H	L	H	H	H	L
7	L	L	H	L	H	H	H
8	H	L	H	L	H	H	H
9	L	H	L	L	H	H	H

6. Set the front panel frequency to 326.810 MHz. This setting programs the fractional-N loop output to 190.0 MHz and the A3A3 divide number to 19.0, so the output of the divider should be 10.0 MHz. Set the front panel frequency increment to 0.1 Hz and press the INCREMENT (up) key. The ERROR LED on top of the A3A3 assembly should blink at a 100 Hz rate and the waveform at TP1 should be a 100 Hz square wave (amplitude ±0.7 Vdc). Each time the frequency is incremented, the frequency of the blinking LED and the waveform at TP1 will increase by 100 Hz. Press the Increment (down) key until the frequency display is below 326.810 MHz. The LED and TP1 behave exactly the same as described, above. When the frequency is exactly 326.810 MHz, the signal at TP1 should be a dc value somewhere in the range of ±0.7 Vdc (most likely value is +0.7 Vdc or -0.7 Vdc). The LED may be either lit or off but should not be blinking. If this circuitry is functioning normally, continue with step 7. Otherwise, there is a problem with the phase detector circuitry so continue troubleshooting this circuitry to find the cause.

NOTE

The waveforms shown on the schematic for TP12 and TP13 are taken with the Phase Lock Loop in an out-of-lock condition and are not representative of the waveforms for step 7 of this procedure.

7. Set the front panel frequency to 326.810 MHz an frequency increment to 10 Hz. Look at TP13 on an oscilloscope (DC coupled, 0.5 V/div vertical, 1 ms/div horizontal). There should be no waveform present and the level should be near ground (±1/2 division with the settings given).

   Press the INCREMENT (up) key. Negative going pulses should appear on TP13 (amplitude of approximately 1.0 V). Pressing the

INCREMENT (up) key again should cause the frequency of the pulses to increase.

Set the front panel frequency to 326.810 MHz and look at TP12 with an oscilloscope. There should be no waveform present and the level should be near ground (±1/2 division). Press the INCREMENT (down) key. Positive pulses should appear on TP12 (amplitude of approximately 2.0 V). Look closely since they are faint at the scope settings given, above. Pressing the INCREMENT (down) key again should cause the frequency of the pulses to increase.

If either or both of these waveforms is not correct, there is a problem in the frequency detector circuitry. Troubleshoot this part of the circuitry to find the cause of the problem.

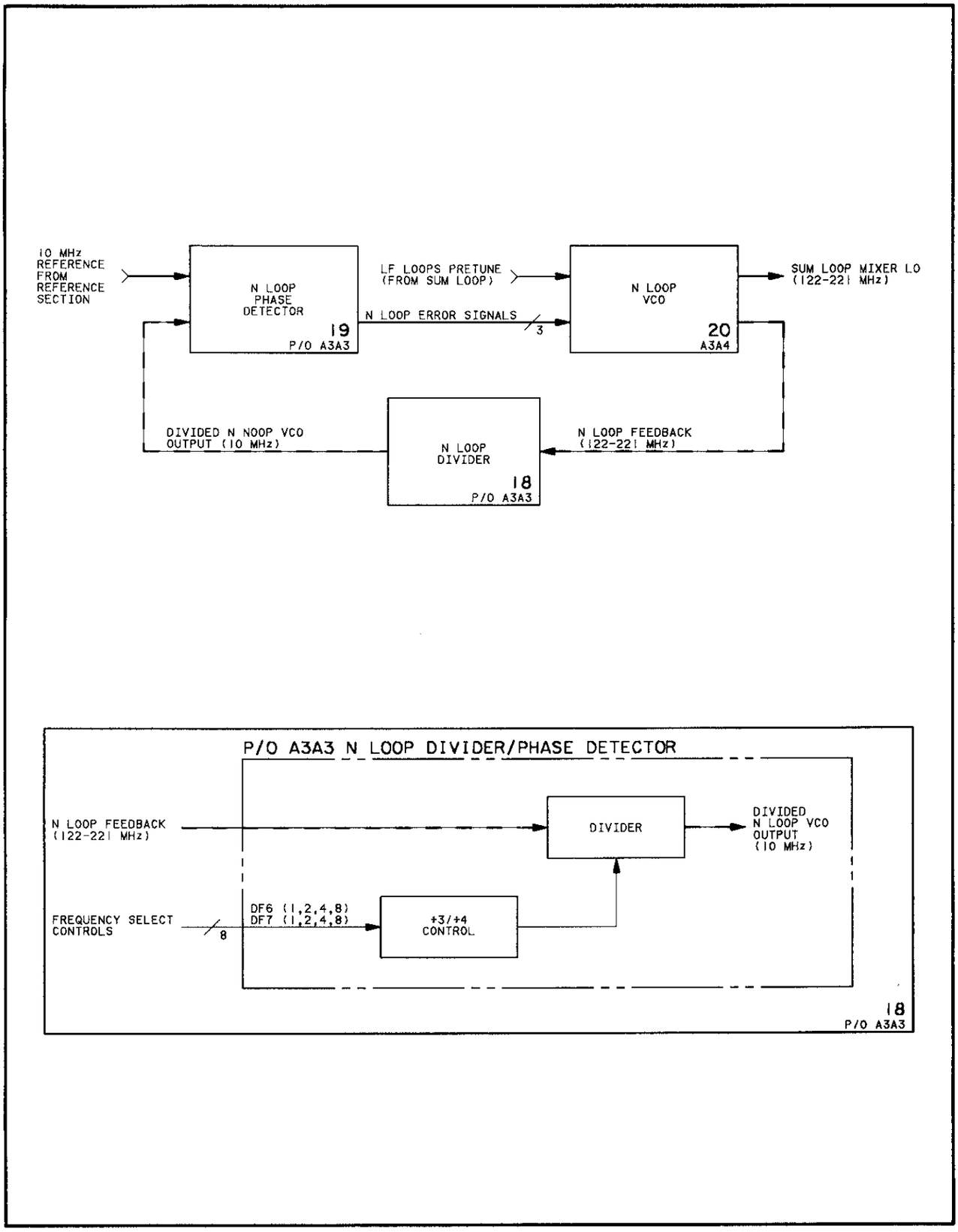


Figure 8-421. P/O A3A3 N Loop Divider/Phase Detector Block Diagrams

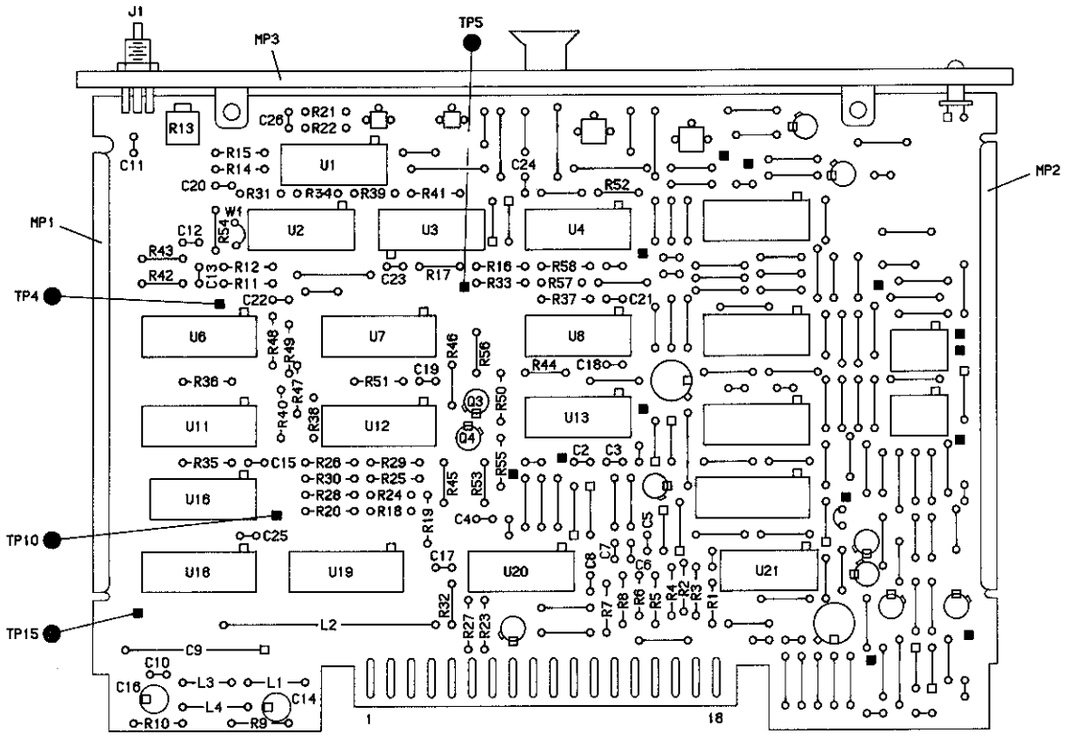


Figure 8-422. P/O A3A3 N Loop Divider/Phase Detector Component Locator

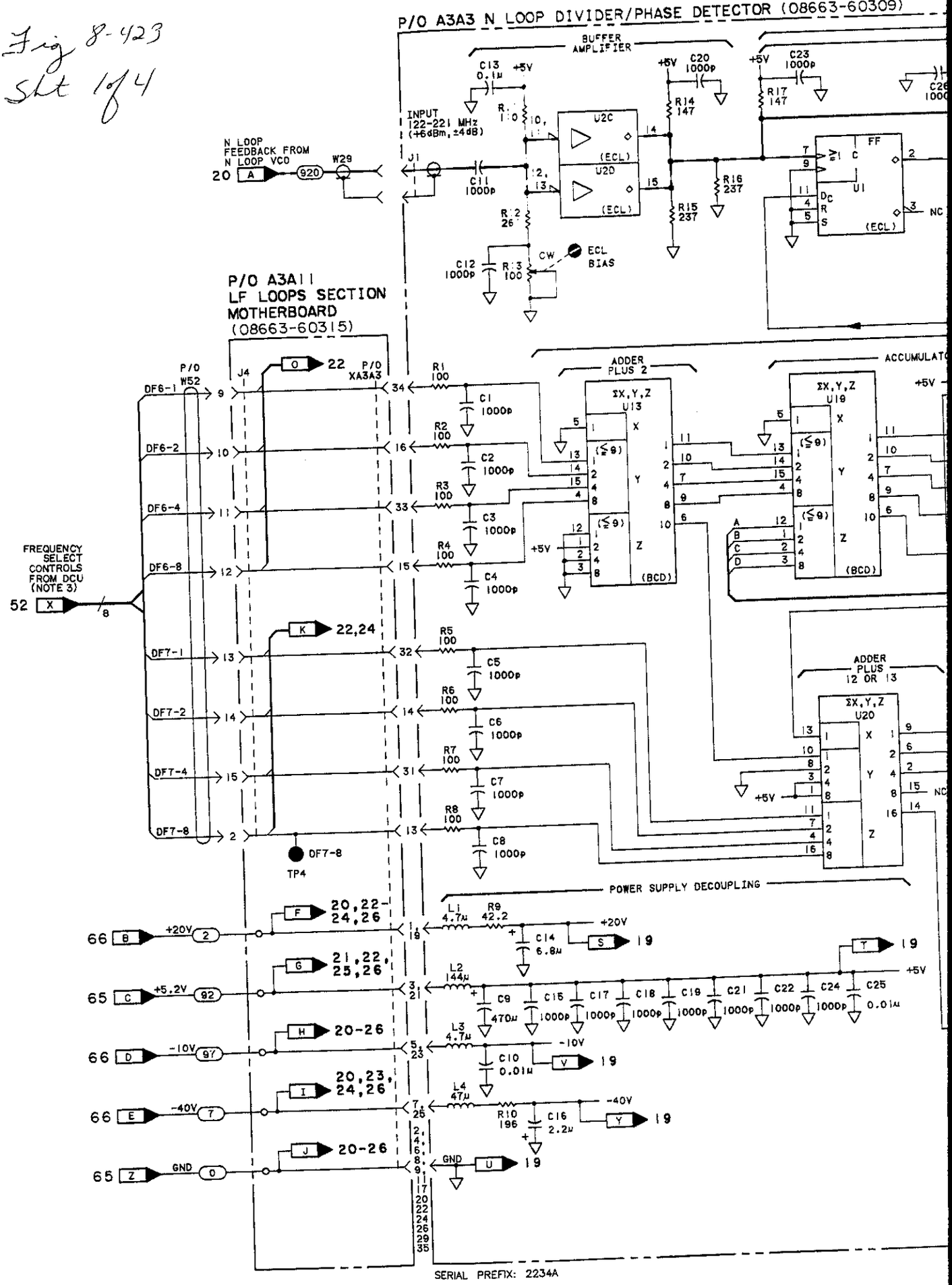
CHANGES

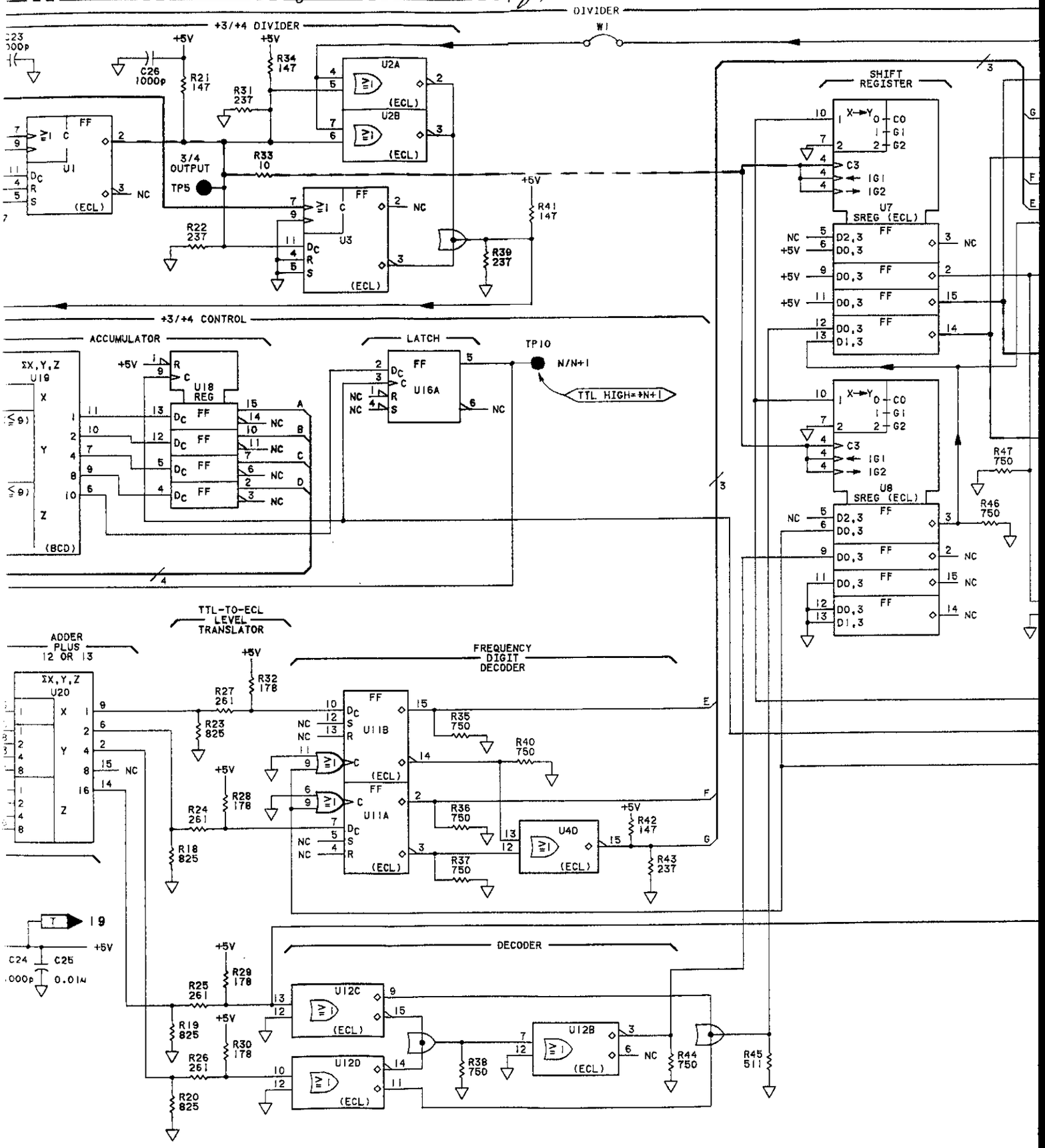
All serial prefixes

On the A3A3 schematic:

- A3A3R1-R8 – Change the value of R1-R8 to 178 ohms.

Fig 8-423
Sht 1 of 4




DIVIDER
+3/+4 DIVIDER
W1
+5V
C26 1000p
R21 147
R34 147
R31 237
U2A
U2B
(ECL)
U1
FF
3/4 OUTPUT
TP5
R33 10
NC
U3
R22 237
R41 147
R39 237
SHIFT REGISTER
U7 SREG (ECL)
U8 SREG (ECL)
X→Y
CO
G1
G2
C3
1G1
1G2
D2,3
D0,3
D1,3
R47 750
R46 750
+3/+4 CONTROL
ACCUMULATOR
ΣX,Y,Z
U19
(BCD)
U18 REG
LATCH
U16A
TP10
N/N+1
TTL HIGH=+N+1
TTL-TO-ECL LEVEL TRANSLATOR
ADDER PLUS 12 OR 13
U20
FREQUENCY DIGIT DECODER
U11B
U11A
U4D
R27 261
R32 178
R23 825
R28 178
R24 261
R18 825
R35 750
R40 750
R36 750
R37 750
R42 147
R43 237
DECODER
C24 .000p
C25 0.01u
R25 261
R29 178
R19 825
R30 178
R26 261
R20 825
U12C
U12D
U12B
R38 750
R44 750
R45 511

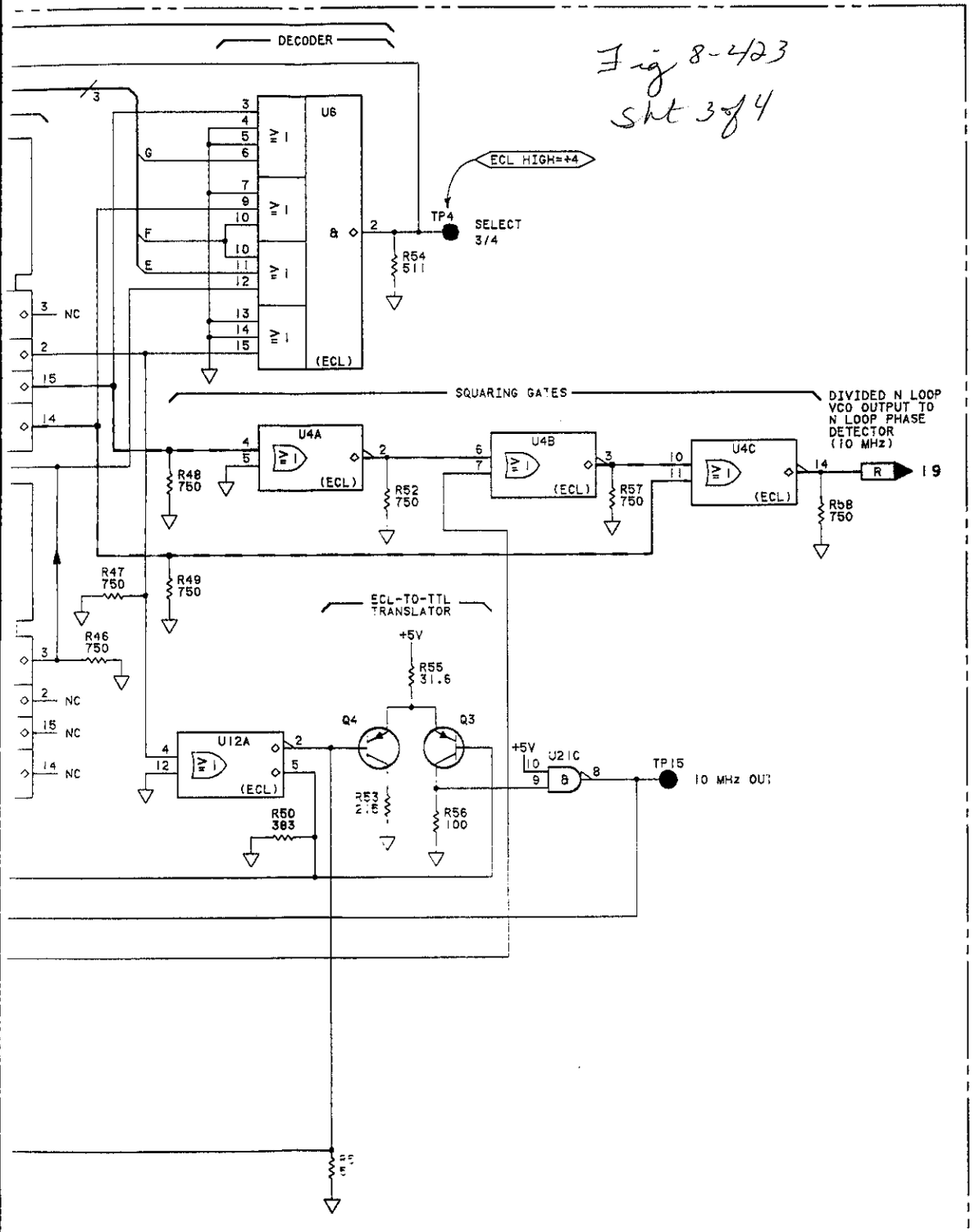


Fig 8-423 Sht 3 of 4

NOTES

1. SEE TABLE 8-102 FOR SCHEM DIAGRAM NOTES.
2. TROUBLE SHOOTING VALUES A THEY ARE ACTUAL MEASURED YOUR MEASUREMENTS MAY BE SI DIFFERENT THAN WHAT IS SH
3. MNEMONICS DF6-1 TO DF7-8 THE FREQUENCY DIGITS ON T PANEL AND THE BCD WEIGHTI
4. LOGIC LEVELS FOR ECL DEVI INSTRUMENT ARE NON-STANDA THE SUPPLY VOLTAGE USED. IS >+4.0V : A LOW VOLTAGE

REFERENCE DESIGNATIONS

NO PREFIX	A3A11
W29,52	J4 TP4 XA3A3
A3A3	
C1-26 J1 L1-4 Q3,4 R1-58 TP4,5,10,15 U1-4,6-8,11-13,16,18-21 W1	

LOGIC LEVELS

	TTL	ECL (NOTE 4)
HIGH	>+2V	>+4.0V
LOW	<+0.8V	<+3.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	LOW
GROUND	LOW	HIGH

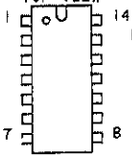
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q3,4	1853-0034
U1,3	1820-0794
U2,4	1820-0796
U6	1820-0813
U7,8	1820-0825
U11	1820-1817
U12	1820-0801
U13,19	1820-1777
U16	1820-0693
U18	1820-1191
U20	1820-0305
U21	1820-0681

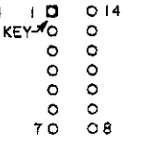
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1-4,6-8, 11,12	+5V -1,16 ▽ -8
U13,18,19	+5V -16 ▽ -8
U16,21	+5V -14 ▽ -7
U20	+5V -5 ▽ -12

A3A3 U16,21 TOP VIEW



CIRCUIT BOARD TOP VIEW



NOTES

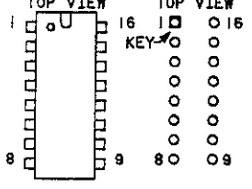
1. SEE TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLE SHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. MNEMONICS DF6-1 TO DF7-8 REPRESENT THE FREQUENCY DIGITS ON THE FRONT PANEL AND THE BCD WEIGHTING.
4. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NON-STANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS ≥+4.0V ; A LOW VOLTAGE IS ≤+3.5V.

Fig 8-423
Sht 4 of 4

REFERENCE DESIGNATIONS

NO PREFIX	A3A11
W29,52	J4 TP4 XA3A3
A3A3	
C1-26 J1 L1-4 Q3,4 R1-58 TP4,5,10,15 U1-4,6-8,11-13,16,18-21 W1	

A3A3
U1-4,6-8,
11-13,18-20
TOP VIEW



CIRCUIT BOARD
TOP VIEW

LOGIC LEVELS

	TTL	ECL (NOTE 4)
HIGH	>+2V	>+4.0V
LOW	<+0.8V	<+3.5V
< IS MORE NEG.THAN > IS MORE POS.THAN		
OPEN	HIGH	LOW
GROUND	LOW	HIGH

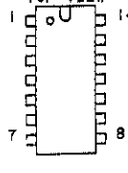
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q3,4	1853-0034
U1,3	1820-0794
U2,4	1820-0796
U6	1820-0813
U7,8	1820-0825
U11	1820-1817
U12	1820-0801
U13,19	1820-1777
U16	1820-0693
U18	1820-1191
U20	1820-0305
U21	1820-0681

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1-4,6-8, 11,12	+5V -1,16 ▽ -8
U13,18,19	+5V -16 ▽ -8
U16,21	+5V -14 ▽ -7
U20	+5V -5 ▽ -12

A3A3 U16,21
TOP VIEW



CIRCUIT BOARD
TOP VIEW

SERVICE SHEET 18

P/O A3A3

Figure 8-423. P/O A3A3 N Loop Divider/Phase Detector Schematic

SERVICE SHEET 19
P/O A3A3 N LOOP DIVIDER/PHASE DETECTOR

REFERENCE BLOCK DIAGRAM 5
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-3. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

General

This service sheet contains the circuitry for the phase detector portion of the N loop. Inputs include the 10 MHz N loop phase detector reference signal from the reference section (service sheet 1) and the 10 MHz phase detector variable from the N Loop Divider (service sheet 18). The phase detector reference signal splits and goes to both the phase and frequency detector circuits, as does the phase detector variable signal. The outputs from this section are phase and frequency error signals which are sent to the N Loop VCO (service sheet 20).

Frequency Detector Circuitry

The frequency detector circuitry determines if the frequency at the output of the N loop divider is above or below the 10 MHz reference signal. If the N loop frequency is more than several MHz from the reference, the loop won't lock by itself because the signal is out of the phase detector's range. The frequency detector section determines which direction to tune the frequency so that the signal is within the phase detector's range. Q1 and Q2 form the 45-degree phase shifter circuits. U5, U9 and U14 are used as dual exclusive-or gates.

Of the two 45-degree phase shifter circuits, one shifts the detector reference signal in the +45-degree direction and the other shifts in the -45 -degree direction. This puts the resulting signals to the dual exclusive-or gates 90 degrees out of phase with each other. The exclusive-or gates function similarly to double-balanced mixers. The signals at their outputs are filtered by the 2 MHz low-pass filters. These filtered outputs are the difference frequencies between pin 10 on U5D and the reference divider inputs to Q1 and Q2. The signals sent to the comparators are triangle waves and are measurable at TP7 and TP9, where the phase difference is still 90 degrees. These triangle waves are converted to square waves by comparators U10 and U15. The outputs from these comparators enter U16, a control flip-flop.

If TP11 goes HI when TP8 is LO, then a LO is transferred to pin 9 of U16B to trigger monostable U17A. U17A produces a 4.5 microsecond pulse that turns OFF Q6 and causes CR11 and CR12 to turn ON. Q6 turns OFF when CR9 turns ON, which occurs when pin 13 goes HI and pin 4 goes LO. Current flows from the summing junction of the N Loop

VCO, causing the frequency to go up. At the same time, pin 5 of U17B is LO. This keeps CR10 OFF so that no current flows into the junction of R119 and R120. When the loop is locked, U17A and U17B are not triggered and there is no current flowing through R118, R119, or R121. When pin 5 of U17B goes HI, current is sent to the junction through CR10 and the frequency decreases.

Phase Detector Circuitry

The input to the phase detector section is composed of limiters Q5 and Q10. These produce square waves at TP14 and TP16. From here the signals enter the phase detector formed by Q11 and Q12. This phase detector acts like an exclusive-or gate. When TP14 and TP16 have different voltages (either Q5 or Q10 is HI) one of the two phase detector transistors turns ON and sums current into R85 and R86, causing the emitter of Q9 to go HI. The output voltage from Q9 is LO when both inputs are the same.

Q9 is used in a low impedance emitter-follower configuration and acts to drive the 1 MHz and 6 MHz notch filters. The six notch filters (which follow Q9) filter the spurs generated in the N loop fractional-N circuitry. These spurs occur at sub-multiples of the reference frequency. CR5 and CR6 limit the phase range over which the phase detector can tune the oscillator. The phase error signal at pin 10 goes to the summing junction on the N Loop VCO Assembly (service sheet 48).

Out-of-Lock Circuitry

When the output of the phase detector is HI (indicating an out-of-lock condition), the TTL level translator formed by Q8 and U21 turns ON Q7, causing the out-of-lock lamp to light.

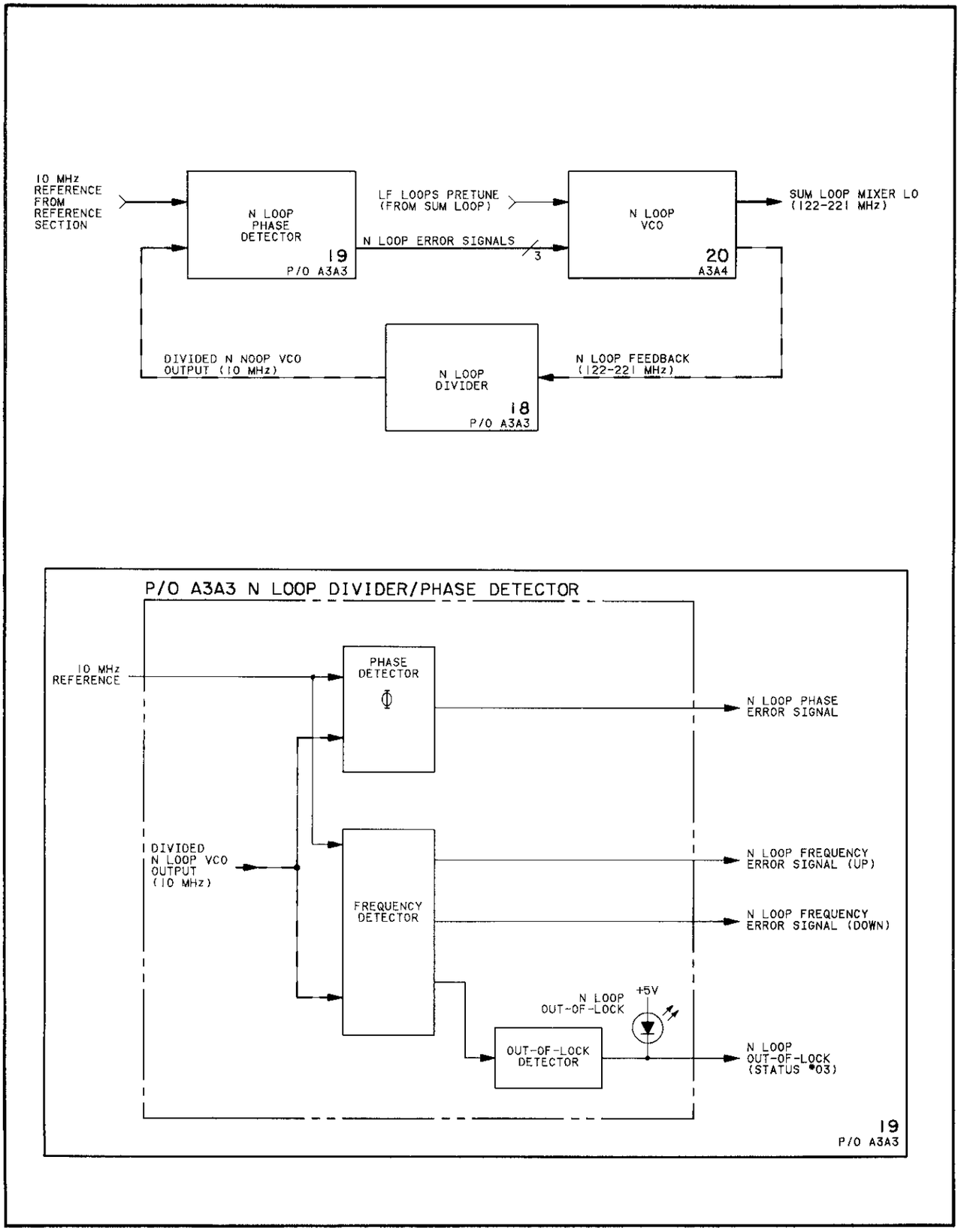


Figure 8-424. P/O A3A3 N Loop Divider/Phase Detector Block Diagrams

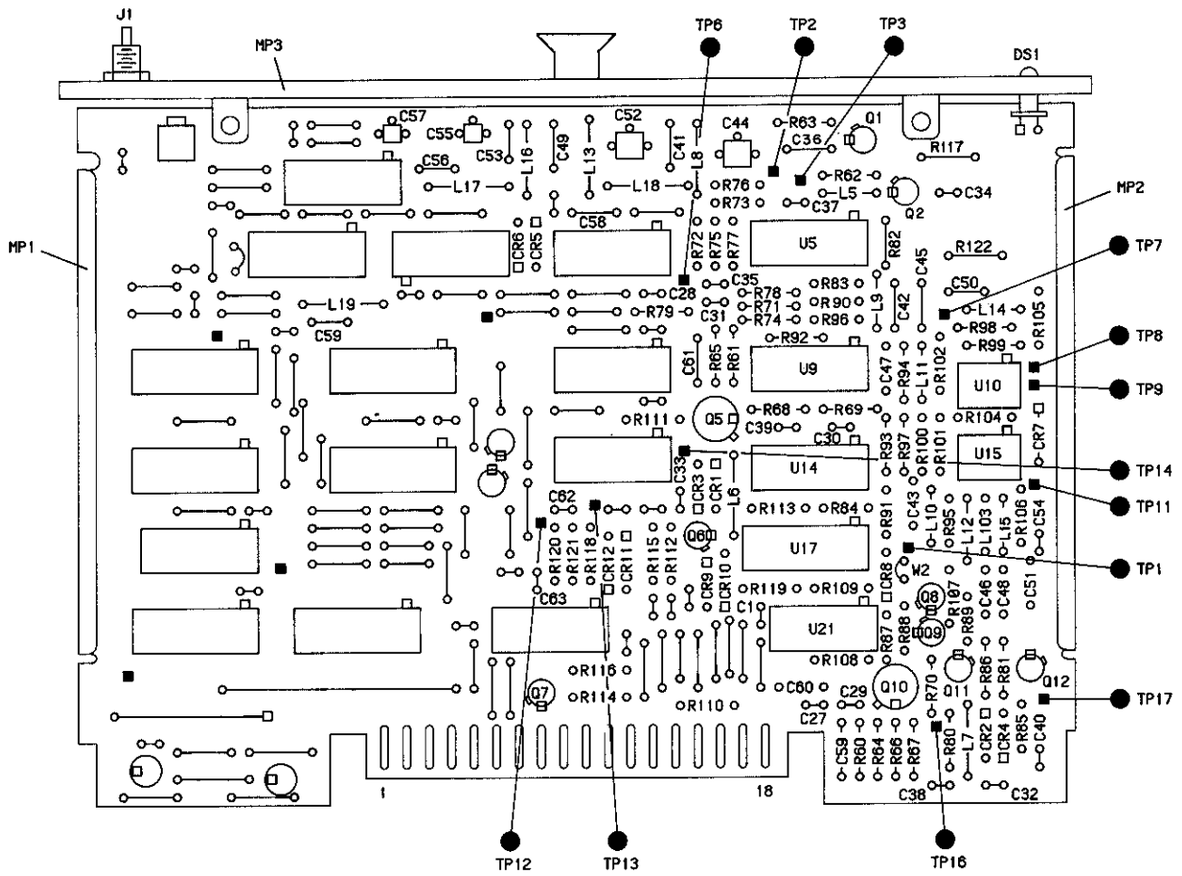


Figure 8-425. P/O A3A3 N Loop Divider/Phase Detector Component Locator

CHANGES

2245A and Above

On the A3A3 component locator:

- A3A3R123 - Add resistor, R123, directly above edge connector pad 12.

On the A3A3 schematic:

- A3A3R123 - At the right edge of the schematic, in the circuitry labeled "N LOOP OUT-OF-LOCK INDICATOR", add resistor R123 (237 ohms) as a series resistor to the right of DS1 in the path leading to pin 12.

Fig 8-426
Sht 1 of 4

P/O A3
LF LOOPS
SECTION
MOTHERBOARD
(08663-60305)

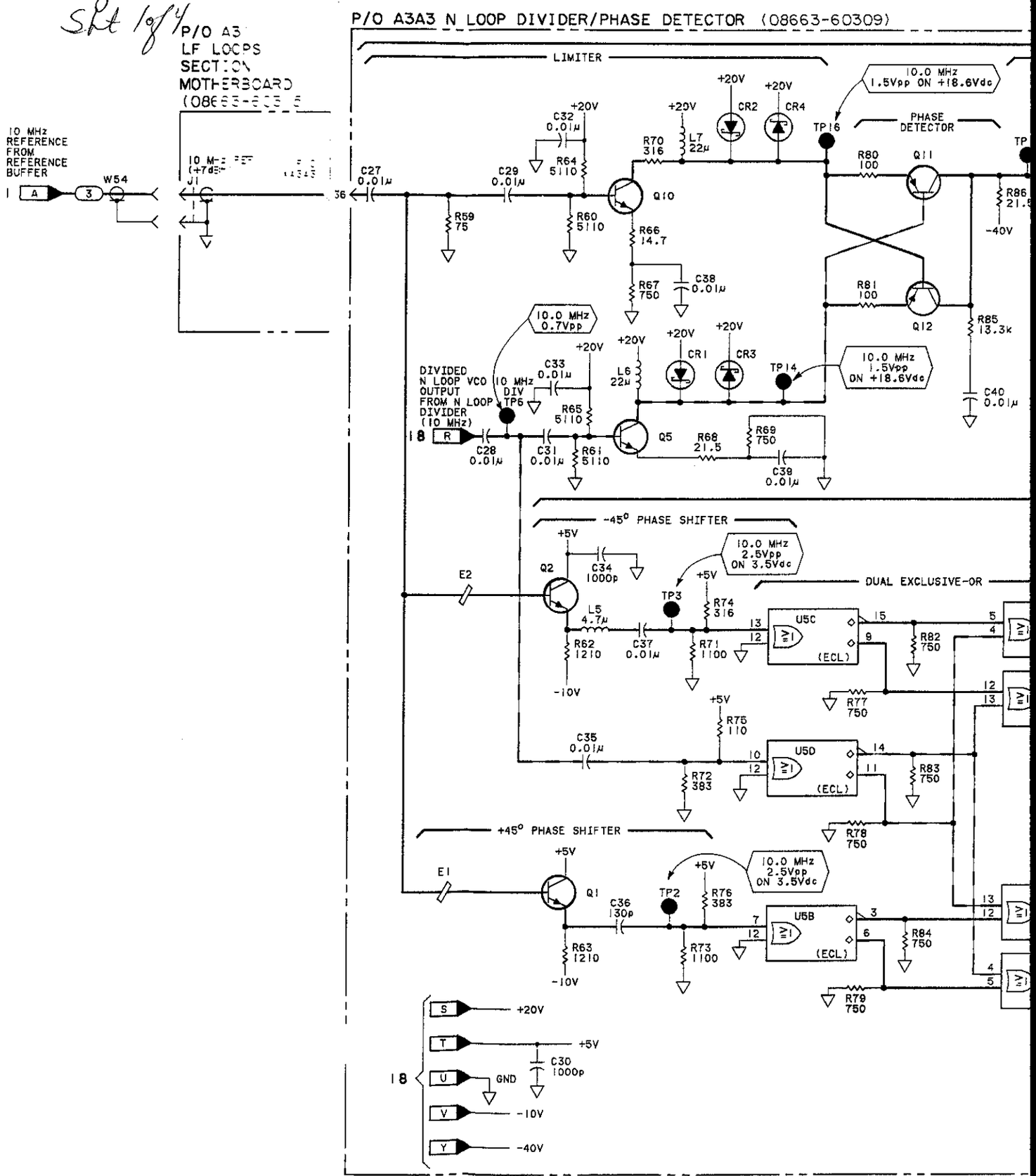


Fig 8-426 Sht 2 of 4

3-60309)

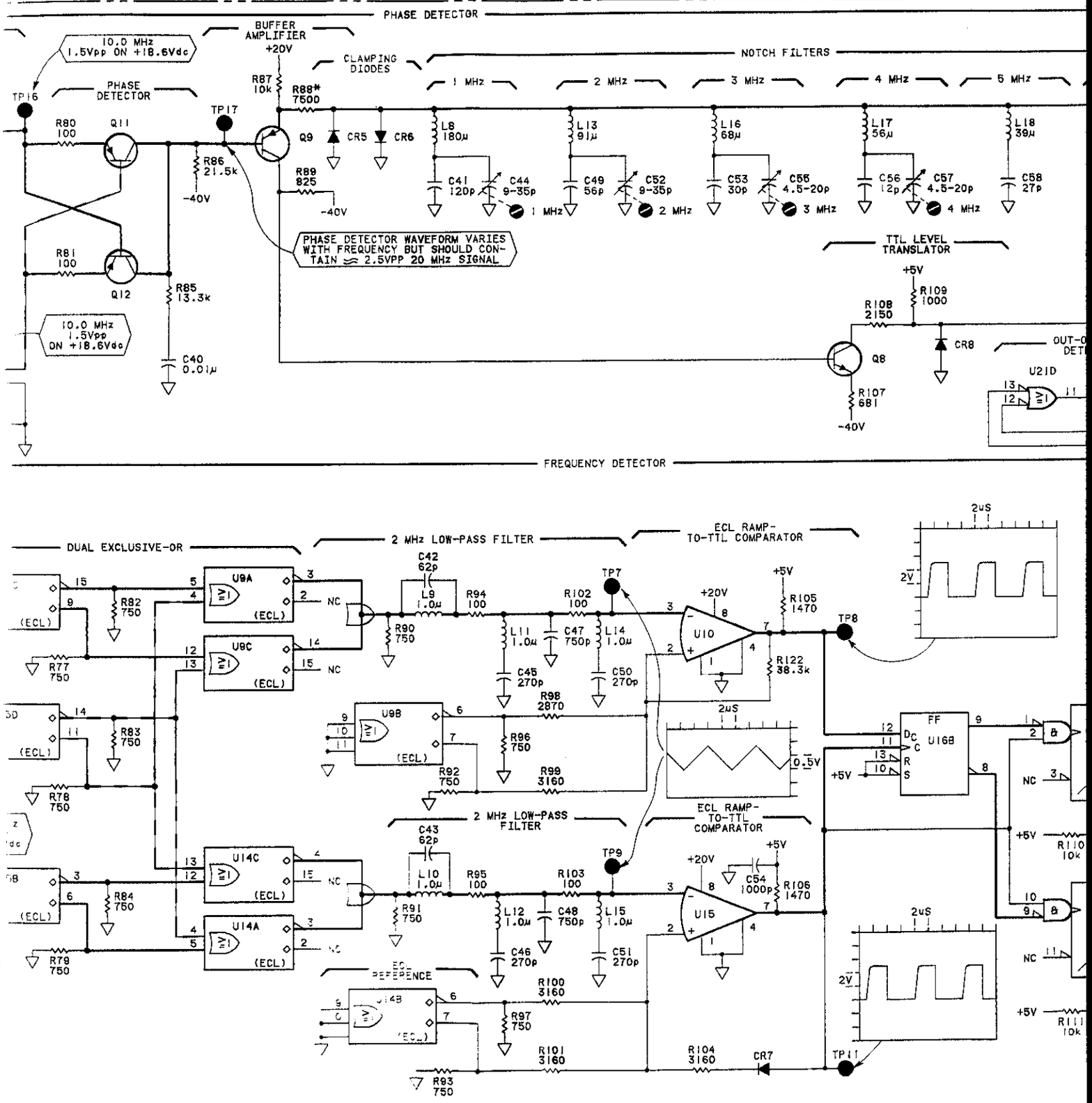


Fig 8-426 Sht 3 of 4

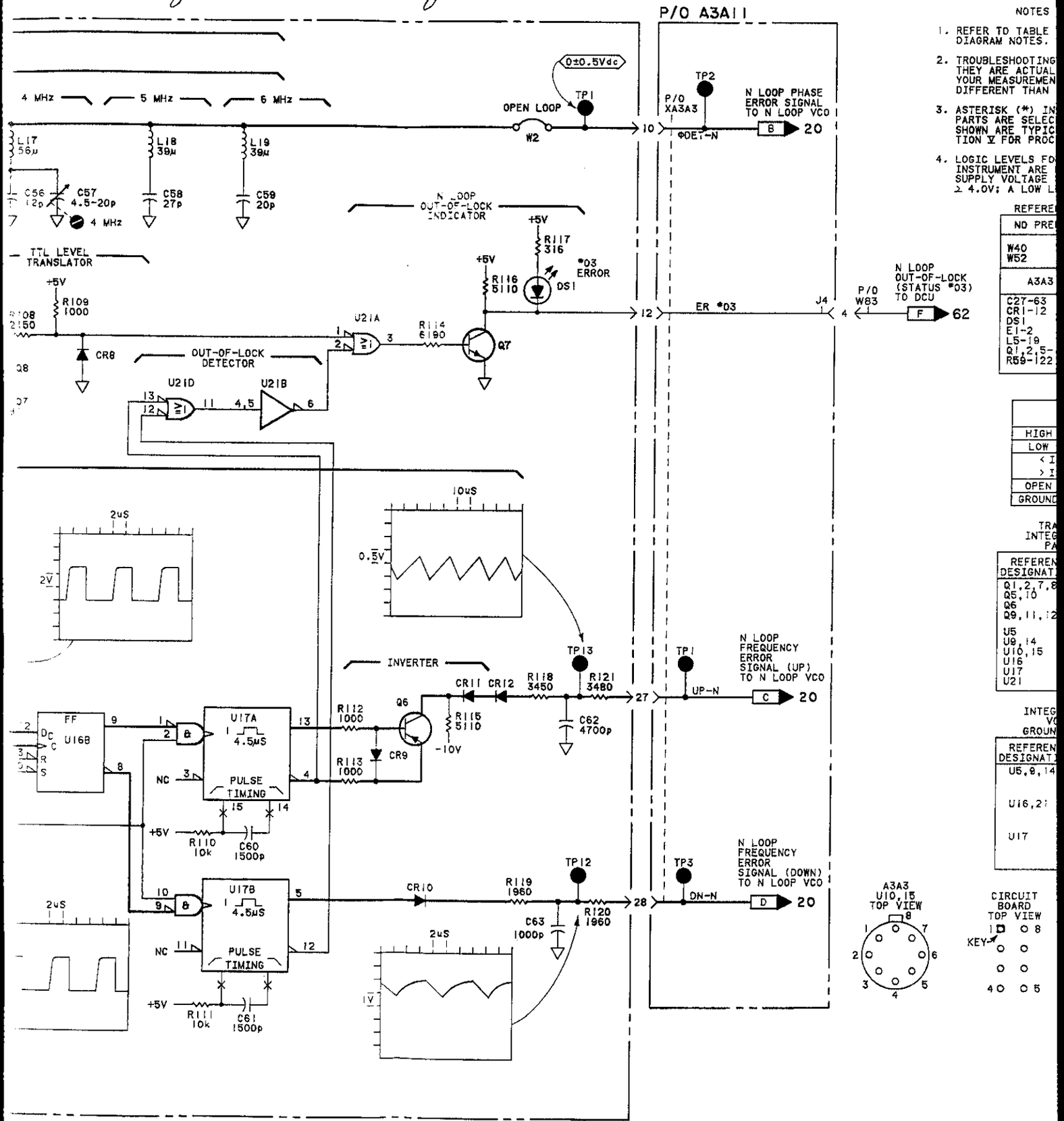


Fig 8-426
Sht 4 of 4

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. ASTERISK (*) INDICATES THAT THESE PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL ONLY. REFER TO SECTION V FOR PROCEDURE.
4. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NONSTANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS ≥ 4.0V; A LOW LEVEL IS ≤ +3.5V.

REFERENCE DESIGNATIONS

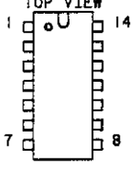
NO PREFIX	A3A3 CONT
W40 W52	TP1-3,6-9, 11-14,16,17 U5,9,10,14, 15-17,21 W2
A3A3	
C27-63 CR1-12 DS1 E1-2 L5-19 Q1,2,5-12 R59-122	A3A11 J1,4 TP1-3 XA3A3

N LOOP
OUT-OF-LOCK
(STATUS *03)
TO DCU
F 62

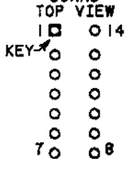
LOGIC LEVELS

	TTL	ECL (NOTE 4)
HIGH	>+2V	>+4.0V
LOW	<+0.8V	<+3.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	LOW
GROUND	LOW	HIGH

A3A3 U16,21 TOP VIEW



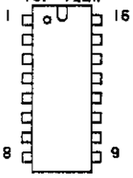
CIRCUIT BOARD TOP VIEW



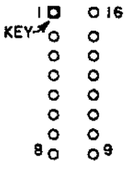
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,2,7,8	1854-0404
Q5,10	1854-0247
Q6	1853-0007
Q9,11,12	1853-0451
U5	1820-0801
U9,14	1820-0803
U10,15	1826-0026
U16	1820-0693
U17	1820-0579
U21	1820-0681

A3A3 U5,9,14,17 TOP VIEW



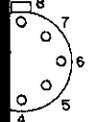
CIRCUIT BOARD TOP VIEW



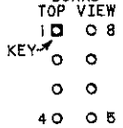
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U5,9,14	+5V - 1,16 ▽ - 8
U16,21	+5V - 14 ▽ - 7
U17	+5V - 16 ▽ - 8

3A3
0,15
VIEW



CIRCUIT BOARD TOP VIEW



SERVICE SHEET 19
A3A3

Figure 8-426. P/O A3A3 N Loop Divider/Phase Detector Schematic

SERVICE SHEET 20
A3A4 N LOOP VCO

REFERENCE BLOCK DIAGRAM 5
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

General

This service sheet contains the voltage controlled oscillator and associated circuitry for the Low Frequency N Loop. There are four frequency control inputs to this board and two outputs. The outputs extend from 122 MHz to 221 MHz. One output is the N loop N-divider drive, the other is the S loop mixer local oscillator input. The frequency control inputs are summed, shaped, amplified, and filtered before being used to control the frequency of the voltage controlled oscillator.

Current Summing Junction

The inputs to this assembly go through a summing junction and are amplified by Q10. Q10 converts the summed currents to a control voltage.

One of the four inputs is a pretune (pin 15) that coarsely tunes the oscillator to within a couple of MHz of the correct frequency for locking. The other three inputs are loop signals. The signal at pin 11 is the phase error signal from the phase detector that is located on the N Loop Divider Board. The other two signals are from the frequency detector circuitry on service sheets 46 and 47. One of them sums current into the summing junction and makes the frequency decrease, the other one removes current from the emitter of Q10 and makes the frequency increase. These inputs are at board pins 10 and 9, respectively. The pretune line has a gain adjustment which allows the range of the VCO to be set. The maximum tune range is approximately 100 MHz with the 7 volt (maximum) pretune voltage.

Shaping Network and Buffer Amplifier

The shaping network (in the collector circuit of Q10) is a diode-resistor network composed of CR2, CR3, R12, R13, R16, and R19. This network shapes the VCO pretune voltage so that a change in voltage causes a linear change in the VCO output frequency.

Following the shaping network is an emitter-follower stage formed by Q6. It drives the filter network that removes the spurious signals from the loop and drives the phase lag network consisting of R29, R31, and C19. The actual varactor voltage (at TP2) goes through R33 to the oscillator tank at CR7 and CR8. This is a negative voltage of

between -2 volts and -18 volts (-2 volts is the limit for the low frequency end and -18 volts is the limit for the high frequency end).

Gain Set Switch

Q9 is a transistor switch that increases the loop gain voltage as determined by the conduction threshold of CR3. When Q9 turns ON, it shunts R25 so that the gain from the emitter of Q6 to TP2 is increased by approximately 6 dB. This causes loop gain to increase and compensate for the decrease in capacitance of the varactors, which occurs close to the high frequency end.

Charge-Discharge Switch

Transistors Q5 and Q8 switch current into C19 through R26 and R31. These transistors are biased so that when the voltage at TP4 is 2 volts greater than the voltage on C19, either Q5 or Q8 turn ON and quickly charge C19. This increases switching speed.

Voltage Controlled (Hartley) Oscillator

The oscillator itself is formed by Q7, which is a common gate FET amplifier. Capacitor C22 is a bypass capacitor for the varactors. L8 is a tapped inductor. The feedback loop feeds through C24 to the source of the FET. R27 and R28 set the dc current in the FET.

Signal Splitter

The output of the VCO is tapped from inductor L8 very close to ground and goes through R34 to transformer T1, which is a power splitter. This splitter supplies half-power to each of the two amplifiers and provides substantial isolation between them.

Output and Loop Buffer Amplifiers

The two buffer amplifiers are identical. The loop buffer amplifier consists of Q3 and Q1 and the output buffer amplifier consists of Q4 and Q2. The two transistors within each amplifier assembly are cascaded. The output of each amplifier is attenuated by a 3 dB pad before being output from the assembly. One of the outputs is sent to the N loop divider to provide feedback to the N loop phase detector; the other is sent to the sum loop mixer (LO input).

Minus 26 Volt Supply

The -26 volt on-board supply is derived from the main -40 volt supply. It is used as a reference voltage (for the frequency breakpoints) by the shaping network.

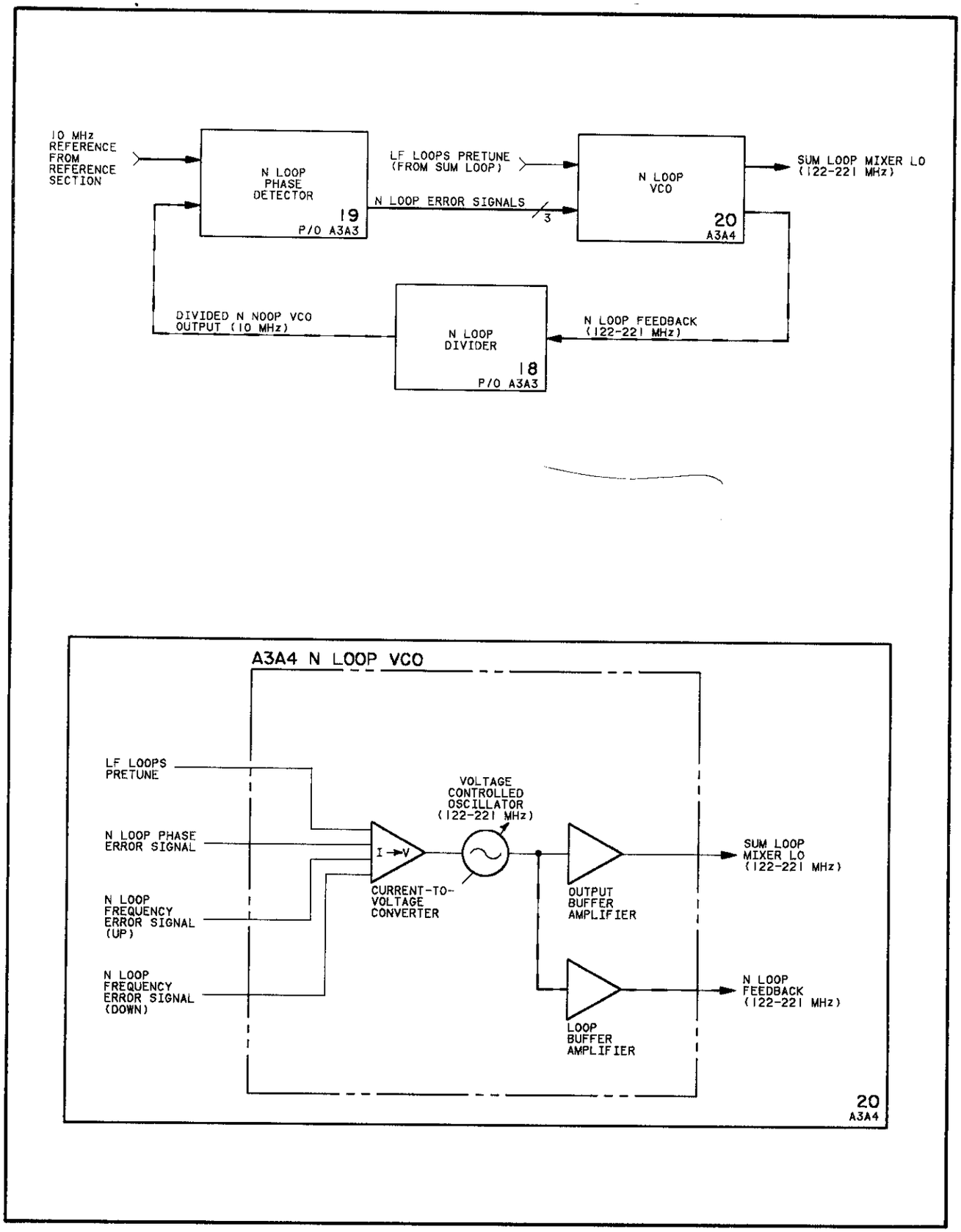


Figure 8-427. A3A4 N Loop Voltage Controlled Oscillator Block Diagrams

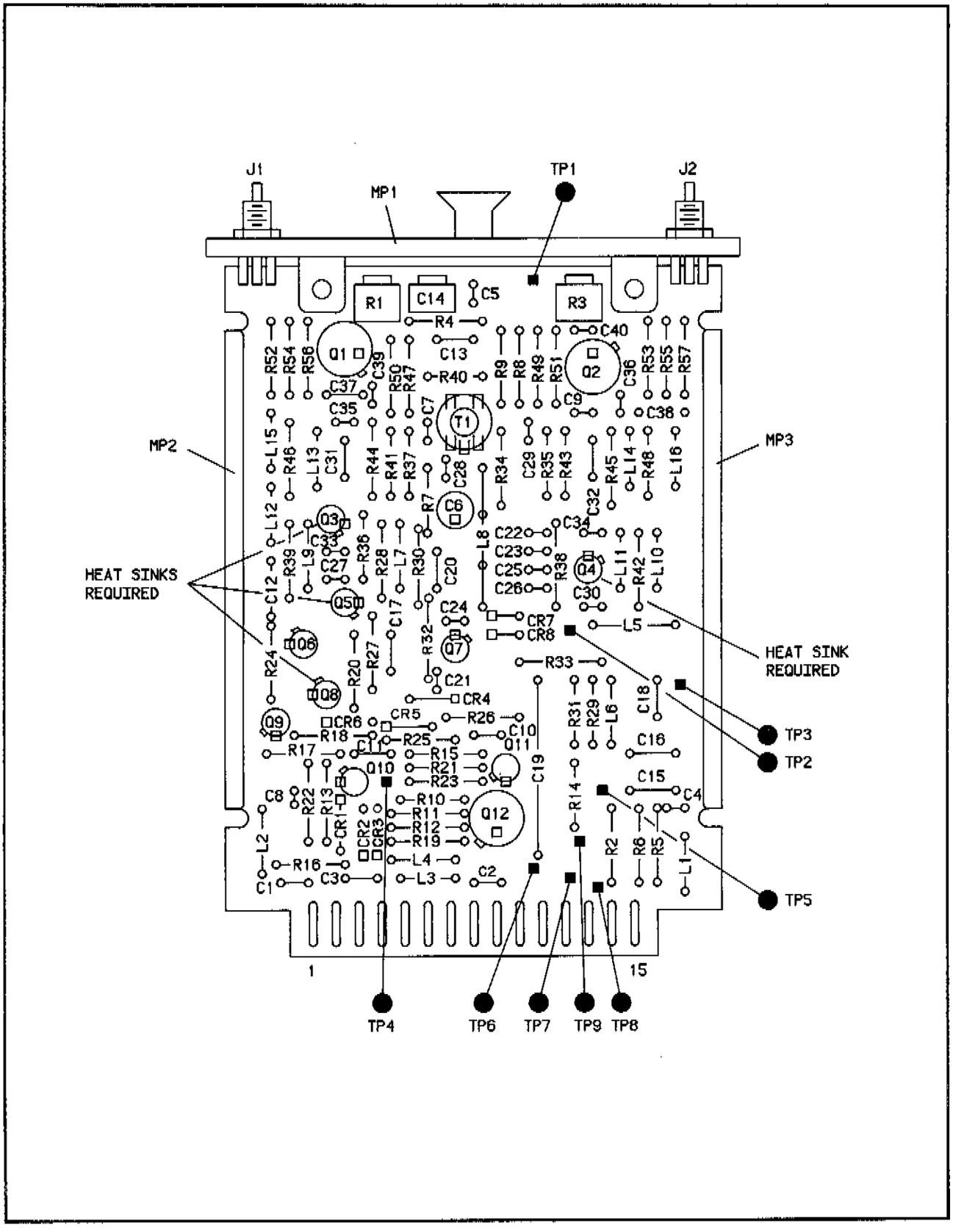


Figure 8-428. A3A4 N Loop Voltage Controlled Oscillator Component Locator

CHANGES

2441A and above	**On the A3A4 schematic:** • **A3A4R10, R12, R13, R16, R19** - Change the values of these resistors to the new values shown below: R10 to 3.83k R12 to 17.8k R13 to 21.5k R16 to 14.7k R19 to 75k
2549A and above	**On the A3A4 schematic:** • **A3A4R1, R12, R13, R16, R24, R25** - Change the values of these resistors to the new values shown below: R1 to 100k R12 to 23.7k R13 to 34.8k R16 to 31.6k R19 to 422 ohms R25 to 1k
2619A and above	**On the A3A4 schematic:** • **A3A4R24, R25** - Change the value of R24 to 26.1 ohms. Change the value of R25 to 316 ohms.
2936A and above	**On the A3A4 schematic:** • **A3A4R27, R28** - Change the value of R27 and R28 to 1k.

Fig 8-129
Sht 1 of 3

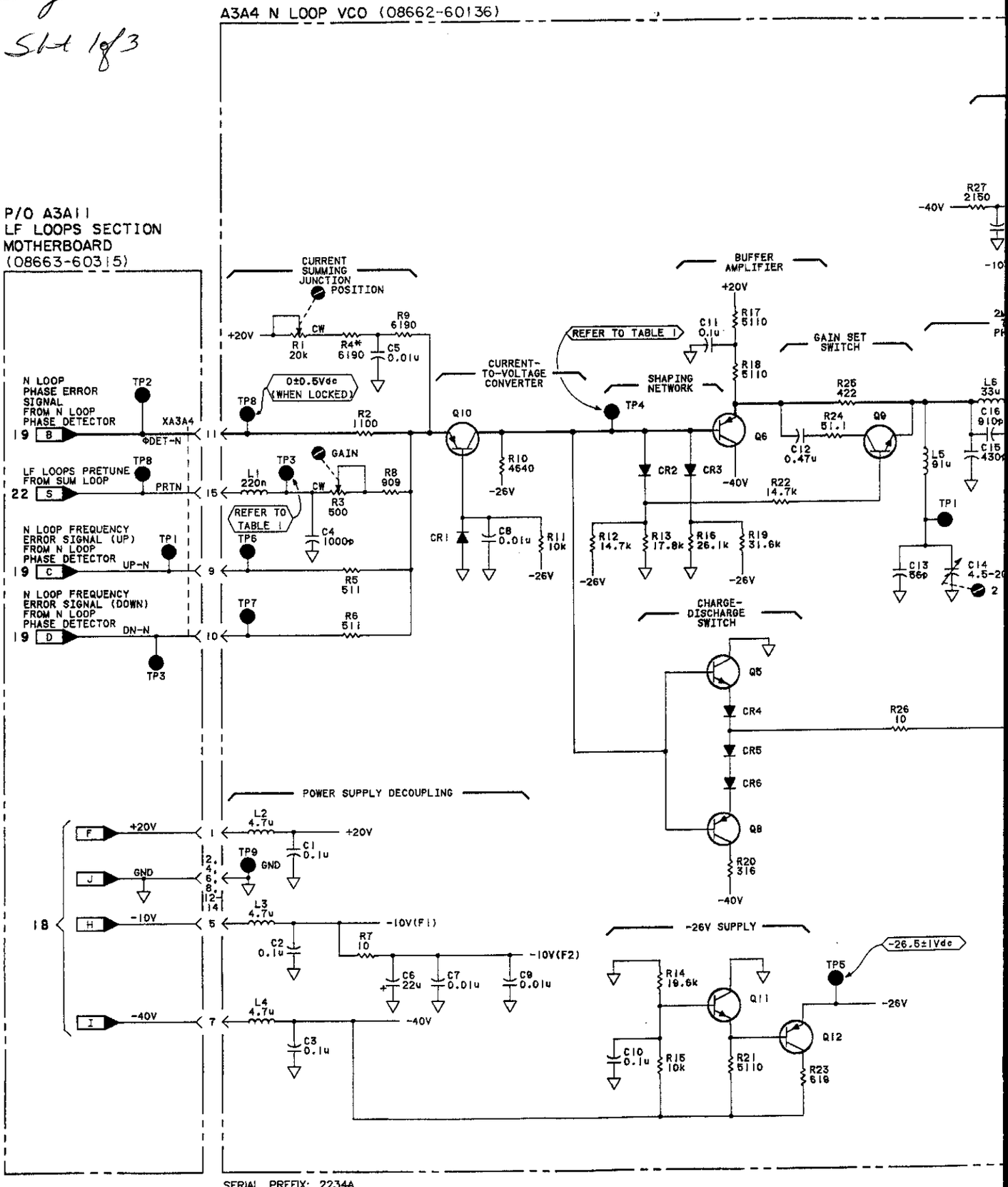


Fig 8-429 Sht 2 of 3

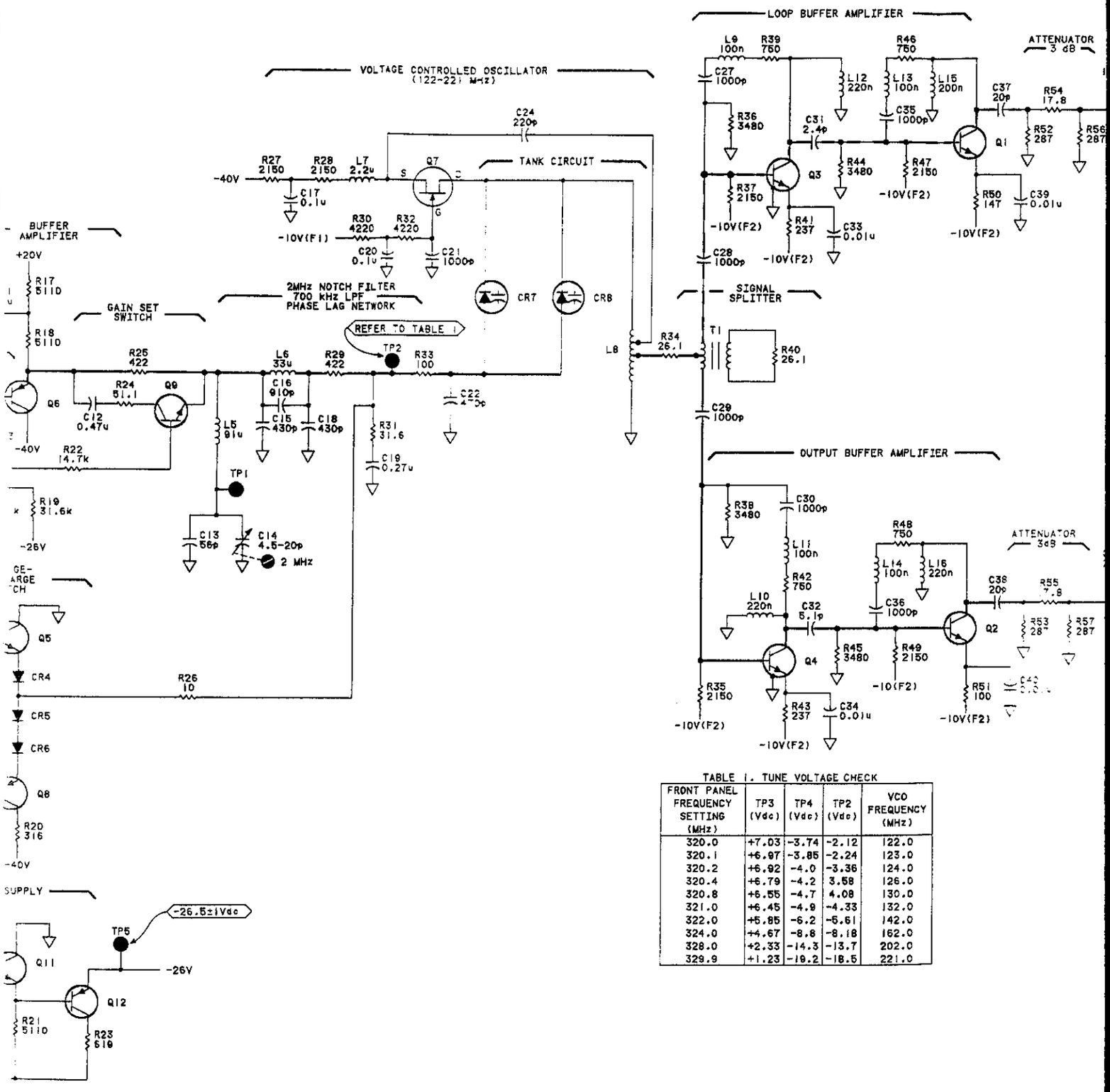
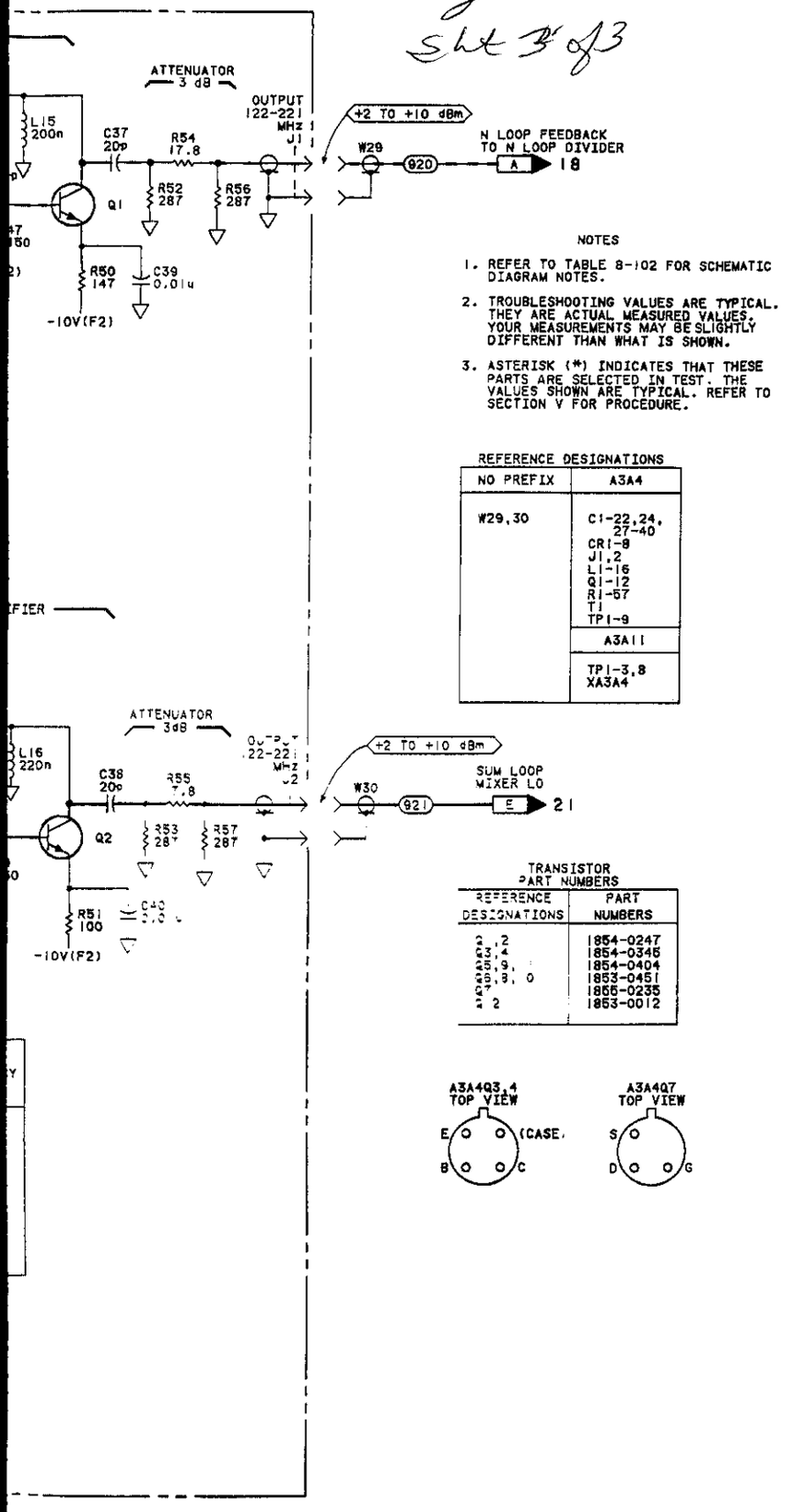


TABLE I. TUNE VOLTAGE CHECK

FRONT PANEL FREQUENCY SETTING (MHz)	TP3 (Vdc)	TP4 (Vdc)	TP2 (Vdc)	VCO FREQUENCY (MHz)
320.0	+7.03	-3.74	-2.12	122.0
320.1	+6.97	-3.85	-2.24	123.0
320.2	+6.92	-4.0	-3.36	124.0
320.4	+6.79	-4.2	3.58	126.0
320.8	+6.55	-4.7	4.08	130.0
321.0	+6.45	-4.9	-4.33	132.0
322.0	+5.85	-6.2	-5.61	142.0
324.0	+4.67	-8.8	-8.18	162.0
328.0	+2.33	-14.3	-13.7	202.0
329.9	+1.23	-19.2	-18.5	221.0

Fig 8-429
Sht 3 of 3



SERVICE SHEET 20

A3A4

Figure 8-429. A3A4 N Loop Voltage Controlled Oscillator Schematic

SERVICE SHEET 21
A3A5 SUM LOOP MIXER

REFERENCE BLOCK DIAGRAM 5
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

General

There are two main circuits on the Sum Loop Mixer Board. The mixer takes the Sum Loop VCO and N Loop VCO signals, mixes them down to a frequency band of 1 MHz to 2 MHz, and sends this band to the frequency detector. The frequency detector is composed of U2 through U6. This circuit detects when the sum loop frequency is greater than the N loop frequency and sends a Sum loop frequency error signal to the Sum Loop VCO Assembly (Service Sheet 23).

Mixer Circuitry

The sum loop mixer RF from the Sum Loop VCO (service sheet 23) and the sum loop mixer LO from the N Loop VCO (service sheet 20) enter the board via the J2 and J1 inputs, respectively. The S loop RF passes through a 10 dB pad and a limiter formed by U1. U1 has a gain of 10 dB and limits at +1 dBm. The output of this limiter stage is then capacitively coupled to the RF input of mixer U7.

The S loop LO signal from the N Loop VCO (service sheet 20) is limited by CR1 and CR3 and attenuated by the 3 dB pad formed by R7, R9, and R11. The signal is then applied to the LO input of the mixer. The output IF from the mixer varies between 1 MHz and 2 MHz. The output of the mixer is filtered by a 10 MHz low-pass filter formed by C14, L3, C15, L4, and C16, and then enters the limiter/buffer amplifier formed by transistors Q1 and Q2. The resulting signal is the sum loop IF signal. The level of this signal is approximately 4V p-p.

Frequency Detecting Circuitry

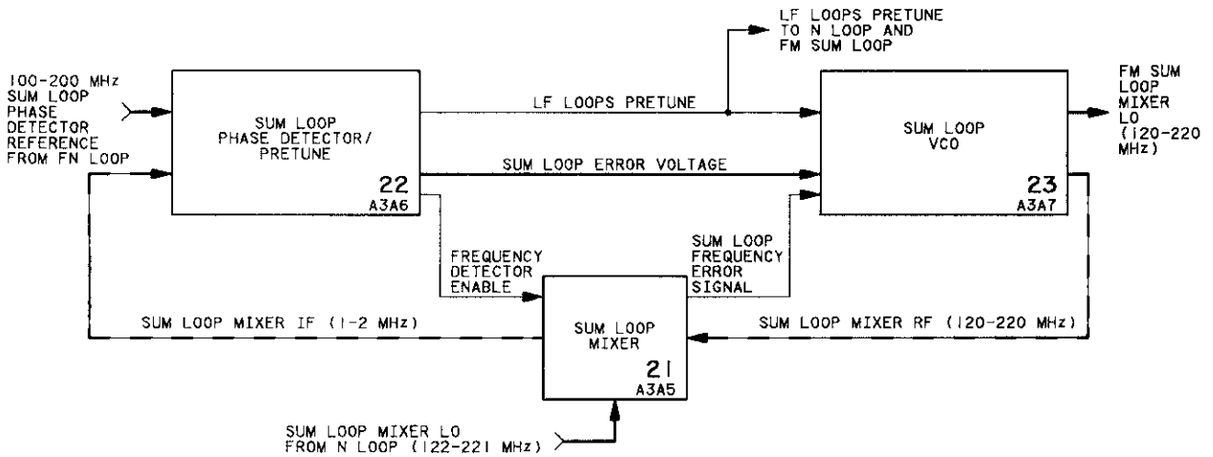
The frequency detecting circuit determines if the S loop frequency exceeds the N loop frequency. The S loop normally extends from 120 MHz to 220 MHz; the N loop's frequency range is from 122 MHz to 221 MHz. The S loop frequency should always be 1 MHz to 2 MHz below the N loop frequency. If it becomes more than 2 MHz above the N loop, the S loop will reverse and send the VCO in the wrong direction.

The frequency detecting circuit keeps the S Loop VCO frequency below that of the N loop. The decade divider circuits (U2 and U3) divide the outputs of the two VCOs by 10. The divided signals at TP1 and TP2 enter frequency detector U4, which determines when the S loop

frequency is greater than the N loop frequency. When the S loop frequency is greater, the output at pin 12 of U4 goes HI, causing a ramp voltage to be applied to pin 2 of comparator U5.

The ramp voltage at pin 2 of U5 is compared against the reference voltage at pin 3, and a TTL pulse is generated at the pin 7 output. This TTL pulse triggers monostable one-shot U6, producing a 3.4 microsecond pulse which is sent to the S Loop VCO as a frequency error signal. A pulse train is output from U6 as long as the S loop frequency is greater than the N loop frequency. This pulse train is filtered, summed with the S loop error and pretune currents, and converted to a voltage so that it can be used to help decrease the S Loop VCO frequency.

The frequency detector is disabled by the frequency detector enable line (at board pin 11) when the S Loop VCO is locked. The frequency detector enable line is also sent to pin 14 of U2 and U3, turning OFF the dividers to prevent spurs from being generated.



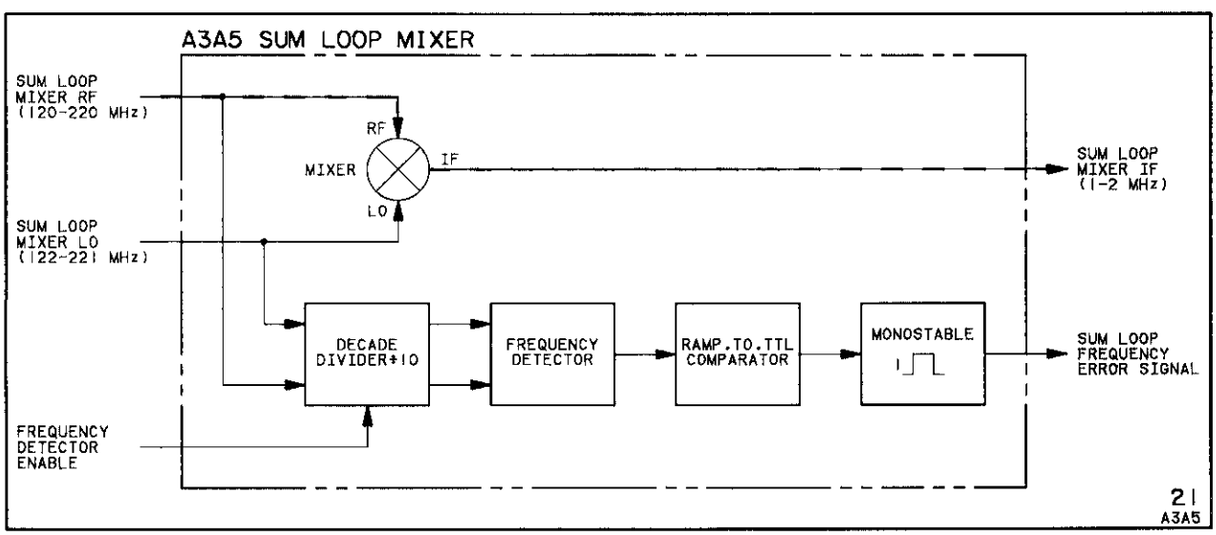


Figure 8-430. A3A5 Sum Loop Mixer Block Diagrams

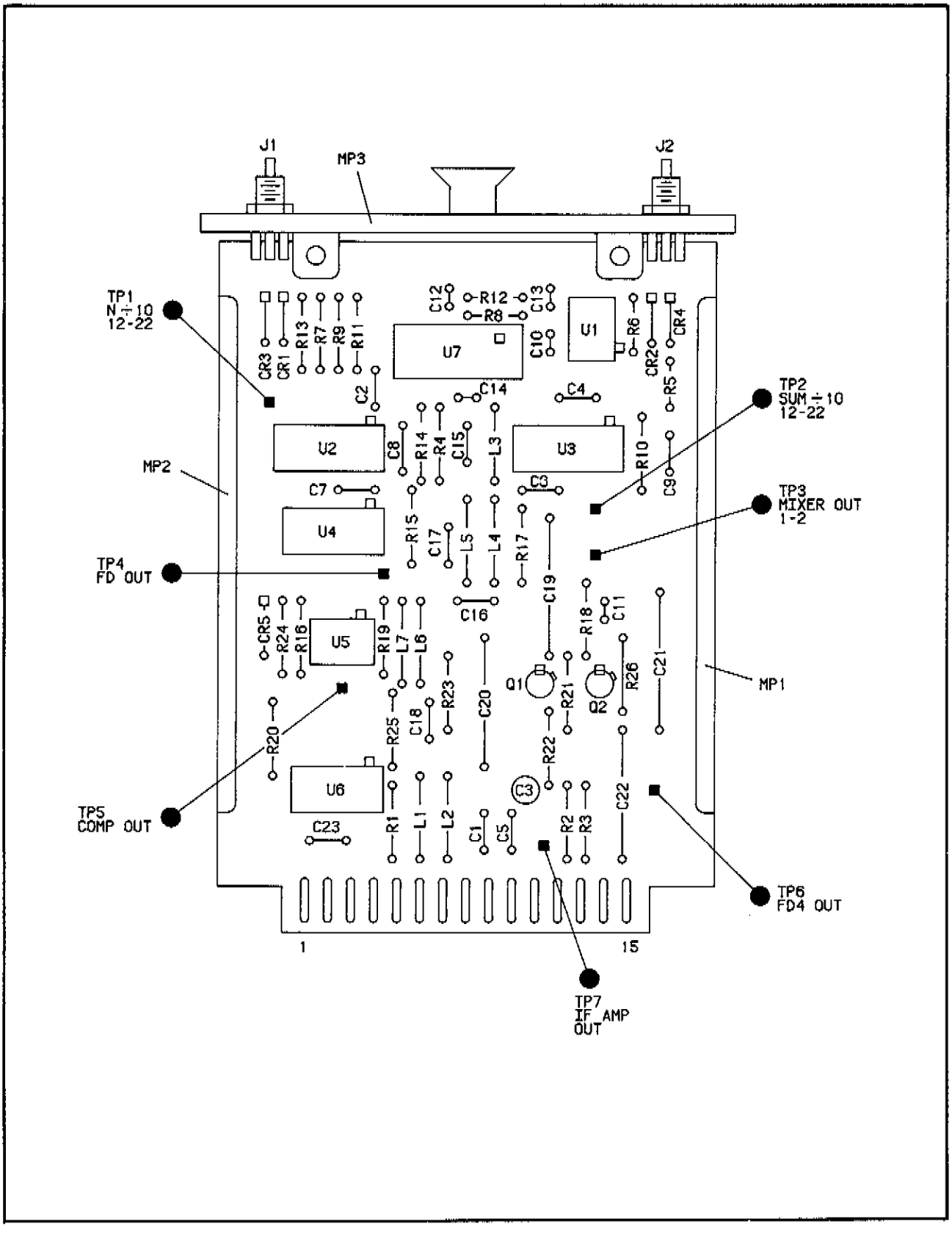


Figure 8-431. A3A5 Sum Loop Mixer Component Locator

CHANGES

2234A to 2416A

On the schematic:

- NOTES - Add NOTE 4 as follows:

  4. For instruments with serial number prefixes lower than 2419A: A3A5U2 and A3A5U3 must be replaced as a set with HP part number 1820-3517. In addition to replacing both U2 and U3, R13 and R14 must be removed from the board and replaced with terminal studs. The studs should be soldered in the existing R13 and R14 holes and the new value of R13 and R14 (0698-3443) should be soldered to the studs along with capacitors C24 and C25 (0160-4803). C24 should be soldered in parallel to R13 and C25 should be soldered in parallel to R14.

- A3A5U2, U3 - In the Table of Transistor and Integrated Circuit Part Numbers, change the part number of U2 and U3 to 1820-3517 and add the note, "Refer to NOTE 4."

On the A3A5 schematic:

- A3A5U2, U3 - Next to U2 and U3, add "(NOTE 4)".

2419A and Above

On the A3A5 component locator:

- A3A5C24, C25 - Add C24 parallel to R13. Add C25 parallel to R14.

- A3A4MP4-MP7 - Add MP4-7 in the mounting holes for R13 and R14. (MP4-7 are posts to which R13, R14, C24, and C25 are soldered.)

On the A3A5 schematic:

- A3A5C24, C25 - Add C24 (68p) in parallel with R13 and add C25 (68p) in parallel with R14.

- A3A5R13, R14 - Change the value of R13 and R14 to 287 ohms.

Fig 8-432
Sht 1 of 3

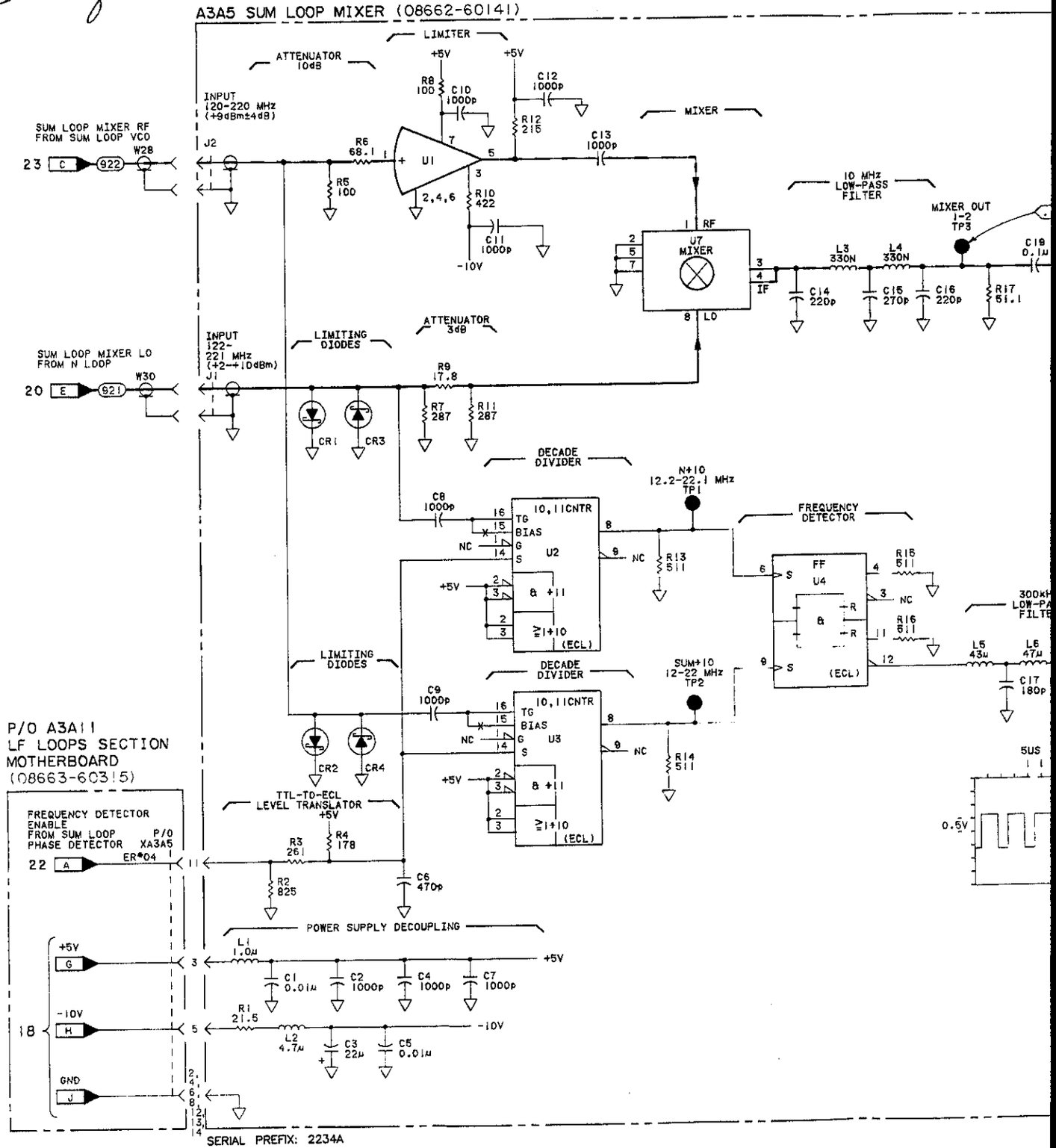
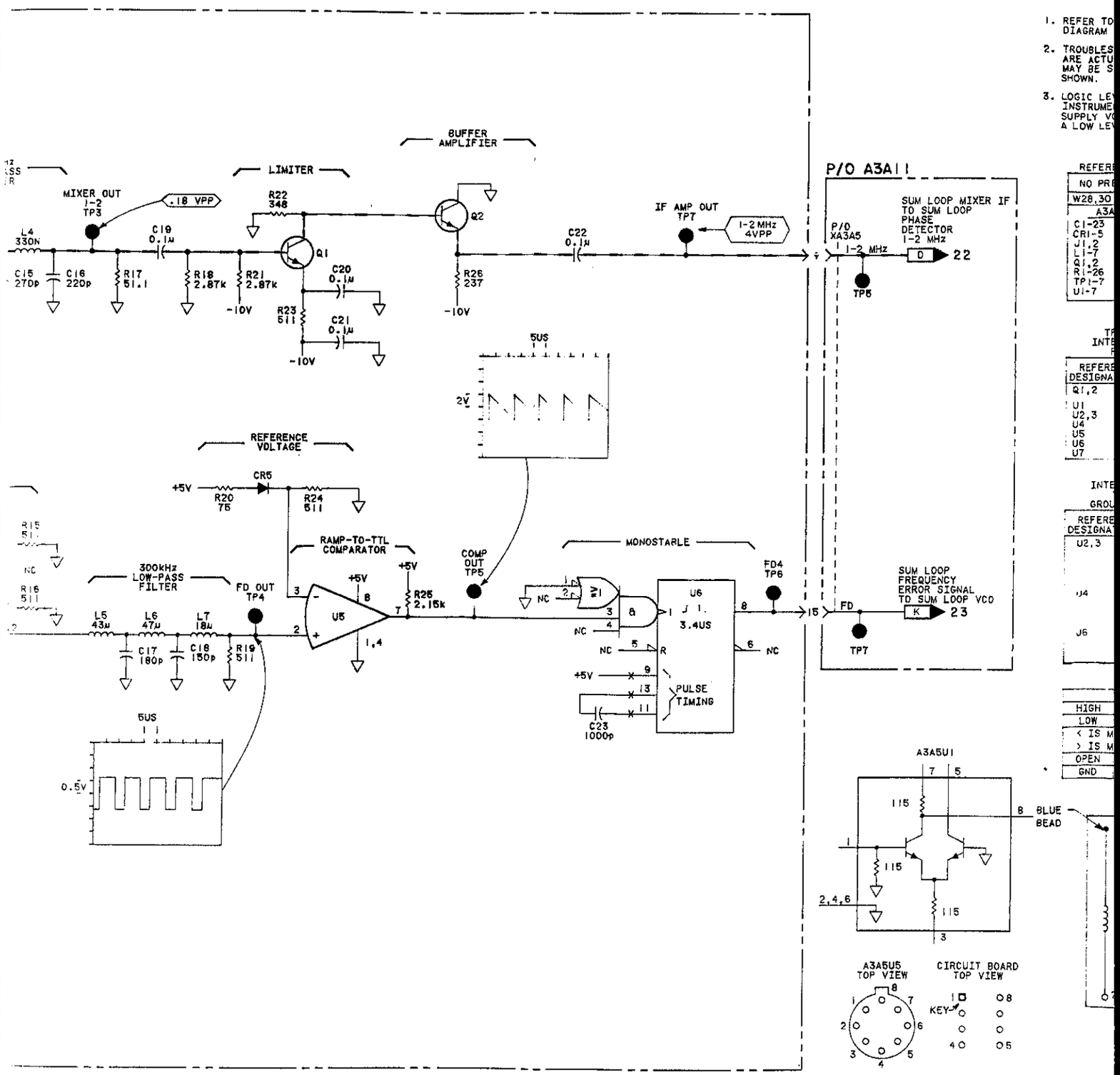


Fig 8-432
Sht 2 of 3



1. REFER TO DIAGRAM
2. TROUBLES ARE ACTU MAY BE S SHOWN.
3. LOGIC LE INSTRUME SUPPLY VO A LOW LE

REFER
NO PR
W28,30
A3A
C1-23
CR1-5
J1,2
L1-7
Q1,2
R1-26
TP1-7
U1-7

REFERE DESIGNA
Q1,2
U1
U2,3
U4
U5
U6
U7

REFERE DESIGNA
U2,3
U4
U6

HIGH
LOW
< IS M
> IS M
OPEN
GND

Fig 8-432
Sht 3 of 3

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NONSTANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS ≥4.0V; A LOW LEVEL IS ≤3.5V

A3A11

SUM LOOP MIXER IF TO SUM LOOP PHASE DETECTOR 1-2 MHz

D 22

SUM LOOP FREQUENCY ERROR SIGNAL TO SUM LOOP VCO

K 23

REFERENCE DESIGNATIONS

NO PREFIX	A3A11
W28,30	TP5,7
A3A5	XA3A5
C1-23	
CR1-5	
J1,2	
L1-7	
Q1,2	
R1-26	
TP1-7	
U1-7	

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,2	1854-0404
U1	1826-0372
U2,3	1820-1780
U4	1820-1344
U5	1826-0026
U6	1820-0704
U7	0955-0095

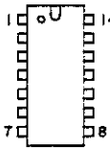
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U2,3	+5V - 4,5 ▽ - 10,12,13 NC - 6,7,11
U4	+5V - 1,14 ▽ - 7
U6	+5V - 14 ▽ - 7

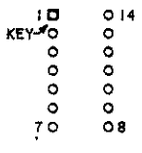
LOGIC LEVELS

	TTL	ECL (NOTE3)
HIGH	>+2V	>+4.0V
LOW	<+0.8V	<+3.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	LOW
GND	LOW	HIGH

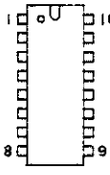
A3A5U4,6 TOP VIEW



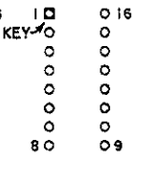
CIRCUIT BOARD TOP VIEW



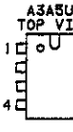
A3A5U2,3 TOP VIEW



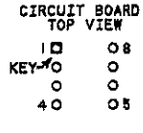
CIRCUIT BOARD TOP VIEW



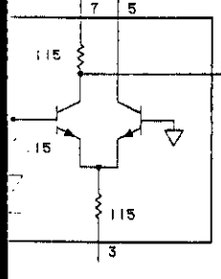
A3A5U1 TOP VIEW



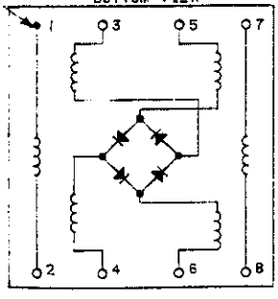
CIRCUIT BOARD TOP VIEW



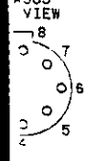
A3A5U1



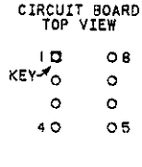
A3A5U7 MIXER BOTTOM VIEW



A5U5 VIEW



CIRCUIT BOARD TOP VIEW



SERVICE SHEET 21

A3A5

Figure 8-432. A3A5 Sum Loop Mixer Schematic

SERVICE SHEET 22
A3A6 SUM LOOP PHASE DETECTOR AND PRETUNE

REFERENCE BLOCK DIAGRAM 5
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

General

There are two independent circuits on the Sum Loop Phase Detector Board. One is a pretune circuit that coarsely tunes the three oscillators in the low frequency loops to within 3 MHz of the correct frequency so that the search and lock time for the loop is decreased.

The upper portion of the service sheet shows the phase detector circuitry. This section has two inputs. One is the S loop IF signal input and the other is the fractional-N loop VCO output (S Loop phase detector reference). The S loop IF signal is compared against the reference signal, and error pulses are generated at the output to keep these two signals at the same frequency. The error pulses generate an error voltage which is sent to the S Loop VCO (service sheet 23).

Pretune Circuitry

The pretune circuit consists of transistors Q1 through Q14. Q1 through Q8 are controlled by BCD lines from the Frequency Output Board via pins 10-13 and 25-28. The BCD weighted currents at the collectors of transistors Q1 through Q8 in the D/A converter are summed at TP4. These weighted currents are subtracted from the current that would normally flow through Q10 from R44 and R45. The net current out of Q10 appears as a voltage across R47. As more transistors are turned ON, less current flows through Q10 and the voltage across R47 approaches 0 volts.

Q9 sets a reference voltage that clamps the emitter of Q10 to 10 volts. Q11 and Q14 form a dual emitter-follower buffer amplifier. Its output range is 1.2 volts to 7.0 volts. After passing through a 1 MHz low-pass filter, this voltage is sent to the VCO summing junctions for the N loop, S loop and FMS loop. This pretunes the three oscillators to frequencies where the loops should lock.

Phase Detector Circuitry

The reference signal for the phase detector circuitry comes from the Fractional-N Loop at 100 MHz to 200 MHz. It is divided by 100 by a circuit formed by U1 and U2 and is then sent to U4A.

The second input to the phase detector circuitry is the sum loop IF signal that comes from the S Loop Mixer Board (service sheet 21). This signal enters the board via pin 9 and goes to pins 1 and 2 of U3, a schmitt trigger. The input waveform is converted to a square wave by this circuit so that it can be used by the digital phase detector.

The phase detector is formed by flip-flops U4A, U4B and gate U3B. One flip-flop is latched HI by the S loop phase detector reference signal and one is latched HI by the S loop IF signal. Once both flip-flops are set, the output of U3B goes HI, resetting them. As a result, the output of the flip-flops is a signal with a pulse width equal to the time difference between the signals driving U4A and U4B. The pulse width is wide when there is a large phase or frequency difference and is narrow when both signals are in phase. A ramp shaped signal appears at TP3 and TP6 (only one; never both) depending on the direction of the frequency phase shift.
The ramp waveform at either TP3 or TP6 is sent to the differential amplifier integrator formed by Q13, Q15, and Q12. The feedback loop for this circuit is composed of C31 and R57. The output of the integrator passes through R65 and R66 before leaving the board as the error voltage to the L Loop VCO (service sheet 23). When locked, this output (at pin 30) is 0 $\pm$ 0.5 volts. Diodes CR2 through CR7 limit the total voltage at C31 (in the feedback loop) so that the charge time of C31 is not increased if a transient occurs during locking.

Out-of-Lock Detector Circuitry

The out-of-lock detector formed by U3C and U5C produces a pulse that triggers the monostable one-shot formed by U6 when the pulses from U4 are wide. U6 in turn lights the out-of-lock LED. A signal is also output from pin 25 and is sent to the Sum Loop IF Board, enabling the frequency detector circuitry.

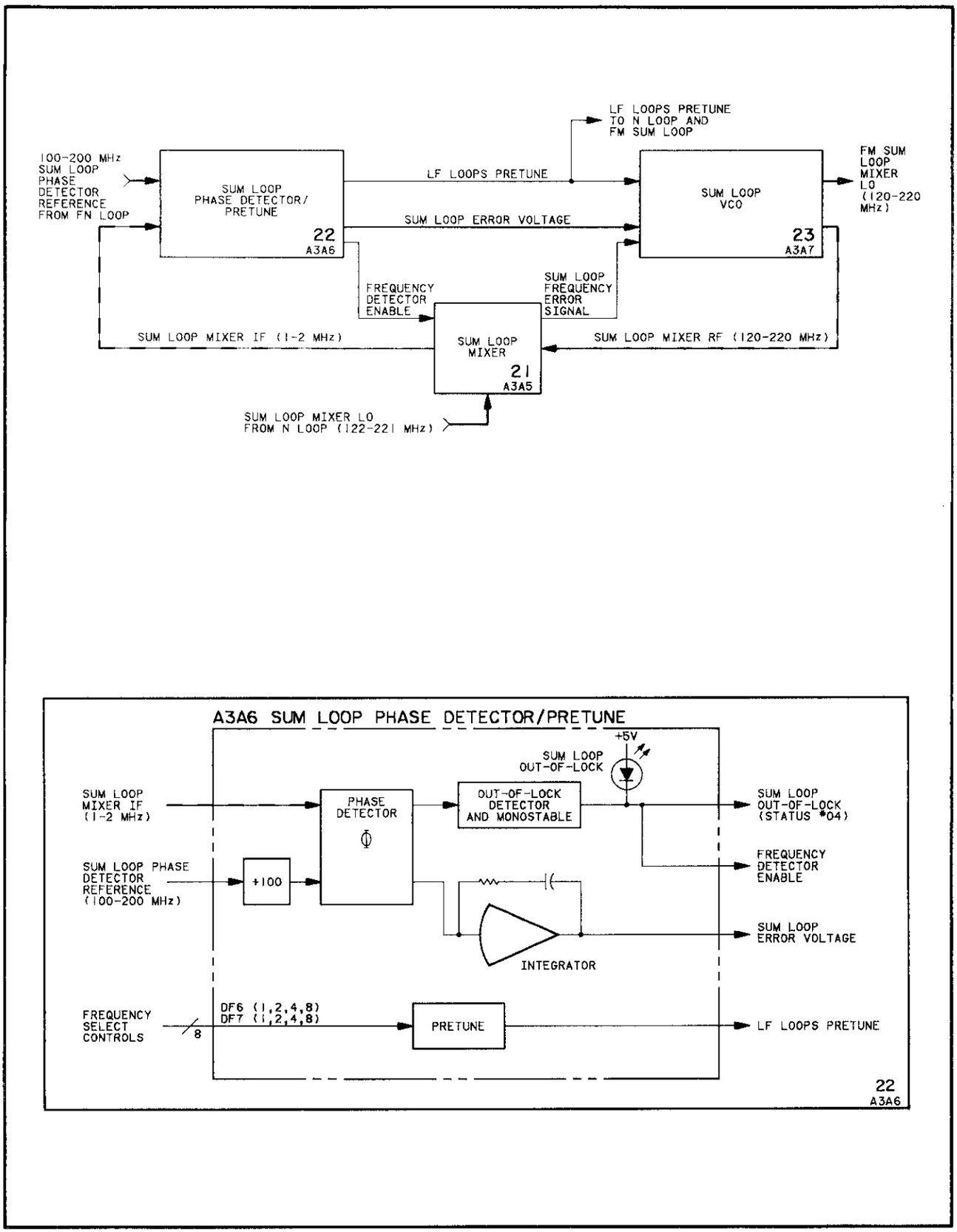


Figure 8-433. A3A6 Sum Loop Phase Detector Block Diagrams

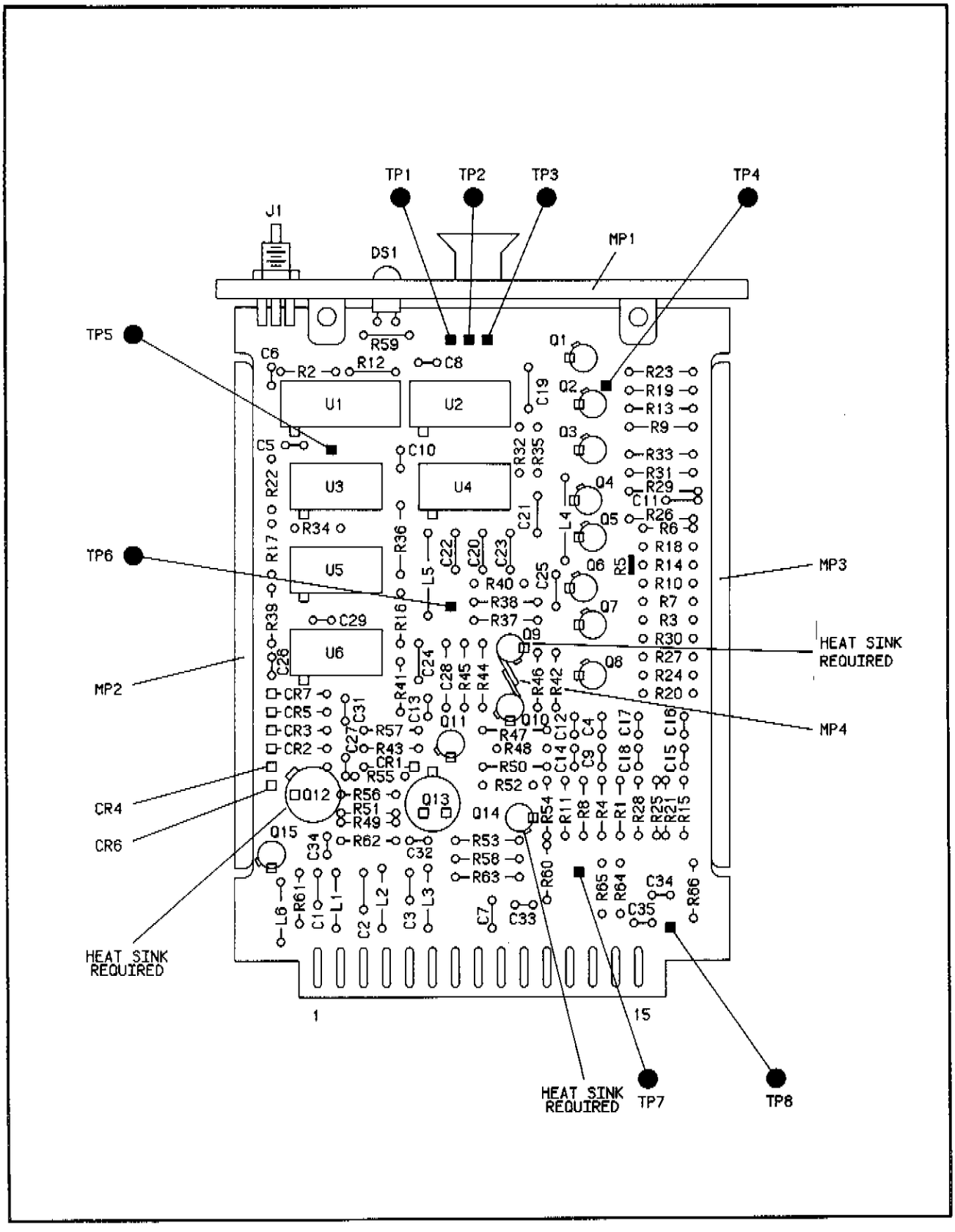


Figure 8-434. A3A6 Sum Loop Phase Detector Component Locator

CHANGES

All serial prefixes

On the A3A6 schematic:

- A3A6R1, R4, R8, R11, R15, R21, R25, R28 - Change the value of these resistors to 909 ohms.
- A3A6R3, R7, R10, R20, R24, R27, R30 – Change the value of these resistors to 2.37k.
- A3A6R14 - Change the value of R14 to 681 ohms.

2601A and Above

On the schematic:

- A3A6Q13 - In the Table of Transistor and Integrated Circuit Part Numbers, change the part number of Q13 to 1854-1046.

Fig 8-435 Sht 10f4

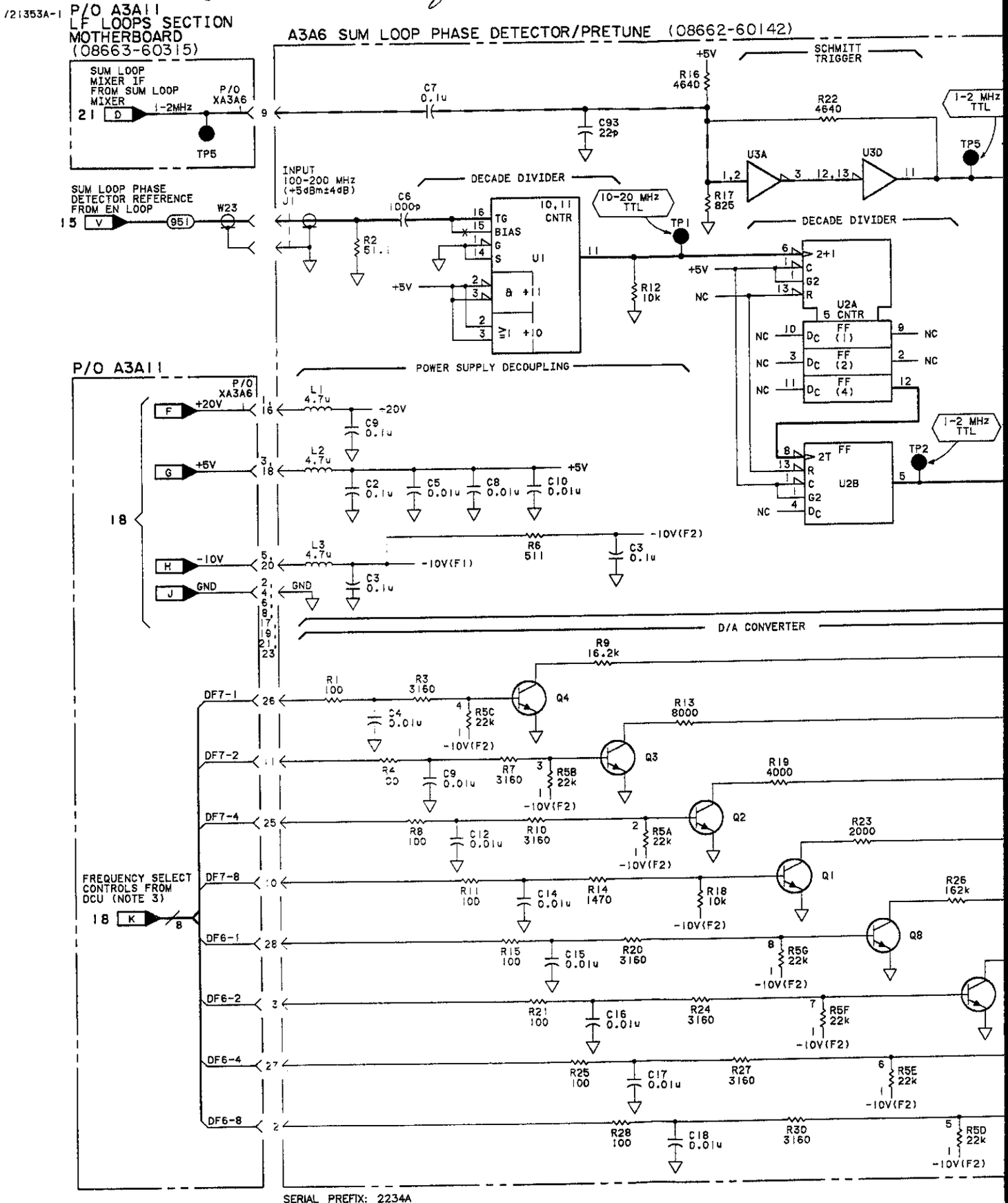


Fig 8-435 Sht 2 of 4

(662-60142)

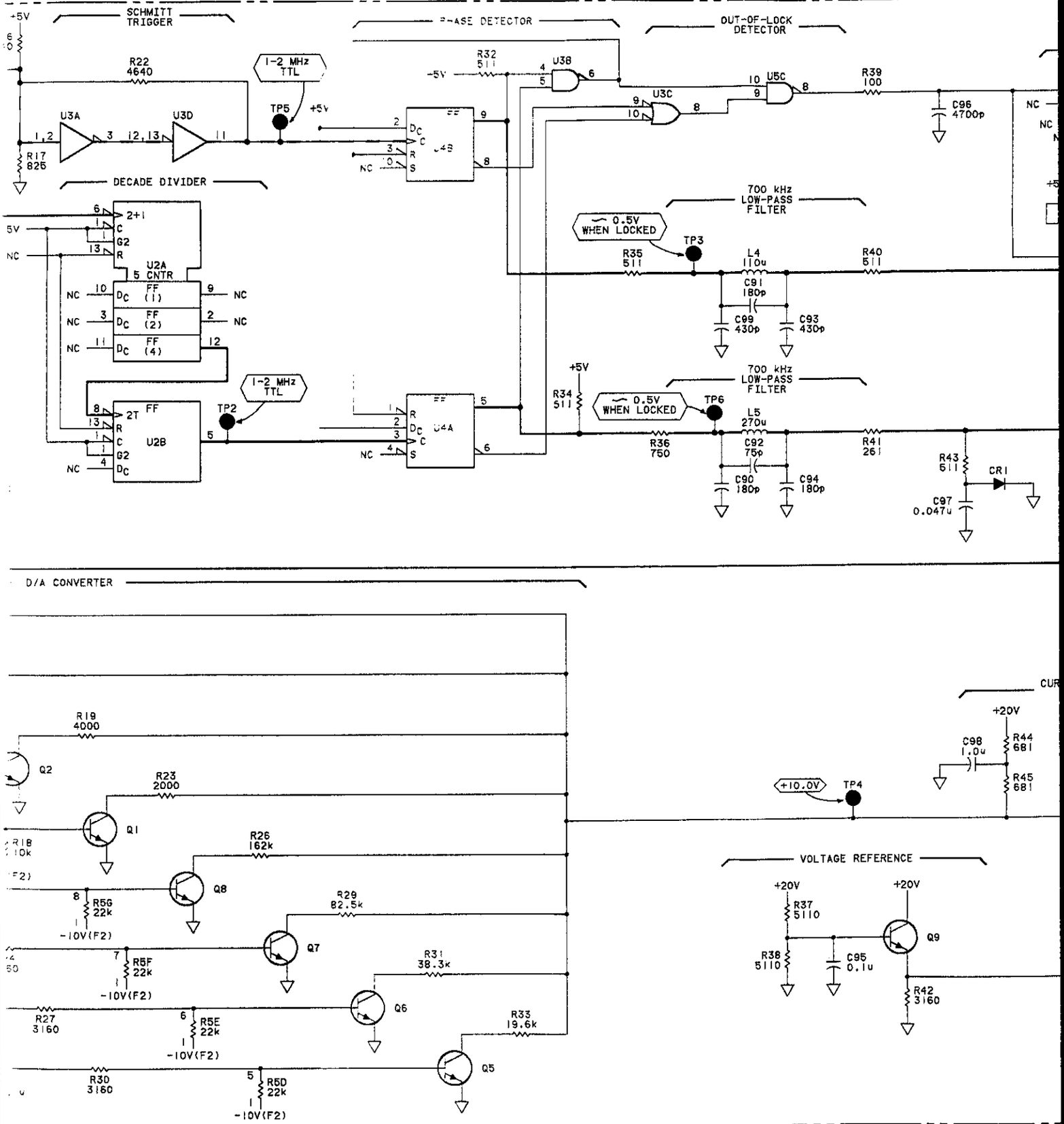
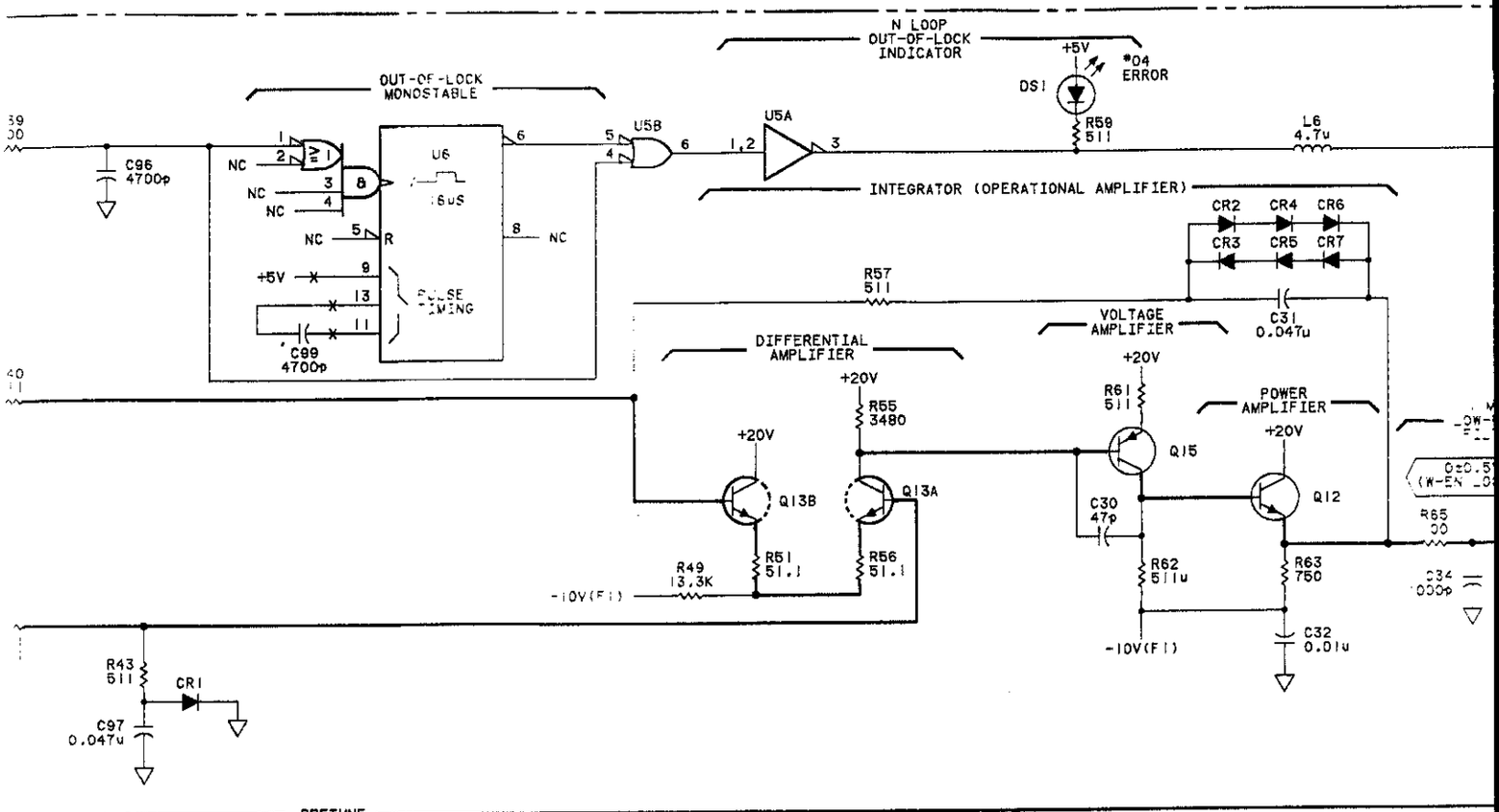


Fig 8-435 Sht 3 of 4



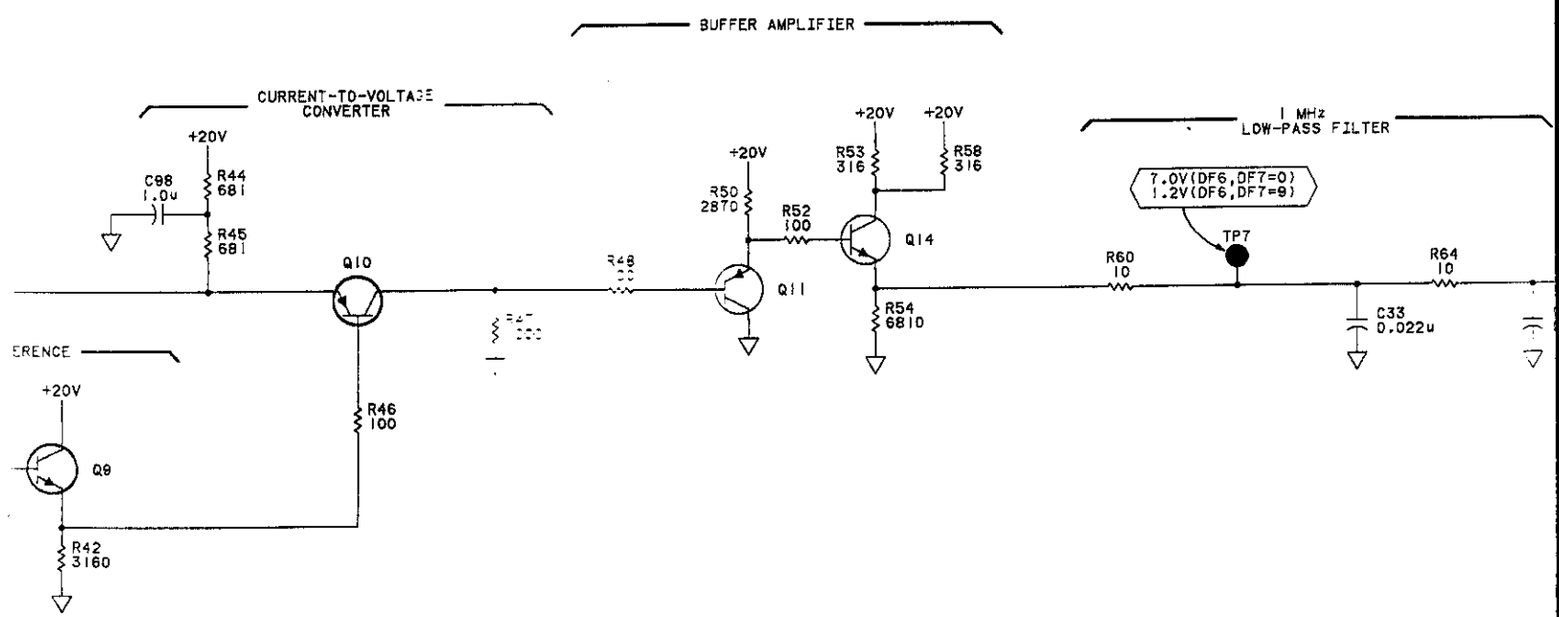
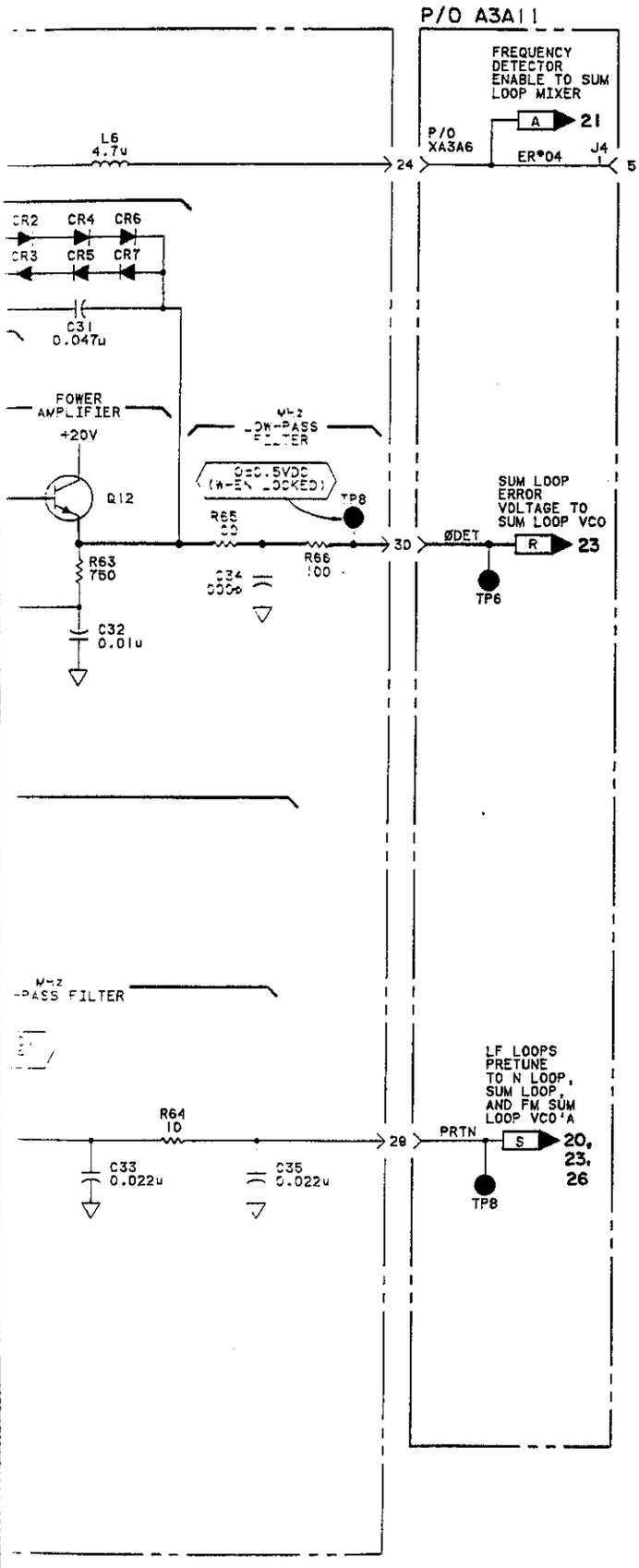


Fig 8-435 Sht 4 of 4



NOTES

1. SEE TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENT MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. MNEMONICS DF6-1 TO DF7-8 REPRESENT THE FREQUENCY DIGITS ON THE FRONT PANEL AND THE BCD WEIGHING.

REFERENCE DESIGNATIONS

NO PREFIX	A3A11
W23 W52	J4 TP5,6,8 XA3A6
A3A6	
C1-35 CR1-7 DS1 J1 L1-6 Q1-15 R1-66 TP1-8 U1-6	

LOGIC LEVELS

	TTL
HIGH	> +2V
LOW	< +0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW

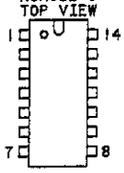
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1-9,14	1854-0404
Q10,11,15	1853-0451
Q12	1854-0247
Q13	1854-0475
U1	1820-1780
U2	1820-0751
U3	1820-1197
U4	1820-1112
U5	1820-0681
U6	1820-0704

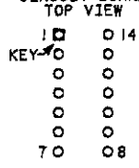
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V - 4,5 ▽ - 10,12,13 NC - 6-9
U2-6	+5V - 14 ▽ - 7

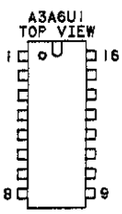
A3A6U2-6 TOP VIEW



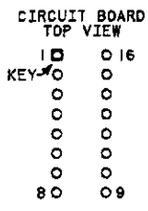
CIRCUIT BOARD TOP VIEW



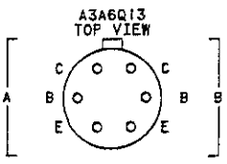
A3A6U1 TOP VIEW



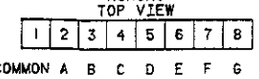
CIRCUIT BOARD TOP VIEW



A3A6Q13 TOP VIEW



A3A6R5 TOP VIEW



SERVICE SHEET 22

A3A6

Figure 8-435. A3A6 Sum Loop Phase Detector Schematic

SERVICE SHEET 23
A3A7 SUM LOOP VCO

REFERENCE BLOCK DIAGRAM 5
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

General

This board contains the voltage controlled oscillator and associated circuitry for the FM Sum Loop. There are three frequency control inputs to this board and two outputs. One output is the FM sum loop mixer RF; the other goes to the high frequency loops section. The frequency control inputs are summed, shaped, amplified and filtered before being used to control the frequency of the voltage controlled oscillator.

Current Summing Junction

The inputs are combined at the summing junction before entering amplifier Q10. Q10 amplifies the summed currents from the three frequency control inputs and converts them to a control voltage.

One of the three inputs is the sum loop frequency error signal (pin 11) which comes from the Sum Loop Mixer Board (service sheet 49). The other two are the pretune signal (pin 10) and the sum loop error signal (pin 9). Both come from the Sum Loop Phase Detector Board (service sheet 22). The pretune line has a gain adjustment which allows the range of the VCO to be set. The maximum tune range is approximately 100 MHz (+1.2 to +7.0 Vdc pretune voltage range).

Shaping Network and Buffer Amplifier

The shaping network in the collector of Q10 is a diode-resistor network composed of CR5, CR6, R13, R15, R17, and R20. This network shapes the pretune voltage so that a change in voltage produces a linear change in output frequency. Normally, varactors CR13 and CR14 in the VCO give it a non-linear output. The diode network, however, cancels out the non-linearity by switching in the diodes at the appropriate points.

Following the shaping network is an emitter-follower stage formed by Q7. This stage drives the filter network that removes the spurious signals from the loop and drives the phase lag network consisting of R32 and C20. The varactor voltage (at TP3) goes through R34 to the oscillator tank at CR13 and CR14. This is a negative voltage of -2 volts to -18 volts (-2 volts is the limit for the low frequency end and -18 volts is the limit for the high frequency end).

Gain Set Switch

Q6 is a transistor switch which increases the loop gain voltage as determined by the threshold point of CR6. Q6 turns on and shunts R26 so that the gain of Q7 at TP3 is increased by approximately 6dB. This causes the loop gain to increase and compensate for the decrease in gain of the varactors, which occurs close to the high frequency end.

Charge-Discharge Switch

Transistors Q5 and Q9 switch current into C20 through R24. These transistors are biased so that when the voltage at TP4 is two volts greater than the voltage at C20, either Q5 or Q9 turn on to quickly charge C20. This increases switching speed.

Voltage Controlled (Hartley) Oscillator

The oscillator itself is formed by Q8, which is a common gate FET amplifier. Capacitor C23 is a bypass capacitor for the varactors. L8 is a tapped inductor. The feedback loop feeds through C25 to the source of the FET. R28 and R30 set the dc current in the FET. R31 and R33 set the dc voltage at the gate.

Signal Splitter

The output of the VCO is tapped from L8 very close to ground and goes through R36 to transformer T1, which is a power splitter. This splitter supplies half power to each of the two amplifiers and provides substantial isolation between them.

Output and Loop Buffer Amplifiers

The loop buffer amplifier consists of Q1 and Q3. The output buffer amplifier consists of Q2 and Q4. The two transistors within each amplifier assembly are cascaded. The output of each amplifier is attenuated by a 3 dB pad before being output from the assembly. One of the outputs is sent to the FM sum loop mixer (LO input), the other to the sum loop mixer (RF input).

Minus 26 Volt Supply

The -26 volt on-board supply is powered by the main -40 volt supply. It is used as a reference voltage for the frequency breakpoints by the shaping network consisting of CR5 and CR6.

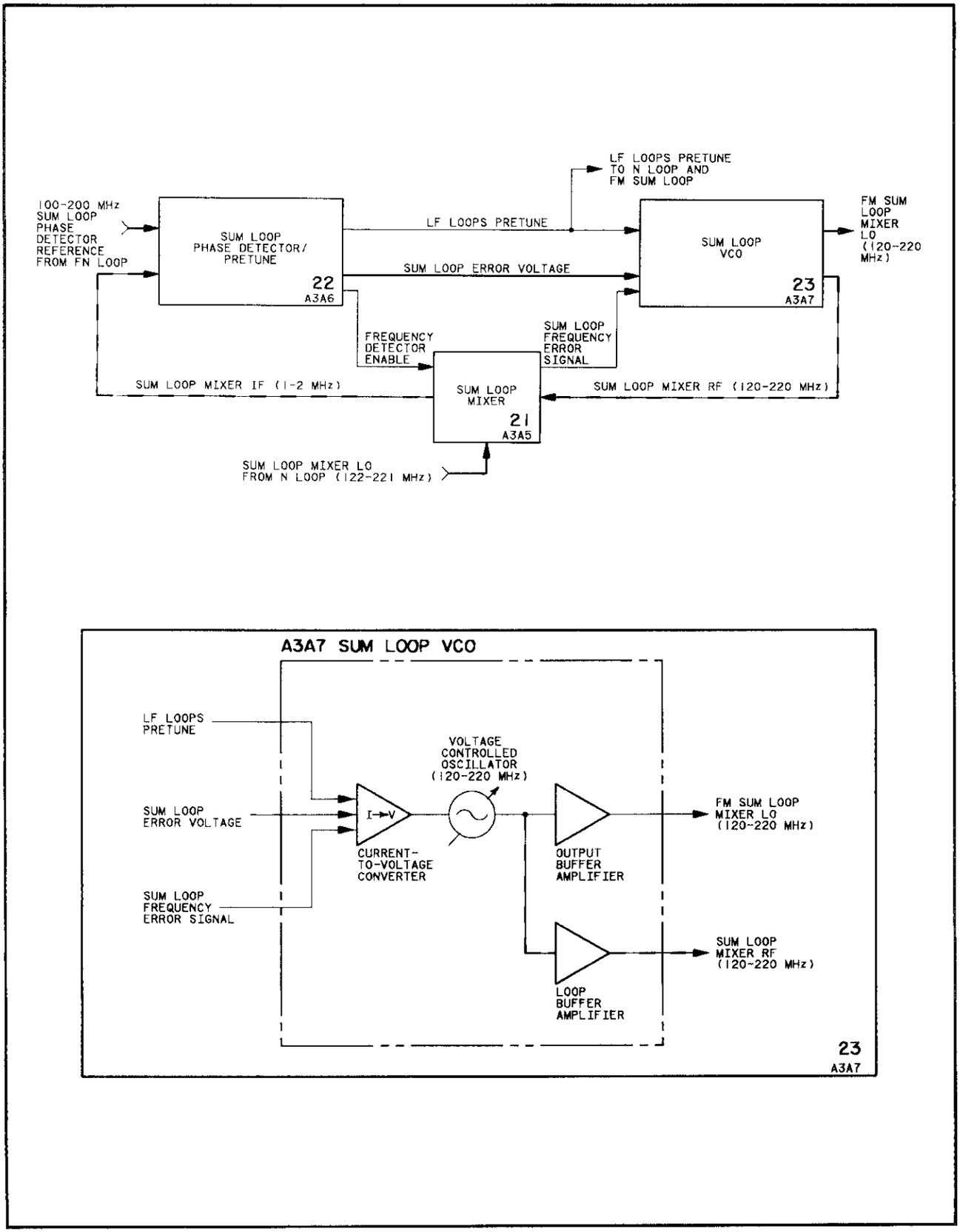


Figure 8-436. A3A7 Sum Loop Voltage Controlled Oscillator Block Diagrams

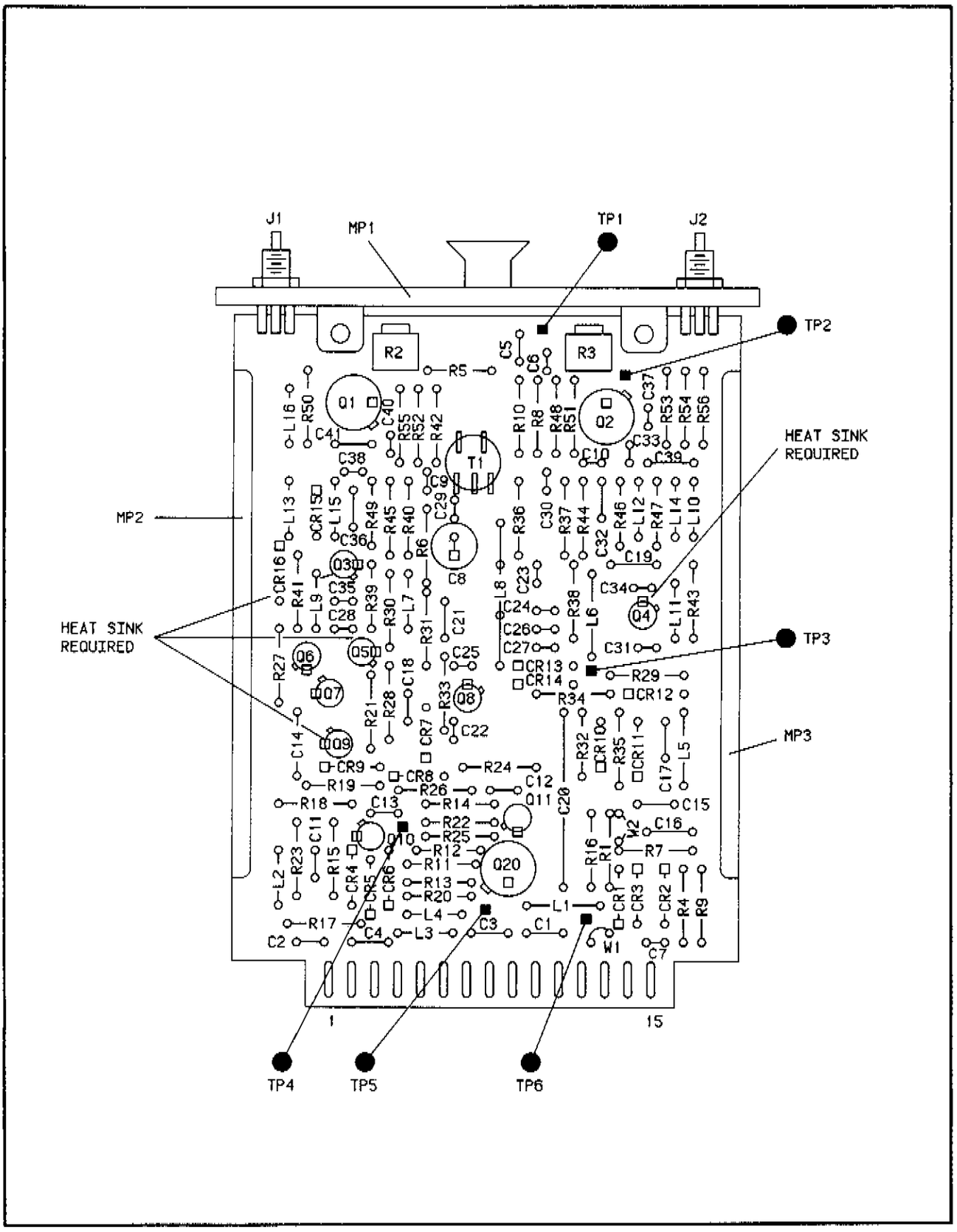


Figure 8-437. A3A7 Sum Loop Voltage Controlled Oscillator Component Locator

CHANGES

All Serial Prefixes	**On the A3A7 Component Locator:** • A3A7C23, C24, C26, C27 - Delete A3A7C23, C24, and C26. Change the existing C27 to C23.
2441A and above	**On the A3A7 Schematic:** • A3A7R12, R13, R15, R17, R20 - Change the values of these resistors to the new values shown below: R12 to 3.83k R13 to 17.8k R15 to 21.5k R17 to 14.7k R20 to 75k
2449A and above	**On the A3A7 schematic:** • A3A7R28, R30 - Change the value of R28 and R30 to 1.21k.
2549A and above	**On the A3A7 Schematic:** • A3A7R5*, R10, R12, R13, R15, R17, R20 - Change the values of these resistors to the new values shown below: R5* to 5.11k R10 to 5.11k R12 to 4.22k R13 to 21.5k R15 to 34.8k R17 to 26.1 ohms R20 to 90.9k
2936A and above	**On the A3A7 schematic:** • A3A7R28, R30 - Change the value of R28 and R30 to 1k.
All Serial Prefixes	**On the A3A7 schematic:** • A3A7R55 - Change the value of R55 to 100.

Fig 8-438 Sht 1 of 3

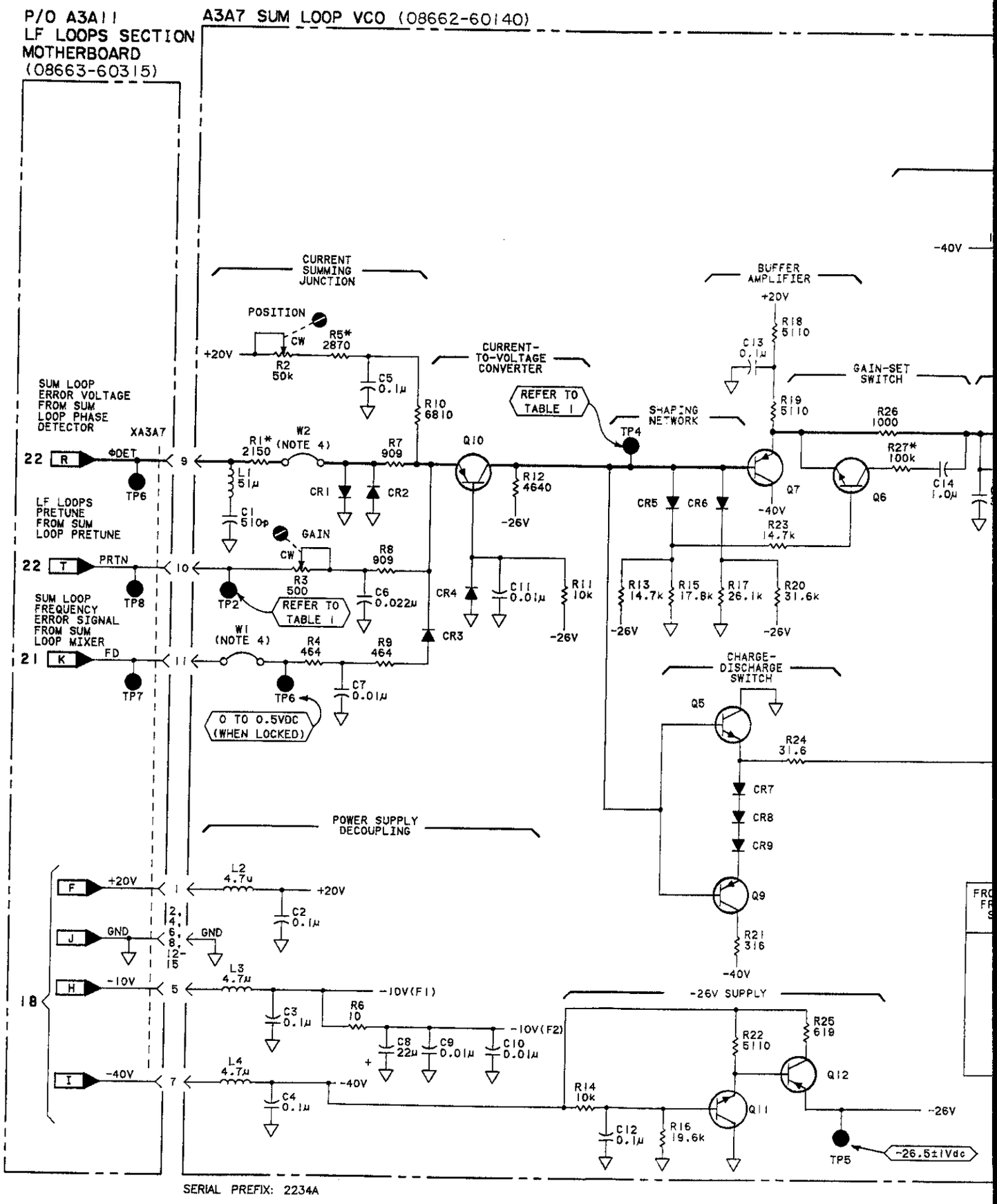


Fig 8-438 Sht 2 of 3

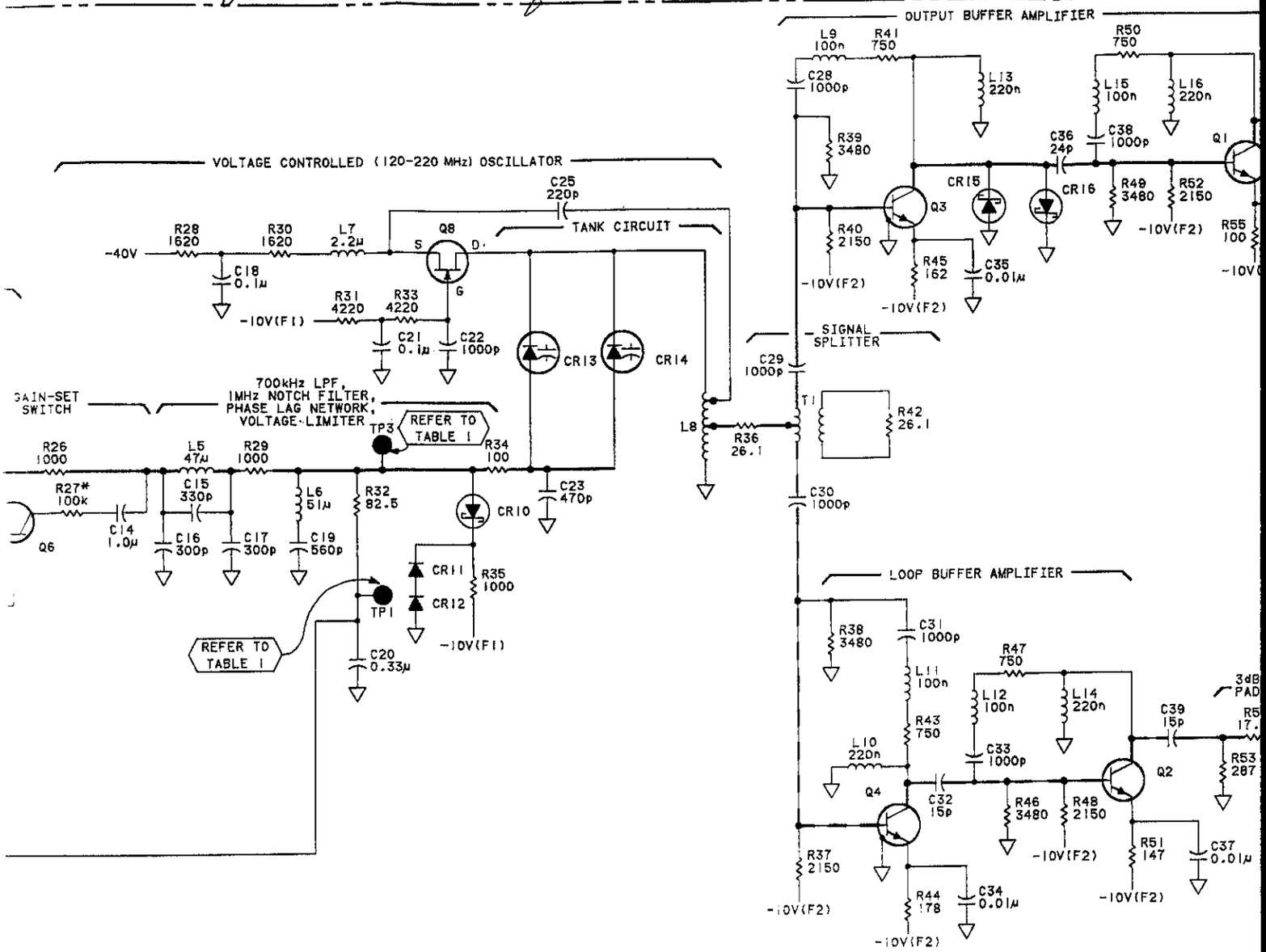
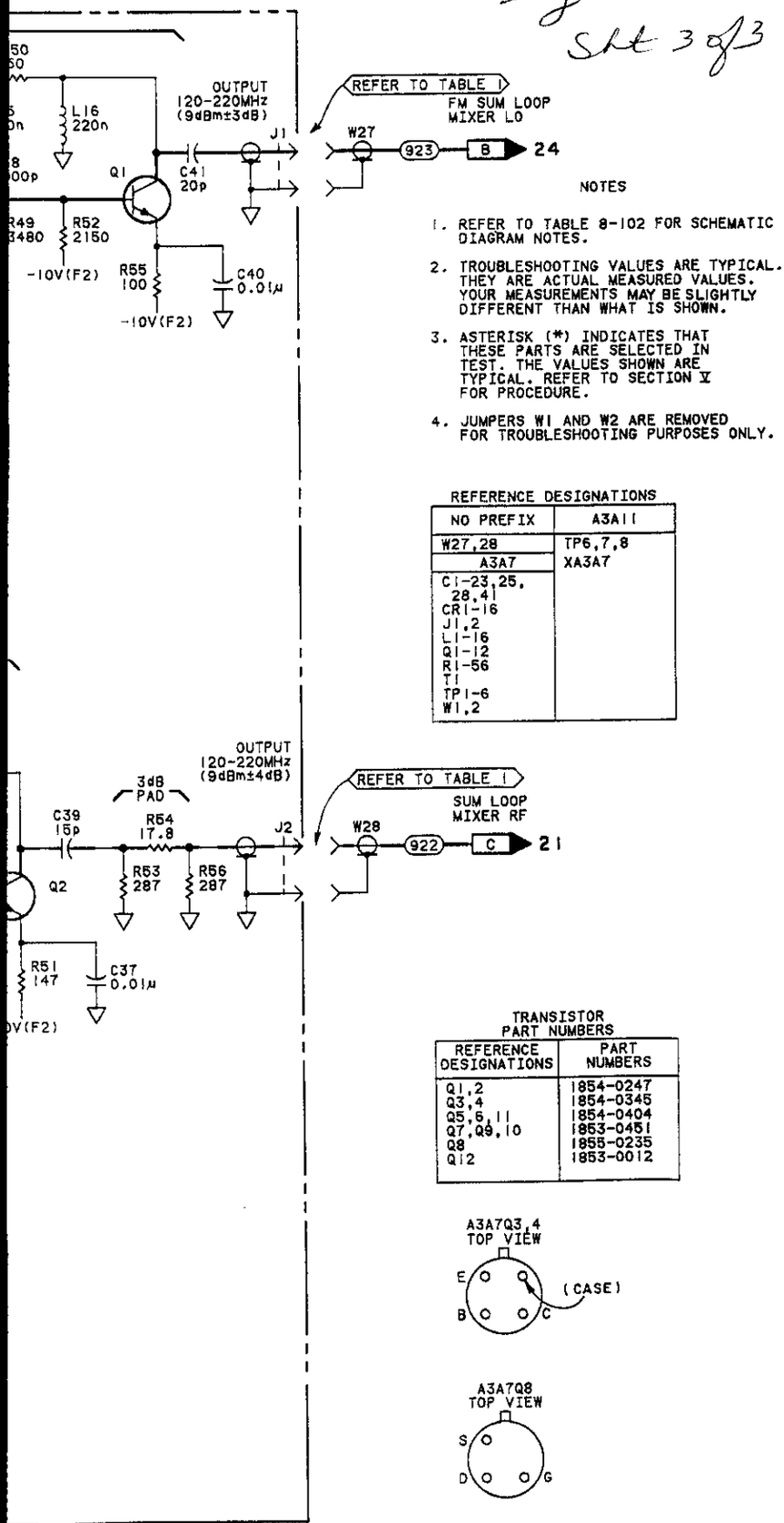


TABLE 1 TUNE VOLTAGE CHECK

FRONT PANEL FREQUENCY SETTING (MHz)	TP2 (Vdc)	TP4 (Vdc)	TP3 (Vdc)	TP1 (Vdc)	VCO FREQUENCY (MHz)
320.0	+7.03	-3.83	-3.23	-3.21	120.0
320.1	+6.97	-3.95	-3.35	-3.34	121.0
320.2	+6.91	-4.08	-3.47	-3.46	122.0
320.4	+6.78	-4.33	-3.73	-3.72	124.0
320.8	+6.55	-4.85	-4.24	-4.23	128.0
321.0	+6.44	-5.11	-4.51	-4.50	130.0
322.0	+5.85	-6.46	-5.86	-5.84	140.0
324.0	+4.67	-9.15	-8.54	-8.53	160.0
328.0	+2.33	-14.6	-13.9	-13.9	200.0
329.9	+1.23	-18.7	-18.0	-18.0	219.0

Fig 8-438
Sht 3 of 3



NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. ASTERISK (*) INDICATES THAT THESE PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL. REFER TO SECTION V FOR PROCEDURE.
4. JUMPERS W1 AND W2 ARE REMOVED FOR TROUBLESHOOTING PURPOSES ONLY.

REFERENCE DESIGNATIONS

NO PREFIX	A3A11
W27,28	TP6,7,8
A3A7	XA3A7
C1-23,25, 28,41 CR1-16 J1,2 L1-16 Q1-12 R1-56 T1 TP1-6 W1,2	

TRANSISTOR PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,2	1854-0247
Q3,4	1854-0345
Q5,6,11	1854-0404
Q7,Q9,10	1853-0451
Q8	1855-0235
Q12	1853-0012

SERVICE SHEET 23

A3A7

Figure 8-438. A3A7 Sum Loop Voltage Controlled Oscillator Schematic

SERVICE SHEET 24
A3A9 FM SUM LOOP MIXER

REFERENCE BLOCK DIAGRAM 5
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

General

There are two separate circuits on this service sheet. The upper portion of the schematic shows the integrator. The integrator takes the FM sum loop phase and frequency error signals from the FM Sum Loop Phase Detector Board (service sheet 25) and generates an FM sum loop error current which is sent to the FM Sum Loop VCO Board (service sheet 26).

The lower portion of the schematic shows the mixer circuitry. This section takes the FM sum loop VCO signal (service sheet 26) and the sum loop VCO signal (service sheet 23) and mixes them to produce the FM sum loop IF which is sent to the FM sum loop phase detector (service sheet 25).

Mixer Circuitry

The FM sum loop mixer RF (FMS loop VCO output) enters the board via J1, passes through the 3 dB attenuator pads and a 250 MHz low-pass filter before entering pin 1 of mixer U1. The FM sum loop mixer LO (sum loop VCO output) enters the board via J3 and is passed through a 300 MHz low-pass filter before entering pin 8 of the mixer. The signal outputs from pins 3 and 4 of the mixer are passed through a 3 dB pad and a 40 MHz low-pass filter before leaving the board as the FM sum loop IF at J2. The output level of this 20 MHz IF signal is -16 dBm $\pm$3 dB.

Integrator Circuitry

Q1A and Q1B form a discrete differential amplifier within the integrator circuitry. One input to the amplifier is a frequency error signal (pin 8); the other is a phase error signal (pin 6). The signal at pin 8 should normally be at 0 volts when locked. At 0 volts, CR1 and CR2 are biased OFF and the base of Q1B is close to 0 volts. The phase error signal at pin 6 operates the differential amplifier to control the phase of the signal. The output voltage of the differential amplifier is amplified by Q7 and Q4 and is used to drive the voltage to current converter (Q3). The constant current source for the converter is formed by Q6.

The FM sum loop error current which flows through pin 3 of the board is the difference between the current flowing through Q6 and the

current flowing through Q3. The current flowing through Q3 is dependent on the voltage at the output of the integrator. The output of the integrator is controlled by feedback. When Q5 turn OFF, less current flows through Q3 for a given voltage at TP3. Q5 is turned ON and OFF by digital lines from the Microprocessor Board which enter the FM Sum Loop Mixer/Assembly via pins 9, 10, 19, and 20.

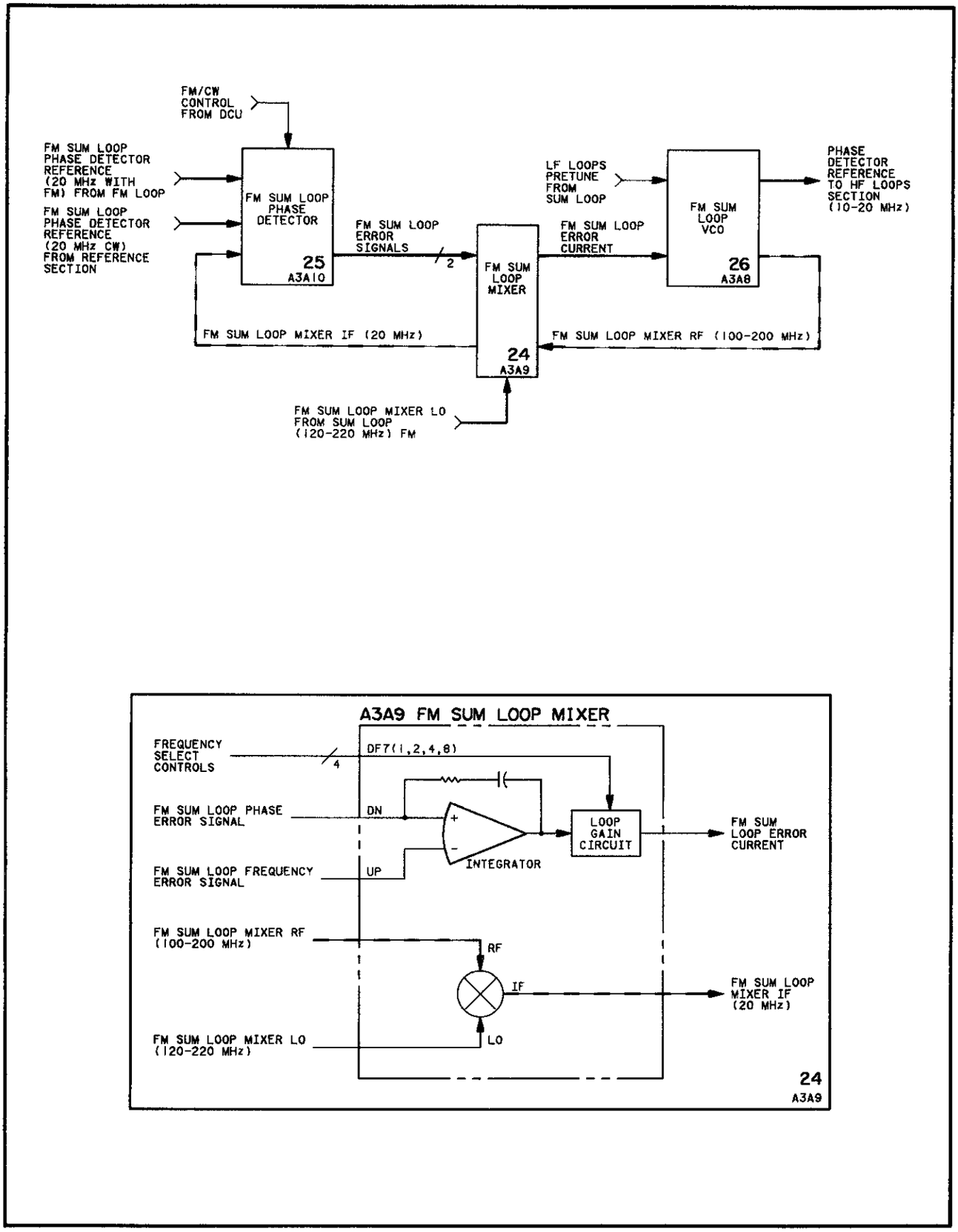


Figure 8-439. A3A9 FM Sum Loop Mixer Block Diagrams

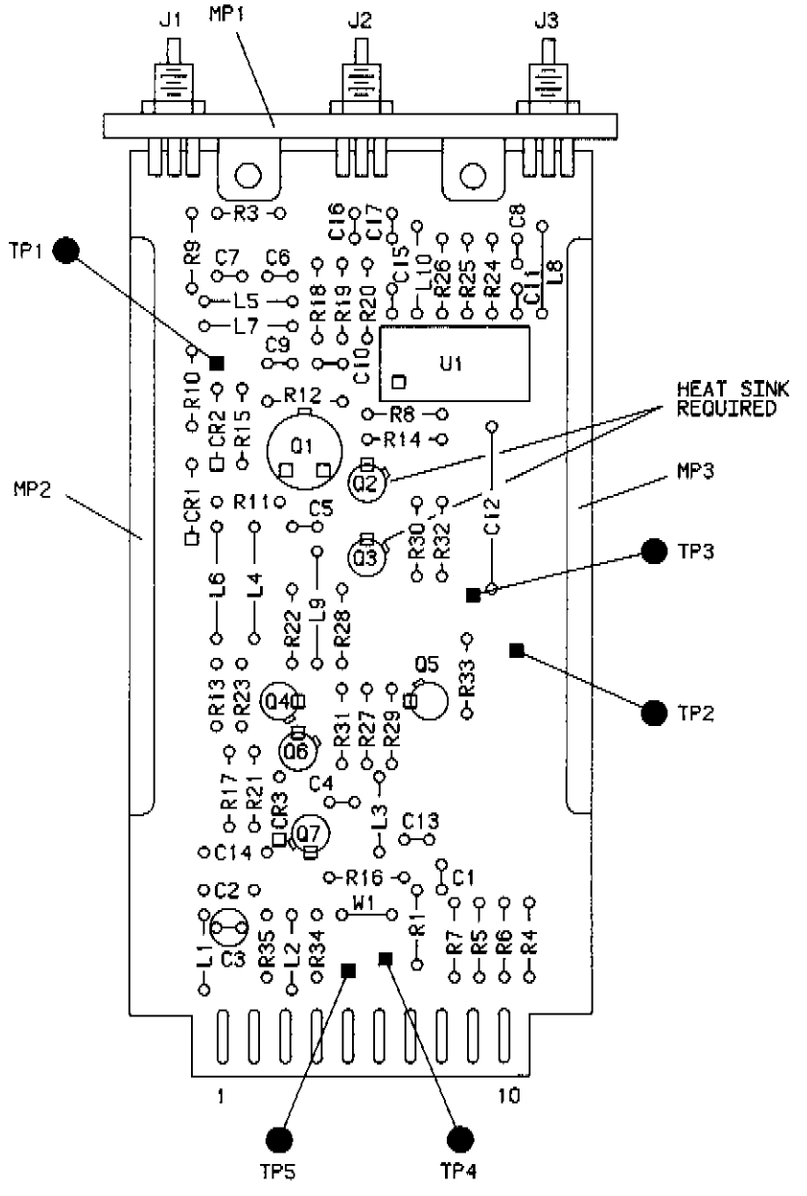


Figure 8-440. A3A9 FM Sum Loop Mixer Component Locator

CHANGES

2533A and Above

On the A3A9 schematic:

- A3A9R7, R9-R12 - Change the value of these resistors to those shown below:

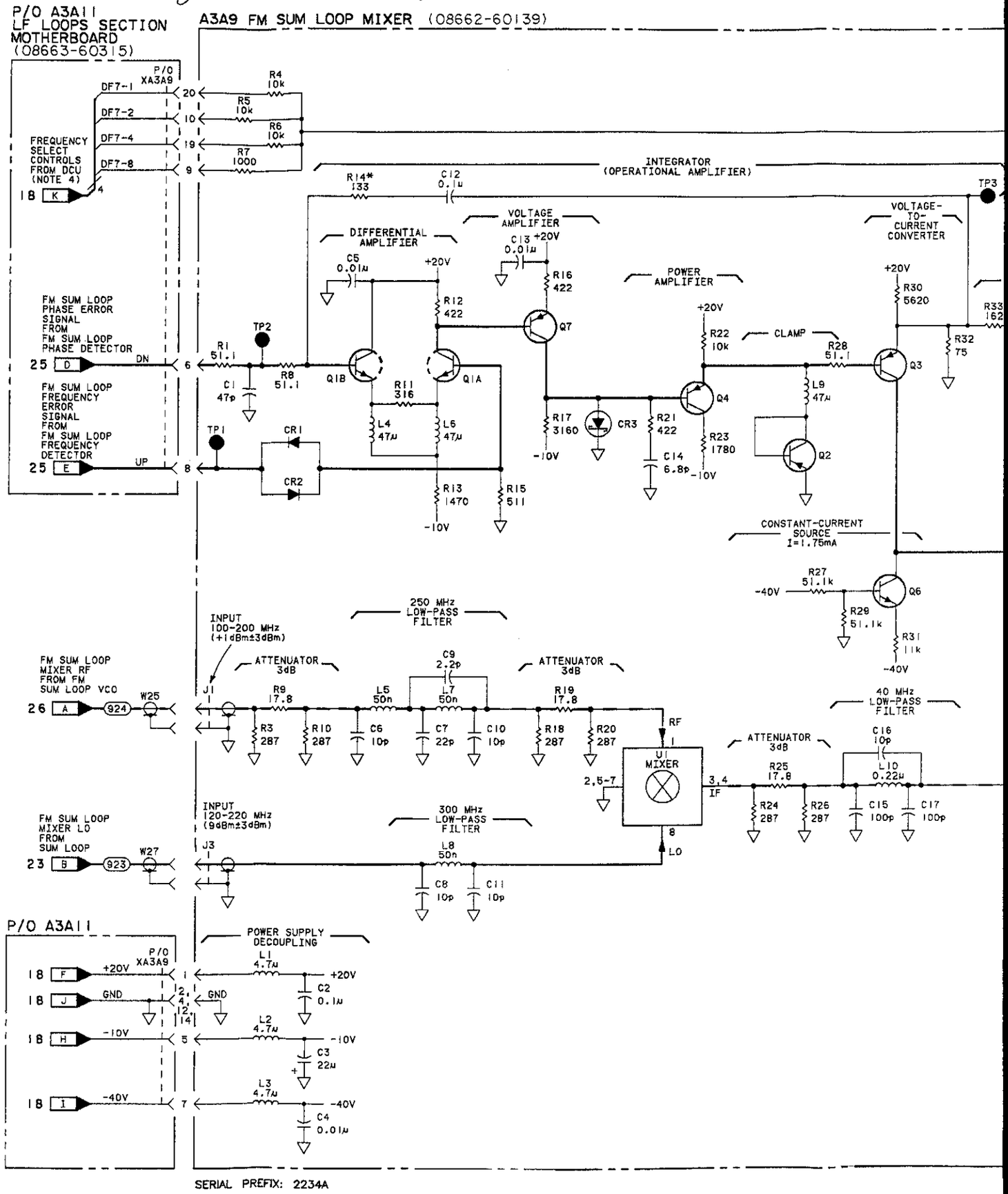
R7	2.87k
R9	1k
R10	7.5k
R11	28.7k
R12	196k

2601A and Above

On the schematic:

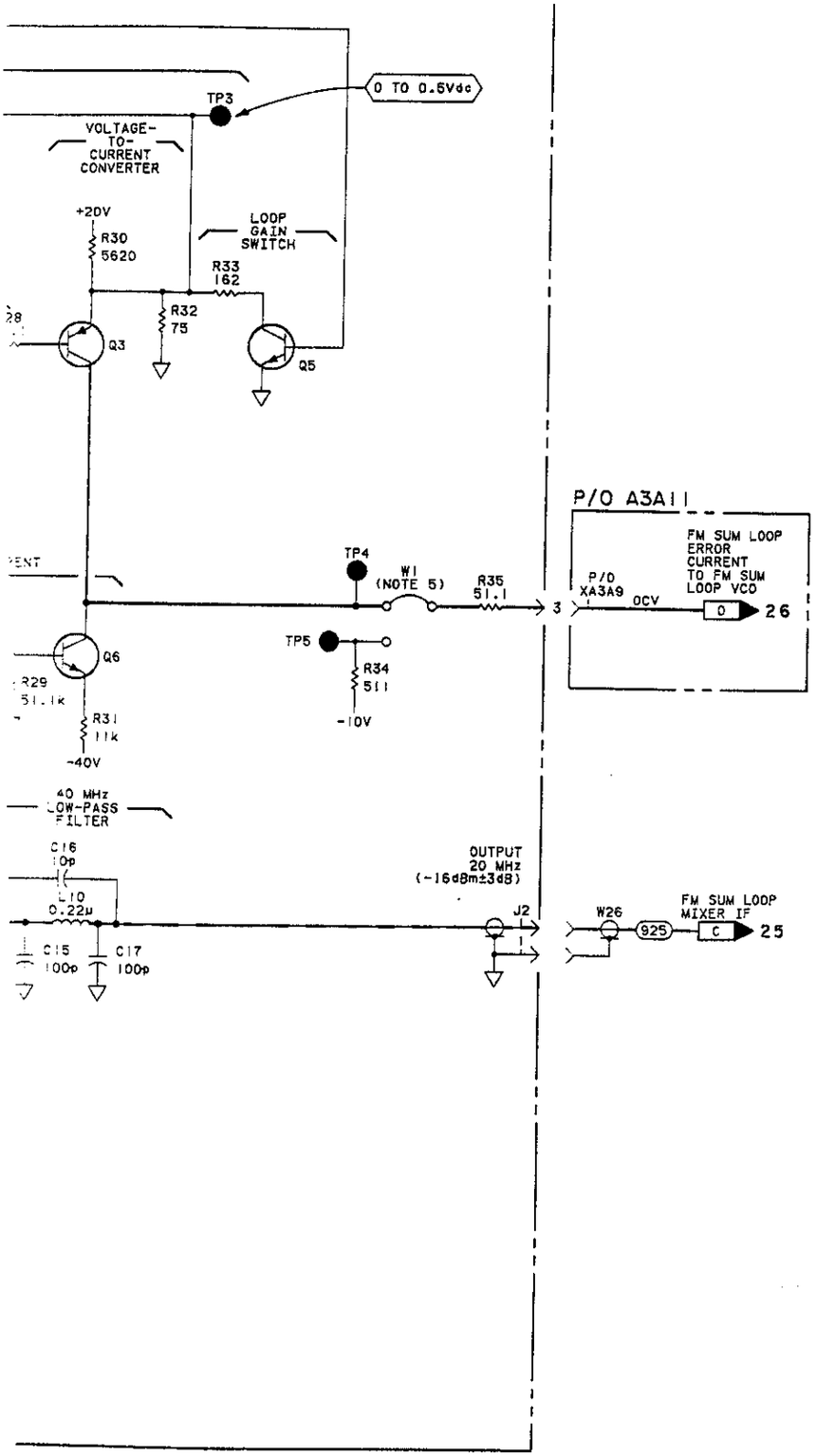
- A3A9Q1 - In the Table of Transistor and Integrated Circuit Part Numbers, change the part number of Q1 to 1854-1046.

Fig 8-441 Sht 1 of 2



SERIAL PREFIX: 2234A

Fig 8-441
Sht 2 of 2



NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. ASTERISK (*) INDICATES THAT THESE PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL ONLY. REFER TO SECTION Ⅸ FOR PROCEDURE.
4. MNEMONICS DF7-1 TO DF7-8 REPRESENTS THE FREQUENCY DIGITS ON THE FRONT PANEL AND THE BCD WEIGHTING.
5. JUMPER W1 AT TP4 IS CONNECTED TO TP5 FOR TROUBLESHOOTING PURPOSES ONLY.

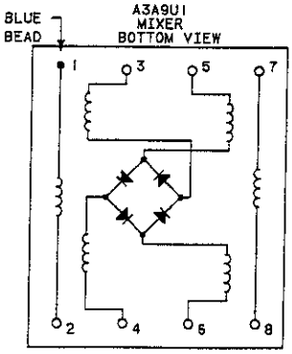
REFERENCE DESIGNATIONS

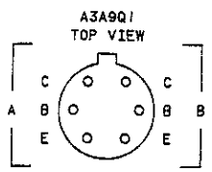
NO PREFIX	A3A11
W25-27	XA3A9
A3A9	
C1-17 CR1-3 J1-3 L1-10 Q1-7 R1,3-35 TP1-5 U1 W1	

NOT ASSIGNED: A3A9R2

TRANSISTOR PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1	1854-0475
Q2-4,7	1853-0451
Q5,6	1854-0404
U1	0955-0096





SERVICE SHEET 24
A3A9

Figure 8-441. A3A9 FM Sum Loop Mixer Schematic

SERVICE SHEET 25
A3A10 FM SUM LOOP PHASE DETECTOR

REFERENCE BLOCK DIAGRAM 5
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

General

It is on the FM Sum Loop Phase Detector Board that either the 20 MHz continuous wave (CW) signal from the reference section or the 20 MHz FM signal (generated within the modulation section) is summed with the 120 MHz to 220 MHz (1 Hz step resolution) Low Frequency Sum Loop signal. The net result is a 100 MHz to 200 MHz CW or FM signal at the output of the FM Sum Loop VCO (service sheet 26). This signal is divided by the decade divider on the same board to produce the 10 MHz to 20 MHz (0.1 Hz step resolution) reference signal that is used by the Output Sum Loop Phase Detector in the high frequency loops section.

Inputs to the Phase Detector Board include the FM sum loop CW and FM phase detector reference signals (pins 10 and 8), the FM sum loop IF from the Sum Loop Mixer at J1 and the FM/CW control at pin 15. Outputs include the FM sum loop phase error signal (pin 14) and the FM sum loop frequency error signal (pin 12).

Phase Detector Circuitry

The FM sum loop IF signal passes through a 20 MHz low-pass filter and through 60 MHz and 100 MHz notch filters before being amplified by the 20 MHz bandpass amplifier formed by Q1. The notch filters eliminate spurious signals from the FM Sum Loop Mixer Board. Following the bandpass amplifier, the signal passes through a 3 dB pad before splitting in two directions. One path is through Q2, which toggles one flip-flop of the frequency detector formed by U1. The other path is to the RF input of phase detector U2 (the LO input will be discussed subsequently). The output of the phase detector passes through R30 and a 20 MHz low-pass filter before leaving the board to be sent as an error signal to the integrator on the FM Sum Loop Mixer Board (service sheet 24).

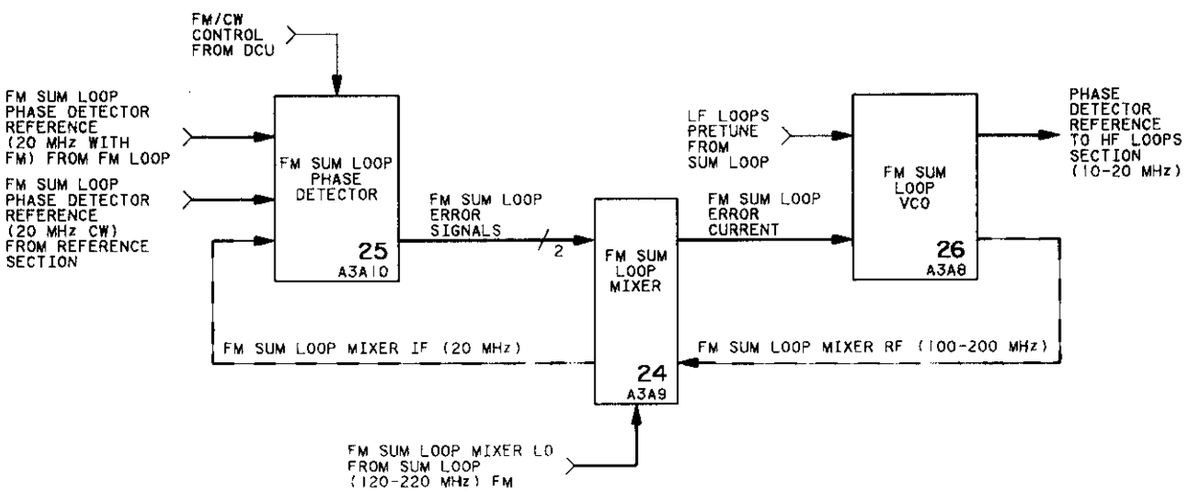
FM/CW Selector Circuitry

Selection of either the FM or CW sum loop phase detector reference signals is handled by the FM/CW selector circuitry formed by U4. This selector is controlled by the FM/CW control line which enters the board via pin 15. The outputs of the selector are at pins 6 and 3. These two outputs are wire ORed and the resulting signal is sent

to the LO input of phase detector U2 and the second toggle input (pin 6) of frequency detector U1.

Frequency Detector Circuitry

The frequency detector outputs a pulse whenever the FM sum loop IF frequency differs from either the FM or CW sum loop phase detector reference signals (whichever happens to selected). The output from the frequency detector is sent to comparators U3A and U3B. The square wave outputs of the comparators are sent to an inverter circuit that sums the currents to produce a voltage at the junction of R39 and R42. This voltage outputs as the FM sum loop frequency error signal at pin 12. When the system is in lock, the output at this point is about $\pm$0.5 volts. Q5 is used as an OR gate for the outputs of the two comparators. Whenever either of the comparators goes HI, Q5 turns on and lights the out-of-lock LED indicator.



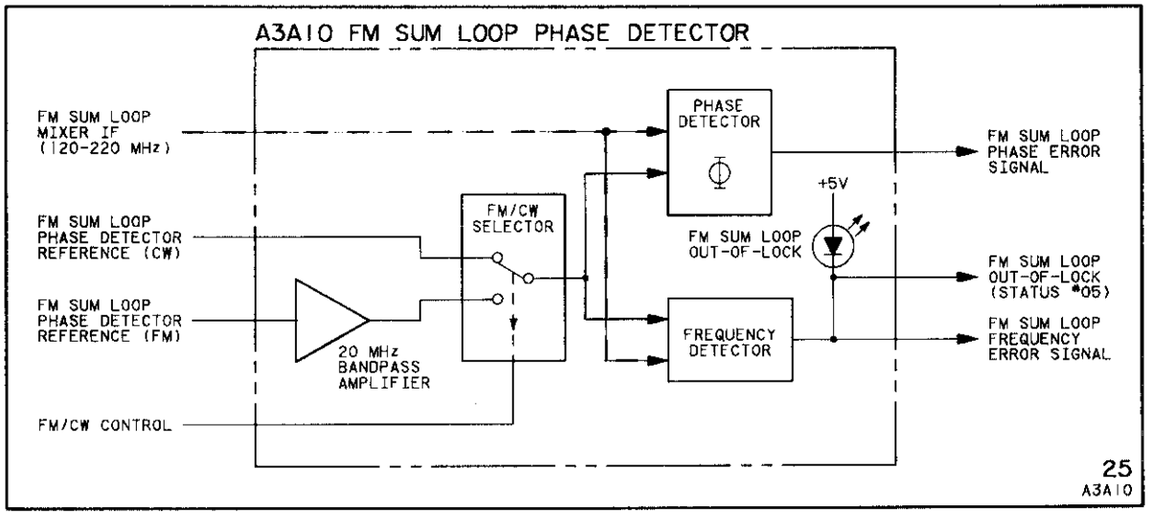


Figure 8-442. A3A10 FM Sum Loop Phase Detector Block Diagrams

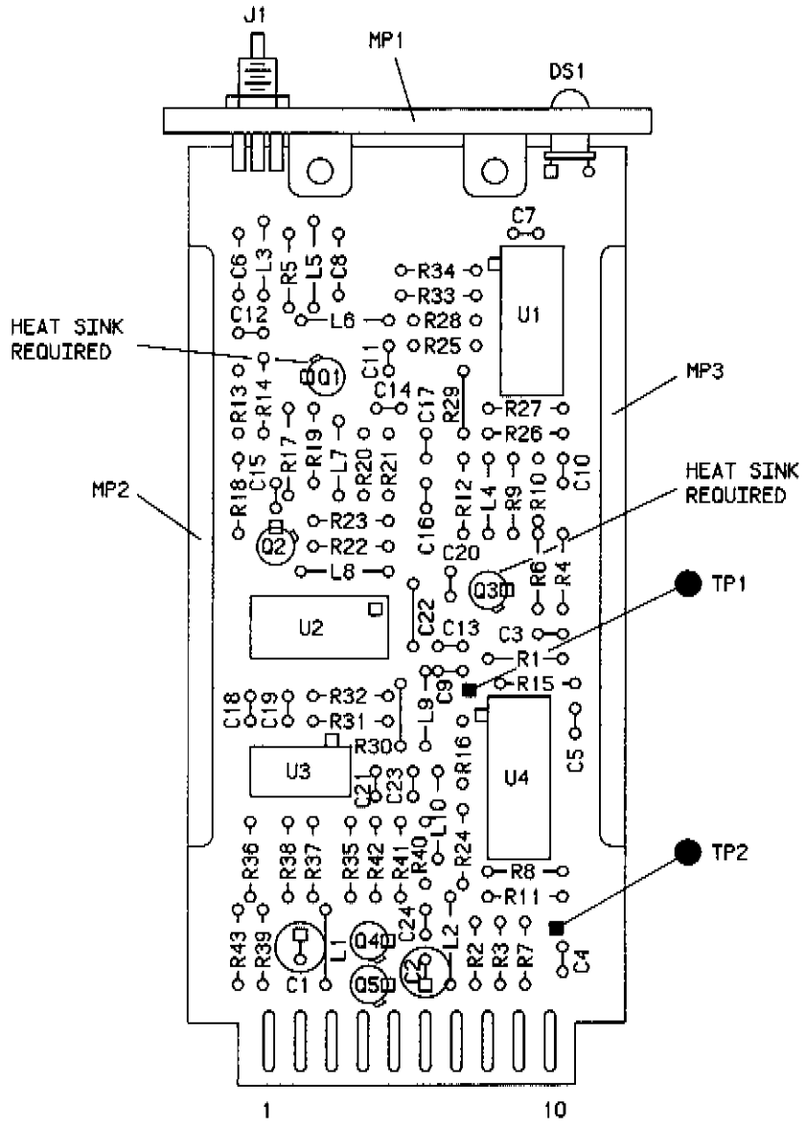


Figure 8-443. A3A10 FM Sum Loop Phase Detector Component Locator

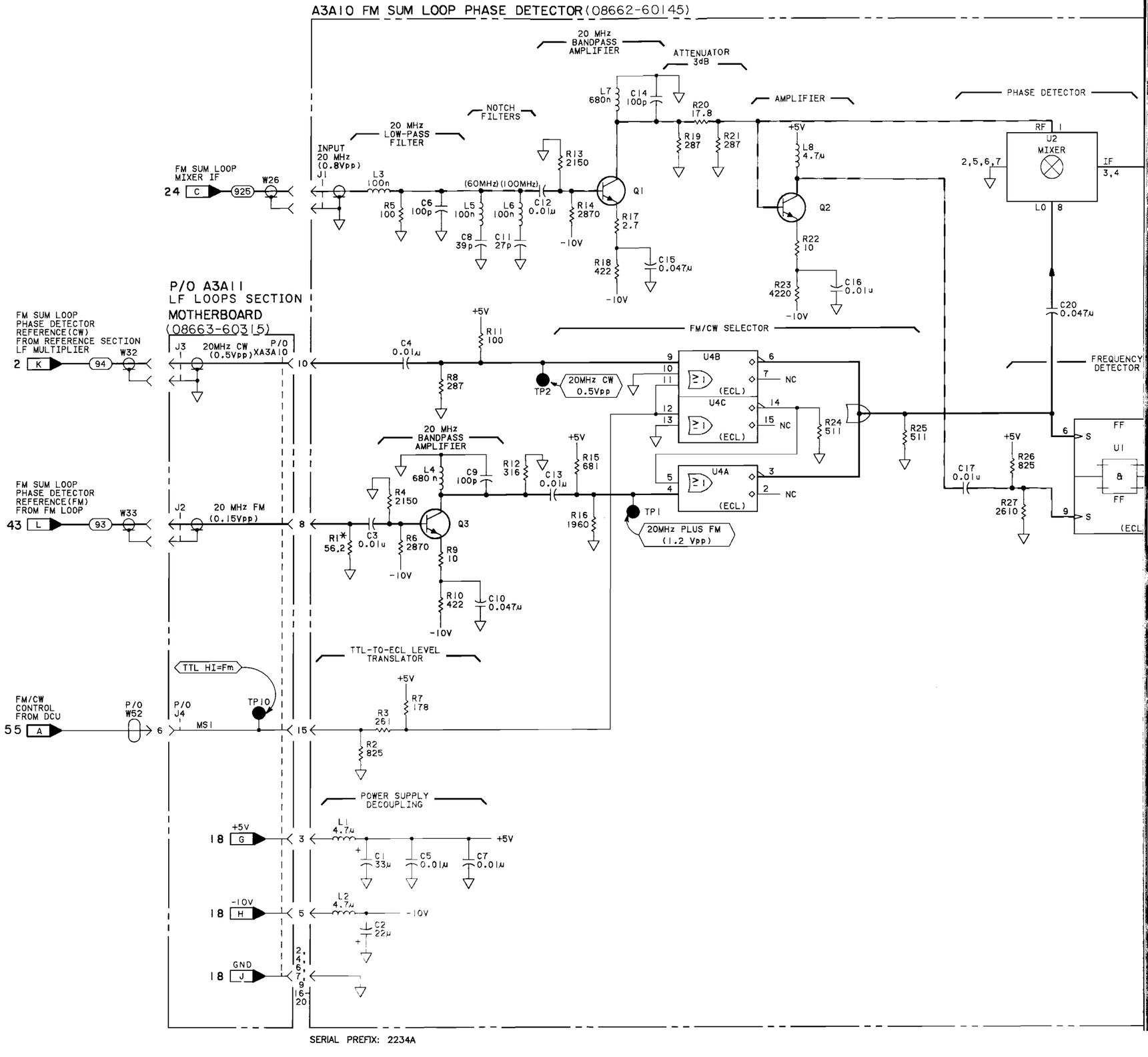
CHANGES

All serial prefixes

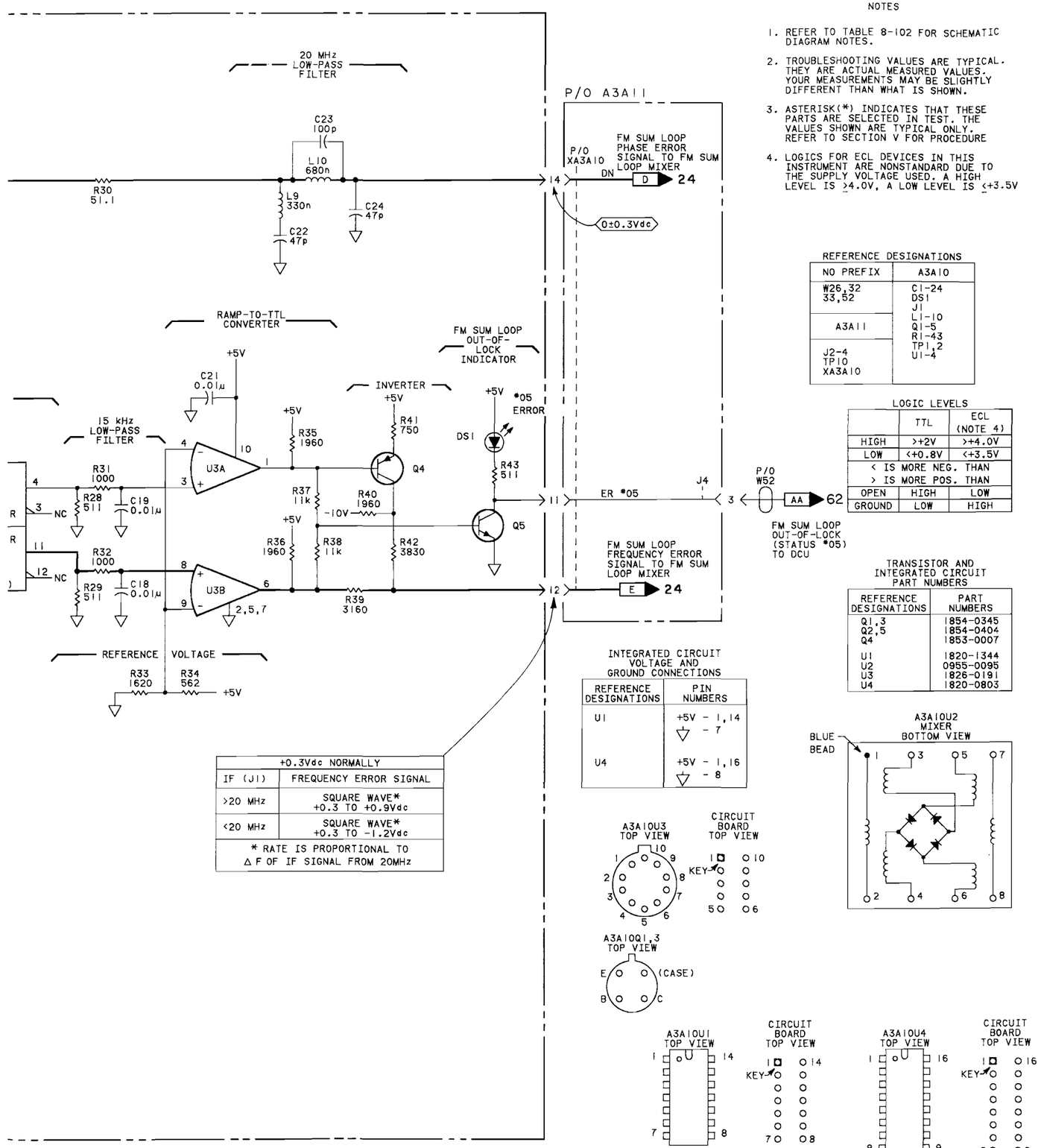
On the A3A5 schematic:

- A3A10C9 – Change the value of C9 to 110p.

A3A10 FM SUM LOOP PHASE DETECTOR (08662-60145)



SERIAL PREFIX: 2234A



NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. ASTERISK(*) INDICATES THAT THESE PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL ONLY. REFER TO SECTION V FOR PROCEDURE
4. LOGICS FOR ECL DEVICES IN THIS INSTRUMENT ARE NONSTANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS ≥4.0V, A LOW LEVEL IS ≤+3.5V

REFERENCE DESIGNATIONS

NO PREFIX	A3A10
W26,32 33,52	C1-24 DS1 J1 L1-10 Q1-5 R1-43 TP1,2 U1-4
A3A11	
J2-4 TP10 XA3A10	

LOGIC LEVELS

	TTL	ECL (NOTE 4)
HIGH	>+2V	>+4.0V
LOW	<+0.8V	<+3.5V
< IS MORE NEG. THAN		
> IS MORE POS. THAN		
OPEN	HIGH	LOW
GROUND	LOW	HIGH

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,3	1854-0345
Q2,5	1854-0404
Q4	1853-0007
U1	1820-1344
U2	0955-0095
U3	1826-0191
U4	1820-0803

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V - 1,14 ▽ - 7
U4	+5V - 1,16 ▽ - 8

+0.3Vdc NORMALLY	
IF (J1)	FREQUENCY ERROR SIGNAL
>20 MHz	SQUARE WAVE* +0.3 TO +0.9Vdc
<20 MHz	SQUARE WAVE* +0.3 TO −1.2Vdc
* RATE IS PROPORTIONAL TO Δ F OF IF SIGNAL FROM 20MHz	

A3A10U2 MIXER BOTTOM VIEW

A3A10U3 TOP VIEW

CIRCUIT BOARD TOP VIEW

A3A10Q1,3 TOP VIEW

A3A10U1 TOP VIEW

CIRCUIT BOARD TOP VIEW

A3A10U4 TOP VIEW

CIRCUIT BOARD TOP VIEW

SERVICE SHEET 25
A3A10

Figure 8-444. A3A10 FM Sum Loop Phase Detector Schematic

SERVICE SHEET 26
A3A8 FM SUM LOOP VCO

REFERENCE BLOCK DIAGRAM 5
Table 4-1. Recommended Performance Tests After Adjustments or Repairs.
Table 5-2. Post-Repair Adjustment Procedures.

PRINCIPLES OF OPERATION

General

The FM Sum Loop VCO utilizes back-to-back varactors instead of bypass capacitors used on the other two VCO assemblies. This allows greater bandwidth and higher frequency modulation of the oscillator.

There are two inputs to the Sum Loop VCO Board. One is a pretune from the Sum Loop Phase Detector Board which enters the FM Sum Loop Board via pin 10. This input is fed through a linearizer circuit and is then buffered by Q3 and Q4. The resulting voltage at TP3 is used to pretune the voltage controlled oscillator within lock range. The FM sum loop error current enters the board via pin 9 and passes through a 40 MHz low-pass filter, formed by L7 and C8, before being summed with the loop pretune signal. This signal provides fine tuning to the VCO and guides it to final lock.

Signal splitter T1 (in the output section of this board) divides the power of the signal tapped at L12 and distributes it to limiters U2 and U1. Limiter U2 has two outputs. One of them is a test output with a frequency range of 100 MHz to 200 MHz. The other output is passed through a divide-by-ten circuit to provide the 10 MHz to 20 MHz phase detector reference (0.1 Hz step resolution) signal needed by the Output Sum Loop in the high frequency loops section. The output of limiter U1 passes through a 300 MHz low-pass filter and outputs from the board to the FM Sum Loop Mixer (service sheet 24), providing feedback for the FM Sum Loop.

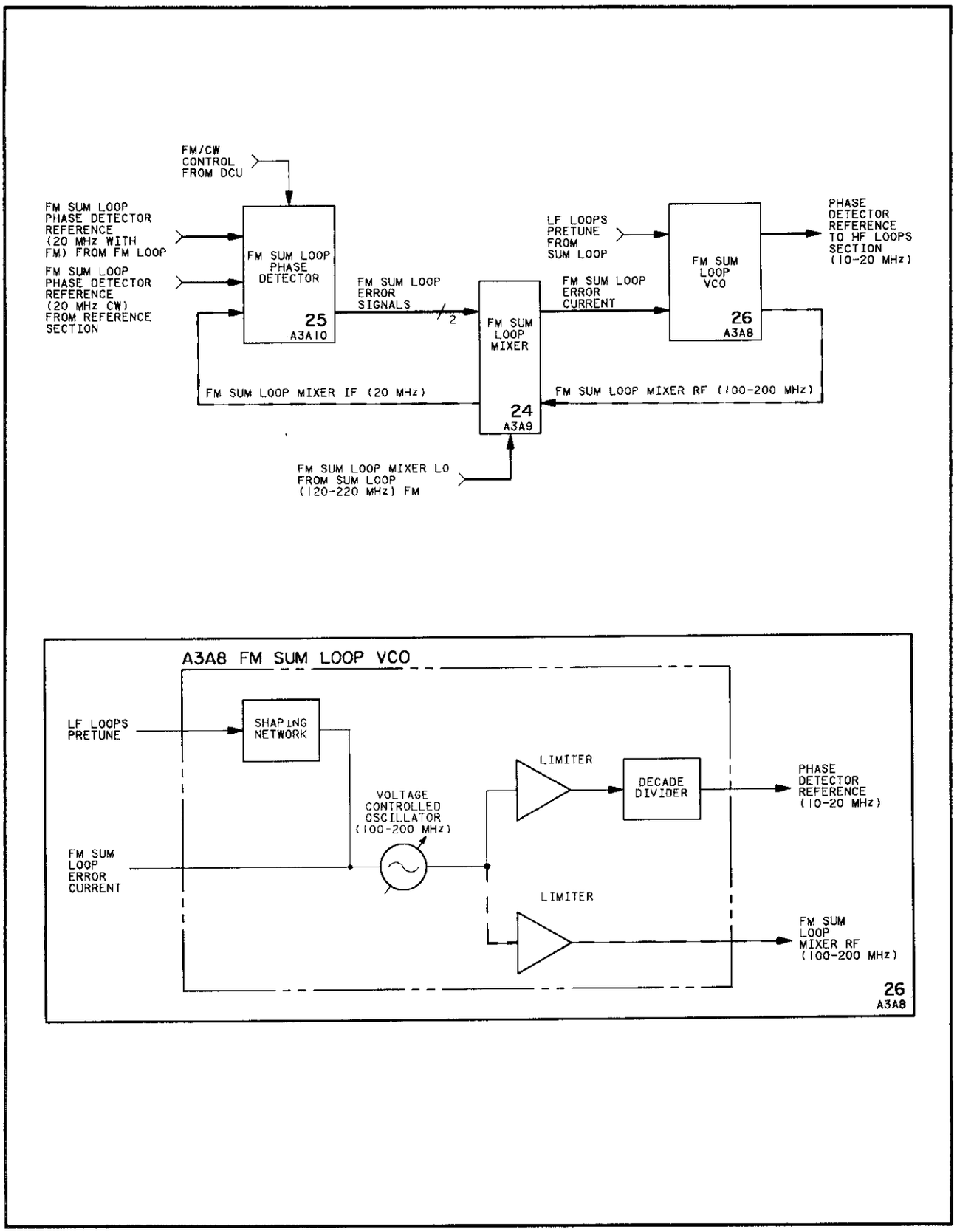


Figure 8-445. A3A8 FM Sum Loop Voltage Controlled Oscillator Block Diagrams

CHANGES

2533A and Above

On the A3A8 schematic:

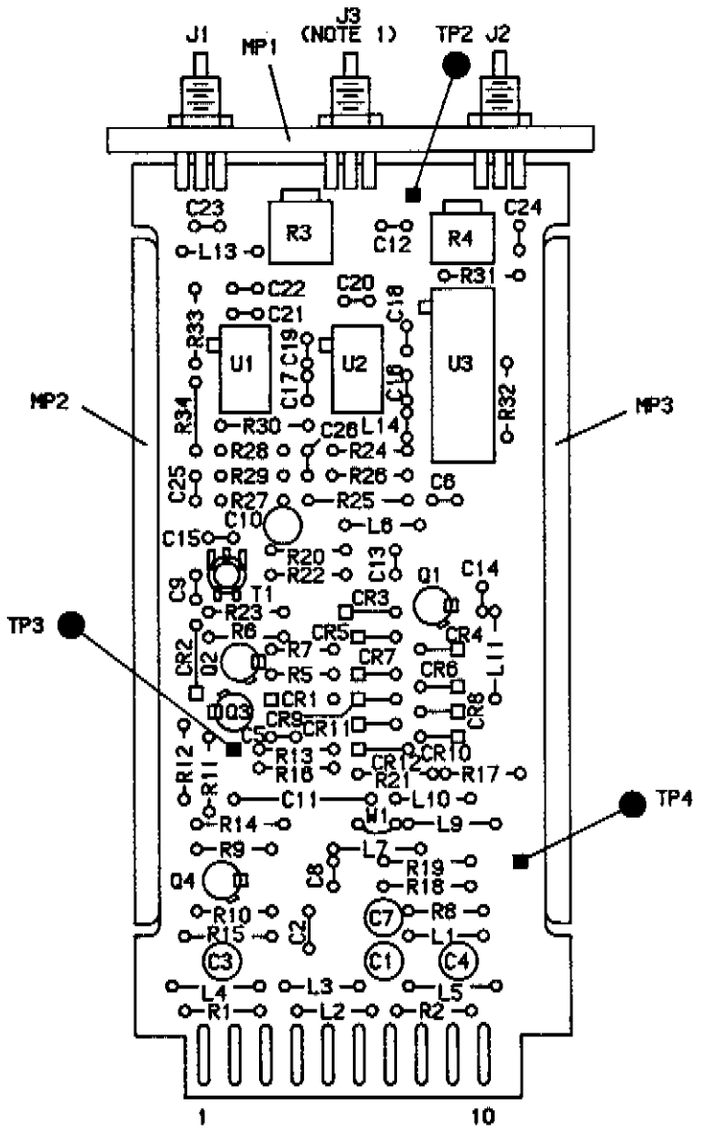
- A3A8R4-6, R14, R32, R33- Change the value of these resistors to those shown below:

R4	5.11k
R5	3.48k
R6	1k
R14	147 ohms
R32	90.9 ohms
R33	75 ohms

2748A and Above

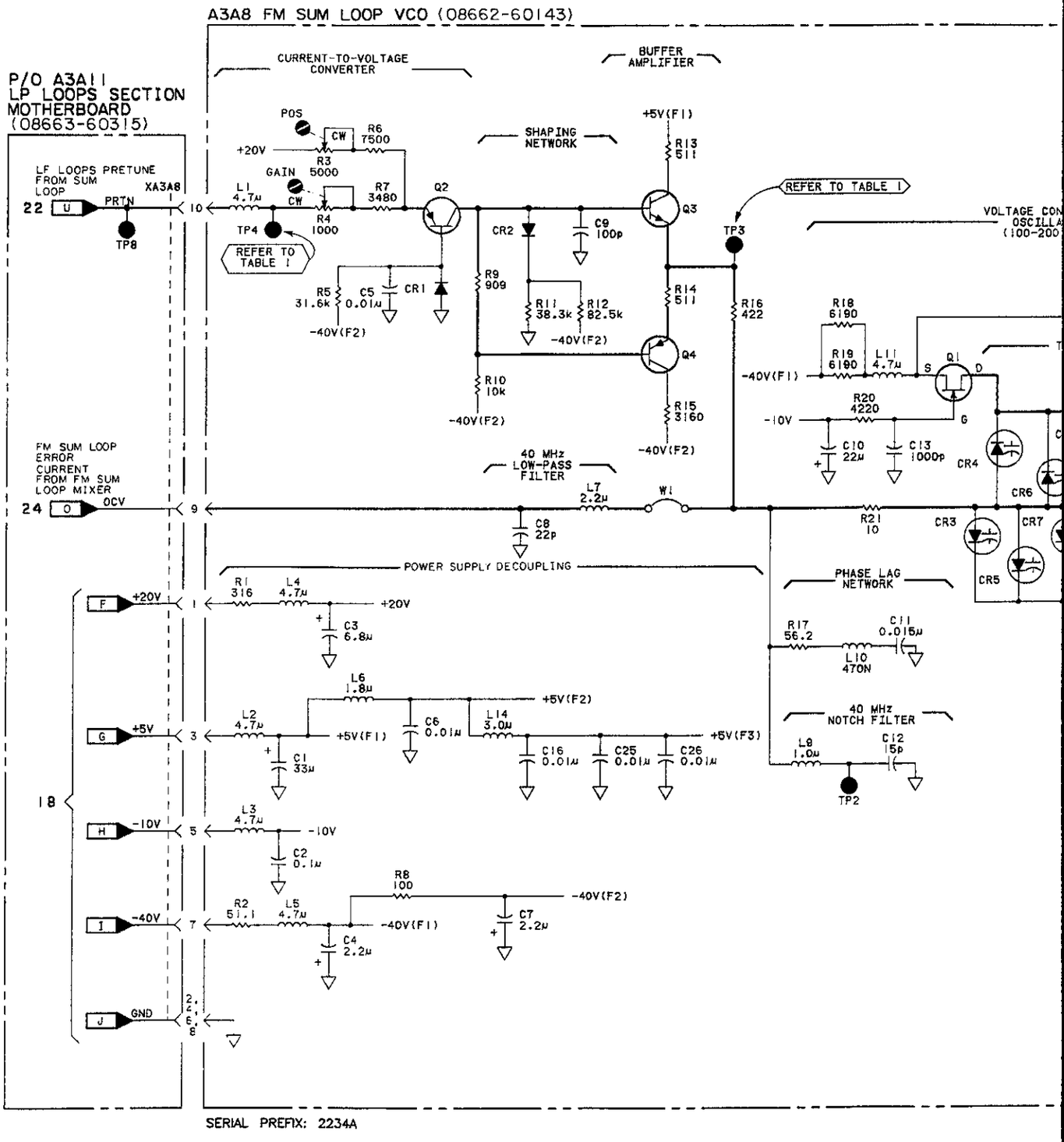
On the A3A8 schematic:

- A3A8R6, R12 - Under **CURRENT-TO-VOLTAGE CONVERTER** locate R6 and change its value to 6.8k ohms. Under **SHAPING NETWORK** locate R12 and change its value to 261 ohms.



8-446. A3A8 FM Sum Loop Voltage Controlled Oscillator Component Locator.

Fig 8-447
Sht 1 of 3



SERIAL PREFIX: 2234A

Fig 8-447
Sht 2 of 3

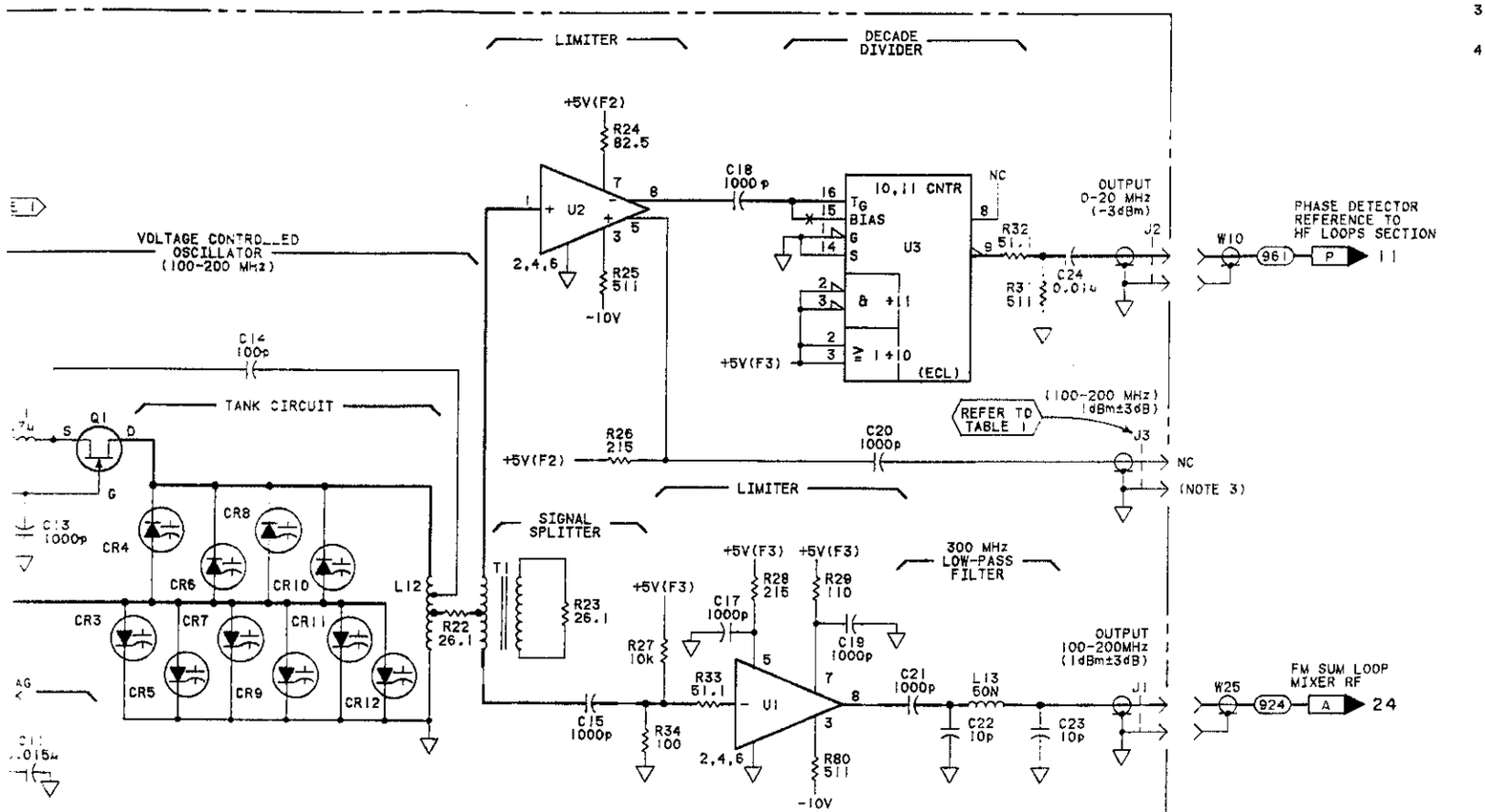


TABLE 1. TUNE VOLTAGE CHECK

FRONT PANEL FREQUENCY SETTING	TP3 (Vdc)	TP4 (Vdc)	TP1 (J3) NOTE 3 (MHz)
320.0	-1.45	+7.03	100.0
320.1	-1.56	+6.97	101.0
320.2	-1.66	+6.91	102.0
320.4	-1.90	+6.78	104.0
320.8	-2.33	+6.54	108.0
321.0	-2.52	+6.44	110.0
322.0	-3.68	+5.84	120.0
324.0	-5.98	+4.66	140.0
328.0	-10.5	+2.37	180.0
329.9	-12.9	+1.22	199.0

Fig 8-447 Sht 3 of 3

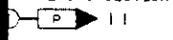
NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. RF CONNECTOR J3 IS USED AS TP1 FOR TROUBLESHOOTING PURPOSES ONLY.
4. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NON-STANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS ±4.0V, A LOW LEVEL IS ≤±3.5V.

REFERENCE DESIGNATIONS

NO PREFIX	A3A11
W10,25	XA3A8
A3A8	TP8
C1-26 CR1-12 J1-3 L1-7,9-14 Q1-4 R1-34 T1 TP2-4 U1-3 W1	

PHASE DETECTOR REFERENCE TO HF LOOPS SECTION



LOGIC LEVELS

	TTL	ECL (NOTE 4)
HIGH	>+2V	>+4.0V
LOW	<+0.8V	<+3.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	LOW
GROUND	LOW	HIGH

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

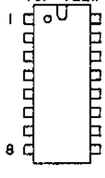
REFERENCE DESIGNATIONS	PART NUMBERS
Q1	1855-0235
Q2,4	1853-0451
Q3	1854-0404
U1,2	1826-0372
U3	1820-1780

FM SUM LOOP MIXER RF

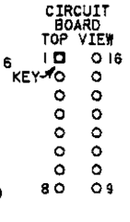
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U3	+5V(F3)-4,5 -10,12,13 NC -6,7,11

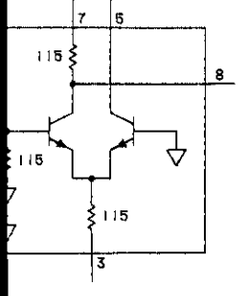
A3A8U3 TOP VIEW



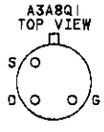
CIRCUIT BOARD TOP VIEW



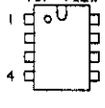
A3A8U1,U2



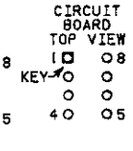
A3A8Q1 TOP VIEW



A3A8U1,2 TOP VIEW



CIRCUIT BOARD TOP VIEW



SERVICE SHEET 26

A3A8

Figure 8-447. A3A8 FM Sum Loop Voltage Controlled Oscillator Schematic

CHANGES

All serial prefixes	**On the A3A8 schematic:** • **SS26** - On service sheet 26 delete the page number and add a revsion date in its place of *rev.20DEC88*.
2533A and above	**On the A3A8 schematic:** • **R4-6, R14, R32, R33** - Change the value of these resistor to those shown below: R4 5.11K R5 3.48K R6 1K R14 147 ohm R32 90.9 ohm R33 75 ohm
2706A and above	**On the A3A8 schematic:** • **R6 - R12** - Under CURRENT-TO-VOLTAGE CONVERTER locate R6 and change its value to 6.8K ohm. Under SHAPING NETWORK locate R12 and change its value to 261 ohm.
2846A and above	**On the A3A8 schematic:** • **R31** - In the upper right corner of the schematic change the value of R31 to 1K ohm.

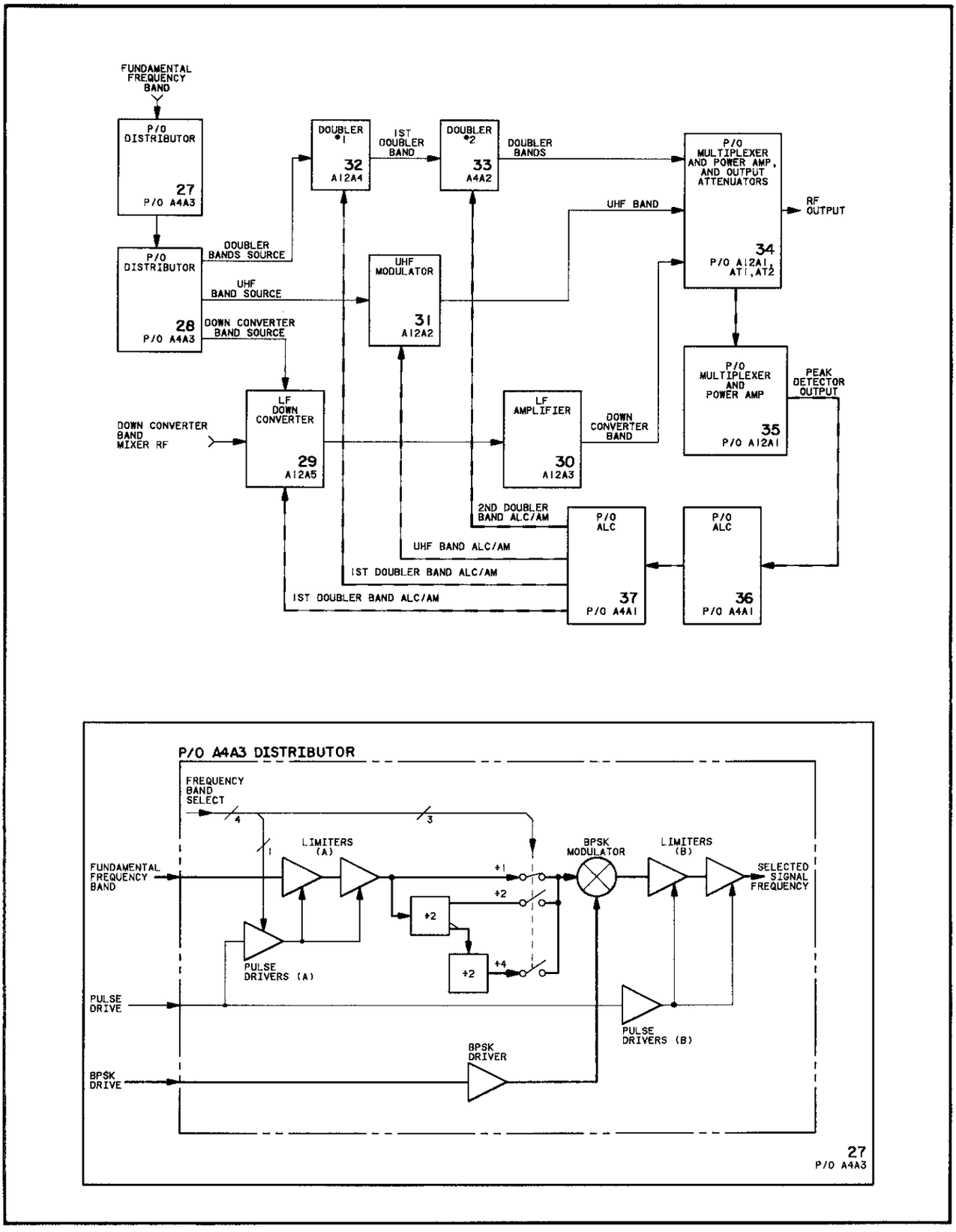


Figure 8-501. P/O A4A3 Distributor Block Diagrams

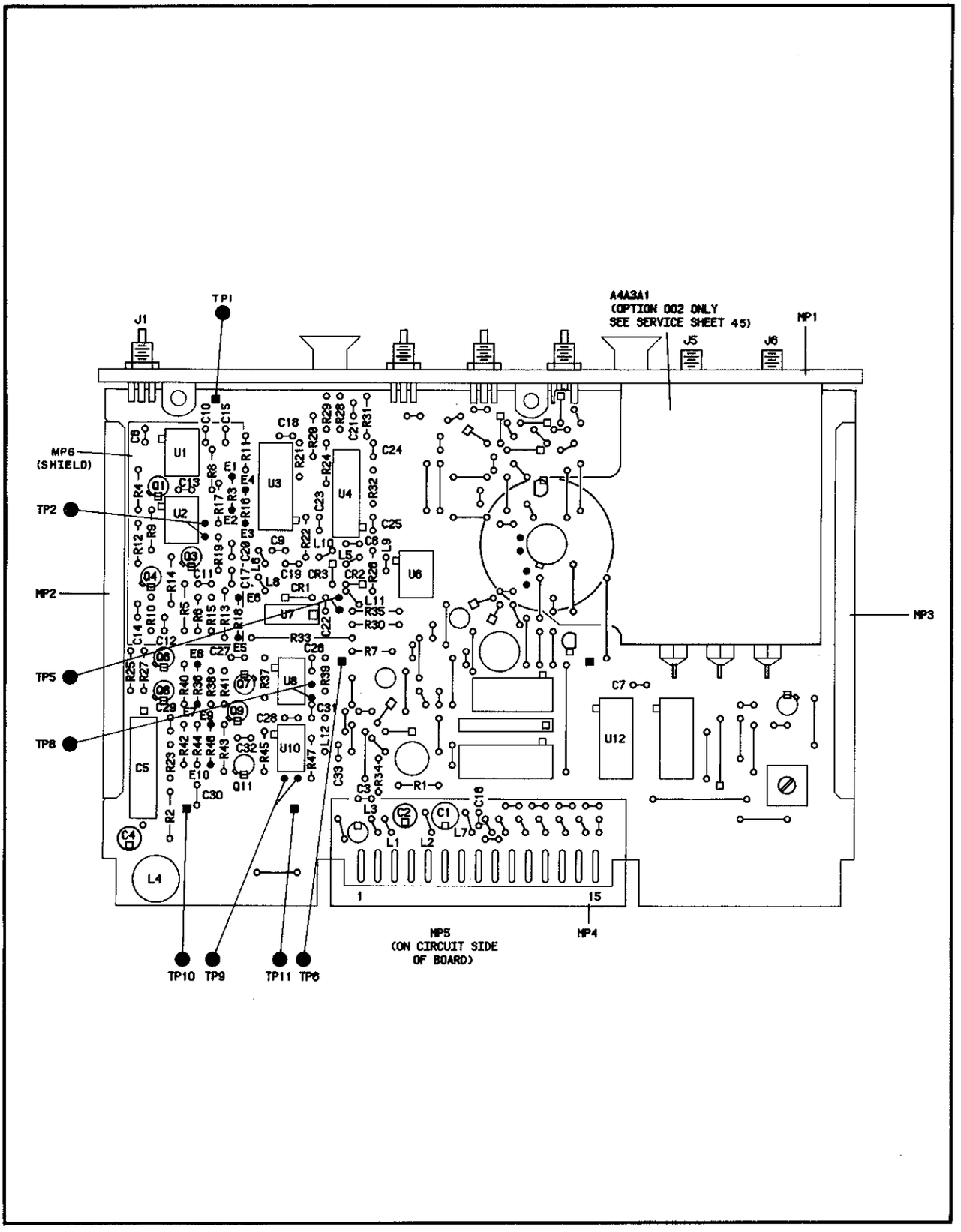


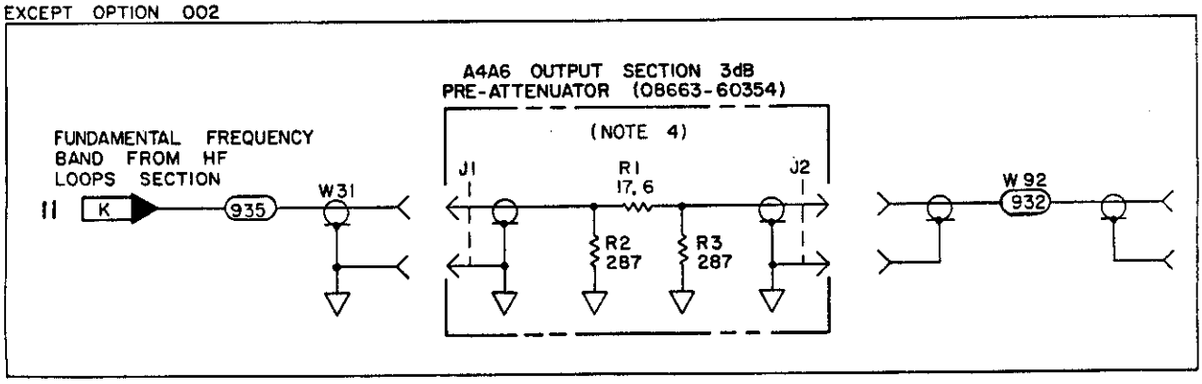
Figure 8-502. P/O A4A3 Distributor Component Locator

CHANGES

All Serial Prefixes	**On the schematic:** • **+5V Bullet "C"** - On the left side of the A4A3 schematic, change the service sheet reference for the bullet labeled "C" to 65. **On the A4A3 schematic:** • **A4A3R2** - Change the value of R2 to 3.83 ohms. • **A4A3C24** - The symbol shown for C24 (470p) is a resistor. Change the symbol to a capacitor symbol. • **A4A3L11** - On the upper right-hand side of the schematic, change the symbol for L11 to an inductor.
2245A and above	**On the schematic:** • **A4A6** - On the left side of the schematic, add A4A6 as shown in the figure "P/O Figure 8–503. P/O Distributor Schematic (2245A and above)" on page 8–502.3. • **NOTES** - On the right side of the schematic under NOTES, add note 4 as follows: 4. The small chip components of this assembly require low-temperature soldering techniques. Use silver solder.
2350A and above	**On the A4A3 schematic:** • **W2** - Modify the schematic as shown in the partial schematic, "P/O Figure 8-502. P/O Distributor Schematic (2350A and above)," on page 8–502.4. • **NOTES** - On the right side of the schematic under NOTES, add note 5 as follows: 5. W2 is a quarter wavelength open-circuit coaxial stub used to attenuate a 4 MHz spur. **On the A4A3 component locator:** • **W2** - Use the component locator "P/O Figure 8-502. P/O A4A3 Distributor Component Locator (2350A and above)," on page 8–502.3.

CHANGES

2401A and above	**On the A4A3 schematic:** • **A4A3C65** - Add capacitor C65 (100p) from the node of R34 and L10 to ground. **On the A4A3 component locator:** • **A4A3C65** - Add capacitor C65 between U4 and L10. (Use component locator on page 8–502.3.)
2451A and above	**On the A4A3 schematic:** • **A4A3** - Change the part number of the A4A3 Assembly to 08663-60362 (standard) and 08663-60361 (option 002) • **A4A3** - Modify the schematic as shown in the partial schematic, "P/O Figure 8–503. P/O Distributor Schematic (2451A and above)," on page 8-502.5. • **W2, NOTES** - W2 and NOTE 5 were added on serial break 2350A. W2 is no longer used; in its place is an open circuit stub (printed circuit trace). Change NOTE 5 to read: 5. A quarter wavelength open-circuit coaxial stub is used to attenuate a 4 MHz spur. The stub is a printed circuit trace. • **A4A3C65** - Change the value of C65 to 10p. • **A4A3L10** - Change the value of L10 to 120μ. **On the A4A3 component locator:** • **A4A3** - Modify the component locator as shown in the partial component locator, "P/O Figure 8–502. P/O A4A3 Distributor Component Locator (2451A and above)," on page 8-502.5.



P/O Figure 8-503. P/O Distributor Schematic (2245A and above)

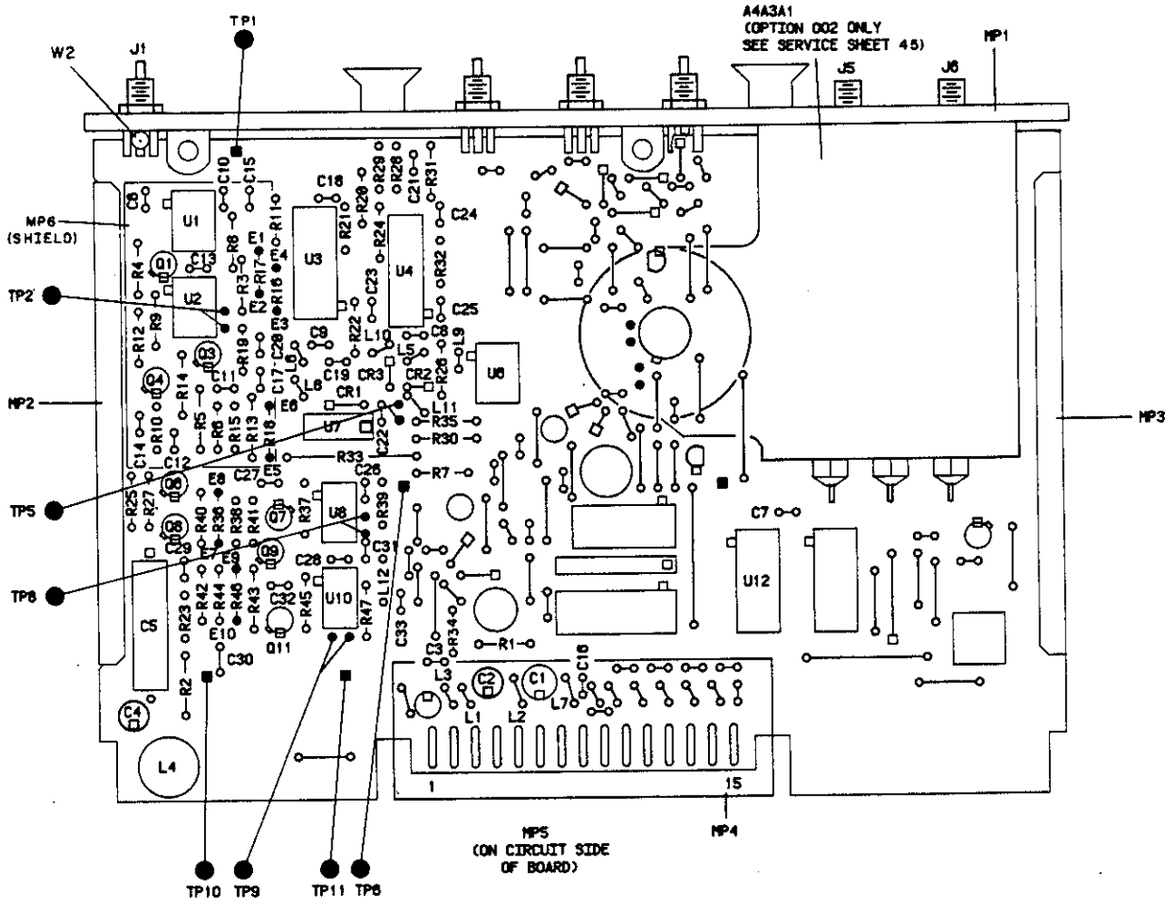


Figure 8-502. P/O A4A3 Distributor Component Locator (2350A and above)

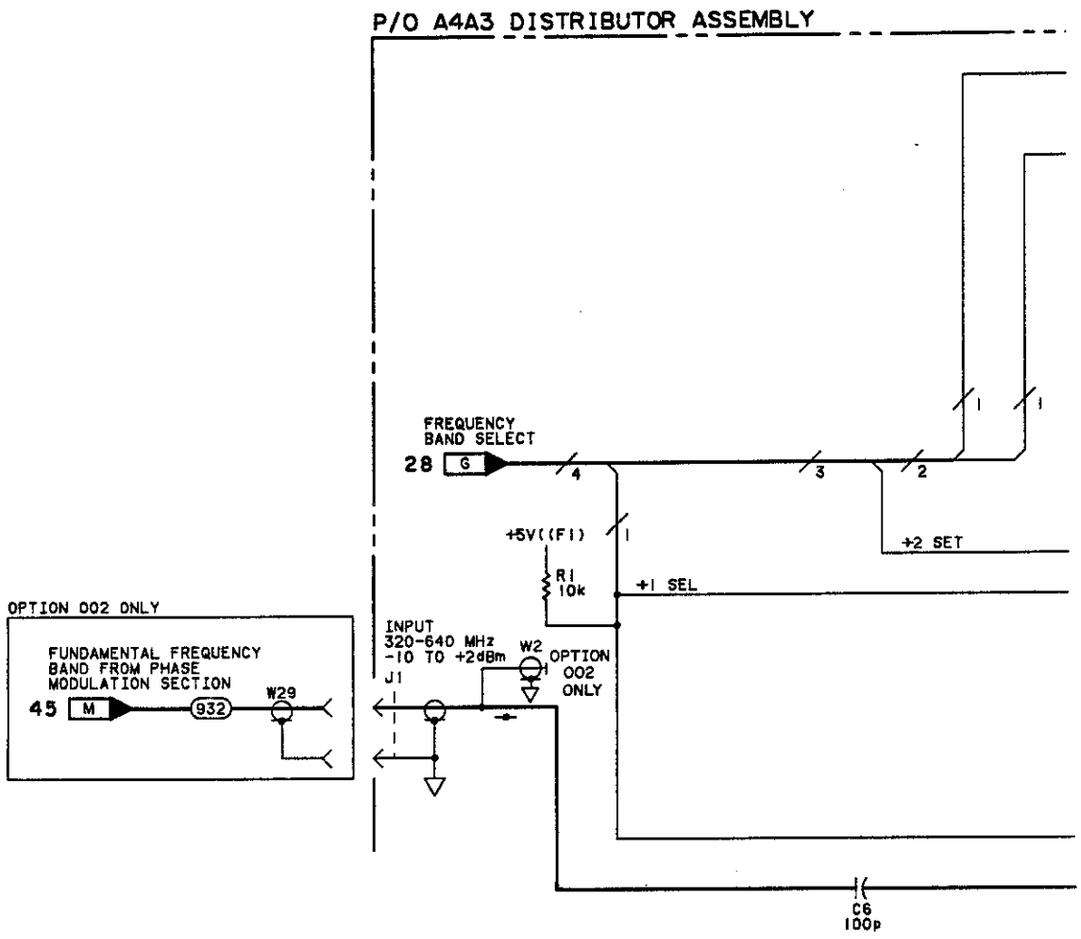


Figure 8-503. P/O Distributor Schematic (2350A and above)

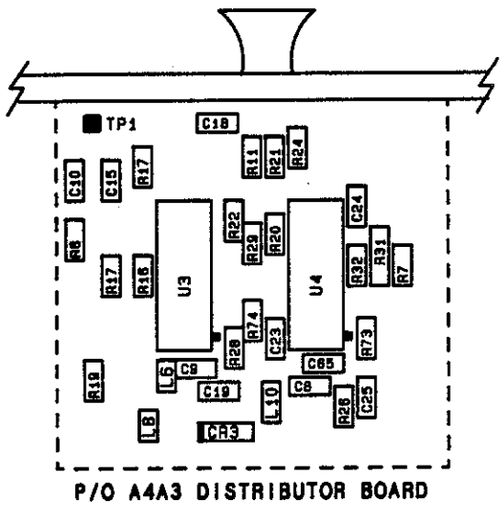
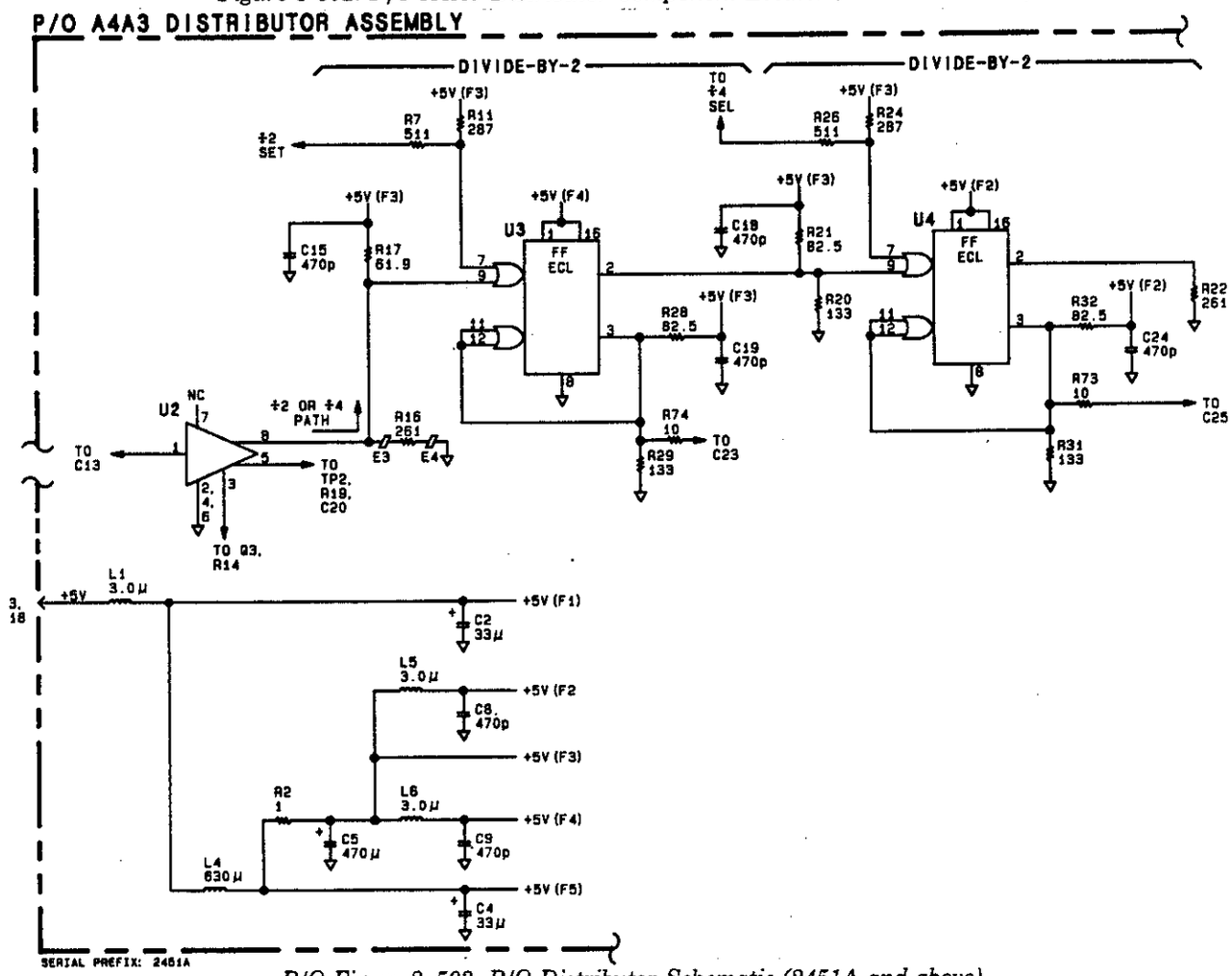
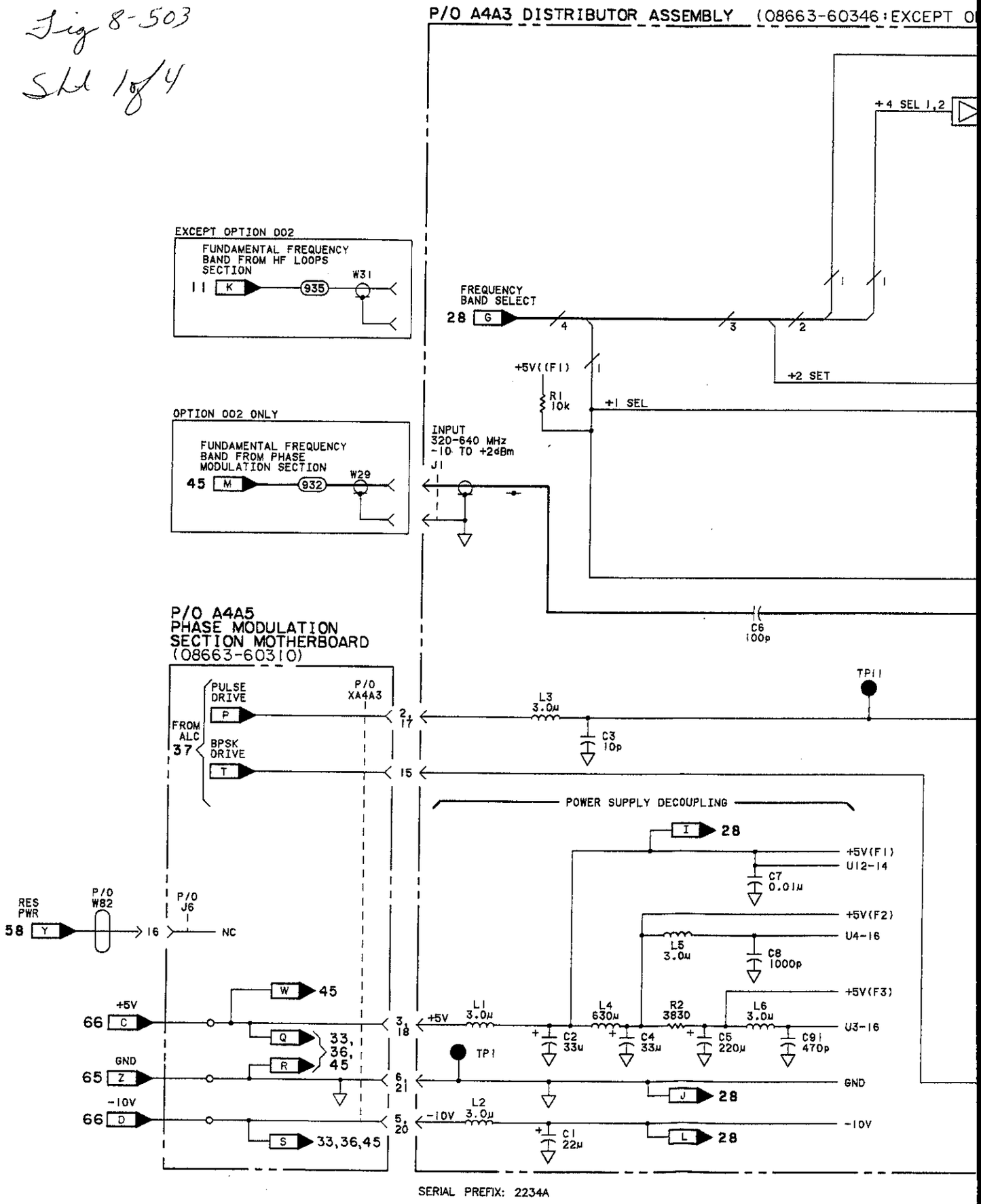


Figure 8-502. P/O A4A3 Distributor Component Locator (2451A and above)



P/O Figure 8-503. P/O Distributor Schematic (2451A and above)

Fig 8-503
Sht 1 of 4



SERIAL PREFIX: 2234A

Fig 8-503 Sht 2 of 4

60346: EXCEPT OPTION 002)

(08663-60304 OPTION 002 ONLY) (NOTE 3)

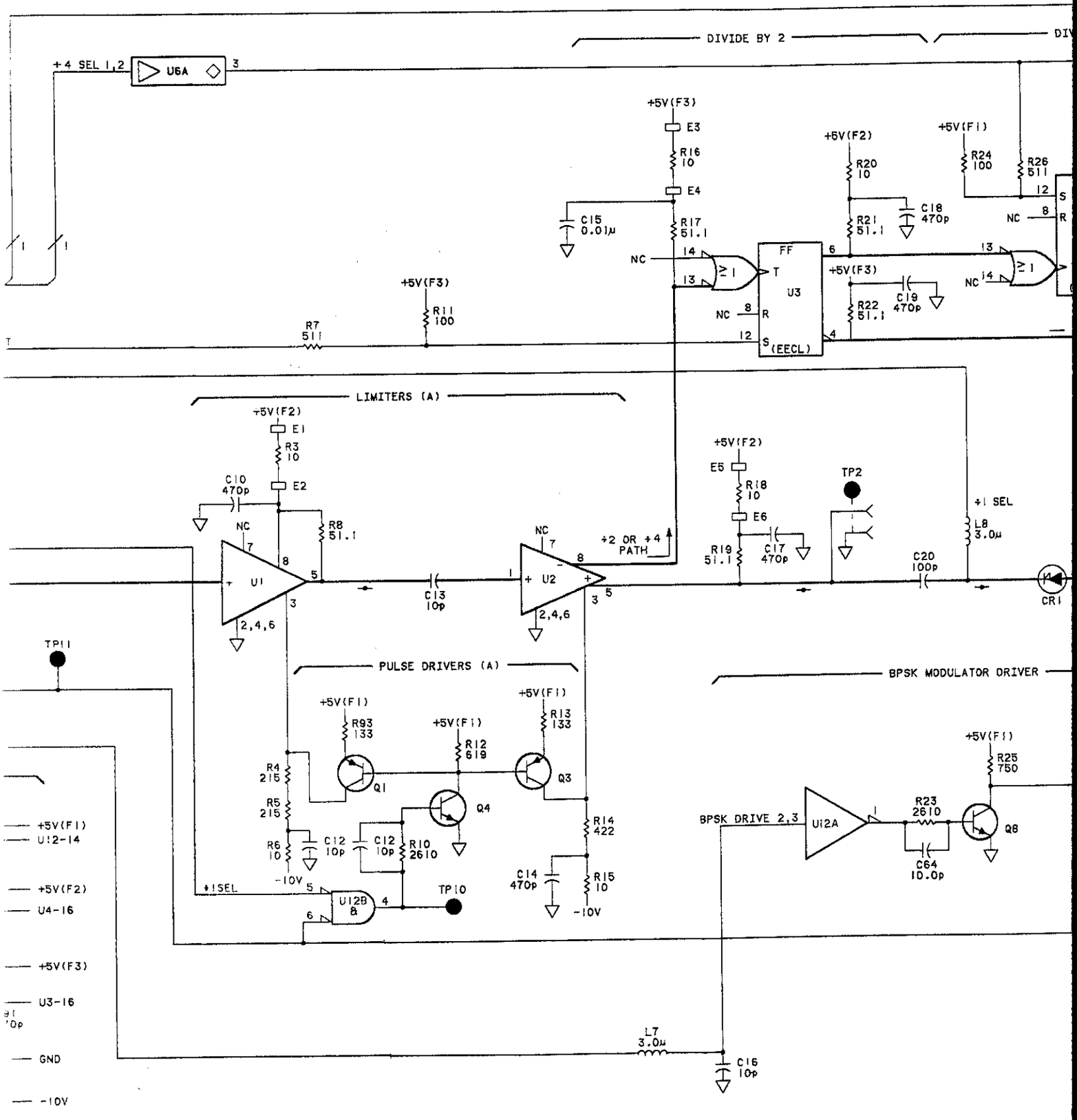


Fig 8-503 Sht 3 of 4

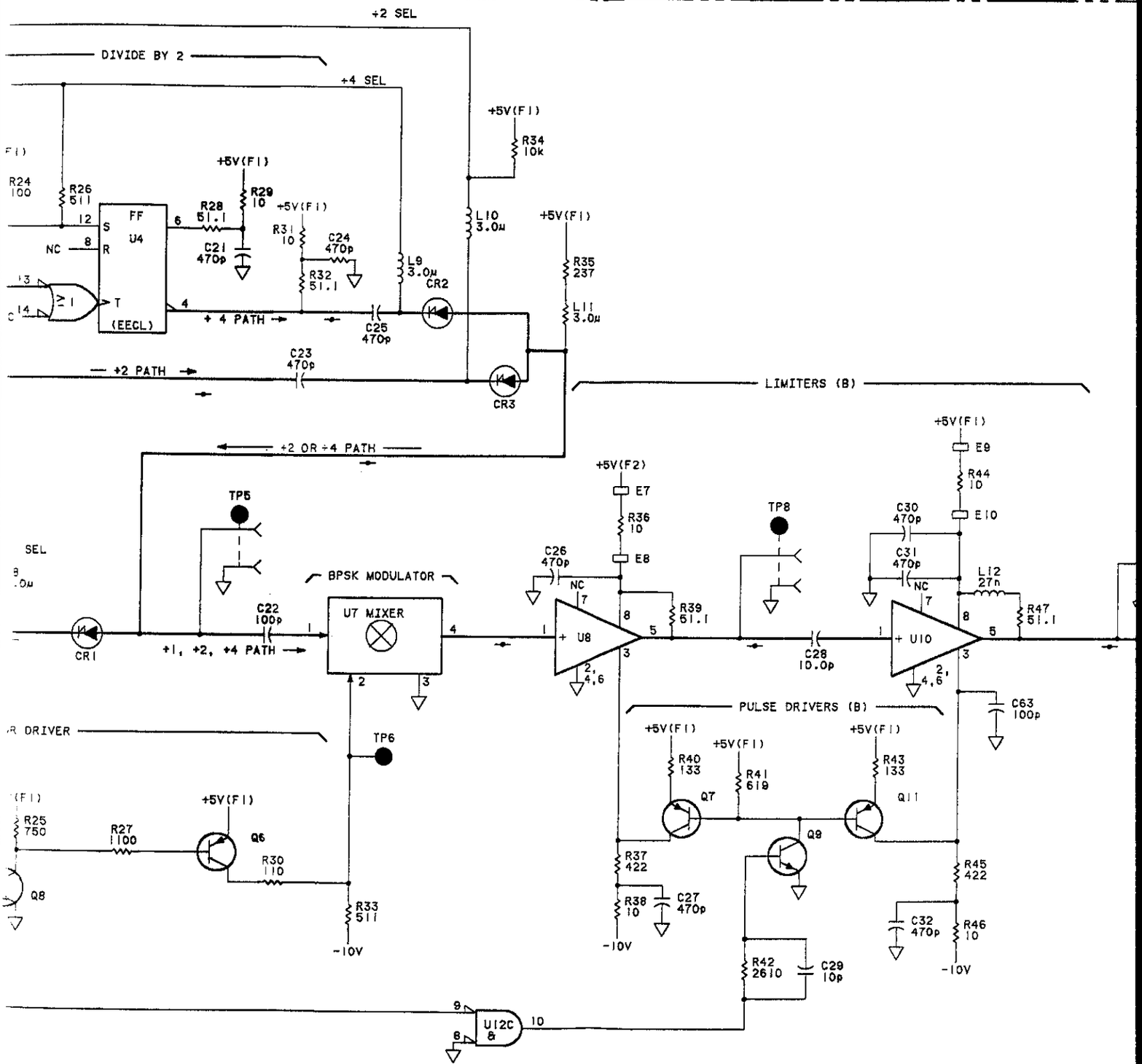


Fig 8-503
Sht 4 of 4

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. THE A4A3 DISTRIBUTOR ASSEMBLY PART NUMBER IS 08663-60346 FOR STANDARD AND OPTION 001 INSTRUMENTS, AND 08663-60304 FOR OPTION 002 INSTRUMENTS. OPTION 002 A4A3 ASSEMBLIES INCLUDE 4 GHz PHASE MODULATION OSCILLATOR A4A4A1. (SEE SERVICE SHEET 45)

LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

REFERENCE DESIGNATIONS

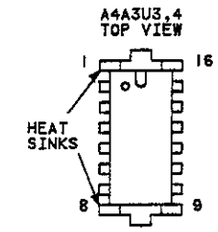
NO PREFIX	U1-4,7,8,10,12 R1-47 TP1,2,5,6,8-11
W29,31,82	
A4A3	
C1-33,63,64 CR1-3 E1-10 L1-12 Q1,3,4,6-9,11	A4A5
	XA4A3

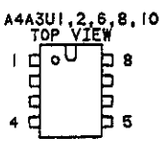
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

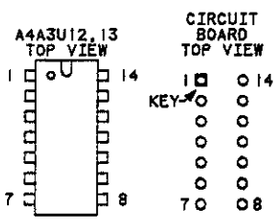
REFERENCE DESIGNATIONS	PART NUMBERS
Q1,3,6,7,11 Q4,8,9	1853-0405 1854-0809
U1,2,8,10	1826-0372
U3,4	1820-1940
U6	1820-0535
U7	0955-0147
U12	1820-1322
U13	1820-1197

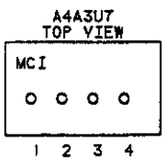
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

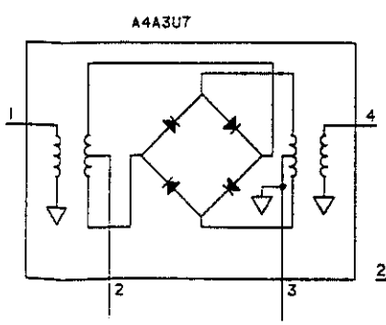
REFERENCE DESIGNATIONS	PIN NUMBERS
U3,4	⏚ - 1,3,5,7,9-11,15
U6	+5V(F1) - 8 - 4 ⏚
U12	⏚ - 7

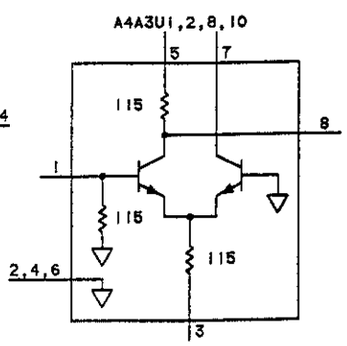


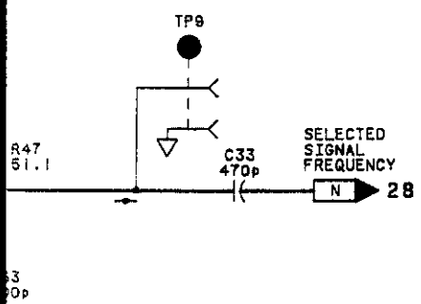












SERVICE SHEET 27

P/O A4A3

Figure 8-503. P/O Distributor Schematic

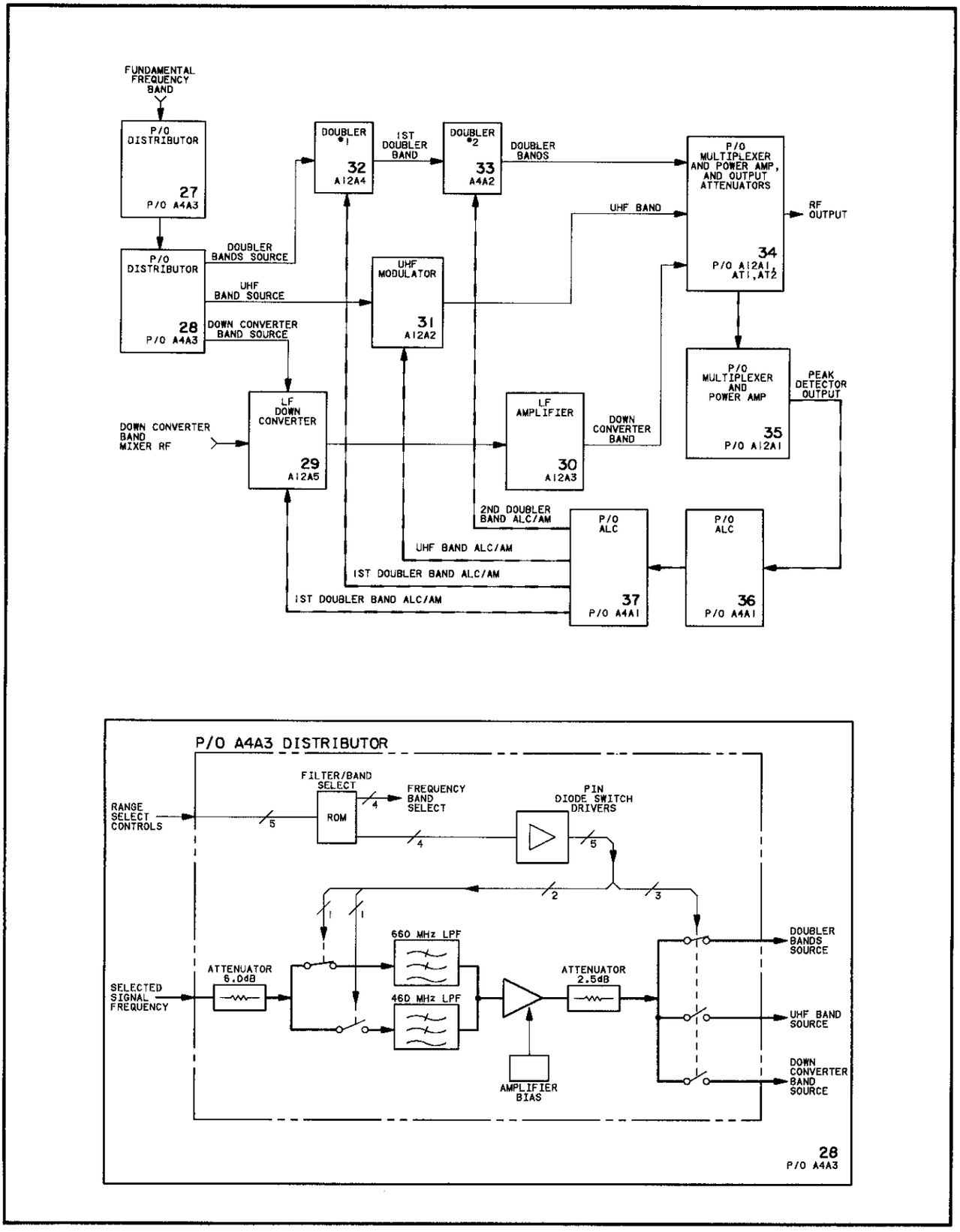


Figure 8-504. P/O A4A3 Distributor Block Diagrams

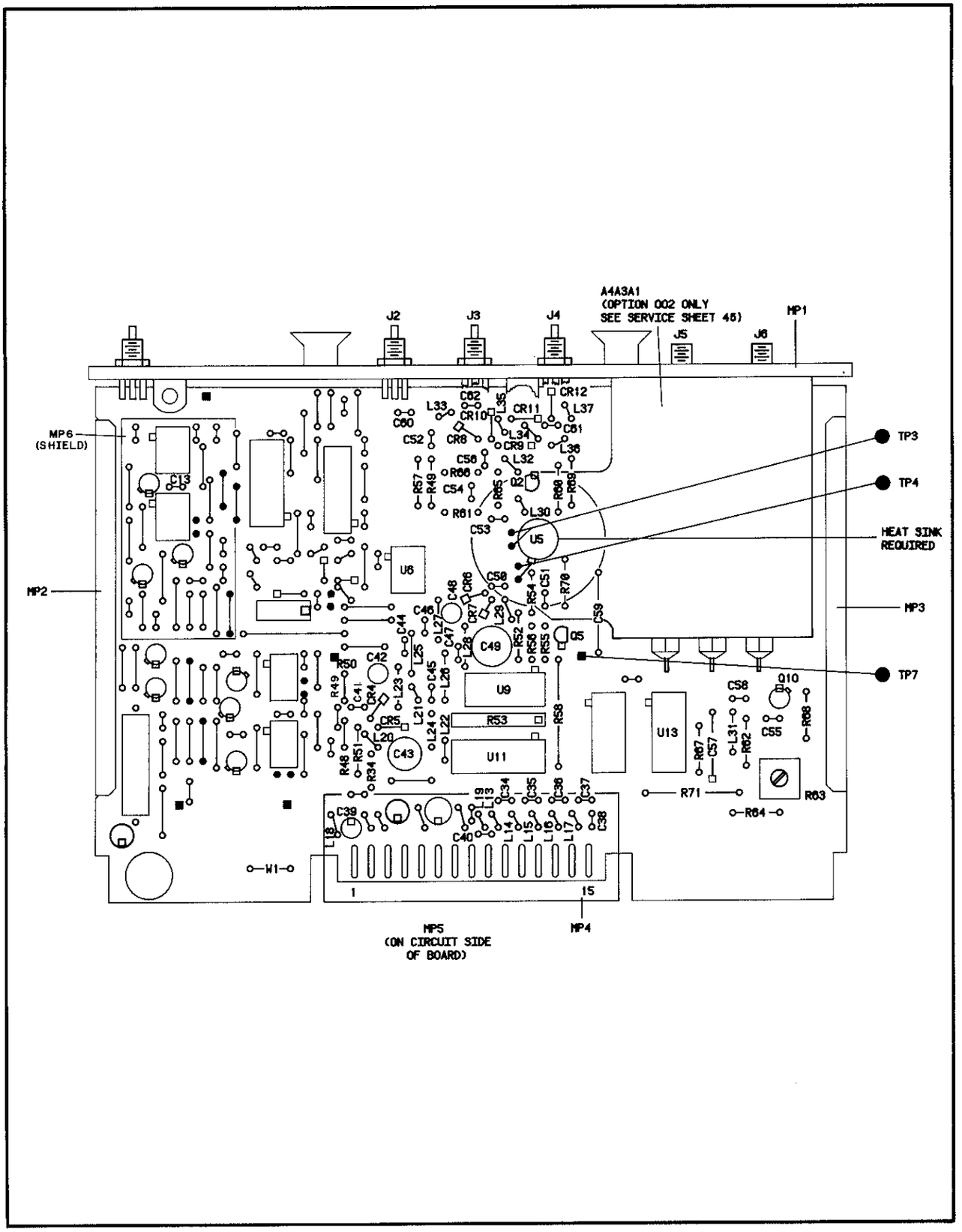


Figure 8-505. P/O A4A3 Distributor Component Locator

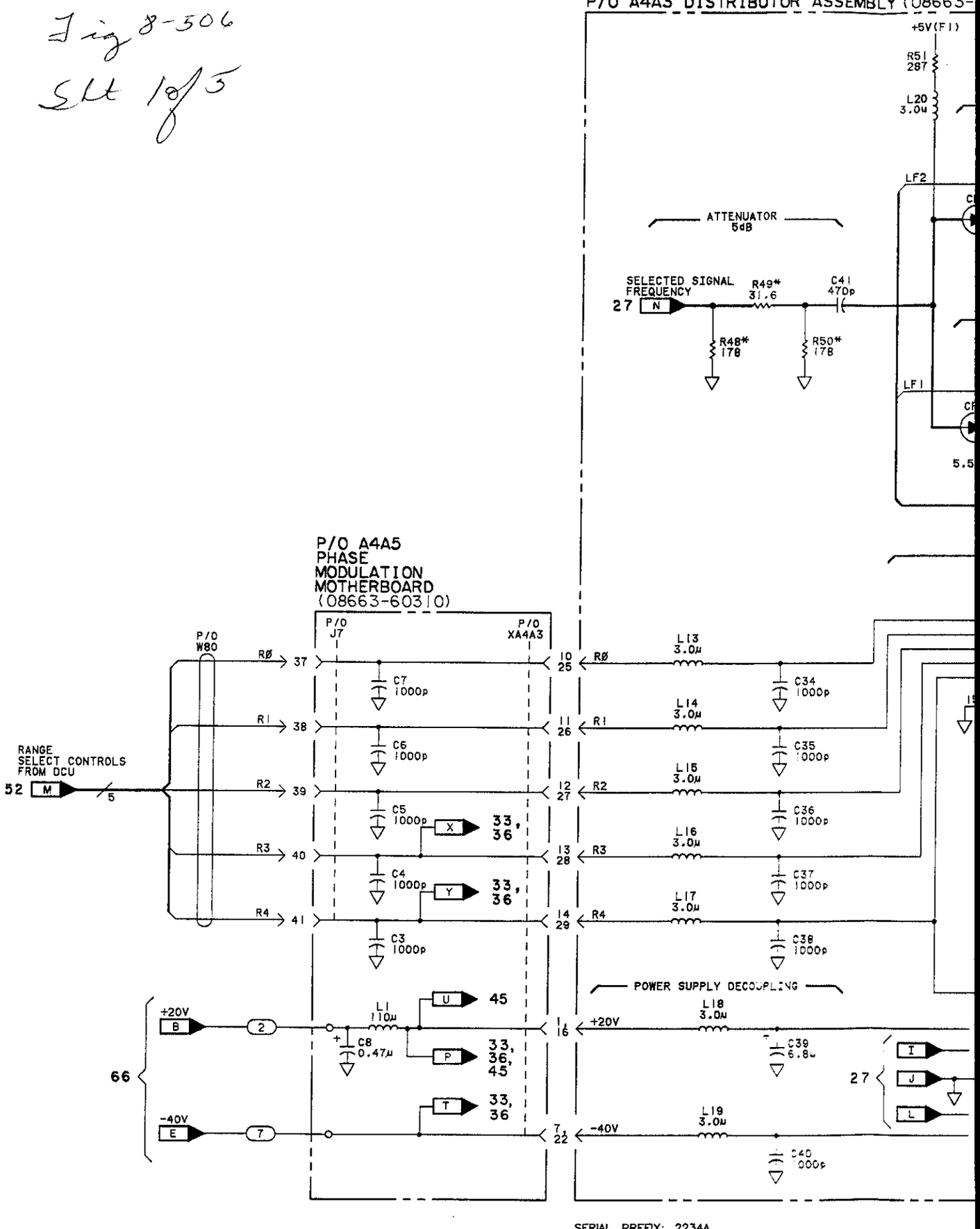
CHANGES

2350A and Above

On the A4A3 component locator:

- A4A3R63 - Change R63 to show side adjustment rather than top adjustment.

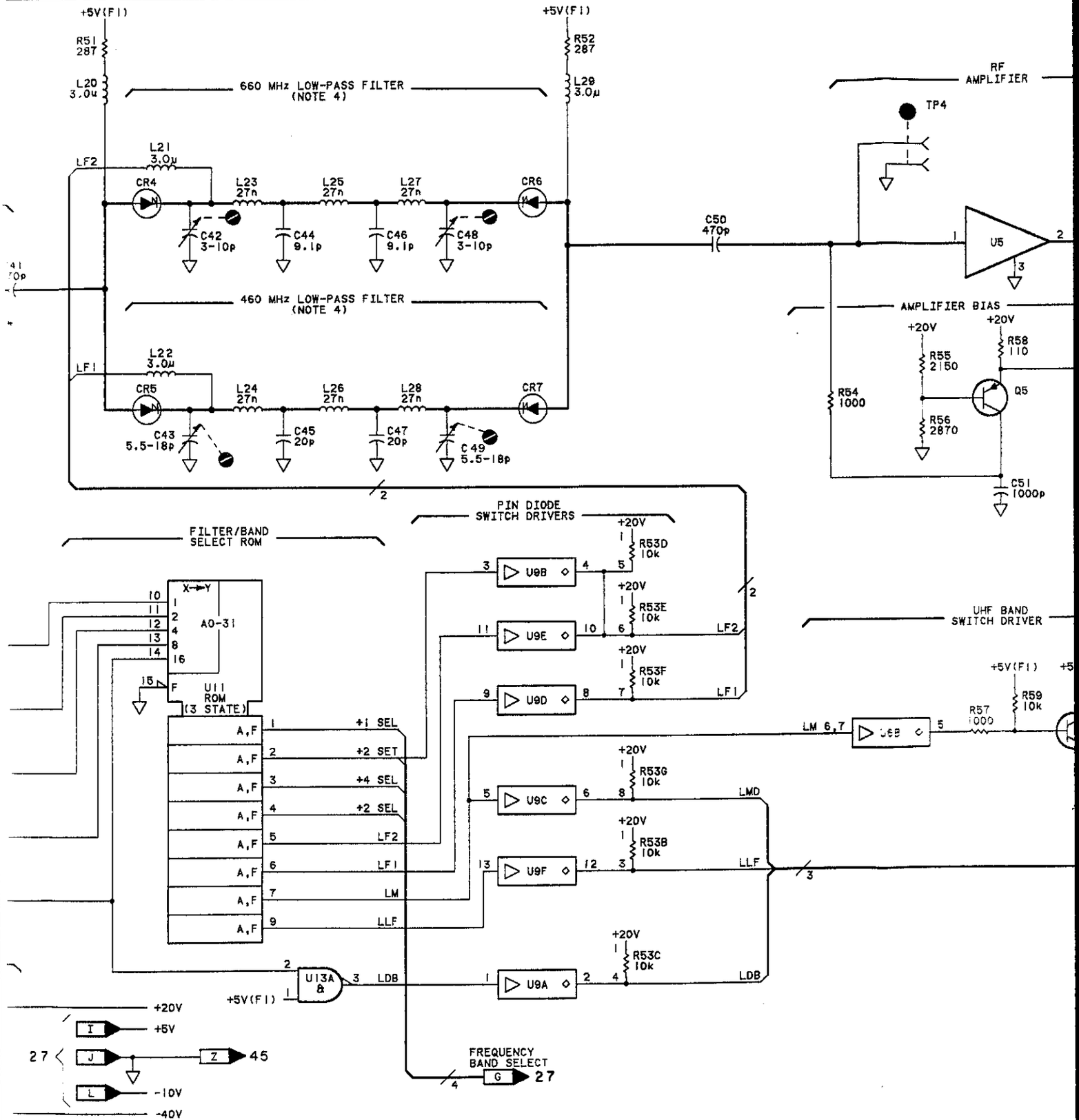
Fig 8-306
Sht 1 of 5



SERIAL PREFIX: 2234A

Fig 8-506 Sht 2 of 5

SEMBLY (08663-60346: EXCEPT OPTION 002) (08663-60304: OPTION 002 ONLY) (NOTE 3)



002 ONLY) (NOTE 3) Fig 8-506 Sht 3 of 5

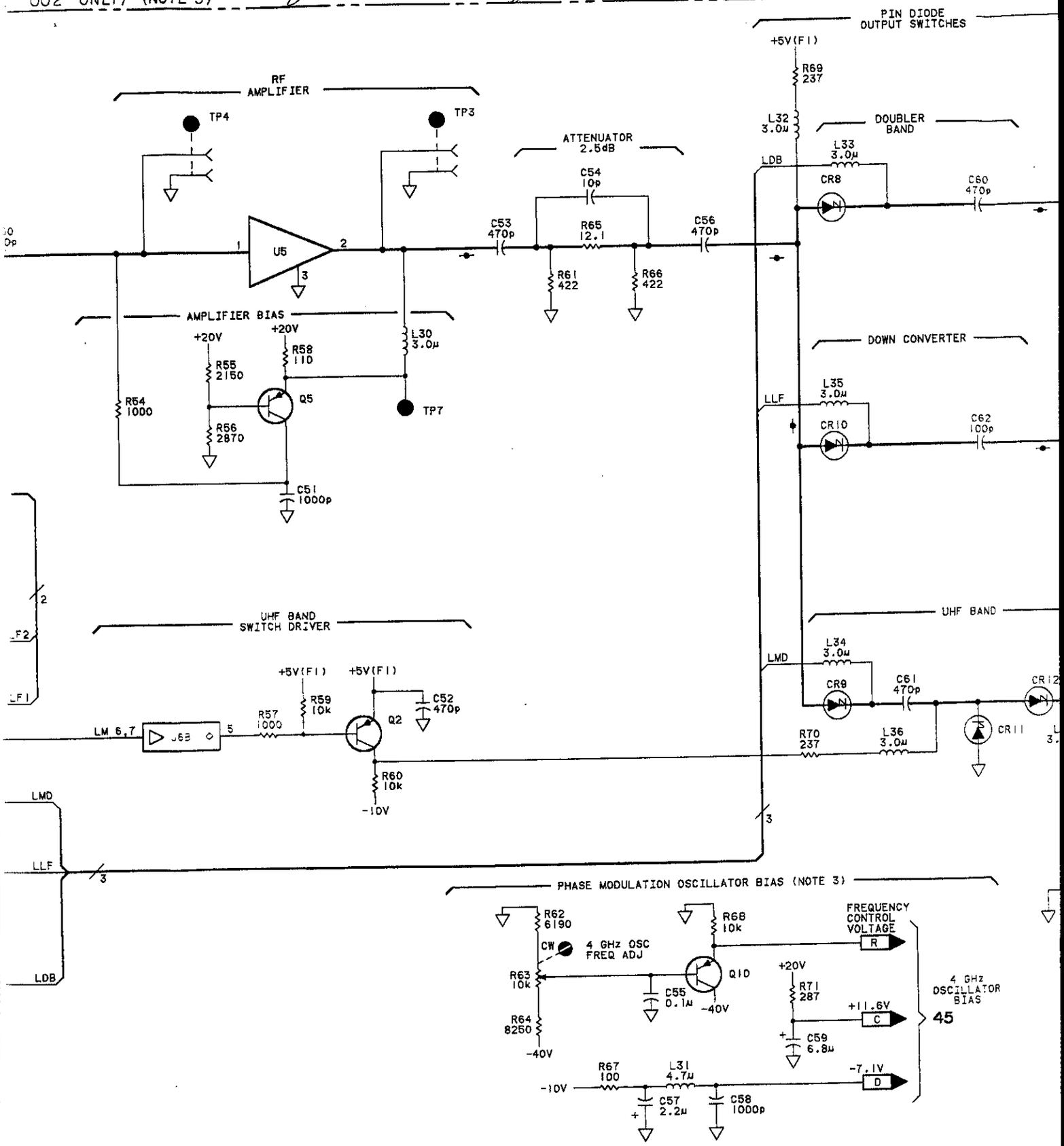
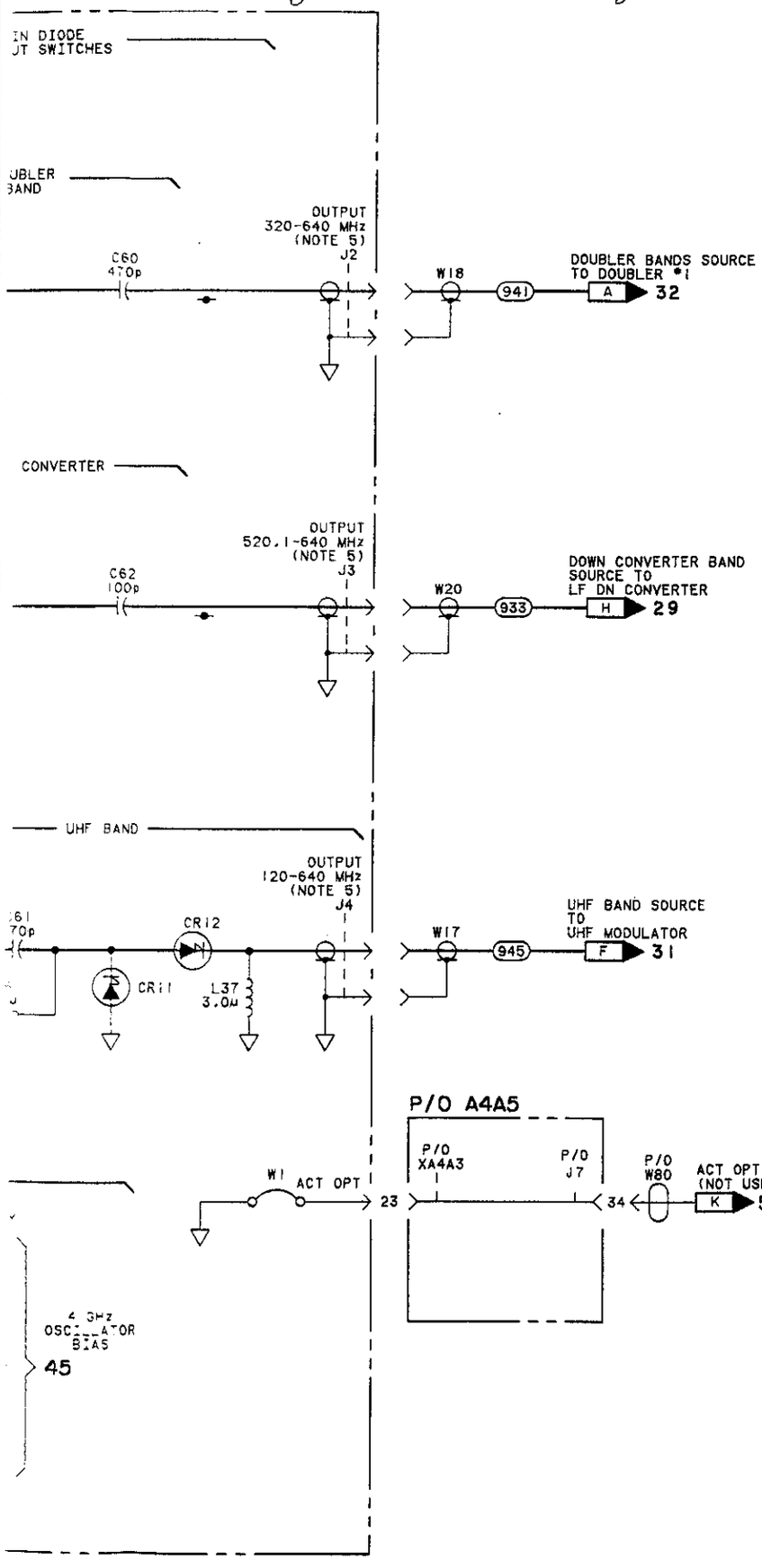


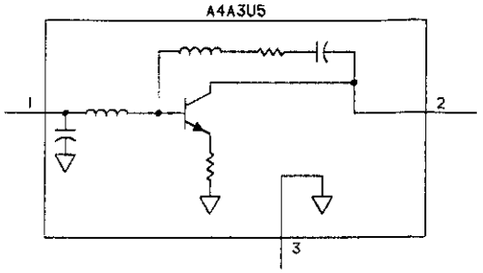
Fig 8-506 Sht 4 of 5



NOTES

1. REFER TO TABLE 8- FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. A4A3 DISTRIBUTOR PART NUMBER IS 08663-60346 FOR STANDARD AND OPTION 001 INSTRUMENTS, AND 08663-60304 FOR OPTION 002 INSTRUMENTS. OPTION 002 A4A3 ASSEMBLIES INCLUDE 4 GHz PHASE MODULATION OSCILLATOR A4A3A1. SEE SERVICE SHEET 45. ALL A4A3 ASSEMBLIES INCLUDE OSCILLATOR BIAS NETWORK SHOWN.
4. VARIABLE CAPACITORS AT INPUT AND OUTPUT NODES OF LOW-PASS FILTERS PROVIDE FOR FILTER FREQUENCY RESPONSE ADJUSTMENT. SEE SECTION V FOR PROCEDURES.
5. FOR 320-640 MHz AT J2, SET GENERATOR'S OUTPUT FREQUENCY TO 640-2560 MHz. FOR 520.1 -640 MHz AT J3, SET OUTPUT TO 10 KHz-120 MHz. FOR 120-640 MHz AT J4, SET OUTPUT TO 120-640 MHz

A4A3U5



REFERENCE DESIGNATIONS

NO PREFIX	A4A5
W17,18,20,80	C3-8 J7 L1 XA4A3
A4A3	
C34-62 CR4-12 L13-37 Q2,5,10 R48-71 TP3,4,7 U5,6,9 11,13	

LOGIC LEVELS

	TTL
HIGH	>+2.0V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW

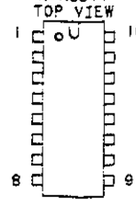
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U6	+5V(F1)- ▽ - +5V(F1)-
U9,13	▽ - +5V(F1)-
U11	▽ -

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

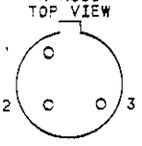
REFERENCE DESIGNATIONS	PART NUMBERS
Q2,5	1853-0459
Q10	1853-0281
U5	08662-67002
U6	1820-0535
U9	1820-0668
U11	08663-80003
U13	1820-1197
U14	08663-60033

A4A3U11
TOP VIEW



CIRC
BOA
TOP
KEY
8

A4A3U5
TOP VIEW



A4A3R53
TOP VIEW

1	2	3	4	5	6	7	8

COMMON A B C D E F G

NOTES

FER TO TABLE 8- FOR SCHEMATIC
AGRAM NOTES.

ROUBLESHOOTING VALUES ARE TYPICAL.
HEY ARE ACTUAL MEASURED VALUES.
OUR MEASUREMENTS MAY BE SLIGHTLY
FFERENT THAN WHAT IS SHOWN.

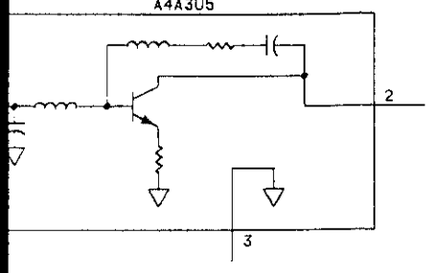
A3 DISTRIBUTOR PART NUMBER IS 08663-60346 FOR
ANDARD AND OPTION 001 INSTRUMENTS, AND 08663-60304
R OPTION 002 INSTRUMENTS. OPTION 002
A3 ASSEMBLIES INCLUDE 4 GHz PHASE MODULATION
SCILLATOR A4A3A1. SEE SERVICE SHEET 45. ALL A4A3
SSEMBLIES INCLUDE OSCILLATOR BIAS NETWORK SHOWN.

ARIABLE CAPACITORS AT INPUT AND OUTPUT NODES OF
W-PASS FILTERS PROVIDE FOR FILTER FREQUENCY
SPONSE ADJUSTMENT. SEE SECTION V FOR PROCEDURES.

R 320-640 MHz AT J2, SET GENERATOR'S OUTPUT FREQUENCY
640-2560 MHz. FOR 520.1 -640 MHz AT J3. SET OUTPUT
10 KHz-120 MHz. FOR 120-640 MHz AT J4, SET OUTPUT
120-640 MHz

Fig 8-506
Sht 5 of 5

A4A3U5



REFERENCE DESIGNATIONS

NO PREFIX	A4A5
W17,18,20,80	C3-8 J7 L1 XA4A3
A4A3	
C34-62 CR4-12 L3-37 Q2,5,10 R48-71 TP3,4,7 U5,6,9 [illegible]13	

LOGIC LEVELS

	TTL
HIGH	>+2.0V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW

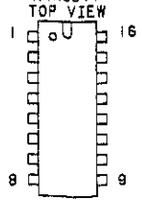
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U6	+5V(F1)- 8 ▽ - 4
U9,13	+5V(F1)- 14 ▽ - 7
U11	+5V(F1)- 16 ▽ - 8

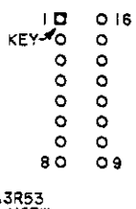
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q2,5	1853-0459
Q10	1853-0281
U5	08662-67002
U6	1820-0535
U9	1820-0668
U11	08663-80003
U13	1820-1197
U14	08663-60033

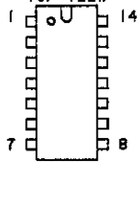
A4A3U11 TOP VIEW



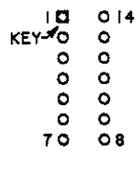
CIRCUIT BOARD TOP VIEW



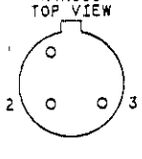
A4A3U9,13 TOP VIEW



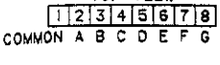
CIRCUIT BOARD TOP VIEW



A4A3U5 TOP VIEW



A4A3R53 TOP VIEW



SERVICE SHEET 28

P/O A4A3

Figure 8-506. P/O Distributor Schematic

SERVICE SHEET 29
A12A5 LOW FREQUENCY DOWN CONVERTER

REFERENCE BLOCK DIAGRAM 6
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Low Frequency Down Converter Board generates the 10 kHz to 120 MHz low frequency RF band. It does this by mixing the 520.1 MHz to 640 MHz down converter source signal from the Distributor Board (service sheet 28) with the 520 MHz down converter band mixer RF from the reference section.

The 520.1 MHz to 640 MHz down converter source signals from the distributor enter the Down Converter Board by way of J1. This signal is boosted from +1.75 dBm to approximately +11 dBm by microcircuit amplifier U1. The signal is then coupled, via C14, to a narrow-band tuned amplifier formed by Q2. Tuning is accomplished by variable capacitor C16 in conjunction with L9. The gain of this stage is approximately 10 dB, boosting the signal to +20 dBm.

The 680 MHz low-pass filter reduces harmonics present in the output to 40 dB below signal level. The 3 dB attenuator attenuates the signal output to +17 dBm and creates a better broadband match to the LO input of the mixer.

The 520 MHz input from the reference section enters the Down Converter Board via the J3 input at +1 dBm. To compensate for the insertion loss of the AM modulator, the signal is amplified to +10 dBm by the +9 dB amplifier formed byQ6. This amplifier is biased from the negative supply.

PIN Modulator

The PIN diode AM modulator formed by CR1, CR2, CR3, and CR4, modulates the 520 MHz input signal with the signal from the ALC Board (service sheet 37). The ALC signal enters the Down Converter Board via pin 9 and is injected between CR2 and CR3. The signal splits and goes through both the right and left set of diodes. The more current that flows in the line, the lower the impedance of the diodes. This results in lower insertion loss and a greater amplitude output signal.

Following modulation, the signal is amplified by the +9 dB amplifier formed by Q5. The output of this amplifier is approximately -5 dBm. The signal then passes through a 680 MHz low-pass filter and a 3 dB

attenuator and is fed into the RF input of the mixer at approximately-8 dBm.

Mixer

The mixer takes the 520.1 MHz to 640 MHz down converter source signal and hetrodynes it with the 520 MHz reference RF to produce the 10 kHz to 120 MHz low level down converter band. The 25 dB difference between the LO and RF inputs of the mixer is necessary to reduce the effect of spurs. If the difference is greater than 25 dB, the signal will become buried in noise. Part of the effect of the ALC loop is to ensure that the mixer operates within the 25 dB range.

The output of the mixer is about -16 dBm. Before being sent to the output amplifier stages, it is amplified by the Low Frequency Amplifier (service sheet 30).

Bias Regulators and Down Converter Enable

The bias regulators for the two down converter source amplifiers are formed by Q3 and Q4. The down converter enable line from the MULTIPLEXER/POWER AMP (service sheet 34) is used to switch the Down Converter Board ON and OFF through transistor Q4, which is the ground source for the bias regulators.

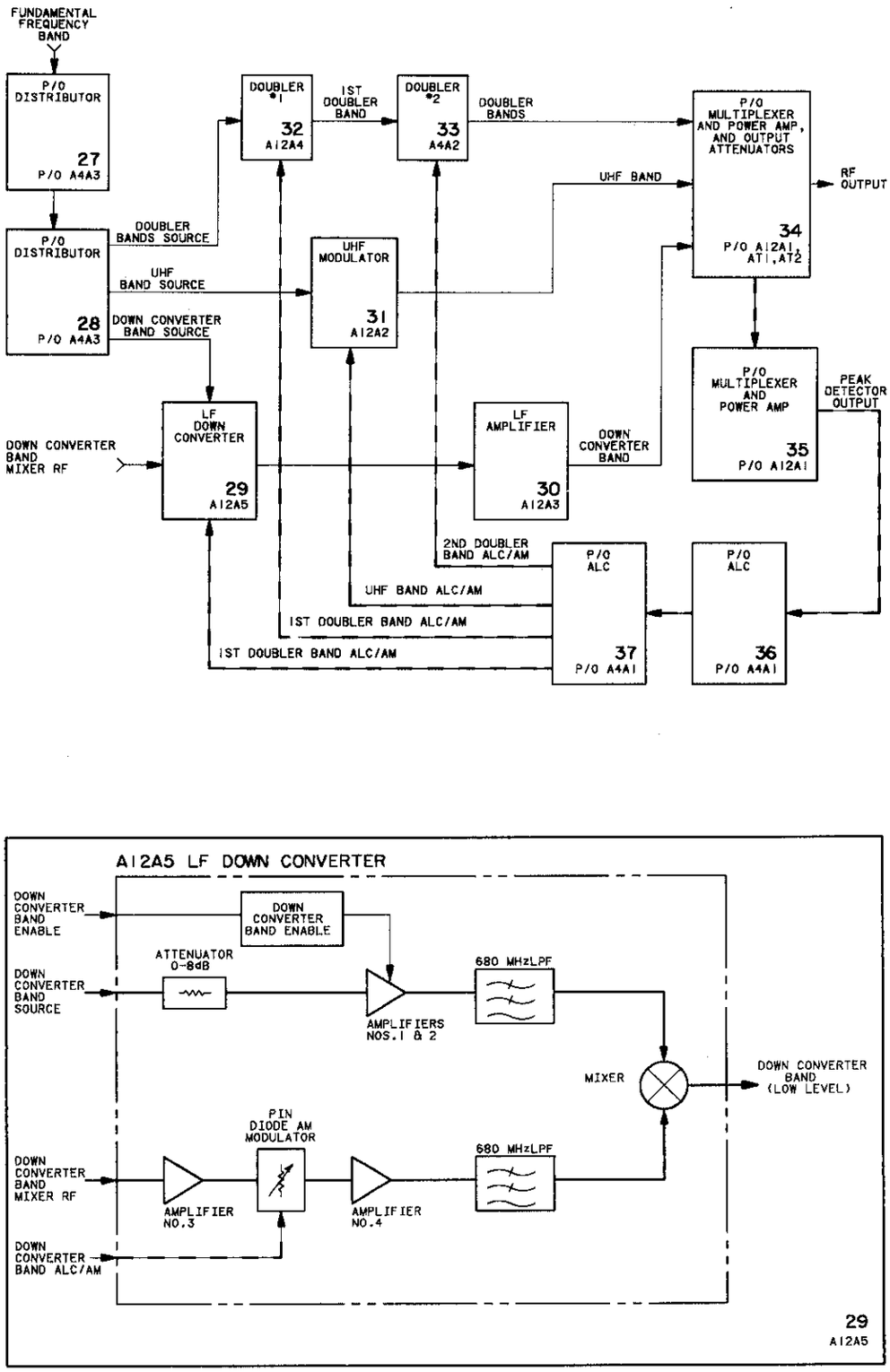


Figure 8-507. A12A5 LF Down Converter Block Diagrams

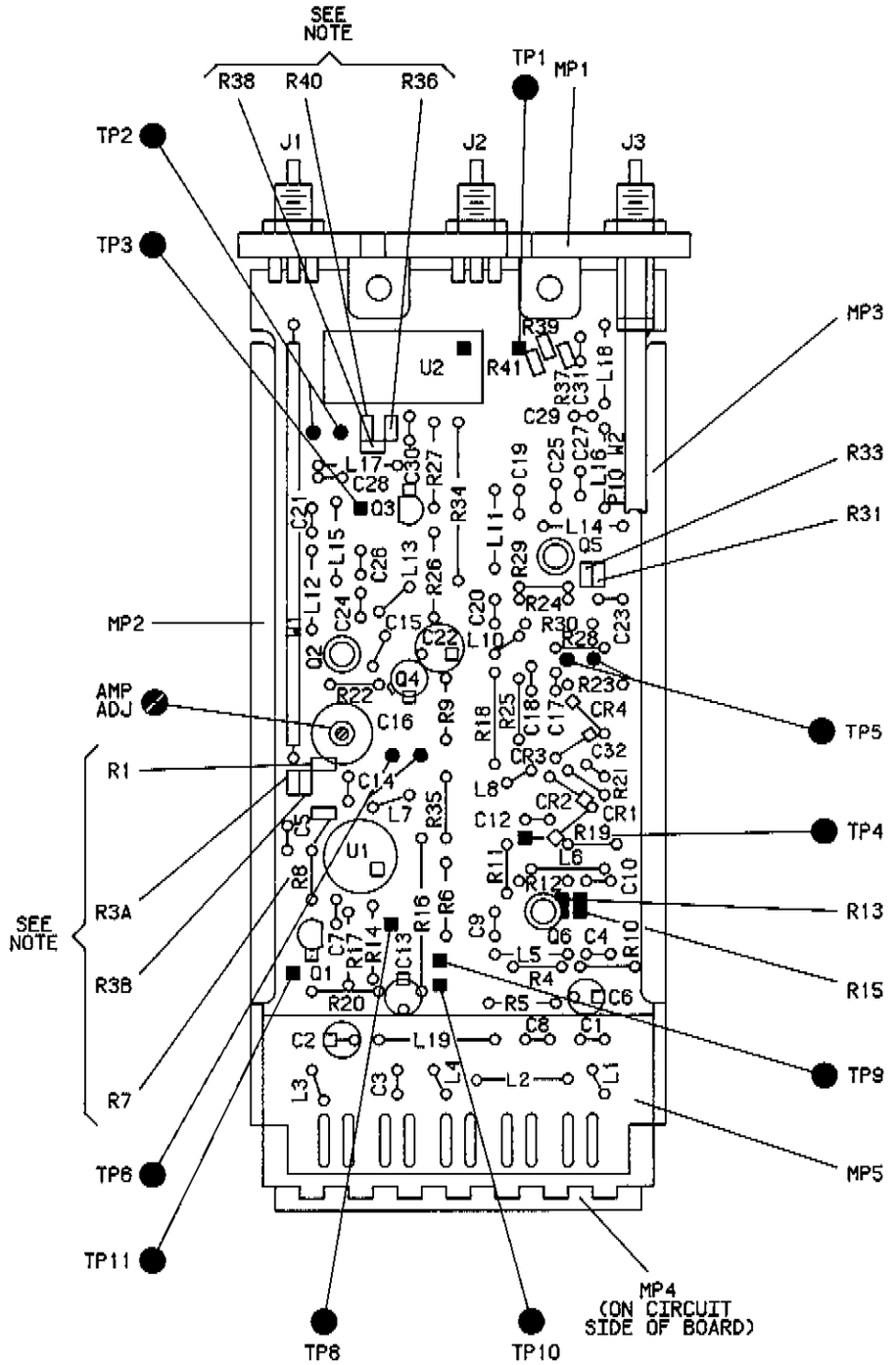


Figure 8-508. A12A5 LF Down Converter Component Locator

CHANGES

All serial prefixes

On the A12A5 schematic:

- A12A5R42 – Delete R42.

2333A and Above

On the A12A5 schematic:

- A12A5J3 – In the middle of the left side of the schematic, above A12A5J3, change the label to read, "Input 520 MHz (–1 dBm ±.75 dBm)".

Fig 8-509
Sht 1 of 4

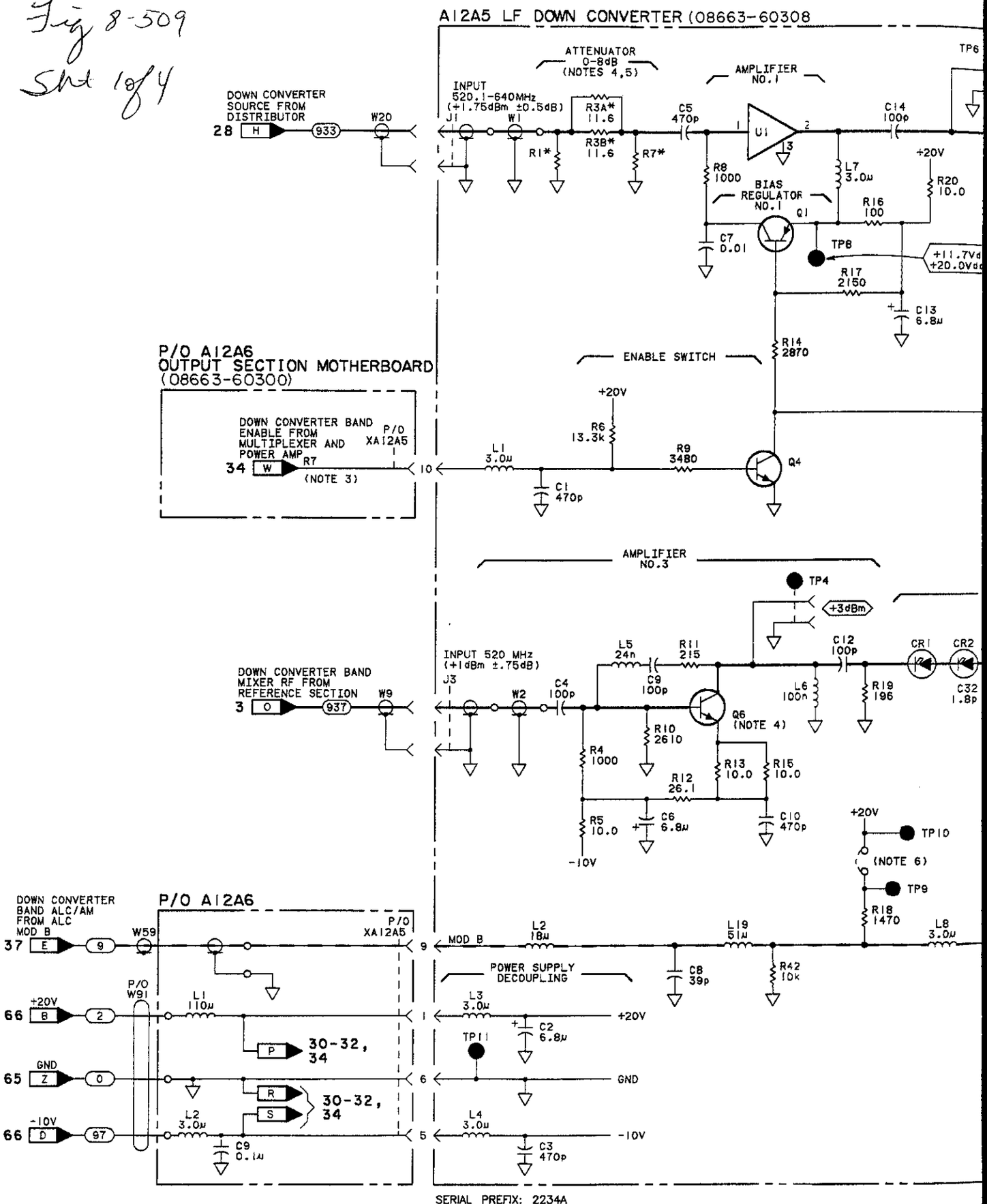


Fig 8-509 Sht 2 of 4

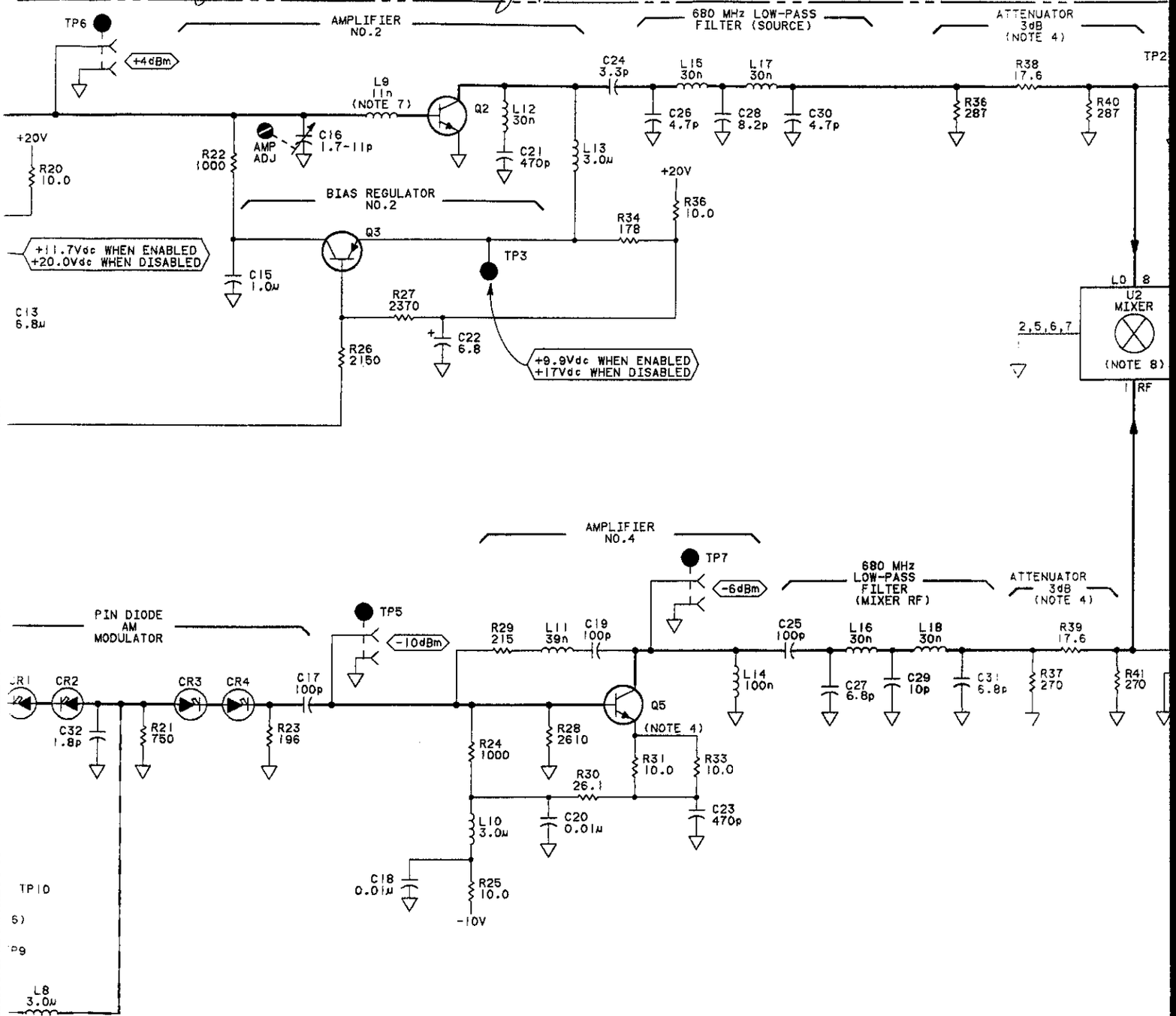
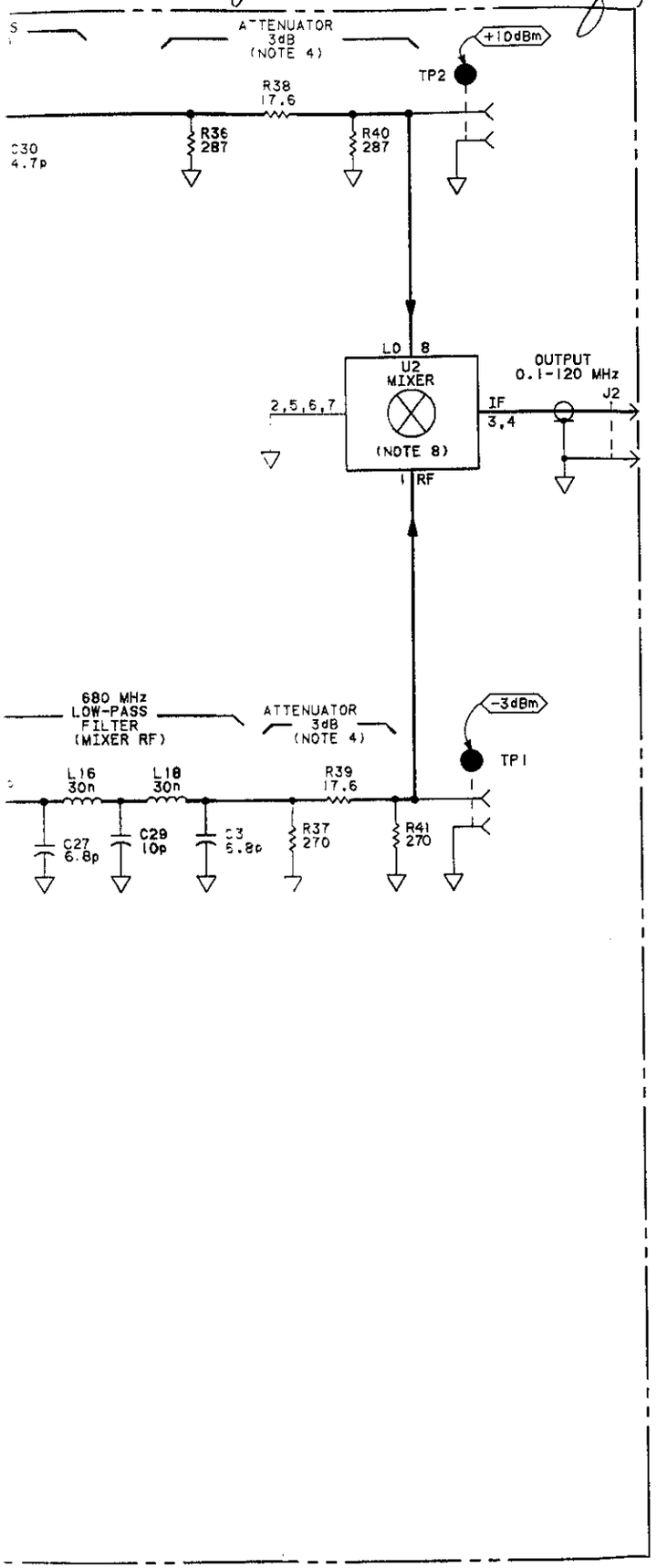


Fig 8-509 Sht 3 of 4



CAUTION

RF TEST POINTS (PC BOARD CUP CONNECTORS) MUST BE AC COUPLED TO TEST EQUIPMENT. OTHERWISE DAMAGE MAY OCCUR TO THE TEST EQUIPMENT OR THE CIRCUIT UNDER TEST. USE THE SPECIAL CAPACITOR COUPLED CABLE ADAPTOR FOUND IN THE SERVICE KIT.

NOTES

1. REFER TO TABLE 8- FOR SCHEMATI DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICA THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTL DIFFERENT THAN WHAT IS SHOWN.
3. R7 IS A TTL LEVEL HIGH (THAT IS, THE ENABLE CONDITION) ONLY WHEN THE OUTPUT FREQUENCY IS BELOW 120 MHz
4. THE SMALL CHIP RESISTORS ON THIS ASSEMBLY REQUIRE LOW TEMP- ERATURE SOLDERING TECHNIQUES. USE SILVER SOLDER.
5. ASTERISK (*) INDICATES THAT PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL AND REPRESENT 0dB ATTENUATION. REFER TO SECTION V FOR PROCEDURE
6. JUMPER IS INSTALLED TO TURN MODULATOR FULLY ON. REMOVE A4A1 BEFORE CONNECTING. LEVEL AT TP5 SHOULD BE APPROXIMATELY -2dBm WITH JUMPER INSTALLED
7. INDUCTOR L9 IS NOT A DISCRETE COMPONENT. IT IS A PC BOARD TRACE.
8. U2 SHOULD BE SOLDERED AT PINS 1 AND 8.

† BACKDATING INFORMATION IS SECTIO

REFERENCE DESIGNATIONS

NO PREFIX	A12A6
W16-18	C9 L1,2 W59 XA12A5
A12A5	
C1-10,12-32 CR1-4 J1-3 L1-19 Q1-6 R1,3-31,33-42 TP1-11 U1,2 W1,2	

LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

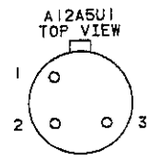


Fig 8-509
Sht 4 of 4

CAUTION

TEST POINTS (PC BOARD CUP
NECTORS) MUST BE AC COUPLED
TEST EQUIPMENT. OTHERWISE
AGE MAY OCCUR TO THE TEST
IPMENT OR THE CIRCUIT UNDER
T. USE THE SPECIAL CAPACITOR
PLED CABLE ADAPTOR FOUND IN
SERVICE KIT.

W16 — 934 — A — 30 — DOWN CONVERTER BAND (LOW LEVEL -4dBm) TO LF AMPLIFIER

NOTES

1. REFER TO TABLE 8- FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. R7 IS A TTL LEVEL HIGH (THAT IS, THE ENABLE CONDITION) ONLY WHEN THE OUTPUT FREQUENCY IS BELOW 120 MHz
4. THE SMALL CHIP RESISTORS ON THIS ASSEMBLY REQUIRE LOW TEMPERATURE SOLDERING TECHNIQUES. USE SILVER SOLDER.
5. ASTERISK (*) INDICATES THAT PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL AND REPRESENT 0dB ATTENUATION. REFER TO SECTION V FOR PROCEDURES.
6. JUMPER IS INSTALLED TO TURN MODULATOR FULLY ON. REMOVE A4A1 BEFORE CONNECTING. LEVEL AT TP5 SHOULD BE APPROXIMATELY -2dBm WITH JUMPER INSTALLED
7. INDUCTOR L9 IS NOT A DISCRETE COMPONENT. IT IS A PC BOARD TRACE.
8. U2 SHOULD BE SOLDERED AT PINS 1 AND 8.

† BACKDATING INFORMATION IS SECTION VII

REFERENCE DESIGNATIONS

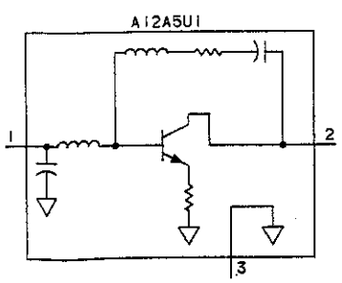
NO PREFIX	A12A6
W16-18	C9 L1,2 W59 XA12A5
A12A5	
C1-10,12-32 CR1-4 J1-3 L1-19 Q1-6 R1,3-31,33-42 TP1-11 U1,2 W1,2	

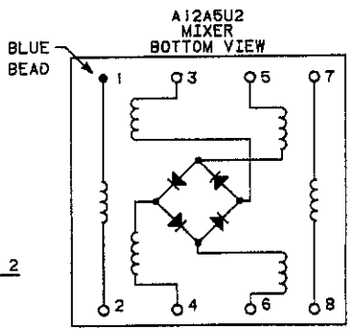
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

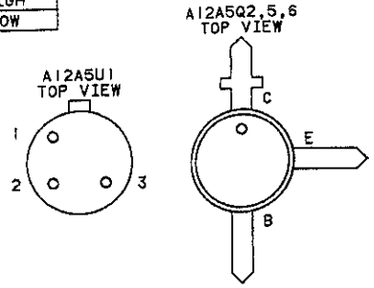
REFERENCE DESIGNATIONS	PART NUMBERS
Q1,3 Q2,5,6 Q4	1853-0036 1854-0720 1854-0477
U1 U2	08662-67002 0960-0495

LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW







SERVICE SHEET 29
A12A5

Figure 8-509. LF Down Converter Schematic

SERVICE SHEET 30
A12A3 LOW FREQUENCY AMPLIFIER

REFERENCE BLOCK DIAGRAM 6
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The low level (-16 dBm typical) 0.1 to 120 MHz output from the Low Frequency Down Converter (service sheet 29) is pre-amplified by the Low Frequency Amplifier before it is sent to the final output amplifiers.

Low-Pass Input Filter

The signal from the Low Frequency Down Converter enters the Low Frequency Amplifier at J1. Here, the mixer sum frequency signal is terminated by a 50 ohm load so that it will not reflect back into the mixer. The desired difference frequency is passed through 120 MHz and 140 MHz low-pass filters, preventing any RF or LO signals from entering the amplifier.

Amplifier Section

The two feedback amplifiers formed by Q1 and Q3 are low in noise. The amplifier formed by Q1 has a gain of approximately 13 dB. Buffer amplifier Q2 minimizes loading of Q1 and matches impedance to the next stage. The signal level at the output of this buffer is -3 dBm. The second feedback amplifier (formed by Q3) provides 7 dB of gain and has an output signal level of about +4 dBm.

Switchable Attenuators

The switchable attenuators following Q3 control the output signal level. The attenuators attenuate at 2 dB, 4 dB, and 8 dB so that any desired attenuation between 2 dB and 14 dB can be accomplished in 2 dB steps. These attenuators are switched in and out by the low frequency amplifier level-control lines, which come from the DCU. The output of the Low Frequency Amplifier Board is sent to the Multiplexer and Power Amp Board (service sheets 34 and 35).

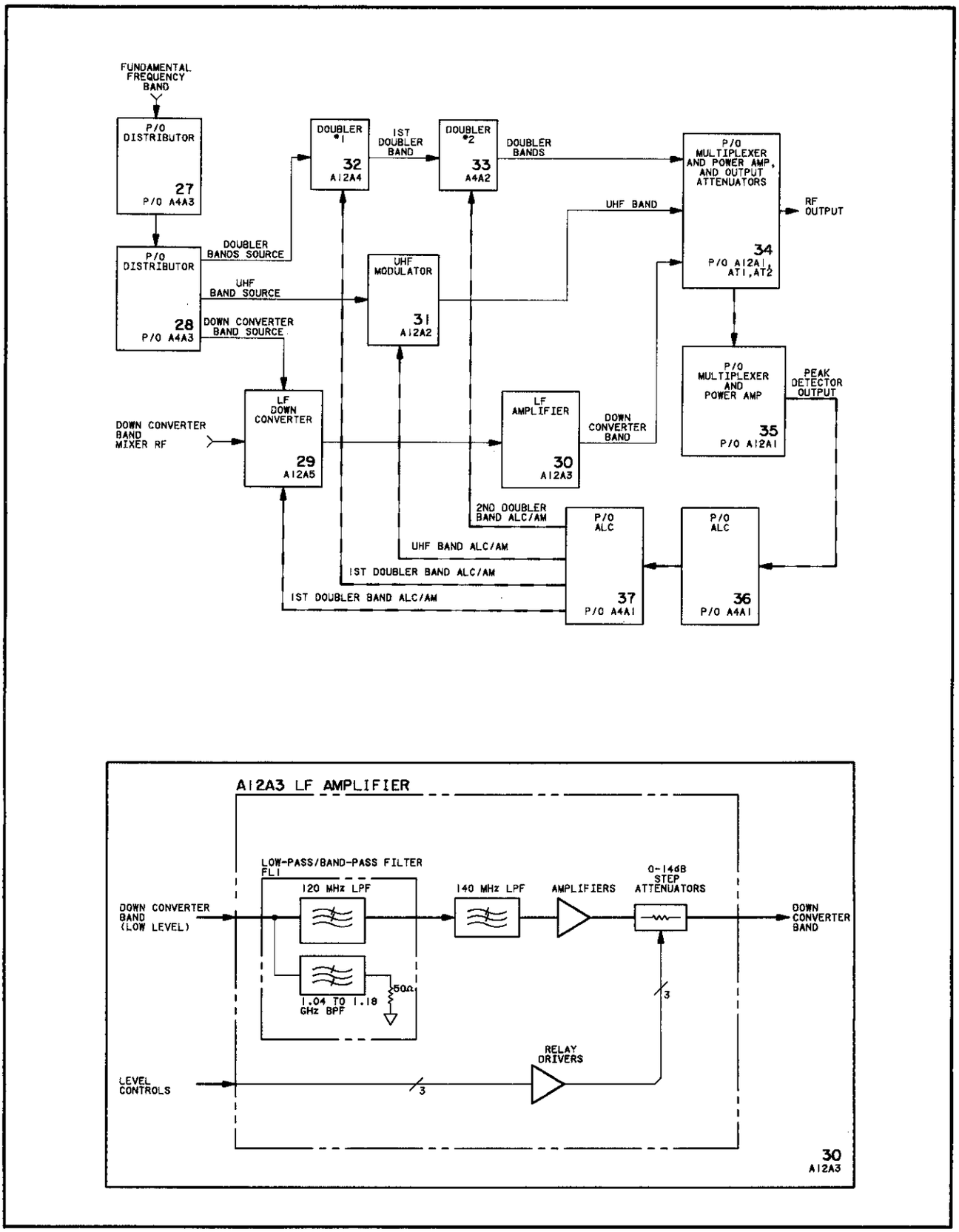


Figure 8-510. A12A3 LF Amplifier Block Diagrams

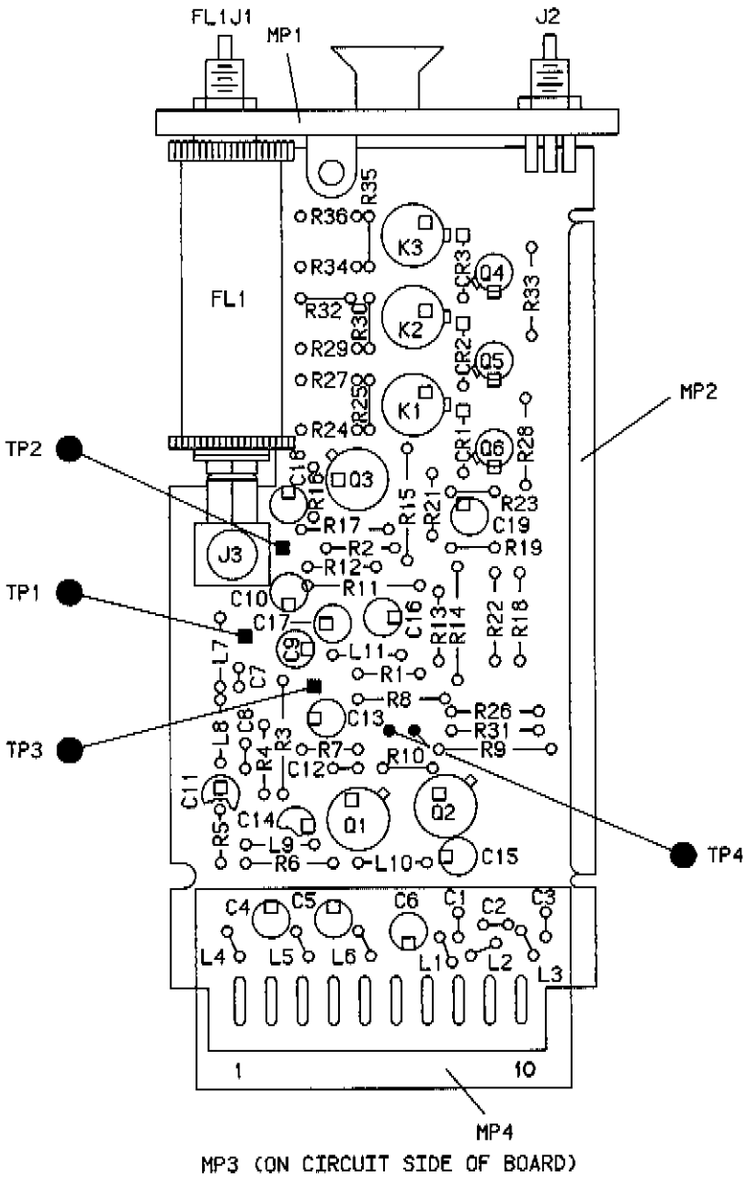


Figure 8-511. A12A3 LF Amplifier Component Locator

CHANGES

All serial prefixes

2339A and Above

On the A12A3 schematic:

- A12A3L4, L6 - Change the value of L4 and L6 to 630u.

On the A12A3 schematic:

- A12A3C20 - On the right side of the schematic, add C20 (22p) from the node of R35 and K3A pin 2, to ground.
- A12A3L9 - Change the value of L9 to 0.39u.
- A12A3R19*, R23* - Change the value of R19* and R23* to 464 ohms.
- A12A3R21* - Change the value of R21* to 12.1 ohms.
- A12A3R24, R27 - Change the value of R24 and R27 to 383 ohms.
- A12A3R29, R32 - Change the value of R29 and R32 to 215 ohms.
- A12A3R30 - Change the value of R30 to 26.1 ohms.
- A12A3R34, R36 - Change the value of R34 and R36 to 110 ohms.

Fig 8-512
Sht 1 of 4

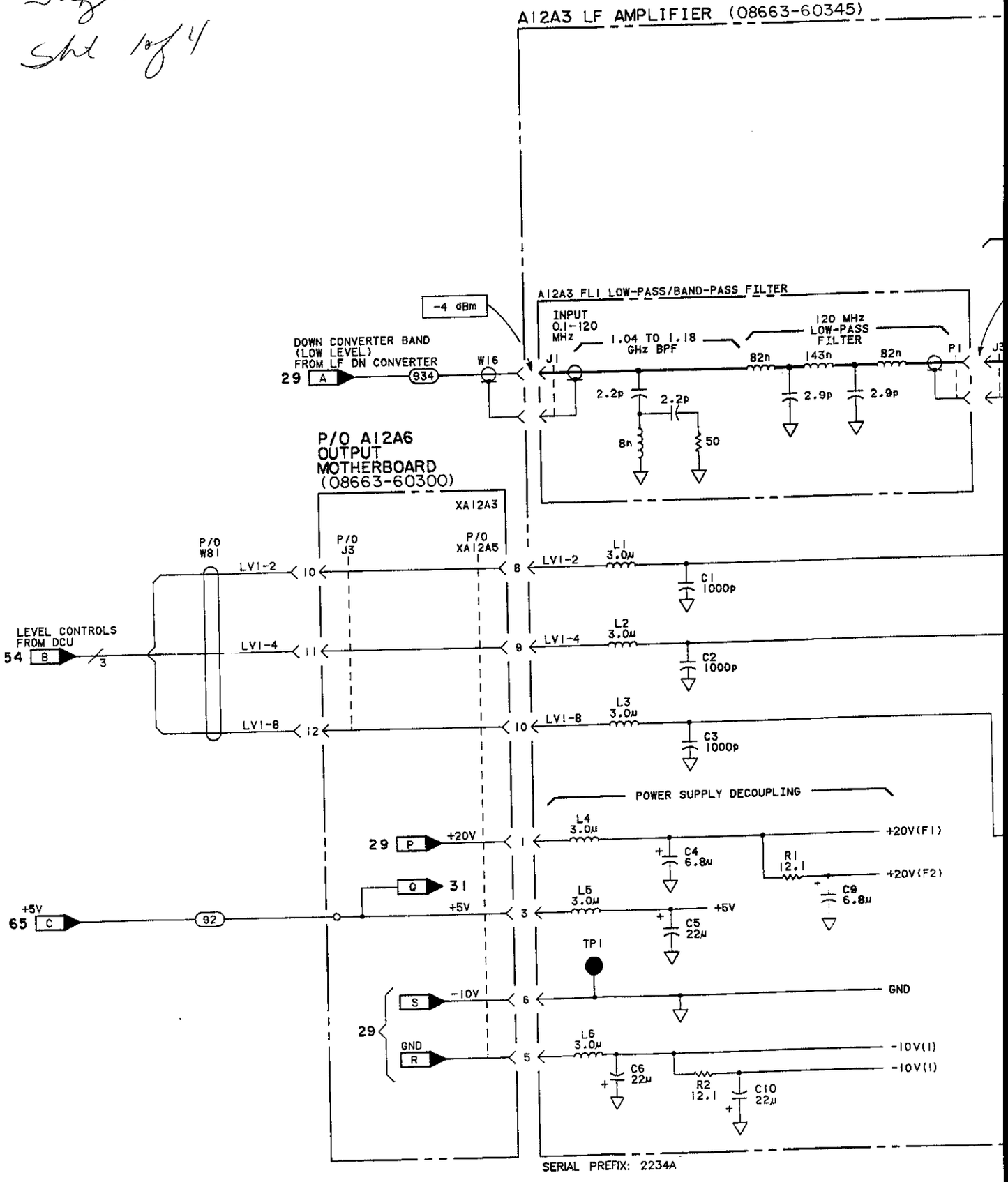
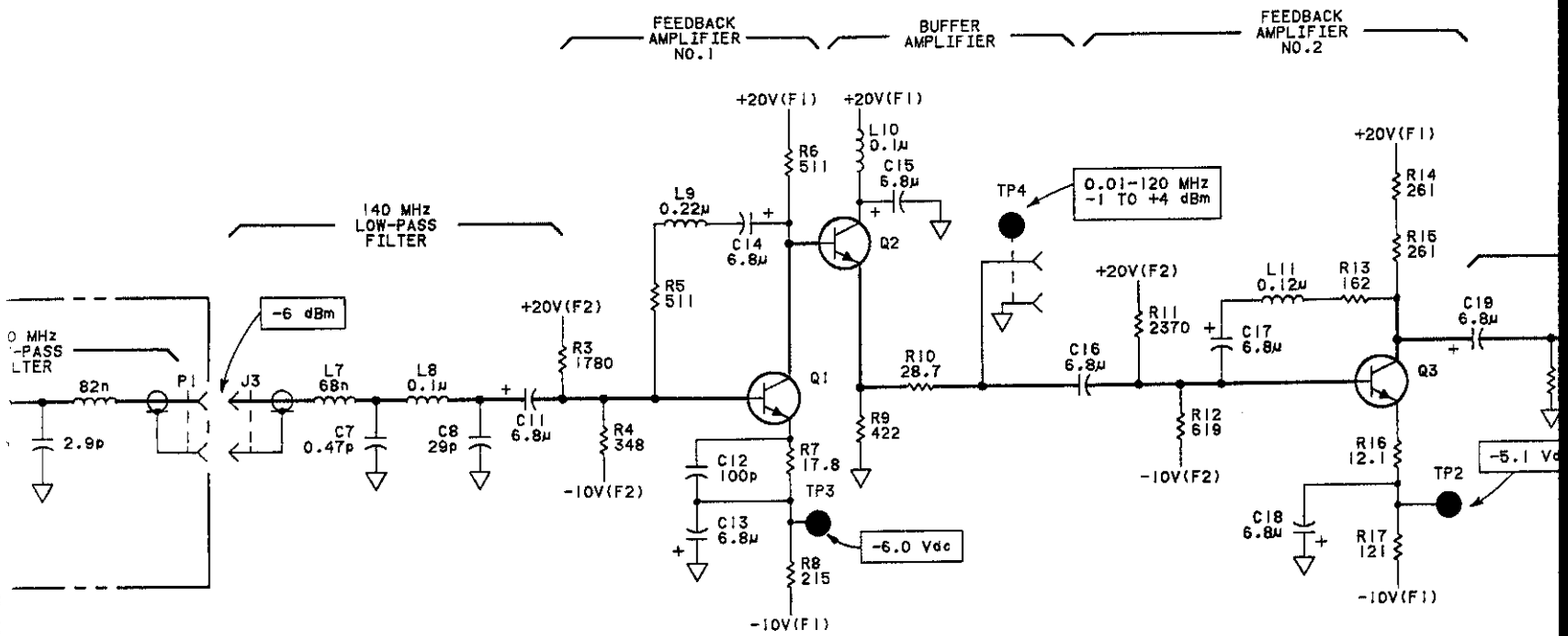


Fig 8-512
Sht 2 of 4

345)



+20V(F1)

+20V(F2)

C9
6.8μ

GND

-10V(1)

-10V(1)

Fig 8-512
Sht 30/4

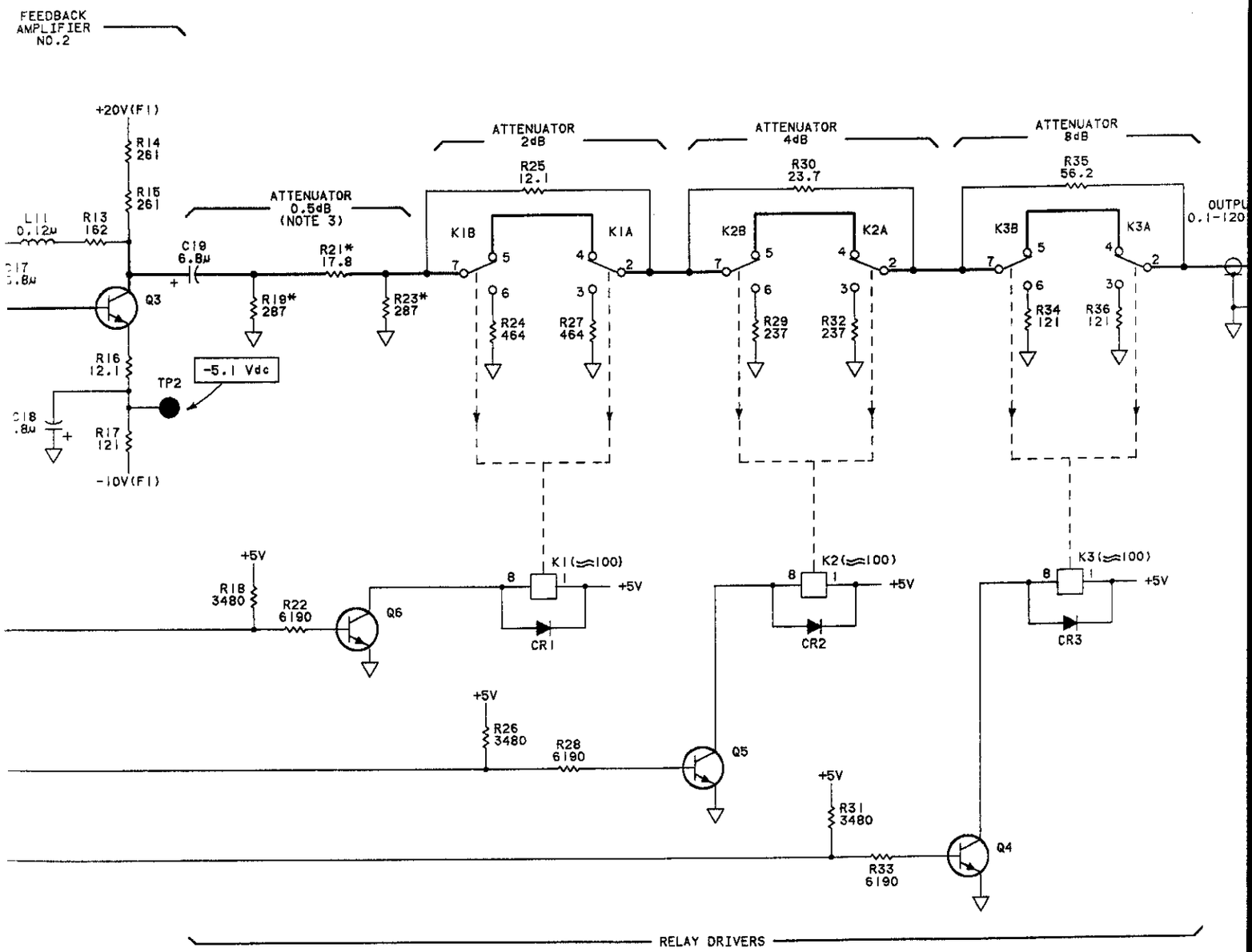
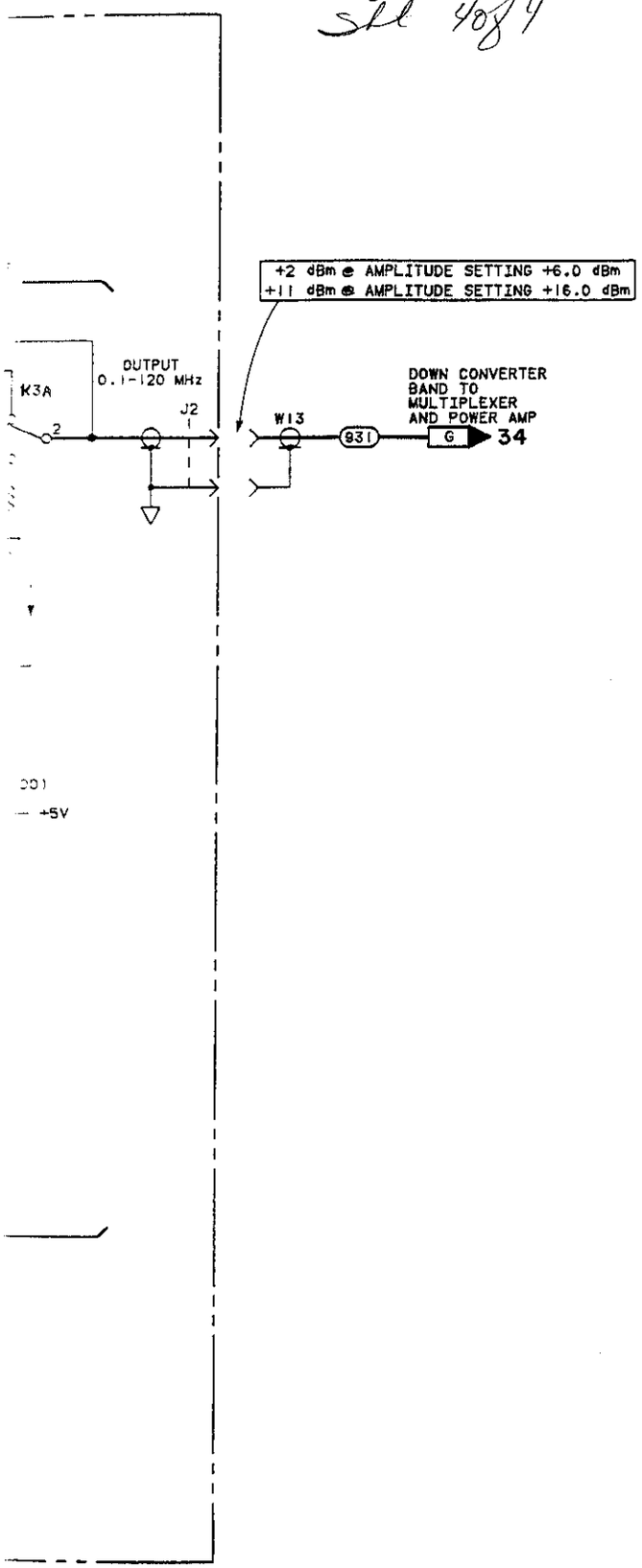


Fig 8-512
Sht 4 of 4



CAUTION

RF TEST POINTS (PC BOARD CUP CONNECTORS) MUST BE ACCOUPLED TO TEST EQUIPMENT. OTHERWISE DAMAGE MAY OCCUR TO THE TEST EQUIPMENT OR THE CIRCUIT UNDER TEST. USE THE SPECIAL CAPACITOR-COUPLED CABLE ADAPTER FOUND IN THE SERVICE KIT.

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. ASTERISK (*) INDICATES THAT THESE PARTS ARE SELECTED IN TEST. VALUES SHOWN ARE TYPICAL AND REPRESENT 3dB OF ATTENUATION. REFER TO SECTION V FOR PROCEDURES.

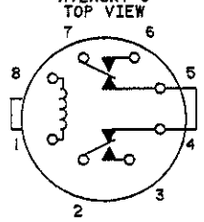
REFERENCE DESIGNATIONS

ND PREFIX	A12A5
W16,13 W81	J6 XA4A3
A12A3	
C1-19 CR1-3 FL1 J2-3 R1-3 L1-11 Q1-6 R1-19 R1-21,36 TP1-4	

TRANSISTOR PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1-2	1854-0247
Q3	1854-0721
Q4,5,6	1854-0477

A12A3K1-3
TOP VIEW



SERVICE SHEET A12A3 30

Figure 8-512. A12A3 LF Amplifier Schematic

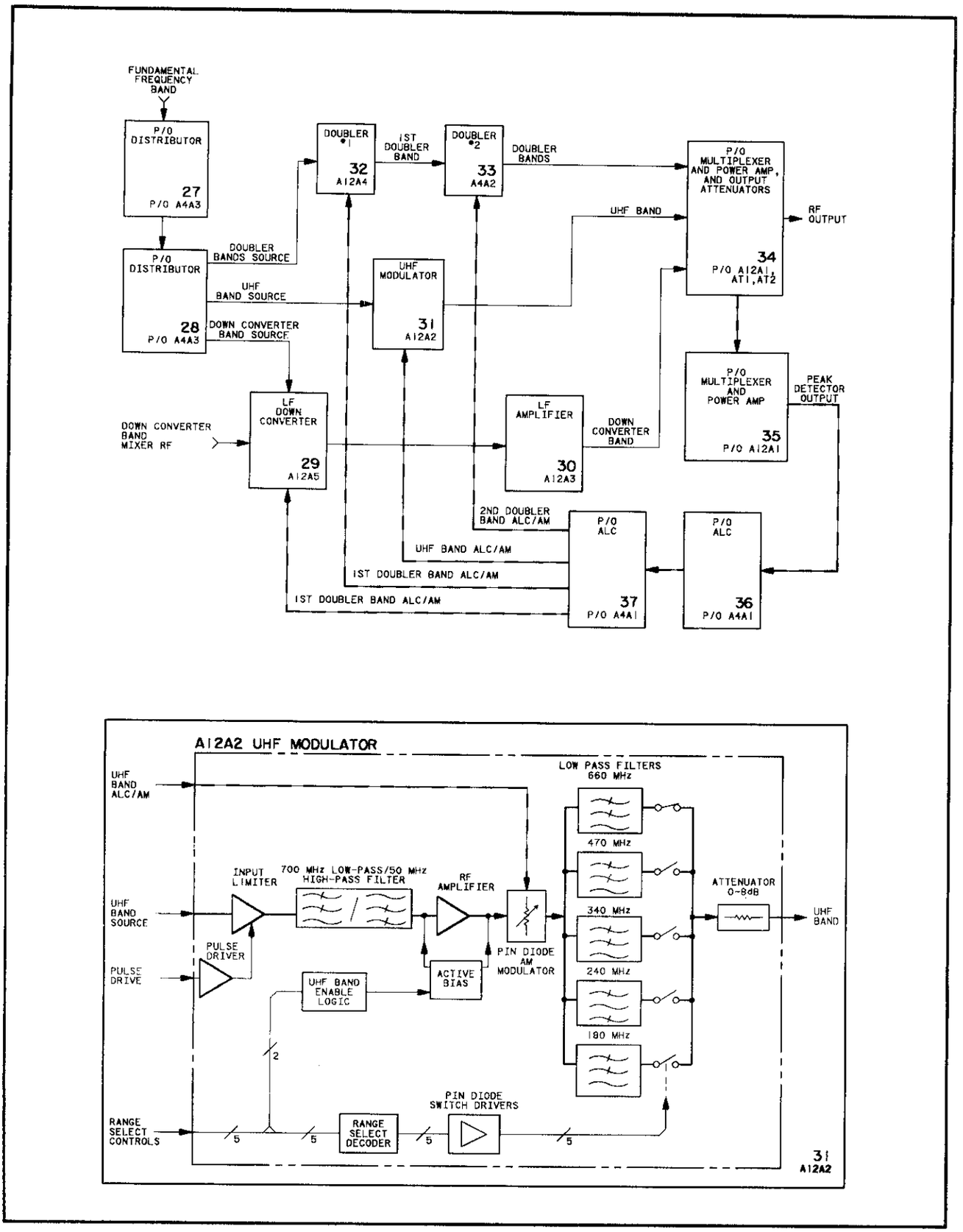


Figure 8-513. A12A2 UHF Modulator Block Diagrams

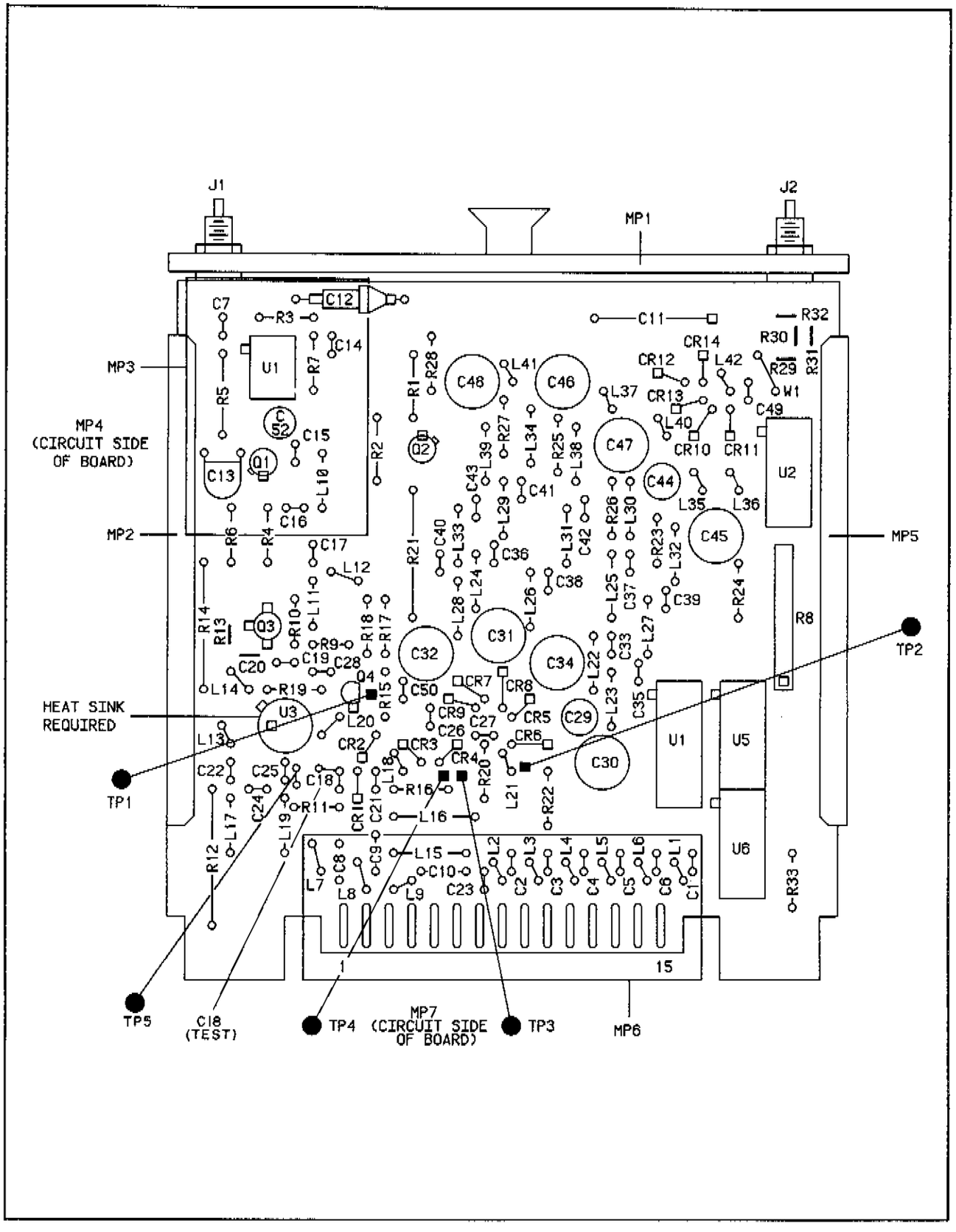


Figure 8-514. A12A2 UHF Modulator Component Locator

CHANGES

All serial prefixes

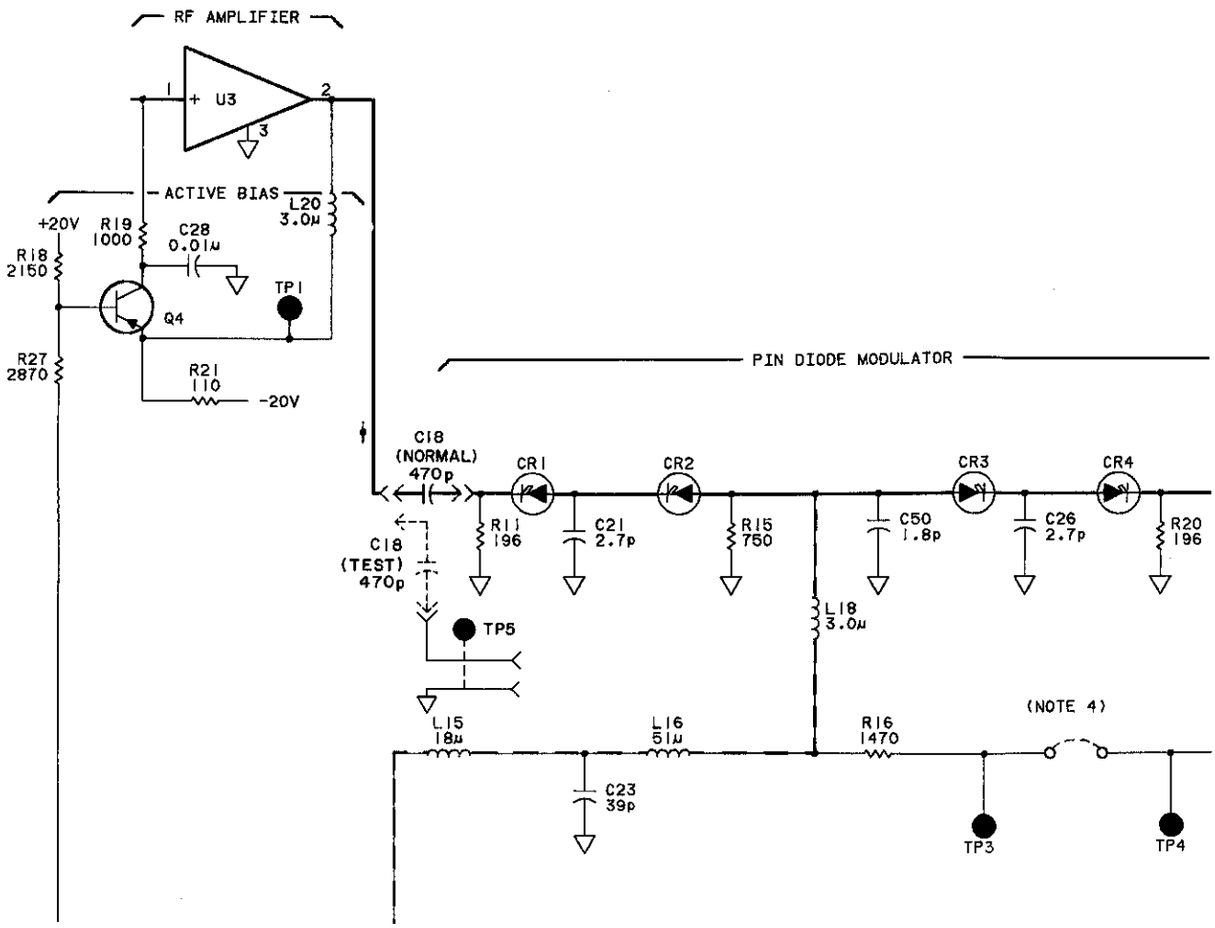
On the A12A2 schematic:

- A12A2 - Modify the schematic as shown in the partial schematic "P/O Figure 8-515. UHF Modulator Schematic" on page 8-522.3.
- A12A2C51 - Delete C51.
- A12A2R16 - Change the value of R16 to 3.16k.
- A12A2R18 - Change the value of R18 to 1.1k.
- A12A2R27 (R17) - There are two resistors labeled R27. Change the label of the R27 resistor connected to the base of Q4 to R17 and change its value to 1.47k.
- A12A2L11, R9, R11 - Add an asterisk (*) to L11, R9, and R11, to indicate factory selected components.
- A12A2L11*, R9*, R11* - Add "(NOTE 6)" next to the reference designators R9, L11, and R11.

On the schematic:

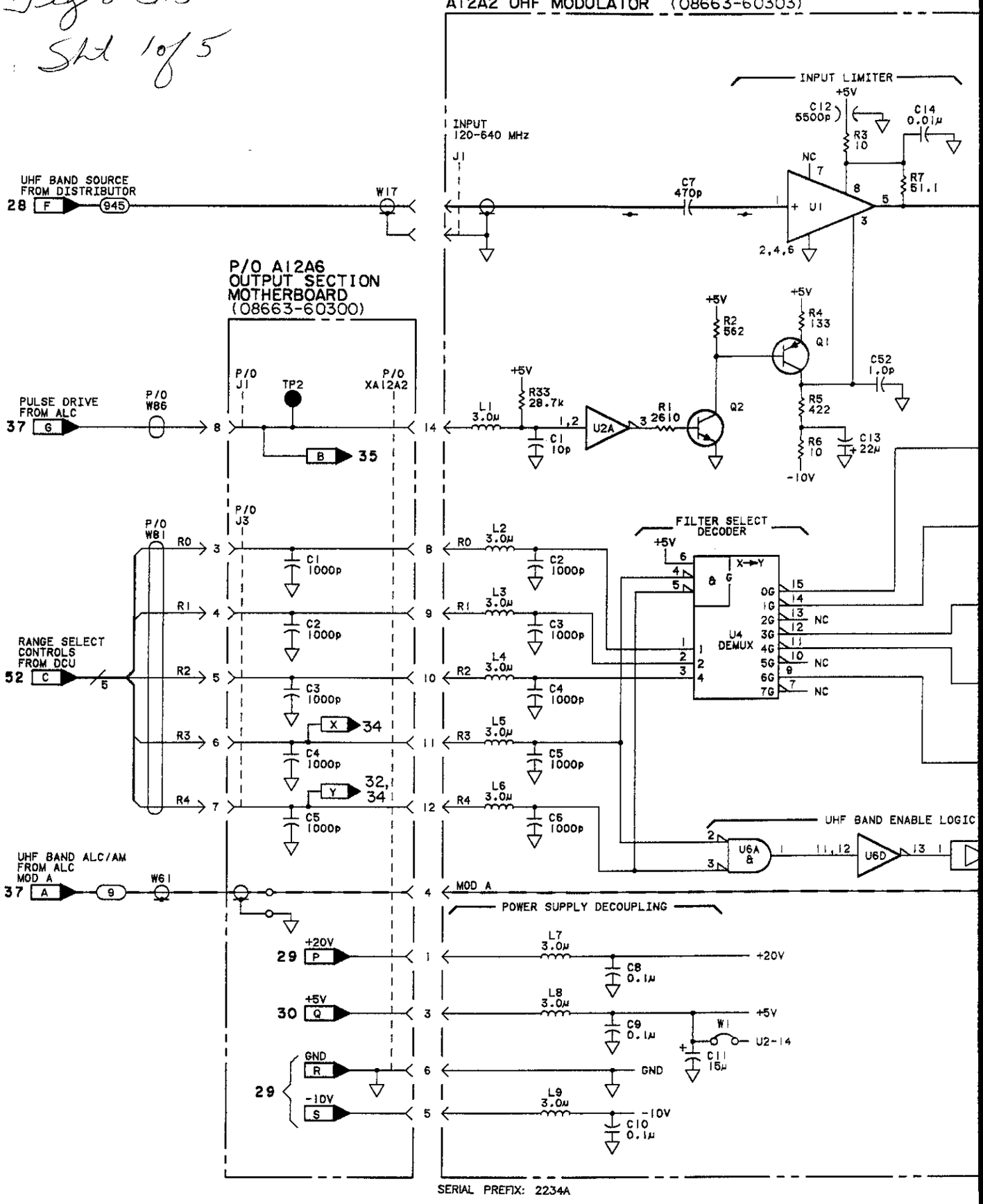
- NOTES - Add note 6 as follows:

  6. These factory selected components are connected to circuit by sockets.



P/O Figure 8-515. *A12A2 UHF Modulator Schematic*

Fig 8-515
Sht 1 of 5



SERIAL PREFIX: 2234A

Fig 8-515 Sht 2 of 5

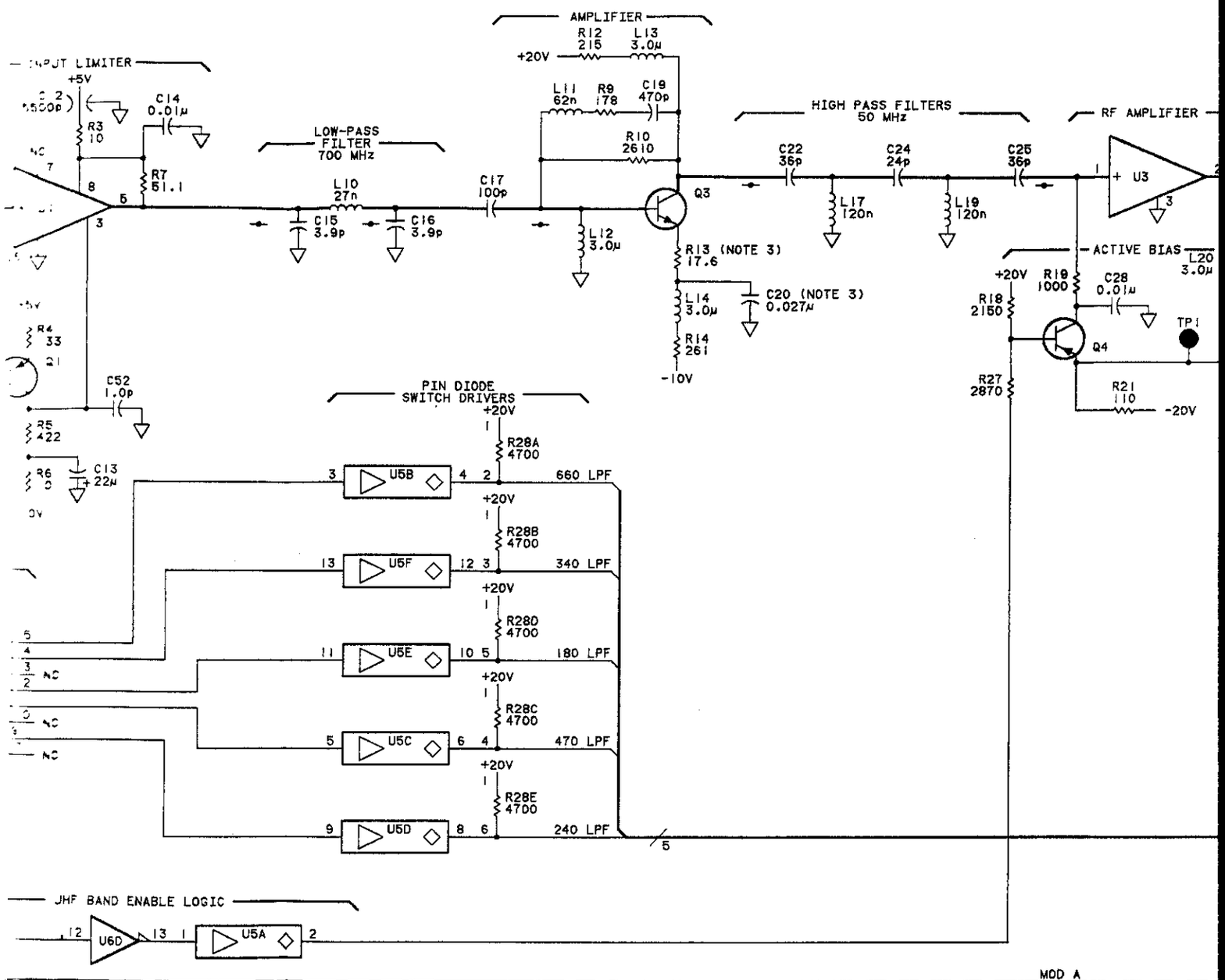
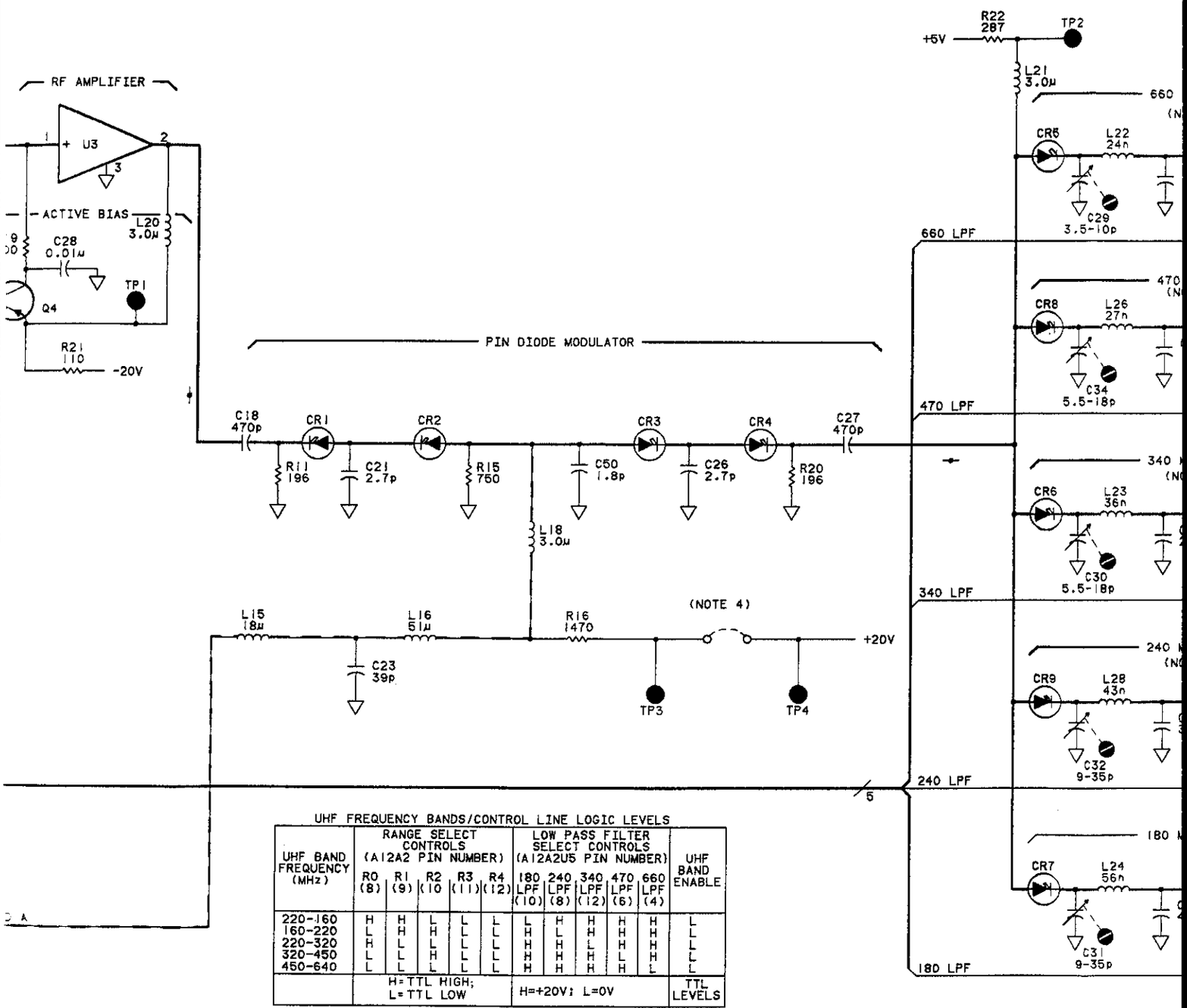


Fig 8-515 Sht 3 of 5



UHF FREQUENCY BANDS/CONTROL LINE LOGIC LEVELS

UHF BAND FREQUENCY (MHz)	RANGE SELECT CONTROLS (A12A2 PIN NUMBER)					LOW PASS FILTER SELECT CONTROLS (A12A2U5 PIN NUMBER)					UHF BAND ENABLE
	R0 (8)	R1 (9)	R2 (10)	R3 (11)	R4 (12)	180 LPF (10)	240 LPF (8)	340 LPF (12)	470 LPF (6)	660 LPF (4)	
220-160	H	H	L	L	L	L	H	H	H	H	L
160-220	L	H	H	L	L	H	L	H	H	H	L
220-320	H	L	L	L	L	H	H	L	H	H	L
320-450	L	L	H	L	L	H	H	H	L	H	L
450-640	L	L	L	L	L	H	H	H	H	L	L
	H=TTL HIGH; L=TTL LOW					H=+20V; L=0V					TTL LEVELS

Fig 8-515 Sht 4 of 5

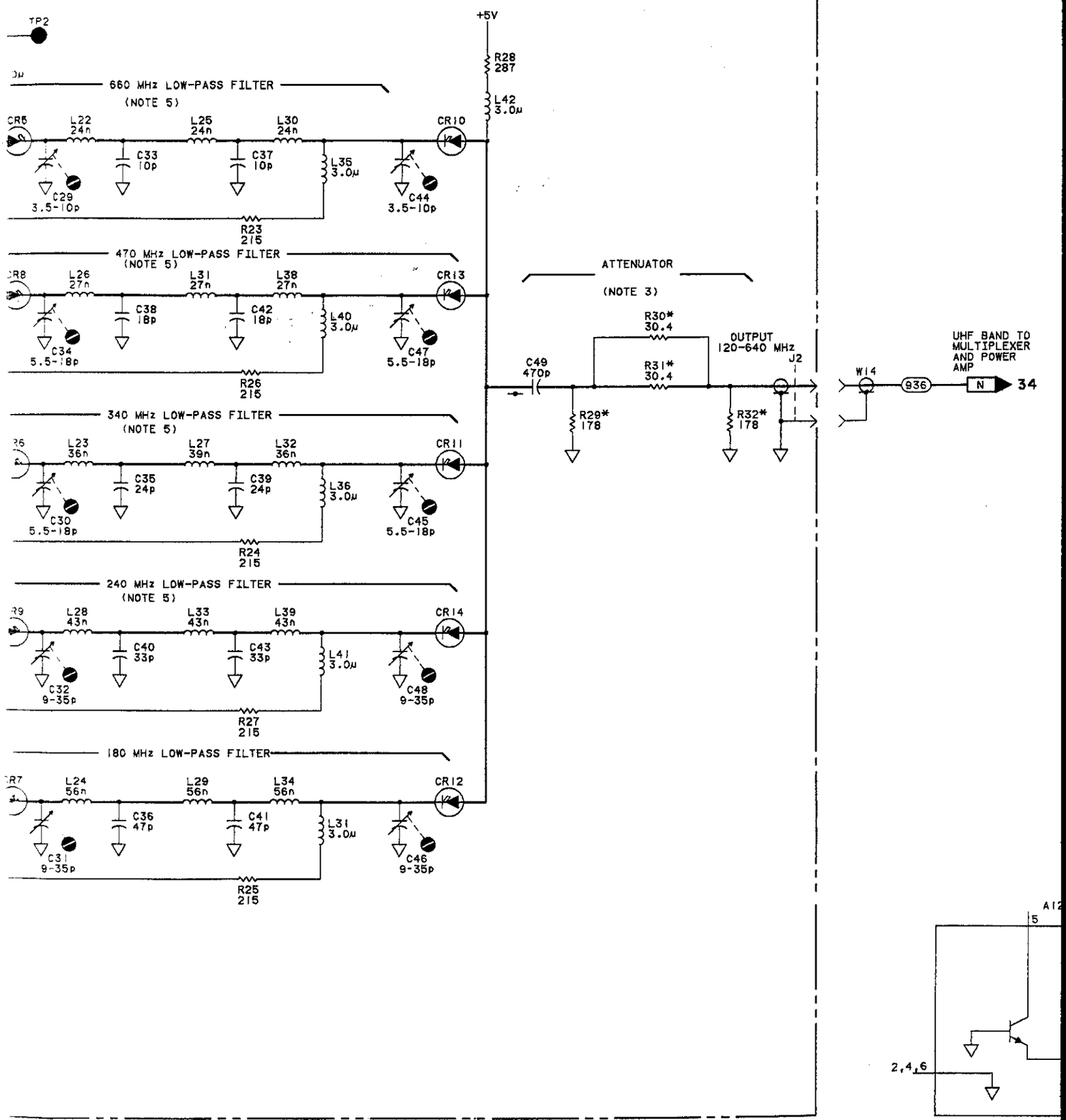
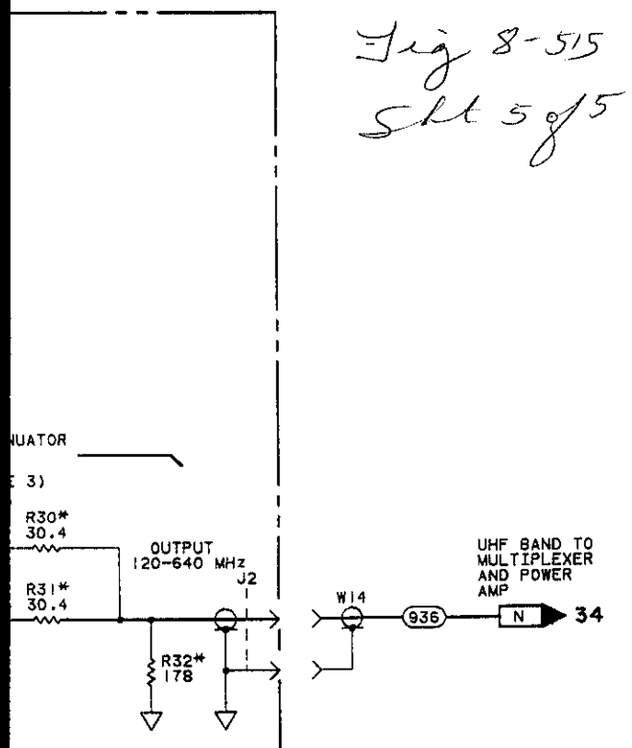


Fig 8-515
Sht 5 of 5

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. THE SMALL CHIP COMPONENTS ON THIS ASSEMBLY REQUIRE LOW TEMPERATURE SOLDERING TECHNIQUES. USE SILVER SOLDER.
4. JUMPER WIRE IS INSTALLED FOR TROUBLESHOOTING PURPOSES ONLY TO TURN PIN DIODE MODULATOR FULLY ON.
5. VARIABLE CAPACITORS AT INPUT AND OUTPUT NODES OF LOW-PASS FILTERS PROVIDE FOR FILTER RESPONSE ADJUSTMENT. SEE SECTION V FOR PROCEDURES.



LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	< +0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1	1853-0405
Q2	1854-0809
Q3	1854-0720
Q4	1853-0459
U1	1826-0372
U2	1820-0681
U3	08662-67002
U4	1820-1216
U5	1820-0668
U6	1820-1144

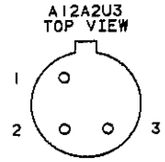
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U2,5,6	+5V - 14 ▽ - 7
U4	+5V - 16 ▽ - 8

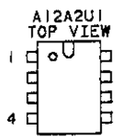
REFERENCE DESIGNATIONS

NO PREFIX	

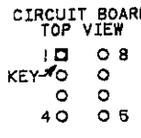
A12A2U3
TOP VIEW



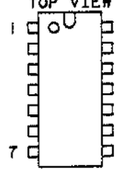
A12A2U1
TOP VIEW



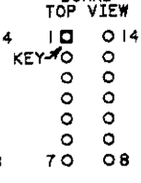
CIRCUIT BOARD
TOP VIEW



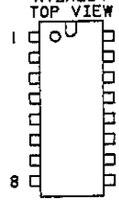
A12A2U2,5,6
TOP VIEW



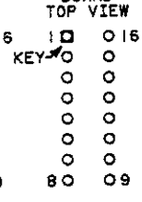
CIRCUIT
BOARD
TOP VIEW



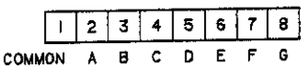
A12A2U4
TOP VIEW



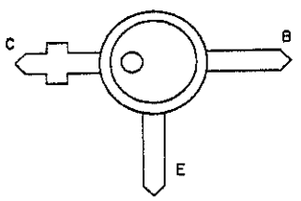
CIRCUIT
BOARD
TOP VIEW



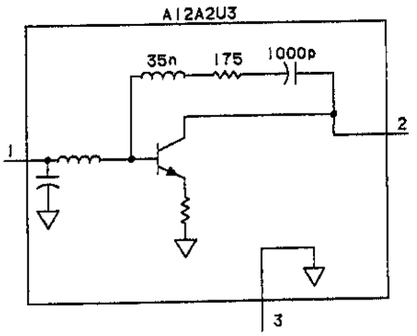
A12A2R28
TOP VIEW



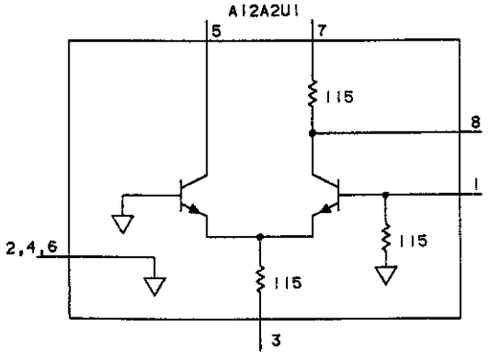
A12A2Q3
TOP VIEW



A12A2U3



A12A2U1



SERVICE SHEET 31
A12A2

Figure 8-515. A12A2 UHF Modulator Schematic

SERVICE SHEET 32
A12A4 DOUBLER #1

REFERENCE BLOCK DIAGRAM 6
Table 4-1. Recommended Performance Tests After Adjustments or Repairs
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Doubler #1 Board doubles the basic band frequency from the Distributor Board so that the 640 MHz to 1280 MHz frequency range can be generated.

Doubler Filter Microcircuit (A12A4U2)

The doubler band frequency enters the doubler filter (a microcircuit which is located on the A12A4 board) at J1. The input frequency is 320 MHz to 640 MHz (at +1.75 dBm) The signal is first amplified and then sent to the doubler. Following the doubler is a voltage-tuned filter. This is a bandpass filter made of varactor diodes in a back-to-back arrange (to minimize harmonic generation).

The last block in A12A4U2 is the final amplifier stage. The signal enters it from the voltage-tuned filter at 0 dBm and is amplified to +10 dBm. The output of this amplifier is sent to the modulator filter (A12A4U3) through a coaxial cable.

Modulator Filter (A12A4U3)

The output signal from J2 of A12A4U2 enters A12A4U3J1. The first stage in this microcircuit is the voltage-tuned filter. Following this is a pi-type PIN modulator. The PIN diodes behave as RF resistors. Their resistance is controlled by the amount of dc bias current flowing through them. The amount of control current used by the modulator varies from 0mA to 5mA. Following the modulator is another amplifier. The output from it is 640 MHz to 1280 MHz at +5 dBm maximum (depending on the modulator settings).

ALC and Doubler Enable Circuitry

The ALC circuitry controls the gain of the modulator in microcircuit A12A4U3 so that the Generator's RF output is constant. The ALC signal comes from the ALC board (service sheet 37) and enters the Doubler Assembly via pin 6. The doubler in microcircuit A12A4U2 is enabled by the Doubler #1 enable circuitry found on the Doubler #1 Board. The signals which control this circuit come from the DCU.

Filter Tuning Circuitry

The tune voltages for the two voltage-tuned filters, one in the Doubler-Filter U2 and the other in the Modulator-Filter U3, are developed by the ROM U4 and the D/A Converter U5 working in conjunction with the Doubler-Filter Tracking Amplifier U1A and the Modulator-Filter Tracking Amplifier U1B.

Information for the automatic correction of the tuning curves for each of the voltage-tuned filters is stored in the ROM U4. This information is used to determine which frequencies will be passed or rejected by the two voltage-tuned filters. Each filter can be programmatically advanced in 2 MHz steps from 640 MHz to 1280 MHz. The actual frequency selection signals that address the data stored in ROM come from the DCU. The ROM output is enabled at the same time as the doubler in U2. Although the addresses that select the ROM outputs to the D/A Converter cannot be listed in a truth table. The ROM address lines can be incremented by placing the instrument in the sweep mode. Verification can be made by stepping the frequency in 2 MHz increments from 640 MHz to 1280 MHz while monitoring the doubler band output on a spectrum analyzer at J2. It should be noted that the frequency will still increment even if the filter is not working.

CAUTION

The output of J2 is at a dc level of about +12 Vdc. Some spectrum analyzers are dc coupled and cannot be connected directly to this output. If the input of the spectrum analyzer is dc coupled, a blocking capacitor adapter must be used in series with the input or damage will occur.

NOTE

Any time either one or both of the microcircuits U2 or U3 are replaced, a new ROM U4 must also be replaced. Any non-linearities that exist within the two microcircuits are accounted for when the ROM is programmed. The data stored in the ROM is unique to the two microcircuits. Therefore, a new ROM must be programmed whenever either microcircuit is replaced.

Transistor Q3 forms a constant reference voltage source which can be adjusted by the DOUBLER-FILTER TRACKING HIGH pot R29. This source provides the voltage reference to the D/A Converter U5 which determines the maximum frequency pass band of the voltage-tuned filter in the Doubler-Filter U2. The ROM output is used by the D/A Converter to attenuate this reference voltage and produce a current which will track the tuning curves of the voltage-tuned filters.

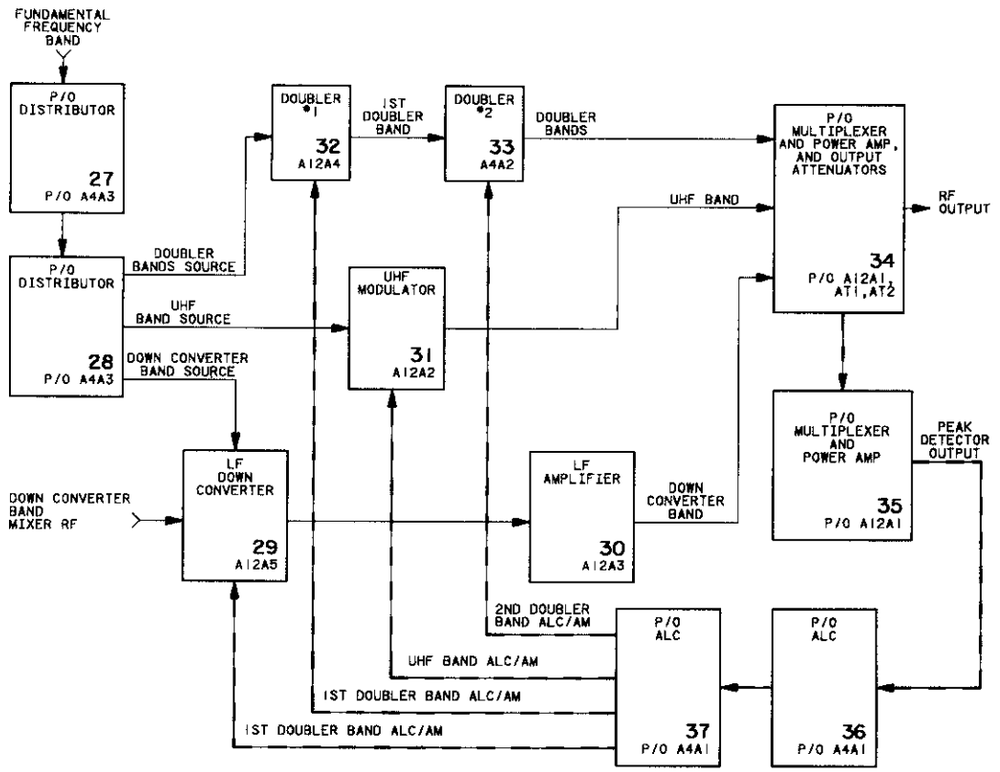
This current is coupled to the input of the Doubler-Filter Tracking Amplifier U1A where it is converted into the tune voltage for the

voltage-tuned filter in the Doubler-Filter U2. The DOUBLER-FILTER TRACKING LOW pot R40 sets the lower limit for this tune voltage.

The tune voltage from the Doubler-Filter Tuning Amplifier U1A is also coupled to the input of the Modulator-Filter Tracking Amplifier U1B. The MODULATOR-FILTER TRACKING LOW pot R56 sets the lower limit for the tune voltage to the voltage-tuned filter in the Modulator-Filter U3, while the MODULATOR-FILTER TRACKING HIGH pot R58 sets the upper limit.

TROUBLESHOOTING

This assembly contains a unique ROM (U4) which is programmed at the factory to match the voltage-tuned filters in the two microcircuits. If the ROM or either microcircuit fails, the entire A12A4 Doubler #1 assembly must be replaced. A rebuilt assembly is available (see section VI, Replaceable Parts, for part number). All other parts can be replaced. It is more economical to replace components where possible.



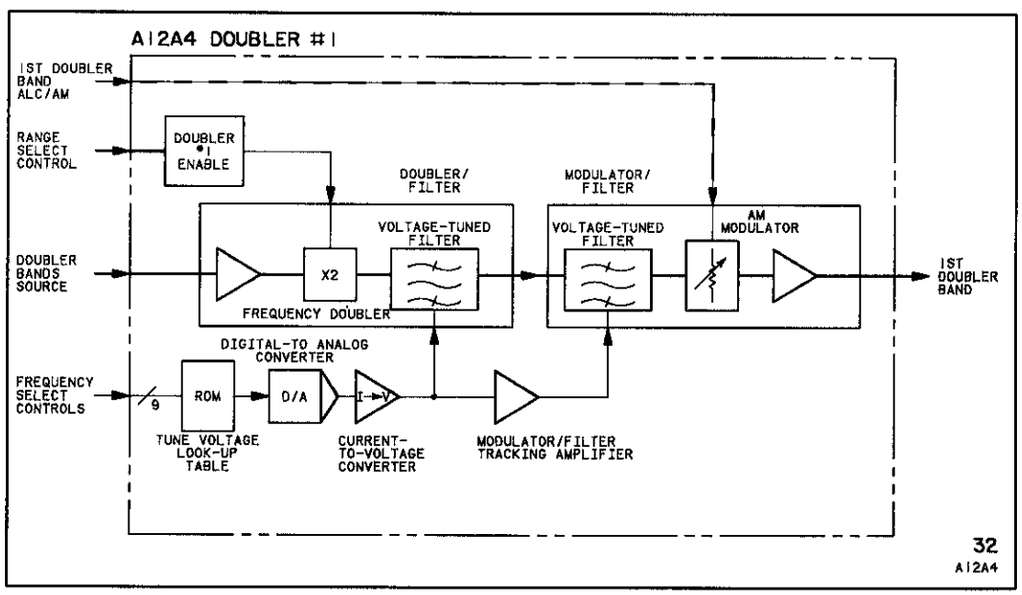


Figure 8-516. A12A4 Doubler #1 Block Diagrams

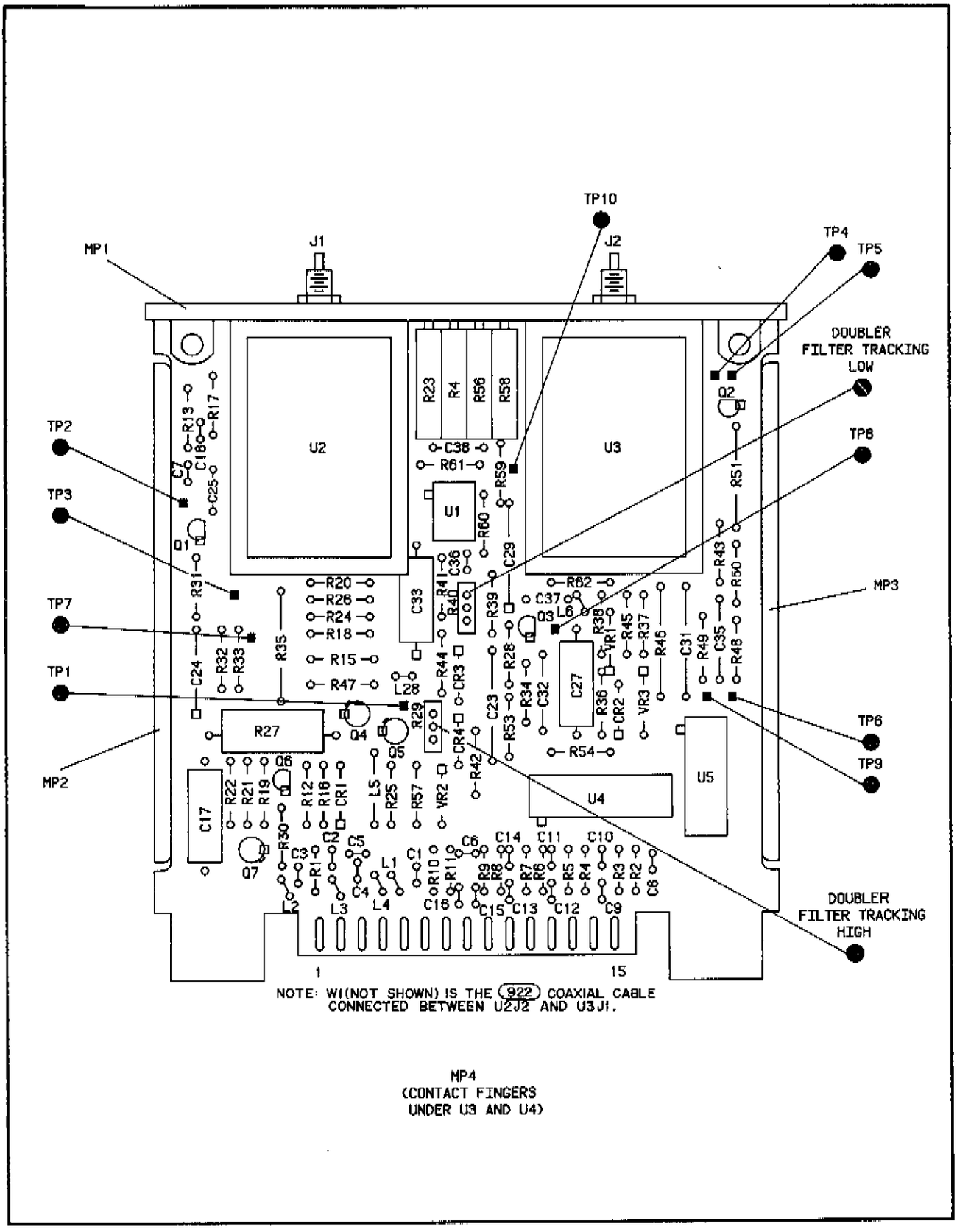
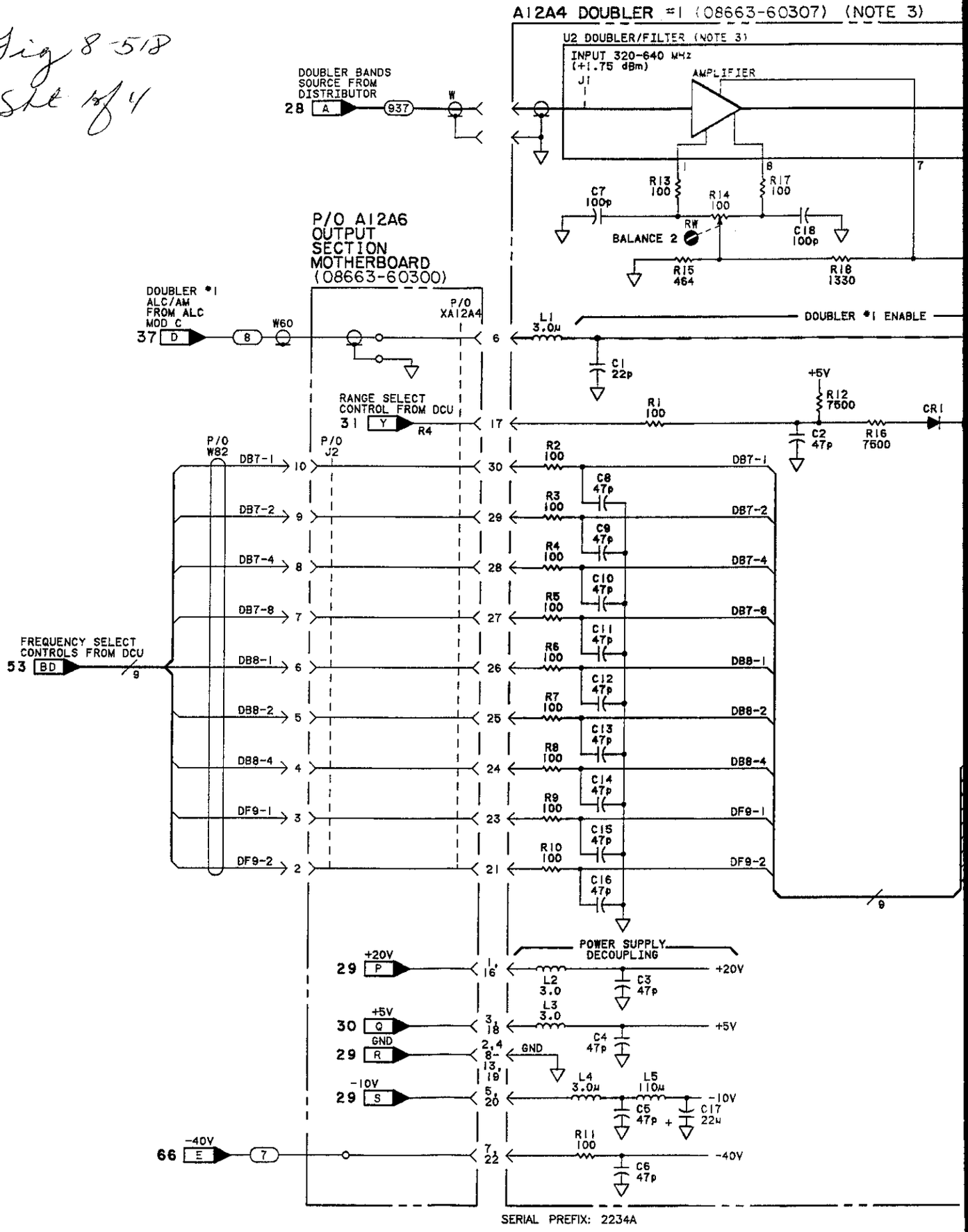


Figure 8-517. A12A4 Doubler #1 Component Locator

CHANGES

2824A and above	**On the A12A4 schematic:** • A12A4R43 - In the upper right hand corner of the schematic locate R43 under BIAS and change its value to 4.22k.
All Serial Prefixes	**On the A12A4 Schematic:** • R39 - Change the value of R39 to 17.8k.

Fig 8-51B
Sht 3 of 4



.07) (NOTE 3) Fig 8-518 Sht 2 of 4

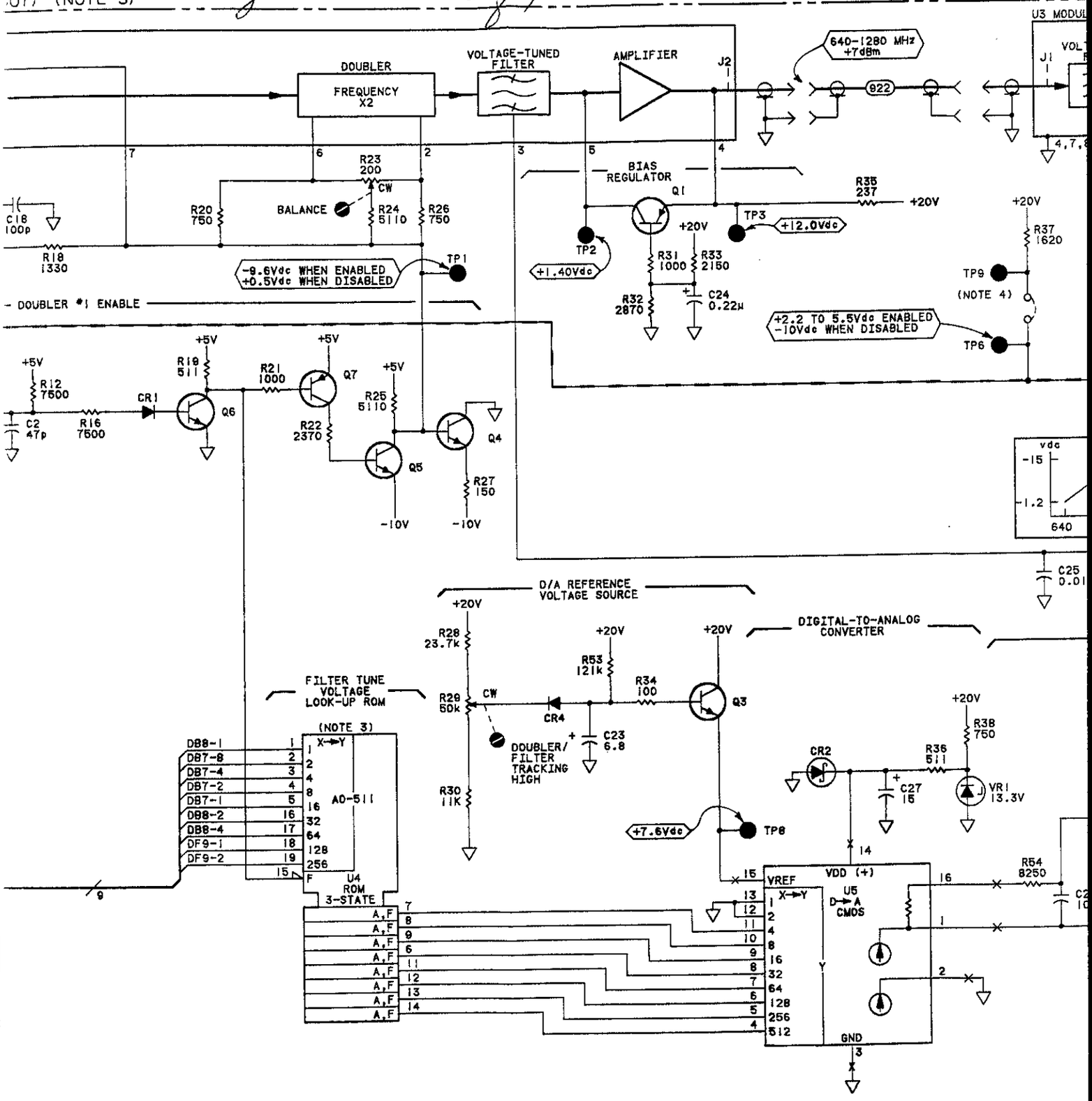
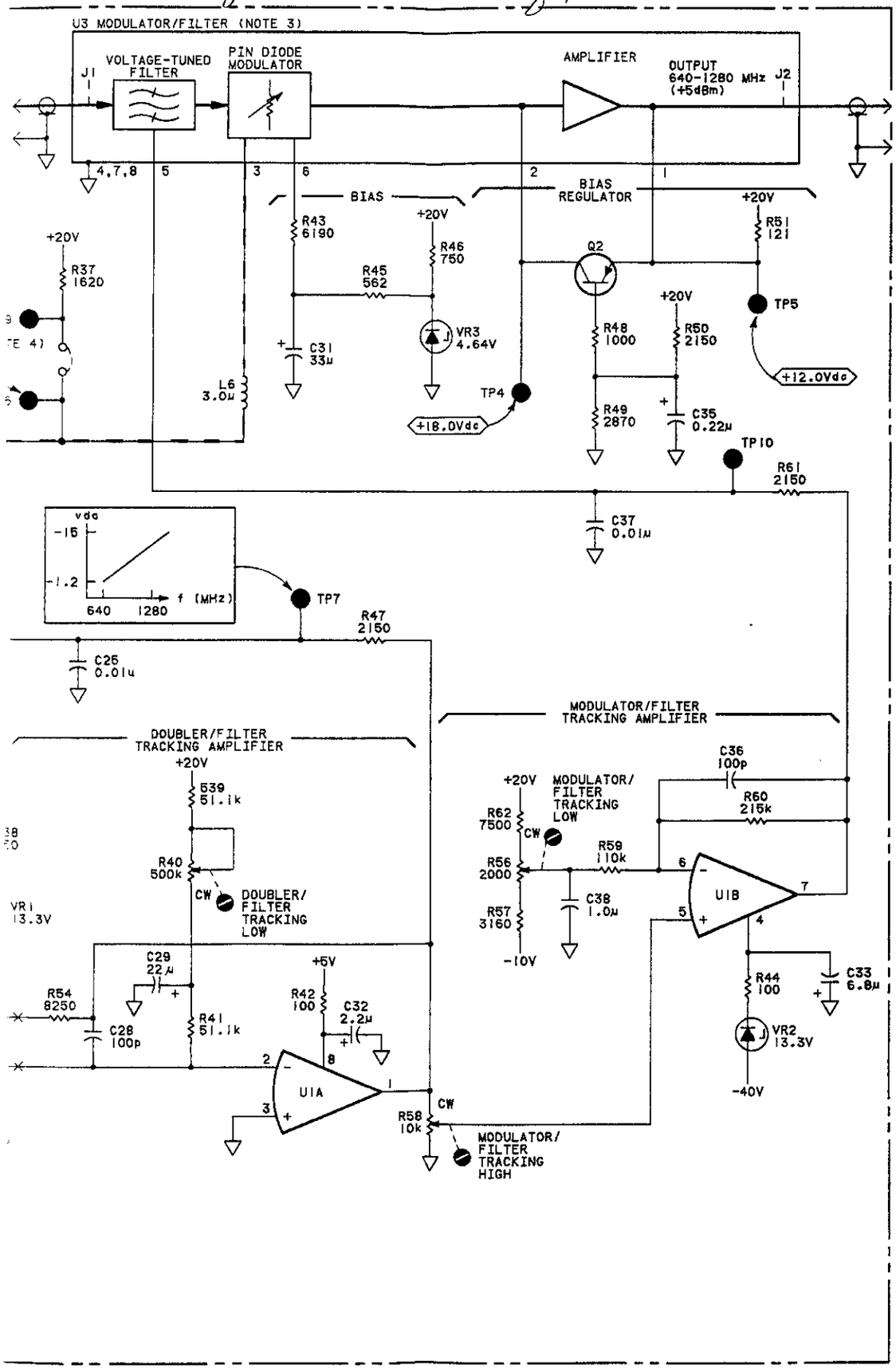


Fig 8-518 Sht 3 of 4



THE OUTPUT OF A
TO TEST EQUIPME
OCCUR TO TEST E
UNDER TEST.

1. REFER TO TAB
DIAGRAM NOTE
2. TROUBLESHOOT
THEY ARE ACT
YOUR MEASURE
DIFFERENT TH
3. MICROCIRCUIT
ARE NOT SEPA
IF ONE OF TH
EXCHANGE PC
4. JUMPER WIRE
SHOOTING TO
FULLY ON.

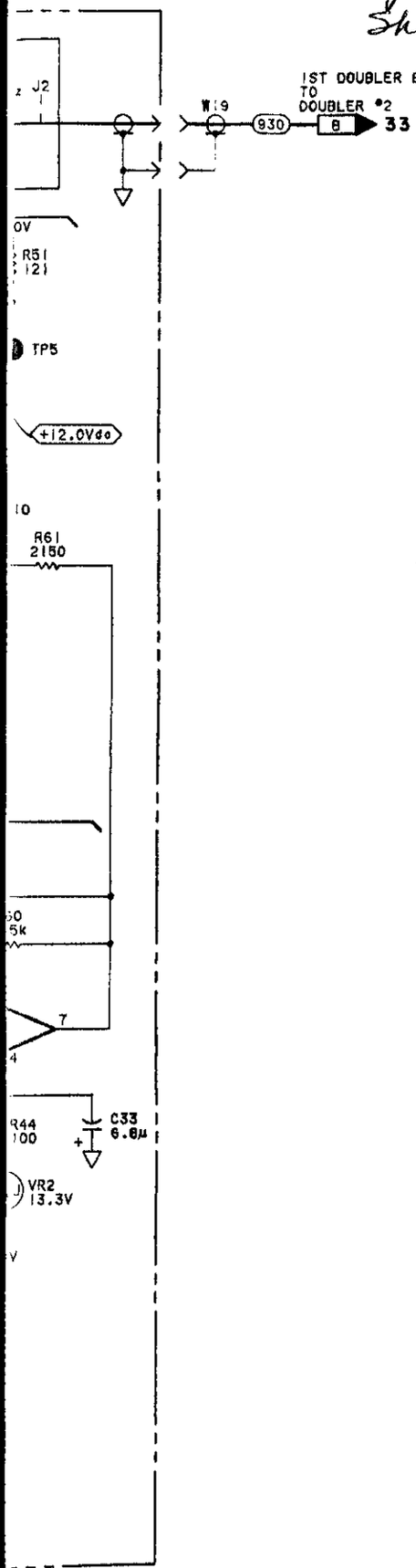
† BACKDATING I

REFERE
NO PRE
W
A12A
C1-18,2 27-29,3 35-38 CR1,2,4 L1-6 Q1-7 R1-5,1 56-62

REFERE DESIGNAT
Q1,2,7 Q3-6
U1 U2-4 U5

REFERE DESIGNAT
U4

Fig 8-518
Sht 4 of 4



⚠ CAUTION

THE OUTPUT OF A12A4U3 MUST BE AC-COUPLED TO TEST EQUIPMENT. OTHERWISE DAMAGE MAY OCCUR TO TEST EQUIPMENT OR THE CIRCUIT UNDER TEST.

NOTES

1. REFER TO TABLE 8- FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. MICROCIRCUITS U2 AND U3, AND ROM U4 ARE NOT SEPARATELY REPLACEABLE. IF ONE OF THESE FAIL, ORDER AN EXCHANGE PC BOARD HP 08662-60293.
4. JUMPER WIRE INSTALLED FOR TROUBLESHOOTING TO TURN THE MODULATOR FULLY ON.

† BACKDATING INFORMATION IN SECTION VII

REFERENCE DESIGNATIONS

NO PREFIX	A12A4 CONT.
W	TP1-10 U1-5 WR1-3
A12A4	A12A6
C1-18,23-25 27-29,31-33 35-38 CR1,2,4 L1-6 Q1-7 R1-51,53,54 56-62	J XA12A4

LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,2,7 Q3-6	1853-0020 1854-0071
U1 U2-4 U5	1826-0547 (NOTE 3) 1826-0921

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U4	+5V - 20 ⏚ - 10

SERVICE SHEET 32

A12A4

Figure 8-518. A12A4 Doubler #1 Schematic

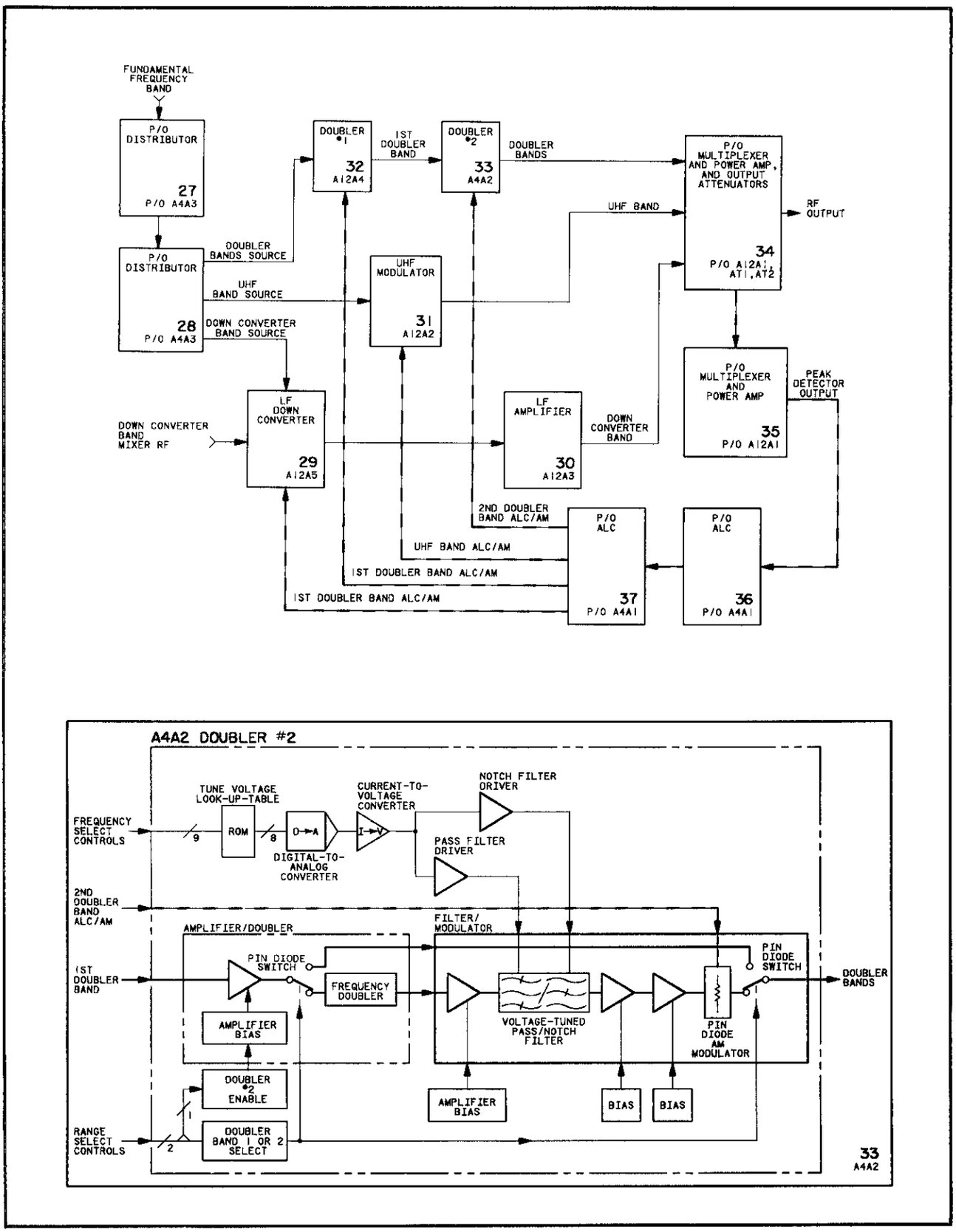


Figure 8-519. A4A2 Doubler #2 Block Diagrams

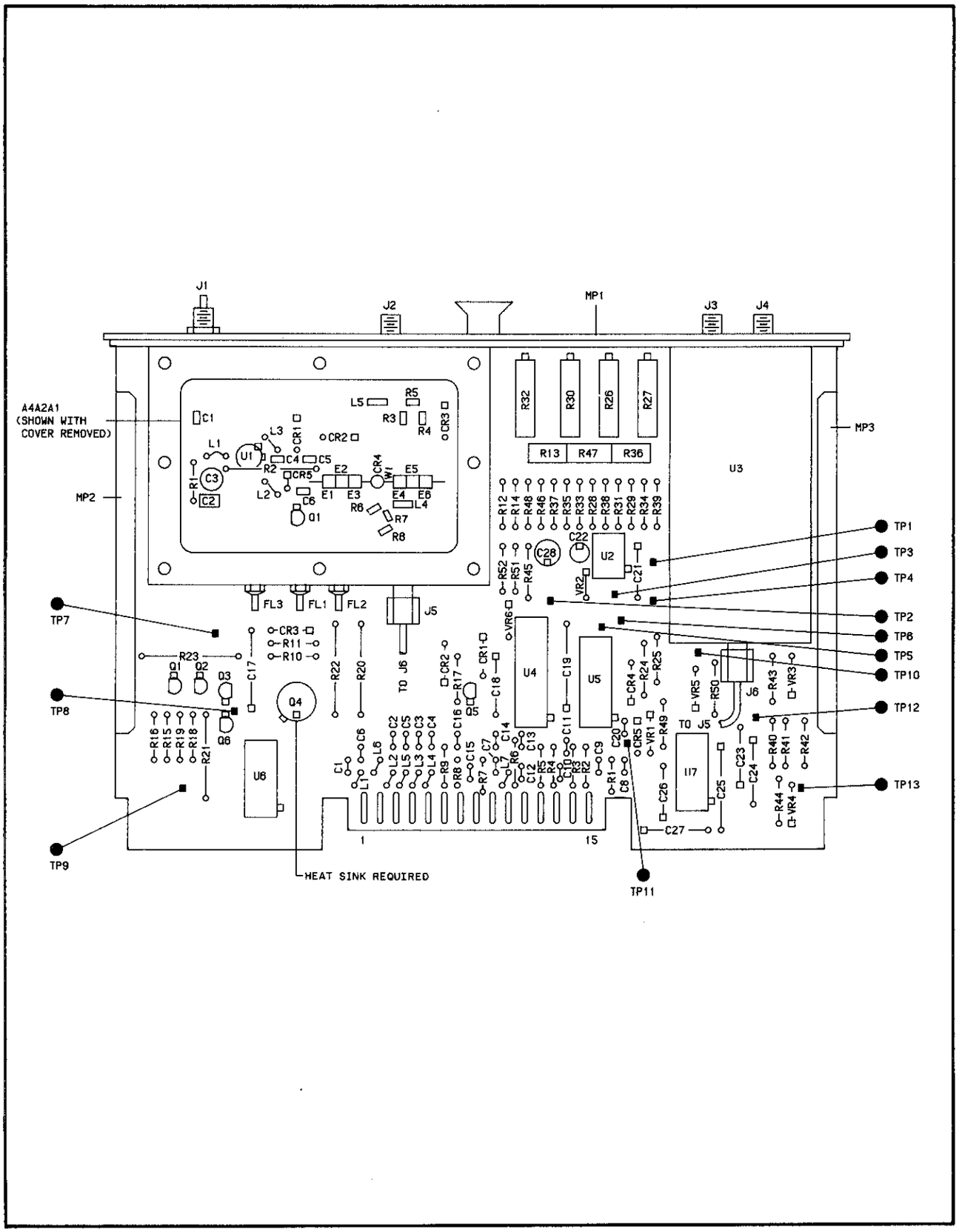


Figure 8-520. A4A2 Doubler #2 Component Locator

CHANGES

All serial prefixes	On the A4A2 schematic: • A4A2U5 - In the table of Transistor and Integrated Circuit Part Numbers, change the part number of U5 to 1826-0921. • W39 -Assign reference designator W39 to the coaxial cable connecting A4A2A1 FREQ X1 output to U3 640-1280 MHz input. • W1 - Assign refernce designator W1 to the coaxial cable connecting A4A3A1 FREQ X2 output to U3 1280-2560 MHz input. • U3 - On U3 (AMP/FILT/MOD) locate *OUTPUT AMPLIFIER* and change U3 pin 2 signal path to U7D pin 12. Change U3 pin 9 signal path (FET gate) to U7D pin 14 (through R50). • U7B - Under **DRIVER AMPLIFIER BIAS REGULATOR**, connect U7B pin 8 to the gate of the *U3 DRIVER AMPLIFIER* and connect U7B pin 3 to the drain of the *U3 DRIVER AMPLIFIER*.
2248A and above	On the A4A2 Component Locator: • - Use the A4A2 component locator on page 8-534.3. On the A4A2 schematic: • - Change the part number of the A4A2 Assembly to 08663-60351.
2840A and above	On the A4A2 schematic: • R26, R28, R33, R38 - In the center of the schematic under **PASS FILTER DRIVER**, locate and change the value of R26 to 20K, R28 to 13.3K, R33 to 42.2K, and, R38 to 17.8K.

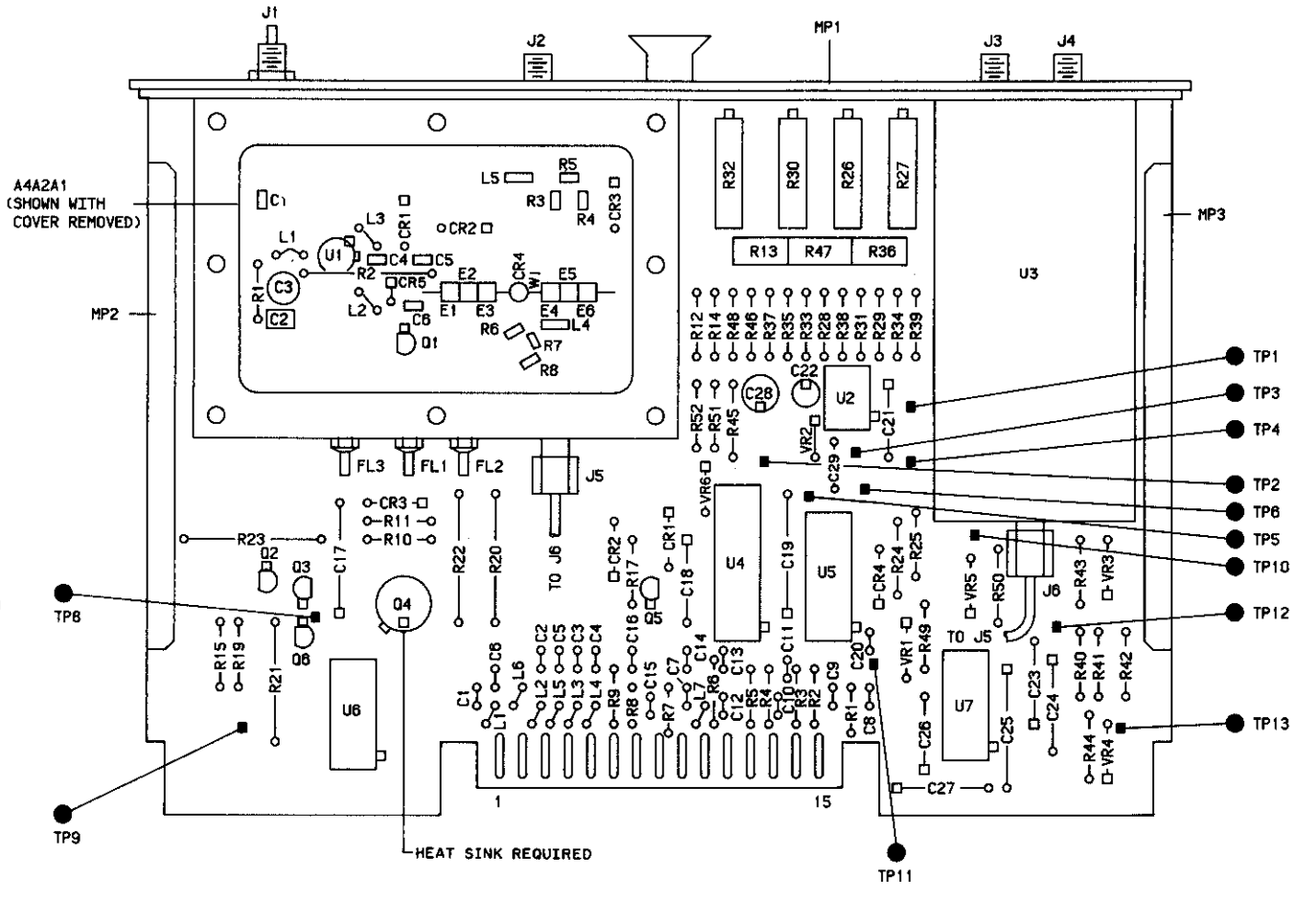
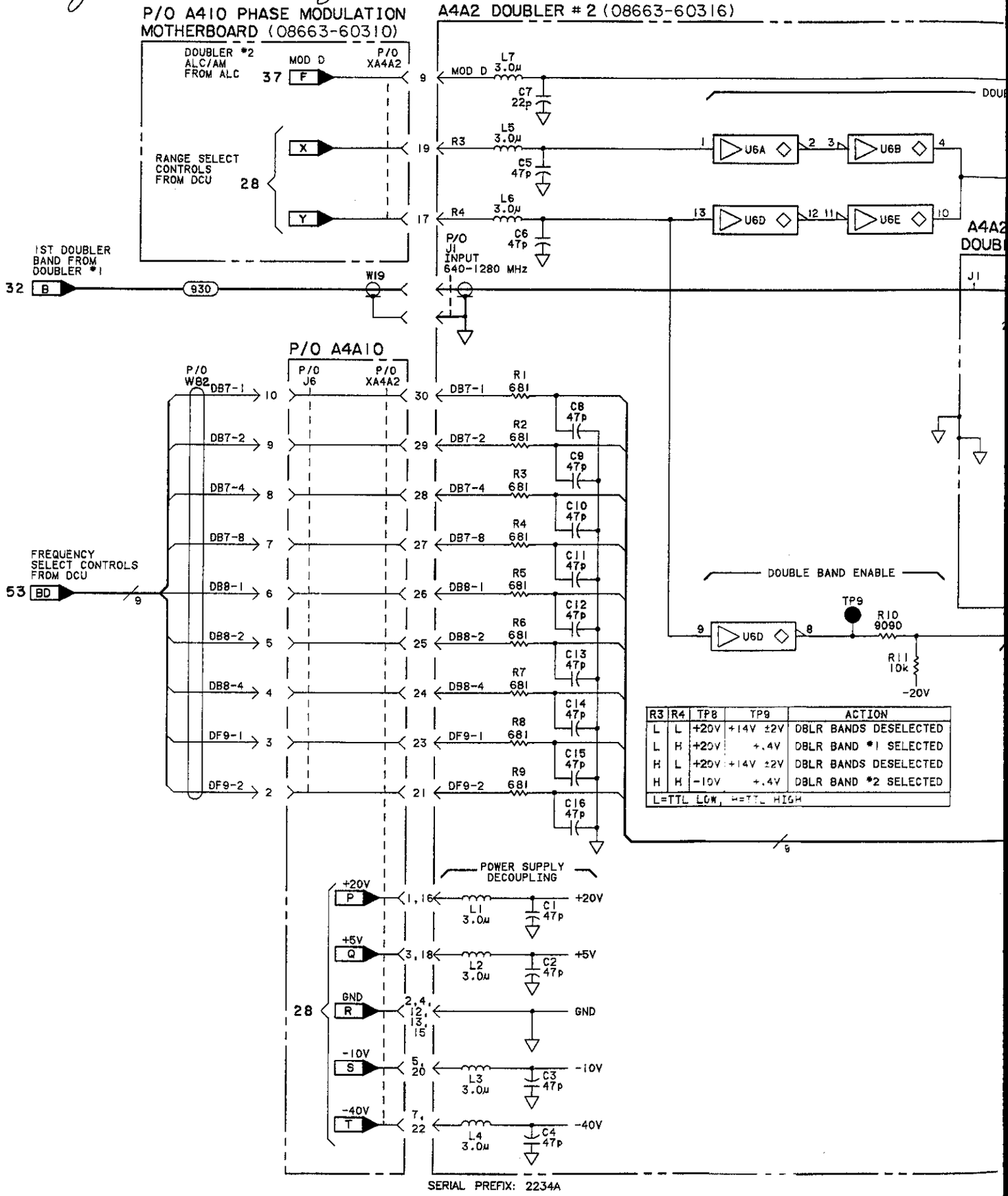


Figure 8–520. *A4A2 Doubler #2 Component Locator (2248A)*

Fig 8-521 Sht 1 of 5



R3	R4	TP8	TP9	ACTION
L	L	+20V	+14V ±2V	DBLR BANDS DESELECTED
L	H	+20V	+.4V	DBLR BAND #1 SELECTED
H	L	+20V	+14V ±2V	DBLR BANDS DESELECTED
H	H	-10V	+.4V	DBLR BAND #2 SELECTED

L=TTL LOW, H=TTL HIGH

Fig 8-521 Sht 2 of 5

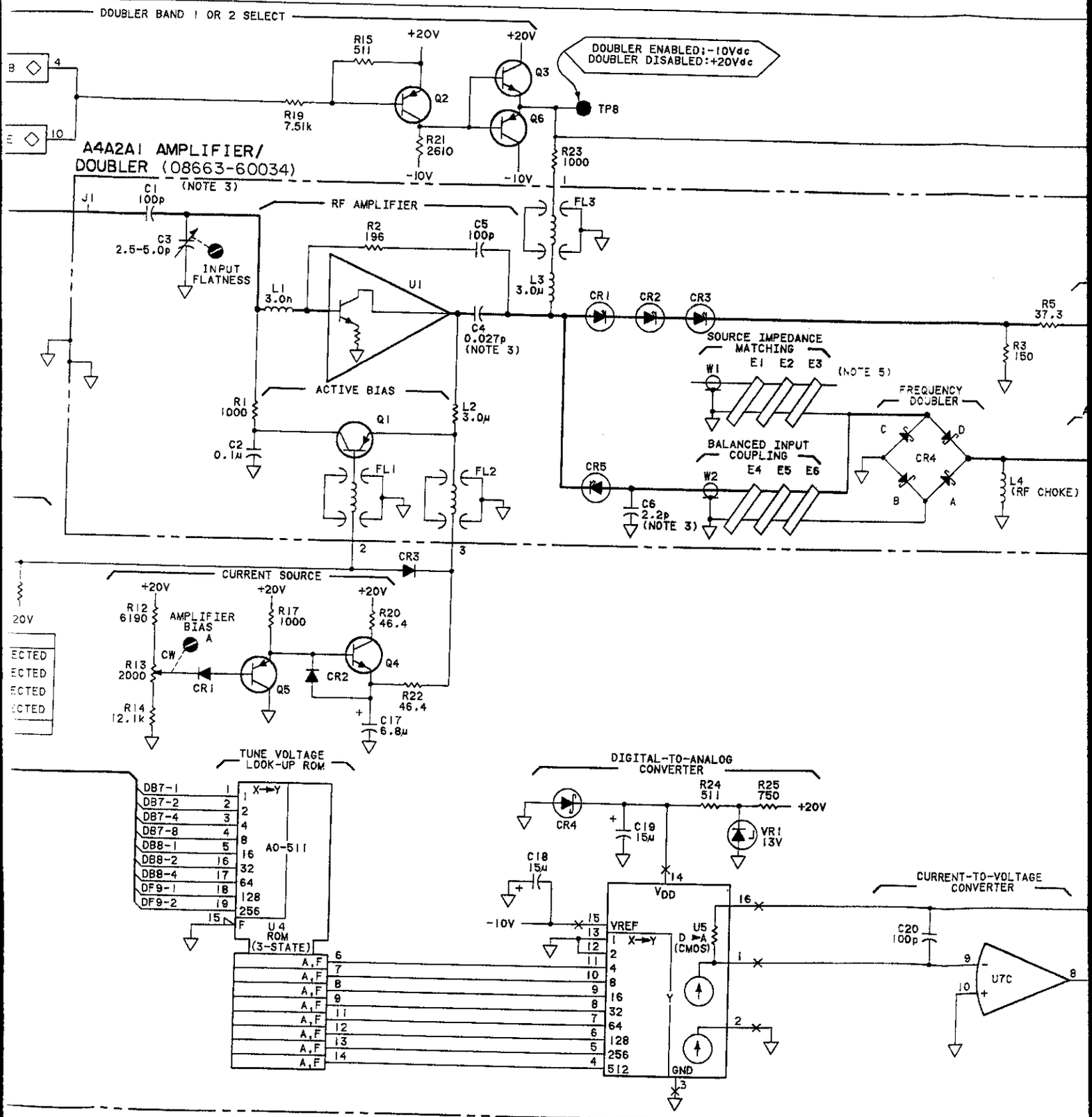


Fig 8-501 Sht 3 of 5

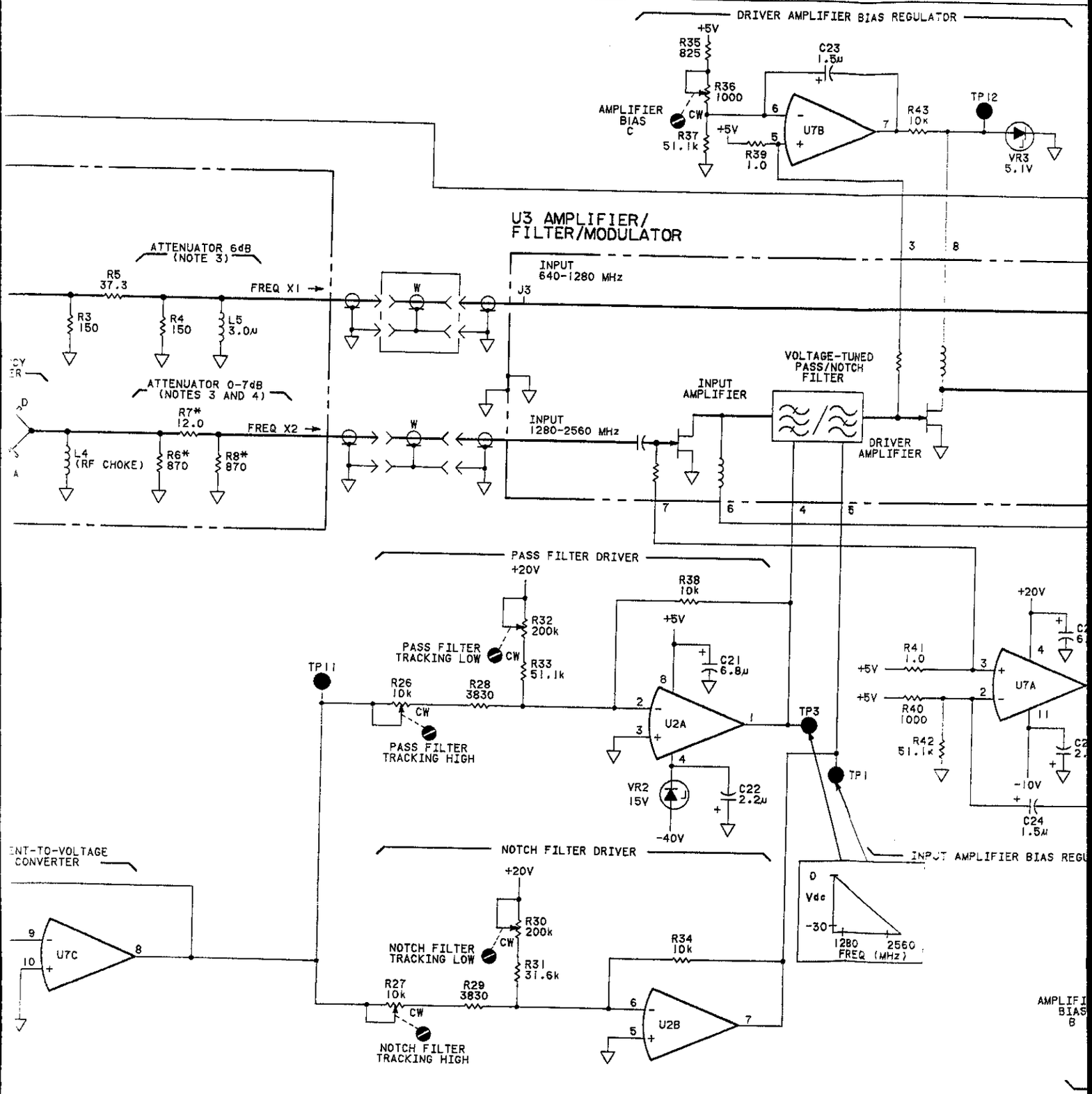
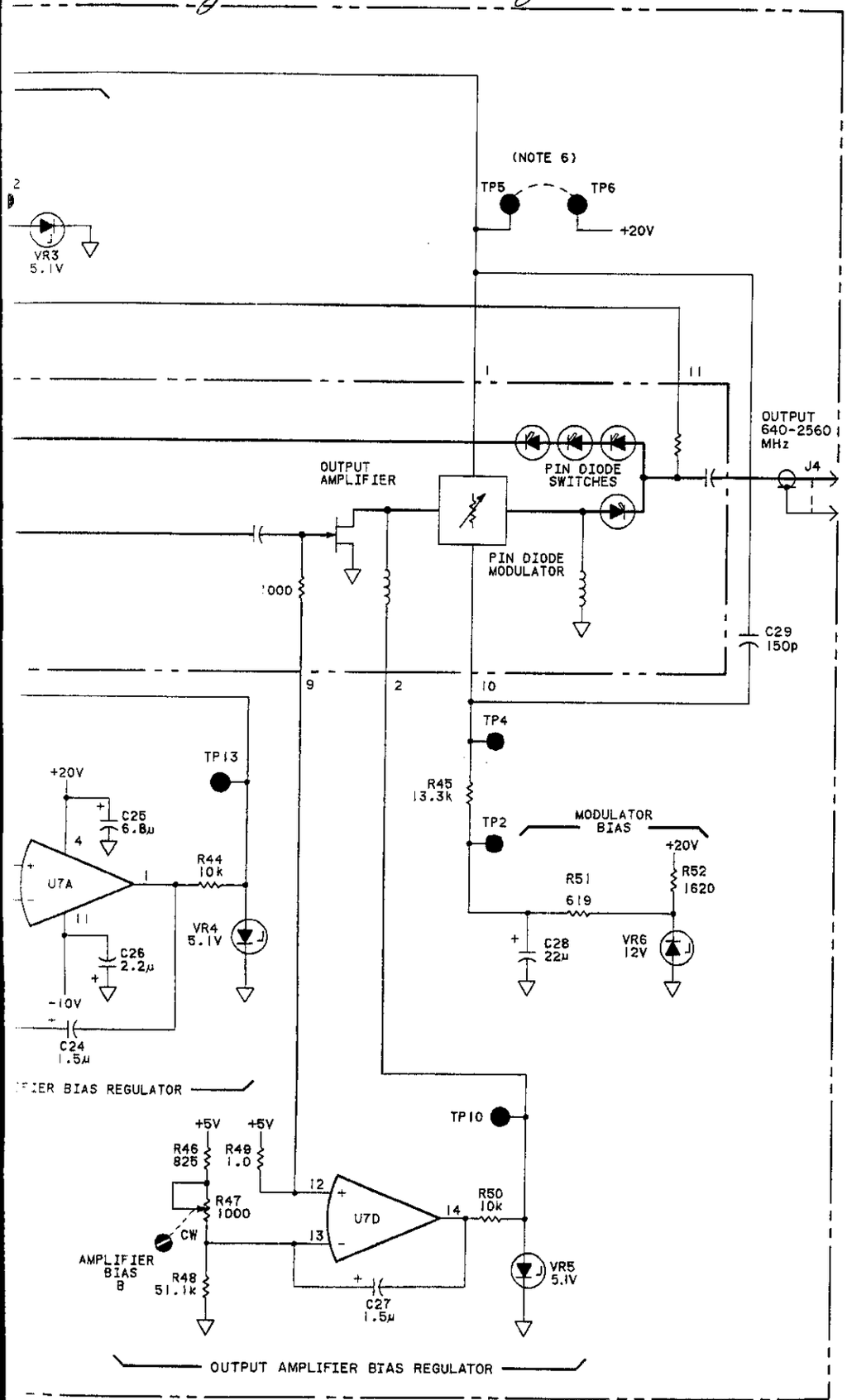
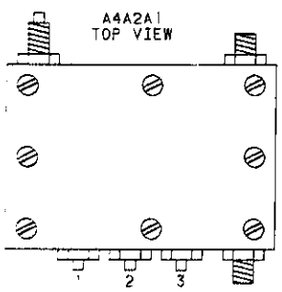
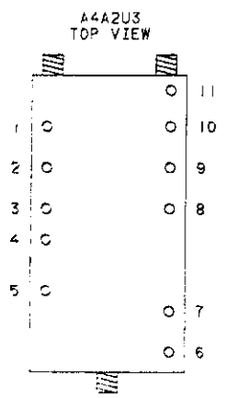


Fig 8-521 Sht 4 of 5







NOT

1. REFER TO TABLE 8 DIAGRAM NOTES.
2. TROUBLESHOOTING THEY ARE ACTUAL YOUR MEASUREMENT DIFFERENT THAN W
3. THE SMALL CHIP C ASSEMBLY REQUIRE SOLDERING TECHNI SOLDER.
4. ASTERISK (*) IND SELECTED IN TEST ARE TYPICAL AND UATION. REFER TO CEDURES.
5. FERRITE BEADS E2 TIVE REACTANCE, ANCE TO GROUND A CR4C AND D TO MA JUNCTION OF CR4 OUTER SHIELD OF
6. JUMPER WIRE IS I SHOOTING ONLY, T MODULATOR FULLY

LOGIC
HIGH
LOW
< IS MORE
> IS MORE
OPEN
GROUND

TRANSIS
INTEGRATE
PART N

REFERENCE DESIGNATIONS
Q1,2,5,6
Q3
Q4
U2
U3
U4
U5
U6
U7

INTEGRATE
VOLTAG
GROUND CO

REFERENCE DESIGNATIONS
U4
U6

REFERENCE D

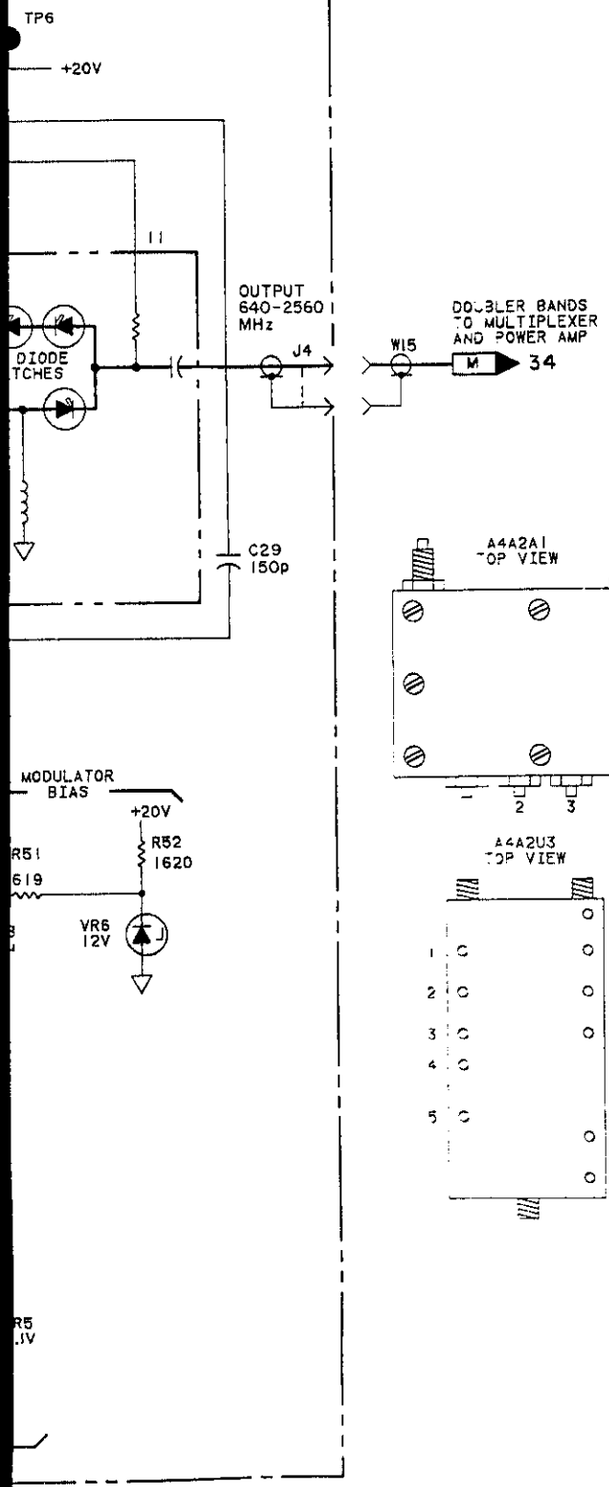
NO PREFIX
W

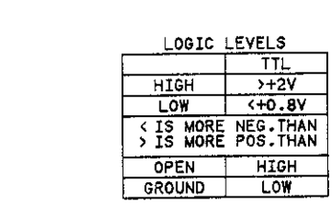
A4A2
C1-28
CR1-5
L1-7
Q1-6
R1-62
TP1-8, 10-13
U2-7
VR1-6

Fig 8-521
Sht 5 of 5

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. THE SMALL CHIP COMPONENTS ON THIS ASSEMBLY REQUIRE LOW TEMPERATURE SOLDERING TECHNIQUES. USE SILVER SOLDER.
4. ASTERISK (*) INDICATES THAT PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL AND REPRESENT 0dB ATTENUATION. REFER TO SECTION V FOR PROCEDURES.
5. FERRITE BEADS E2-E3 CREATE AN INDUCTIVE REACTANCE, ENABLING THE IMPEDANCE TO GROUND AT THE JUNCTION OF CR4C AND D TO MATCH THAT AT THE JUNCTION OF CR4 A AND B. ONLY THE OUTER SHIELD OF COAX W1 IS USED.
6. JUMPER WIRE IS INSTALLED FOR TROUBLESHOOTING ONLY, TO TURN PIN DIODE MODULATOR FULLY ON.





LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

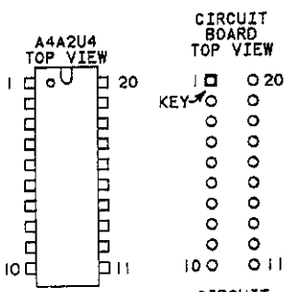
REFERENCE DESIGNATIONS	PART NUMBERS
Q1,2,5,6 Q3 Q4	1853-0459 1854-0810 1854-0637
U2 U3 U4 U5 U6 U7	1826-0547 08663-67001 1816-1008 1826-0931 1820-0471 1826-0600

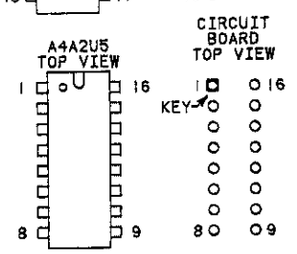
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

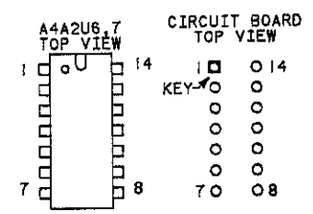
REFERENCE DESIGNATIONS	PIN NUMBERS
U4	+5V - 20 ▽ - 10
U6	+5V - 14 ▽ - 17

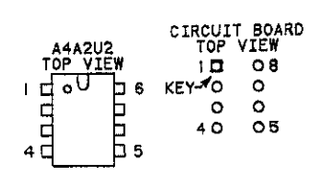
REFERENCE DESIGNATIONS

NO PREFIX	A4A2A1
W	C1-6 CR1-5 E1-6 FL1-3 J1 L1-5 Q1 R1-8 U1 W1,2
A4A2	A4A10
C1-28 CR1-5 L1-7 Q1-6 R1-52 TP1-8,10-13 U2-7 VR1-6	J6 XA4A2









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A4A2

Figure 8-521. A4A2 Doubler #2 Schematic

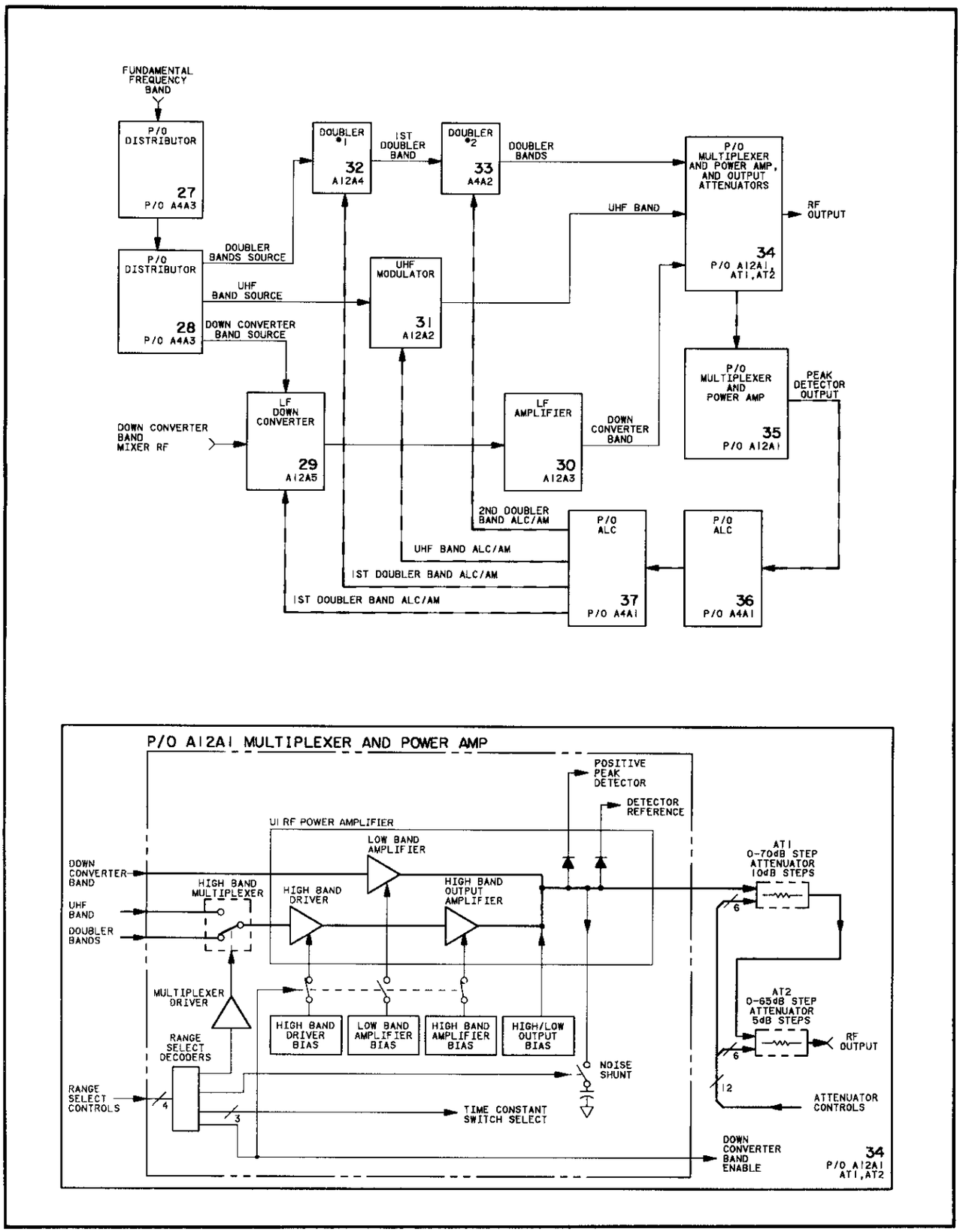


Figure 8-522. P/O A12A1 RF Multiplexer/Power Amplifier and Output Attenuators Block Diagrams

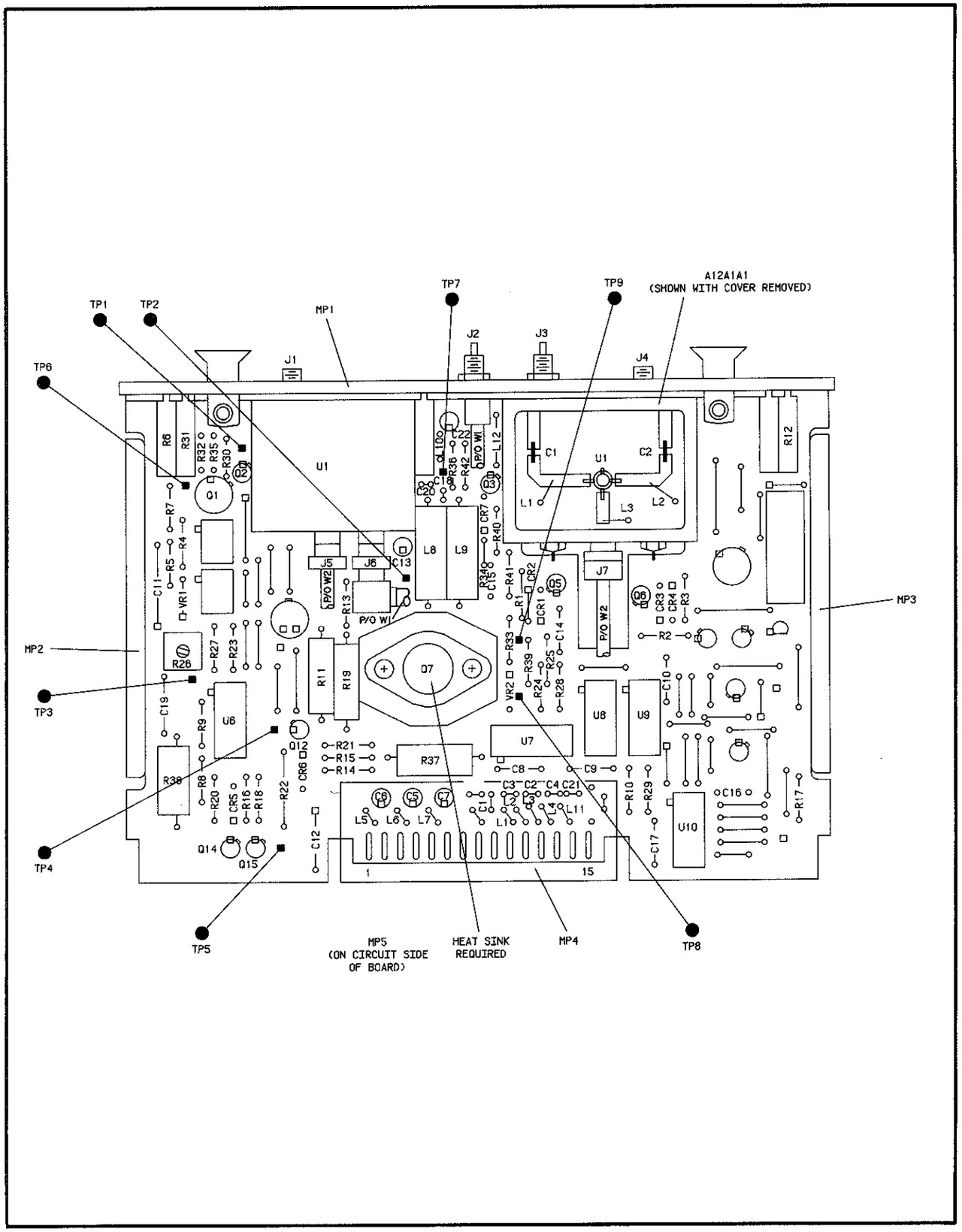


Figure 8-523. P/O A12A1 RF Multiplexer/Power Amplifier and Output Attenuators Component Locator

CHANGES

All serial prefixes

On the A12A1 schematic:

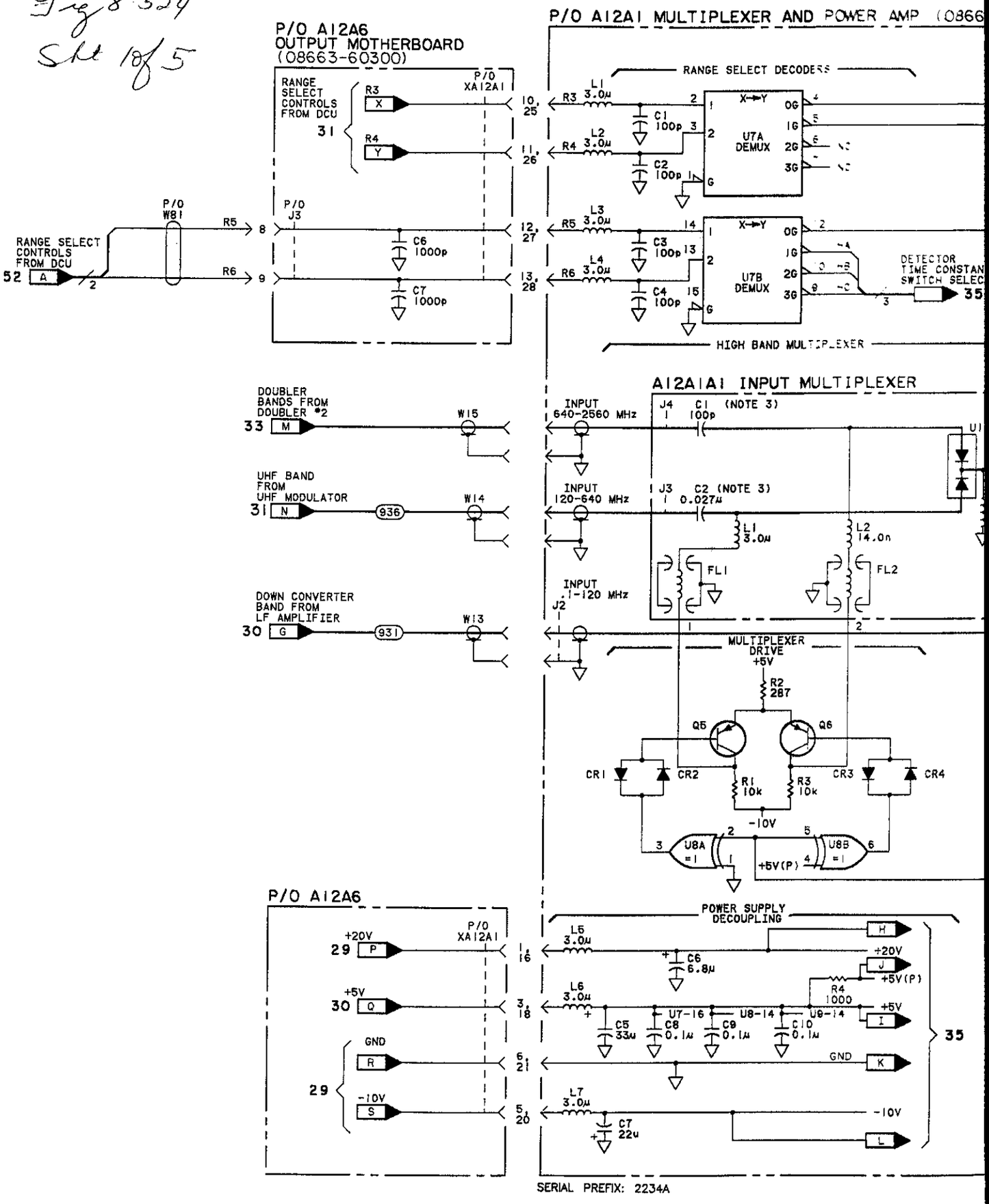
- A12A1E1-10 - Add E1-10, ferrite beads, to W7.
- A12A1L10 - Change the value of L10 to 3u.
- A12A1R41 - Change the value of R41 to 10k.

2451A and Above

On the A12A1 schematic:

- A12A1L7 - Change the value of L7 to 630u.

Fig 8-524
Sht 1 of 5



SERIAL PREFIX: 2234A

ID POWER AMP (08663-60301) Fig 8-524 Sht 2 of 5

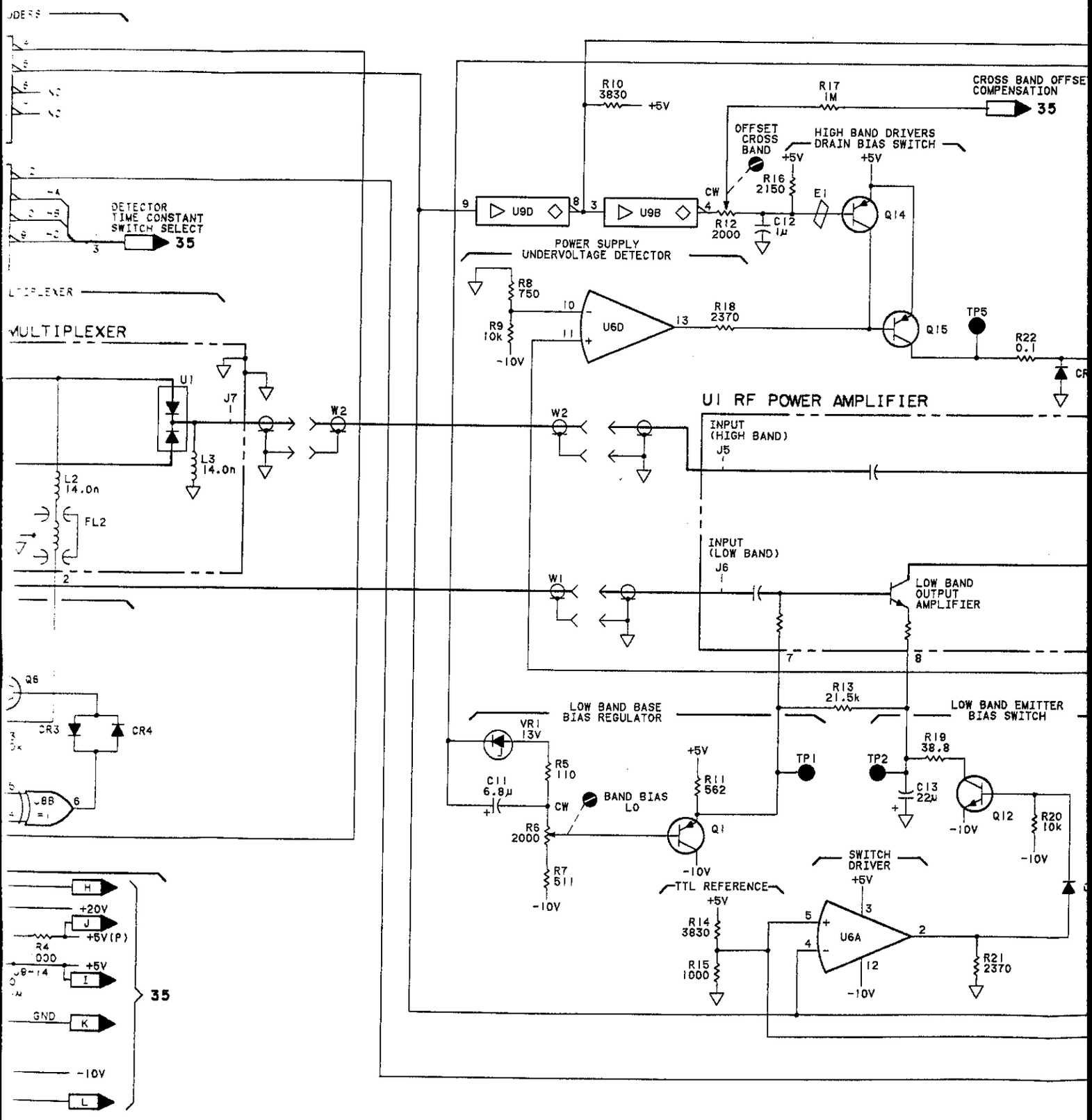


Fig 8-524 Sht 3 of 5

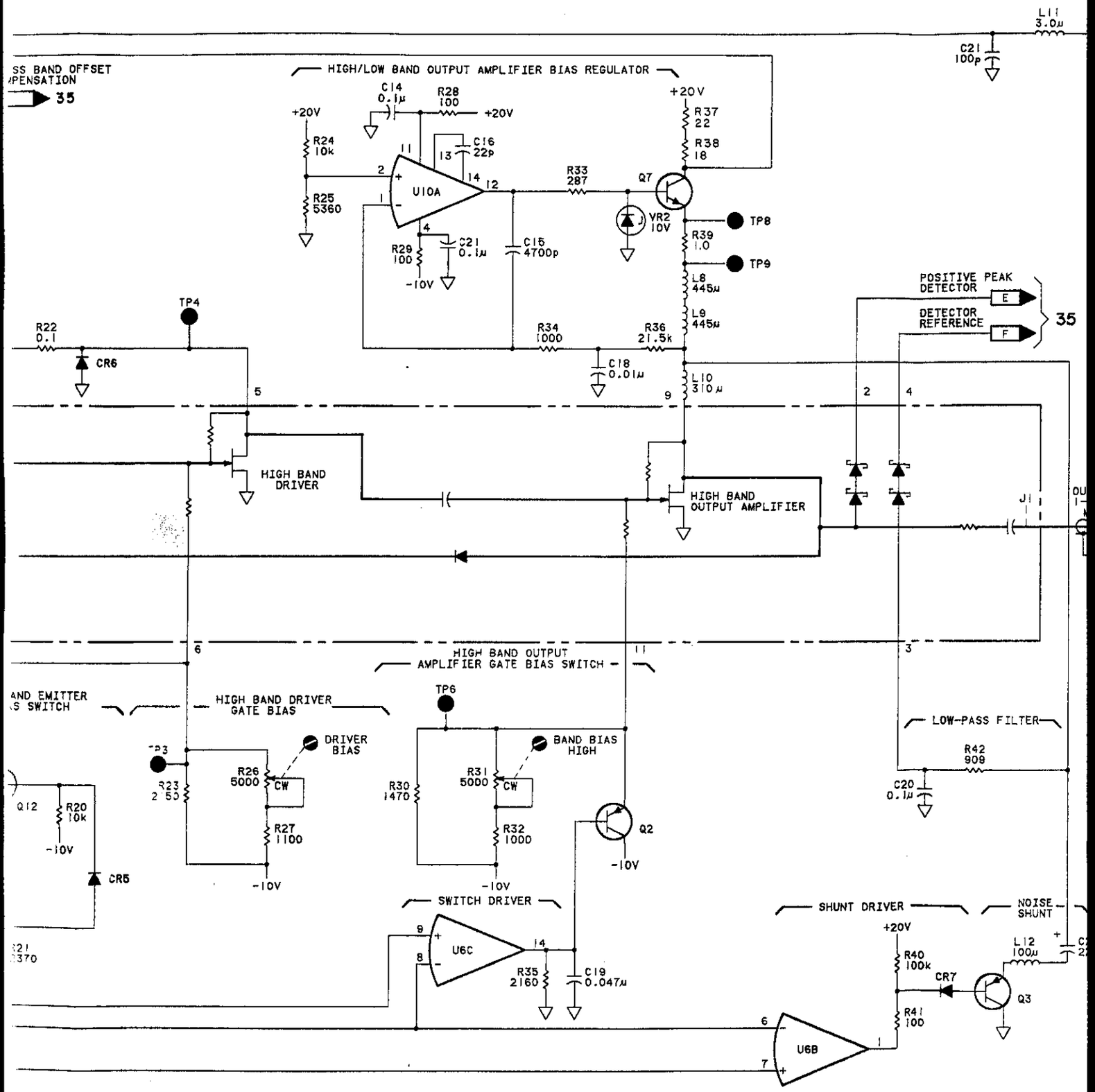
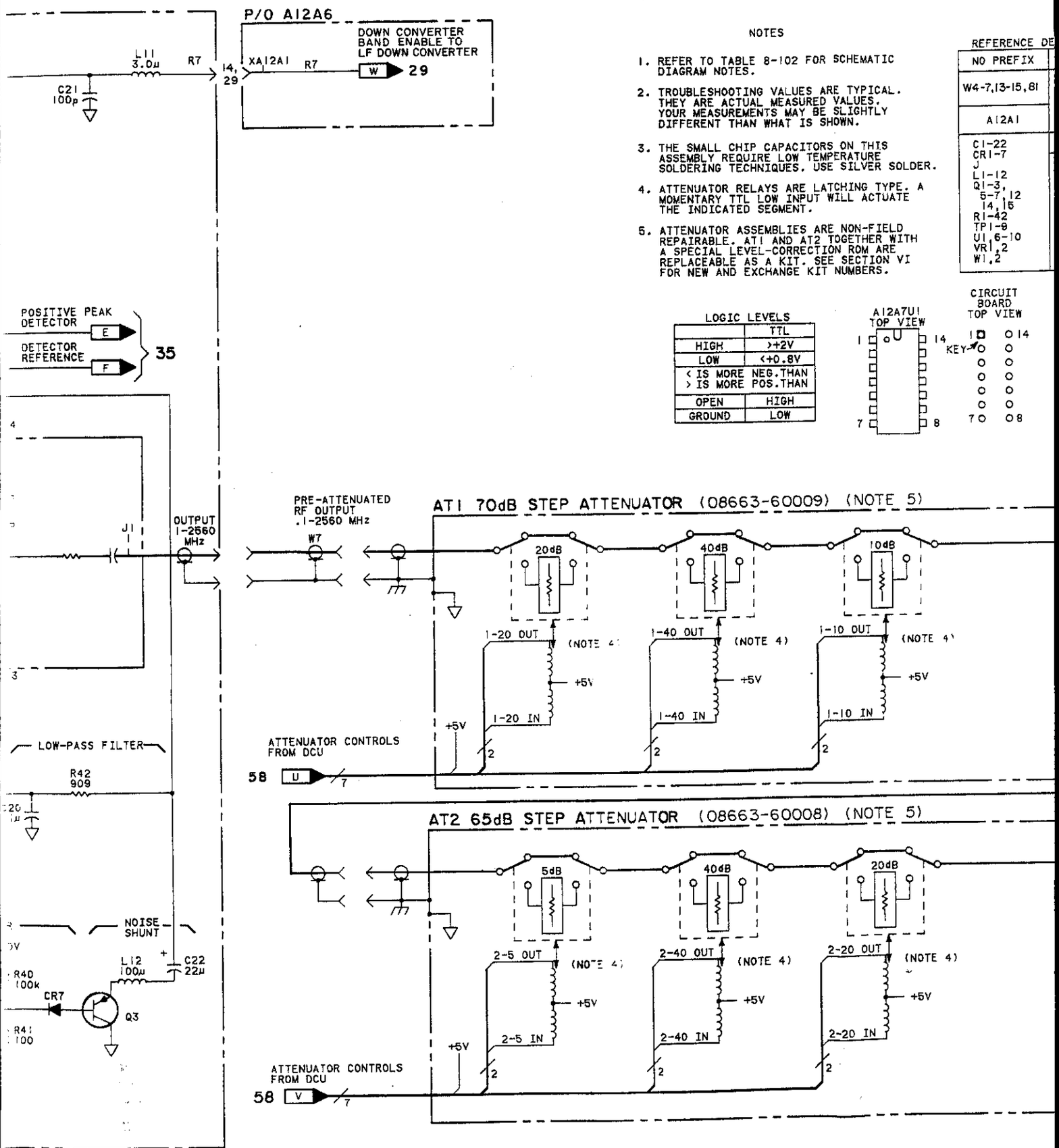


Fig 8-524 Sht 4 of 5



NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. THE SMALL CHIP CAPACITORS ON THIS ASSEMBLY REQUIRE LOW TEMPERATURE SOLDERING TECHNIQUES. USE SILVER SOLDER.
4. ATTENUATOR RELAYS ARE LATCHING TYPE. A MOMENTARY TTL LOW INPUT WILL ACTUATE THE INDICATED SEGMENT.
5. ATTENUATOR ASSEMBLIES ARE NON-FIELD REPAIRABLE. AT1 AND AT2 TOGETHER WITH A SPECIAL LEVEL-CORRECTION ROM ARE REPLACEABLE AS A KIT. SEE SECTION VI FOR NEW AND EXCHANGE KIT NUMBERS.

REFERENCE DE
NO PREFIX
W4-7,13-15,81
A12A1
C1-22 CR1-7 J L1-12 Q1-3, 5-7, 12 14, 15 R1-42 TP1-8 U1, 6-10 VR1, 2 W1, 2

LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

A12A7U1 TOP VIEW

CIRCUIT BOARD TOP VIEW

Fig 8-524 Sht 5 of 5

NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. THE SMALL CHIP CAPACITORS ON THIS ASSEMBLY REQUIRE LOW TEMPERATURE SOLDERING TECHNIQUES. USE SILVER SOLDER.
4. ATTENUATOR RELAYS ARE LATCHING TYPE. A MOMENTARY TTL LOW INPUT WILL ACTUATE THE INDICATED SEGMENT.
5. ATTENUATOR ASSEMBLIES ARE NON-FIELD REPAIRABLE. AT1 AND AT2 TOGETHER WITH A SPECIAL LEVEL-CORRECTION ROM ARE REPLACEABLE AS A KIT. SEE SECTION VI FOR NEW AND EXCHANGE KIT NUMBERS.

REFERENCE DESIGNATIONS

NO PREFIX	A12A1A1
W4-7,13-15,81	C1-2 FL1,2 J3,4,7 L1-3 U1
A12A1	
C1-22 CR1-7 J L1-12 Q1-3, 5-7,12 14,15 R1-42 TP1-9 U1,6-10 VR1,2 W1,2	A12A6 C6,7 J3 XA12A1

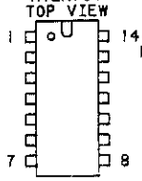
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
A12A1	
Q1	1853-0314
Q2	1853-0459
Q3,5,6,14	1853-0281
Q7	1854-0814
Q12	1854-0668
Q15	1853-0393
U1	08663-67002
U6	1826-0138
U7	1820-1281
U8	1820-1211
U9	1820-0471
U10	1826-0889
A12A1A1	08663-60035

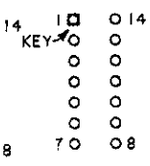
LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW

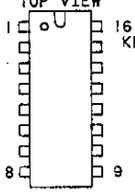
A12A7U1 TOP VIEW



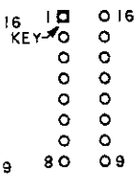
CIRCUIT BOARD TOP VIEW



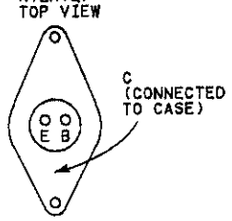
12A1U6,8-10 TOP VIEW

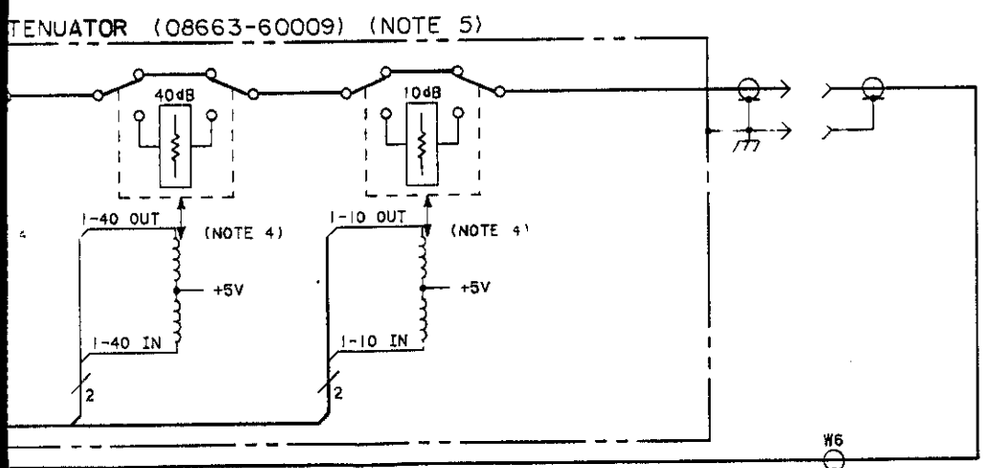


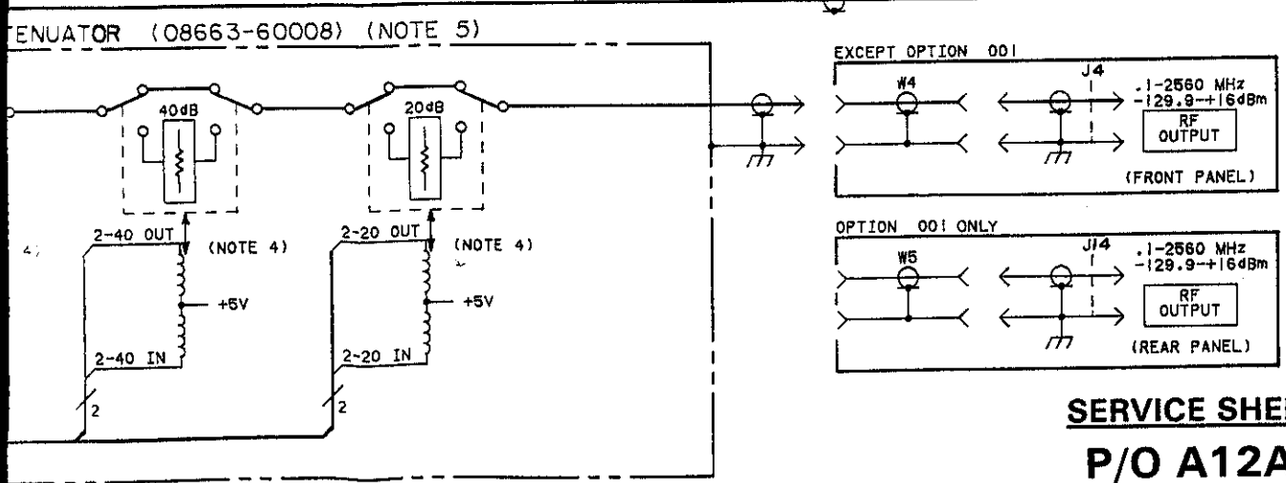
CIRCUIT BOARD TOP VIEW



A12A1Q7 TOP VIEW







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P/O A12A1

Figure 8-524. P/O A12A1 RF Multiplexer/Power Amplifier and Output Attenuators Schematic

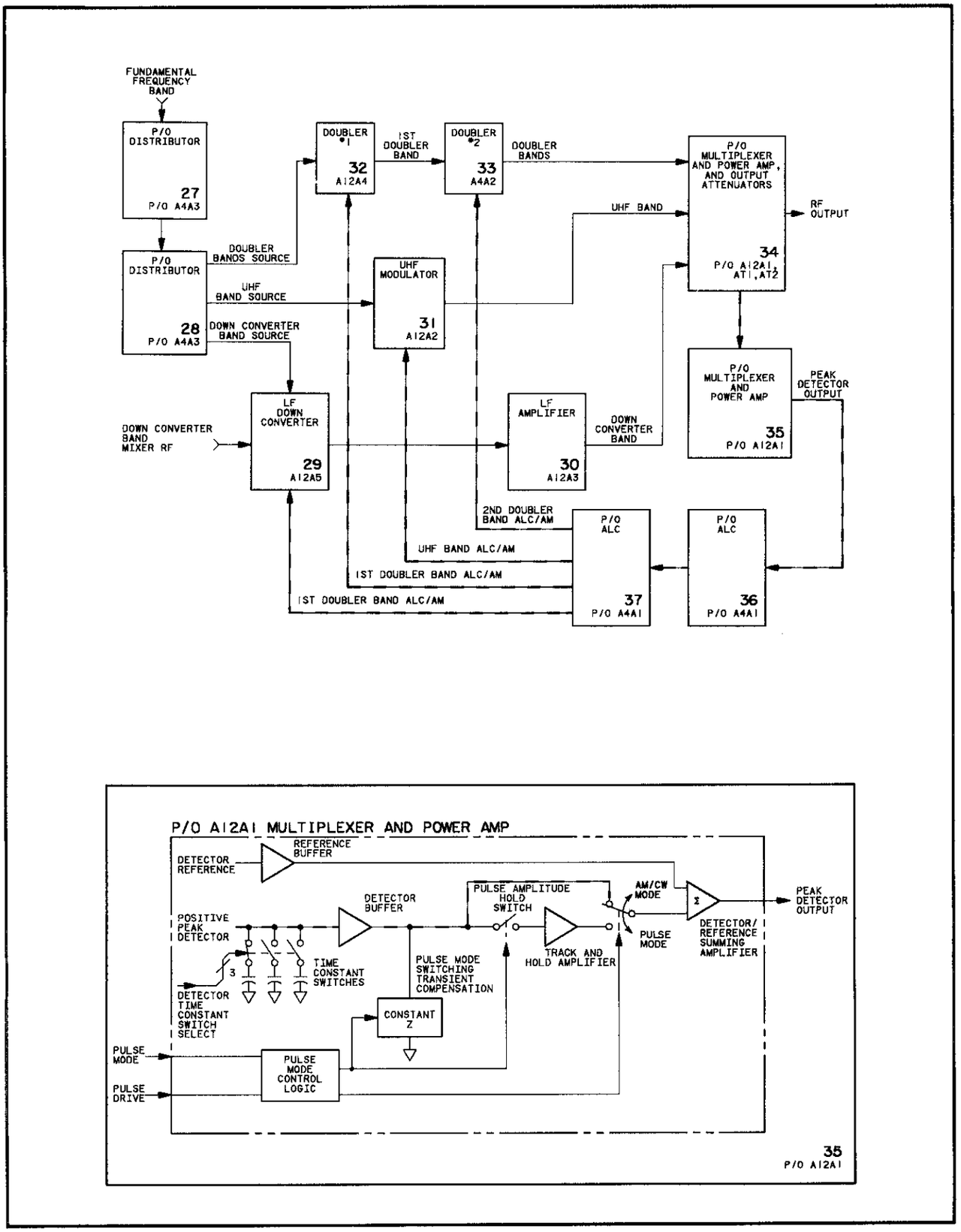


Figure 8-525. P/O A12A1 RF Multiplexer/Power Amplifier Block Diagrams

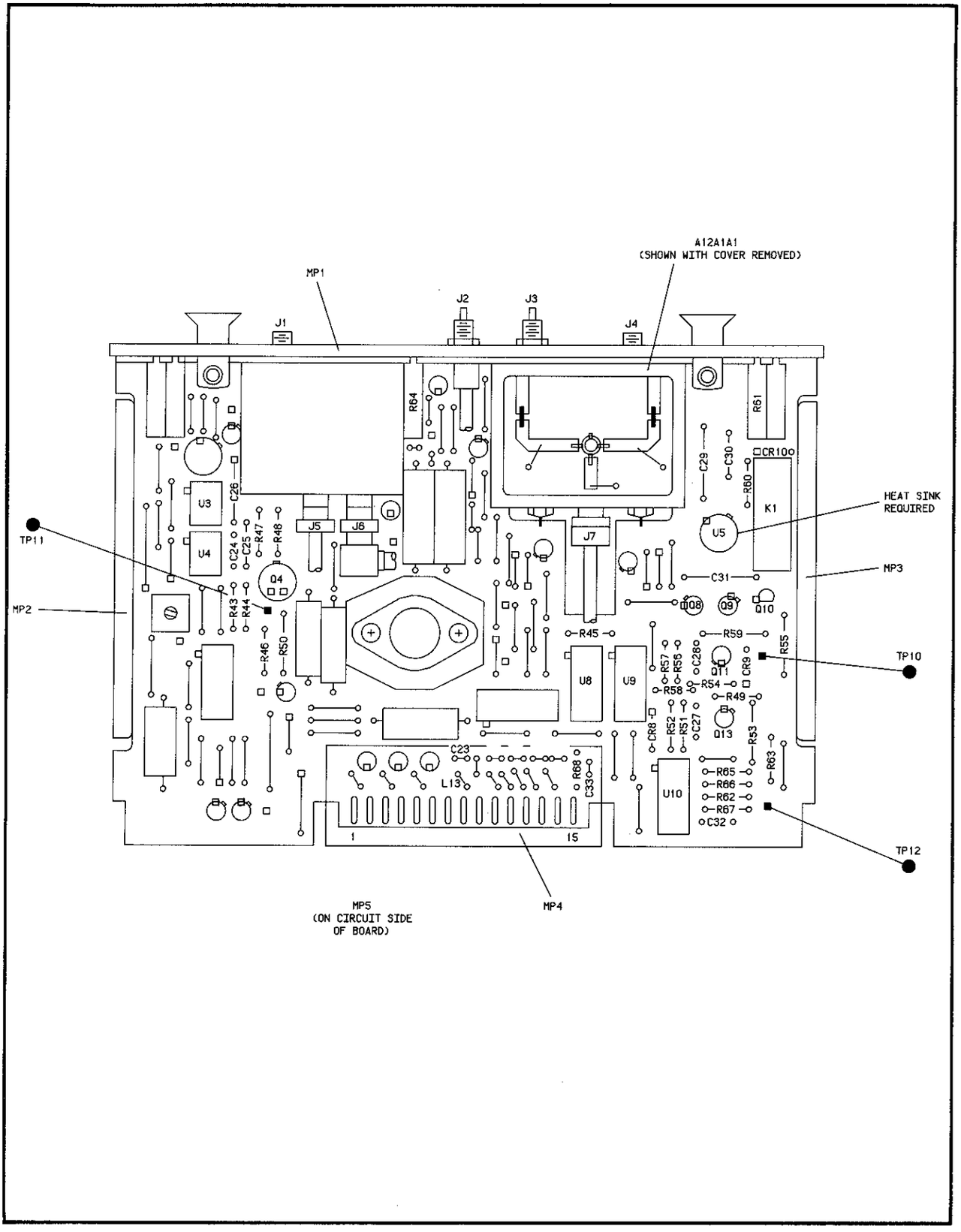


Figure 8-526. P/O A12A1 RF Multiplexer/Power Amplifier Component Locator

CHANGES

All serial prefixes

On the A12A1 schematic:

- A12A1C24, C25 - Change the value of C24 to 4700p. Change the value of C25 to 2200p.

2326A and Above

On the A12A1 schematic:

- A12A1R65 - Change the value of R65 to 464k.

2405A and Above

On the A12A1 component locator:

- A12A1C34 - In the bottom left corner of the A12A1 component locator, add C34 between R67 and C32.

On the A12A1 schematic:

- A12A1C34 - In the top right corner of the schematic, in the circuitry labeled "DETECTOR/REFERENCE SUMMING AMPLIFIER", add C34 (100p) in parallel with R67.

2601A and Above

On the schematic:

- A12A1Q4 - In the Table of Transistor and Integrated Circuit Part Numbers, change the part number of Q4 to 1854-1046.

Fig 8-527
Sht 1 of 5

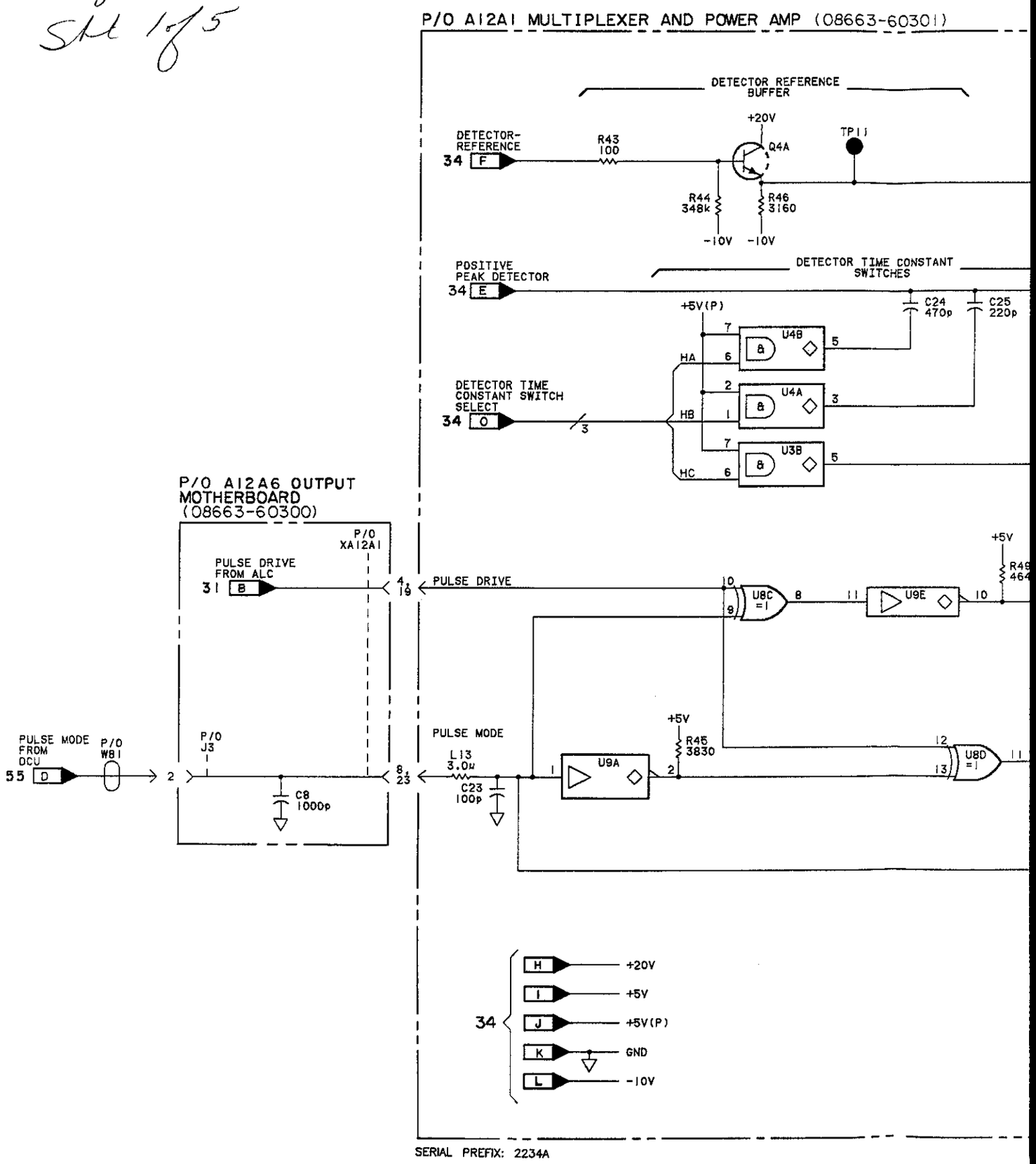


Fig 8-537 Sht 2 of 5

08663-60301)

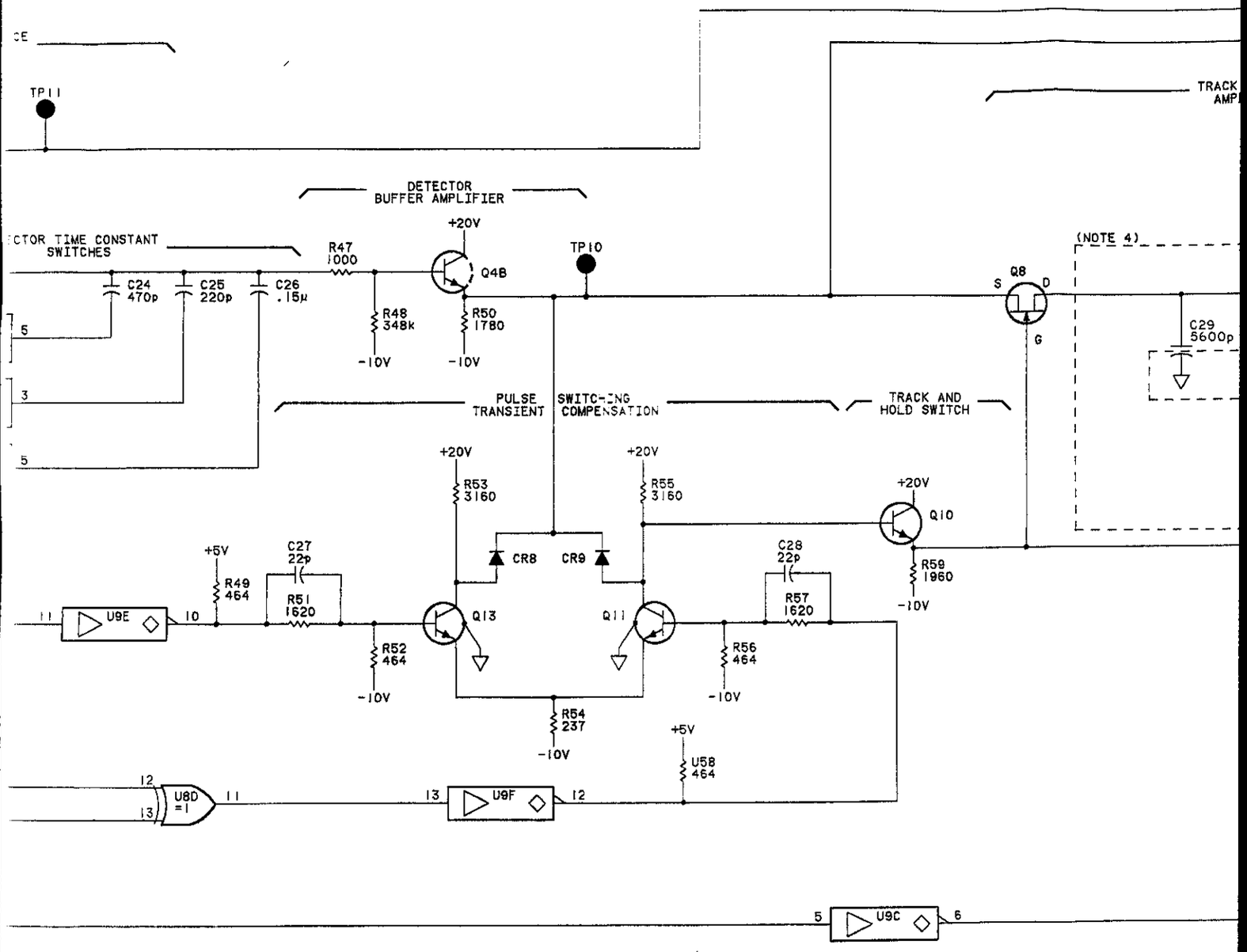


Fig 8-527 Sht 3 of 5

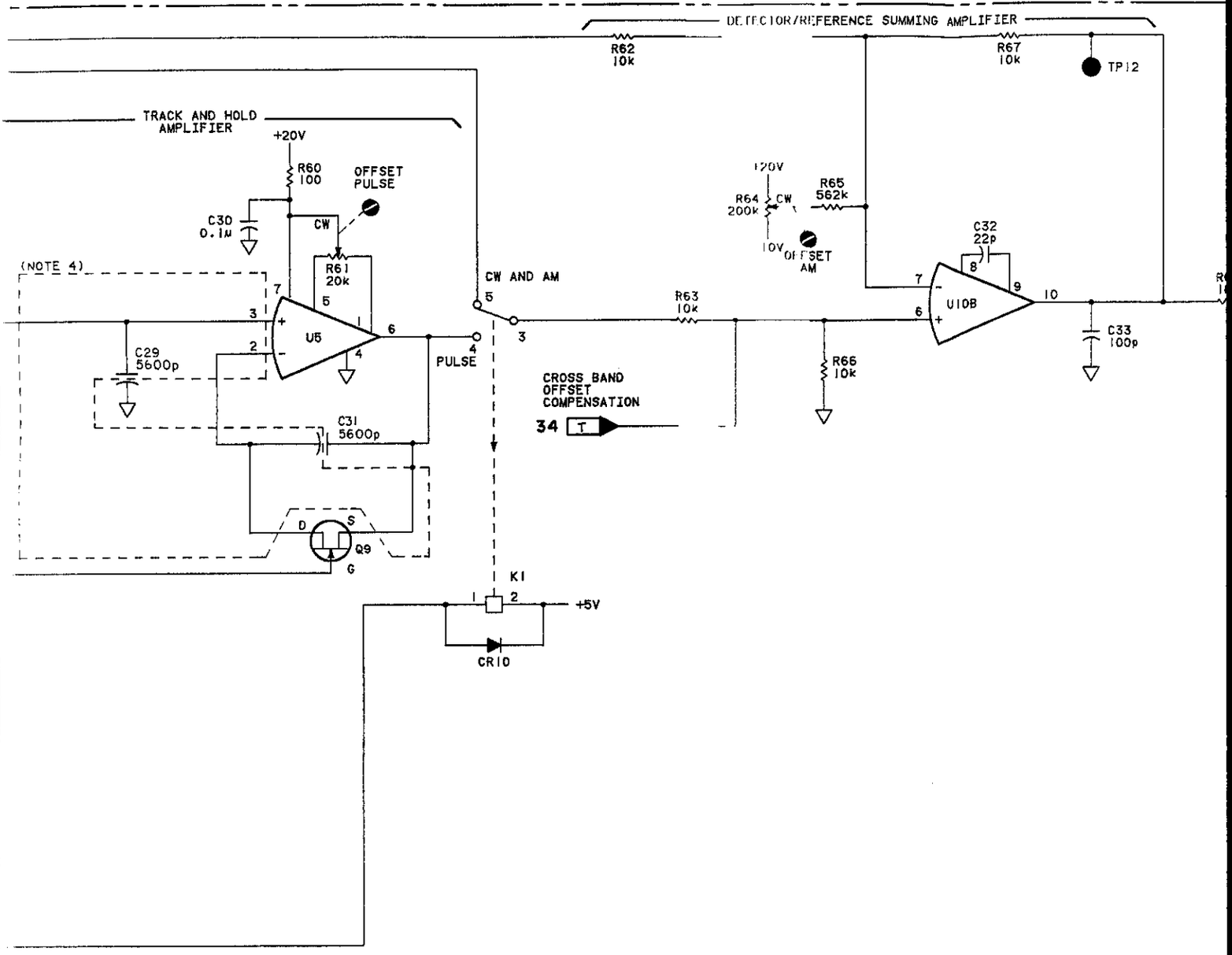
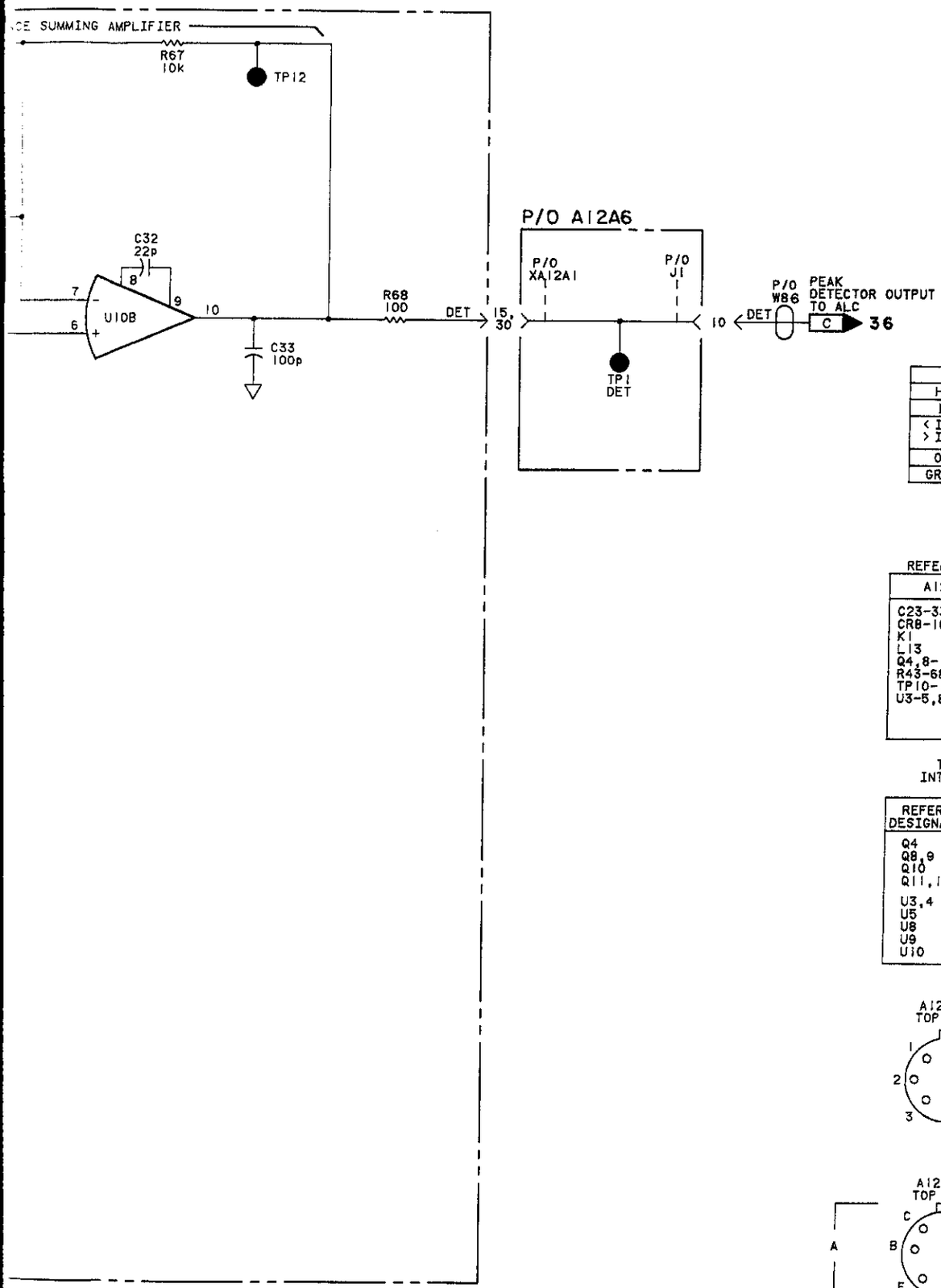


Fig 8-527 Sht 4 of 5



1. REFE
DIAG
2. TROU
THEY
YOUR
DIFF
3. SHOWN
SCHEM

LOGIC LEVELS	
	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

REFERENCE DESIGNATIONS	
A12A1	NO PREFIX
C23-33 CR8-10 K1 L13 Q4,8-11,13 R43-68 TP10-12 U3-5,8,10	W81 A12A6 CB J1,3 TP1 XA12A1

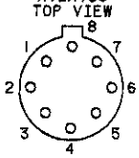
4. INDIC
CIRCU
IS NO

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS	
REFERENCE DESIGNATIONS	PART NUMBERS
Q4	1854-0475
Q8,9	1855-0420
Q10	1854-0811
Q11,13	1854-0486
U3,4	1820-0535
U5	1826-0358
U8	1820-1211
U9	1820-0471
U10	1826-0889

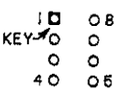
INTEGRA
VOL
GROUND

REFERENCE DESIGNATIO
U3,4

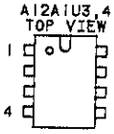
A12A1U5
TOP VIEW



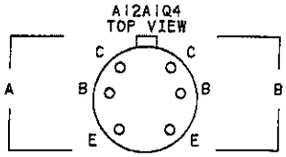
CIRCUIT BOARD
TOP VIEW



A12A1U3,4
TOP VIEW



A12A1Q4
TOP VIEW



A12A1U8-10
TOP VIEW

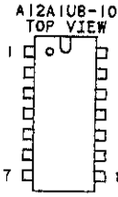


Fig 8-527
Sht 5 of 5

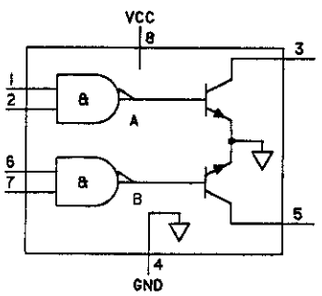
NOTES

1. REFER TO TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. SHOWN BELOW IS A SIMPLIFIED SCHEMATIC OF A12A1U3,4.

PEAK DETECTOR OUTPUT TO ALC
C ▶ 36

LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW



4. INDICATED SHIELD IS A PRINTED CIRCUIT TRACE. THIS GUARD TRACE IS NOT AT GROUND POTENTIAL.

REFERENCE DESIGNATIONS

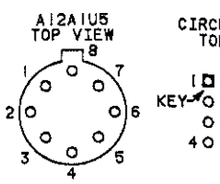
A12A1	NO PREFIX
C23-33 CR8-10 K1 L13 Q4,8-11,13 R43-68 TP10-12 U3-5,8,10	W81 A12A6 C8 J1,3 TP1 XA12A1

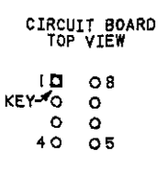
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

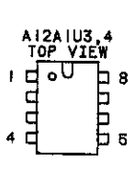
REFERENCE DESIGNATIONS	PART NUMBERS
Q4	1854-0475
Q8,9	1855-0420
Q10	1854-0811
Q11,13	1854-0485
U3,4	1820-0535
U5	1826-0358
U8	1820-1211
U9	1820-0471
U10	1826-0889

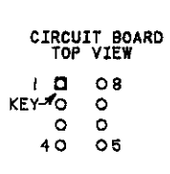
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

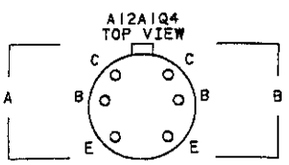
REFERENCE DESIGNATIONS	PIN NUMBERS
U3,4	+5V - 8 ▽ - 4

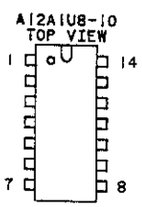


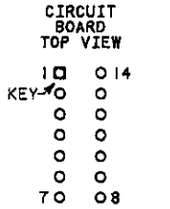












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P/O A12A1

Figure 8-527. P/O A12A1 RF Multiplexer/Power Amplifier Schematic

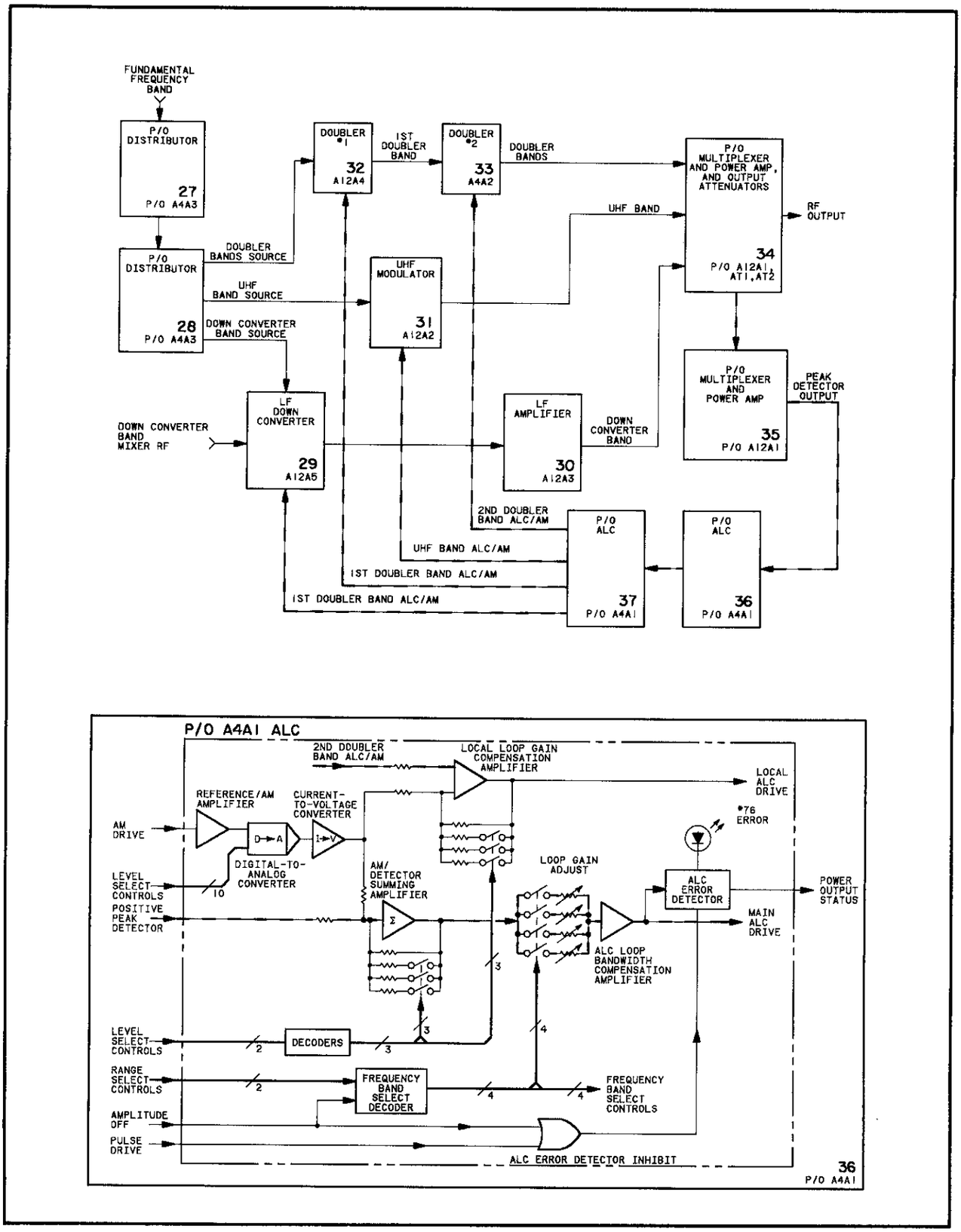


Figure 8-528. P/O A4A1 Automatic Level Control Block Diagrams

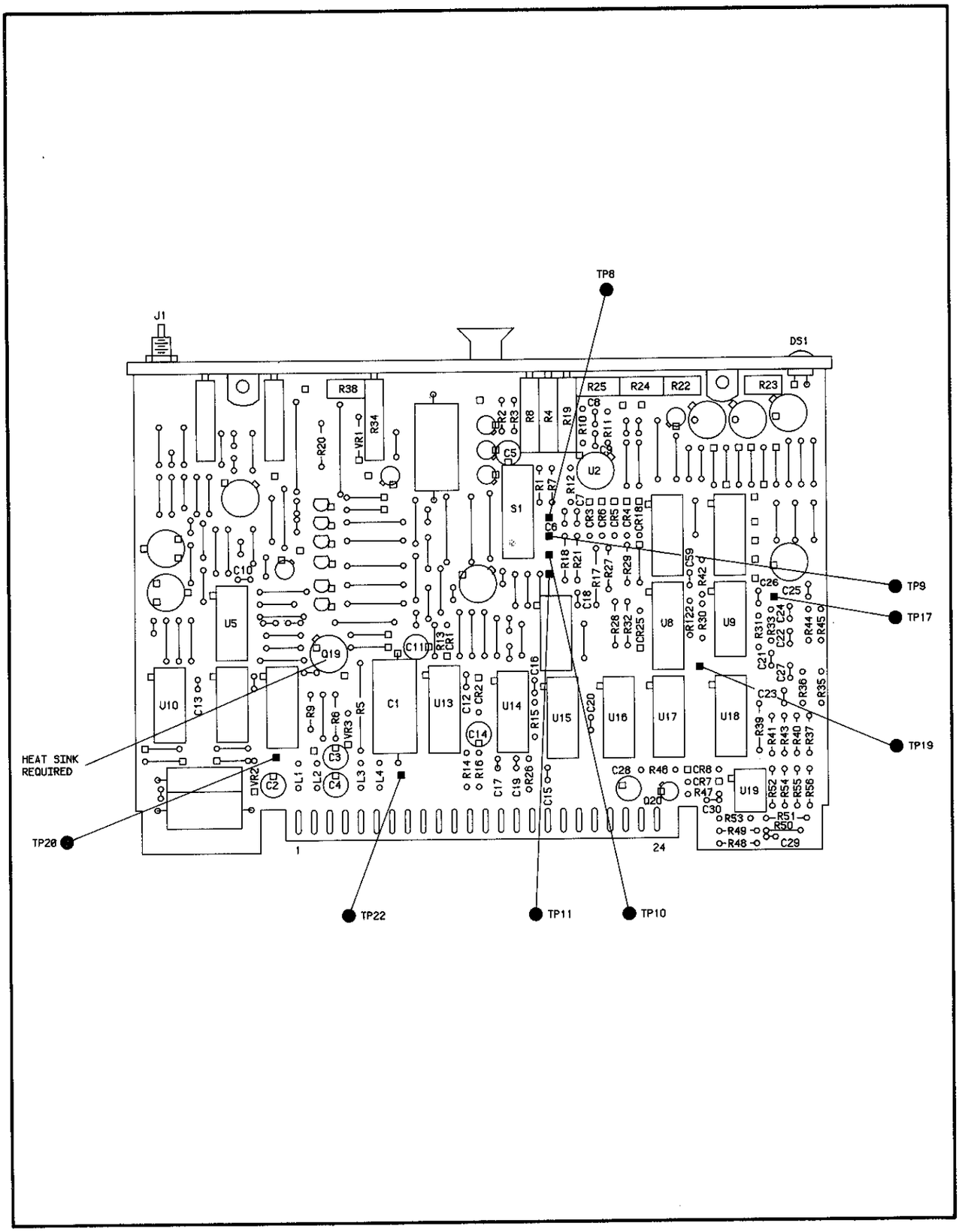


Figure 8-529. P/O A4A1 Automatic Level Control Component Locator

CHANGES

All Serial Prefixes	On the A4A1 Component Locator:
	• A4A1R38 - Change the value of R38 to 50k.

Fig 8-530
Sht 1 of 5

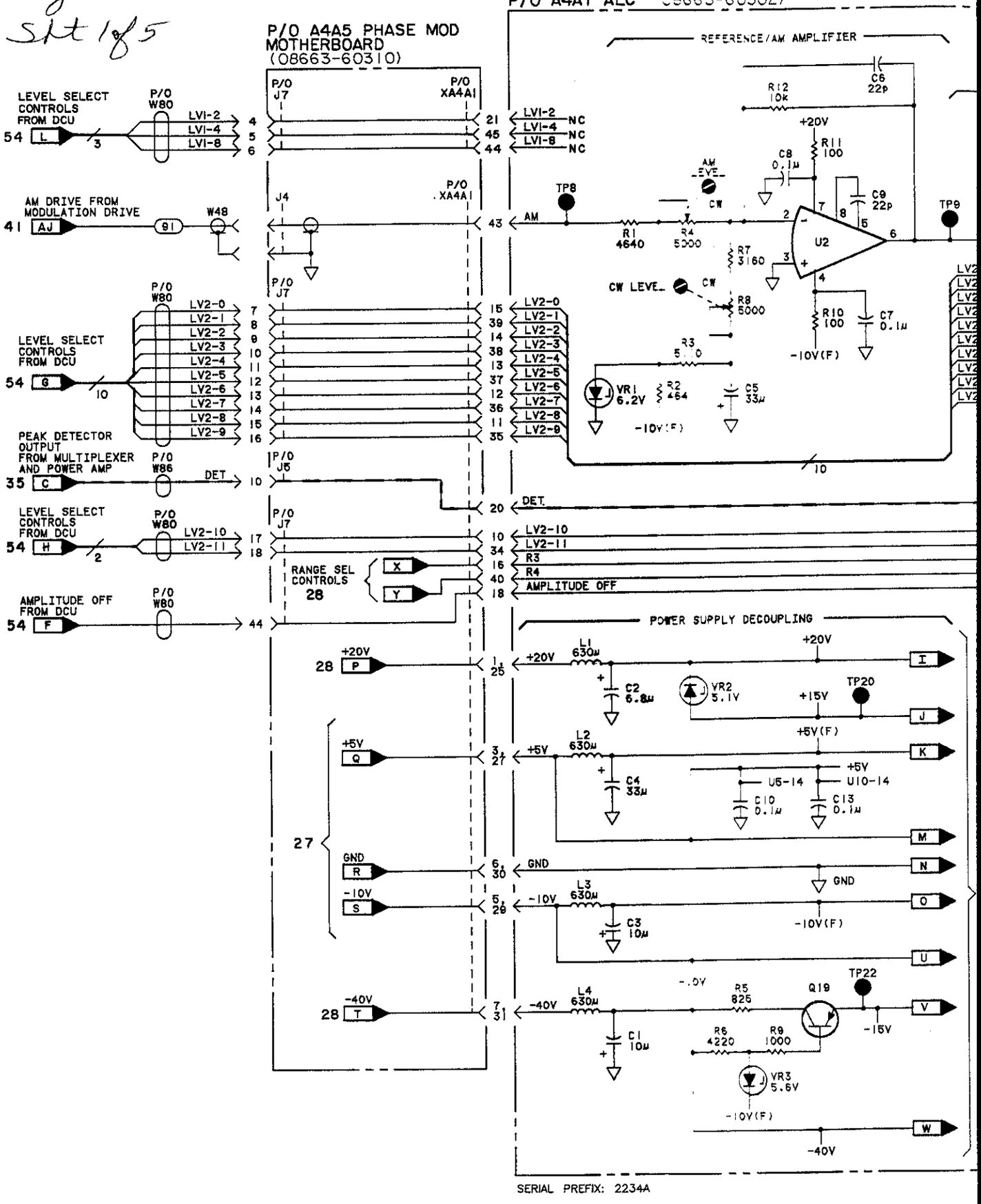


Fig 8-530 Sht 2 of 5

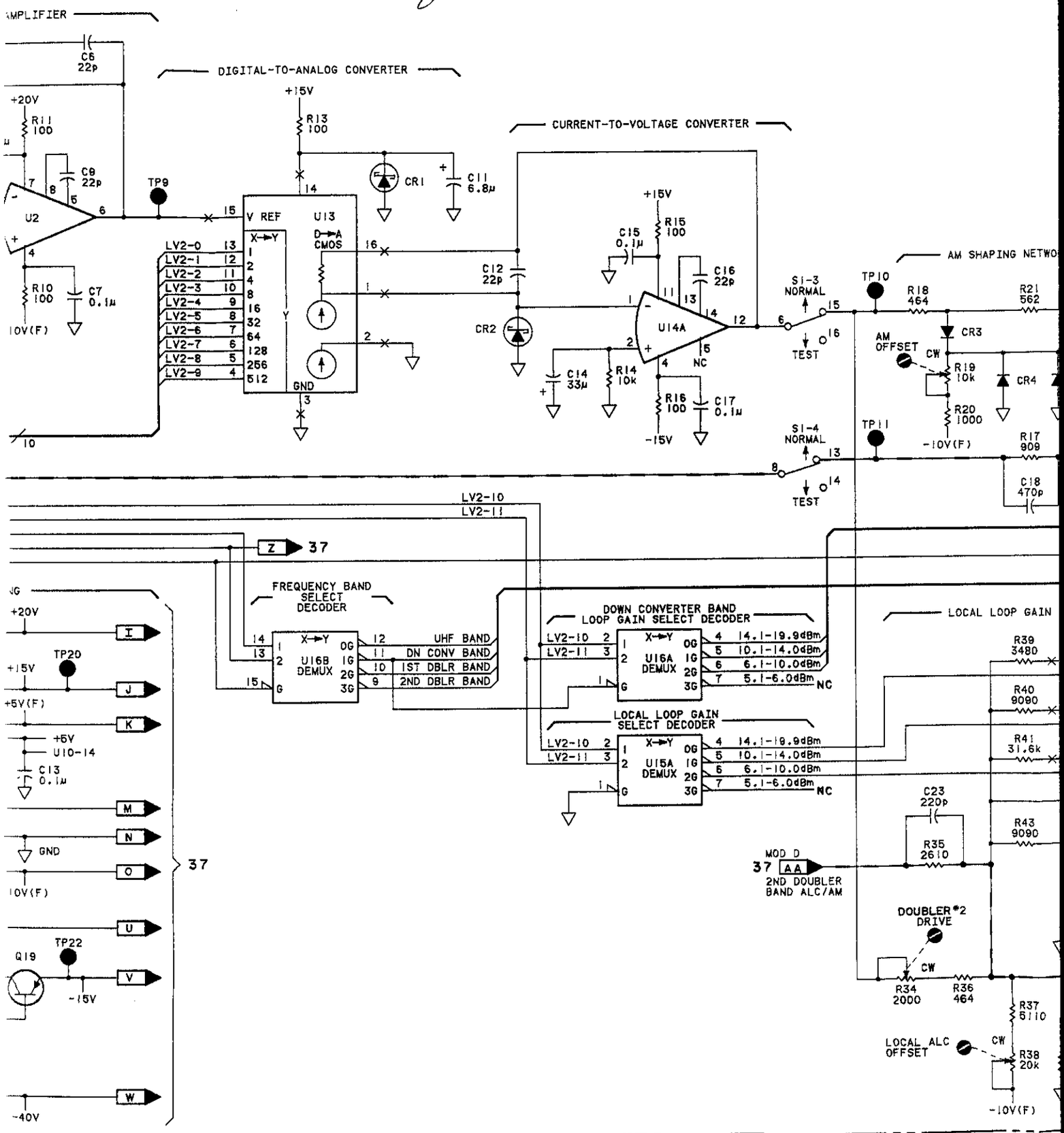


Fig 8-530 Sht 3 of 5

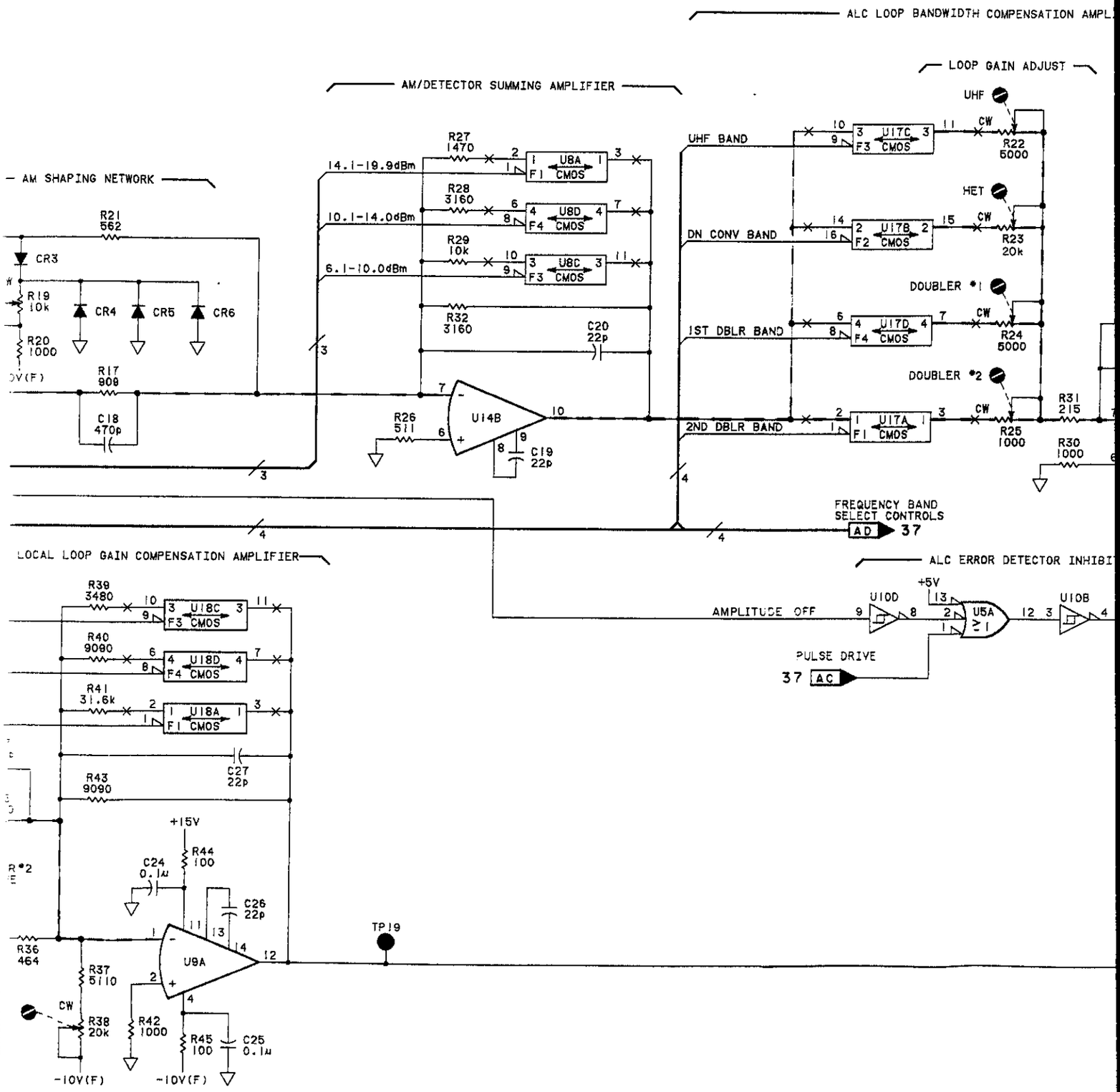
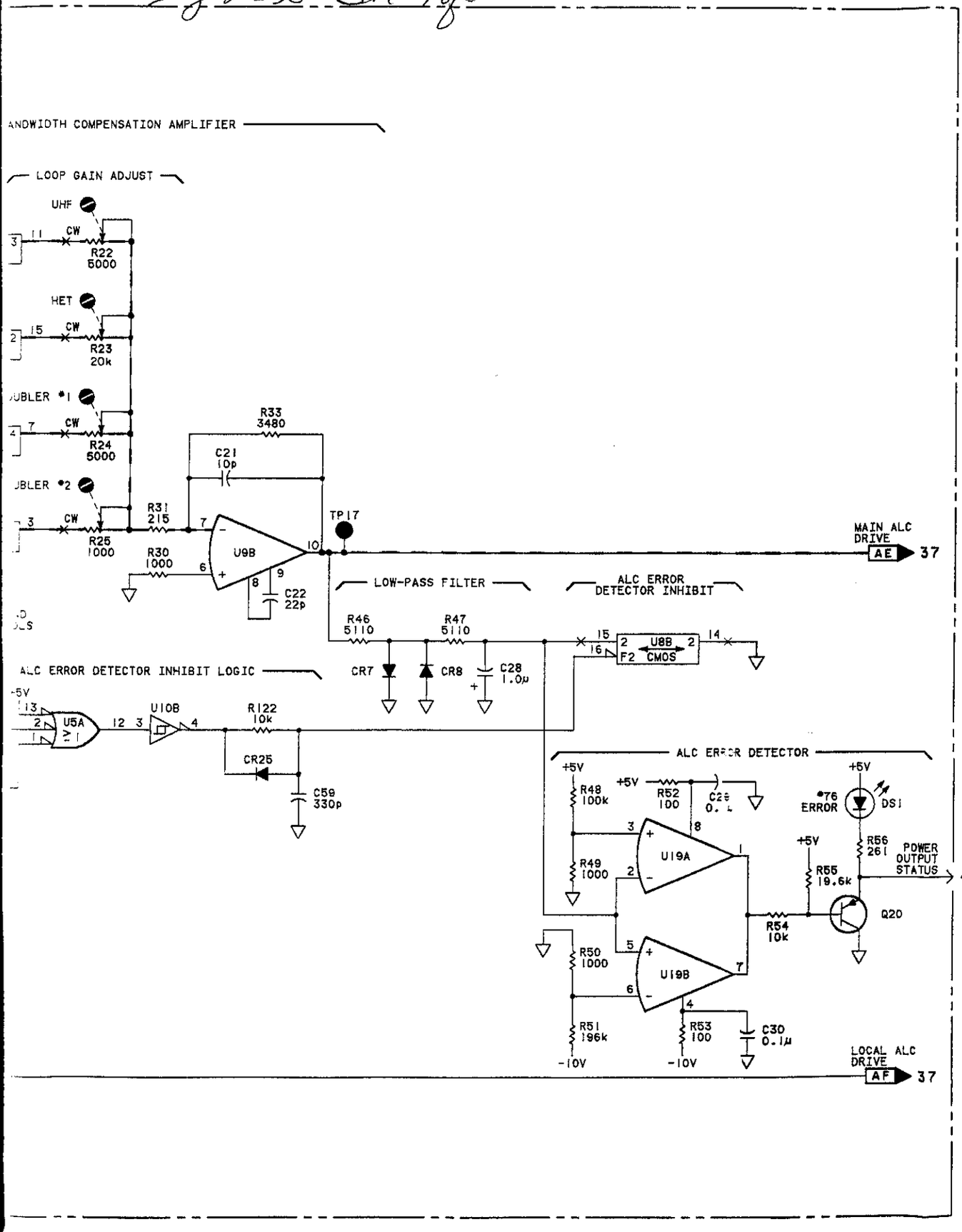


Fig 8-530 SH 4 of 5



NOTES

1. SEE TABLE 8-102 DIAGRAM NOTES.
2. TROUBLESHOOTING THEY ARE ACTUAL YOUR MEASUREMEN DIFFERENT THAN

REFERENCE DESIGN

NO PREFIX	
W46,80,86	J4, XA4
A4A1	
C1-30,59 CR1-8,25 DS1 L1-4 Q19,20 R1-56,122 TP8-11,17, 19,20,22 U2,5,8-10, 13-19 VR1,3	

INTEGRATED CIR VOLTAGE AND GROUND CONNECT

REFERENCE DESIGNATIONS	P NU
U8,17	+15 +5V -10V
U15,16	+5V
U18	+20 +5V -10V

Fig 8-530
Sht 5 of 5

NOTES

1. SEE TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

REFERENCE DESIGNATIONS

NO PREFIX	A7A4
W48,80,86	J4,5,7 XA4A1
A4A1	
C1-30,59 CR1-8,25 DS1 L1-4 Q19,20 R1-56,122 TP8-11,17, 19,20,22 U2,5,8-10, 13-19 VR1,3	

LOGIC LEVELS

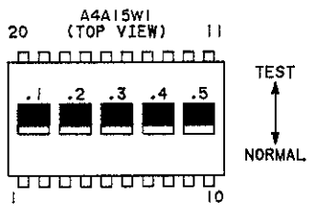
	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW

TRANSISTOR INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q19	1853-0314
Q20	1853-0405
U2	1826-0783
U5	1820-1202
U8,17,18	1826-0850
U9,14	1826-0889
U10	1820-1416
U13	1826-0264
U15,16	1820-1281
U19	1826-0412

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U8,17	+15V - 13 +5V - 12 ▽ - 5 -10V(F)- 4
U15,16	+5V - 16 ▽ - 8
U18	+20V - 13 +5V - 12 ▽ - 5 -10V(F)- 4



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P/O A4A1

Figure 8-530. P/O A4A1 Automatic Level Control Schematic

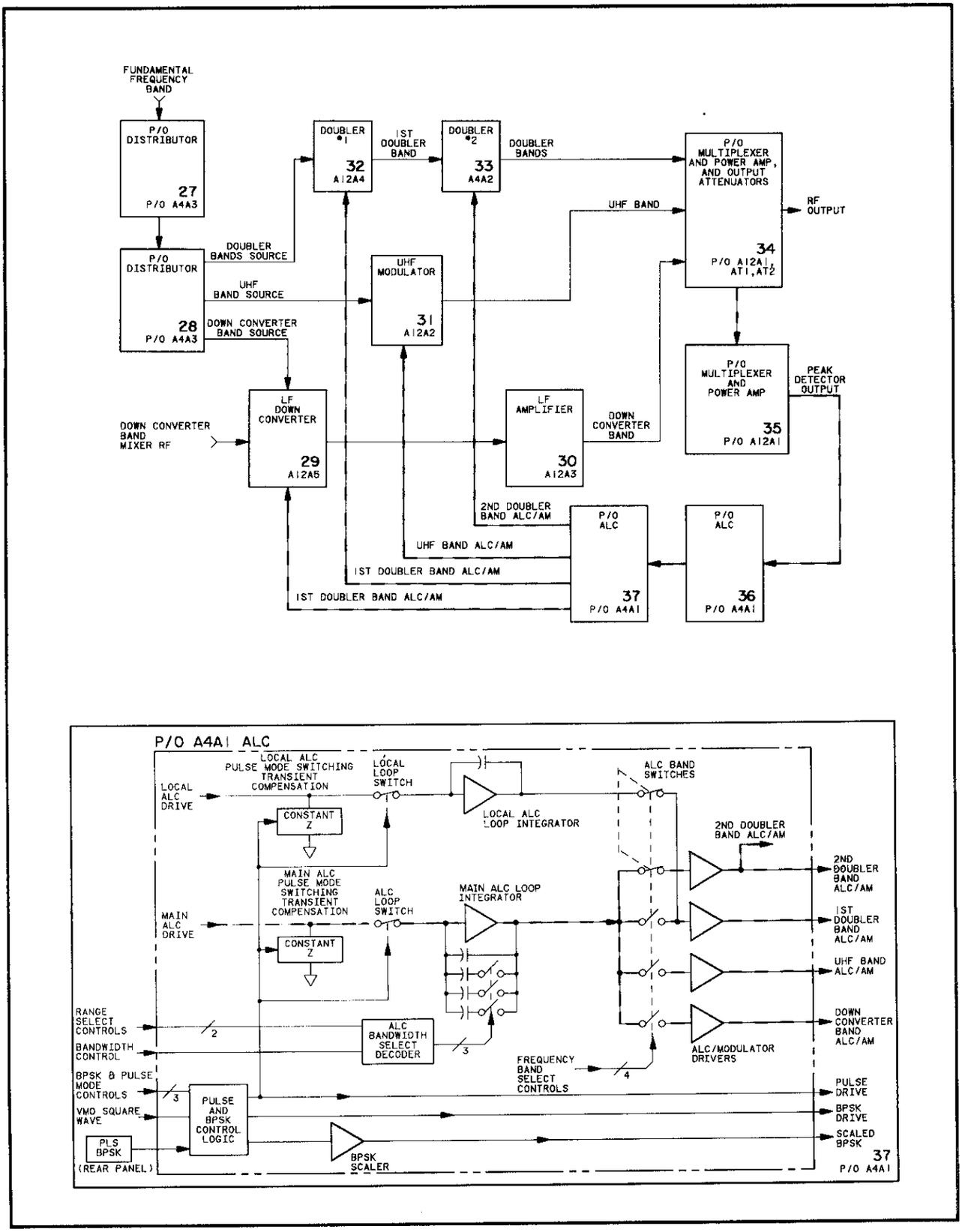


Figure 8-531. P/O A4A1 Automatic Level Control Block Diagrams

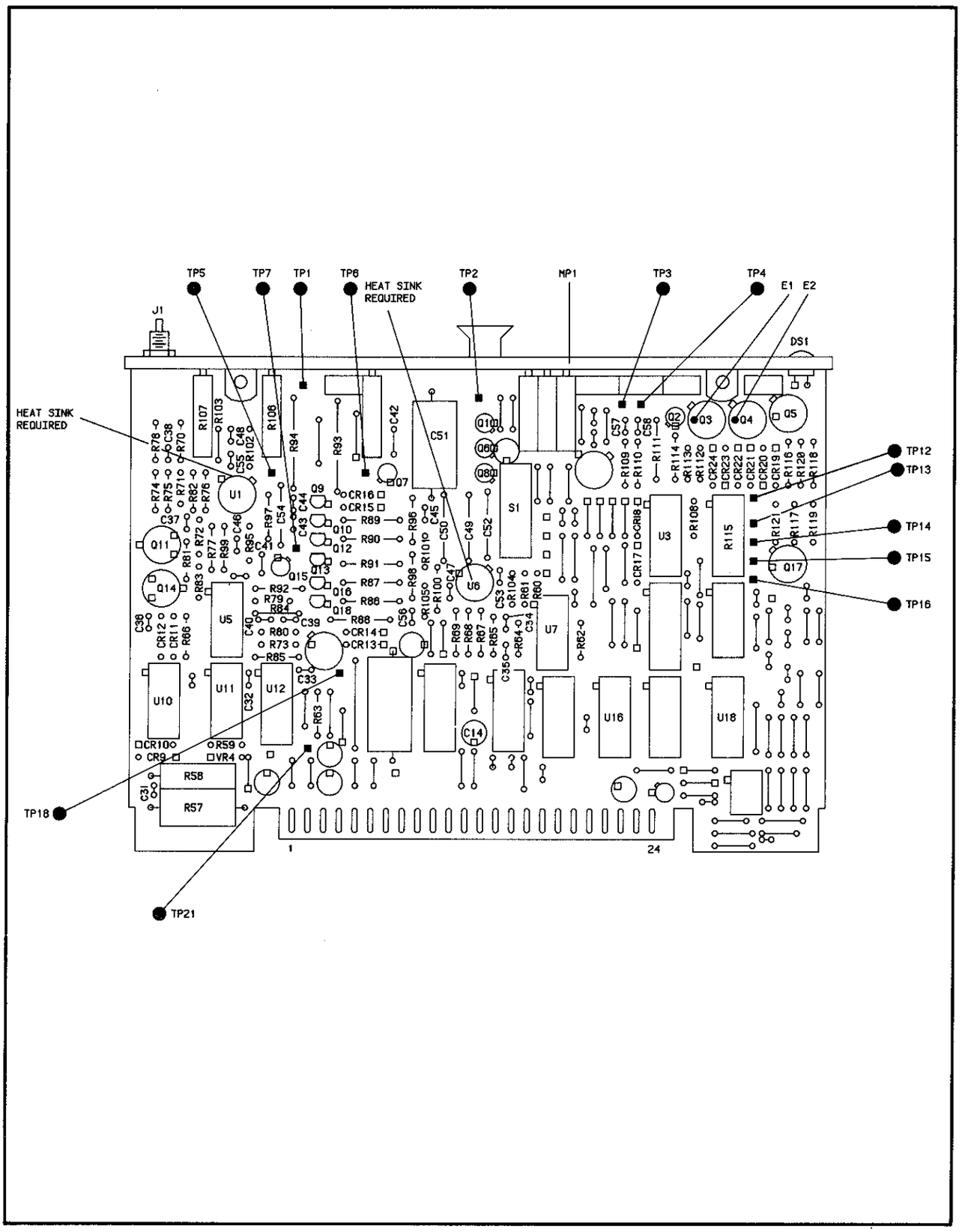
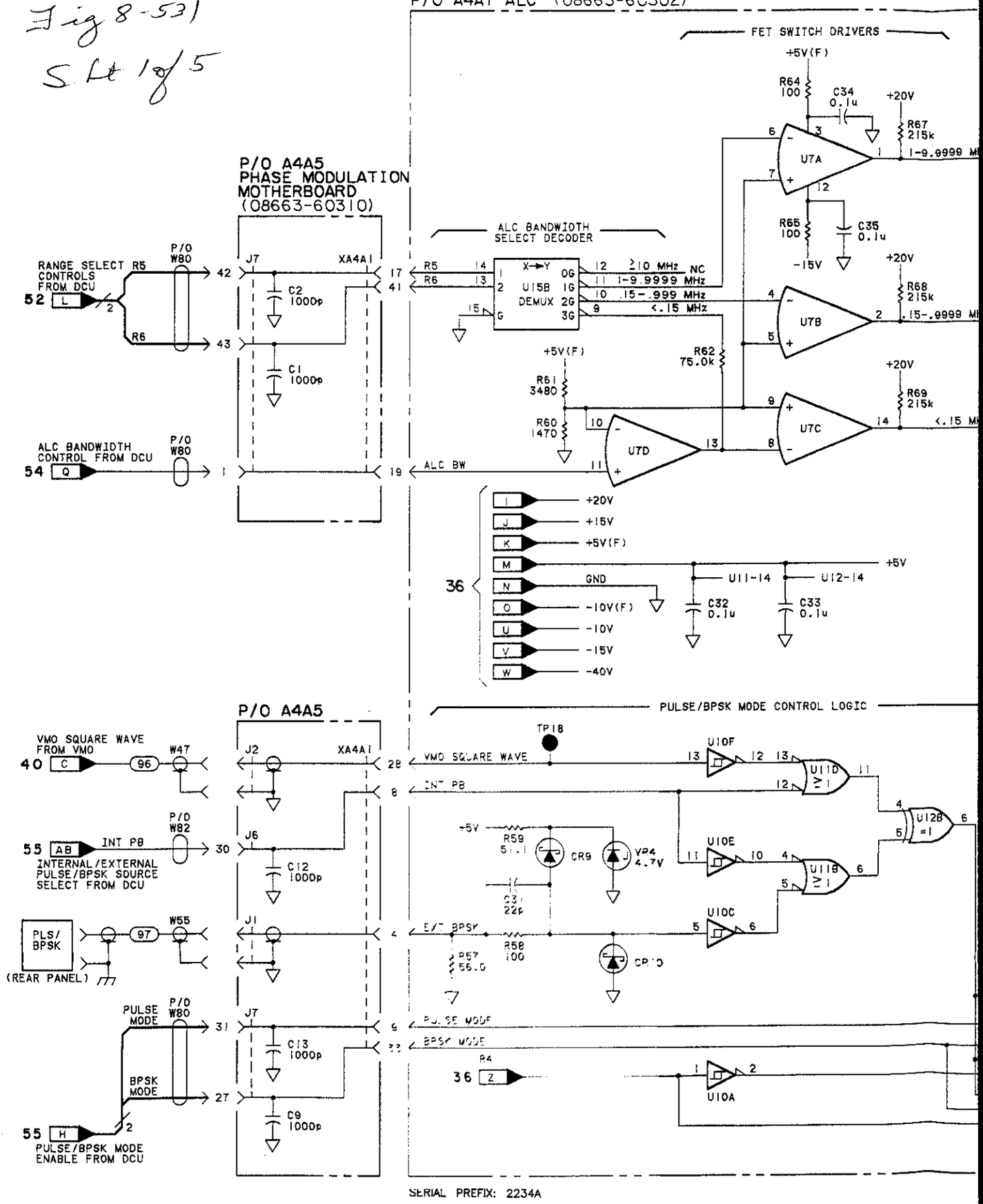


Figure 8-532. P/O A4A1 Automatic Level Control Component Locator

Fig 8-531
Sht 1 of 5



SERIAL PREFIX: 2234A

Fig 8-531 Sht 2 of 5

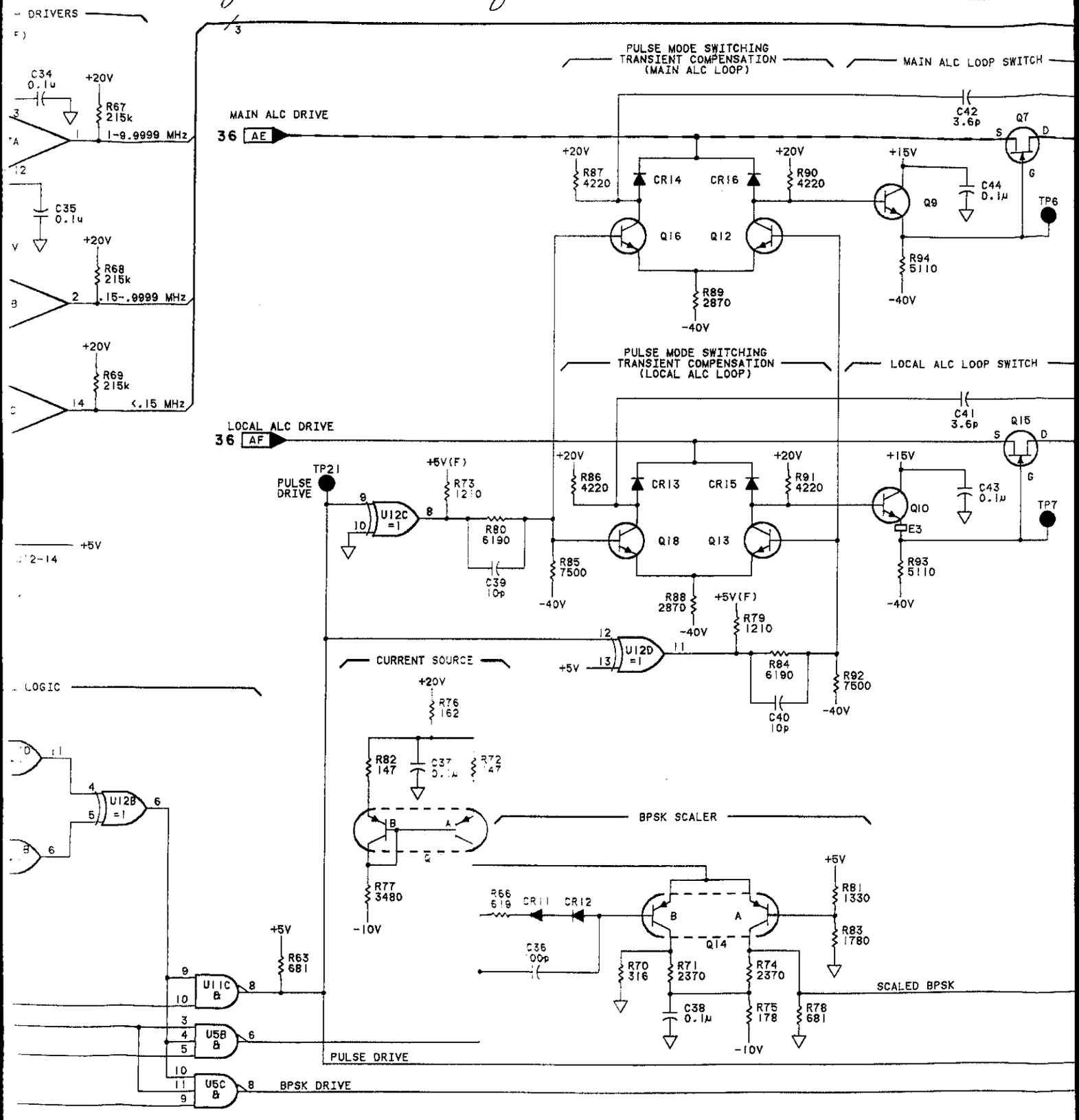


Fig 8-531 Sht 3 of 5

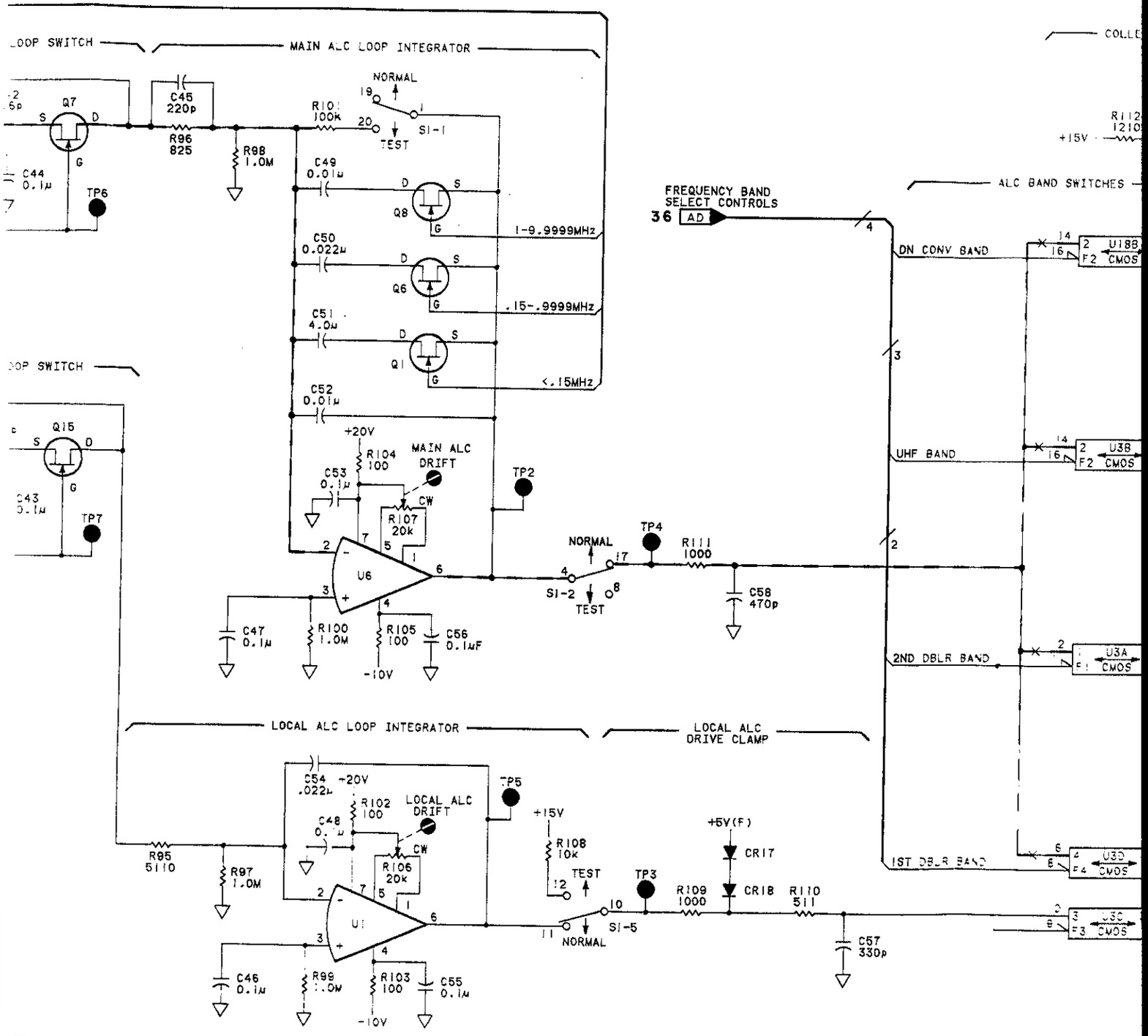


Fig 8-531 Sht 4 of 5

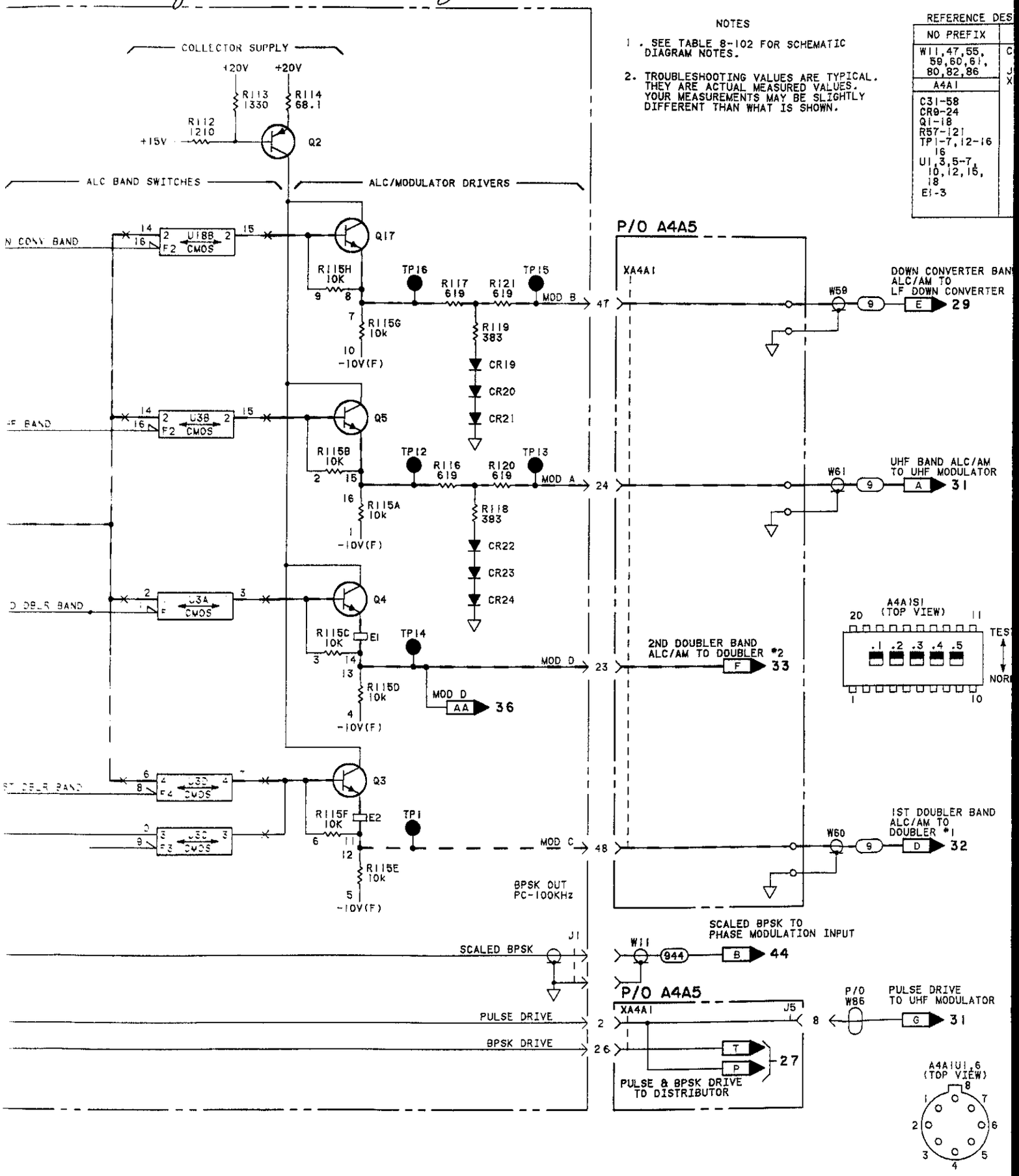


Fig 8-531
Sht 5 of 5

NOTES

1. SEE TABLE 8-102 FOR SCHEMATIC DIAGRAM NOTES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MAY BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

REFERENCE DESIGNATIONS

NO PREFIX	A4A5
W11,47,55, 59,60,61, 80,82,86	C1,2,9,12, 13
A4A1	J1,2,6,7 XA4A1
C31-58 CR9-24 Q1-18 R57-121 TP1-7,12-16 16 U1,3,5-7, 10,12,15, 18 E1-3	

LOGIC LEVELS

	TTL
HIGH	>+2V
LOW	<+0.8V
< IS MORE NEG.THAN > IS MORE POS.THAN	
OPEN	HIGH
GROUND	LOW

P/O A4A5

XA4A1

W59 — 9 — E — 29 — DOWN CONVERTER BAND ALC/AM TO LF DOWN CONVERTER

W61 — 9 — A — 31 — UHF BAND ALC/AM TO UHF MODULATOR

2ND DOUBLER BAND ALC/AM TO DOUBLER #2 — F — 33

W60 — 9 — D — 32 — 1ST DOUBLER BAND ALC/AM TO DOUBLER #1

W11 — 944 — B — 44 — SCALED BPSK TO PHASE MODULATION INPUT

P/O A4A5

XA4A1 — J5 — 8 — P/O W86 — G — 31 — PULSE DRIVE TO UHF MODULATOR

T — P — 27 — PULSE & BPSK DRIVE TO DISTRIBUTOR

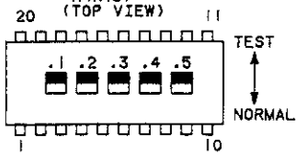
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,6-8,15	1855-0414
Q2	1853-0459
Q3-5,17	1854-0637
Q9,10,12, 13,16,18	1854-0811
Q11,14	1853-0316
U1,6	1826-0358
U3,18	1826-0850
U5	1820-1202
U7	1826-0347
U10	1820-1416
U11	1820-0681
U12	1820-1211
U15	1820-1281

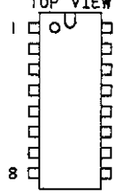
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U3,18	+20V - 13 +5V - 12 ▽ - 7
U15	-10V(f) - 4 +5V - 16 ▽ - 8

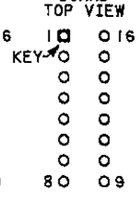
A4A1S1 (TOP VIEW)



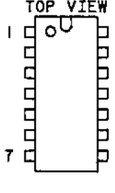
A4A1, U3,15,18 TOP VIEW



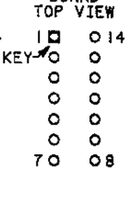
CIRCUIT BOARD TOP VIEW



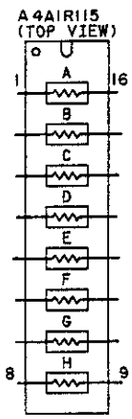
A4A1, U5,7,10,12 TOP VIEW



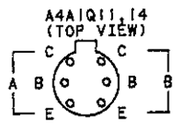
CIRCUIT BOARD TOP VIEW



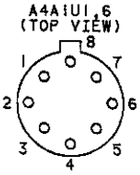
A4A1R15 (TOP VIEW)



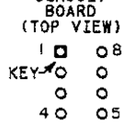
A4A1Q11,14 (TOP VIEW)



A4A1U1,6 (TOP VIEW)



CIRCUIT BOARD (TOP VIEW)



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P/O A4A1

Figure 8-531. P/O A4A1 Automatic Level Control Schematic

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