SERVICE SHEET BD3---Source Circuits Block Diagram

PRINCIPLES OF OPERATION

General

Service Sheet BD3 covers the source circuits which consist of the oscillator and its output circuits.

Oscillator (A5)

The Oscillator is conceptually similar to the Notch Filter in that it is a state-variable design; that is, it is formed by combining various circuit blocks which perform simple mathematical functions (amplification, inversion, summation, and integration). A simplified diagram of the basic oscillator is shown in Figure 8C-1. Each integrator causes 270° phase shift (that is, 90° plus an inversion) and the Sum Amplifier and Fine Tune circuits cause an inversion. Thus, there are 720° total phase shift around the loop which gives rise to positive feedback—a necessary condition for oscillation. The output of the circuit (not shown on the simplified diagram) is taken from Integrator 1.

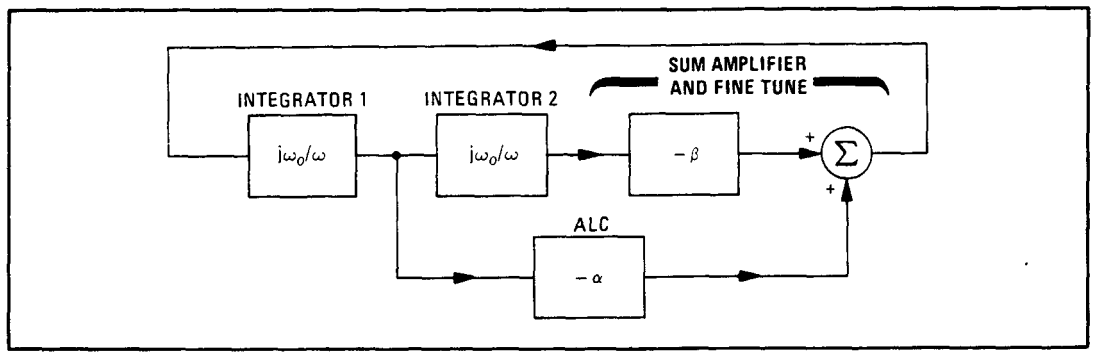


Figure 8C-1. Simplified Diagram of the Basic Oscillator

The equation governing the frequency of oscillation for the circuit is

$$s = \tfrac{1}{2}\omega_0(\alpha \pm \sqrt{\alpha^2 - 4\beta}),$$

where s is the complex frequency.

Assume for a moment that $\alpha = 0$. The radian frequency of oscillation consists only of the imaginary term and is

$$s = j\omega = j\omega_0\sqrt{\beta} = j2\pi f_0\sqrt{\beta}.$$

The frequency is coarse tuned by adjusting ω_0 in the simplified diagram (Rs and Cs in Integrators 1 and 2). Fine tuning is accomplished by adjustment of β. Tuning is done by the Controller which uses the Counter to check frequency. Special Functions 55, 56, and 57 can be used to manually set the tuning of the Oscillator.

To obtain stable, low-distortion oscillation at the prescribed frequency and level (3 Vrms) requires exact adjustment of gain α to obtain a purely imaginary term for s. If s contains a positive term, the amplitude of oscillation grows; if it contains a negative term, oscillation decays. Adjustment of α is done through the use of negative feedback in an automatic leveling control (ALC) circuit. The ALC circuit must correct for an amplitude disturbance (such as during a frequency change) within a few cycles of oscillation and yet introduce no distortion.

Refer now to Figure 8C-101. The leveling circuit consists of two Sample and Hold amplifiers, two error amplifiers, and a Level Setting Multiplier. Some of the important waveforms in the circuit are shown in Figure 8C-2. The figure shows the situation that occurs when the level suddenly decreases.

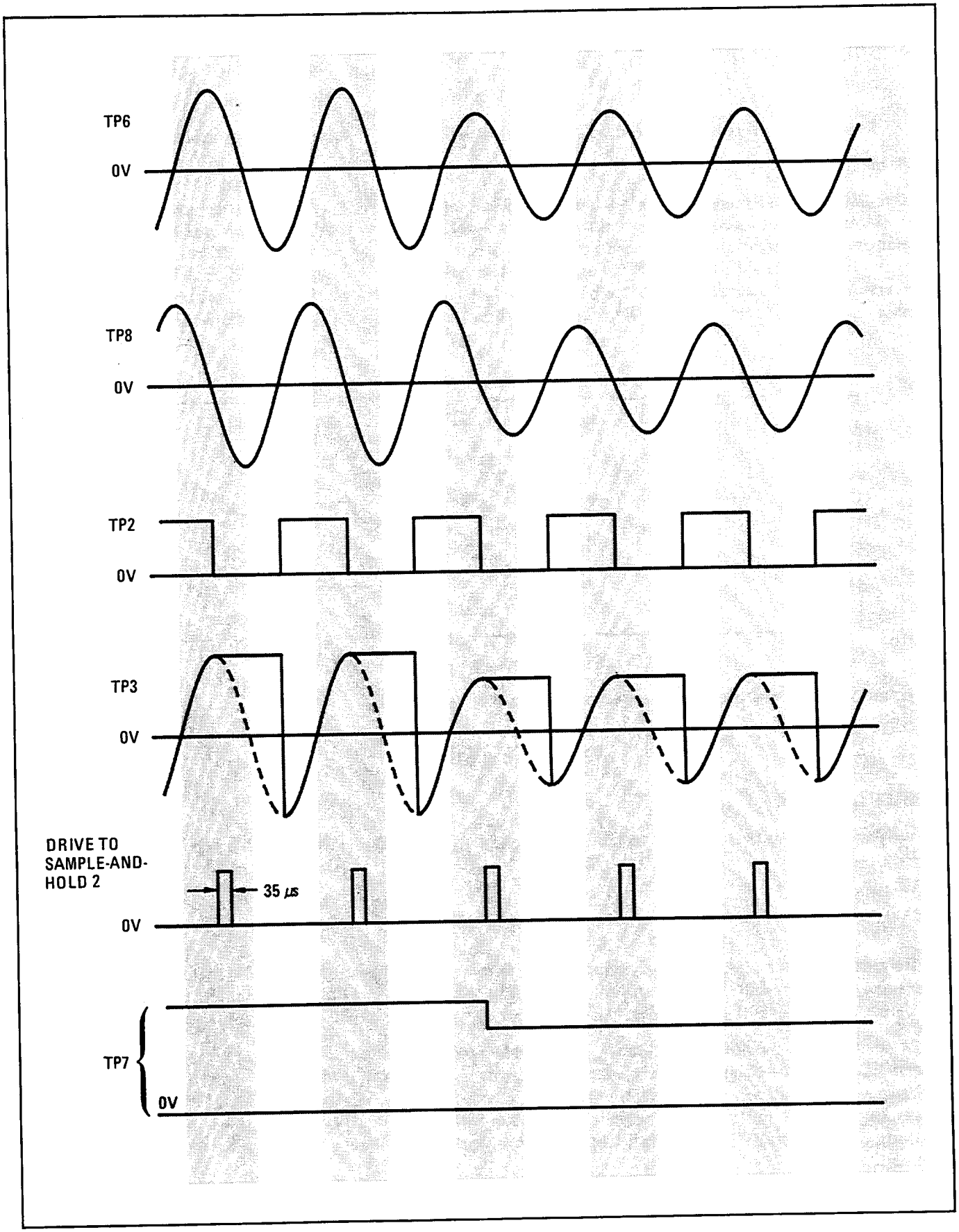


Figure 8C-2. Oscillator ALC Waveforms

The signal from Integrator 1 (at TP6) is buffered then sampled by Sample and Hold 1. The sampling switch is driven by a signal which is in phase with the output from Integrator 2 (at TP8) which lags the output of Integrator 1 by 90°. The sample switch drive voltage appears at TP2. When sampling begins (TP2 goes high), the output of Integrator 1 is at its negative peak. Sampling continues until the positive peak is reached (the negative-going zero crossing of Integrator 2) then the sampling switch opens and the peak voltage is held on a storage capacitor. (The circuit is thus a track-and-hold circuit.) The sampled signal, which has been buffered, appears at TP3. (In actuality, the buffer clips the negative peaks, but this is of little consequence.)

The negative going edge of the sample switch drive signal also triggers a 35 μs monostable multivibrator which closes the sample switch of Sample and Hold 2. The voltage from Sample and Hold 1 is then transferred to the storage capacitor of Sample and Hold 2 and then held. This signal, after being buffered, appears at TP7 and is a dc voltage equal to the peak of the signal from Integrator 1. (At high frequencies, the OR gate that drives the sampler switch holds the duty cycle at 50% even though the pulse width is less than 35 μs.)

This peak signal is compared against a very stable dc reference by the Proportional Error Amplifier. The amplified level error drives one input to the Level Setting Multiplier. The multiplier can be visualized as a variable-gain amplifier with an ac input from Integrator 1. The dc control input from the Proportional Error Amplifier controls the gain and polarity of this "amplifier". The output of the multiplier drives and input to the sum amplifier which injects a signal of the proper magnitude and phase to bring the output of Integrator 1 to the correct level.

The Proportional Error Amplifier provides coarse, fast-responding ALC action. The amplifier's output is also applied to the Error Integrator through a switch which is also driven by the 35 μs monostable multivibrator. The Error Integrator drives a second dc control input of the Level Setting Multiplier and provides exact ALC correction.

The complete loss of oscillation is sensed by the 200 ms Oscillator Restart monostable multivibrator. It is always retriggered by the signal from Integrator 2 unless the signal ceases. At that time a switch is momentarily closed to force a large restart error in the Proportional Error Amplifier. Normally, the oscillator will restart by the normal action of the ALC circuit, this circuit, however, provides a backup.

The ALC Loop Gain Adjust keeps the loop gain relatively constant regardless of signal level by adjusting the sensitivity of the multiplier to its control voltages. Thus the ALC loop reacts equally well for large or small signals which are produced momentarily during tuning.

Output Attenuator (A6)

The Oscillator is always on and outputs a constant level. The Output Attenuator circuits provide a controllable level to the OUTPUT connectors and also allow the signal to be effectively turned off.

Amplifier 1 is used for fine setting of the output level. Its gain can be programed from approximately −12 to 0 dB. The equation that governs the gain of Amplifier 1 is:

$$\text{gain} = (1 - 0.5M)\frac{N + 256}{511},$$

where N is an integer between 0 and 255 and M is either 0 or 1. In practice N is usually kept between 100 and 255 for a range of approximately 3 dB. M is set to 1 when the output is set to the "off" condition. The gain of Amplifier 1 can be manually programed by Special Functions 58 (which sets the value of N) and 59 (which sets the value of M).

Amplifier 2 is programed from approximately −17.5 to 0 dB gain in 2.5 dB steps. In the "off" condition, the gain is set to approximately −60 dB. The gain of Amplifier 2 can be manually controlled by Special Function 59.

Attenuator A is a programmable, passive voltage divider with an attenuation of 0, 20, or 40 dB and an "off" state (a short to ground). The attenuation can be manually controlled by Special Function 59.

The Output Amplifier Driver has a fixed gain of 1.9 (+5.58 dB). It prevents the Floating Output Amplifier from loading Attenuator A.

The Floating Output Amplifier has a gain of 1.12 and has differential outputs. The LOW OUTPUT connector can be conveniently grounded or floated by a front-panel switch. The output impedance of the amplifier itself is 50Ω.

Attenuator B is a floating, 50Ω attenuator which can be programed to 0 or 20 dB. The attenuation of Attenuator B can be manually controlled by Special Function 59. The impedance of the source can be set to either 50Ω or 600Ω. For instruments with serial prefix 2730A and below, this is implemented with a non-programmable front panel switch. For instruments with serial prefix 2742A and above, Special Function 47.X is used to select the output impedence. This feature enables the user to program the output impedence of the source via HP-IB as well as from the front panel.

If an external voltage exceeding +12 or −12V is applied to the HIGH or LOW OUTPUT connector, the Over-Voltage Detector opens the two relays in the output paths. The Relay Drive-One Shot holds the relays open for 1s after the over-voltage condition has been removed to prevent relay chatter if the overload signal is pulsing. The Voltage Clamp protects the output circuits from the initial overvoltage transient until the relays open.

TROUBLESHOOTING

General

Procedures for checking the source circuits of the instrument are given below. The blocks or points to check are marked on the bolck diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. The procedures assume that the measurement circuits of the instrument (for example, AC Level and Frequency) are working properly. A second Audio Analyzer is needed only if distortion is out of specification and it cannot be determined whether the instrument's source or distortion measurement is at fault. Before performing any check, perform all the checks on Service Sheet BD1.

Equipment

Audio Analyzer ..... HP 8903B or HP 339A
Oscilloscope ..... HP 1740A
Power Supply ..... HP 6215A

⟨✓1⟩ Oscillator Tuning Check

NOTE

This check assumes that the internal reference frequency is properly adjusted; see paragraph 5-7.

1. Key in 41.0 SPCL to initialize the instrument. Set the INPUT switch to ground. Set the 80 kHz LOW PASS filter off. Connect A5TP6 (OSC 1) to the HIGH INPUT with a short cable.

2. Key in 55.3 SPCL, 56.128 SPCL, and 57.128 SPCL to set the Oscillator frequency to its highest range, middle coarse tune, and middle fine tune settings. The frequency should be between 55.3 and 57.3 kHz. The amplitude should be between 2.65 and 3.05 Vrms.

Hint: If there is no signal, short A5TP9 (ALC) to A5TP6 (OSC 1). If a signal now appears with the frequency approximately correct but the amplitude is about 2 Vrms, perform ⟨✓2⟩ *Oscillator Leveling Check.* If there still is no signal, the fault probably lies with the frequency range and coarse tune circuits; continue on with the following steps to determine which tuning circuits are not responding properly.

Hint: If the signal is present at approximately the correct frequency but the level is incorrect, perform ⟨✓2⟩ *Oscillator Leveling Check* or if only slightly out of limits perform the *Oscillator and Output Attenuator Adjustment,* paragraph 5-15.

Hint: If the signal level is correct but the frequency is incorrect, continue with the following steps to determine which tuning circuits are not responding properly.

3. Key in the following Special Functions and observe the frequency. The frequency should be within the limits shown in Table 8C-1.

Table 8C-1. Frequency Limits at A5TP6, ⟨✓1⟩ Step 3

Special Functions	Frequency Limits (Hz)	
	Minimum	Maximum
55.2	6930	7810
55.1	856	887
55.0	108.7	112.7

Hint: If the frequencies for Special Functions 55.0 to 55.3 are all out of limits, continue with the following steps to determine which tuning circuits are not responding properly. If at least one frequency, but not all

frequencies, for Special Functions 55.0 to 55.3 are correct, see Service Sheet 8 and check the range switching circuits.

4. Key in 55.2 SPCL. Key in the pairs of Special Functions shown in Table 8C-2 and observe the frequency for each Special Function. Calculate the percent change in frequency between the first and second Special Function. For example, if the frequency for 56.128 SPCL is 7040.5 Hz and for 56.127 SPCL is 6994.3 Hz the percent change frequency is

$$\text{Frequency Change} = \frac{6994.3 - 7040.5}{7040.5} \times 100\% = -0.66\%.$$

The frequency change should be within the limits shown. If faulty, see Service Sheet 8 and check the coarse tune switching circuits.

Table 8C-2. Limits of Frequency Change at A5TP6, ⟨✓1⟩ Step 4

Special Functions	Limits of Frequency Change (%)	
	Minimum	Maximum
56.128, 56.127	−1.37	−0.14
56.64, 56.63	−2.13	−0.88
56.32, 56.31	−3.67	−2.38
56.16, 56.15	−6.77	−5.38
56.8, 56.7	−12.9	−11.3
56.4, 56.3	−25.8	−22.7
56.2, 56.1	−49.9	−47.9

5. Key in 56.128 SPCL. Key in 57.255 SPCL and note the frequency, then key in 57.0 SPCL and note the frequency. Calculate the ratio: (frequency for 57.255 SPCL) ÷ (frequency for 57.0 SPCL). The ratio should be between 1.105 and 1.113. If faulty, see Service Sheet 8 and check the fine tune switching circuits.

6. Key in the following pairs of Spcial Functions and check that the frequency for the second entry is higher than the frequency for the first entry. If faulty, see Service Sheet 8 and check the fine tune switching circuits.

Special Functions	Special Functions
57.254, 57.255	57.239, 57.240
57.253, 57.254	57.223, 57.224
57.251, 57.252	57.191, 57.192
57.247, 57.248	57.127, 57.128

7. Key in FREQ 20 Hz. The frequency should read between 19.94 and 20.6 Hz. If faulty, see Service Sheet 8.

8. Key in FREQ 100 kHz. The frequency should read between 99.7 and 100.3 kHz. If faulty, see Service Sheet 8.

⟨✓2⟩ Oscillator Leveling Check

1. On the Audio Analyzer, key in 41.0 SPCL to initialize the instrument. Connect a high-impedance, dc coupled oscilloscope to A5TP6 (OSC 1). The waveform should be an undistorted sine wave with an amplitude between 7 and 9 Vpp and a period of approximately 1 ms.

Hint: If no signal is present, short A5TP9 (ALC) to A5TP6 (OSC 1). The waveform should be a distorted sine wave with an amplitude between 6 and 8 Vpp and a period of approximately 1 ms. If there is now a signal, continue on with step 2. If there still is no signal, see Service Sheet 8 and check the analog ICs.

Hint: If the signal is proper, continue on with step 9.

2. Connect the oscilloscope to A5TP2 (S/H GATE). The waveform should be a TTL square wave with a period of approximately 1 ms. If faulty, see Service Sheet 9 and check the Zero Crossing Detector.

3. Connect the oscilloscope to A5TP3 (S/H). The waveform should be as shown in Figure 8C-3. If faulty, see Service Sheet 9 and check Sample and Hold 1.

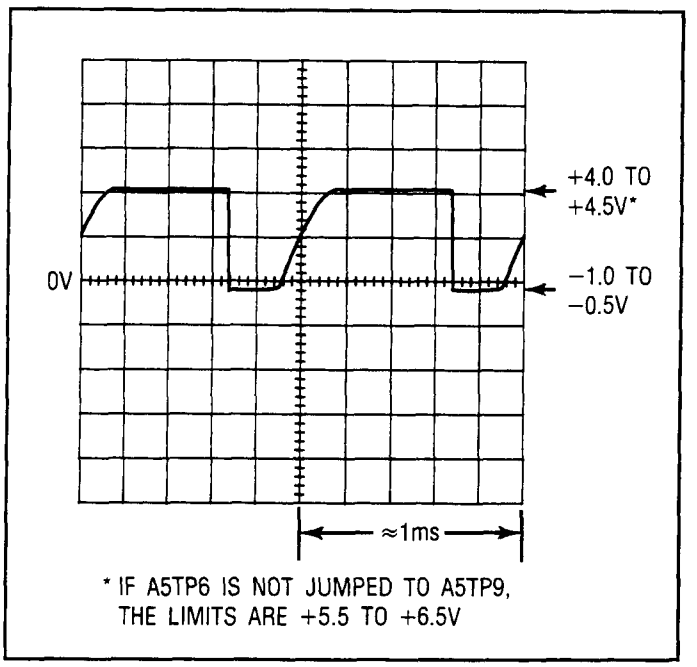


Figure 8C-3. Oscilloscope Waveform at A5TP3, ⟨J2⟩ Step 3

4. Connect the oscilloscope to A5TP7 (V PEAK). The waveform should be a dc level equal to the peak voltage noted in step 1. If faulty, see Service Sheet 9 and check Sample and Hold 2.

5. Short A5TP9 (ALC) to A5TP6 (OSC 1) if not already shorted. Connect the oscilloscope to A5TP5 (PROP ERROR). The waveform should be a dc level greater than +2 Vdc. If faulty, see Service Sheet 9 and check the Proportional Error Amplifier.

6. Short A5TP9 (ALC) to ground. The waveform should be a dc level less than −2 Vdc. If faulty, see Service Sheet 9 and check the Proportional Error Amplifier.

7. Connect the oscilloscope to A5TP11 (INT ERROR). The waveform should go to about +1 Vdc then drift slowly to 0 Vdc. If faulty, see Service Sheet 9 and check the Error Integrator.

Hint: If the signal in step 6 is correct, but the signal of step 1 was either at an incorrect level or required the jumper between A5TP6 adn A5TP9, see Service Sheet 9 and check the Level Setting Multiplier and Reference.

8. Remove the short on A5TP9. Jumper A5TP6 to A5TP9. The waveform should be less than −1 Vdc (and will have some 1 kHz ripple). If faulty, see Service Sheet 9 and check the Error Integrator. (See also the hint under step 7.)

9. Remove the jumper between A5TP6 and A5TP9, if present. Connect the oscilloscope to A5TP6. Key in FREQ 20 Hz. The waveform should be an undistorted sine wave with an amplitude of 7.5 to 9.5 Vpp and a period of approximately 50 ms. If faulty, see Service Sheet 9.

10. Key in FREQ 100 kHz. The waveform should be an undistorted sine wave with an amplitude of 7.5 to 9.5 Vpp and a period of approximately 10 μs. If faulty, see Service Sheet 9.

⟨✓3⟩ Output Attenuator Check

1. Key in 41.0 SPCL to initialize the instrument. Set the INPUT and OUTPUT switches to ground. Set IMPEDANCE to 600Ω.

NOTE

In the following checks the limits of the levels measured assume a source loading of 100 kΩ (the impedance of the HIGH INPUT). Use of a high-impedance ac voltmeter may give erroneous readings.

2. Connect A5TP6 (OSC 1) to the HIGH INPUT. The amplitude should be between 2.7 and 3.0 Vrms and the frequency should be approximately 1 kHz. If the frequency is faulty, see Oscillator Tuning. If the amplitude is faulty, see ⟨✓2⟩ *Oscillator Leveling Check.*

3. Press RATIO. Connect A6TP6 (AMP 1) to the HIGH INPUT. Key in 59.0 SPCL and the Special Functions listed in Table 8C-3. For each setting, the amplitude ratio should be within the limits indicated. If faulty, see Service Sheet 10 and check Amplifier 1.

Table 8C-3. Amplitude Ratio Limits at A6TP6, ⟨✓3⟩ Step 3

Special Function	Amplitude Ratio Limits (%)	
	Minimum	Maximum
58.255	100.40	101.40
58.127	75.25	76.00
58.63	62.67	63.30
58.31	56.39	56.95
58.15	53.24	53.78
58.7	51.67	52.19
58.3	50.89	51.40
58.1	50.49	51.00
58.0	50.30	50.80

4. Key in 58.255 SPCL and 59.32 SPCL to activate the "off" state. The relative amplitude should be between 50.2 and 50.7%.

5. Key in 59.0 SPCL. Press RATIO twice to establish a new reference. Connect A6TP5 (AMP 2) to the HIGH INPUT.

6. Key in the Special Functions listed in Table 8C-4. For each setting, the amplitude ratio should be within the limits indicated. If faulty, see Service Sheet 10 and check Amplifier 2.

7. Key in 59.0 SPCL. Press RATIO twice. Connect A6TP4 (AMP 3) to the HIGH INPUT.

8. Key in the Special Functions listed in Table 8C-5. For each setting, the amplitude ratio should be with in the limits indicated. If faulty, see Service Sheet 10 and check Attenuator A and the Output Amplifier Driver.

9. Key in 59.0 SPCL. Press RATIO twice. Connect A6TP3 (FLT HI) to the HIGH INPUT. The relative amplitude should be between 111 and 113%. If faulty, see Service Sheet 11 and check the Floating Amplifier.

10. Connect the HIGH OUTPUT to the HIGH INPUT. The relative amplitude should remain between 111 and 112%. If faulty, see Service Sheet 11 and check Attenuator B.

11. Press RATIO twice. Key in 59.8 SPCL. The relative amplitude should be between 9.9 and 10.1%. If faulty, see Service Sheet 11 and check Attenuator B.

Table 8C-4. Amplitude Ratio Limits at A6TP5, ⟨✓3⟩ Step 6

Special Function	Amplitude Ratio Limits (%)	
	Minimum	Maximum
59.0	98.33	99.32
59.1	73.75	74.49
59.2	55.29	55.84
59.3	41.49	41.91
59.4	31.09	31.41
59.5	23.32	23.55
59.6	17.49	17.67
59.7	13.12	13.25
59.32	–	0.10

Table 8C-5. Amplitude Ratio Limits at A6TP4, ⟨✓3⟩ Step 8

Special Function	Amplitude Ratio Limits (%)	
	Minimum	Maximum
59.0	188	192
59.16	18.8	19.2
59.24	1.88	1.92
59.32	–	0.01

12. Key in 59.0 SPCL. Set IMPEDANCE to 50Ω. The relative amplitude should raise by 0.6% (to a nominal 100.6%). If faulty, see Service Sheet 11 and check the impedance switch relay.

13. Press RATIO twice. Connect the HIGH INPUT to the LOW OUTPUT. Set the LOW OUTPUT switch to FLOAT. Short the center conductor of the HIGH OUTPUT connector to ground. The right display should read between 94.7 and 95.7%. If faulty, see Service Sheet 11 and check the Floating Output Amplifier.

14. Disconnect the short from the HIGH OUTPUT connector. Press S (Shift) DC LEVEL. Connect a dc power supply to the HIGH INPUT. Set the supply to +12.5 to +13.5 Vdc.

15. Connect the power supply to the HIGH OUTPUT then the LOW OUTPUT. For each connection relay K2 should audibly click when the supply is connected then click again 1s after it is removed. If faulty, see Service Sheet 11 and check the Over-Voltage Protect circuits.

16. Connect the power supply again to the HIGH INPUT. Set the supply to −13.5 and −12.5 Vdc.

17. Repeat step 15.

⟨✓4⟩ Source Distortion Check

NOTE

This check is used to pinpoint the source of distortion when it is slightly out of specification. Use an external distortion analyzer unless it is known that the internal distortion analyzer is operating properly.

1. On the Audio Analyzer, key in 41.0 SPCL to initialize the instrument. Set the INPUT and OUTPUT switches to ground. Key in AMPTD 6 V.

2. Connect a distortion analyzer to the test points listed in Table 8C-6 and measure the distortion. Set the low-pass filter of the distortion analyzer to 30 kHz. The distortion should be less than 0.01% in each case. If faulty, see the service sheet and check the circuits listed in Table 8C-6.

Table 8C-6. Source Distortion Troubleshooting, ⟨J4⟩ Step 2

Test Point	Service Sheet	Most Probable Cause
A5TP6 (OSC 1)	9	Oscillator Leveling
A6TP6 (AMP 1)	10	Amplifier 1
A6TP5 (AMP 2)	10	Amplifier 2
A6TP4 (AMP 3)	10	Output Amplifier Driver
HIGH OUTPUT	11	Floating Output Amplifier

SERVICE SHEET 8---A5 Oscillator Assembly (State-Variable Circuits)

PRINCIPLES OF OPERATION

General

This portion of the Oscillator Assembly (A5) contains the basic state-variable circuitry which generates a signal at a specific frequency. (See the discussion of the Oscillator on Service Sheet BD3.) It includes two integrators, a fine tune circuit, a sum amplifier, and their control circuitry.

Integrators

The two integrators are nearly identical. A simplified diagram of an integrator is shown in Figure 8B-32 (in the discussion of the Notch Filter). For Integrator 1, FETs Q12 through Q14 switch the feedback capacitors to change ranges. FETs Q4 through Q11 switch the input resistors to coarse tune the oscillator. The FETs are driven by the Oscillator Control Drivers whose control inputs come from the Controller via the Latch Assembly (see Service Sheet 12).

Fine Tune

Fine tuning is accomplished by varying the total amount of input current from Integrator 2 into the Sum Amplifier U5. The Fine Tune circuit inverts the output from Integrator 2. Its gain is determined by the closing of FETs Q28 to Q31 and the switches of U19. The output of U12B produces a current in R60 of opposite polarity to the current in R57.

Sum Amplifier

The Sum Amplifier sums the currents from Integrator 2 and the Fine Tune via R57 and R60 and the current from the ALC circuit (see Service Sheet 9). The currents from Integrator 2 affect the Oscillator frequency, and the current from the ALC circuit affects the level.

TROUBLESHOOTING

General

Procedures for checking the Oscillator Assembly are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are shown on the schematic also inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements. These procedures assume that the measurement circuits of the instrument (for example, ac level and frequency) are working properly.

Equipment

Oscilloscope ..... HP 1740A

⟨✓1⟩ Tuning Check

1. On the Audio Analyzer, key in 41.0 SPCL to initialize the instrument. Set the INPUT and OUTPUT switches to ground. Key in AMPTD 3 V. Key in 55.3 SPCL, 56.255 SPCL, and 57.255 SPCL to set the Oscillator frequency to its highest range, coarse tune, and fine tune settings. Connect the HIGH OUTPUT to the HIGH INPUT.

2. Connect a high-impedance, dc coupled oscilloscope to A5TP6 (OSC 1), A5TP8 (OSC 2), then A5TP4 (OSC 3). Use a low-capacitance 10:1 divider probe. The dc level should be between −50 and +50 mVdc at A5TP6 and A5TP4 and between −250 and +250 mVdc at A5TP8. The ac level at A5TP6 and A5TP8 should be between 8.3 and 8.7 Vpp. The frequency should be between 110 and 130 kHz.

Hint: If the dc level is out of limits, check U4, U5, and U11. The amplifiers are connected in a negative dc feedback loop; a failure in one amplifier will upset the bias of the others. Check that the output voltages have the proper sense. (For example, a positive offset at pin 2 of U4 should result in a negative output at pin 6. It should approach −15V.)

Hint: If the dc level is correct but there is no ac signal, short A5TP9 (ALC) to A5TP6. If a signal now appears with the frequency approximately correct but an amplitude of about 5.5 Vpp, see Service Sheet 9 and check the Oscillator leveling circuits. The signal will be distorted.

Hint: If the dc and ac levels are correct but the frequency is incorrect, continue with the following steps to determine which tuning circuits are not responding properly.

3. On the Audio Analyzer, key in the Special Functions listed in Table 8C-7. For each setting, connect the oscilloscope to the drains of the FETs indicated. (Use a probe.) A signal of several volts should be present when 55.3 SPCL is keyed in, but not when the Special Function listed is keyed in. If the signal is faulty, also check the control line indicated. (All control lines should be −15V for 55.3 SPCL.)

Table 8C-7. Check of FET Drains, ⟨✓1⟩ Step 3

Special Function	Drains to Check	Level (Vdc) at U18 Pin		
		1	2	14
55.2	Q12, Q25	0	−15	−15
55.1	Q13, Q26	−15	0	−15
55.0	Q14, Q27	−15	−15	0

4. On the Audio Analyzer, key in 55.2 SPCL. Key in the Special Functions listed in Table 8C-8. For each setting, connect the oscilloscope to the drains of the FETs indicated. A signal of several volts should be present when the Special Function is keyed in, but not when 56.255 is keyed in. If the signal is faulty, also check the control lines indicated. (All control lines should be 0 Vdc for 56.255 SPCL.)

Table 8C-8. Check of FET Drains, ⟨√1⟩ Step 4

Special Function	Drains to Check	Level (Vdc) at U17 Pin				Level (Vdc) at U16 Pin			
		2	14	13	1	2	1	13	14
56.254	Q6, Q19	0	0	0	0	0	0	0	−15
56.253	Q7, Q20	0	0	0	0	0	0	−15	0
56.251	Q4, Q17	0	0	0	0	0	−15	0	0
56.247	Q5, Q18	0	0	0	0	−15	0	0	0
56.239	Q8, Q21	0	0	0	−15	0	0	0	0
56.223	Q11, Q24	0	0	−15	0	0	0	0	0
56.191	Q10, Q23	0	−15	0	0	0	0	0	0
56.127	Q9, Q22	−15	0	0	0	0	0	0	0

5. On the Audio Analyzer, key in 56.255 SPCL. Key in the Special Functions listed in Table 8C-9. For each setting, connect the oscilloscope to the drain of the FET indicated. A signal of several volts should be present when the Special Function is keyed in, but not when 57.0 is keyed in. If the signal is faulty, also check the control lines indicated. (All control lines should be 0 Vdc for 57.0 SPCL.)

Table 8C-9. Check of FET Drains, ⟨√1⟩ Step 5

Special Function	Drain to Check	Level (Vdc) at U20 Pin			
		2	1	14	13
57.128	Q31	0	0	0	−15
57.64	Q30	0	0	−15	0
57.32	Q29	0	−15	0	0
57.16	Q28	−15	0	0	0

6. On the Audio Analyzer, key in the Special Functions listed in Table 8C-10. For each setting, connect the oscilloscope to the pin of U19 indicated. A signal of several volts should be present when the Special Function is keyed in, but not when 57.15 is keyed in. If the signal is faulty, also check the control lines indicated. (All control lines should be a TTL high for 57.15 SPCL.)

Table 8C-10. TTL Levels at A5U19, ⟨√1⟩ Step 6

Special Function	Pin On U19 to Check	Level (TTL) at U19 Pin			
		1	8	9	16
57.7	15	H	H	H	L
57.11	10	H	H	L	H
57.13	7	H	L	H	H
57.14	2	L	H	H	H

Hint: This step concludes a check of the functioning of the tuning circuits. If the fault is excessive distortion (particularly at low frequencies), the cause may be a leaky FET switch. The particular FET can be ascertained by observing which switch is on when the distortion goes away. If the fault is a frequency error as observed in the *Oscillator Tuning Check* of Service Sheet BD3, the faulty resistor or FET switch can be ascertained by noting which Special Functions give correct readings and which do not. Table 8C-11 should assist in correlating the Special Functions and range switches.

Table 8C-11. Special Function 55.N Vs. Range Switches Closed, ⟨J1⟩ Step 6 Hint

Special Function	Switches Closed
55.3	None
55.2	Q12, Q25
55.1	Q13, Q26
55.0	Q14, Q27

Table 8C-12 should assist in correlating the Special Functions and the coarse-tune switches.

NOTE

For Special Function 56.N, let N=N8+N7+N6+N5+N4+N3+N2+N1. The value of N determines which switches are closed. For example, 56.18 SPCL will close Q8, Q21, Q7, and Q20. N5+N2=16+2=18.

Table 8C-12. Special Function 56.N Vs. Coarse-Tune Switches Closed, ⟨J1⟩ Step 6 Hint

Component of N	Value	Switches Closed
N8	128	Q9, Q22
N7	64	Q10, Q23
N6	32	Q11, Q24
N5	16	Q8, Q21
N4	8	Q5, Q18
N3	4	Q4, Q17
N2	2	Q7, Q20
N1	1	Q6, Q19

Table 8C-13 should assist in correlating the Special Functions and the fine-tune switches.

NOTE

For Special Function 57.N, let N=255-(N8+N7+N6+N5+N4+N3+N2+N1). The value of N determines which switches are closed as follows. For example, 57.237 SPCL closes switches U19D and U19B. 255-N5-N2=255-16-2=237.

Table 8C-13. Special Function 57.N Vs. Fine-Tune Switches Closed, ⟨J1⟩ Step 6 Hint

Component of N	Value	Switch Closed
N8	128	Q31
N7	64	Q30
N6	32	Q29
N5	16	Q28
N4	8	U19D
N3	4	U19C
N2	2	U19B
N1	1	U19A

7. On the Audio Analyzer, ground A5TP9 (ALC). Key in 55.3 SPCL, 56.1 SPCL, and 57.0 SPCL. Connect the oscilloscope to A5TP6. The waveform should be less than 2 mVpp and between −50 and +50 mVdc.

Hint: If the signal is too large, an FET switch is leaking. A leaking FET will cause excessive distortion at 20 Hz.

SERVICE SHEET 9---A5 Oscillator Assembly (ALC Circuits)

PRINCIPLES OF OPERATION

General

This portion of the Oscillator Assembly (A5) contains the ALC circuitry which senses the level of the output and injects into the oscillator circuitry a signal of proper phase and amplitude to correct for any error in the Oscillator output level.

Sample-and-Hold Circuits

The output of the sample-and-hold circuits is a dc voltage equal to the positive peak of the Oscillator output. The sample switch, FET Q16, of Sample-and-Hold 1 is driven in quadrature with the signal which is to be sampled. The quadrature drive comes from Integrator 2 of the Oscillator (see Service Sheet 8) via the Zero-Crossing Detector. The Zero-Crossing Detector produces a low output whenever its input is less than 0V. R67 and R70 provide a small amount of hysteresis to assure a rapid and complete output transition once it begins. The output is inverted by NOR gate U1B and translated to a level compatible with Q16 by U8D. A low on the output of U8D (−15V) turns Q16 off; a high (output off) permits Q16 to be turned on by the low gate-to-source resistance of R84.

The signal to be sampled comes from Integrator 1 of the Oscillator. It is buffered by a unity-gain amplifier, U9 and Q2. Q2 boosts the current-drive capability of the amplifier since it must drive a capacitor, C39, when Q16 is on. Sampling begins at the negative peak of the input signal and continues to the positive peak when Q16 shuts off—holding the signal peak on C39. (CR5 actually clamps the negative level to −0.6V.) The circuit thus performs a track-and-hold function. The peak dc voltage is buffered by a high-impedance, unity-gain amplifier, U13.

The sampled peak is further sampled by Sample-and-Hold 2. The sample-and-hold switch, FET Q15, is also driven by the quadrature signal, but the length of the drive pulse is shortened to 35 μs or less by U1C. Monostable multivibrator U7A is triggered by the quadrature signal. Its duration is 35 μs. Its low-true output is combined with the quadrature signal in NOR gate U1C. Should the half-period of the quadrature signal be less than 35 μs, U7A is retriggered before its timeout is completed. The output pulses of U1C, then, have a duration less than 35 μs.

The output from U1C is translated to a level compatible with Q15 by U8C (similar to U8D). A signal out of phase with the output to the gate of Q15 is fed through C46 to cancel the turn-on spikes created by the junction capacitances of Q15. The guard traces surrounding the ungrounded nodes of C39 and C45 hold the surrounding printed circuit board area at a potential that is approximately equal to the level being held on the capacitors. Leakage currents, caused by potential differences near the capacitors, thus flow to the guard trace and to the output of U13 or U14 rather than to the capacitor. The sampled output is buffered by U14.

Level Error Amplifiers and Level Setting Multiplier

The ac signal from the Oscillator is fed into one input (−X) of the Level Setting Multiplier (U6, U12A, and associated components). The multiplier, U6, acts as a variable-gain amplifier. The gain of the multiplier is proportional to the difference in voltage between the two Y inputs. The sense of the gain (that is, inverting or non-inverting) is determined by the sign of the difference in the two voltages.

The dc output of the sampler, which is equal to the peak of the ac signal from the Oscillator, is compared to a Reference. The difference between the dc level and the Reference is amplified by the Proportional Error Amplifier, U10B, and is fed into the −Y input of the multiplier. U10B has a gain of 2. (The ALC circuit is designed to react to a change in level in less than one cycle of the input signal.)

The level error voltage from U10B is also integrated and inverted by the Error Integrator, U15, and fed into the +Y input of the multiplier. This integrator gives the ALC loop high gain for long-term level accuracy. It, however, reacts slowly to level errors. The input to the Error Integrator is applied only briefly (for 35 μs or less) each cycle by FET Q3. This provides an integration function over most of the frequency range of the Oscillator.

The overall gain of the multiplier is further controlled by the current into the IX input. This current is produced by common-base stage Q1. The current is proportional to the voltage at the output of U14. The additional control holds the gain of the ALC loop more nearly constant as a function of level. This is particularly important when large amplitude perturbations occur such as when the Oscillator range is changed.

The output of the multiplier is a current. U12A forms a transresistance amplifier which converts the differential current to a single-ended voltage. The output drives the Sum Amplifier of the Oscillator (see Service Sheet 8).

Reference

The Reference produces a temperature-stable voltage which the Proportional Error Amplifier compares with the dc voltage from Sample-and-Hold 2. The voltage is derived from voltage reference diode VR5. The voltage across R98 and R102 is the same as across VR5. The current produced in these resistors flows into R97 and produces a constant voltage. The voltage at the output of U10A is equal to the voltage across R97, R98, and R102 and is set (by adjustment of R102) to equal twice the desired peak voltage of the Oscillator.

Oscillator Restart

Monostable multivibrator U7B is normally retriggered by the signal from the Oscillator (via the Zero-Crossing Detector). If the input frequency drops below 5 Hz (corresponding to a period of 200 ms), U7B times out and switches on FET Q34 (via Q33 and Q32). This pulls the non-inverting (+) input of U10B down to approximately 2.4V minus the voltage across VR3. The abnormally low voltage at U10B creates a large error which, by the action of the ALC loop, restarts the Oscillator. (The Oscillator is assumed to be stopped if the frequency is below 5 Hz.)

TROUBLESHOOTING

General

Procedures for checking the Oscillator Assembly are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are shown on the schematic also inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements. These procedures assume that the measurement circuits of the instrument (for example, ac level and frequency) are working properly.

Equipment

Oscilloscope ..... HP 1740A

⟨✓1⟩ Oscillator Leveling Check

1. On the Audio Analyzer, key in 41.0 SPCL to initialize the instrument. Short A5TP9 (ALC) to A5TP6 (OSC 1).

2. Connect a high-impedance, dc coupled oscilloscope to A5TP2 (S/H GATE). The waveform should be a TTL square wave with a period of approximately 1 ms.

Hint: If no signal is present, check A5TP8 (OSC 2). The waveform should be a sine wave with an amplitude between 12 and 13 Vpp. If no signal is present, see Service Sheet 8 and check Oscillator tuning. If signal is present at A5TP8 but at the wrong level, continue on with the following steps.

Hint: If signal is present but at the wrong frequency, see Service Sheet 8 and check Oscillator tuning.

3. Connect the oscilloscope to pin 2 of U9. The waveform should be as shown in Figure 8C-4.

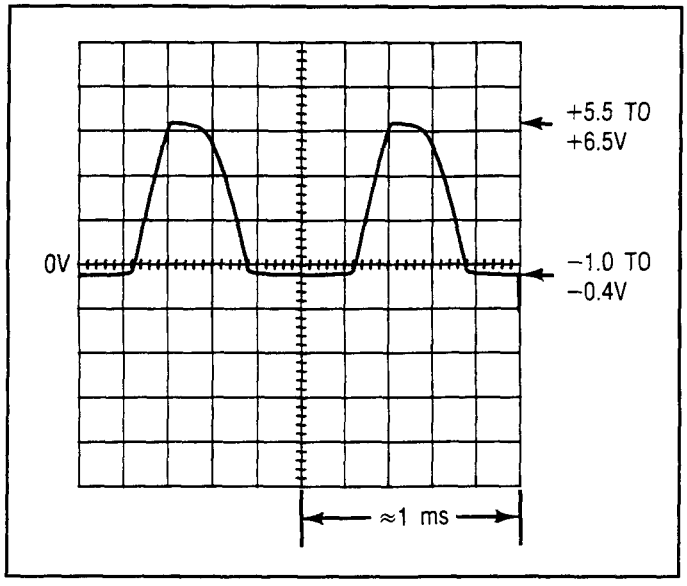


Figure 8C-4. Waveform at Pin 2 of U9, ⟨✓1⟩ Step 3

4. Connect the oscilloscope to pin 14 of U8D. The waveform should be as shown in Figure 8C-5.

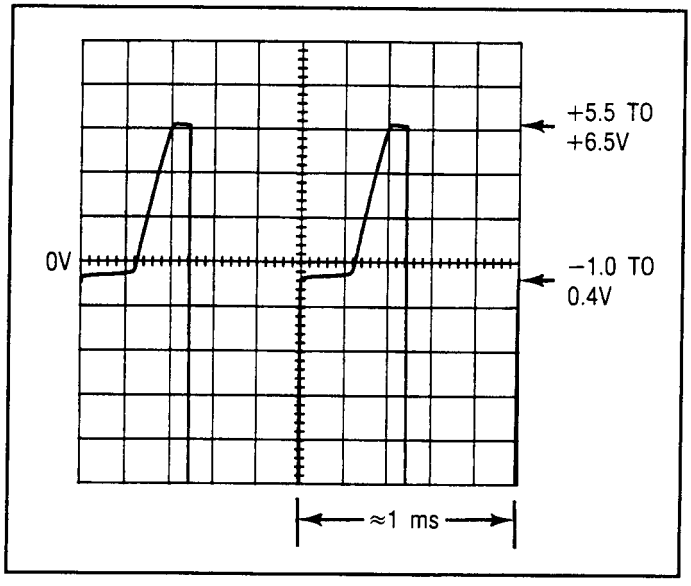


Figure 8C-5. Waveform at Pin 14 of U8D, ⟨✓1⟩ *Step 4*

5. Connect the oscilloscope to A5TP3 (S/H). The waveform should be as shown in Figure 8C-6.

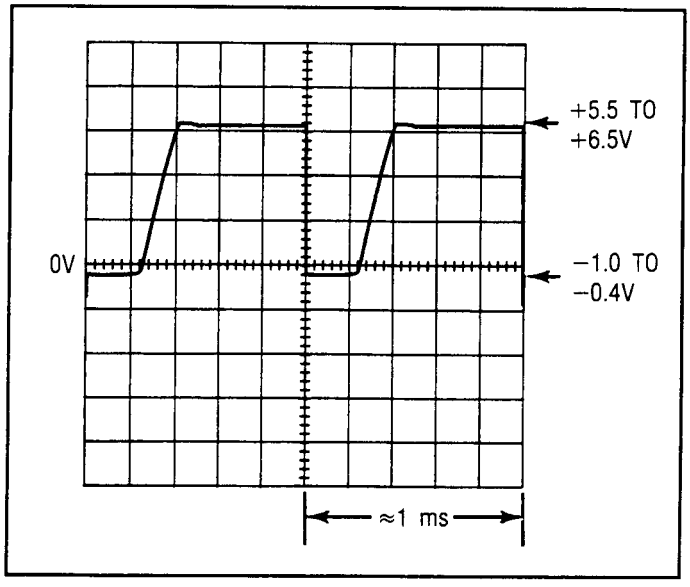


Figure 8C-6. Waveform at A5TP3, ⟨✓1⟩ *Step 5*

6. Connect the oscilloscope to pin 13 of U8C. The waveform should be as shown in Figure 8C-7.

7. Connect the oscilloscope to A5TP7 (V PEAK). The waveform should be a dc signal with a level equal to the peak level of the signal at A5TP3 (see step 5).

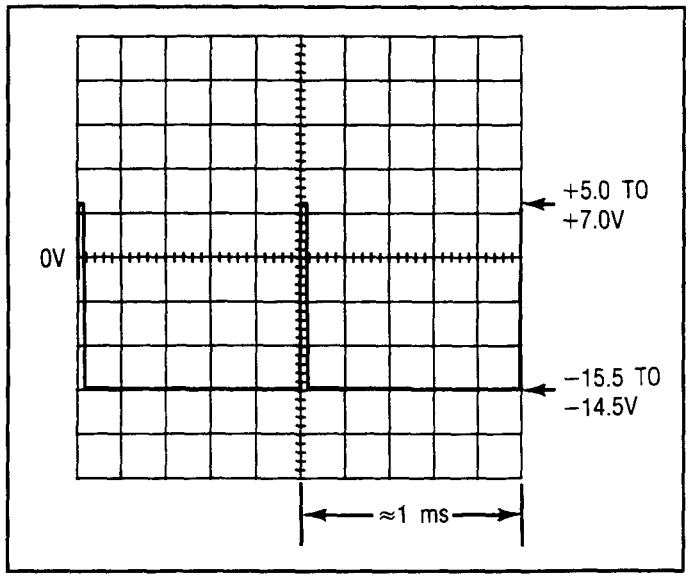


Figure 8C-7. Waveform at Pin 13 of U8C, ⟨J1⟩ Step 6

8. Connect the oscilloscope to pin 1 of U10A. The dc level should be between +7.8 and +8.2 Vdc.

Hint: If the level is only slightly out of limits, perform the *Oscillator and Output Attenuator Adjustment*, paragraph 5-15.

9. Connect the oscilloscope to A5TP5 (PROP ERROR). The dc level should be between +3.2 and +3.7 Vdc.

Hint: If the level is faulty, measure the voltage at pin 5 of U10B. It should be the same as that observed in step 8. If it is not, also check pin 5 of U7B; it should be a TTL high; Q32 and Q33 should be on; and Q34 should be off. (If Q34 is on, pin 5 of U10B will be approximately +2.3 Vdc and the output of U10B, if working properly, will be approximately −3.7 Vdc.)

10. Connect the oscilloscope to A5TP11 (INT ERROR). The waveform should be as shown in Figure 8C-8.

Hint: The waveform at pin 2 of U8B should be pulses with a 1 ms period, width approximately 35 μs, upper peak approximately +3V, and lower peak approximately −15V.

11. Connect the oscilloscope to pin 1 of U12A. The waveform should be as shown in Figure 8C-9.

Hint: The voltage at pin 2 of U6 should be approximately +10 Vdc with an ac waveform superimposed having an amplitude of 0.8 Vpp. (The shape of the waveform should be the same as shown above.) The voltage at pin 14 of U6 should be approximately +10 Vdc with an ac waveform superimposed having an amplitude of 1.7 Vpp. The output of U12A should equal 2.6 times the difference in voltage between pin 14 and pin 2 of U6. (Note that the ac waveform at pins 14 and 2 of U6 are out of phase with each other; thus the ac output of U12A is 2.6 times the sum of the peak-to-peak voltages at pin 14 and pin 2 of U6.)

Hint: The voltage drop across R119 should be 2.9 Vdc.

Hint: This step concludes a check of the function of the leveling circuits with the leveling loop open. The following steps check the closed-loop performance.

12. Remove the short between A5TP9 and A5TP6. Connect the oscilloscope to A5TP6. The waveform should be an undistorted sine wave with an amplitude between 7.8 and 8.2 Vpp.

Hint: If the steps up to 11 give positive results, but step 12 is out of limits, the problem may lie with the loop dynamics. Look for RF oscillations in the amplifiers of the loop. If distortion is excesive, check U6.

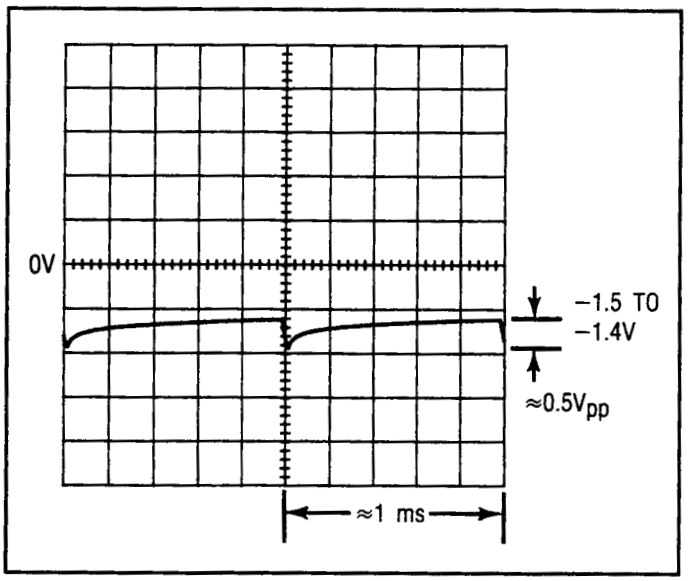


Figure 8C-8. Waveform at A5TP11, √1 Step 10

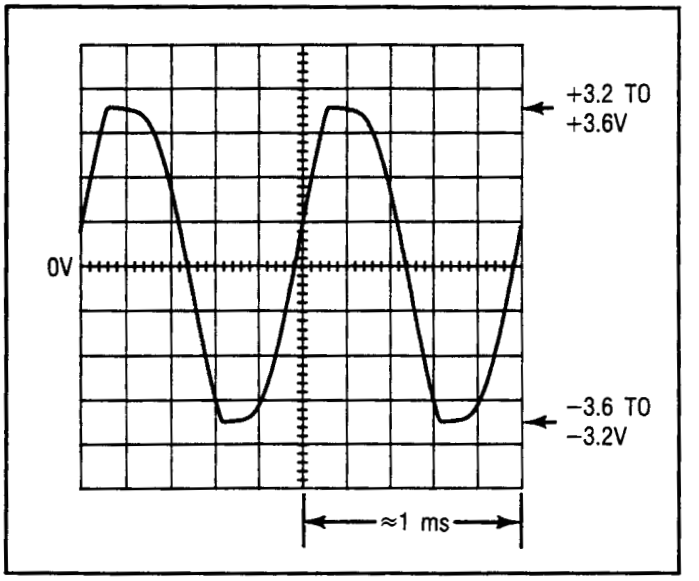


Figure 8C-9. Waveform at Pin 1 of U12A, √1 Step 11

13. Set the oscilloscope to a slow sweep rate. Short pin 3 of U10A to ground rapidly several times in succession and observe the oscilloscope. When the pin is grounded, the amplitude should drop to about 6 Vpp. When the waveform changes level (either higher or lower), the change should appear to be instantaneous and have less than 0.5V overshoot or undershoot.

SERVICE SHEET 10---A6 Output Attenuator Assembly (Input Circuits)

PRINCIPLES OF OPERATION

General

This portion of the Output Attenuator Assembly (A6) contains two programmable-gain amplifiers, a programmable attenuator, and a fixed-gain amplifier. The input to the circuits comes from the output of the Oscillator.

Amplifier 1

Amplifier 1 provides gain programmable in fine steps. U9 is configured as an inverting operation amplifier; the amplifier's maximum gain is 1. The gain is determined by the setting of DAC U13 which controls the feedback of the high-gain, differential amplifier U9. Refer to Figure 8C-10, which shows the interaction of U13 and U9 in a simplified form. The DAC is programed by lines AT AMP 0 through AT AMP 7 and AT OFF. When AT OFF is high, the gain setting is reduced an additional 6 dB. CR1 and CR2 protect U13 from static discharge. C11 frequency compensates the amplifier.

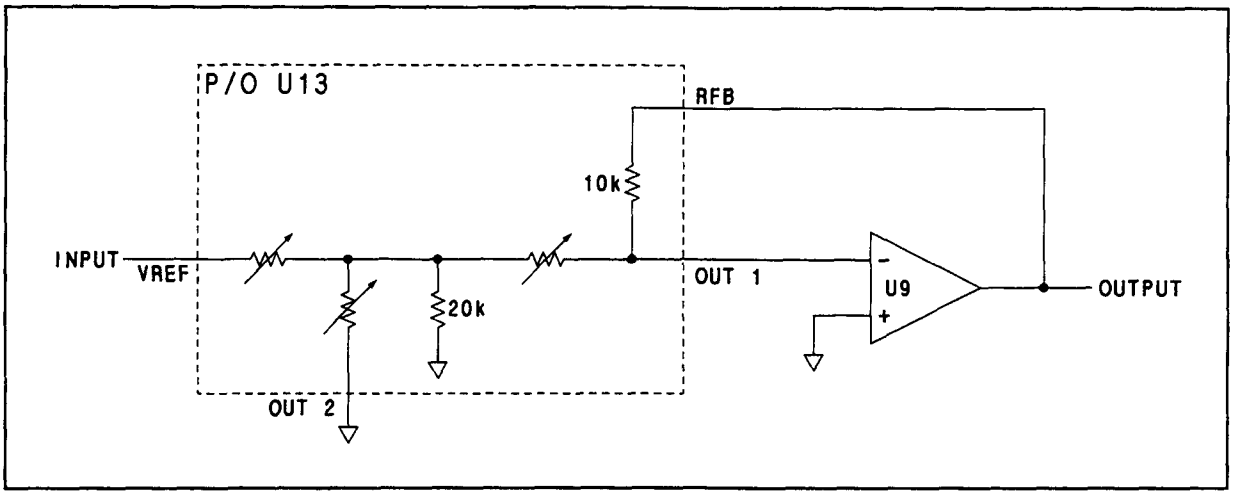


Figure 8C-10. Simplified Diagram of Amplifier 1

Amplifier 2

Amplifier 2 provides gain programmable in 2.5 dB steps from approximately −17.5 to 0 dB. Operation of Amplifier 2 is similar to Amplifier 1. The DAC (U10) is programed by lines AT AMP 8 through AT AMP 11 and AT OFF. These control lines, however, are further decoded by two ROMS (U11 and U12) to introduce a slight gain offset to compensate a quantization error in the 2.5 dB gain steps. When AT OFF is high, the gain of Amplifier 2 becomes approximately −60 dB.

Attenuator A

Attenuator A is a programmable 0, 20, and 40 dB voltage divider. It is programed by lines AT AMP 8 through AT AMP 12 and AT OFF as decoded by ROM U11 and the NAND gates of U14. When AT OFF is high, switch U15D shorts the attenuator output to ground.

Output Amplifier Driver

The amplifier formed by Q5 and U3 has a gain of 1.9. The high input impedance of the FETs of Q5 prevents loading of Attenuator A. Variable resistor (OUTPUT OFFSET ADJ) R32 adjusts the overall, dc coupled output chain for 0 Vdc offset.

TROUBLESHOOTING

General

Procedures for checking the Output Attenuator Assembly are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are shown on the schematic also inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements. These procedures assume that the measurement circuits of the instrument (for example, ac level and frequency) are working properly.

Equipment

Oscilloscope ..... HP 1740A

⟨✓1⟩ Amplifier and Attenuator Check

1. Key in 41.0 SPCL to initialize the instrument. Set the INPUT and OUTPUT switches to ground.

NOTE

In the following checks the limits of the levels measured assume a source loading of 100 kΩ (the impedance of the HIGH INPUT). Use of a high-impedance ac voltmeter may give erroneous readings.

2. Connect A5TP6 (OSC 1) to the HIGH INPUT. The amplitude should be between 2.67 and 2.95 Vrms and the frequency should be approximately 1 kHz.

Hint: If the signal is faulty, see Service Sheet 8 and check the Oscillator tuning.

3. Press RATIO. Connect A6TP6 (AMP 1) to the HIGH INPUT. Key in 59.0 SPCL and the Special Functions listed in Table 8C-14. For each setting, the amplitude ratio should be within the limits indicated. If the signal is faulty, also check the control lines indicated.

Table 8C-14. Amplitude at A6TP6, ⟨✓1⟩ Step 3

Special Function	Amplitude Ratio Limits (%)		Level (TTL) at U13 Pin								
	Minimum	Maximum	12	11	10	9	8	7	6	5	4
58.255	100.40	101.40	H	H	H	H	H	H	H	H	H
58.127	75.25	76.00	H	H	H	H	H	H	H	L	H
58.63	62.67	63.30	H	H	H	H	H	H	L	L	H
58.31	56.39	56.95	H	H	H	H	H	L	L	L	H
58.15	53.24	53.78	H	H	H	H	L	L	L	L	H
58.7	51.67	52.19	H	H	H	L	L	L	L	L	H
58.3	50.89	51.40	H	H	L	L	L	L	L	L	H
58.1	50.49	51.00	H	L	L	L	L	L	L	L	H
58.0	50.30	50.80	L	L	L	L	L	L	L	L	H

4. Key in 58.255 SPCL and 59.32 SPCL to activate the "off" state. The right display should read between 50.2 and 50.7%.

Hint: Pin 4 of U13 should be a TTL low. Pins 5 through 12 of U13 should be TTL highs.

5. Key in 59.0 SPCL. Press RATIO twice to establish a new reference. Connect A6TP5 (AMP 2) to the HIGH INPUT.

6. Key in the Special Functions listed in Table 8C-15. For each setting, the amplitude ratio should be within the limits indicated. If the signal is faulty, also check the control lines indicated.

Table 8C-15. Amplitude at A6TP5, ⟨✓1⟩ Step 6

Special Function	Amplitude Ratio Limits (%)		Level (TTL) at U12 Pin											Level (TTL) at U11 Pin			
	Minimum	Maximum	10	11	12	13	14	9	7	6	5	4	1	9	7	6	5
59.0	98.33	99.32	L	L	H	H	H	H	H	H	H	H	H	L	H	L	L
59.1	73.75	74.49	H	L	H	H	H	H	L	H	H	H	H	L	H	H	H
59.2	55.29	55.84	L	H	H	H	H	H	L	L	L	H	H	H	L	L	H
59.3	41.49	41.91	H	H	H	H	H	L	H	H	L	H	L	H	L	H	H
59.4	31.09	31.41	L	L	L	H	H	L	H	L	H	L	L	L	L	L	L
59.5	23.32	23.55	H	L	L	H	H	L	L	H	H	H	H	L	L	L	L
59.6	17.49	17.67	L	H	L	H	H	L	L	H	L	H	H	L	H	L	L
59.7	13.12	13.25	H	H	L	H	H	L	L	H	L	L	L	L	H	H	H
59.32	–	0.10	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L

7. Key in 59.0 SPCL. Press RATIO twice. Connect A6TP4 (AMP 3) to the HIGH INPUT.

8. Key in the Special Functions listed in Table 8C-16. For each setting, the amplitude ratio should be with in the limits indicated. If the signal is faulty, also check the control lines indicated.

Table 8C-16. Amplitude at A6TP4, ⟨✓1⟩ Step 8

Special Function	Amplitude Ratio Limits (%)		Level (TTL) at IC Pin							
			U14							U5
	Minimum	Maximum	13	12	10	4	11	8	6	16
59.0	188	192	H	H	H	L	L	H	H	H
59.16	18.8	19.2	L	H	H	L	H	L	H	H
59.24	1.88	1.92	L	H	L	H	H	H	L	H
59.32	–	0.01	H	L	L	L	H	H	H	L

Hint: The gain of the Output Amplifier Driver should be 1.9.

SERVICE SHEET 11---A6 Output Attenuator Assembly (Output Circuits)

PRINCIPLES OF OPERATION

General

This portion of the Output Attenuator Assembly (A6) contains the Floating Output Amplifier, Attenuator B, and Over-Voltage Protection. The output is floating (that is, not referenced to ground) unless chassis-mounted switch S2 is closed.

Floating Output Amplifier

The Floating Output Amplifier is a single-ended-to-differential converter. Conversion is accomplished by a precise combination of negative feedback, positive feedback, and cross-coupling which yields a symmetrical differential output with high common-mode rejection and a well-defined output impedance of 50Ω. The complexity of the circuit makes detailed analysis difficult. (For a more detailed discussion, see *Hewlett-Packard Journal,* August 1980, pp. 12, 13.)

Output transistors Q1 through Q4 boost the current drive capability of differential amplifiers (U1 and U2). Constant-current sources CR23 through CR26 provide bias current for diodes CR4 through CR7 and the bases of Q1 through Q4. CR4 through CR7 thermally compensate the base-emitter junctions of Q1 through Q4.

When relay K4 is open, R103 adds another 550Ω to the output impedance to the amplifier's output to bring the total impedance to 600Ω. R89 references the amplifier at ground when the output connectors are floating. Diodes CR8 through CR11 and CR19 through CR22 protect the Floating Output Amplifier from reverse-voltage transients while the over-voltage protection relays deactivate. The diodes are referenced to −12 or +12V generated by VR2 and VR1 respectively. C25 (HF BALANCE) is adjusted for optimum common-mode rejection at 100 kHz where the RFI rejection components (C29, A13C13, and A13C14) and stray circuit capacitance upset the circuit balance.

Attenuator B

Output Attenuator B is a 20 dB, pi-section pad switched by relay K1.

Over-Voltage Protection

The instantaneous voltage across the HIGH and LOW OUTPUT connectors is monitored by the Over-Voltage Detector. If the instantaneous differential voltage exceeds approximately −12 or +12V (usually due to an inadvertent application of a signal to the output), the Over-Voltage Detector causes relays K2 and K3 to open the two signal paths to prevent damage to the output circuits.

The two 12V thresholds are derived from two 0.42V references (voltage dividers R94 and R96 and R95 and R97) and two voltage dividers on the output lines (R90 through R93). The detector consists of four, wired-OR comparators (U8A, U8B, U8C, and U8D). Comparators U8D and U8C compare the HIGH and LOW outputs, respectively, against the +0.42V reference; U8A and U8B compare the HIGH and LOW outputs, respectively, against the −0.42V reference. Whenever either reference level is exceeded, the associated comparator goes low and triggers the Relay Drive One Shot (U7), which deactivates K2 and K3 by outputting a TTL high. The duration of the high output is 1s unless U7 is retriggered by the presence of the reverse voltage. Thus, a repetative overload (one with a period less than 1s) will hold the relay open until the overload is removed.

The two voltage dividers formed by R90 through R93 limit the current flow to the Over-Voltage Detector inputs for large overvoltage situations.

TROUBLESHOOTING

General

Procedures for checking the Output Attenuator Assembly are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are shown on the schematic also inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements. These procedures assume that the measurement circuits of the instrument (for example, ac level and frequency) are working properly.

Equipment

Oscilloscope ..... HP 1740A

⟨✓1⟩ Floating Output Amplifier Check

1. On the Audio Analyzer, key in 41.0 SPCL to initialize the instrument. Set the INPUT and OUTPUT switches to ground. Set IMPEDANCE to 600Ω. Key in FREQ 100 Hz. Key in 58.127 SPCL and 59.7 SPCL to preset the SOURCE amplitude. Connect the HIGH INPUT to A6TP4 (AMP 3). The left display should read approximately 100 Hz, and the right display should read between 0.525 and 0.546 Vrms.

Hint: If the signal is faulty, see Service Sheet 10 and check Amplifier 3.

2. On the Audio Analyzer, press RATIO. Connect the HIGH INPUT to A6TP3 (FLT HI). The relative amplitude display should read between 111 and 113%.

Hint: If no signal is present, check U1, U2, and Q1 through Q4. If signal is present but at the wrong level, continue with the following steps. If the signal is correct, continue on at step 10.

3. On the Audio Analyzer, ground A6TP2 (FLT LO) and A6TP3 (FLT HI). Connect the HIGH INPUT to the junction of R68 and R69. The relative amplitude should read between 57.2 and 57.8%.

Hint: If the signal is faulty, check R48 and R61. (The amplifier gain is the ratio R61/R48 expressed in %.)

4. Connect the HIGH INPUT to pin 3 of U1. The right display should read between 35.6 and 36.0%.

Hint: If the signal is faulty, check R47, R55, and R56. (The amplifier gain is the ratio R/(R+R72) expressed in %, where R is the parallel combination of R55, R56, and the 100 kΩ input resistance.)

5. Connect the HIGH INPUT to the junction of R66 and R67. The relative amplitude should read between 56.3 and 57.5%.

Hint: If the signal is faulty, check R46 and R64. (The amplifier gain is the ratio of step 4, excluding the loading of the 100 kΩ input resistance, times 1+R54/R46 expressed in %.)

6. Remove the ground from A6TP3. Place a short across R70. Connect the HIGH INPUT to A6TP3. On the Audio Analyzer, press RATIO twice to establish a new reference.

7. Connect the HIGH INPUT to pin 3 of U2. The right display should read between 31.4 and 31.8%.

Hint: If the signal if faulty, check R49, R57, and R58. (The amplifier gain is R/(R+R57) expressed in %, where R is the parallel combination of R49, R58, and the 100 kΩ input resistance.)

8. Remove the short from R70. Connect the HIGH INPUT to A6TP4. On the Audio Analyzer, press RATIO twice to establish a new reference.

9. Connect the HIGH INPUT to the HIGH OUTPUT. The right display should read between 111 and 113%.

Hint: If the signal is faulty, check R70 and any component in series or parallel with the path from A6TP3 to the HIGH OUTPUT connector, such as K1, K2, K3, R103, etc.

10. On the Audio Analyzer, set the LOW OUTPUT to FLOAT. Remove the ground from A6TP2. Ground A6TP3. Connect the HIGH INPUT to the LOW OUTPUT. The right display should read between 106 and 108%.

Hint: If the signal is faulty, check R71, R89, K2, and K3.

⟨J2⟩ Attenuator B Check

1. Key in 41.0 SPCL to initialize the instrument. Set the INPUT and OUTPUT switches to ground. Key in 58.255 SPCL and 59.0 SPCL to preset the source amplitude to 6V. Set IMPEDANCE to 600Ω. Connect the HIGH INPUT to A6TP3 (FLT HI). The left display should read approximately 1000 Hz, and the right display should read between 5.9 and 6.1 Vrms.

Hint: If the signal is faulty, see ⟨J1⟩ *Floating Output Amplifier Check.*

2. Press RATIO. Connect the HIGH INPUT to the HIGH OUTPUT. The right display should read between 99.3 and 99.5%.

Hint: Relay K1 should be in the through-path position. Pins 1, 2, and 3 of U4 should be TTL high.

Hint: The two pairs of contacts of K2 and K3 should be closed.

Hint: If the reading is 100%, check K4.

3. Press RATIO twice to establish a new reference. Key in 59.8 SPCL to switch in Attenuator B. The right display should read between 9.95 and 10.05%.

Hint: Pin 1 of U4 should be a TTL high; pins 2 and 3 of U4 should be a TTL low.

⟨J3⟩ Over-Voltage Detector Check

1. On the Audio Analyzer, key in 41.0 SPCL to initialize the instrument. Key in AMPTD 1 V. Set the OUTPUT switch to ground. Set IMPEDANCE to 600Ω.

2. Connect a high-impedance, dc coupled oscilloscope through a tee to the HIGH OUTPUT. Connect a BNC-to-cliplead adapter to the tee. Set the oscilloscope to 5V per division and adjust the oscilloscope to observe the 1 kHz, 1 Vrms sine wave.

Hint: If the signal is faulty, see ⟨J1⟩ *Floating Output Amplifier Check.*

3. Momentarily touch the center-conductor cliplead (but not the ground lead) to the +15V power supply on the A6 assembly. (The + end of C1 is a convenient place to touch the clip lead.) The signal observed on the oscilloscope should jump to +15V with no ac present, then return to normal after about 1s.

4. Momentarily touch the clip lead to the −15V power supply. (The − end of C3 is a convenient place to touch the cliplead.) The signal should jump to −15V with no ac present, then return to normal after about 1s.

5. On the Audio Analyzer, set the LOW OUTPUT switch to FLOAT. Connect the oscilloscope to the LOW OUTPUT. Short the HIGH OUTPUT to ground. (A 50Ω load can also be used for this.) Repeat steps 3 and 4. The results should be the same.

⟨J4⟩ Impedance Switch Check

1. On the Audio Analyzer, key in 41.0 SPCL to initialize the instrument. Key in AMPTD 1 V. Set the INPUT and OUTPUT switches to ground. Set IMPEDANCE to 600Ω. Connect the HIGH INPUT to A6TP3 (FLT HI). The left display should read approximately 1 kHz, and the right display should read approximately 1 Vrms.

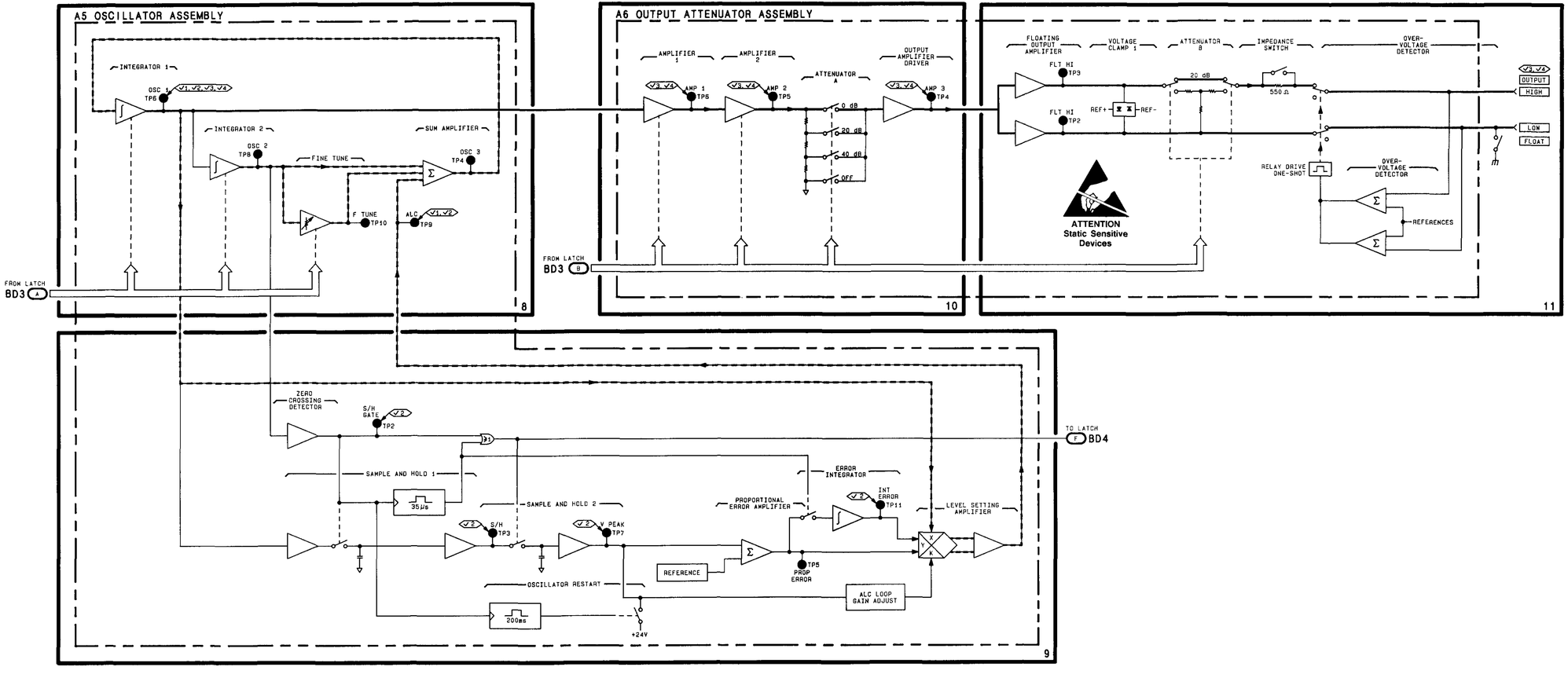
Hint: If the signal is faulty, see ⟨J1⟩ *Floating Output Amplifier Check.*

2. Press RATIO. Short the HIGH OUTPUT to ground. The right display should read between 90.6 and 92.6%.

Hint: If the signal is faulty, check K4. A6TP7 (50/600Ω) should be a TTL high.

3. Set IMPEDANCE to 50Ω. The right display should read less than 1%.

Hint: If the signal is faulty, check K4. A6TP7 (50/600Ω) should be a TTL low.



BD3
Figure 8C-101
8C-101

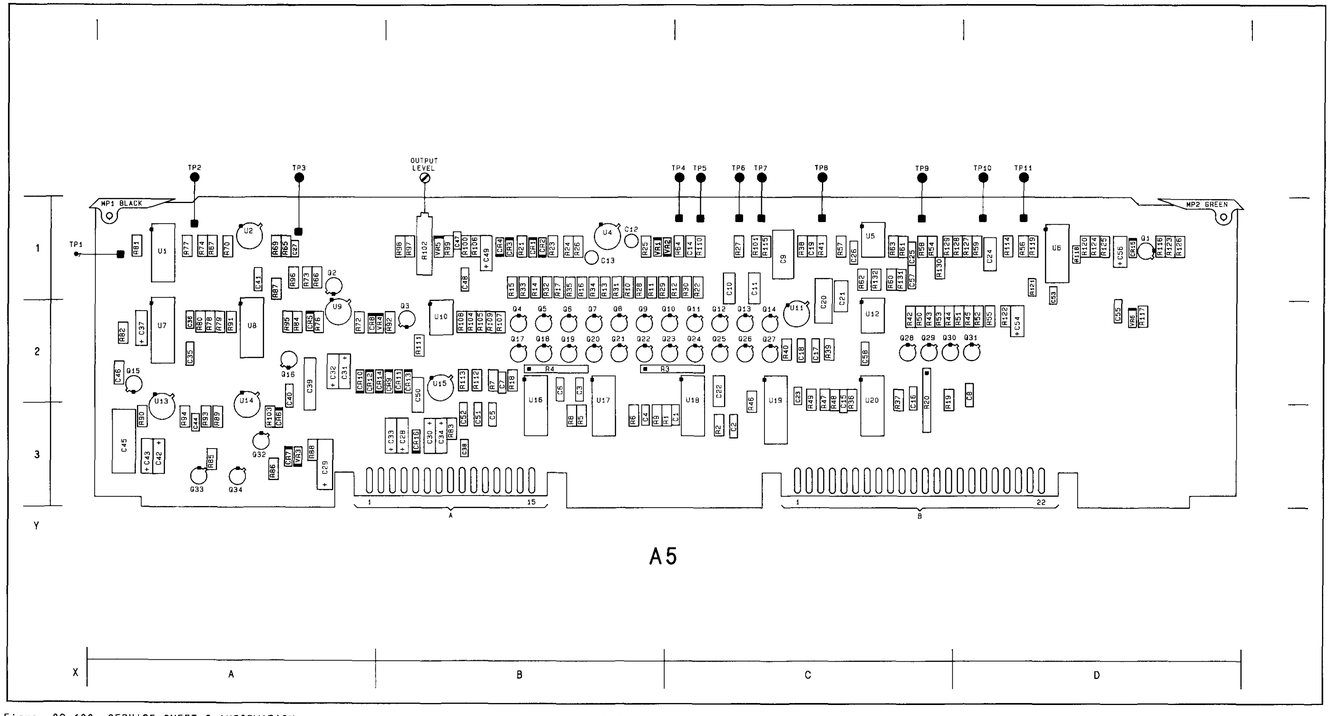


Figure 8C-102. SERVICE SHEET 8 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y
C1	C3
C2	C3
C3	B2
C4	B3
C5	B3
C6	B2
C7	B2
C8	D2
C9	C1
C10	C1
C11	C1
C12	B1
C13	B1
C14	C1
C15	C2
C16	D2
C17	D2
C18	D2
C19	C1
C20	C1
C21	C1
C22	C2
C23	C2
C24	D1
C25	C1
C26	C1
CR1	B1
CR2	B1
CR3	B1
CR4	B1
CR16	B3
Q4	B2
Q5	B2
Q6	B2
Q7	B2
Q8	B2
Q9	B2
Q10	B2
Q11	C2
Q12	C2
Q13	C2
Q14	C2
Q17	B2
Q18	B2
Q19	B2
Q20	B3
Q21	B2
Q22	B2
Q23	B2
Q24	C2
Q25	C2
Q26	C2
Q27	C2
Q28	C2
Q29	C2
Q30	C2
Q31	D2
R1	B3
R2	C3
R3	B2
R4	B2
R5	B3
R6	B3
R7	B2
R8	B3
R9	B3
R10	B1
R11	B1
R12	C1
R13	B1
R14	B1
R15	B1
R16	B1
R17	B1
R18	B2
R19	C2
R20	C2
R21	B1
R22	C1
R23	B1
R24	B1
R25	B1
R26	B1
R27	C1
R28	B1
R29	B1
R30	C1
R31	B1
R32	B1
R33	B1
R34	B1
R35	B1
R36	C2
R37	C2
R38	C1
R39	C2
R40	C2
R41	C1
R42	C2
R43	C2
R44	C2
R45	B2
R46	C2
R47	C2
R48	C2
R49	C2
R50	C2
R51	C2
R52	D2
R53	C2
R54	C1
R55	D2
R56	D1
R57	C1
R58	C1
R59	D1
R60	C1
R61	C1
R62	C1
R63	C1
R64	C1
TP1	C1
TP6	C1
TP8	C1
TP9	C1
TP10	D1
U4	B1
U5	C1
U11	C2
U12	C2
U16	B2
U17	B2
U18	C2
U19	C2
U20	C2
VR1	B1
VR2	B1

Source Circuits Block Diagram **BD3**

SEE REVERSE SIDE

NOTES

1. Decouple probe with 10k ohm resister when measuring this voltage.
2. Ground TP9 to stop oscillator when measuring this voltage.
3. Measure with 57.255 SPCL.

A5Q4-14 TOP VIEW

A5U4,5,11,12 TOP VIEW

A5R3,4,20 TOP VIEW

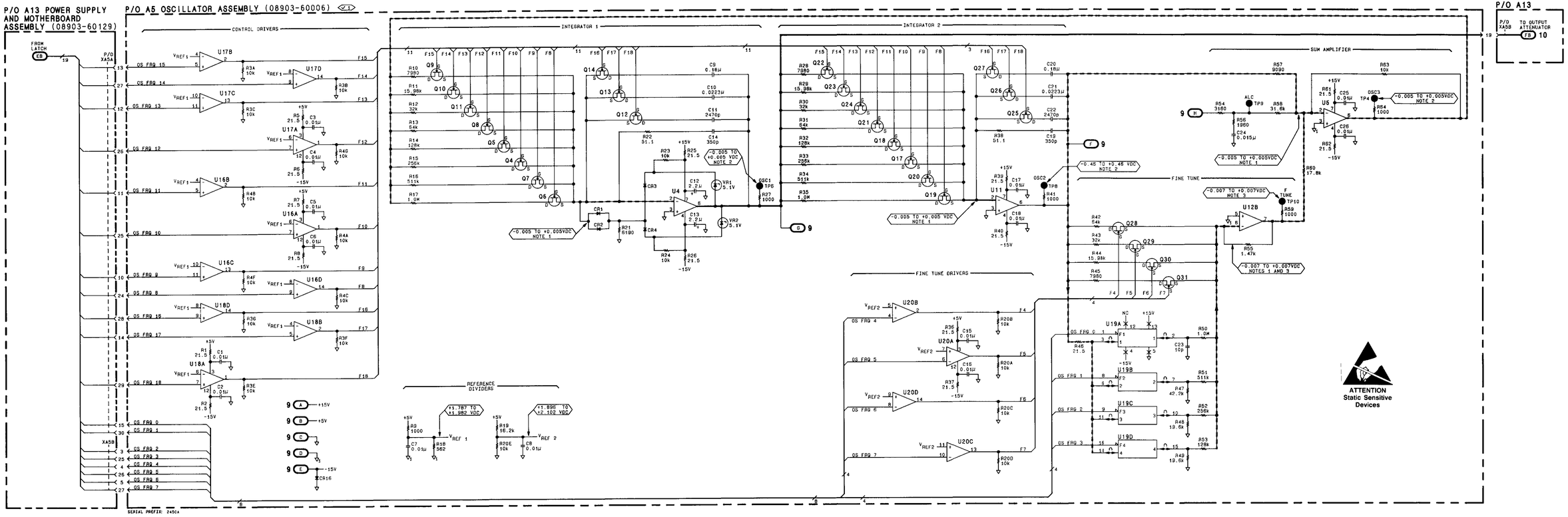
PIN NO.

COMMON	1	GND
A	2	
B	3	
C	4	
D	5	
E	6	
F	7	
G	8	

Schematic General Information

CHANGES

2717A to 2742A	**On the A13 schematic:** • **08903-60192** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60192.
2723A and above	**On the A5 schematic:** • **C59, C60** - Under INTEGRATOR 1, add pin 8 (compensation) between pins 4 and 6 of U4. To pin 8, add C59, 1.5pF to ground. Under INTEGRATOR 2, add pin 8 (compensation) between pins 4 and 6 of U11. To pin 8 add C60 1.5pF to ground. **On the A5 Component Locator:** • **C59, C60** - Add C59 to the backside of the board between pins 3 and 8 of U4. Add C60 to the backside of the board between pins 3 and 8 of U11. **On the A5 Component Coordinates:** • **C59, C60** - Add C59 B,1 and C60 C,2 to the coordinates table.
2813A and above	**On the A13 schematic:** • **08903-60292** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60292.



SS8
Figure 8C-103
8C-103

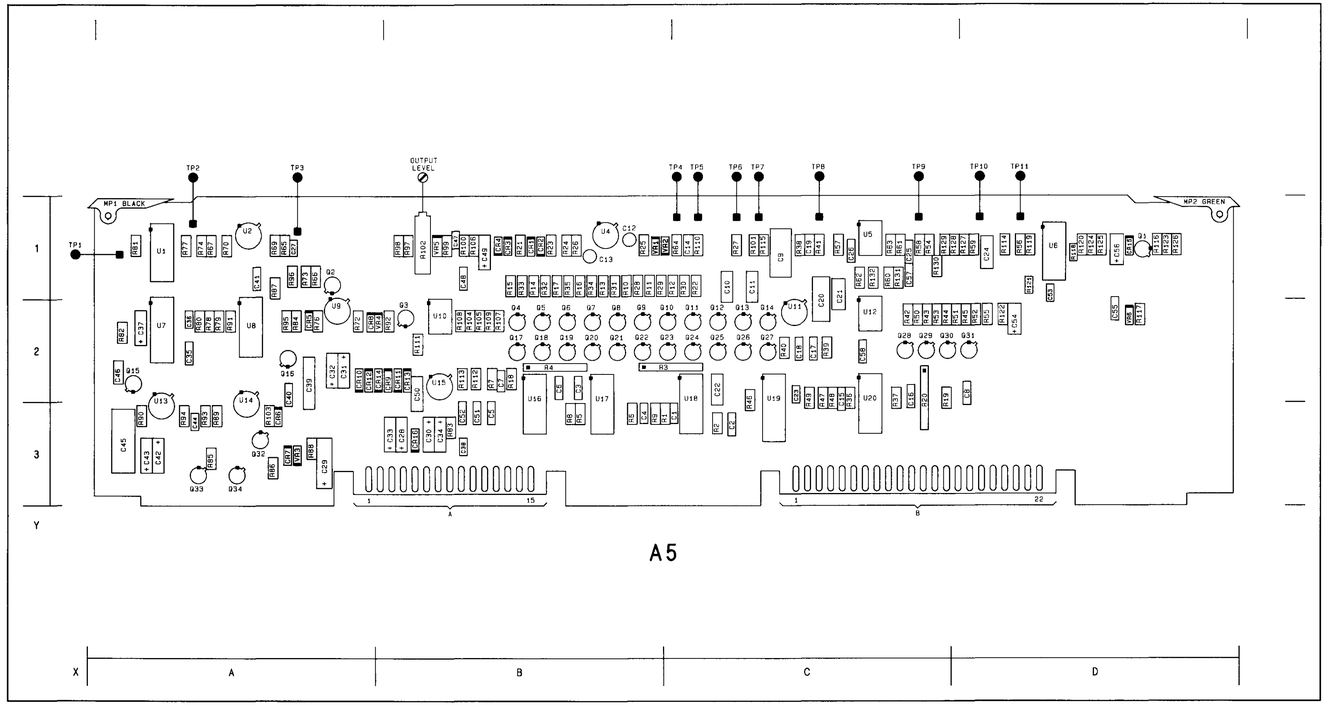


Figure 8C-104. SERVICE SHEET 9 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C27	A1	R102	B1				
C28	B3	R103	A3				
C29	A3	R104	B2				
C30	B3	R105	B2				
C31	A2	R106	B1				
C32	A2	R107	B2				
C33	B3	R108	B2				
C34	B3	R109	B2				
C35	A2	R110	C1				
C36	A2	R111	B2				
C37	A2	R112	B2				
C38	B3	R113	B2				
C39	A2	R114	D1				
C40	A2	R115	C1				
C41	A1	R116	D1				
C42	A3	R117	D2				
C43	A3	R118	D1				
C44	A3	R119	D1				
C45	A3	R120	D1				
C46	A2	R121	D1				
C47	B1	R122	D2				
C48	B1	R123	D1				
C49	B1	R124	D1				
C50	B2	R125	D1				
C51	B3	R126	D1				
C52	B3	R127	D1				
C53	D1	R128	C1				
C54	D2	R129	C1				
C55	D2	R130	C1				
C56	D1	R131	C1				
C57	C1	R132	C1				
C58	C2						
		TP1	A1				
CR5	A2	TP2	A1				
CR6	A3	TP3	A1				
CR7	A3	TP5	C1				
CR8	A2	TP7	C1				
CR9	B2	TP11	D1				
CR10	A2						
CR11	B2	U1	A1				
CR12	A2	U2	A1				
CR13	B2	U6	D1				
CR14	A2	U7	A2				
CR15	D1	U8	A2				
		U9	A2				
Q1	D1	U10	B2				
Q2	A1	U12	C2				
Q3	B2	U13	A2				
Q15	A2	U14	A2				
Q16	A2	U15	B2				
Q30	A3						
Q33	A3	VR3	A3				
Q34	A3	VR4	A2				
		VR5	B1				
R65	A1	VR6	D2				
R66	A1						
R67	A1						
R68	A1						
R70	A1						
R72	A2						
R73	A1						
R74	A1						
R76	A2						
R77	A1						
R78	A2						
R79	A2						
R80	A2						
R81	A1						
R82	A2						
R83	B3						
R84	A2						
R85	A3						
R86	A3						
R87	A1						
R88	A3						
R89	A3						
R90	A3						
R91	A2						
R92	B2						
R93	A3						
R94	A3						
R95	A2						
R96	A1						
R97	B1						
R98	B1						
R99	B1						
R100	B1						
R101	C1						

P/O A5 — Oscillator-State-Variable Circuits — SS8

SEE REVERSE SIDE

NOTES

1. Decouple probe with 10k ohm resister when measuring this voltage.
2. Ground TP9 to stop oscillator when measuring this voltage.

A5Q3,15, 16,34 TOP VIEW

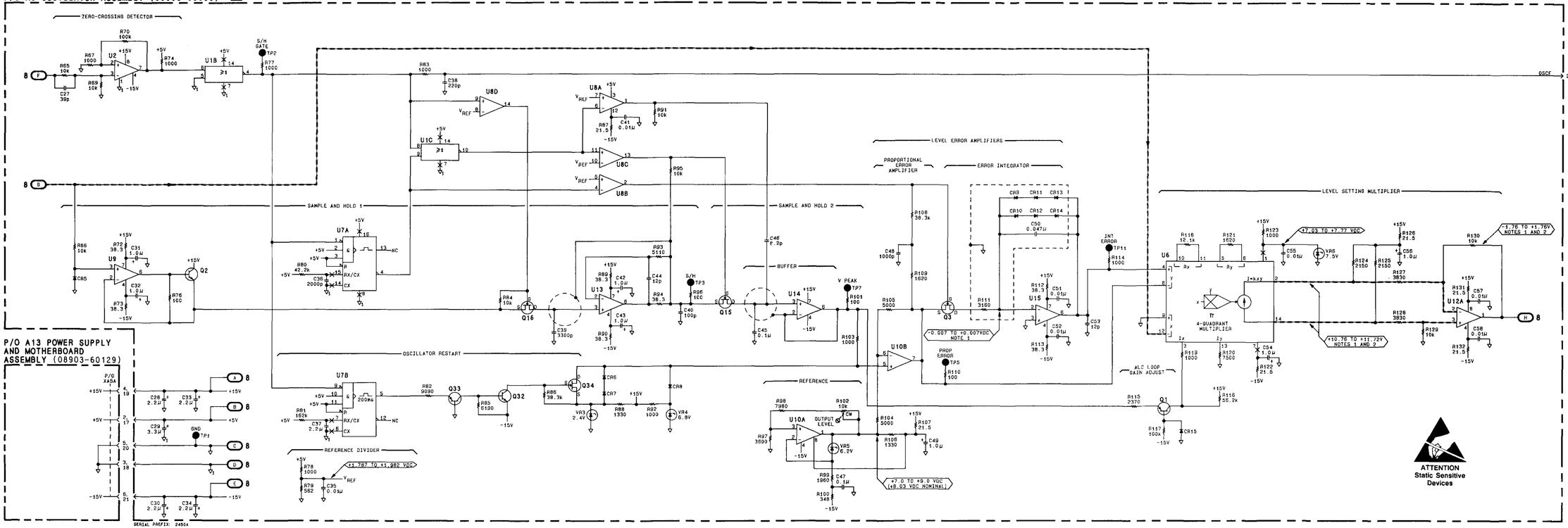
A5U2,3,9,10, 12-15 TOP VIEW

Schematic General Information

CHANGES

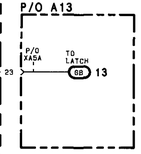
2717A to 2742A	**On the A13 schematic:** • **08903-60192** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60192.
2813A and above	**On the A13 schematic:** • **08903-60292** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60292.

P/O A5 OSCILLATOR ASSEMBLY (08903-60006) ⚠1



P/O A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY (08903-60129)

P/O A13



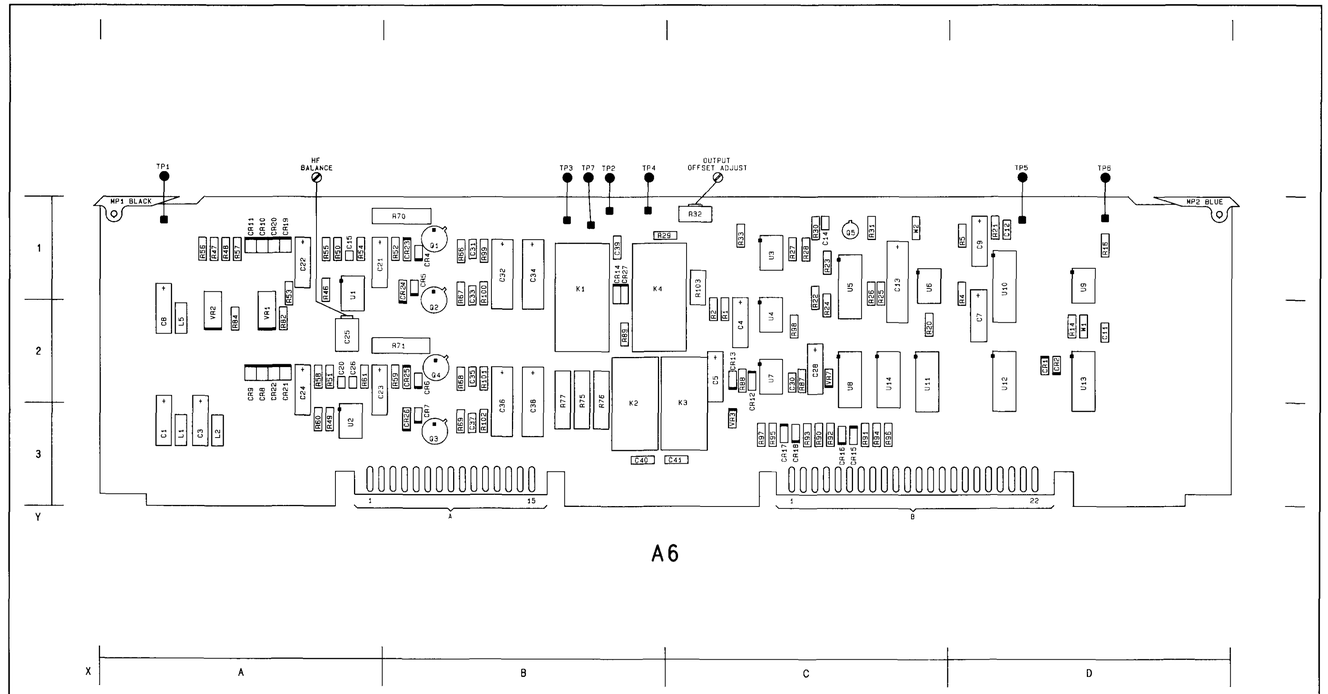


Figure 8C-106. SERVICE SHEET 10 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	A3						
C3	A3						
C4	C2						
C5	C2						
C7	D2						
C8	A2						
C9	D1						
C11	D2						
C12	D1						
C13	C1						
C14	C1						
CR1	D2						
CR2	D2						
L1	A3						
L2	A3						
L5	A2						
Q5	C1						
R1	C2						
R2	C2						
R4	D1						
R5	D1						
R14	D1						
R16	D1						
R20	C2						
R21	D1						
R22	C1						
R23	C1						
R24	C2						
R25	C1						
R26	C1						
R27	C1						
R28	C1						
R29	B1						
R30	C1						
R31	C1						
R32	C1						
R33	C1						
TP4	B1						
TP5	D1						
TP6	D1						
U3	C1						
U5	C1						
U6	C1						
U9	B1						
U10	D1						
U11	C2						
U12	D2						
U13	D2						
U14	C2						
W1	D2						
W2	C1						

P/O A5 Oscillator-ALC Circuits **SS9**

SEE REVERSE SIDE

NOTES

1. ↓V2 indicates a second analog ground trace used for certain capacitors on the floating output amplifier located on service sheet 11.

Q5 TOP VIEW

LOGIC LEVELS

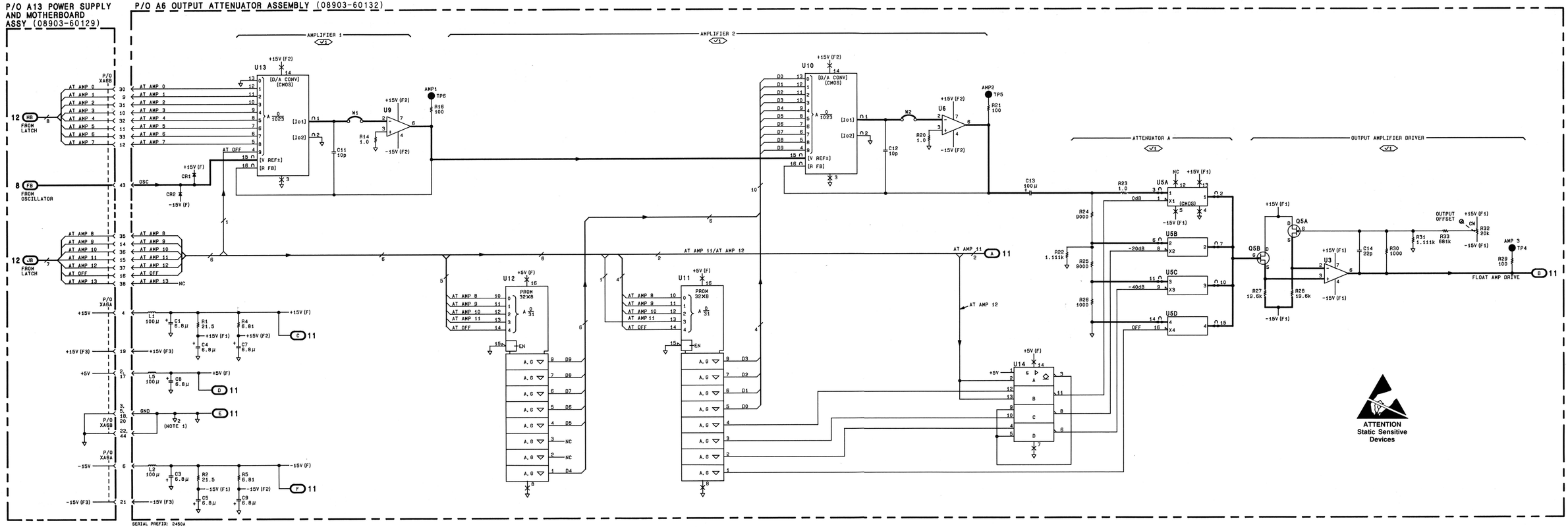
	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN	
> IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

K1 AND K4 BOTTOM VIEW

Schematic General Information

CHANGES

2717A to 2742A	**On the A13 schematic:** • **08903-60192** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60192.
2813A and above	**On the A13 schematic:** • **08903-60292** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60292.



SS10
Figure 8C-107
8C-107

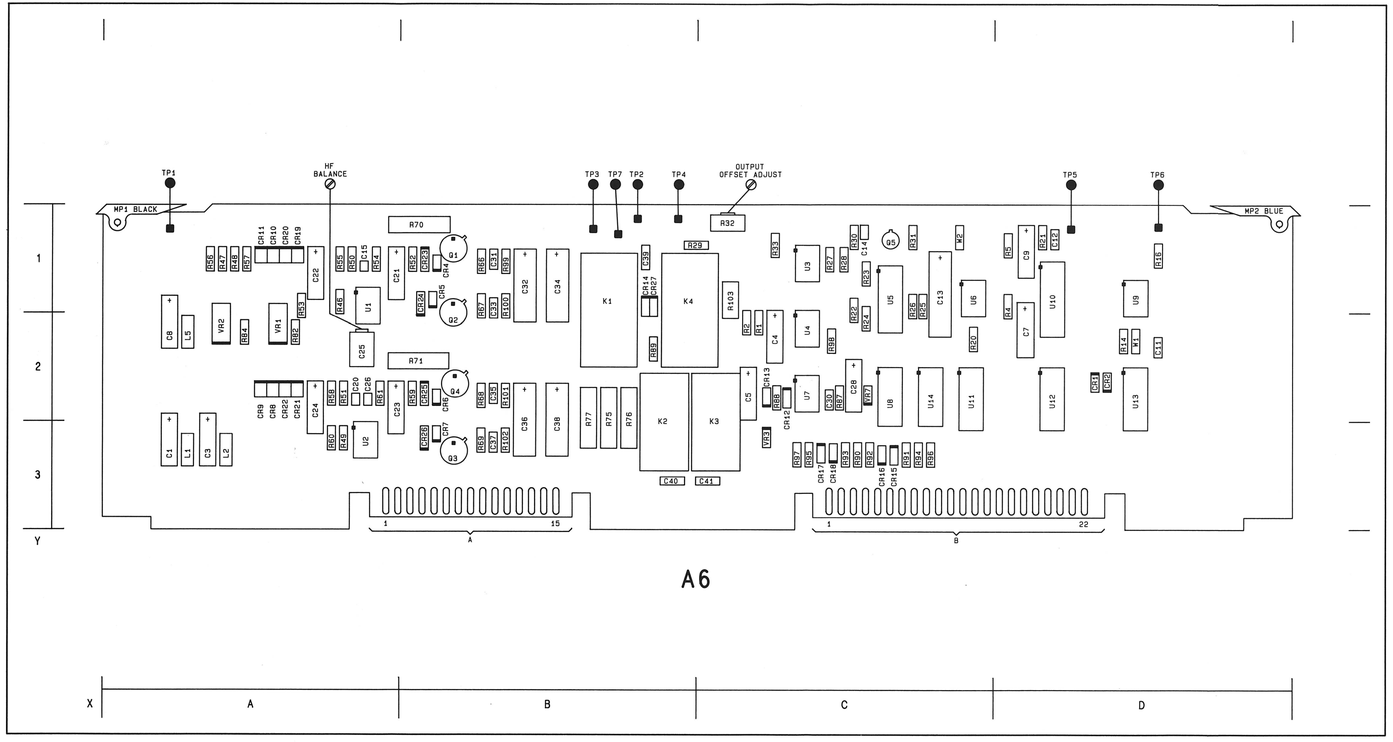


Figure 8C-108. SERVICE SHEET 11 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C15	A1	R91	C3				
C20	A2	R92	C3				
C21	A1	R93	C3				
C22	A1	R94	C3				
C23	A2	R95	C3				
C24	A2	R96	C3				
C25	A2	R97	C3				
C26	A2	R98	C2				
C28	C2	R99	B1				
C30	C2	R100	B1				
C31	B1	R101	B2				
C32	B1	R102	B3				
C33	B1	R103	C1				
C34	B1						
C35	B2	TP1	A1				
C36	B3	TP2	B1				
C37	B3	TP3	B1				
C38	B3	TP7	B1				
C39	B1						
C40	B3	U1	A1				
C41	C3	U2	A3				
		U4	C2				
CR4	B1	U7	C2				
CR5	B1	U8	C2				
CR6	B2						
CR7	B3	VR1	A2				
CR8	A2	VR2	A2				
CR9	A2	VR3	C3				
CR10	A1	VR7	C2				
CR11	A1						
CR12	C2						
CR13	C2						
CR14	B1						
CR15	C3						
CR16	C3						
CR17	C3						
CR18	C3						
CR19	A1						
CR20	A1						
CR21	A2						
CR22	A2						
CR23	B1						
CR24	B1						
CR25	B2						
CR26	B3						
CR27	B1						
K1	B1						
K2	B2						
K3	C3						
K4	B1						
Q1	B1						
Q2	B1						
Q3	B3						
Q4	B2						
R46	A1						
R47	A1						
R48	A1						
R49	A3						
R50	A1						
R51	A2						
R52	B1						
R53	A1						
R54	A1						
R55	A1						
R56	A1						
R57	A1						
R58	A2						
R59	B2						
R60	A3						
R61	A2						
R66	B1						
R67	B1						
R68	B2						
R69	B3						
R70	B1						
R71	B2						
R75	B3						
R76	B3						
R77	B3						
R82	A2						
R84	A2						
R87	C2						
R88	C2						
R89	B2						
R90	C3						

P/O A6 Output Attenuator-Input Circuits **SS10**

SEE REVERSE SIDE

NOTES

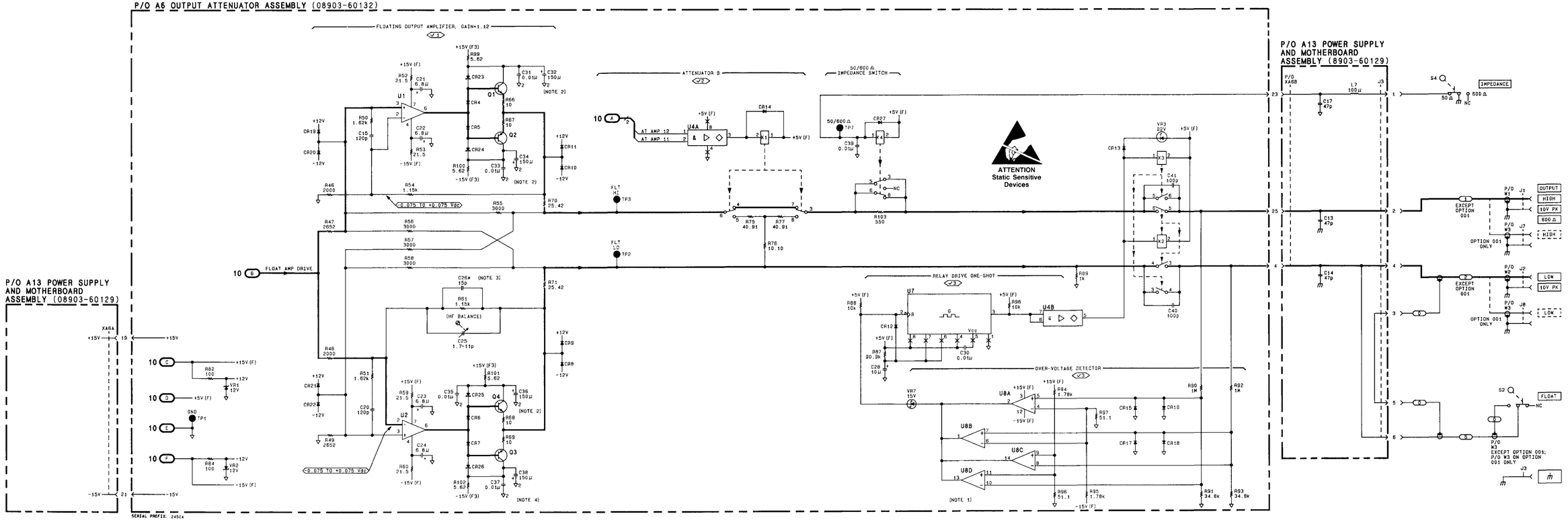
1. Comparator A6U8 has open collector.
2. ∇_2 indicates a second analog ground trace used for these capacitors on the floating output amplifier for improved current isolation. This second ground trace connects into common ground on the mother-board.
3. * Asterisk indicates factory selected values.

K2,3
BOTTOM VIEW

Schematic General Information

CHANGES

2717A to 2742A	**On the A13 schematic:** • **08903-60192** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60192.
2742A and above	**On the A6 schematic:** • **P/O A13** - In the upper right portion of the schematic delete the circuitry for the impedance switch.
2813A and above	**On the A13 schematic:** • **08903-60292** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60292.
2818A and above	**On the A6 schematic:** • **R91, R93, R94, R95** - In the lower right hand corner of the schematic under OVER-VOLTAGE DETECTOR, change the values of R91 and R93 to 21.5K ohms, and change the component values of R94 and R95 to 2.61K ohms.



SS11
Figure 8C-109
8C-109

CHANGES

2742A and above On the schematic:

- P/O A13 - In the upper right portion of the schematic delete the circuitry for the impedance switch.

SERVICE SHEET BD4---Digital Circuits Block Diagram

PRINCIPLES OF OPERATION

General

Service Sheet BD4 covers the Counter, Keyboard and Display, Latches, Controller, and Remote Interface; that is, it covers most of the digital circuits of the instrument.

Counter (P/O A8)

The Counter consists of the input switching, Clock Counter, Cycle Counter, and counter control circuits. The Counter is used in two modes: (1) to measure frequency (from either the input circuits, the output circuits, or the Oscillator) or (2) to measure the duration of the dc voltmeter Stop Count pulse. The Clock and Cycle Counters are both utilized for the frequency measurement; however, only the Clock Counter is used for the voltage measurement. The Cycle Counter counts the number of cycles of the input frequency (FMUX) and has two stages, giving a total division ratio of 32. The Clock Counter counts the 2 MHz Clock Out (Φ) signal, which originates at the Crystal Oscillator of the CPU. The Clock Counter has three stages, giving a total division ratio of 2048.

To select the frequency-count mode, the Voltmeter Gate switch is opened and the Clock Counter Gate set to route the path from the Frequency Gate into the Clock Counter. The Controller then clears (resets) the counters and at the same time arms the Mode Select. At the beginning of the next Cycle of the input signal (FMUX), the Mode Select closes both the Frequency Gate and Cycle Counter Gate switches. After a short period, carries are generated at the outputs of both the Clock and Cycle Counters. The Controller counts the carries via the Carry Gating circuit which is now enabled. When a predetermined number of carries from the Clock Counter has been counted, the Controller disarms the Mode Select. At the beginning of the next cycle of the input signal, the Mode Select opens both the Frequency Gate and Cycle Counter Gates switches. This guarantees that at least one cycle of the input signal is counted.

The Count Transfer Logic then transfers the count of the individual stages of both counters in parallel to the Controller via the Counter Output Gating. First, the output from Stage 1 of the Cycle Counter is transferred. Then the output from Stage 2 of the Cycle Counter and Stage 3 of the Clock Counter is loaded into Stage 1 of the Cycle Counter and the output is again transferred. This process is again repeated with Stage 2 of the Clock Counter loading into Stage 1 of the Cycle Counter via Stage 3 of the Clock Counter and Stage 2 of the Cycle Counter and transferring. Finally, Stage 1 of the Clock Counter is loaded into Stage 1 of the Cycle Counter via the intermediate stages and transferred.

To make a voltage measurement, the Controller first sets the Clock Counter Gate to receive the signal from the Voltmeter Gate. The Stop Count Gate was closed after completing the previous measurement. The Controller then arms the Voltmeter Gate and initiates the ramp in the Voltage-to-Time Converter (via the Ramp Gate line). The first pulse on the Clock Out (Φ) line closes the Voltmeter Gate. The Clock Counter now begins counting the 2 MHz clock pulses. After an interval determined by the dc level being measured, the Voltage-to-Time Converter generates a Stop Count pulse which opens the Stop Count Gate. The Count accumulated in the Clock Counter is thus proportional to the input voltage. (Note that the Cycle Counter is not used in this measurement.) The count is transferred to the Controller in the same manner as for a frequency measurement.

Controller (P/O A8)

The Controller consists of a Microprocessor, Read-Only Memory (ROM), Random-Access Memory (RAM), a Memory Select Decoder, and input/output interface circuitry. The Microprocessor is divided into two devices: the Central Processing Unit (CPU) and a Static Memory Interface (SMI). A third device, a Peripheral Input/Output (PIO on A9), is also included when the Microprocessor interfaces with the Remote Interface Assembly.

The Controller's program is stored in ROM. To retrieve information from ROM, the SMI, under control of the CPU, outputs the appropriate address on the Address Bus. Four of the sixteen address bits are decoded by the Memory Select Decoder to enable one of the ROM devices. Eleven address bits address the individual ROMs. The enabled ROM then outputs eight bits of data onto the Data Bus from the location corresponding

to the input address. Information in ROM may be either a program instruction or data. In a similar manner temporary information is written to or read from the RAM. The RAM, however, is addressed by only eight of the eleven address bits, and inputs or outputs only four data bits. The RAM is enabled by Address 15 (A15). **Serial Prefix 2652A and Above**: Fifteen address bits are used to address the ROM. The enabled ROM then outputs eight bits of data onto the Data Bus from the location corresponding to the input address.

The CPU interprets bytes from the ROM as data or instructions depending on the context of the program. If the byte is an instruction, the outcome depends on the nature of the instruction. A simple instruction (such as add or shift) is executed immediately and the instruction in the next address fetched. More complex instructions fetch additional data or instructions from following addresses and, in the case of jumps and subroutine calls, cause program execution to move to another location in memory.

When a front-panel key is pressed, an interrupt is generated. The interrupt causes program execution to jump to a specified address location where the interrupt service subroutine is located. The subroutine interrogates the Keyboard to determine which key was pressed and then takes the appropriate action. HP-IB codes and commands interrupt the Microprocessor in a similar way.

The CPU communicates with the SMI and PIO through the ROM Control (ROMC) lines and the Data bus. The CPU does data manipulation (arithmetic and logic computations) and contains the clocking and control circuitry. The 2 MHz clock comes from the Crystal Oscillator and is also used as the Counter time-base reference. The SMI interfaces with the ROMs and RAM.

The CPU also contains bidirectional input/output (I/O) ports for communicating with the instrument hardware. This is done via the Instrument Bus discussed in the next paragraph. Four of the Instrument I/O bits, however, are reserved for servicing the Controller. Four LEDs, driven from the port, indicate errors encountered during power-up verification tests, measurement cycles, and Keyboard and HP-IB interrupts. Four test points on the port can be used to initiate troubleshooting routines which use signature analysis. Refer to *Controller LEDs and Test Points,* paragraph 8-28.

Latches (A7) and Instrument Bus

Figure 8D-1 shows a typical hookup on the Instrument Bus. The Instrument Bus lines are broken into three groups: enable (e), select (s), and data (d). The enable code (e0 to e3) comes from I/O lines 10 through 13 of the CPU (A8U5). Three of the lines are decoded by the Enable Code Decoder (A8U22) to activate one of eight unique enable lines (e=0 to e=7). The fourth line enables the decoder itself. The enable lines run to the Keyboard, Remote Interface, and Latch Assemblies and to the Counter on the Controller/Counter Assembly. Typically, each line is dedicated to a specific operational function; for example, enable line e=6 controls Oscillator tuning.

The select (s0 to s3) and data codes (d0 to d3) come from I/O lines 00 to 07. The eight lines also run to the Keyboard, Remote Interface, and Latch Assemblies and to the Counter where they are decoded. The Latch Assembly decodes the Instrument Bus for all of the measurement and source assemblies. Up to 16 data codes for each of the 16 select codes are possible for each active enable line. The select code typically selects a functional category and the data code selects the specific function or configuration. For a given function, the select codes are decoded only while the corresponding enable line is active. The data codes are decoded and latched only when triggered by the decoded select line. The latched data drive the digital-to-analog devices which control the instrument hardware.

On the schematic diagrams, the lines leaving the I/O ports of the CPU are labeled with a mnemonic such as s2(L) for line 02. The "s" indicates a select code, "2" indicates that it is the third least significant bit of the un-decoded select code, and "(L)" indicates that the line is true (1) when the logic level is low. All bit-position numbering begins with 0. The select codes go out on the Instrument Bus through Select Buffers which are simple inverters. Thus s2(L) goes out on the bus as s2(H). Decoded codes are labeled as e=1(L) for example. The "e" indicates an enable code, "=" indicates decoding, "1" indicates a decoded hexadecimal 1 (binary 0001), and "(L)" indicates the logic level corresponding to a true. The mnemonic e=1 corresponds to e3e2e1e0=0001. Data codes are also buffered. However, unbuffered data lines are also connected to the Instrument Bus for reading data back to the I/O ports.

PRINCIPLES OF OPERATION—SERVICE SHEET BD4

The example of Figure 8D-1 will be used to illustrate how the 8 dB gain setting is selected for the Programmable Gain Amplifier on the Input Amplifier Assembly. The amplifier (not shown) is set for 8 dB gain when the output line labeled 8 dB(L) of Data Latch A7U11 goes low. A7U11 is on the Latch Assembly. Register U11 is simply

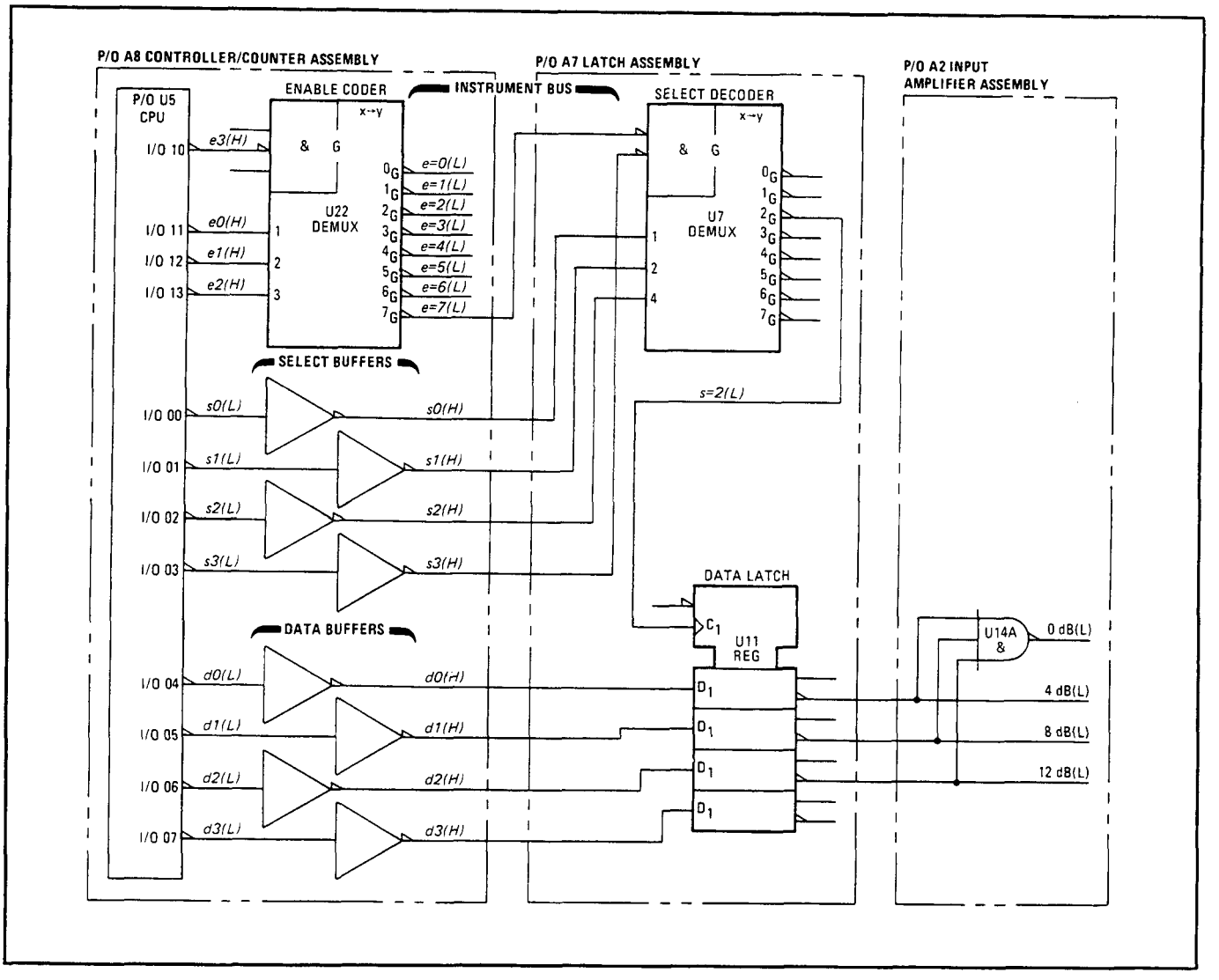


Figure 8D-1. Example Showing Instrument Bus Hookup

a latch; it does not decode the data. To set the amplifier gain to 8 dB, the CPU sends out the binary enable code 0111 (hexadecimal 7), select code 0010 (hexadecimal 2), and data code 0010 (hexadecimal 2). The Enable Decoder activates the line e=7(L). (The decoder was enabled because e3(H) was low.) Since s3(H) is low, and since e=7(L) is also low, the Select Decoder (A7U7) is enabled. The three least significant bits of the select code are decoded and activate the s=2(L) line out of the decoder. This line clocks the data into the Data Latch A7U11. Since the d1(H) line is high, the 8 dB(L) line goes low. This sets the amplifier gain to 8 dB. (NAND gate A2U14A decodes the three least significant bits of A7U11. It causes the 0 dB(L) line to go low when e=7, s=2, d0=0, d1=0, and d2=0.)

There is a direct relationship between the codes output on the Instrument Bus and the Direct Control Special Functions discussed in paragraph 8-22. If the enable, select, and data codes are combined into a hexadecimal number "*esd*", this becomes the Direct Control suffix. In the example here it is 722, corresponding to Direct Control code 0.722 discussed in the example there. Instrument control can be visualized as a series of Direct Control Special Functions issued under program control.

The example above decoded only three of the four select code bits and used the data bits directly (or inverted them). Notice that if the code *esd*=727 were issued, the 4 dB, 8 dB, and 12 dB lines would all be activated. On some assemblies the data codes may be decoded and select codes above 7 may be used. On other assemblies

certain select codes are used to enable readback devices which read back status or measurement data onto the unbuffered data lines. This is discussed in more detail in connection with *Direct Control Special Functions*, paragraph 8-22.

In addition to the Instrument Control Latches which interface the communication between the Controller and the measurement and source circuits, the Latch Assembly also contains the Counter input conditioning circuits and plotter control circuits.

The Parity Check latch is used on power-up to check the integrity of the Data lines of the Instrument Bus. Overload conditions from either the Input Overload Detector of the Overload Detector on the output amplifier circuit (see Service Sheet BD2) are read back to the Instrument Bus through the Overload Readback latch.

The Counter Input Switch selects whether the input to the Counter Schmitt Trigger is from the Input Amplifier or Output Amplifier. The Counter Input Schmitt Trigger conditions the analog input signal to make it compatible with the TTL logic of the Counter. It has self-setting upper and lower references. Input peak detectors set the two references at one-half the level of the positive peak. This gives excellent noise immunity over a wide range of input levels. The FMUX Select switch selects the input to the Counter from either the Counter Input Schmitt Trigger or the Oscillator.

The X Axis and Y Axis DACs provide X and Y outputs to the rear panel for plotting during a frequency sweep. The DACs themselves output current which is converted to a voltage by transresistance amplifiers at their outputs. (The amplifiers also filter the signal.) Each DAC amplifier can output 0 to +10V in 255 steps. They are programed by the Controller via the Plotter Control and Input Latches, which also control the Pen Lift line.

Keyboard and Display (A1)

The Keyboard and Display Assembly is both an input peripheral and an output peripheral to the Controller. The pressing of a key is sensed by the Keystroke Detector. The detector interrupts the Microprocessor which then enters an interrupt service routine. The routine causes the key rows and columns to be scanned sequentially via the Key Row and Column Scanner to ascertain which key is down. This is accomplished by driving the rows in sequence with the select decoder and reading the state of the columns with the data readback lines (unbuffered data lines). If no key closure is found after 50 ms, the Microprocessor leaves this routine and begins making a new measurement.

Lighting of the key and annunciator lights and display digits and decimal points is by a straight-forward decoding of the Instrument Bus. The segments of the displays are lighted (and latched) one segment at a time. Note that the lights in the keys do not light as a direct result of a key closure. This is done by the Microprocessor, having recognized a key closure, sending the command out on the Instrument Bus to light the key light.

Remote Interface (A9)

The Remote Interface Assembly interfaces the Controller with the Hewlett-Packard Interface Bus (HP-IB). It performs necessary handshake operations, interprets the HP-IB control lines, and is both an input and an output peripheral to the Controller.

As an input peripheral, it accepts a byte from the HP-IB data lines under control of the bus handshake lines. It then interprets the data byte and the bus control lines to see if the byte is an address (talk or listen), a command, or a data byte. When a byte is processed, one of three things happens: (1) the byte is ignored, (2) the byte is processed in hardware (for example, some bus commands), or (3) the byte causes a Microprocessor interrupt (for example, codes received while addressed to listen). The Microprocessor treats an HP-IB interrupt as it would an interrupt from the Keyboard. However, the HP-IB interrupt service routine first checks whether or not the byte is a command (for example, Device Clear), address, or data (for example, "M1"). If it is an address or command, the byte is processed. If it is data, the routine first checks whether or not the instrument is in remote. If it is, the incoming byte is processed as program code. If not, the byte is ignored. After processing a byte, the Microprocessor tells the Remote Interface what to do next (for example, input another byte, set a status latch, or prepare to output a byte).

As an output peripheral, the Remote Interface takes a byte of status or measurement data from the Microprocessor and processes it over the HP-IB. It does this only after determining that the Audio Analyzer has been addressed to talk. The Require Service message (SRQ) is also output via the Remote Interface.

The Remote Interface Assembly consists of Handshake Logic, HP-IB Input/Output Transceivers, Interface Control Logic, Address Decoder, part of the Microprocessor, and Instrument Bus interface circuits. The Handshake Logic controls the asynchronous transfer of bytes over the HP-IB. It does this without interruption of the Microprocessor whenever the byte is data but the Audio Analyzer is not addressed to listen or whenever the byte is not an interrupting bus command. It also provides the means for the Microprocessor to complete the handshake if the byte is an interrupting type.

When the Audio Analyzer is accepting bytes, the Handshake Logic monitors the Microprocessor and HP-IB and signals the HP-IB talker or bus controller when the Audio Analyzer is ready to receive, tells the Microprocessor when valid data is on the HP-IB, and tells the HP-IB talker when the Microprocessor has accepted the data. When the Audio Analyzer is outputting data or status bytes, the Handshake Logic tells the Microprocessor when the HP-IB listener is ready to receive, provides the Microprocessor with logic to tell the listener when data is valid, and tells the Microprocessor when the listener has accepted data.

The HP-IB Input/Output transceivers act as HP-IB buffers and send/receive switches. They are controlled by the Interface Control Logic.

The Interface Control Logic, together with the Address Decoder, determines the talk or listen status of the interface and whether or not the Microprocessor should be interrupted. The ROM in the Handshake Control Logic is addressed by two of the HP-IB data lines, the Address Decoder, and one of the HP-IB control lines (Attention, ATN). The ROM contains the control information for the Interface Control Logic and the Microprocessor.

If the Audio Analyzer's listen address is recognized by the Address Decoder, the Microprocessor attempts to set the Remote Enable Flip-Flop. If the HP-IB Remote Enable (REN) control line is true, the flip-flop is set (if not already set), and the Microprocessor sets a status bit in memory. Each time the Microprocessor performs any remote-dependent operation, it checks both the status bit and the flip-flop output (Remote Enable Latch, RNL). Both must be set for the instrument to remain in remote. If REN goes false at any time, the Remote Enable Flip-Flop is cleared, and the instrument is no longer in remote.

The Address Decoder compares the address set by the Address Switches with the five least-significant input bits to determine if the instrument is being addressed. The Interface Control Logic looks at the output of the Address Decoder and the next two input bits to determine if it is a talk or listen address and if the instrument should respond to it. The result of this determination modifies the address to the ROM in the Interface Control Logic.

The Address Readback Gates output the address from the Address Switches onto the Instrument Bus data lines when Special Function 21 (HP-IB Address) is selected. This is how the Controller reads the HP-IB address. (See *HP-IB Address* in the *Detailed Operating Instructions* in Section 3.)

The portion of the Microprocessor that directly handles the HP-IB input/output resides on the Remote Interface Assembly. This is the Peripheral Input/Output (PIO). The PIO is a device that routes the HP-IB data to and from the CPU and the HP-IB, provides a communication link between the CPU and the Remote Interface hardware, and provides the means for interrupting the CPU. One of the two, eight-bit PIO output ports connects to the HP-IB data lines and the other to the handshake and control logic.

Although the Remote Interface Assembly receives data and operating information from the PIO, it is primarily through the Instrument Bus that it is controlled. (Commands such as SRQ that need rapid processing come from the PIO.) A Select Decoder decodes the select lines when enabled by code e=3. The decoded select lines enable or disable parts of the Remote Interface Assembly.

TROUBLESHOOTING

General

Procedures for checking the digital circuits of the instrument are given below. The blocks or points to check are marked on the block diagram with a check mark and a number inside, for example, ⟨✓3⟩. Before performing any check, perform all the checks on Service Sheet BD1.

Equipment

Digital Test/Extender Board	HP 08903-60018
Oscilloscope	HP 1740A
Signature Analyzer	HP 5005A
Voltmeter	HP 3455A

⟨✓1⟩ Counter (Including Counter Input) Check

NOTE

For this check, the Audio Analyzer's Source is assumed to be working properly.

1. On the Audio Analyzer, key in 41.0 SPCL to initialize the instrument. Set the INPUT and OUTPUT switches to ground. Set the 80 kHz LOW PASS filter off. Set FREQ to 100 kHz and AMPTD to 1V. Connect the HIGH OUTPUT to the HIGH INPUT.

2. Connect a high-impedance, dc coupled oscilloscope to A7TP2 (FMUX).

3. On the Audio Analyzer, key in 46.0 SPCL to set the Counter to measure the Oscillator frequency. The waveform on the oscilloscope should be a TTL square wave with a period of approximately 10 μs. If faulty, see Service Sheet 13 and check the FMUX Select.

4. Disconnect the cable to the Audio Analyzer's INPUT. The waveform on the oscilloscope should remain unchanged. If faulty, see Service Sheet 13 and check the FMUX Select.

5. Reconnect the cable to the Audio Analyzer's INPUT. Key in 46.1 SPCL to set the Counter to measure the input frequency. The waveform should remain unchanged. If faulty, see Service Sheet 13 and check the Input Select, Counter Input Schmitt Trigger, and the FMUX Select.

6. Disconnect the cable to the Audio Analyzer's INPUT. The waveform on the oscilloscope should be a steady TTL high or low. If faulty, see Service Sheet 13 and check the Input Select and Counter Input Schmitt Trigger.

7. Reconnect the cable to the Audio Analyzer's INPUT. Key in 46.3 SPCL to set the Counter to measure the frequency at the output amplifier. The waveform on the oscilloscope should again be a TTL square wave with a period of approximately 10 μs. If faulty, see Service Sheet 13 and check the Input Select.

8. Disconnect the cable to the Audio Analyzer's INPUT. The waveform on the oscilloscope should become a steady TTL high or low. If faulty, see Service Sheet 13 and check the Input Select.

9. Reconnect the cable to the Audio Analyzer's INPUT. Connect the oscilloscope to A8TP5 (CYC). The waveform on the oscilloscope should be bursts of TTL square waves where the period of the pulses in the bursts is approximately 10 μs and the bursts, although difficult to measure, are approximately 170 ms apart. If faulty, see Service Sheet 14 and check the Mode Select and Cycle Counter Gate.

10. Connect the oscilloscope to A8TP6 (CLK). The waveform on the oscilloscope should be bursts of TTL square waves where the period of the pulses in the bursts is 500 ns and the bursts, although difficult to measure, are approximately 170 ms apart. If faulty, see Service Sheet 14 and check the Mode Select and Frequency Gate.

11. Connect the oscilloscope to A8TP2 (CLK CRY). The waveform on the oscilloscope should be bursts of TTL square waves where the period of the pulses in the bursts is 1 ms and the bursts, although difficult to measure, are approximately 170 ms apart. If faulty, see Service Sheet 14 and check the Clock Counter.

12. Connect the oscilloscope to A8TP1 (CYC CRY). The waveform on the oscilloscope should be bursts of TTL square waves where the period of the pulses in the bursts is 320 μs and the bursts, although difficult to measure, are approximately 170 ms apart. If faulty, see Service Sheet 14 and check the Cycle Counter.

Hint: If all steps above give positive results but the Counter is still suspected to be faulty, see Service Sheet 14 and check the Carry Gating and the Counter Output Gating.

⟨√2⟩ Controller Kernel Check

CAUTION

MOS and CMOS ICs can be damaged by static charges and circuit transients. Do not remove the A8 Controller/Counter Assembly from the instrument while power is applied. Discharge the board and replacement IC to the same potential. (Use a conductive foam pad such as HP 4208-0094.) When unplugging ICs, place the board on a conductive pad. When the IC is unplugged, insert it into the foam also.

Several ICs on these assemblies are held in high-grip sockets. Both the socket and the device can be damaged if an attempt is made to remove the device with an IC extraction tool. The recommended procedure is to first ground the tip of a small blade-type screwdriver, then slide the tip between the IC and the socket and slowly pry up the IC one pair of pins at a time.

1. Switch LINE to OFF. Extend the A8 Controller/Counter Assembly with the Digital Test/Extender Board. Connect the ribbon cable on the extender board to the empty socket A8J1 (ADR BUS). Switch LINE to ON.

2. Check A8TP14 (+12V) with dc voltmeter. The voltage should be between +11.4 and +12.6 Vdc. If faulty, see Service Sheet 20 and check the +12V Regulator.

3. Short A8TP4 (RES) to A8TP3 (GND). This resets the Controller and forces a short write (instruction) cycle. Connect a high-impedance, dc coupled oscilloscope to A8TP13 (WRT). The waveform should be TTL pulses with a period of 2 μs. If faulty, see Service Sheet 15 and check the clock circuit and Φ line.

4. Set the switches labeled ROMC on the extender board to CLOSED. This forces the SMI to step through its addresses.

5. On the A8 Controller/Counter Assembly, connect the signature analyzer clipleads as follows:

Clock	A8TP13 (WRT)
Ground	A8TP3 (GND)

On the extender board, connect the signature analyzer clipleads as follows:

Start	ADDRESS 15
Stop	ADDRESS 15

6. Set the signature analyzer's start, stop, and clock to trigger as follows:

Start	Falling Edge
Stop	Falling Edge
Clock	Rising Edge

7. Check the following test points listed in Table 8D-1 on the extender board or on A8 with the signature analyzer probe. If all signatures are bad except GND, see Service Sheet 15 and replace the SMI. If only one ADDRESS line is faulty, see Service Sheets 15 and 16 and check the SMI and the address line.

8. Check A8TP17 (RAM write) and A8TP18 (CPU read) with a dc coupled oscilloscope. RAM write should be a TTL high, CPU read should be a TTL square wave with a period of 2 μs. If faulty, see Service Sheet 15 and check the SMI and the load on the two lines.

TROUBLESHOOTING—SERVICE SHEET BD4

Table 8D-1. Signatures for Address Lines, √2 Step 7

Test Point	Signature	Test Point	Signature
A8TP16 (+5V)	0001	ADDRESS 8	HC89
A8TP3 (GND)	0000	ADDRESS 7	52F8
ADDRESS 15	755U	ADDRESS 6	UPFH
ADDRESS 14	3827	ADDRESS 5	0AFA
ADDRESS 13	3C96	ADDRESS 4	5H21
ADDRESS 12	HAP7	ADDRESS 3	7F7F
ADDRESS 11	1293	ADDRESS 2	CCCC
ADDRESS 10	HPP0	ADDRESS 1	5555
ADDRESS 9	2H70	ADDRESS 0	UUUU

8. Check A8TP17 (RAM write) and A8TP18 (CPU read) with a dc coupled oscilloscope. RAM write should be a TTL high, CPU read should be a TTL square wave with a period of 2 μs. If faulty, see Service Sheet 15 and check the SMI and the load on the two lines.

9. Switch LINE to OFF. Remove A8U30 (CPU External Register or RAM) from its socket.

10. Switch LINE to ON. Check the CONTROL BUS test points listed in Table 8D-2 on the extender board with the signature analyzer probe. If signatures are faulty, see Service Sheet 15 and check the Decoders and ROMs. **Serial Prefix 2652A and Above**: If signatures are faulty, replace the ROM.

Serial Prefix 2450A to 2520A:

NOTE

The signatures listed in Table 8D-2 are valid only for the software with the specified date (or ROM part numbers) listed in Table 8D-3.

Table 8D-2. Signatures for Data Lines, √2 Step 10

Test Point	Signature	Test Point	Signature
DATA 0	6AF2	DATA 4	HP04
DATA 1	6PH9	DATA 5	57A4
DATA 2	1AAH	DATA 6	FF71
DATA 3	C317	DATA 7	C96A

Table 8D-3. Valid ROM Part Numbers, √2 Step 10 Note*

ROM Number	Part Number	ROM Number	Part Number
1	08903-80016	6	08903-80021
2	08903-80017	7	08903-80022
3	08903-80018	8	08903-80023
4	08903-80019	9	08903-80024
5	08903-80020		
* Valid software date 11.15 1984.			

TROUBLESHOOTING—SERVICE SHEET BD4

NOTE

The signatures listed in Tables 8D-2a and 8D-2b are valid only for the software with the specified date (or ROM part numbers) listed in Tables 8D-3a or 8D-3b.

Serial Prefix 2520A to 2614A:

Table 8D-2a. Signatures for Data Lines, √2 Step 10

Test Point	Signature	Test Point	Signature
DATA 0	5F7C	DATA 4	FU4U
DATA 1	5427	DATA 5	9A27
DATA 2	508A	DATA 6	9C65
DATA 3	0487	DATA 7	6074

Table 8D-3a. Valid ROM Part Numbers, √2 Step 10 Note*

ROM Number	Part Number	ROM Number	Part Number
1	1818-3741	6	1818-3746
2	1818-3742	7	1818-3747
3	1818-3743	8	1818-3748
4	1818-3744	9	1818-3749
5	1818-3745		
* Valid software date 2.11 1985.			

Serial Prefix 2652A and Above

Table 8D-2b. Signatures for Data Lines, √2 Step 10

Test Point	Signature	Test Point	Signature
DATA 0	UU90	DATA 4	860U
DATA 1	3FHU	DATA 5	UCC0
DATA 2	9HCP	DATA 6	AU5P
DATA 3	6498	DATA 7	2207

Table 8D-3b. Valid ROM Part Number, √2 Step 10 Note*

ROM Number	Part Number
10	08903-80036
* Valid software date 8.22 1986.	

√3 CPU External Register (RAM) Check

1. Perform the *Power-Up Checks on Service Sheet BD1.*

√4 CPU I/O Port Check

1. Switch LINE to OFF. Extend the A8 Controller/Counter Assembly with the Digital Test/Extender Board. Switch LINE to ON.

NOTE

Check that the switches labeled ROMC on the extender board are set to OPEN.

2. Key in 0.0 SPCL. Check the Instrument Bus test points listed in Table 8D-4 on the extender board with an oscilloscope or signature analyzer probe (used as a logic probe). If faulty, see Service Sheet 15 and check the CPU and I/O port decoders and buffers.

Table 8D-4. Levels on Instrument Bus, ⟨✓4⟩ Step 2

Test Point	Measured Signal
ENABLE 0	Low-Going TTL Pulses, Period ≈30 ms
SELECT 0 to 3	TTL Low
DATA (H) 0 to 3	TTL Low
DATA (L) 0 to 3	TTL High

3. Key in 0.0 S (Shift) 5 S 5 SPCL. Recheck the test points listed in Table 8D-5. If faulty, see Service Sheet 15 and check the CPU and I/O port decoders and buffers.

Table 8D-5. Levels on Instrument Bus, ⟨✓4⟩ Step 3

Test Point	Measured Signal
SELECT 0 to 3	TTL High
DATA (H) 0 to 3	TTL High
DATA (L) 0 to 3	TTL Low

4. Key in the Special Functions listed in Table 8D-6. For each entry, the indicated ENABLE test point on the extender board should show low-going TTL pulses with a period of approximately 30 ms. All other ENABLE test points should be TTL highs. If faulty, see Service Sheet 15 and check the Enable Decoder and CPU.

Table 8D-6. Pulses, ⟨✓4⟩ Step 4

Special Function	Test Point
0.0	ENABLE 0
0.1	ENABLE 1
0.3	ENABLE 3
0.4	ENABLE 4
0.5	ENABLE 5
0.6	ENABLE 6
0.7	ENABLE 7

⟨✓5⟩ Keyboard Key Check

1. Key in 60.0 SPCL. As the Special Function code is entered, 60.0 should appear in the display. This indicates that the Controller responds to keyboard interrupts. If faulty, see ⟨✓7⟩ *Front-Panel LED Check.* While pressing the SPCL key, 33 should appear in the display. After the SPCL key is released, 99 should appear. If other numbers appear, continue on.

2. Jumper pin 7 of A8U6 (EXT INT) to A8TP3 (GND). This defeats the keyboard interrupt.

3. Press the keys one at a time and compare the display with the key codes shown in Figure 8D-2. If a code other

than 99 appears in the display with no key pressed, the key corresponding to the displayed key code is probably stuck down; see Service Sheet 17. If a wrong code appears for one or more keys, check the corresponding key and decoder; see Service Sheet 20.

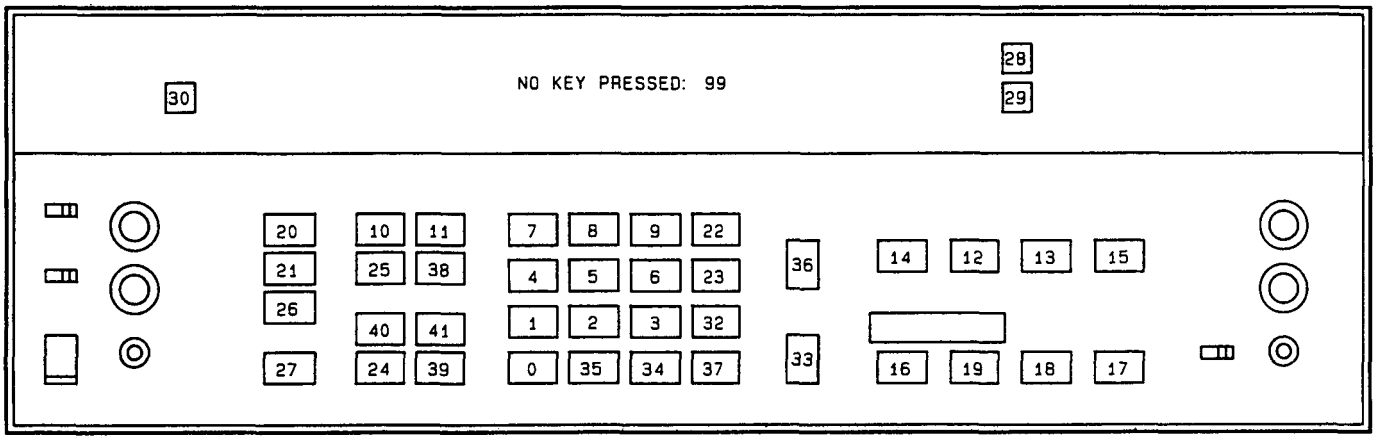


Figure 8D-2. Key Codes for Special Function 60.0, ⟨✓5⟩ Step 3

⟨✓6⟩ Keyboard Interrupt Check

1. Connect high-impedance, dc coupled oscilloscope to pin 7 of A8U6 (EXT INT). The voltage should read a TTL high. Pressing any key should result in a TTL low which should remain low for 40 to 60 ms after the key is released. If faulty, see Service Sheet 17 and check the Keystroke Detector.

⟨✓7⟩ Front-Panel LED Check

1. Perform the *Front-Panel LED Check* on Service Sheet BD1.

⟨✓8⟩ HP-IB Check

1. See Service Sheet 19.

⟨✓9⟩ Instrument Control Latches and Parity Check and Overload Readback Check

1. See Service Sheet 12.

⟨✓10⟩ Plotter Control Circuits Check

NOTE

The following procedure assumes that the instrument is capable of making a swept ac level measurement.

1. On the Audio Analyzer, key in 41.0 SPCL to initialize the instrument. Set the OUTPUT and INPUT switches to ground. Set AMPTD to 1V. Connect the HIGH OUTPUT to the HIGH INPUT.

2. Connect a dc voltmeter to the rear-panel X AXIS, Y AXIS, and PEN LIFT outputs and observe the voltage as the keys indicated in Table 8D-7 are pressed.

Hint: If the upper limits of the X AXIS or Y AXIS outputs are only slightly out of limits, consult Table 5-1, *Factory Selected Components*, for A7R8 and A7R10.

Table 8D-7. Plotter Control Circuits Check, ⟨✓10⟩ Step 2

Key Pressed	X AXIS	Y AXIS	PEN LIFT
START FREQ	−10 to +10 mVdc	−10 to +10 mVdc	TTL High
STOP FREQ	+9.7 to +10.3 Vdc	+9.7 to +10.3 Vdc	TTL High
SWEEP	Slow increase from ≈0 to ≈ +10 Vdc	Steady at ≈ +5 Vdc	TTL Low

SERVICE SHEET 12---A7 Latch Assembly (Data Latches)

PRINCIPLES OF OPERATION

NOTE

The following discussions require an understanding of the operation of the Instrument Bus (see Instrument Bus, *Service Sheet BD4) and of the Instrument Bus readback (see* Direct Control Special Functions, *paragraph 8-22).*

General

This portion of the Latch Assembly (A7) contains many of the select decoders and data latches which decode the Instrument Bus and drive the digital-to-analog devices in the instrument hardware. The circuit also includes two overload flip-flops and a Parity Check.

Data Latches and Select Decoder

The Data Latches are of two types. One type (for example, register U9) decodes and latches all four data lines of the Instrument Bus when enabled by a unique select code (for example, U9 is enabled by s=3(L) from Select Decoder U7). Continuing the example, U7 is enabled when e=7(L) is low (that is, true) and s3(H) is low (that is, false, in other words, *s* is between 0 and 7). Thus, U9 responds to *esd*=73*d*, where *d* is the arbitrary data input.

The other type (for example, register U22) is enabled by a unique enable code (for example, *e*=6). The three least significant bits of the select code (*s*0, *s*1 and *s*2) are then decoded, and the input (for example, d0(H)) is loaded and latched into the output enabled by the decoding of the select inputs. Thus for example, if *esd*=631, a high is loaded into OS FRQ4. Note that d0(H) is high since *d*=1 (binary 0001). The other outputs of the data latch are unaffected. Also note that more than one data latch can be activated with a single Direct Control Special Function (for example, if *esd*=633, a high is loaded into both OS FRQ5 of U23 and OS FRQ4 of U22).

Overload Flip-Flops

When an input overload is detected (see Service Sheet 2), Input Overload Flip-Flop U14 is reset. Pin 5 of U14A resets Data Latches U9, U11, and U12 which sets the gain of the input circuits to minimum. The state of U14A is read by the Controller via U15B. To read U14A, the Controller issues *esd*=700 to the Instrument Bus. If d0(L) is low, the Input Overload Flip-Flop is known to be reset. To set U14A, the Controller issues *esd*=772 to the Instrument Bus. Since d1(H) is high, pin 8 of U14B is low, which sets U14A.

The Output Overload Flip-Flop, U13, operates in a manner similar to U14. When an overload is detected (see Service Sheet 6), U10 is reset which sets the gain of the Output Amplifier to minimum. The state of U10 is read when the Controller issues *esd*=740 to the Instrument Bus. The code *esd*=760 sets the flip-flop.

Parity Check

The Parity Check circuit allows the Controller to test the integrity of the data lines of the Instrument Bus. To check parity, the Controller sends out the sixteen codes *esd*=740 to *esd*=74F. For each code, the output of exclusive-OR gate U8C is read back by the Controller. The output of U8C is low when *d*0+*d*1+*d*2+*d*3 is even, or high when it is odd. Parity is checked only during instrument power up (see *Power-Up Checks,* paragraph 8-27).

TROUBLESHOOTING

General

Procedures for checking the Latch Assembly are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. The A8 Controller/Counter Assembly must be extended using the extender board (HP 08903-60018). The A7 Latch Assembly must be extended using three 44 pin extender boards.

Equipment

Digital Test/Extender Board	HP 08903-60018
Oscilloscope	HP 1740A
Signature Analyzer	HP 5005A
44 Pin Extender Boards (3)	HP 08901-60084

⟨✓1⟩ Latches Check---Using Signature Analysis

1. Switch LINE to OFF. Extend the A8 Controller/Counter Assembly using the digital test/extender board (HP 08903-60018) and the A7 Latch Assembly using the three 44 pin extender boards (HP 08901-60084).

2. Interconnect the Controller/Counter Assembly, the Latch Assembly, the extender boards, and the signature analyzer as shown in Figure 8D-3. Set the switches on the digital test/extender board to the OPEN position.

3. Unplug assemblies A2 through A6. (They do not need to be completely removed.)

4. Set the signature analyzer's start, stop, and clock to trigger as follows:

Start	Falling Edge
Stop	Falling Edge
Clock	Rising Edge

5. Connect A8TP9 (TEST C) to A8TP3 (GND).

NOTE

Disregard the front-panel indications when performing signature analysis.

6. Set LINE switch to ON. Verify that Test LEDs A, B, and D light and remain lit.

7. Remove the ground from A8TP9. Verify that Test LED C lights and remains lit.

8. Check the pins on the ICs indicated in Table 8D-8 with the signature analyzer.

NOTE

In addition to the signatures shown in Table 8D-8, Service Sheet 13 contains signatures that can be checked using the current test setup.

Hint: If nearly all signatures are faulty, see Service Sheet BD4 and check the CPU I/O port.

⟨✓2⟩ Latches Check---Using Direct Control Special Functions

NOTE

If the keyboard is operating properly, the latches can be checked using Direct Control Special Functions and a logic probe. A signature analyzer is not needed. Extend the Latch Assembly when performing this check.

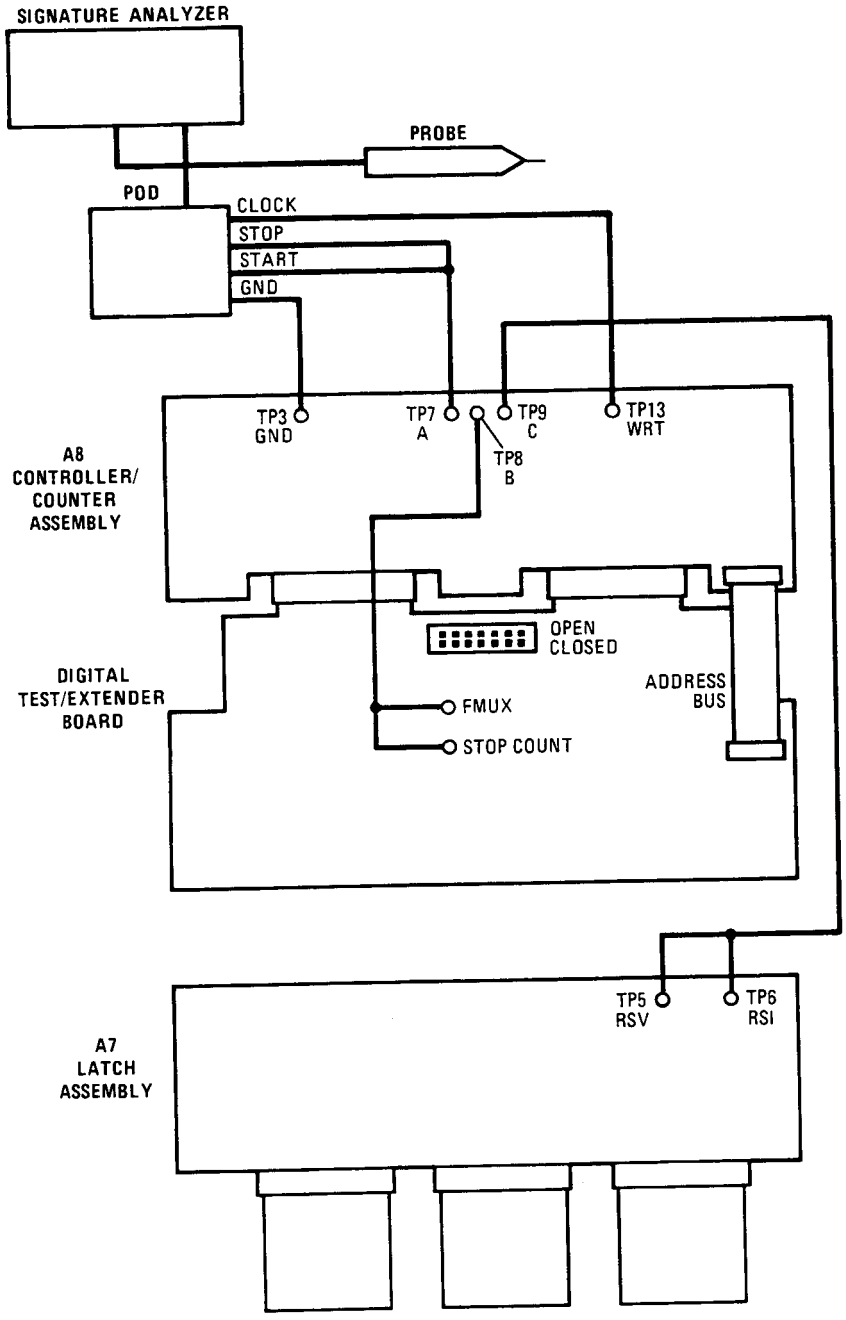


Figure 8D-3. Latch Assembly Troubleshooting Setup, ⟨J1⟩ *Step 2*

Table 8D-8. Signatures for ⟨J1⟩ Step 8

Pin	U7	U8	U9	U10	U11	U12	U13	U14	U15	Pin
1	600A	2941	801H	AA99	801H	801H	4824	40AA	0000	1
2	9CU7	2941	78A1	C393	8U6U	57H5	57H5	4824	72UC	2
3	7PAA	0000	3085	UCC7	F74C	A345	0A07	HP9P	1UU1	3
4	PH3H	2941	57H5	57H5	57H5	4824	4824	8160	96CA	4
5	35F6	2941	F4F9	F4F9	F4F9	8P2C	F944	801H	F839	5
6	4824	0000	3085	UCC7	F74C	F60U	8160	F839	1UU1	6
7	0A07	0000	78A1	C393	8U6U	0000	0000	0000	0000	7
8	0000	0000	0000	0000	0000	F60U	P2CH	8160	1UU1	8
9	P1A9	0000	H4AA	2308	A5AP	8P2C	AA99	F944	P2CH	9
10	2308	0000	78A1	C393	8U6U	4824	8160	–	A98H	10
11	3AHU	0000	3085	UCC7	F74C	A345	P1A9	0A07	–	11
12	H4AA	–	5C95	5C95	5C95	F4F9	4824	F4F9	–	12
13	A5AP	–	7FC0	7FC0	7FC0	801H	40AA	–	–	13
14	A345	4824	3085	UCC7	F74C	4824	4824	4824	4824	14
15	HP9P		78A1	C393	8U6U					15
16	4824		4824	4824	4824					16

Pin	U22	U23	U24	U25	U26	U27	U28	U29	U30	Pin
1	600A	600A	600A	600A	600A	600A	600A	600A	HP9P	1
2	9CU7	9CU7	9CU7	9CU7	9CU7	9CU7	9CU7	9CU7	96CA	2
3	7PAA	7PAA	7PAA	7PAA	7PAA	7PAA	7PAA	7PAA	3AHU	3
4	26U7	26U7	26U7	26U7	54UP	54UP	54UP	54UP	72UC	4
5	H3HU	H3HU	H3HU	H3HU	P322	P322	P322	P322	–	5
6	7255	7255	7255	7255	H3CF	H3CF	H3CF	H3CF	–	6
7	9C3C	9C3C	9C3C	9C3C	68U6	68U6	68U6	68U6	0000	7
8	0000	0000	0000	0000	0000	0000	0000	0000	–	8
9	3F58	3F58	3F58	3F58	U12F	U12F	U12F	U12F	–	9
10	HA3H	HA3H	HA3H	HA3H	404F	404F	404F	404F	–	10
11	10U4	10U4	10U4	10U4	F798	F798	F798	F798	–	11
12	2941	2941	2941	2941	6A46	6A46	6A46	6A46	A98H	12
13	57H5	F4F9	5C95	7FC0	57H5	F4F9	5C95	7FC0	P1A9	13
14	77F6	77F6	77F6	77F6	F9P1	F9P1	F9P1	F9P1	4824	14
15	4824	4824	4824	4824	4824	4824	4824	4824		15
16	4824	4824	4824	4824	4824	4824	4824	4824		16

Note: The signature for a high or +5V is 4824. The signature for a low or ground is 0000. The "–" indicates that there is no valid signature for the pin. A blank indicates no pin on the IC.

Select Decoder

1. Key in the Direct Control Special Functions indicated in Table 8D-9. For each setting, check the pins on U7 indicated.

Data Latches U9, U10, and U11

2. Key in the Direct Control Special Functions indicated in Table 8D-10. For each setting, check the pins on the IC indicated.

Hint: Pin 1 on the ICs should be high.

Table 8D-9. Select Decoder Check, ⟨✓2⟩ Step 1

Direct Control Special Function	Level (TTL) at U7 Pin							
	15	14	13	12	11	10	9	7
0.700	*	H	H	H	H	H	H	H
0.710	H	*	H	H	H	H	H	H
0.720	H	H	*	H	H	H	H	H
0.730	H	H	H	*	H	H	H	H
0.740	H	H	H	H	*	H	H	H
0.750	H	H	H	H	H	*	H	H
0.760	H	H	H	H	H	H	*	H
0.770	H	H	H	H	H	H	H	*
* Low-going TTL pulses, approximately 30 ms period.								

Table 8D-10. Data Latches Check, ⟨✓2⟩ Step 2

Direct Control Special Function	IC to Check	Level (TTL) at Pin							
		2	3	7	6	10	11	15	14
0.720	U11	L	H	L	H	L	H	L	H
0.72F	U11	H	L	H	L	H	L	H	L
0.730	U9	L	H	L	H	L	H	L	H
0.73F	U9	H	L	H	L	H	L	H	L
0.750	U10	L	H	L	H	L	H	L	H
0.75F	U10	H	L	H	L	H	L	H	L

Data Latch U12

3. Key in 0.710 SPCL. Pins 6 and 8 of U12 should be low.

4. Key in 0.71F SPCL. Pins 6 and 8 of U12 should be high.

Overload Flip-Flops

5. Momentarily ground A7TP6 (RSI). Pin 5 of U14 should be low; pin 6 should be high.

6. Key in 0.700 SPCL. Pin 5 of U14 should be high; pin 6 should be low.

7. Key in 0.770 SPCL. Momentarily ground A7TP6 again. Key in 0.772 SPCL. Pin 5 of U14 should be high; pin 6 should be low.

8. Momentarily ground A7TP5 (RSV). Pin 9 of U13 should be low; pin 8 should be high.

9. Key in 0.760 SPCL. Pin 9 of U13 should be high; pin 8 should be low.

10. Key in 0.770 SPCL. Momentarily ground A7TP5 again. Key in 0.771 SPCL. Pin 9 of U13 should be high; pin 8 should be low.

Data Latches U22 through U29

11. Key in the Direct Control Special Functions indicated in Table 8D-11. For each setting, check the pin on the ICs indicated. For the special function code 0.6*s*0, the pin should be low, for 0.6*s*F it should be high.

12. Key in the Direct Control Special Functions indicated in Table 8D-12. For each setting, check the pin on the ICs indicated. For the special function code 0.6*s*0, the pin should be low, for 0.6*s*F it should be high.

Table 8D-11. Data Latches Check, ⟨✓2⟩ Step 11

Direct Control Special Function	Pin to Check on U22, U23, U24, and U25
0.600, 0.60F	4
0.610, 0.61F	5
0.620, 0.62F	6
0.630, 0.63F	7
0.640, 0.64F	9
0.650, 0.65F	10
0.660, 0.66F	11
0.670, 0.67F	12

Table 8D-12. Data Latches Check, ⟨✓2⟩ Step 12

Direct Control Special Function	Pin to Check on U26, U27, U28, and U29
0.500, 0.50F	4
0.510, 0.51F	5
0.520, 0.52F	6
0.530, 0.53F	7
0.540, 0.54F	9
0.550, 0.55F	10
0.560, 0.56F	11
0.570, 0.57F	12

Parity Check

13. Key in the Direct Control Special Functions indicated in Table 8D-13. For each setting, check the pins of U8 indicated.

Table 8D-13. Parity Check, ⟨✓2⟩ Step 13

Direct Control Special Function	Level (TTL) at U8 Pin		
	3	6	8
0.670	L	L	L
0.671	H	L	H
0.674	L	H	H
0.675	H	H	L

Readback Check

14. Key in 0.670 SPCL then 0.740 SPCL. The displays should read 0000 0000.

15. Key in 0.671 SPCL then 0.740 SPCL. The displays should read 0001 0000.

16. Key in 0.770 SPCL then 0.700 SPCL. Note the displays as A7TP6 (RSI) is momentarily grounded. The displays should read 0000 0000 when A7TP6 is ungrounded and 0001 0000 when grounded.

17. Key in 0.760 SPCL. Note the displays as A7TP5 (RSV) is momentarily grounded. The displays should read 0000 0000 when A7TP5 is ungrounded and 0001 0000 when grounded.

SERVICE SHEET 13---A7 Latch Assembly (DAC and Counter Trigger Circuits)

PRINCIPLES OF OPERATION

General

This portion of the Latch Assembly (A7) contains some of the data latches, the Counter Input Schmitt Trigger, and the X- and Y-Axis DACs.

Data Latches

The data latches are discussed in the *Principles of Operation* for Service Sheet 12.

Counter Input Schmitt Trigger

The Counter Input Schmitt Trigger converts the analog signal from the Input Amplifier (see Service Sheet 2) or the Output Amplifier (see Service Sheet 5) into a TTL-compatible signal which drives the Counter. Switching of the two signals is via the Input Switch, U18. The switch also grounds the unused input to minimize cross-talk.

U17 is a buffer amplifier which drives two peak detector diodes, CR7B and CR8B. CR7A and CR8A cancel the error in the peak detectors caused by the drop across the diodes. R17 to R20 divide the detected voltages by two. U2C and U2D are comparators that are referenced by the peak detectors. U2C trips at one-half the level of the positive peak of the input, U2D trips at one-half the negative peak. R22 and R23 add a small amount of hysteresis to the comparators. The outputs of U2C and U2D are applied to two inputs of set-reset flip-flop U1C and U1B. The output of U2D, however, is first inverted by U1D. The output of U1C drives NAND gate U16B, which acts as a switch.

Consider the action of the Schmitt trigger on an input signal. Assume that the signal is periodic but at the moment is at 0V and increasing. Also assume that the flip-flop is reset (U1C low). The output of U2C is high because the signal has not yet reached half the level of the positive peak. U2D is low because the signal is more positive than half the negative peak. U1D is high. When the signal reaches one-half the positive peak, U2C goes low and the flip-flop sets (U1C high), but when the signal returns below one-half the positive peak and U2C goes high again, the flip-flop remains set. When the signal goes below one-half the negative peak, U2D goes high and resets the flip-flop, but when the signal returns to above one-half the negative peak and U2D returns low again, the flip-flop remains reset. The action of the Schmitt trigger is depicted in Figure 8D-4.

The Counter Input Schmitt Trigger thus self-biases its upper and lower references to one-half the respective positive and negative peaks. The result is excellent immunity to noisy signals whether large or small. U16 forms an output switch to route the signal from either the Counter Input Schmitt Trigger or the Oscillator to the Counter.

X- and Y-Axis DACs

The X- and Y-Axis DACs are programed by the Controller via the Instrument Bus and Latch Assembly. The DACs output a current proportional to the binary weighting of the inputs. The current is converted to a voltage by transconductance amplifiers U3C and U3D. C23 and C24 provide heavy filtering. The outputs are applied to the rear-panel X AXIS and Y AXIS output connectors. The pen lift function is controlled by the Controller via the Instrument Bus and U6. (A high is issued to lift the pen.)

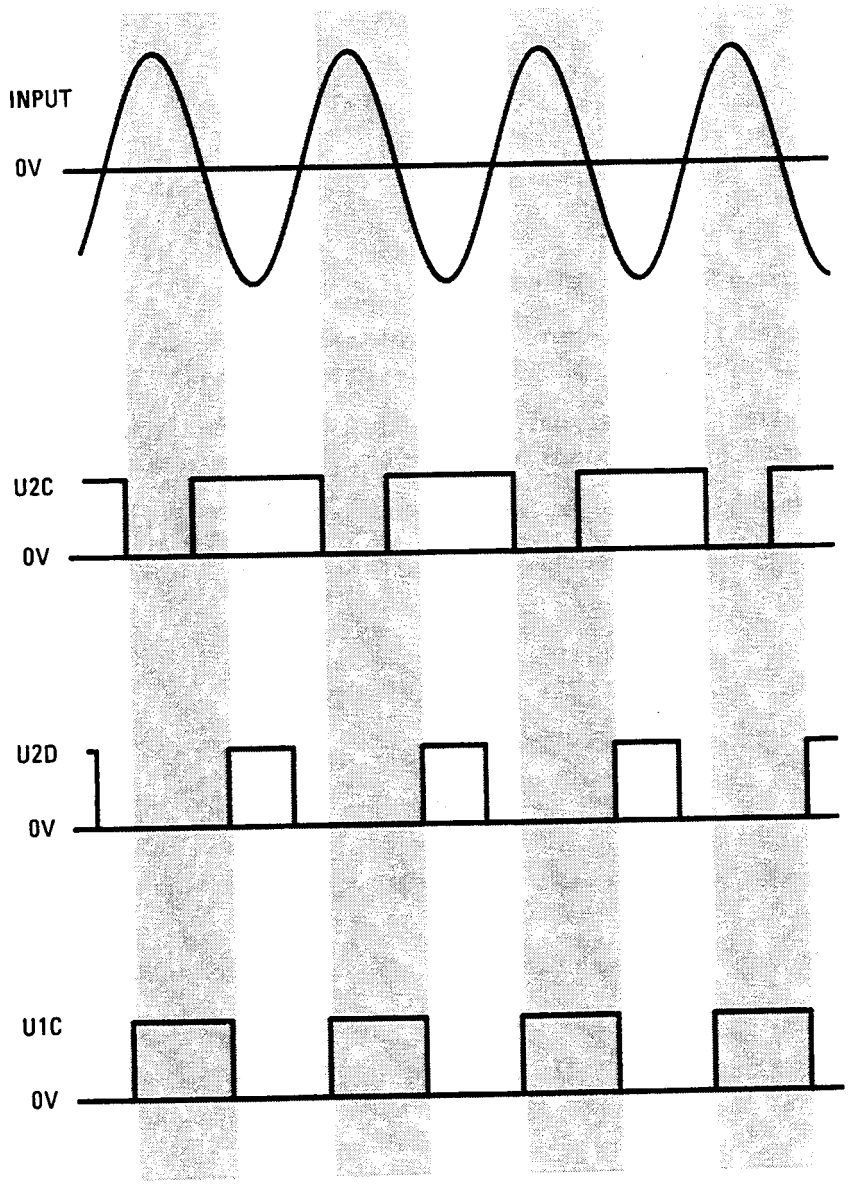


Figure 8D-4. Action of the Counter Input Schmitt Trigger for a Sine Wave Input

TROUBLESHOOTING

General

Procedures for checking the Latch Assembly are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. When troubleshooting the latches, the A8 Controller/Counter Assembly must be extended using the extender board (HP 08903-60018). The A7 Latch Assembly must be extended using three 44 pin extender boards.

Equipment

Digital Test/Extender Board	HP 08903-60018
Digital Voltmeter	HP 3455A
Oscilloscope	HP 1740A
Signature Analyzer	HP 5005A
44 Pin Extender Boards (3)	HP 08901-60084

⟨✓1⟩ Latches Check---Using Signature Analysis

1. Switch LINE to OFF. Extend the A8 Controller/Counter Assembly using the digital test/extender board (HP 08903-60018) and the A7 Latch Assembly using the three 44 pin extender boards (HP 08901-60084).

2. Interconnect the Controller/Counter Assembly, the Latch Assembly, the extender boards, and the signature analyzer as shown in Figure 8D-5. Set the switches on the digital test/extender board to the OPEN position.

3. Unplug assemblies A2 through A6. (They do not need to be completely removed.)

4. Set the signature analyzer's start, stop, and clock to trigger as follows:

Start	Falling Edge
Stop	Falling Edge
Clock	Rising Edge

5. Connect A8TP9 (TEST C) to A8TP3 (GND).

NOTE

Disregard the front-panel indications when performing signature analysis.

6. Set LINE switch to ON. Verify that Test LEDs A, B, and D light and remain lit.

7. Remove the ground from A8TP9. Verify that Test LED C lights and remains lit.

8. Check the pins on the ICs indicated in Table 8D-14 with the signature analyzer.

NOTE

In addition to the signatures shown in Table 8D-14, Service Sheet 12 contains signatures that can be checked using the current test setup.

Hint: If nearly all signatures are faulty, see Service Sheet BD4 and check the CPU I/O port.

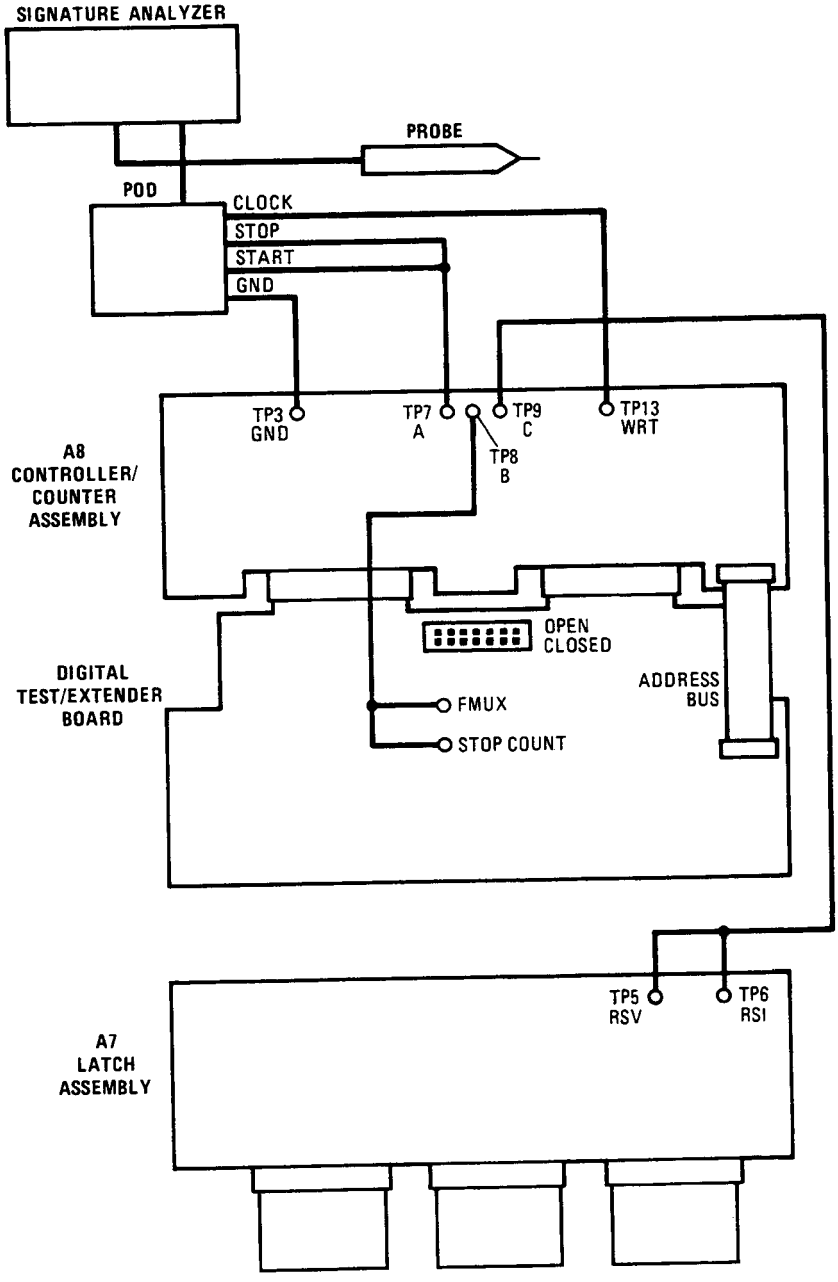


Figure 8D-5. Latch Assembly Troubleshooting Setup

Table 8D-14. Signatures for ⟨√1⟩ Step 8

Pin	U5	U6	U20	U21	Pin
1	600A	600A	600A	600A	1
2	9CU7	9CU7	9CU7	9CU7	2
3	7PAA	7PAA	7PAA	7PAA	3
4	2199	2199	2199	2199	4
5	C551	C551	C551	C551	5
6	6380	6380	6380	6380	6
7	44P4	44P4	44P4	44P4	7
8	0000	0000	0000	0000	8
9	F043	F043	F043	F043	9
10	6PA2	6PA2	6PA2	6PA2	10
11	9C44	9C44	9C44	9C44	11
12	1P0U	1P0U	1P0U	1P0U	12
13	F4F9	57H5	7FC0	5C95	13
14	6420	6420	6420	6420	14
15	4824	4824	4824	4824	15
16	4824	4824	4824	4824	16

Note: The signature for a high or +5V is 4824.
The signature for a low or ground is 0000.

⟨√2⟩ Latches Check—Using Direct Control Special Functions

NOTE

If the keyboard is operating properly, the latches can be checked using Direct Control Special Functions and a logic probe. A signature analyzer is not needed.

1. Key in the Direct Control Special Functions indicated in Table 8D-15. For each setting, check the pin on the ICs indicated. For special function code 0.4*s*0, the pin should be low, for 0.4*s*F it should be high.

Table 8D-15. Data Latches Check, ⟨√2⟩ Step 1

Direct Control Special Function	Pin to Check on U5, U6, U20, and U21
0.400, 0.40F	4
0.410, 0.41F	5
0.420, 0.42F	6
0.430, 0.43F	7
0.440, 0.44F	9
0.450, 0.45F	10
0.460, 0.46F	11
0.470, 0.47F	12

⟨√3⟩ X- and Y-Axis DACs and Pen Lift Check

1. On the Audio Analyzer, key in 41.0 SPCL to initialize the instrument. Set the INPUT switch to ground. Connect the rear-panel X AXIS output to the INPUT or to the input of a dc voltmeter.

2. Key in the Special Functions listed in Table 8D-16. For each setting, key in S (Shift) DC LEVEL or note the

level on the external voltmeter. The dc level should be as indicated. If the level is faulty, also check the pins on U4 indicated.

Table 8D-16. X-Axis Output Level Check, ⟨J3⟩ Step 2

Direct Control Special Function	Level (Vdc) at X AXIS Output	Level (TTL) at U4 Pin							
		5	6	7	8	9	10	11	12
0.450, 0.440	−0.002 to 0.002	L	L	L	L	L	L	L	L
0.448	0.03 to 0.05	L	L	L	L	L	L	L	H
0.444	0.07 to 0.09	L	L	L	L	L	L	H	L
0.442	0.14 to 0.17	L	L	L	L	L	H	L	L
0.441	0.29 to 0.33	L	L	L	L	H	L	L	L
0.440, 0.458	0.59 to 0.66	L	L	L	H	L	L	L	L
0.454	1.2 to 1.3	L	L	H	L	L	L	L	L
0.452	2.4 to 2.6	L	H	L	L	L	L	L	L
0.451	4.8 to 5.2	H	L	L	L	L	L	L	L

Hint: If the dc levels are all uniformly high or low, replace A7R10 with a value selected on the basis described in Table 5-1.

3. Connect the rear-panel Y AXIS output to the INPUT or to the input of a dc voltmeter. Key in the Special Functions listed in Table 8D-17. For each setting, key in S (shift) DC LEVEL or note the level on the external voltmeter. The dc level should be as indicated. If the level is faulty, also check the pins on U5, U6, U20, and U21 indicated.

Table 8D-17. Y-Axis Output Level Check, ⟨J3⟩ Step 3

Direct Control Special Function	Level (Vdc) at Y AXIS Output	Level (TTL) at U19 Pin							
		5	6	7	8	9	10	11	12
0.470, 0.460	−0.002 to 0.002	L	L	L	L	L	L	L	L
0.468	0.03 to 0.05	L	L	L	L	L	L	L	H
0.464	0.07 to 0.09	L	L	L	L	L	L	H	L
0.462	0.14 to 0.17	L	L	L	L	L	H	L	L
0.461	0.29 to 0.33	L	L	L	L	H	L	L	L
0.460, 0.478	0.59 to 0.66	L	L	L	H	L	L	L	L
0.474	1.2 to 1.3	L	L	H	L	L	L	L	L
0.472	2.4 to 2.6	L	H	L	L	L	L	L	L
0.471	4.8 to 5.2	H	L	L	L	L	L	L	L

Hint: If the dc levels are all uniformly high or low, replace A7R8 with a value selected on the basis described in Table 5-1.

4. Connect a dc voltmeter to the rear panel PEN LIFT output. Key in 0.421 SPCL (pen up). The voltage should read a TTL high.

5. Key in 0.420 SPCL (pen down). The voltage should read a TTL low.

⟨J4⟩ Counter Input Check

1. On the Audio Analyzer, key in 41.0 SPCL to initialize the instrument. Set the INPUT and OUTPUT switches both to ground. Set AMPTD to 1V. Key in 46.3 SPCL to set the counter to read the output amplifier signal. Connect the HIGH INPUT to the HIGH OUTPUT.

2. Connect a high-impedance, dc coupled oscilloscope to pin 3 of U18. The signal should be approximately 6 Vpp.

Hint: Pin 8 of U18 should be a TTL low, pin 1 a high. The signal at pin 10 of U18 should also be 6 Vpp; if it is not, see Service Sheet 5 and check Amplifier 4.

3. Key in 46.1 SPCL to set the counter to read the input frequency. The signal at pin 3 of U18 should be approximately 6 Vpp.

Hint: Pin 1 of U18 should be a TTL low, pin 8 a high. The signal at pin 2 of U18 should also be 6 Vpp; if it is not, see Service Sheet 2 and check the Weighting Bandpass and High-Pass Filters.

4. Connect the oscilloscope to pin 2 of U2 then to pin 13 of U2. The waveforms should be pulses with a period of 1 ms. The pulses at pin 2 of U2 should be +5V for 0.65 ms and −15V for 0.35 ms. The pulses at pin 13 should be the complement of those at pin 2.

Hint: The level at pin 5 of U2 should be approximately one half the level of the positive peak of the signal at pin 3 of U17. The level at pin 11 of U2 should be approximately one half the level of the negative peak of the signal at pin 3 of U17.

5. Connect the oscilloscope to pin 8 of U1. The waveform should be a TTL square wave.

6. Connect the oscilloscope to A7TP2 (FMUX). The waveform should be a TTL square wave which should become either high, low, or intermittent if the HIGH OUTPUT is disconnected.

Hint: Pins 4 and 9 of U16 should be a TTL high.

7. Key in 46.0 SPCL to set the counter to read the oscillator signal. The waveform should be a TTL square wave which should persist if the HIGH OUTPUT is disconnected.

Hint: Pin 4 of U16 should be a TTL low. Pin 10 of U16 should be a TTL high.

SERVICE SHEET 14---A8 Controller/Counter Assembly (Counter Circuits)

PRINCIPLES OF OPERATION

NOTE

The following discussions require an understanding of the operation of the Instrument Bus (see Instrument Bus, *Service Sheet BD4) and of the Instrument Bus readback (see* Direct Control Special Functions, *paragraph 8-22).*

General

The Counter consists of the Clock Counter, the Cycle Counter, gating circuits, and the Count Transfer Logic. The final stages of the Clock and Cycle Counters are in the Controller itself. The Clock Counter counts the 2 MHz clock (Φ) signal. The Cycle Counter counts the input or Oscillator signal (FMUX) and is not used when measuring voltage.

Clock Counter

The Clock Counter has three stages (U1, U2, and U14A) which form a divide-by-2048. The input to the counter, when enabled, is 2 MHz, and the output is 976.5625 Hz.

When the Counter is making a frequency measurement, the Frequency Gate (U19B) is armed by the Controller and gated by the input signal (FMUX). To arm the Frequency Gate, the Controller sends *esd*=7F0 out on the Instrument Bus which sets U29A (and also clears the Clock Counter). NAND gate U19B is thus high. Next, the Controller issues *esd*=7E0. This puts a high on the output of U4B, a high on U20C, and thus a low on U4A and the D1 input to U29A. The next falling edge of FMUX clocks the low into U29A and gates U19B, which routes the 2 MHz (Φ) signal into the Clock Counter. (U29B had previously been reset, putting a high on pin 5 of U19B and causing U19C to go high.)

As the count progresses, carries from flip-flop 4 of U14A are output to Instrument Bus line d2(L) via U17D and are counted by the Controller. U17D was enabled by the same signal from the Controller that armed U4A.

After a predetermined number of clock carries have been counted by the Controller, the Controller issues *esd*=7E1 to the Instrument Bus. U20C now goes low which puts a high on the D1 input of U29A. The next falling edge of FMUX clocks the high into U29A and inhibits U19B. If FMUX should be interrupted during the count, the Controller program terminates the count sequence after 16 more clock carries.

When voltage is being measured, the Voltmeter Gate performs functions similar to the Frequency Gate. To make a voltage measurement, the Controller issues *esd*=7E0 to the Instrument Bus. This puts a high on both inputs of NAND gate U4A. The low at the output of U4A enables the Voltmeter Gate U19C. (Mode Select flip-flop U29B had previously been set.) At this point the Stop Count(H) line from the Voltage-to-Time Converter is low. Thus the 2 MHz clock (Φ) signal is gated into the counter via the Stop Count and Voltmeter Gates. After an interval determined by the dc voltage at the input to the Voltage-to-Time Converter, Stop Count(H) goes high which disables the clock signal. The accumulated count is, then, a function of the dc voltage.

Cycle Counter

The Cycle Counter has two stages (U15 and U14B) which form a divide-by-32. The input to the counter, when enabled, is FMUX, the signal from the input or Oscillator. The counter is enabled and disabled by the same signal that enables and disables the Frequency Gate; it is cleared at the same time as the Clock Counter. Carries from the Cycle Counter are output to Instrument Bus line d3(L) via U17B and are counted by the Controller. U17B is enabled at the same time as U17D.

Counter Output Gating

To read back the outputs of the Clock and Cycle Counters after completion of a count sequence, the Controller issues *esd*=7D0 to the Instrument Bus. The output of U4D (which had been low) goes high and enables Counter Output Gates U7B, U7D, U17C, and U17A. The outputs of U15 are inverted and placed on the readback data

lines of the Instrument Bus. Next, the Controller issues *esd*=7C0 to the Instrument Bus. U3C goes low. This causes U15 to be loaded with the output of U14 and also enables the Counter Output Gates since the output of U4D is high. The output of U15 is thus placed on the Instrument Bus through U14. In a similar manner the Controller issues *esd*=7B0 and *esd*=7A0 to copy the outputs of U1 and U2 into the subsequent stages and onto the Instrument Bus.

Select Decoder

For a general discussion of operation and decoding of the Instrument Bus, see *Instrument Bus*, Service Sheet BD4. For a discussion of the readback operation, see *Direct Control Special Functions*, paragraph 8-22.

TROUBLESHOOTING

General

Procedures for checking the Controller/Counter Assembly are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. The A8 Controller/Counter Assembly must be extended using the extender board (HP 08903-60018).

CAUTION

MOS and CMOS ICs can be damaged by static charges and circuit transients. Do not remove this assembly from the instrument while power is applied. Discharge the board and replacement IC to the same potential. (Use a conductive foam pad such as HP 4208-0094.) When unplugging ICs, place the board on a conductive pad. When the IC is unplugged, insert it into the pad also.

Several ICs on this assembly are held in high-grip sockets. Both the socket and the device can be damaged if an attempt is made to remove the device with an IC extraction tool. The recommended procedure is to first ground the tip of a small blade-type screwdriver, then slide the tip between the IC and slowly pry up the IC one pair of pins at a time.

Equipment

Digital Test/Extender Board ..... HP 08903-60018
Signature Analyzer ..... HP 5005A

⟨√1⟩ Counter Check

1. Set LINE to OFF. Extend the A8 Controller/Counter Assembly using the digital test/extender board (HP 08903-60018).

NOTE

It is not necessary to place the A7 Latch Assembly on extender boards for this procedure.

2. Interconnect the Controller/Counter Assembly, the Latch Assembly, the extender board, and the signature analyzer as shown in Figure 8D-6. Set the switches on the digital test/extender board to the OPEN position.

3. Unplug assemblies A2 through A6. (They do not need to be completely removed.)

4. Set the signature analyzer's start, stop, and clock to trigger follows:

Start ..... Falling Edge
Stop ..... Falling Edge
Clock ..... Rising Edge

5. Connect A8TP9 (TEST C) to A8TP3 (GND).

NOTE

Disregard the front-panel indications when performing signature analysis.

6. Set LINE switch to ON. Verify that Test LEDs A, B, and D on the A8 Counter/Controller Assembly light and remain lit.

7. Remove the ground from A8TP9. Verify that Test LED C lights and remains lit.

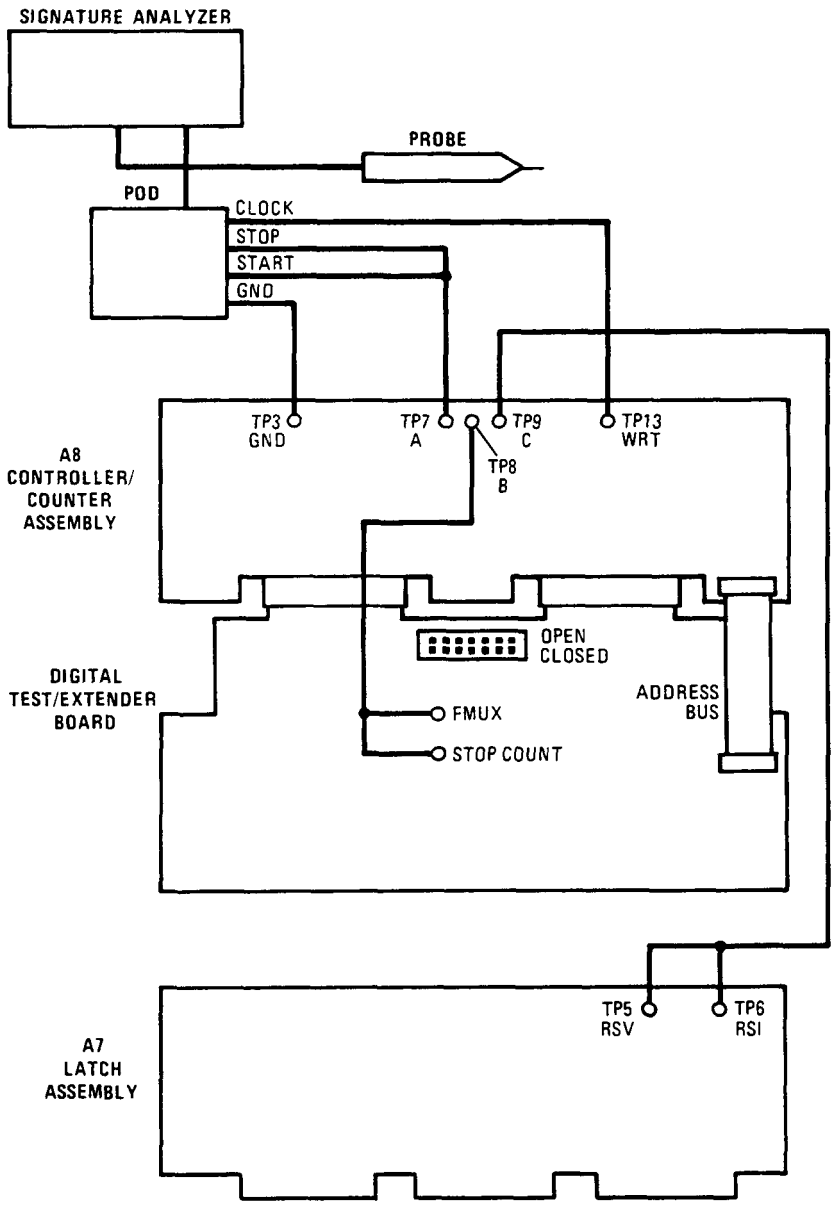


Figure 8D-6. Controller/Counter Assembly Troubleshooting Setup, ⟨J1⟩ Step 2

Table 8D-18. Signatures for ⟨√1⟩ Step 8

Description	Location	Signature
+5V	A8TP16 (+5V)	4824
d0(L)	A8U7 pin 6	1UU1
d1(L)	A8U7 pin 11	8FPH
d2(L)	A8U17 pin 8	13C1
d3(L)	A8U17 pin 3	3494

8. Check the points in Table 8D-18 with the signature analyzer probe.

Hint: If a data line is suspected (for example, if the signature for d2(L) only is faulty), the line itself may be faulty; see the CPU I/O Port Check on Service Sheet BD4. Otherwise, continue with step 9. If no signatures are faulty, perform the Counter Input Check on Service Sheet 13.

9. Remove A8U7 and A8U17 from their sockets.

CAUTION

The IC sockets are a high-grip type. Their lifetime is limited to only a few insertions. Use caution when removing or inserting ICs to avoid damage to the socket or IC.

10. Check the points in Table 8D-19 with the signature analyzer probe (the pin numbers for A8U7 and A17U17 are the socket pin numbers).

Table 8D-19. Signatures for ⟨√1⟩ Step 10

Description	Location	Signature
+5V	A8TP16 (+5V)	4824
d0(L)	A8U7 pin 6	104H
d1(L)	A8U7 pin 11	581P
d2(L)	A8U17 pin 8	UA92
d3(L)	A8U17 pin 3	581P

Hint: If faulty, the problem is with the data line itself; see the CPU I/O Port Check on Service Sheet BD4.

11. Check the points in Table 8D-20 with the signature analyzer probe.

12. Plug in A8U17. Check the pins on A8U17 with the signature analyzer probe as indicated in Table 8D-21.

Hint: A faulty signature indicates a fault in A8U17. If none of the signatures is faulty, A8U7 is probably faulty.

Hint: If the counter is operating properly, only three signatures are different with A8U7 and A8U17 installed. The signatures that differ from Table 8D-21 are:

1. U4, pin 1 is 1UU1 instead of 104H.
2. U20, pin 5 is 57H5 instead of 5869.
3. U20, pin 6 is 1UU1 instead of 104H.

Table 8D-20. Signatures for ⟨J1⟩ Step 11

Pin	U1	U2	U3	U4	U14	U15	U19	U20	U21	U29	Pin
1	U282	4824	5543	104H	8PU6	PF02	4824*	1H67	600A	4824	1
2	A885	A25C	0000*	5A9U	FFC1	1247	4824*	5543	9CU7	P522	2
3	A25C	–	0000*	P522	A1F9	4HF1	0000*	5543	7PAA	5543	3
4	F119	–	U282	12CC	6412	2PCA	U93H	1H67	PH3H	5AF7	4
5	U5U1	F119	3450	12CC	5A7H	HA42	C7A5	5869	0000	C119	5
6	U5U1	F119	8PU6	5A9U	6412	HA42	4824*	104H	35F6	U93H	6
7	0000	0000	0000	0000	0000	0000	0000	0000	5AF7	0000	7
8	42C1	0000*	PF02	–	A8P9	PF85	4824*	5543	0000	C7A5	8
9	A1F9	PUP6	8PU6	–	2PCA	4CPU	0000*	1H67	12CC	UU81	9
10	PUP6	–	2AH0	–	U5U1	FFC1	UU81	5543	PCP3	2F7H	10
11	42C1	–	PF85	07P1	A885	5A7H	AH06	1H67	2AH0	0000	11
12	6412	42C1	U93H	PF02	4HF1	A8P9	0000*	AH06	3450	–	12
13	5AF7	5AF7	5543	PCP3	5AF7	5AF7	4824*	P522	U282	385U	13
14	4824	4824	4824	4824	4824	4824	4824	4824	2F7H	4824	14
15									385U		15
16									4824		16

* Flashing light on test probe.
Note: The signature for a high or +5V is 48824. The signature for a low or ground is 0000. The "–" indicates that there is no valid signature for the pin. A blank indicates no pin on the IC.

Table 8D-21. Signatures on A8U17, ⟨J1⟩ Step 12

Pin	U17	Pin	U17
1	07P1	8	13C1
2	A8P9	9	07P1
3	3494	10	1247
4	5A9U	11	13C1
5	5A7H	12	4HF1
6	3494	13	5A9U
7	0000	14	4824

Note: The signature for a high or +5V is 4824. The signature for a low or ground is 0000.

SERVICE SHEET 15—A8 Controller/Counter Assembly (Controller)

PRINCIPLES OF OPERATION

General

The Controller/Counter Assembly (A8) controls the entire automated portion of the operation of the instrument. The Controller consists of a Microprocessor, ROMs, a RAM, and input/output (I/O) circuits. The Microprocessor, RAM, and I/O circuits are shown on Service Sheet 15, the ROMs on Service Sheet 16. For a general discussion of how the Controller and the Instrument Bus control the operations of the instrument, see *Principles of Operation* for Service Sheet BD4. **Serial Prefix 2652A and Above**: ROMs 1–9 have been consolidated into one ROM (ROM 10), which is located on SS15.

Microprocessor

The Microprocessor is divided into two ICs, the Central Processing Unit (CPU) and the Static Memory Interface (SMI). In addition a third IC, the Peripheral Input/Output (PIO) located on the Remote Interface Assembly (Service Sheet 19), is considered a part of the Microprocessor. The PIO is used when it is necessary to interface the CPU with the HP-IB. The CPU (U5) is an eight-bit parallel processor. Crystal Y1 and capacitors C25, C26, and C27 determine the frequency (2 MHz) of the CPU's internal clock. This clock also serves as the time base reference for the Counter. The CPU inputs and outputs are described in Table 8D-22.

Table 8D-22. Inputs and Outputs of the CPU (U5)

Pin Name	Description	Type
I/O00 thru I/O07	I/O Port Zero	Input/Output
I/O10 thru I/O17	I/O Port One	Input/Output
DB0 thru DB7	Data Bus Lines	Bi-directional (3-state)
ROMC0 thru ROMC4	Control Lines	Output
Φ, WRITE	Clock Lines	Output
EXT RES	External Reset	Input
INT REQ	Interrupt Request	Input
ICB	Interrupt Control Bit	Output
RC	RC Network	Input
XTLX	Crystal Clock Line	Output
XTLY	External Clock Line	Input

The SMI provides most of the interface logic needed to address up to 65 536 bytes of memory in the microprocessor system. In response to control signals from the CPU, the SMI generates the address and control signals needed by the memory devices. The SMI inputs and outputs are described in Table 8D-23.

Table 8D-23. Inputs and Outputs of the SMI (U6)

Pin Name	Description	Type
DB0 thru DB7	Data Bus Lines	Bi-Directional (3-state)
ADDR0 thru ADDR15	Address Lines	Output
ROMC0 thru ROMC4	Control Lines	Input
Φ, WRITE	Clock Lines	Input
INT REQ	Interrupt Request	Output
PRI IN	Priority In Line	Input
RAM WRITE	Write Line	Output
EXT INT	External Interrupt Line	Input
REGDR	Register Drive Line	Input/Output
CPU READ	CPU Read Line	Output

The PIO provides most of the interface logic needed to interface the CPU with the HP-IB. The PIO is described in Service Sheet 19.

Memory

The instrument's memory consists of nine 2048-bit ROMs, a RAM, and some small memory capability within the CPU itself. The RAM is the CPU External Register (U30) and is a 256-address, four-bit scratch pad memory used to read and write four bits (DB0-DB3) to and from the CPU. The Memory Select Decoder (U24) controls which memory IC on the Controller Assembly is enabled. Address line 15 enables the RAM.
Serial Prefix 2652A and Above: The instrument's memory consists of one 256K ROM, a RAM, and some small memory capability within the CPU itself.

To illustrate how a ROM address is accessed for data, assume that the CPU wants to read information from address 255 of ROM 3 (U10). First, the CPU places the necessary information on the ROM Control (ROMC) and the data lines of the Control Bus. The SMI decodes this information from the CPU and outputs the required address information on lines A0(H) through A15(H) and then sets CPU READ(H) high. CPU READ(H) is inverted by U23E and pulls one of the enable inputs low on each ROM and the RAM.

Serial Prefix 2652A and Above: To illustrate how a ROM address is accessed for Data, assume that the CPU wants to read information from a location in the ROM. First, the CPU places the necessary information on the ROM Control (ROMC) and the Data lines of the control Bus. The SMI decodes this information from the CPU and outputs the required address information on lines AO (H) through A15 (H), then sets CPU Read (H) high. CPU Read (H) is inverted by U23E and pulls the Enable line (Pin 22) low on the ROM. The data from that location in ROM is then placed on Data Lines DBO (H) through DB7 (H). The RAM Read and Write functions are similiar to the ROM function. Address lines A13 (H) through A15 (H) are decoded by Address Decoder U34 to enable U30.

Note that this is a read operation and the RAM WRITE(L) line from the SMI is high. Of address lines A11(H) through A15(H), only A12(H) will be high. Memory Select Decoder U24 decodes lines A11(H) through A14(H). Since only line A12(H) is high, output 2—ROM3(L)—of U24 goes low. Since A15(H) is low, the RAM (U30) is not enabled (A15(H) is inverted by U23F). Since CPU READ(L) and ROM3(L) are both low, ROM3 (U10) is enabled.

Since A0(H) through A7(H) are high and A8(H) through A10(H) are low, the data at address 255 is read out of the ROM. The eight bits of information are placed on lines DB0(H) through DB7(H). This information is then read into the CPU (U5).

The RAM read and write functions are similar to the ROM function. The CPU READ(H) and RAM WRITE(L) lines are used to determine which function of the CPU External Register (U30) is activated. Address line A15(H) is used to enable U30.

TEST LEDs and Test Points

The TEST LEDS DS1 through DS4 are controlled by the CPU as described in *Controller Test LEDs and Test Points*, paragraph 8-28. The test points (TP7 through TP10) are used to modify the power-up routine and are also used when performing signature analysis.
Serial Prefix 2652A and Above: Instruments with this serial break have the test points located on a single row connector.

Select and Data Buffers

The Select and Data Buffers (U16 and U23) invert and buffer the I/O 00 through I/O 07 input/output lines from the CPU to the Instrument Bus. For a general discussion of the Instrument Bus, see Service Sheet BD4. In addition, data lines d0(L) through d3(L) are input to the CPU from the Instrument Bus.

Enable Decoder

The Enable Decoder (U22) decodes the e0(H) through e3(H) lines from the CPU into the eight individual enable lines e=0(L) through e=7(L). These are distributed through several assemblies of the instrument to enable the desired select decoder.

Power On Reset

The Power On Reset circuit (Q1 and associated components) applies a momentary low on the EXT RES line of the CPU when power is applied to the instrument. When EXT RES is pulled low and then released, a program originating at memory address 0 is executed.

TROUBLESHOOTING

General

Procedures for checking the Controller/Counter Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Extend the board assembly where necessary to make measurements.

CAUTION

MOS and CMOS ICs can be damaged by static charges and circuit transients. Do not remove this assembly from the instrument while power is applied. Discharge the board and replacement IC to the same potential. (Use a conductive foam pad such as HP 4208-0094.) When unplugging ICs, place the board on a conductive pad. When the IC is unplugged, insert it into the pad also.

Several ICs on this assembly are held in high-grip sockets. Both the socket and the device can be damaged if an attempt is made to remove the device with an IC extraction tool. The recommended procedure is to first ground the tip of a small blade-type screwdriver, then slide the tip between the IC and the socket and slowly pry up the IC one pair of pins at a time.

If the Audio Analyzer powers up correctly, it is a strong indication that the Controller circuits are operating properly. In most cases, the two most common indications of a Controller fault are that the instrument fails to complete even the first phase of the power-up routine or that it behaves very erratically. However, be very careful about assuming a Controller failure when the instrument behaves erratically. Because of the close interrelationship of the circuit components, the data feedback loops, and the software, a failure that is occuring in one section of the instrument can affect other areas. For example, many types of malfunctions will prevent the Audio Analyzer from tuning properly.

In addition, keep the following points in mind when troubleshooting the Controller:

1. It is important to understand the structure of the Controller's buses. Data on these buses is often unstable or meaningless because of multiplexing, switching transients, and open-collector circuits. These conditions cause no problems for the Controller itself since it is synchronous and knows when the bus lines contain stable signals. (This is also true for the signature analyzer.) However, this is not true of other instruments testing the Controller such as a logic probe or oscilloscope. These test instruments, though, can still be used to examine qualitative factors such as general activity, logic levels, waveform timing, and bus conflicts.

2. Since bus structures also make it possible for many devices to be connected together on a single node, finding the one bad device on such a node can be difficult. A current tracer is useful for this purpose.

3. The Controller is a sequential processor. Program flow depends on a long sequence of instructions and events. If even a single bit of information is incorrect, the entire sequence can be changed. Bad memory bits are the most common source of single-bit errors.

4. The proper operation of the clock circuits is critical.

5. An improper reset can cause the Controller to appear to be running, but it may be incorrectly initialized or running the wrong sequence of software.

6. Interrupts are edge triggered. A stuck interrupt will interrupt once and then never again. An intermittent interrupt will keep interrupting. When the Controller is interrupted, the measurement is aborted, and the complete measurement cycle restarts at the beginning. Therefore, if the intermittent interrupt occurs frequently, it will completely prevent the instrument from operating.

TROUBLESHOOTING—SERVICE SHEET 15

Equipment

Digital Test/Extender Board ..... HP 08903-60018
Signature Analyzer ..... HP 5005A

Serial Prefix 2450A to 2614A

⟨J1⟩ Memory Select Decoders and ROM Check

NOTE

This check is a continuation of the Controller Kernel Check of Service Sheet BD4.

1. Switch LINE to OFF. Remove A8U30 (CPU External Register—RAM) from its socket. Extend the A8 Controller/Counter Assembly with the Digital Test/Extender Board. Connect the ribbon cable on the extender board to the empty socket A8J1 (ADR BUS). Switch LINE to ON.

2. Short A8TP4 (RES) to A8TP3 (GND). (Keep this jumper on for all subsequent tests.) Set the switches labeled ROMC on the extender board to CLOSED.

3. On the A8 Controller/Counter Assembly, connect the signature analyzer clipleads as follows:

Clock ..... A8TP13 (WRT)
Ground ..... A8TP3 (GND)

On the extender board, connect the signature analyzer clipleads as follows:

Start ..... ADDRESS 15
Stop ..... ADDRESS 15

4. Set the signature analyzer's start, stop, and clock to trigger as follows:

Start ..... Falling Edge
Stop ..... Rising Edge
Clock ..... Rising Edge

5. Check the pins listed in Table 8D-24 with the signature analyzer probe.

Table 8D-24. Signatures on A8U24, ⟨J1⟩ Step 5

Selected ROM	Pin on U24	Signature	Selected ROM	Pin on U24	Signature
1	1	4CP2	6	6	2F25
2	2	U1U2	7	7	F615
3	3	P352	8	9	6F7P
4	4	340A	9	10	048A
5	5	8UH9			

Hint: If faulty, check U24 and its output lines.

6. Connect the signature analyzer start and stop to the pin on U24 listed in Table 8D-25. Then check the indicated CONTROL BUS test points on the extender board with the signature analyzer probe.

TROUBLESHOOTING—SERVICE SHEET 15

NOTE

The signatures in Table 8D-25 are valid only for the ROMs with the part number listed in Table 8D-26. Consult the Manual Updates packet for signatures corresponding to ROMs with other part numbers.

Table 8D-25. Control Bus Test Point Signatures, √1 Step 6

ROM	Start/Stop to Pin on U24	Signature on CONTROL BUS DATA Test Point							
		0	1	2	3	4	5	6	7
1	1	18C9	305A	09PH	A9AP	P14P	1U96	PPH8	PC3C
2	2	PUC0	5641	4065	U966	2CF8	255F	F8CP	17PF
3	3	82U3	A0A4	44A6	F2FU	6348	7137	UHPH	95C5
4	4	5066	F387	C042	0H72	2494	8562	CFA1	7PPP
5	5	2HP5	A123	80AP	UP9H	8A56	321A	H482	924P
6	6	0439	6AC2	HHU2	A8H1	6858	962A	045F	P643
7	7	76CF	6533	U7U9	58A3	24HA	8H64	384C	36A0
8	9	8P2P	58U5	9337	PU72	6P3U	0813	3454	7C1F
9	10	F5FP	62AP	FHU8	CCPU	HA27	85P6	UA82	2H35

*Table 8D-26. Valid ROM Part Numbers**

ROM Number	Part Number	ROM Number	Part Number
1	08903-80016	6	08903-80021
2	08903-80017	7	08903-80022
3	08903-80018	8	08903-80023
4	08903-80019	9	08903-80024
5	08903-80020		

* Valid software date 11.15 1984.

Hint: A faulty signature indicates a faulty ROM.

Serial Prefix 2652A and above:

√1 Memory Select Decoders and ROM Check

This step is not valid for instruments with prefixes of 2652A and above.

√2 Enable Decoder Check

1. Key in the Direct Control Special Functions indicated in Table 8D-27. For each setting, check the pins on U22 indicated.

Hint: If "enable=2" is bad, these special functions cannot be keyed into the instrument (perform the *Front-Panel Keys and Scanners Check—Using Signature Analysis* on Service Sheet 17).

⟨√3⟩ Select and Data Buffers Check

1. Key in the Direct Control Special Functions indicated in Tables 8D-28 and 8D-29. For each setting, check the pins indicated.

Table 8D-28. Levels at A8U23, ⟨√3⟩ Step 1

Direct Control Special Function	Level (TTL) at U23 Pin							
	9	8	5	6	3	4	1	2
0.000	H	L	H	L	H	L	H	L
0.0FF	L	H	L	H	L	H	L	H

Table 8D-29. Levels at A8U16, ⟨√3⟩ Step 1

Direct Control Special Function	Level (TTL) at U16 Pin							
	12	11	9	8	1	3	5	6
0.000	H	L	H	L	H	L	H	L
0.0FF	L	H	L	H	L	H	L	H

SERVICE SHEET 16---A8 Controller/Counter Assembly (Read Only Memory)

PRINCIPLES OF OPERATION

The read-only memory (ROM) circuits are included in the *Principles of Operation* for Service Sheet 15.

TROUBLESHOOTING

Procedures for checking the ROMs are given in the *Memory Select Decoders and ROM Check* on Service Sheet 15.

SERVICE SHEET 17---A1 Keyboard and Display Assembly (Keyboard)

PRINCIPLES OF OPERATION

NOTE

The following discussion requires an understanding of the operation of the Instrument Bus (see Instrument Bus, *Service Sheet BD4) and of the Instrument Bus readback (see* Direct Control Special Functions, *paragraph 8-22).*

General

The Keyboard and Display Assembly (A1) interrupts the Controller when a key has been pressed and provides the circuitry that enables the Controller to determine which key was pressed.

Keystroke Detector

The Keystroke Detector pulses the External Interrupt line low when a key is pressed. When no key is down (that is, key switches S1 through S41 open), the inverting (−) input to U22B is pulled low by R6C and R6D. The outputs of the Key Row Scanner U30 are normally in the high or off state (the outputs are open-collector). The non-inverting (+) input of U22B is biased at approximately +1.4V. Thus for the condition when no key is pressed, the output of U22B is high, the output of U22A is low, and the output of U23A is high (that is, no interrupt; see Service Sheet 15).

Pressing any key (for example, the SINAD key S20) pulls the inverting input of U22B above +1.4V (via R5G and R2E for the SINAD key). This causes U23A to go low and creates a Controller interrupt. U22B has an open-collector output. When U22B goes low, C3 is rapidly discharged to produce a low on the input to U22A. However, when U22B goes high, C3 can only charge via R9. This action holds the input to U22A low for at least 50 ms regardless of key bounce. R11 adds hysteresis to U22A to improve noise immunity and shorten the transition time of the input to U23A.

Key Scanner and Front-Panel Keys

When the Controller receives an interrupt, it immediately initiates a key scan routine. The scan must identify the pressed key before the key has been released even in the presence of key bounce. Consider the example of pressing the SINAD key (S20). The scan begins by the Controller issuing *esd*=2F0 to the Instrument Bus. This puts an active low on pin 4 of demultiplexer U30. More specifically, *e*=2 and *s*=F. Both 0 and 1 inputs are high since *s*0=1 and *s*1=1. A 3 is demultiplexed. The 4 input is enabled since *s*2=1; the 5 input is disabled. e=2(L) is low and enables input G4. (Input G5 is not enabled because input 5 is not enabled.) Thus only the 3 output of the lower half of the demultiplexer (U30), enabled by input 4, is low.

The same Instrument Bus code enables the readback gates U24A, U25A, U24B, and U25B but not U24D, U25D, U24C, and U25C. Specifically, *s*3=1. Thus, the input to U23C is high. The two inputs to U23D are low. The NAND gates U24A, U25A, U24B, and U25B are enabled and function as inverters. U23B is low and the outputs of the NAND gates U24D, U25D, U24C, and U25C are high, that is, off. The Controller reads back the data (*d*) lines and scans the data giving priority to the highest number decoded. Since all columns are held high by pull-up resistors, the Controller reads *d*=F. The SINAD key has no effect because the output at pin 7 of U30 is off at this time.

The Controller next issues *esd*=2E0. Pin 5 of U30 is now low. U24A, U25A, U24B, and U25B are still enabled and U24D, U25D, U24C, and U25C are still disabled. *d*=F is read back. The sequence then continues with the issuance of *esd*=2D0 and 2C0 with the result that *d*=F is read back each time until *esd*=2C0 when *d*=B will be read back; that is, *d*2=0 (d2(L) is high). The Controller has now learned that the SINAD key was pressed.

If no key had been found in the first four columns, the sequence continues until the issuance of *esd*=270. With this code, the s3(H) input to U23B and U23C goes low. Now U24A, U25A, U24B, and U25B are disabled, and U24D, U25D, U24C, and U25C are enabled. The Controller now starts reading the data lines from U24D, U25D, U24C, and U25C to determine if one of the keys in the second four columns is closed.

If no key was found (that is, d=F always) due to key bounce, the scan repeats until 50 ms have elapsed and then the instrument reverts back to its previous mode of operation. Whether the key was found or not, the measurement cycle that was interrupted is aborted and a new software cycle is initiated.

Key-Light Circuits

The key-light circuits are discussed on Service Sheet 18.

TROUBLESHOOTING

General

Procedures for checking the Keyboard and Display Assembly are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. In addition, any points outside the labeled circuit area that must be checked are identified. Fixed signals are shown on the schematic also inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Remove the front-panel assembly to gain access to the circuit side of the keyboard. Note that the troubleshooting for the Enable Code e=0 Select Decoders (U29 and U29) shown on this service sheet is covered on Service Sheet 18.

Equipment

Digital Test/Extender Board ..... HP 08903-60018
Oscilloscope ..... HP 1740A
Signal Analyzer ..... HP 5005A
Voltmeter ..... HP 3455A

⟨✓1⟩ Keystroke Detector Check

1. Press any key and observe Test LED C on the A8 Controller/Counter Assembly. Each time the key is pressed the LED should toggle, that is, change state. If it does, the Controller is being properly interrupted.

2. Remove the ribbon cable W11.

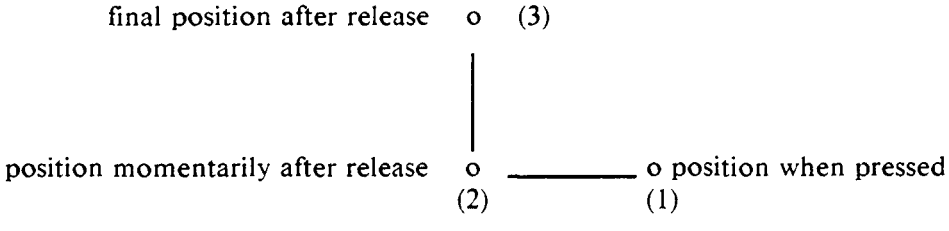
3. Check the voltages in Table 8D-30.

Table 8D-30. Keystroke Detector Check, ⟨✓1⟩ Step 3

Keys Down	Voltage Limits (Vdc) on A1U22				Level (TTL) at U23 Pin 1
	Pin 2	Pin 5	Pin 6	Pin 7	
None	−0.01 to 0.01	0.6 to 1.1	4.5 to 5.5	0 to 0.5	H
One	2.5 to 4.5	3.0 to 4.3	0 to 0.3	4.0 to 5.5	L

Hint: Any key should give the same voltage readings. The voltage at U22 pin 2 will be higher for the condition of one key down if more than one key is down.

4. Connect a high-impedance, dc coupled oscilloscope to U23 pin 1. Connect the oscilloscope's dc coupled external horizontal input to U22 pin 2. Press then release any key. The dot on the oscilloscope should move as follows:



Hint: The dot should dwell at the intermediate position (2) momentarily after release of the key for 40 to 60 ms.

⟨✓2⟩ Front-Panel Keys and Scanners Check---from Keyboard

NOTE

This check assumes proper operation of the following keys: Shift, SPCL, decimal, and all numeric. Otherwise, use ⟨✓3⟩ below which requires a signature analyzer. It also assumes that the Keystroke Detector works properly (see ⟨✓1⟩ above).

1. From Table 8D-31, determine the row of the key to be checked and enter the Direct Control Special Function for that row. (The display should now show 1111.0000.)

2. Disable keyboard interrupts by shorting A8TP3 (GND) to A8U6 pin 7 (EXT IN) on the A8 Controller/Counter Assembly. Extend the A8 Controller/Counter Assembly to make this connection.

3. Pressing any key in the appropriate row of Table 8D-31 should give the display shown. (No key down gives the display 1111.0000. Pressing a key not in the given row gives this display also.)

NOTE

To repeat step 1 above, it is first necessary to remove the jumper from A8TP3.

Table 8D-31. Front-Panel Keys and Scanners Check (Keyboard), ⟨✓1⟩ Step 1

Direct Control Special Function	Display vs. Key Pressed			
	0111.0000	1011.0000	1101.0000	1110.0000
0.250	(None)	(None)	⇑	⇓
0.260	×10	AMPTD INCR	−	AUTO OPERERATION
0.270		CLEAR	SPCL	dBV dB
0.280	(None)	LCL	LOG LIN	RATIO
0.290	SWEEP	PLOT LIMIT	FREQ INCR	÷
0.2A0	Hz mV	kHz V	STOP FREQ	START FREQ
0.2B0	(Right Filter)	30 kHz	80 kHz	(Left Filter)
0.2C0	DISTN	S	SINAD	AC LEVEL
0.2D0	AMPTD	FREQ	9	8
0.2E0	7	6	5	4
0.2F0	3	2	1	0

⟨✓3⟩ Front-Panel Keys and Scanners Check---Using Signature Analysis

1. Ground A8TP10 (TEST D) on the A8 Controller/Counter Assembly.

2. Connect signature analyzer start and stop to A8TP7 (TEST A). Connect signature analyzer clock to A8TP13 (WRT).

3. Set the signature analyzer's start, stop, and clock to trigger as follows:

Start ..... Falling Edge
Stop..... Falling Edge
Clock ..... Rising Edge

4. Set Audio Analyzer's LINE switch to OFF and back to ON. Disregard the front-panel display readouts.

5. Connect the signature analyzer's probe to A8TP8 (TEST B).

6. Press the front-panel keys and note the signature. The signatures are documented in Figure 8D-7.

Hint: Pressing keys simultaneously alters the signatures. If no meaningful results can be obtained, continue on with step 7.

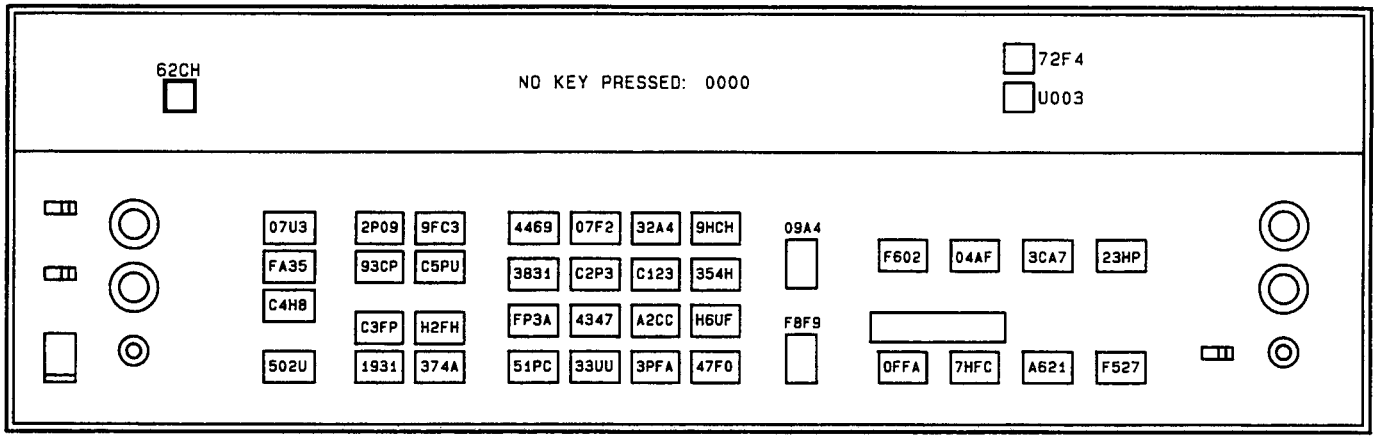


Figure 8D-7. Signatures for the Front-Panel Keys and Scanners Check, ⟨✓3⟩ Step 6

7. Connect the signature analyzer's probe to the points indicated in Table 8D-32 and check the signatures. (No keys should be pressed.)

Table 8D-32. Front-Panel Keys and Scanners Check (Signatures), ⟨✓3⟩ Step 7

Pin	U23	U24	U25	U30	Pin
1	938F	938F	938F	62AU	1
2	0000	U005	U005	7008	2
3	0000	7008	7008	1999	3
4	1381	938F	938F	0000	4
5	7008	U005	U005	0000	5
6	AA4P	7008	7008	0000	6
7	0000	0000	0000	0000	7
8	AA4P	7008	7008	0000	8
9	AA4P	1381	1381	0000	9
10	39F2	938F	938F	0000	10
11	39F2	7008	7008	0000	11
12	7008	1381	1381	0000	12
13	U005	938F	938F	7FC5	13
14	938F	938F	938F	7008	14
15				62AU	15
16				938F	16

Note: The signature for a high or +5V is 938F.
The signature for a low or ground is 0000.

⟨✓4⟩ Key Light Check

1. Key in the Direct Control Special Functions listed in Table 8D-33 to turn on the desired key light.

Table 8D-33. Key Light Check, ◇4◇ Step 1

Direct Control Special Function	Title
0.010	(Left Filter)
0.011	(Right Filter)
0.012	30 kHz
0.013	80 kHz
0.014	AC LEVEL
0.015	SINAD
0.016	DISTN
0.017	S (Shift)

SERVICE SHEET 18—A1 Keyboard and Display Assembly (Display)

PRINCIPLES OF OPERATION

The Keyboard and Display Assembly (A1) contains the front-panel displays, decimal points, annunciators, and key lights and the decoders and latches that control them. Lighting of a display is accomplished by straightforward decoding of the Instrument Bus with one code sent out for each of the seven segments of the display. For example, to display the digit "3" in display U9, the Controller issues *esd*=031, 032, 033, 034, 03D, 03E, and 037 in succession. Register U18 decodes the Instrument Bus code and successively outputs and latches the data present on the Z9 input (that is, d3(H), the most significant bit of the *d* code) to its internal flip-flops. A low on an output of U18 turns on a segment, a high turns it off. Thus, a low appears on the output of flip-flops 1, 2, 3, 4, and 7 (corresponding to *esd*=031, 032, 033, 034, and 037) and turns on the LEDs in segments a, b, c, d, and g respectively in U9. A high appears on the output of flip-flops 5 and 6 (corresponding to *esd*=03D and 03E) and turns off segments e and f. This results in a "3" being displayed.

Lighting of the minus sign (segment g of U8), decimal points, annunciators, and key lights is similar. For example, to light the % annunciator, the Controller issues *esd*=0A3 to the Instrument Bus. This is decoded by register U13 which latches a low into its internal flip-flop 3. The low turns on DS16.

The select decoders and the circuits for lighting the key lights are shown on Service Sheet 17. For a discussion of the Instrument Bus, see the *Principles of Operation* for Service Sheet BD4.

For instruments with serial prefix 2742A and above, an LED is used to indicate which impedence the source has been selected to by the user (50 or 600 Ω). The LED is lit when the source impedence has been set to 50 Ω. The LED (A1DS20) is found on Service Sheet 17.

TROUBLESHOOTING

General

The procedure for checking the Keyboard and Display Assembly is given below. The circuits are set to a desired (static) state using Direct Control Special Functions, and then the logic levels are checked.

Equipment

Voltmeter ..... HP 3455A

⟨✓1⟩ Annunciator and Key Light Check

1. Key in the Direct Control Special Functions listed in Table 8D-34 to turn on the desired annunciator or key light.

Table 8D-34. Annunciator and Key Light Check, ⟨✓1⟩ Step 1

Direct Control Special Function	Title	Light Type
0.024	ADDRESSED	Annunciator
0.025	REMOTE	Annunciator
0.026	kHz	Annunciator
0.027	Hz	Annunciator
0.0A0	mV	Annunciator
0.0A1	V	Annunciator
0.0A2	dB	Annunciator
0.0A3	%	Annunciator
0.090	SPCL	Key Light
0.091	RATIO	Key Light
0.095	SWEEP	Key Light

Hint: With the exception of the ADDRESSED and REMOTE lights, the lights go off when a new Direct Control Special Function is entered. To turn off the ADDRESSED light enter 0.02C and to turn off the REMOTE light enter 0.02D.

⟨✓2⟩ Decimal Point Check

1. Key in the Direct Control Special Functions listed in Table 8D-35 to turn on the desired decimal point. The digit number is the number on the display window directly below the digit.

⟨✓3⟩ Display Check

1. Key in the Direct Control Special Functions listed in Table 8D-36 to turn on the desired digit segment in the desired position. The digit number is the number on the display window directly below the digit.

Table 8D-35. Decimal Point Check, ⟨✓2⟩ Step 1

Direct Control Special Function	Number of Following Digit
Left Display	
0.023	1
0.022	2
0.021	3
0.020	4
Right Display	
0.093	Upper Left Corner
0.0A7	5
0.0A6	6
0.0A5	7
0.0A4	8

Table 8D-36. Display Check, ⟨✓3⟩ Step 1

Digit Number	Direct Control Special Function	Digit Number	Direct Control Special Function
Left Display		**Right Display**	
Digit Before 1	0.0B*d*	Digit Before 5	0.092*
1	0.0C*d*	5	0.03*d*
2	0.0D*d*	6	0.04*d*
3	0.0E*d*	7	0.05*d*
4	0.0F*d*	8	0.06*d*
* *d*=2 only (g is the only segment controlled with this special function.)			

Segment Displayed*	*d*
(None)	0
a	1
b	2
c	3
d	4
e	5
f	6
g	7
* See schematic diagram for identification of segments a through g.	

SERVICE SHEET 19---A9 Remote Interface Assembly

PRINCIPLES OF OPERATION

General

The Remote Interface Assembly (A9) interfaces the Controller with the HP-IB. It performs the necessary handshake operation, interprets the HP-IB control lines, and is both an input and output peripheral to the Controller. The Remote Interface Assembly consists of three basic elements: the HP-IB I/O, the Handshake Logic, and the Interface Control circuits. In addition, other miscellaneous circuits are used on the assembly. The operation of the three basic elements is explained first. Then, a detailed explanation of how the bus controller (for example, a computing controller) addresses the instrument to talk or to listen is presented. The miscellaneous circuits are then briefly discussed. Table 8D-37 lists and identifies the mnemonics used in the Remote Interface and should be referred to while reading the principles of operation.

Table 8D-37. Mnemonics for Remote Interface

Mnemonic	Signal Name
AAD	Acceptor Accepted Data
ACD	Accepted Data
ADS	Addressed
AFC	Address Flip-Flop Clock
ARD	Accepted Received Data
ATL	Addressed to Listen
ATN	Attention
ATT	Addressed to Talk
AVD	Accept Valid Data
CLF	Clear Listen Flip-Flop
CTF	Clear Talk Flip-Flop
DAR	Disable ROM
DAV	Data Valid
DIO1	Data Input/Output 1
DIO8	Data Input/Output 8
DFC	Data Accepted Flip-Flop Clock
EAH	Enable Acceptor Handshake
EIC	Enable Interface Control
ENR	Enable ROM
EOI	End or Identify
ICP	Interrupt CPU

Mnemonic	Signal Name
IFC	Interface Clear
LAD	Listener Accepted Data
LRD	Listener Ready for Data
NDAC	Not Data Accepted
NRFD	Not Ready for Data
RAS	Read Address Selector
RAT	Read Addressing Type
RDR	Reset DAC/RFD
REN	Remote Enable
RFC	REN Flip-Flop Clock
RNL	REN Flip-Flop Latched
RSL	Read Switch Lower
RSU	Read Switch Upper
RTR	Ready to Receive
RVD	Receive Valid Data
SDA	Set Data Accepted
SDV	Set Data Valid
SLF	Set Listen Flip-Flop
SRQ	Service Request
STF	Set Talk Flip-Flop
UUA	Universal Unlisten Address

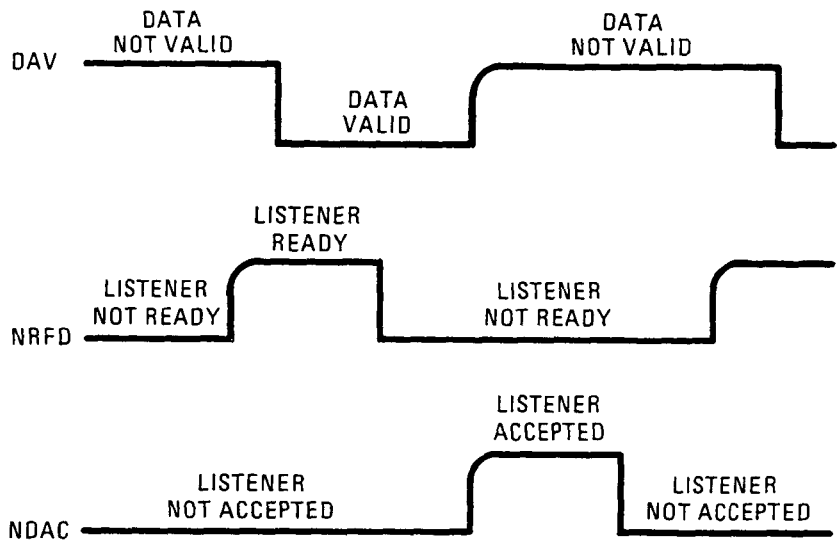
HP-IB I/O Circuits

The HP-IB I/O circuits provide bidirectional interface between the Remote Interface Assembly and the HP-IB. The circuit consists of U7, U8, U9, and U10. When the TALK(L) line is low, the interface is configured to send data to the HP-IB. In this state, U7 and U9 are disabled, and since they are open-collector devices, they are essentially out of the circuit. U8 and U10 provide a direct path from the Peripheral Input/Output (U18) to the HP-IB. When the TALK(L) line is high, the Remote Interface is configured to receive data from the HP-IB. In this mode, U7 and U9 are enabled, and the path through U8 and U10 is reversed. This allows data from the HP-IB to be applied to the Peripheral Input/Output (U18), the Address Decoder (U5), and the Interface Control ROM (U2). Depending upon the function being performed, this data is either sent to the Controller or used to decode the talk or listen address.

Handshake Logic Circuits

Information is communicated over the HP-IB by means of handshakes between instruments. It is assumed in this discussion that the reader is familiar with the use of the DAV, NDAC, and NRFD signals as they are used

on the HP-IB. (Figure 8D-8 illustrates the HP-IB handshake.) The instrument can operate as either a talker or a listener when so directed by the bus controller. The primary control circuits in the Handshake Logic are the DAC Flip-Flop (U3B) and gates U20A, U20B, and U15B.



Start with the talker waiting for the listener to release NRFD (not ready for data) indicating it is ready.

When the listener is ready, NRFD goes high (false). The talker then places valid data on DIO1 through DIO8 and sets DAV (data valid) low (true).

NRFD then goes low (true) and the talker waits for the listener to indicate it has accepted the data (or ignored it) by releasing the NDAC (not data accepted) to a high (false, i.e., data is accepted).

The talker sets DAV high (false) and again waits for the listener to release NRFD.

(NOTE that if ATN is true, all instruments on the bus must handshake regardless of whether they are talkers, listeners, or bystanders. Being in remote or local has nothing to do with handshaking.) If ATN is false, they only handshake if addressed.

Figure 8D-8. Simplified HP-IB Handshake Between a Talker and One Listener

When the instrument is a listener, the ATL(L) line is low, and the high output from U15B enables U20A and U20B. This condition is also true when ATN(L) goes low and is discussed in detail later. In either case, the DAC Flip-Flop (U3B) controls the handshake. If U3B is set, the RTR(L) line from the reset output is low, and the NRFD(L) line from U20B is high indicating that the instrument is ready to receive data. The ACD(L) line from the active-high output of U3B is high, and (since the other input to U20A is also high), the NDAC(L) line is low. When the bus controller sees all of the required NRFD(L) lines high (more than one instrument can be addressed to listen), it sets DAV(L) low. When DAV(L) goes low (indicating the data on the HP-IB is valid), the Interface Control ROM either sets EXT INT low or resets U3B by setting SDA(L) low, depending on whether or not the CPU must be interrupted. (See Table 8D-38 for a complete list of the Interface Control ROM input and output signals.) If the CPU is interrupted, it will reset U3B using the DFC(L) line. In either case, ACD(L) goes low and the NDAC(L) line from U20A goes high. When the bus controller sees all of NDAC(L) lines go high, it sets DAV(L) high. The DAV(L) signal is applied through gates U19B, U14B, and U13B to set the DAC Flip-Flop (U3B). Gates U14B and U13B are used to slow down the handshake and prevent a possible race condition. When the DAC Flip-Flop is set, the instrument is returned to a ready-for-data condition.

When the instrument is a talker, the output from U15B is low because both the ATL(L) and the ATN(L) lines are high. The low output from U15B disables U20A and U20B. This prevents the DAC Flip-Flop from driving

the NDAC(L) and NRFD(L) HP-IB lines. The Controller (A8) now reads the NDAC(L) line through U19C and U13C and the NRFD(L) line through U19D and U13D. Both of these signals are routed to the Controller through the Peripheral Input/Output (U18). The DAV(L) signal is driven by the Controller through U18 and U20C by the SDV(H) line. U20C is enabled by U14A when the TALK(L) line is low. In the talk mode, the handshaking is entirely controlled by the instrument's firmware and Controller.

Interface Control Circuits

The primary control element in the Interface Control circuits is the Interface Control ROM (U2). U2 is enabled when all the following conditions are satisfied:

1. RTR(L) is low. This indicates the instrument is ready to receive data or commands.

2. EAH(L) is low. This enables an acceptor handshake. It is decoded from the ATL and ATN lines by U14D. Therefore, if the instrument is addressed to listen or if attention is true, the gate is enabled.

3. U15C pin 8 is low. This indicates that the Controller (A8) has enabled the interface to receive data. This state is latched by the flip-flop consisting of U15C and U15D. This flip-flop is also used to disable the Interface Control ROM (U2) when the Remote Interface is preparing to talk. U2 is disabled so that its control circuits do not respond to the data that the instrument itself is sending.

4. AVD(L) is low. This indicates that the bus controller is asserting that the data on the HP-IB is valid by putting DAV(L) low.

When all of these conditions are true, U2 is enabled by setting the EIC(L) line from U14C low. The outputs of U2 are then dependent upon the decoded address line inputs. Depending upon the selected output, the Interface Control ROM will set or clear the appropriate flip-flops, complete a handshake, or interrupt the Controller. The 32 possible states of the output lines are listed and defined in Table 8D-38.

How the Remote Interface Handshakes with the HP-IB

The Remote Interface circuits control the asynchronous transfer of bytes over the HP-IB. The following three conditions require that the instrument complete the handshake requirements:

1. When it is a bystander.

2. When the ATN(L) line is low (true). For example, when the bus controller is addressing the instrument to set it to the talk or listen modes. There are also universal commands that can be sent when ATN(L) is low.

3. When it is already addressed to talk or listen.

The instrument handshakes as a bystander whenever ATN(L) is high and it is not addressed to listen. Actually, this handshake is not an interchange of information because under these conditions the instrument never pulls the NRFD(L) and NDAC(L) output lines low. These lines are held high because ATL(L) and the ATN(L) inputs to U15B remain high. ATL(L) remains high because the instrument is not currently addressed to listen. ATN(L) remains high because it is high at the HP-IB and the signal is applied through two inverters (U19E and U13A) to the input of U15B. The resulting low output is applied to U20A and U20B and the NRFD(L) and NDAC(L) lines are always high. In this mode, the Audio Analyzer is essentially "off the bus". Note that the DAC Flip-Flop (U3B) is also applied to these gates and depending upon its output state would also hold one of the gate outputs high if ATN were true or ATL were true.

When the bus controller wants to address the instrument to talk, ATN(L) is set low. The output of U15B goes high and the status of the NRFD(L) line (U20B) and the status of the NDAC(L) line are controlled by the DAC Flip-Flop (U3B). (The DAC Flip-Flop is already set by DAV(L) being high through U19B, U14B, and U13B.) This causes the RTR(L) line from the DAC Flip-Flop to set NRFD(L) high. The bus controller has already placed the instrument's talk address on the bus and it now pulls DAV(L) low indicating that it is valid data.

Since the instrument is not yet addressed to talk, the TALK(L) input to the HP-IB I/O circuits (U7, U8, U9, and U10) is high. The talk address on lines DIO1(L) through DIO5(L) is applied through U7 and U9 to the Address Decoder comparator U5. U5 compares the incoming address with the setting of the first five address switches (S1). If they are the instrument's correct address, the M=N output of U5 goes high. The data on DIO7(L) and

Table 8D-38. Inputs and Outputs of Interface Control ROM

Address						Data								Remarks**
Binary Bit Value						Bit								
16	8	4	2	1	Hex	7	6	5	4	3	2	1	0	
Pin Number						Pin Number								
14	13	12	11	10	x	9	7	6	5	4	3	2	1	
L	L	L	L	L	00	H	•	H	H	H	H	*	L	SCG so AHS only.
L	L	L	L	H	01	H	*	L	H	H	H	•	L	OTA so CTF and AHS.
L	L	L	H	L	02	H	•	H	H	H	H	*	L	OLA so AHS only.
L	L	L	H	H	03	L	*	H	H	H	H	*	H	UBC so INT only.
L	L	H	L	L	04	H	*	H	H	H	H	*	L	SCG so AHS only.
L	L	H	L	H	05	H	*	L	H	H	H	*	L	UNT so CTF and AHS.
L	L	H	H	L	06	H	•	H	H	L	H	•	L	UNL so CLF and AHS.
L	L	H	H	H	07	H	*	H	H	H	H	*	L	NRC so AHS only.
L	H	L	L	L	08	H	•	H	H	H	H	*	L	SCG so AHS only.
L	H	L	L	H	09	H	*	H	L	L	H	•	L	MTA so STF, CLF, and AHS.
L	H	L	H	L	0A	L	•	L	H	H	L	•	H	MLA so SLF, CTF, and AHS.
L	H	L	H	H	0B	L	•	H	H	H	H	•	H	UBC so INT only.
L	H	H	L	L	0C	H	•	H	H	H	H	*	L	SCG so AHS only.
L	H	H	L	H	0D	H	•	L	H	H	H	•	L	UNT so CTF and AHS.
L	H	H	H	L	0E	H	•	H	H	L	H	*	L	UNL so CLF and AHS.
L	H	H	H	H	0F	H	•	H	H	H	H	•	L	NRC so AHS only.
H	L	L	L	L	10	L	•	H	H	H	H	•	H	DATA so INT only.
H	L	L	L	H	11	L	•	H	H	H	H	•	H	DATA so INT only.
H	L	L	H	L	12	L	*	H	H	H	H	•	H	DATA so INT only.
H	L	L	H	H	13	H	•	H	H	H	H	•	L	CDATA so AHS only.
H	L	H	L	L	14	L	•	H	H	H	H	*	H	DATA so INT only.
H	L	H	L	H	15	L	*	H	H	H	H	•	H	DATA so INT only.
H	L	H	H	L	16	L	*	H	H	H	H	*	H	DATA so INT only.
H	L	H	H	H	17	H	*	H	H	H	H	*	L	CDATA so AHS only.
H	H	L	L	L	18	L	•	H	H	H	H	*	H	DATA so INT only.
H	H	L	L	H	19	L	•	H	H	H	H	•	H	DATA so INT only.
H	H	L	H	L	1A	L	*	H	H	H	H	*	H	DATA so INT only.
H	H	L	H	H	1B	H	*	H	H	H	H	•	L	CDATA so AHS only.
H	H	H	L	L	1C	L	*	H	H	H	H	*	H	DATA so INT only.
H	H	H	L	H	1D	L	•	H	H	H	H	*	H	DATA so INT only.
H	H	H	H	L	1E	L	•	H	H	H	H	•	H	DATA so INT only.
H	H	H	H	H	1F	H	*	H	H	H	H	*	L	CDATA so AHS only.

* Don't care condition.

** The outputs are active low. The functions of each output are:

Bit 7: INT, interrupts CPU.
Bit 6: Don't care (NC).
Bit 5: CTF, clear Talk Flip-Flop.
Bit 4: STF, set Talk Flip-Flop.
Bit 3: CLF, clear Listen Flip-Flop.
Bit 2: SLF, set Listen Flip-Flop.
Bit 1: Don't care (NC).
Bit 0: AHS, automatic handshake.

Mnemonics used:

CDATA: DATA from Control group
DATA: DATA (interface responds)
MLA: My Listen Address
MTA: My Talk Address
NRC: Non-Recognized Command
OLA: Other Listen Address
OTA: Other Talk Address
SCG: Secondary Command Group
UBC: Universal Bus Command
UNL: Un-Listen
UNT: Un-Talk

DIO6(L) is applied to the Interface Control ROM (U2) to determine whether the instrument is being addressed to talk or to listen. If it is being addressed to talk, DIO7(L) is low and DIO6(L) is high (that is, 10). If it is being addressed to listen, DIO7(L) is high and DIO6(L) is low (that is, 01). These two bits are the only difference between the DIO inputs from the bus controller to the instrument when it is being set to talk or listen.

The EIC(L) from U14C is low to enable U2 and the other inputs to the address lines of U2 select the memory locations that will set output pin 5 to low. The STF(L) line sets the Talk flip-flop U1A. At the same time, the SDA(L) output at pin 1 of U2 is low and resets the DAC Flip-Flop (U3B). The low output from pin 9 of U3B is applied to U20A and the NDAC(L) line goes high, indicating that the handshake is complete. Note that the CPU did not need to be interrupted.

Remote Enable Flip-Flop

When the instrument is addressed to listen, the CPU is interrupted and must determine whether or not it has been enabled to the remote mode (or whether it is already in the remote mode). The Controller does this by attempting to set the Remote Enable Flip-Flop (U3A). If the REN(L) line on the HP-IB is low (true), it is inverted by U19F and the reset input to U3A pin 1 is high. In this case U3A can be set by the Controller. Conversely, if REN(L) is high, the reset input is low and U3A is held reset. The Controller checks the set output of U3A RNL(H) through inverter U11A and the Peripheral Input/Output (U18). If the instrument receives its listen address and if the output of U3A is high, it enters remote mode and lights the REMOTE annunciator on the front panel.

Serial Poll Enable Flip-Flop

When the Controller recognizes the SPE (Serial Poll Enable) bus command, the CPU is interrupted and attempts to set the Serial Poll Flip-Flop (U12B). IFC(L) from the HP-IB is applied through U19A and U11D to the reset input of U12B. If IFC(L) is high, the Serial Poll Flip-Flop can be set; if it is low U12B is held reset. If U12B is set, the instrument enters the serial poll mode, and this information is read back via the Instrument Bus to the Controller through U4D. When the instrument is subsequently addressed to talk, it again reads back the output of U12B to determine what information to output to the HP-IB: measurement results or the status byte. If it is still in the serial poll mode, the status byte is output. When the SPD (Serial Poll Disable) bus command is received, the Controller resets U12B.

Other Control Lines

The remaining HP-IB control lines to the instrument are EOI(L), SRQ(L), and IFC(L). EOI(L) is not used by the instrument and is terminated in R6N and R6P. SRQ(L) is output to the HP-IB under Controller direction through U18. IFC(L) is used to clear all talkers and listeners off the HP-IB. IFC(L) is buffered into four lines. At the output of U19A, after CR1, one line is applies to the Address Comparator (U5) to disable it. This keeps the Interface Control ROM (U2) from affecting either the Talk or Listen Flip-Flop while IFC is true. Two additional lines (from U12E and U13F) clear the Talk and Listen Flip-Flops (U1A and U1B). The fourth line (from U11D) clears the Serial Poll Flip-Flop.

Address Readback Circuit

When so directed by the operator, the Controller sequentially reads back the status of the Address Switches (S1A through S1E) and the talk-only and listen-only switches (S1G and S1F). This information is processed through gates U4 and U17 under control of the RSU(L) and RSL(L) lines from the Select Decoder (U16). The Controller's internal RAM is also read for service request (SRQ) status. The front-panel display shows not only the HP-IB address and the talk-only or listen-only status, but also whether or not it is issuing a service request (SRQ). (See Special Functions 21.0 and 21.1 in the *Detailed Operating Information* in Section 3.)

Peripheral Input/Output

The Peripheral Input/Output (U18) provides the required I/O interface between the Controller and the HP-IB. Refer to Table 8D-39 for a description of inputs and outputs of U18.

Select Decoder

For a general discussion of instrument control, see *Latches (A7) and Instrument Bus* in the *Principles of Operation* for Service Sheet BD4.

Table 8D-39. Inputs and Outputs of the PIO (U18)

Pin Name	Description	Type
I/O A0 thru I/O A7	I/O Port A	Input/Output
I/O B0 thru I/O B7	I/O Port B	Input/Output
DB0 thru DB7	Data Bus Lines	Bi-Directional (3 state)
ROMC0 thru ROMC4	Control Lines	Input
Φ, WRITE	Clock Lines	Input
EXT INT	External Interrupt	Input
PRI IN	Priority In	Input
PRI OUT	Priority Out	Output
INT REQ	Interrupt Request	Output
DBDR	Data Bus Drive	Output

TROUBLESHOOTING

General

Procedures for checking the Remote Interface Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Extend the board assembly where necessary to make measurements.

CAUTION

MOS and CMOS ICs can be damaged by static charges and circuit transients. Do not remove this assembly from the instrument while power is applied. Discharge the board and replacement IC to the same potential. (Use a conductive foam pad such as HP 4208-0094.) When unplugging ICs, place the board on a conductive pad. When the IC is unplugged, insert it into the pad also.

Several ICs on this assembly are held in high-grip sockets. Both the socket and the device can be damaged if an attempt is made to remove the device with an IC extraction tool. The recommended procedure is to first ground the tip of a small blade-type screwdriver, then slide the tip between the IC and the socket and slowly pry up the IC one pair of pins at a time.

The following checks use the *HP-IB Functional Checks* in the Operating Section (refer to paragraph 3-11) as a basis for troubleshooting the Remote Interface Assembly. It is assumed in the following procedures that the failure was detected during the functional checks. Therefore, it is only necessary to perform the troubleshooting procedures starting with the equivalent functional check in which the failure occured. During the procedures, the 61.N Service Special Functions are also used to help locate the failure.

When using the troubleshooting flowcharts, it is important that the associated notes be read. These notes help clarify the steps that are flagged. The troubleshooting procedures assume that the bus controller and the bus controller's HP-IB interface are operating properly. Therefore, it is assumed that the required inputs are present at the interface to the Audio Analyzer. Always perform all of the HP-IB Functional Checks after any repair to the Remote Interface Assembly.

When using the flowcharts, refer to the principles of operation to clarify the sequence of troubleshooting. Refer to Figure 8D-8 for an explanation of the HP-IB handshake. If replacement of a probably defective part does not correct the Remote Interface problem, check any related circuits that are connected to the faulty area. For example, some bus controllers simultaneously function as both talker and listener. As a result, they may mask a failure of the Remote Interface handshaking capabilities. This can happen when either the NRFD or NDAC output driver on the bus fails in a high state. This type of failure is a very subtle problem. The quickest way to determine what is happening is to monitor the driver outputs while activating both output levels of the individual drivers.

Equipment

Digital Test/Extender Board	HP 08903-60018
Logic Probe	HP 5005A
Oscilloscope	HP 1740A

NOTE

The following are the notes for Figures 8D-9 through 8D-12.

1. The Run indicator shows the status of the handshake between the bus controller and the Audio Analyzer. If it is still on, the handshake was not completed.

2. This Special Function reads back and displays the present state of the Talk and Listen Flip-Flops. (See 61.N Display HP-IB Status *in paragraph 8-23.)*

3. This Special Function reads back and displays the present state of the ATN bus control line and the state of the Remote Enable Flip-Flop.

4. X equals "don't care".

5. If TP4 is low, the handshake logic has satisfied the initial requirements to input address data into the Interface Control ROM. If TP4 is high, this requirement is not complete.

6. Displays HP-IB address set on the Address Switches.

7. Remember that the checkout procedure assumes that the Audio Analyzer is set to address 28. If the instrument has been set for a different address, modify the HP-IB Functional Checks *procedure and the troubleshooting information to match the new address.*

8. Indicated IC is the most likely malfunction. However, if replacement does not fix the problem, check the circuits that drive or are driven by the specified IC and all wiring and components that are connected to the same signals.

9. See Figure 8D-8 for a simplified explanation of the HP-IB Handshake.

⟨√1⟩ Address Recognition Check

1. Perform the steps shown in the *Address Recognition Troubleshooting Flowchart,* Figure 8D-9.

⟨√2⟩ Remote and Local Messages and the LCL Key Check

1. Perform the steps shown in the *Remote and Local Messages and the LCL Key Troubleshooting Flowchart,* Figure 8D-10.

⟨√3⟩ Sending the Data Message Check

1. Perform the steps shown in the *Data Message Troubleshooting Flowchart,* Figure 8D-11.

⟨√4⟩ Receiving the Data Message Check

1. Perform the *Receiving the Data Message* portion of the *HP-IB Functional Checks.*

Hint: Most of the circuits that are used in this check were used in previous checks. Check the inputs and outputs of gates U8 and U10. if they are good, the problem could be U18 (PIO), the Controller (see Service Sheet 15), or the annunciators (see Service Sheet 18).

⟨√5⟩ Local Lockout and Clear Lockout/Set Local Messages Check

1. Perform the *Local Lockout and Clear Lockout/Set Local Messages* portion of the *HP-IB Functional Checks.*

Hint: Most of the circuits that are used in this check were used in previous checks. If the instrument fails this check, the problem is probably in the Controller (see Service Sheet 15) or the front-panel keyboard circuits (see Service Sheet 17).

⟨√6⟩ Clear Message Check

1. Perform the *Clear Message* portion of the *HP-IB Functional Checks.*

Hint: The circuits that are used in this check were used in previous checks. If a problem occurs during the check, repeat the previous checks starting at ⟨√1⟩ *Address Recognition Check.*

⟨√7⟩ Abort Message Check

1. Perform the *Abort Message* portion of the *HP-IB Functional Checks.*

Hint: Most of the circuits that are used in this check were used in previous checks. The flowchart (Figure 8D-12) is primarily used to check the IFC and serial-poll circuits.

⟨✓8⟩ Status Byte Message Check

1. Perform the *Status Byte Message* portion of the *HP-IB Functional Checks.*

Hint: Most of the circuits that are used in this check were used in previous checks. The most important difference is that the Controller must recognize that the Serial Poll Flip-Flop is set and send the status byte when addressed to talk.

⟨✓9⟩ Require Service Message

1. Perform the *Require Service Message* portion of the *HP-IB Functional Checks.*

Hint: Most of the circuits that are used in this check were used in previous checks. The most important difference is that the Controller must drive the SRQ(L) line low. It does this through gate U20D and the PIO (U18). Repeat the check and monitor the input and output of U20D.

⟨✓10⟩ Trigger Message and Clear Key Triggering

1. Perform the *Trigger Message and Clear Key Triggering* portion of the *HP-IB Funtional Checks.*

Hint: Most of the circuits that are used in this check were used in previous checks. The most important difference is that the Controller must recognize that the CLEAR key can be used to trigger the instrument. The problem is probably in the Controller (see Service Sheet 15) or the CLEAR key circuit (see Service Sheet 17).

⟨✓11⟩ Select Decoder and Address Switches Check

1. Key in the Direct Control Special Functions indicated in Table 8D-40. For each setting, check the pins on U16 indicated.

Table 8D-40. Select Decoder Outputs, ⟨✓11⟩ Step 1

Direct Control Special Function	Level (TTL) at U16 Pin							
	15	14	13	12	11	10	9	7
0.300	*	H	H	H	H	H	H	H
0.310	H	*	H	H	H	H	H	H
0.320	H	H	*	H	H	H	H	H
0.330	H	H	H	*	H	H	H	H
0.340	H	H	H	H	*	H	H	H
0.350	H	H	H	H	H	*	H	H
0.360	H	H	H	H	H	H	*	H
0.370	H	H	H	H	H	H	H	*

2. Key in 0.350 SPCL to read back part of S1. The left display should be of the form *abcd* where

a=1 if S1D is open;
b=1 if S1C is open;
c=1 if S1B is open;
d=1 if S1A is open.

3. Key in 0.360 SPCL to read back the rest of S1 and U12B. The left display should be of the form *abcd* where

a=1 if U12B is set;
b=1 if S1G is open;
c=1 if S1F is open;
d=1 if S1E is open.

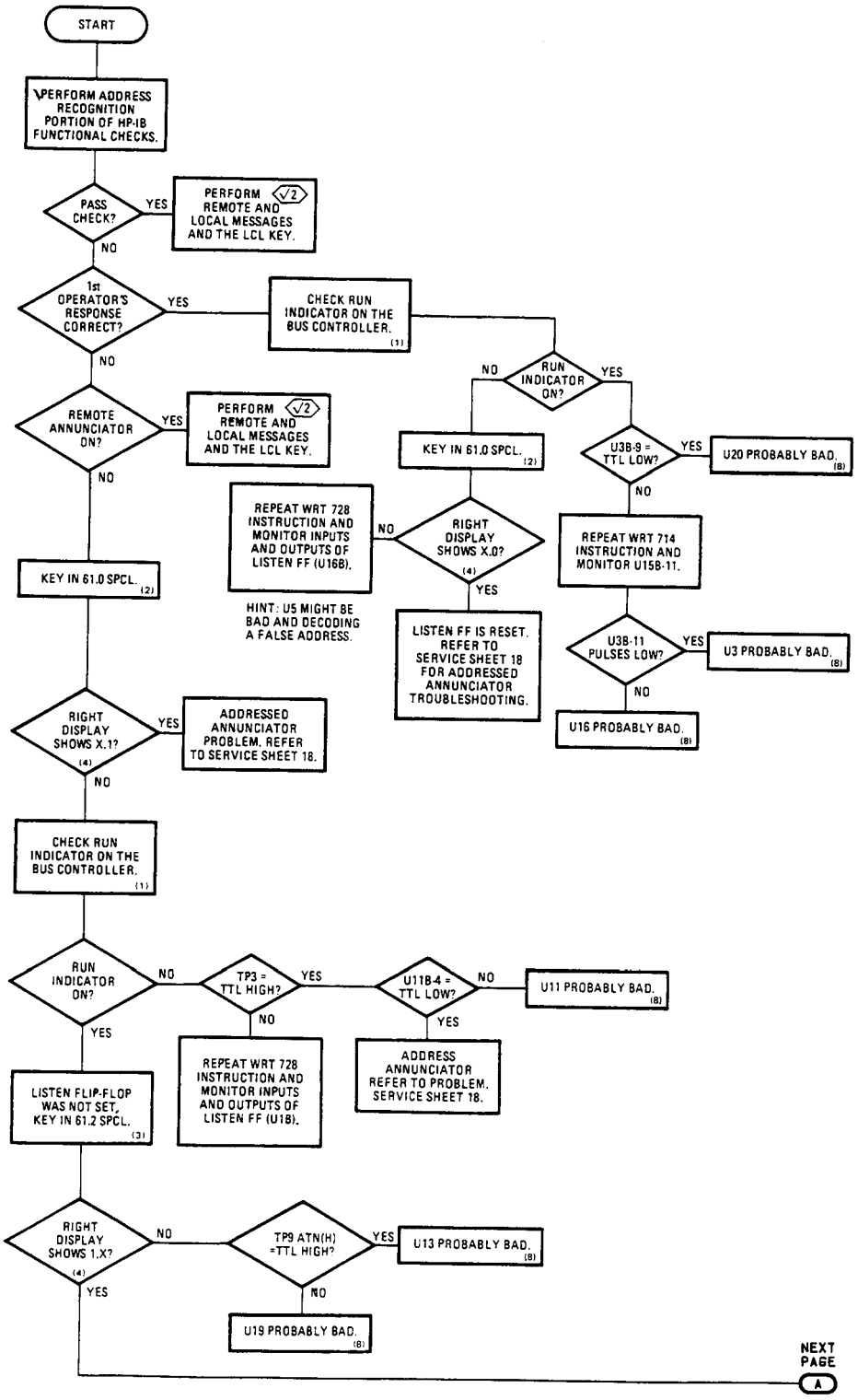


Figure 8D-9. Address Recognition Check Troubleshooting Flowchart, √1 (1 of 2)

TROUBLESHOOTING---SERVICE SHEET 19

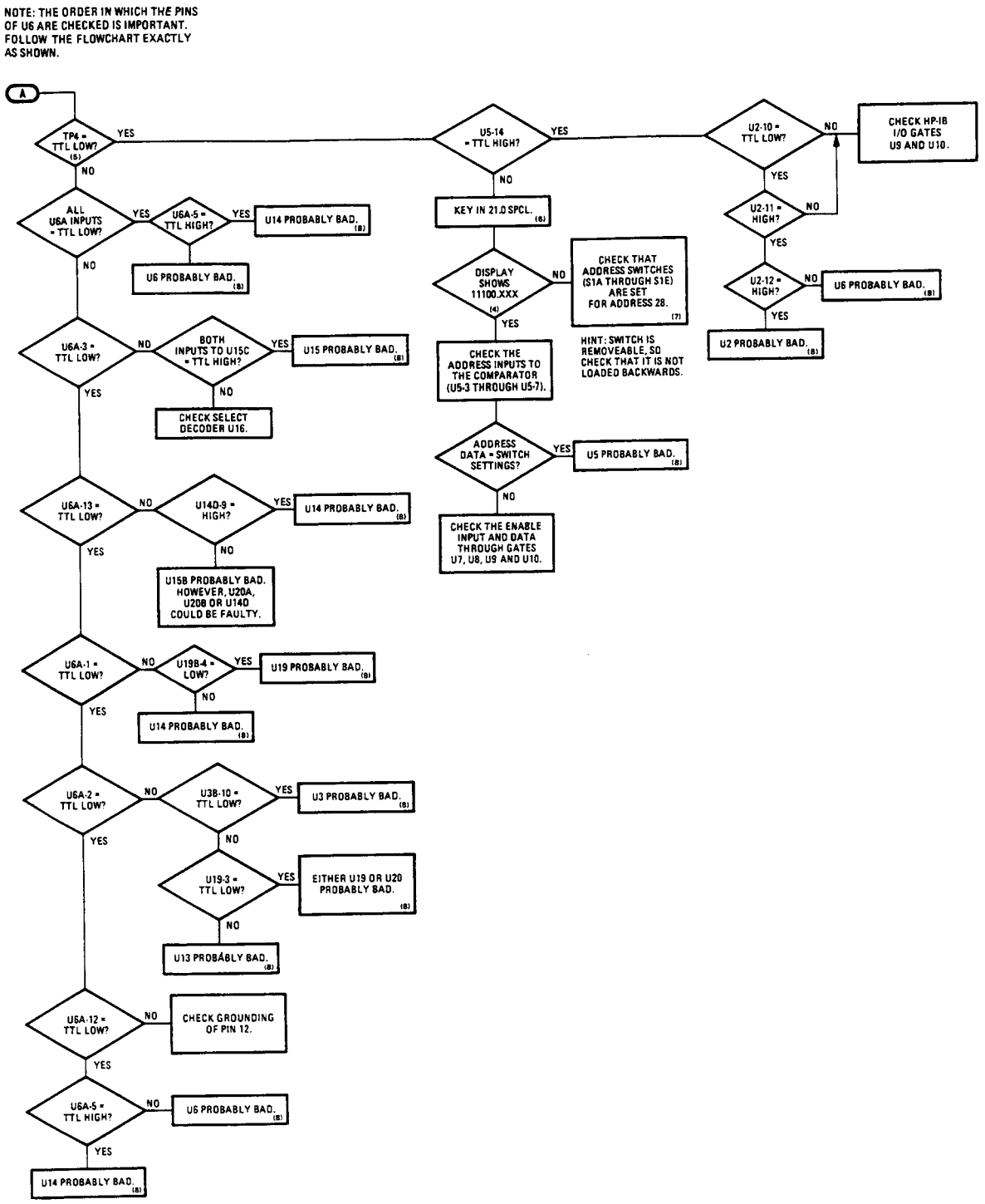


Figure 8D-9. Address Recognition Check Troubleshooting Flowchart, J1 *(2 of 2)*

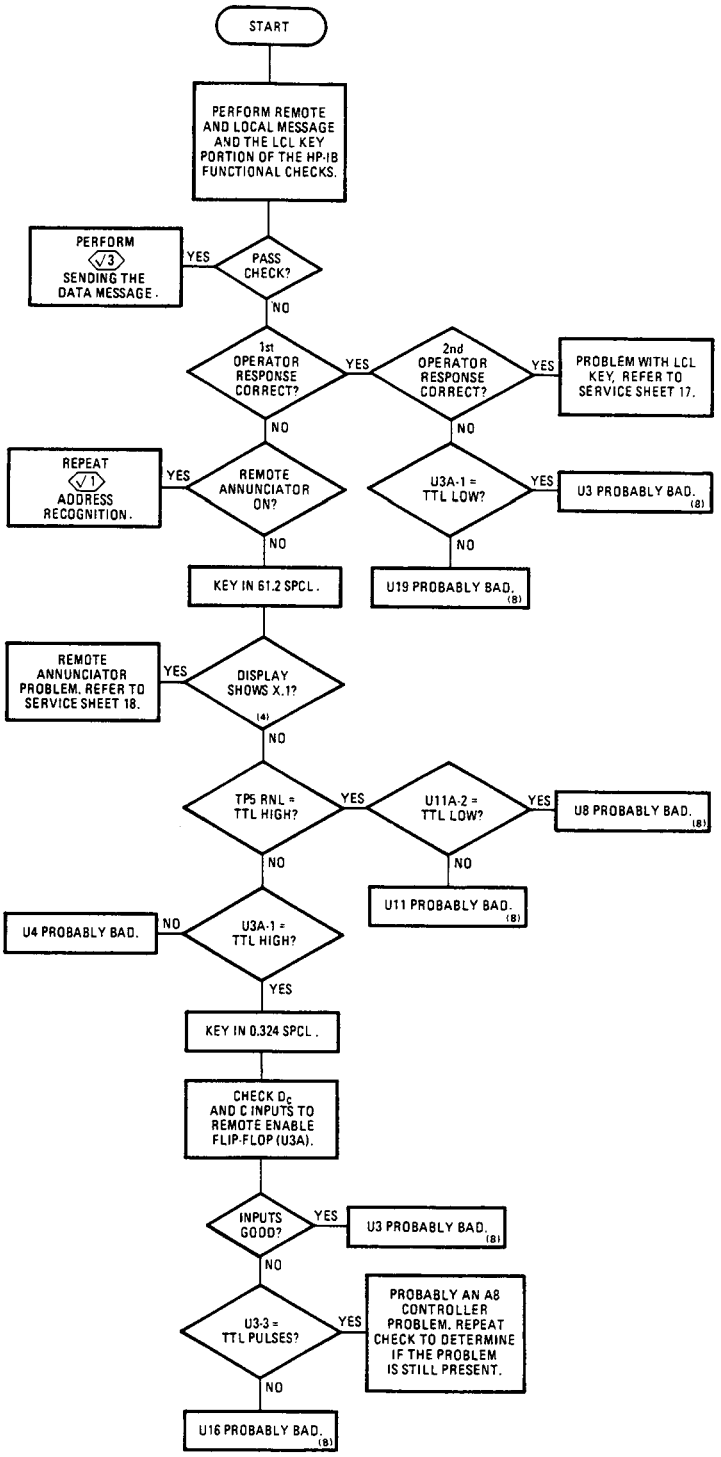


Figure 8D-10. Remote and Local Message and the LCL Key Check Troubleshooting Flowchart, √2

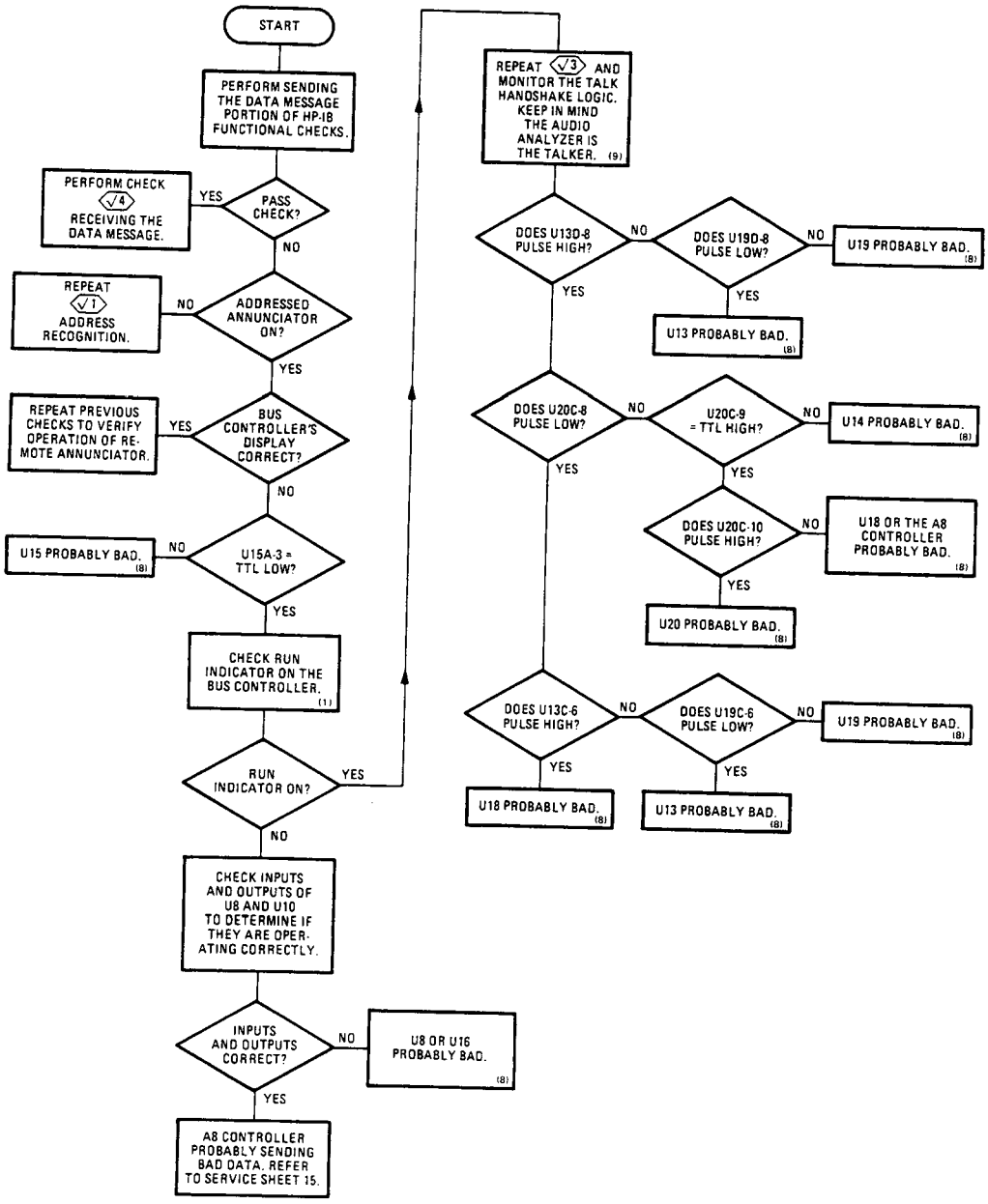


Figure 8D-11. Sending the Data Message Check Troubleshooting Flowchart, √3

TROUBLESHOOTING---SERVICE SHEET 19

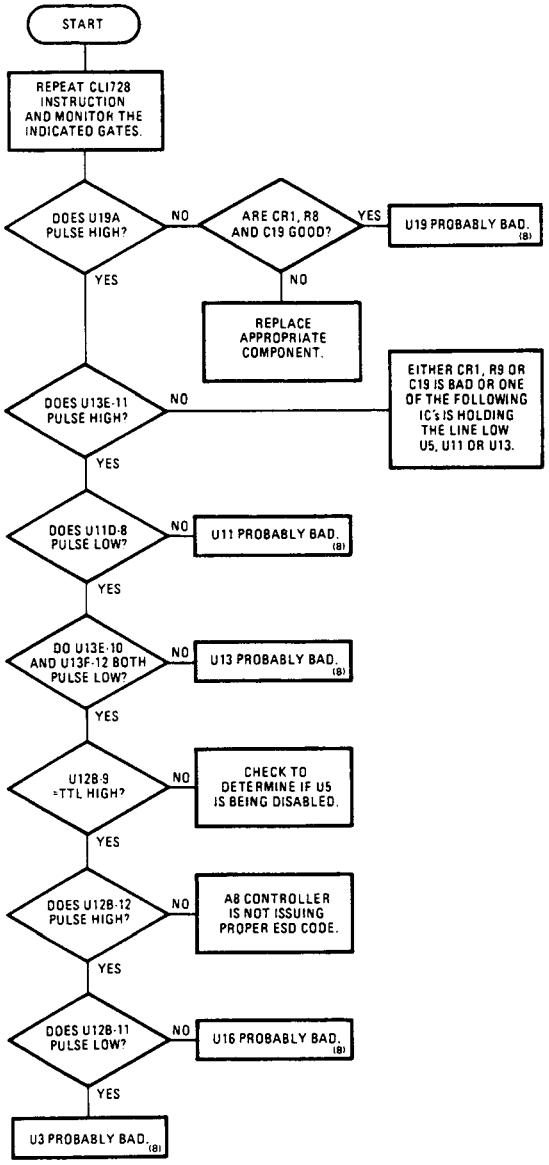
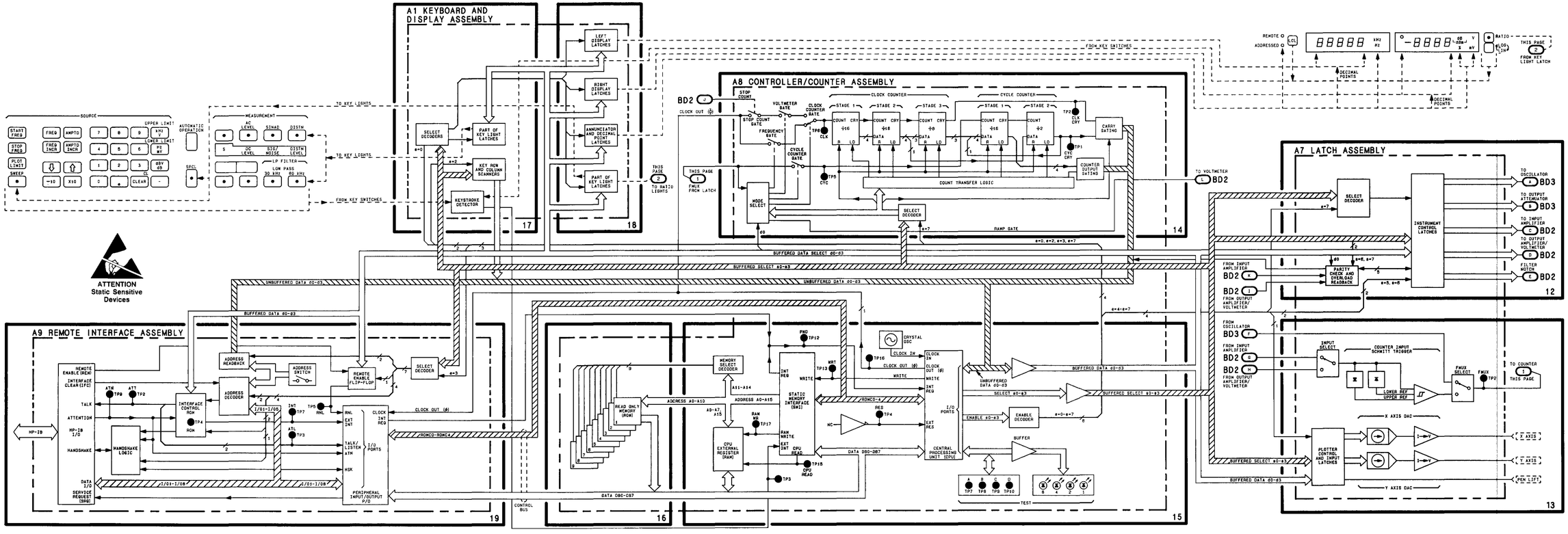


Figure 8D-12. Abort Message Check Troubleshooting Flowchart, ⟨J7⟩



BD4
Figure 8D-101
8D-101

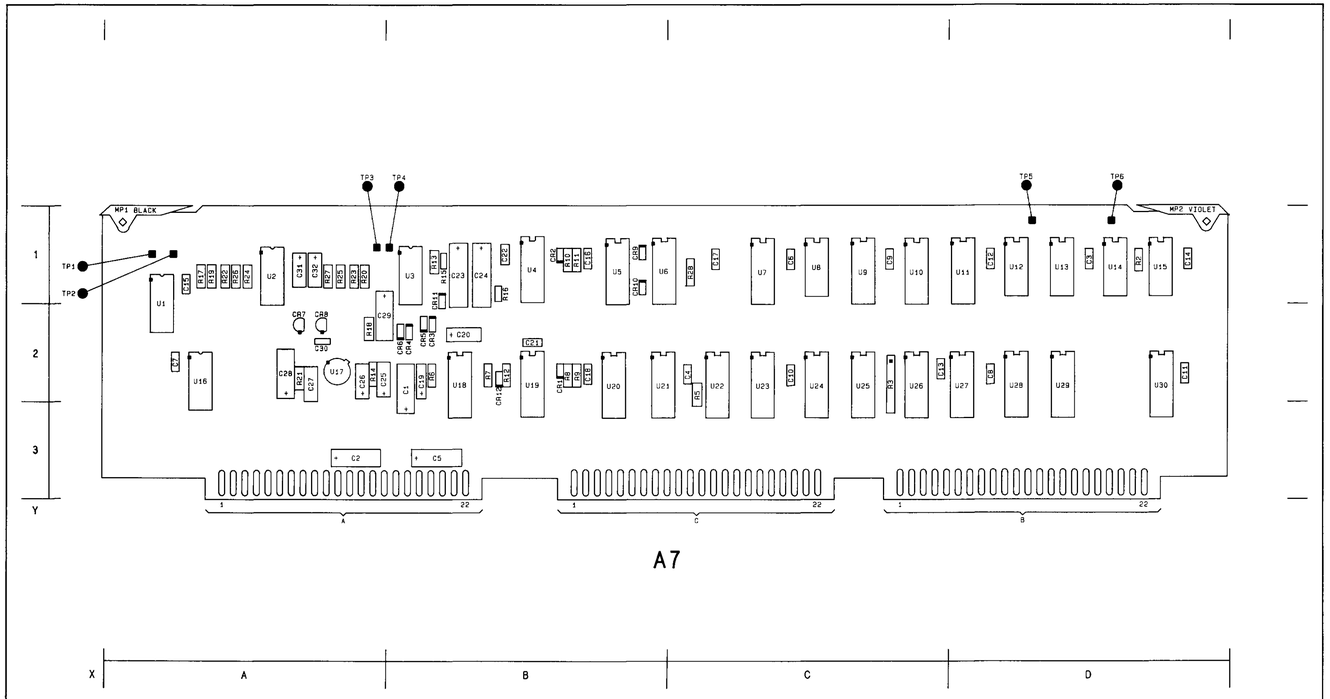


Figure 8D-102. SERVICE SHEET 12 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	B2						
C2	A3						
C3	D1						
C4	C2						
C5	B3						
C6	C1						
C7	A2						
C8	D2						
C9	C1						
C10	C2						
C11	D2						
C12	D1						
C13	C2						
C14	D1						
R2	D1						
R3	C2						
R5	C2						
TP1	A1						
TP5	D1						
TP6	D1						
U7	C1						
U8	C1						
U9	C1						
U10	C1						
U11	D1						
U12	D1						
U13	D1						
U14	D1						
U15	D1						
U23	C2						
U24	C2						
U25	C2						
U26	C2						
U27	D2						
U28	D2						
U29	D2						
U30	D2						

Digital Circuits Block Diagram **BD4**

SEE REVERSE SIDE

NOTES

LOGIC LEVELS

	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN	
> IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

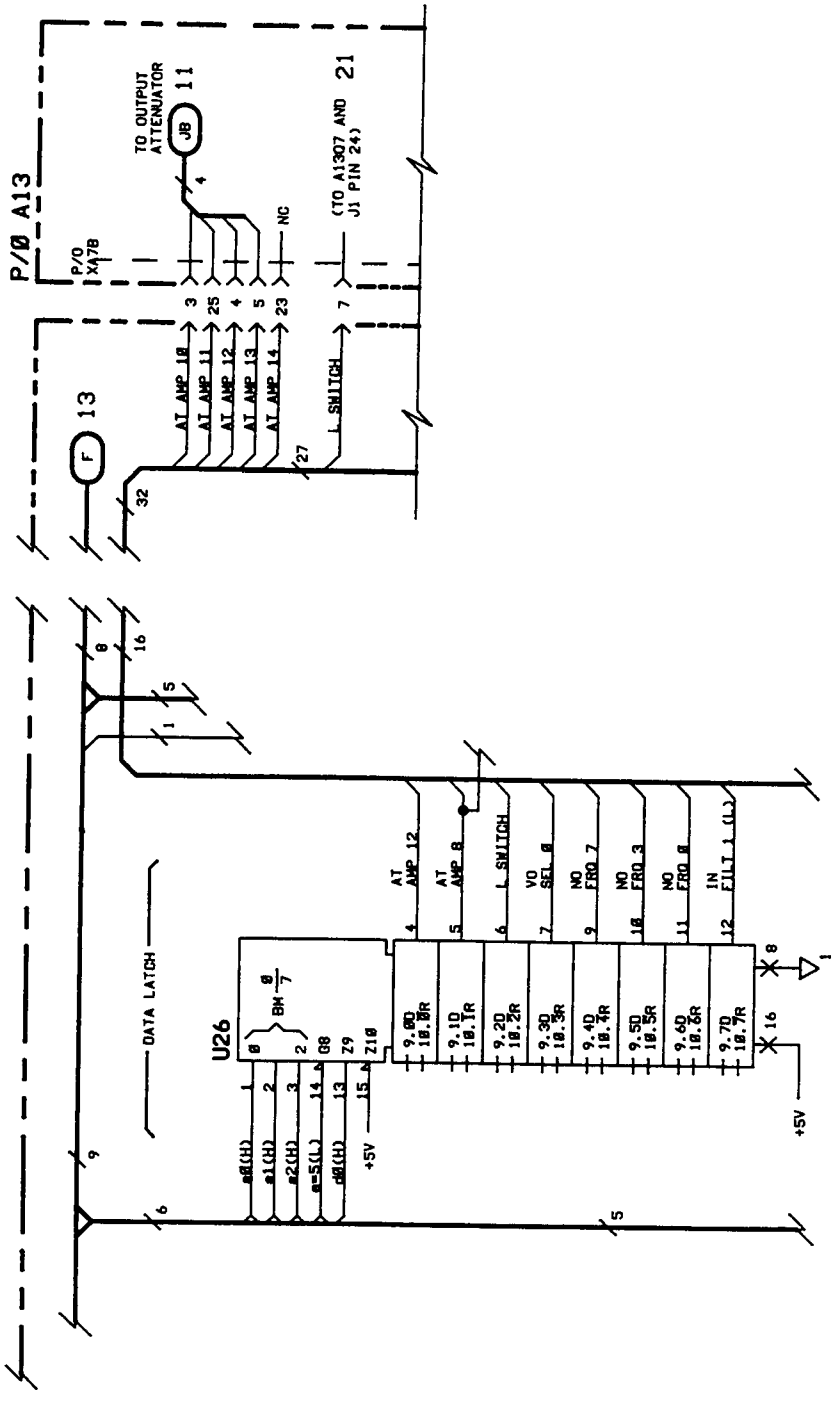
A7R3
TOP VIEW

PIN NO.	1	2	3	4	6	6	7	8
	GND	A	B	C	D	E	F	G

Schematic General Information

CHANGES

All serial prefixes	**On the A13 schematic:** • **U24** - On U24 pin 10 change AT AMP 5 to AT AMP 6 and on U24 pin 11 change AT AMP 1 to AT AMP 2.
2717A to 2742A	**On the A13 schematic:** • **08903-60192** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60192.
2742A and above	**On the A7 schematic:** • **08903-60130** - Use the schematic with the schematic partial on page 8D-102.3. **On the A7 Component Locator:** • **C27** - Mark C27 positive on the end closest to C2.
2813A and above	**On the A13 schematic:** • **08903-60292** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60292.


P/Ø A13
P/O XA7B
TO OUTPUT ATTENUATOR
J8
11
21
(TO A1307 AND J1 PIN 24)
NC
AT AMP 10
AT AMP 11
AT AMP 12
AT AMP 13
AT AMP 14
L SWITCH
27
32
13
DATA LATCH
U26
BM 8/7
AT AMP 12
AT AMP 8
L SWITCH
VO SEL 8
NO FRQ 7
NO FRQ 3
NO FRQ 8
IN FILT 1 (L)
+5V

P/O A13
POWER SUPPLY
AND MOTHERBOARD
ASSEMBLY
(08903-60129)

P/O A7 LATCH ASSEMBLY (08903-60130)

SERIAL PREFIX: 2450A

ATTENTION
Static Sensitive
Devices

SS12
Figure 8D-103
8D-103

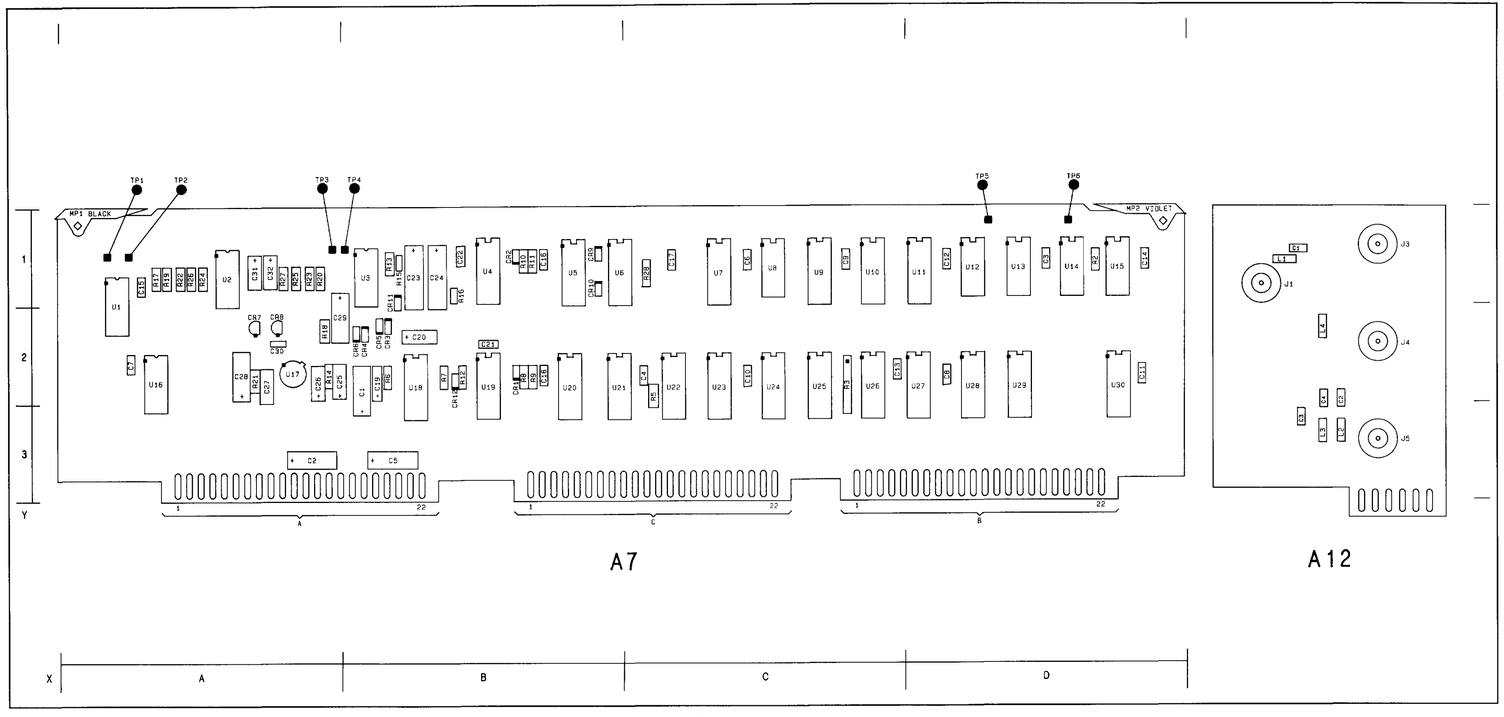


Figure 8D-104. SERVICE SHEET 13 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C15	A1						
C16	B1						
C17	C1						
C18	B2						
C19	B2						
C20	B2						
C21	B2						
C22	B1						
C23	B1						
C24	B1						
C25	A2						
C26	A2						
C27	A2						
C28	A2						
C29	A2						
C30	A2						
C31	A1						
C32	A1						
CR1	B2						
CR2	B1						
CR3	B2						
CR4	B2						
CR5	B2						
CR6	B2						
CR7	A2						
CR8	A2						
CR9	B1						
CR10	B1						
CR11	B1						
CR12	B2						
R6	B2						
R7	B2						
R8	B2						
R9	B2						
R10	B1						
R11	B1						
R12	B2						
R13	B1						
R14	A2						
R15	B1						
R16	B1						
R17	A1						
R18	A2						
R19	A1						
R20	A2						
R21	A2						
R22	A1						
R23	A1						
R24	A1						
R25	A1						
R26	A1						
R27	A1						
R28	C1						
TP2	A1						
TP3	A1						
TP4	B1						
U1	A1						
U2	A1						
U3	B1						
U4	B1						
U5	B1						
U6	B1						
U16	A2						
U17	A2						
U18	B2						
U19	B2						
U20	B2						
U21	B2						

P/O A7 Latch-Data Latches **SS12**

SEE REVERSE SIDE

NOTES

1. Chassis ground is made by mechanical contact of connector with rear panel.
2. * Asterisk indicates factory selected values.

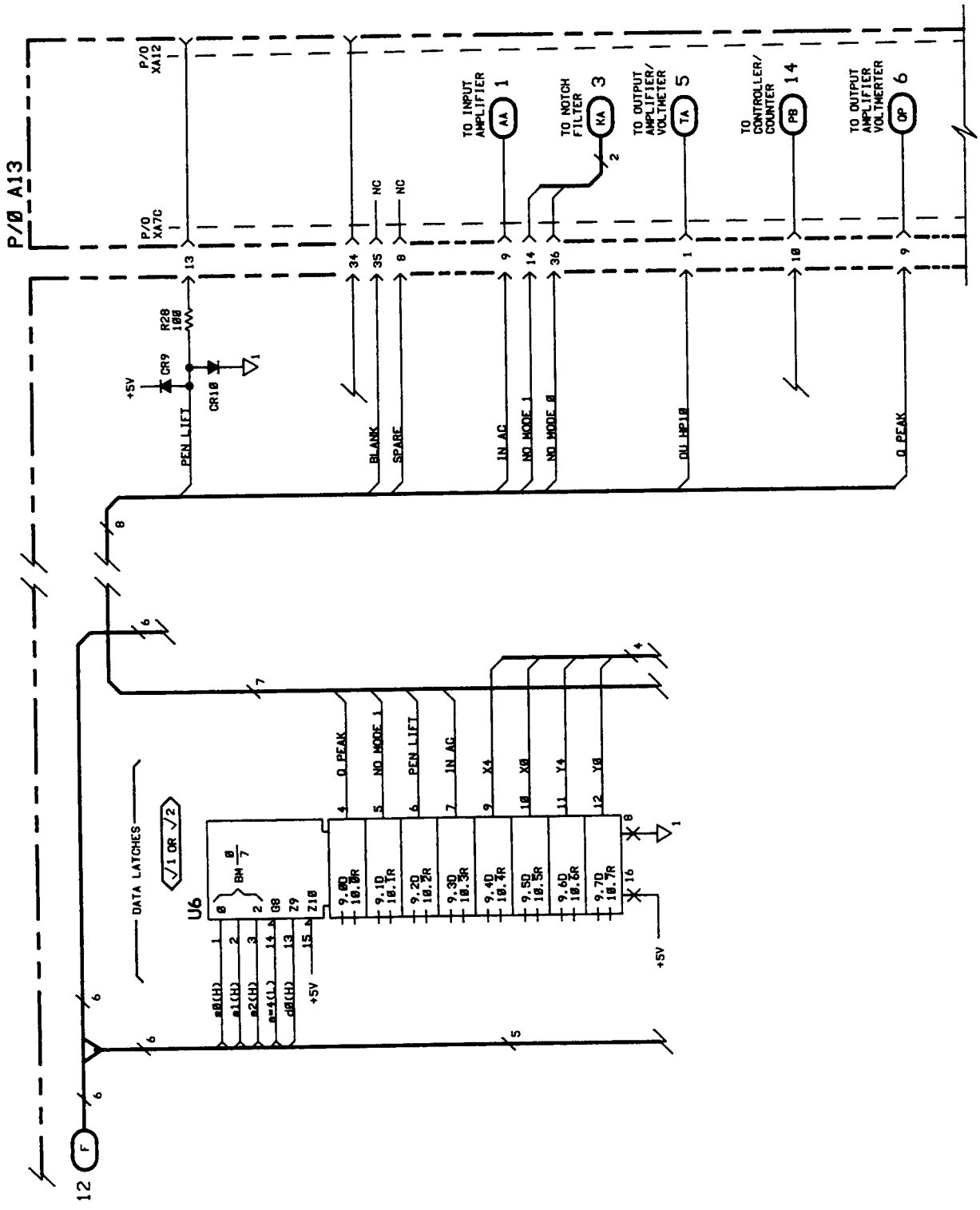
LOGIC LEVELS

	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN	
> IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

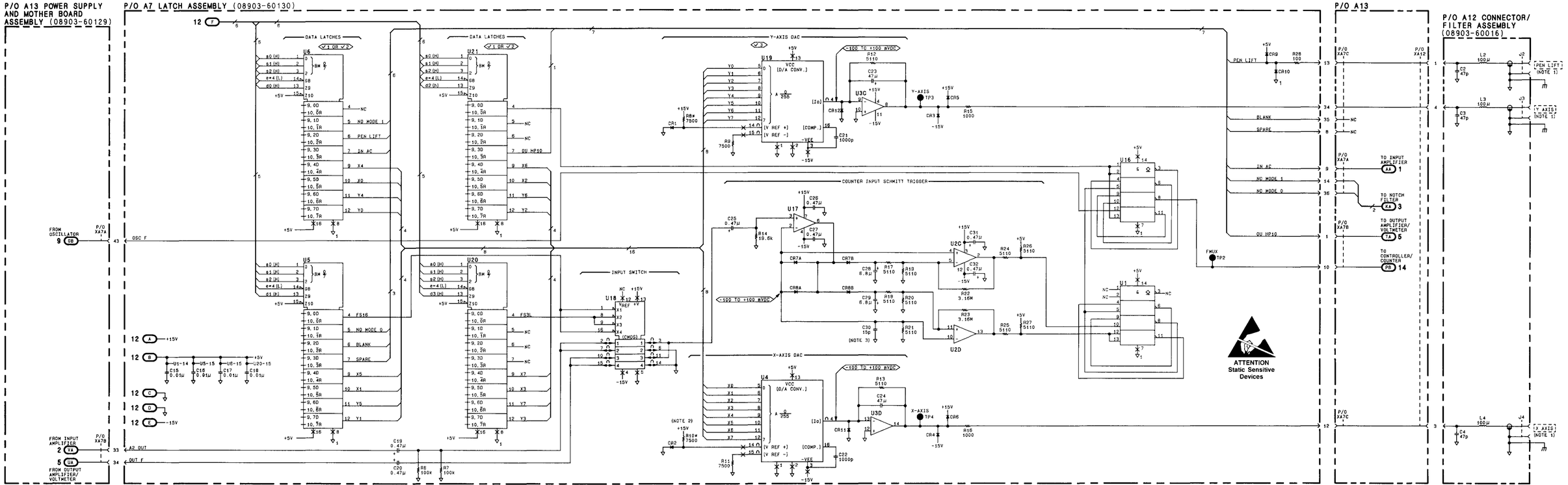
Schematic General Information

CHANGES

All serial prefixes	**On the A12 Component Locator:** • **J3, J4, J5** - Change J3 to J4, J4 to J3, and, J5 to J2.
2717A to 2742A	**On the A13 schematic:** • **08903-60192** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60192.
2742A and above	**On the A7 schematic:** • **R12, R13** - In the center of the P/O A7 LATCH ASSEMBLY, under Y-AXIS DAC, change the value of R12 to 5K and under X-AXIS DAC, change the value of R13 to 5K. • **08903-60130** - Use the schematic with the schematic partial on page 8D-104.3.
2813A and above	**On the A13 schematic:** • **08903-60292** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60292.



P/O A7 LATCH ASSEMBLY (2742A and above)


P/O A13 POWER SUPPLY AND MOTHER BOARD ASSEMBLY (08903-60129)
P/O A7 LATCH ASSEMBLY (08903-60130)
P/O A13
P/O A12 CONNECTOR/ FILTER ASSEMBLY (08903-60016)
DATA LATCHES
Y-AXIS DAC
COUNTER INPUT SCHMITT TRIGGER
INPUT SWITCH
X-AXIS DAC
FROM OSCILLATOR
FROM INPUT AMPLIFIER
FROM OUTPUT AMPLIFIER/ VOLTMETER
OSC F
A2 OUT
OUT F
PEN LIFT
BLANK
SPARE
IN AC
NC MODE 1
NC MODE 0
QU HP10
FMUX
TO INPUT AMPLIFIER
TO NOTCH FILTER
TO OUTPUT AMPLIFIER/ VOLTMETER
TO CONTROLLER/ COUNTER
ATTENTION Static Sensitive Devices
SERIAL PREFIX: 2450A

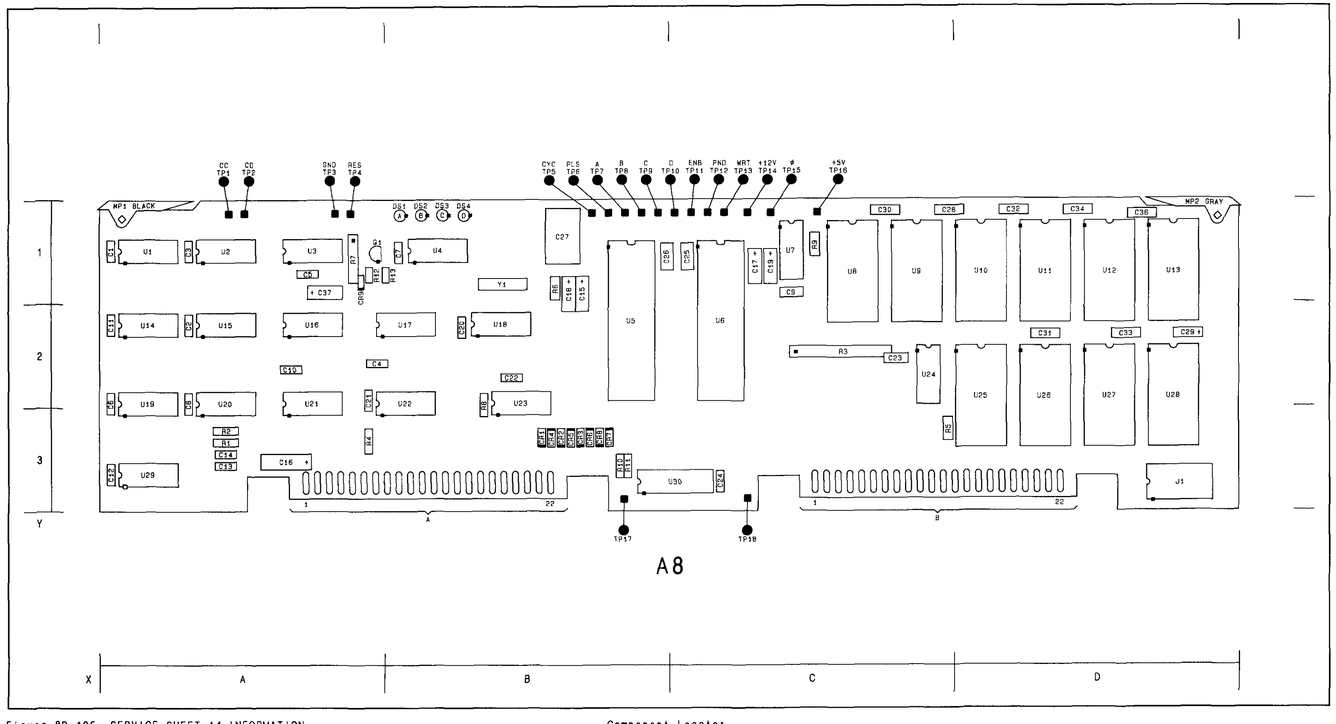


Figure 8D-106. SERVICE SHEET 14 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	A1						
C2	A2						
C3	A1						
C4	A2						
C5	A1						
C6	A2						
C7	B1						
C8	A2						
C9	C1						
C10	A2						
C11	A2						
C12	A3						
C13	A3						
C14	A3						
R1	A3						
R2	A3						
TP1	A1						
TP2	A1						
TP5	B1						
TP6	B1						
U1	A1						
U2	A1						
U3	A1						
U4	B1						
U7	C1						
U14	A2						
U15	A2						
U17	B2						
U19	A3						
U20	A3						
U21	A2						
U29	A3						

P/O A7, P/O A12
SEE REVERSE SIDE

Latch-DAC and Counter Trigger Circuits

SS13

NOTES

LOGIC LEVELS

	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

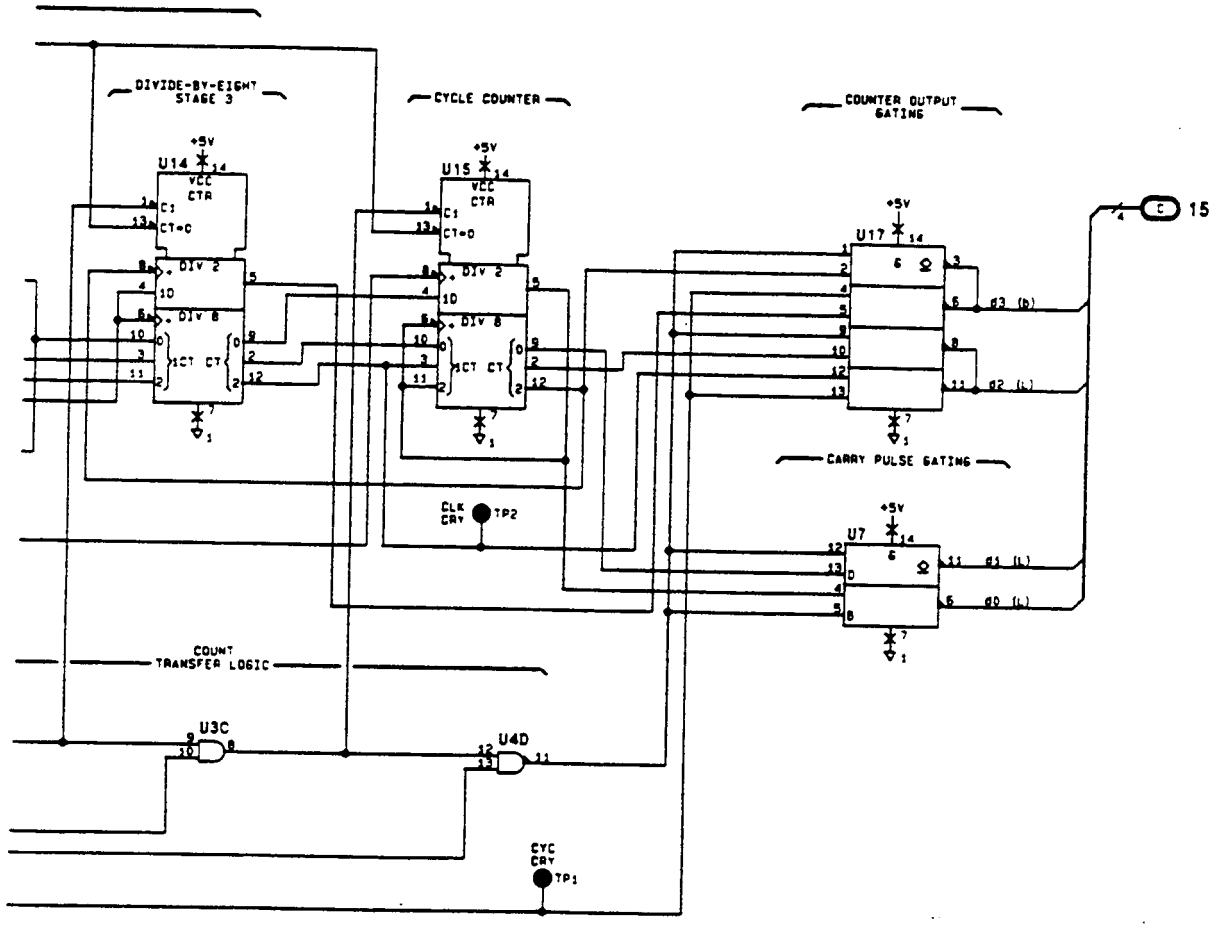
Schematic General Information

CHANGES

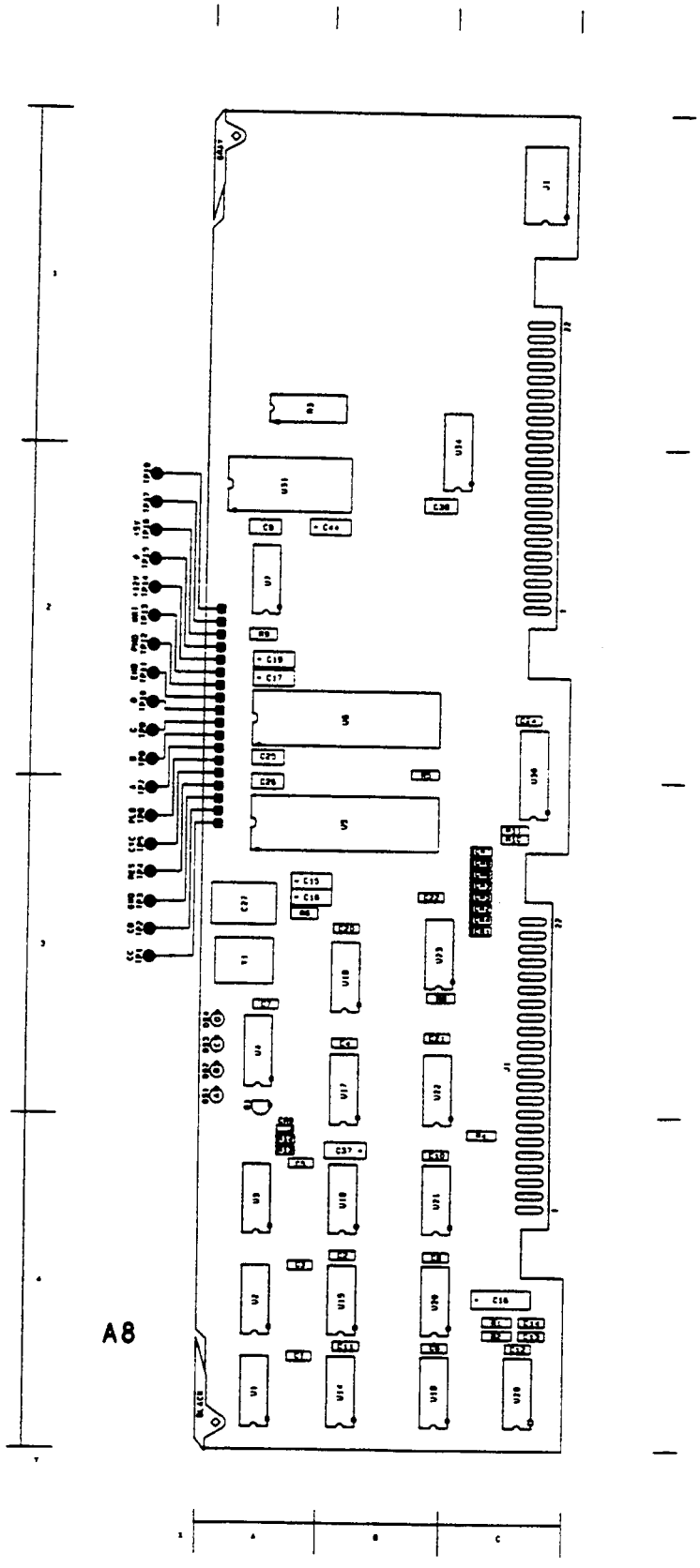
All serial prefixes	**On the A8 schematic:** • **08903-60134** - Modify Service Sheet 14 by adding the new partial schematic P/O SS14, P/O A8 CONTROLLER/COUNTER ASSEMBLY on page 8D-106.3.
2652A only	**On the A8 schematic:** • **08903-60184** - Change the part number of the A8 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60184. **On the A8 Component Locator:** • **08903-60184** - Use the new A8 component locator on page 8D-106.4. **On the A8 Component Coordinates:** • **08903-60184** - Use the new A8 component coodinates on page 8D-106.5.
2717A to 2742A	**On the A13 schematic:** • **08903-60192** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60192.
2813A to 2922A	**On the A13 schematic:** • **08903-60292** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60292.
2944A and above	**On the A8 schematic:** • **08903-60300** - Use the new schematic foldout on page 8D-106.11. SS14 with the revision date of rev.01OCT89. **On the A8 Component Locator:** • **08903-60300** - Use the new A8 Component Locator on page 8D-106.8 with the revision date of rev.01OCT89. **On the A8 Component Coordinates:** • **08903-60300** - Use the new A8 Component Coordinates on page 8D-106.9 with the revision date of rev.01OCT89.

CHANGES

2948A and above	**On the A13 schematic:** • **08903-60392** - Use the new schematic foldout on page 8D-106.11. SS14 with the revision date of rev.01OCT89.



P/O SS14 A8 Controller/Counter Assembly

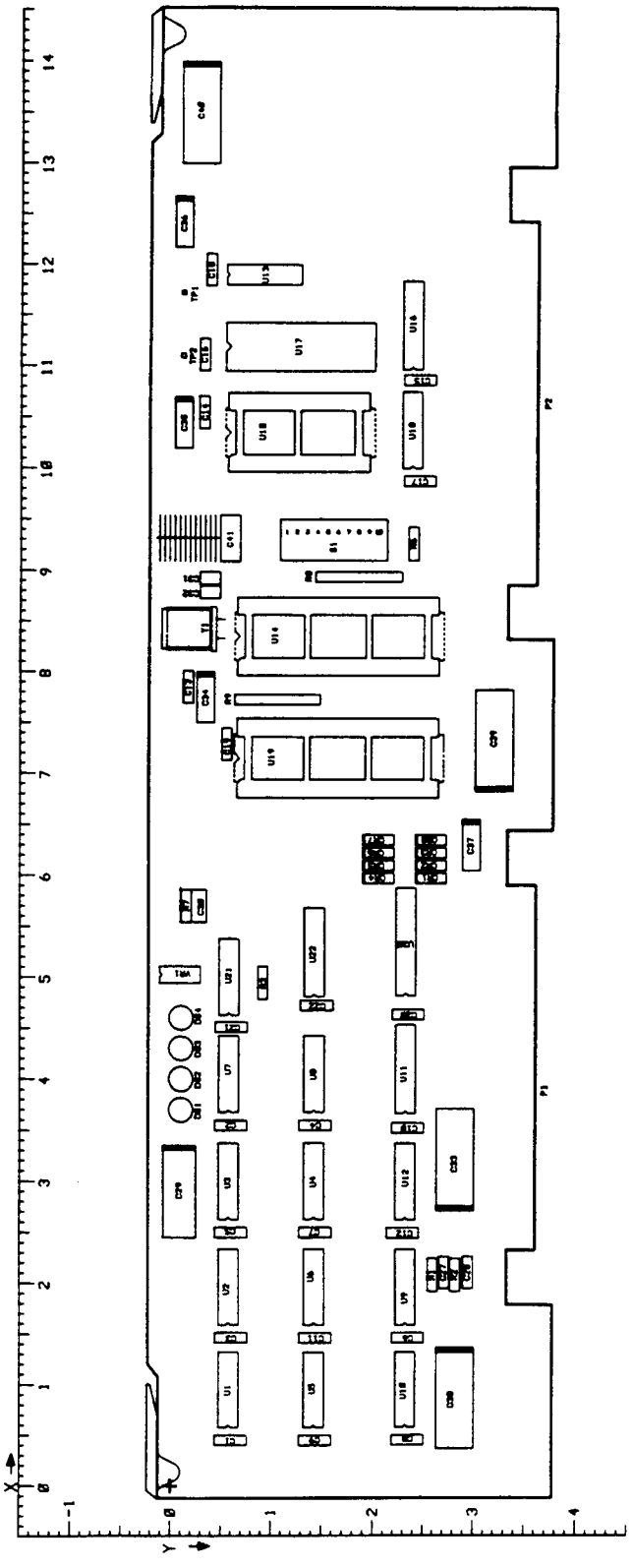


A8 Component Locator (2652A only)

A8 Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	A,4	R1	C,4	U20	B,4				
C2	B,4	R3	A,1	U21	B,4				
C3	A,4	R4	C,4	U22	B,1				
C4	B,1	R5	B,2	U23	B,1				
C5	A,4	R6	A,3	U30	C,2				
C6	B,4	R8	B,1	U31	A,2				
C7	A,3	R9	A,2	U34	C,2				
C8	B,4	R10	C,3						
C9	A,2	R11	C,3	Y1	A,3				
C10	B,4	R12	A,4						
C11	B,4	R13	A,4						
C15	A,3								
C17	A,2	TP1	A,3						
C18	A,3	TP2	A,3						
C19	A,2	TP3	A,3						
C20	B,1	TP4	A,3						
C21	B,1	TP5	A,2						
C22	B,1	TP6	A,2						
C24	C,2	TP7	A,2						
C25	A,2	TP8	A,2						
C26	A,3	TP9	A,2						
C27	A,3	TP10	A,2						
C37	B,4	TP11	A,2						
C38	B,2	TP12	A,2						
C44	B,2	TP13	A,2						
		TP14	A,2						
CR1	C,3	TP15	A,2						
CR2	C,3	TP16	A,2						
CR3	C,3	TP17	A,2						
CR4	C,3	TP18	A,2						
CR5	C,3								
CR6	C,3	U1	A,4						
CR7	C,3	U2	A,4						
CR8	C,3	U3	A,4						
CR9	A,4	U4	A,3						
		U5	B,1						
DS1	A,3	U6	B,2						
DS2	A,3	U7	A,2						
DS3	A,3	U14	B,4						
DS4	A,3	U15	B,4						
		U16	B,4						
J1	C,1	U17	B,1						
		U18	B,1						
Q1	A,3	U19	B,4						

A8 Component Coordinates (2652A only)



A8 Component Locator
2948A (HP8903B)
2946A (HP8903E)

SS14

COMP	X	Y	COMP	X	Y	COMP	X	Y
C1	0.5	0.4	DS1	3.7	0.1			
C2	3.6	0.4	DS2	4.0	0.1			
C3	1.5	0.4	DS3	4.3	0.1			
C4	3.6	1.2	DS4	4.6	0.1	VR1	4.9	-0.1
C5	2.5	0.4						
C6	1.5	2.1	P1	4.1	3.6	Y1	8.3	0.5
C7	2.5	1.2	P2	10.6	3.6			
C8	0.5	2.1						
C9	0.5	1.2	R1	1.8	2.6			
C10	3.5	2.1	R2	1.8	2.8			
C11	1.5	1.2	R3	4.7	0.9			
C12	2.5	2.1						
C13	7.6	0.2						
C14	10.3	0.3	R6	9.0	2.4			
C15	10.9	2.2	R7	5.5	0.1			
C16	10.9	0.3	R8	8.9	1.5			
C17	9.9	2.2	R9	7.7	0.7			
C18	11.7	0.4						
C19	7.1	0.6						
C20	4.6	2.1	S1	9.2	1.2			
C21	4.5	0.4						
C22	4.7	1.2						
			TP1	11.7	0.1			
			TP2	11.1	0.1			
C27	1.9	2.7	U1	0.7	0.7			
C28	1.9	3.0	U2	1.7	0.7			
C29	3.4	0.1	U3	2.7	0.7			
C30	5.5	0.3	U4	2.7	1.6			
C31	8.9	0.4	U5	0.7	1.6			
C32	8.8	0.4	U6	1.7	1.6			
C33	2.6	2.8	U7	3.8	0.7			
C34	8.1	0.3	U8	3.8	1.6			
C35	10.8	0.1	U9	1.7	2.5			
C36	12.8	0.1	U10	0.7	2.5			
C37	6.6	3.0	U11	3.8	2.5			
C38	1.4	2.8	U12	2.7	2.5			
C39	6.8	3.2	U13	11.8	0.6			
C40	14.1	0.3	U14	8.1	0.7			
C41	9.3	0.6	U15	10.1	0.6			
			U16	11.1	2.5			
CR1	6.0	2.4	U17	10.9	0.6			
CR2	6.1	2.4	U18	10.1	2.5			
CR3	6.2	2.4	U19	6.9	0.7			
CR4	6.0	1.9	U20	4.9	2.5			
CR5	6.1	1.9	U21	4.7	0.7			
CR6	6.2	1.9	U22	4.9	1.6			
CR7	6.4	1.9						
CR8	6.4	2.4						

A8 Component Coordinates
2948A (HP8903B)
2946A (HP8903E)

P/O A8 CONTROLLER/COUNTER ASSEMBLY (08903-60300 FOR HP8903B / 8903-60301 FOR HP8903E)

P/O A13 POWER SUPPLY AND MOTHER BOARD ASSEMBLY (08903-60129 FOR HP8903B/ 08903-60395 FOR HP8903E)

FROM OUTPUT AMPLIFIER/ VOLTMETER

7 DB

P/O XA8A

P1(39)

STOP_COUNT_(H)

FROM LATCH

13 P8

P1(12)

FMUX

DB(H)

SS16 H

STOP COUNT GATE

VOLTMETER GATE

MODE SELECT

FREQUENCY GATE

SS15, 16 C(H) K

SELECT DECODER

SS16 J S0-S3(H)

SS16 E E7(L)

CLOCK COUNTER GATE

CYCLE COUNTER GATE

CLOCK COUNTER

DIVIDE-BY-SIXTEEN STAGE 1

DIVIDE-BY-SIXTEEN STAGE 2

DIVIDE-BY-EIGHT STAGE 3

CYCLE COUNTER

COUNTER OUTPUT GATING

COUNT TRANSFER LOGIC

RAMP GATE (L)

P1(9)

P/O A13

P/O XA8A

CB SS7

TO OUTPUT AMPLIFIER/ VOLTMETER

DB-D3(L) C SS16

D3(L)

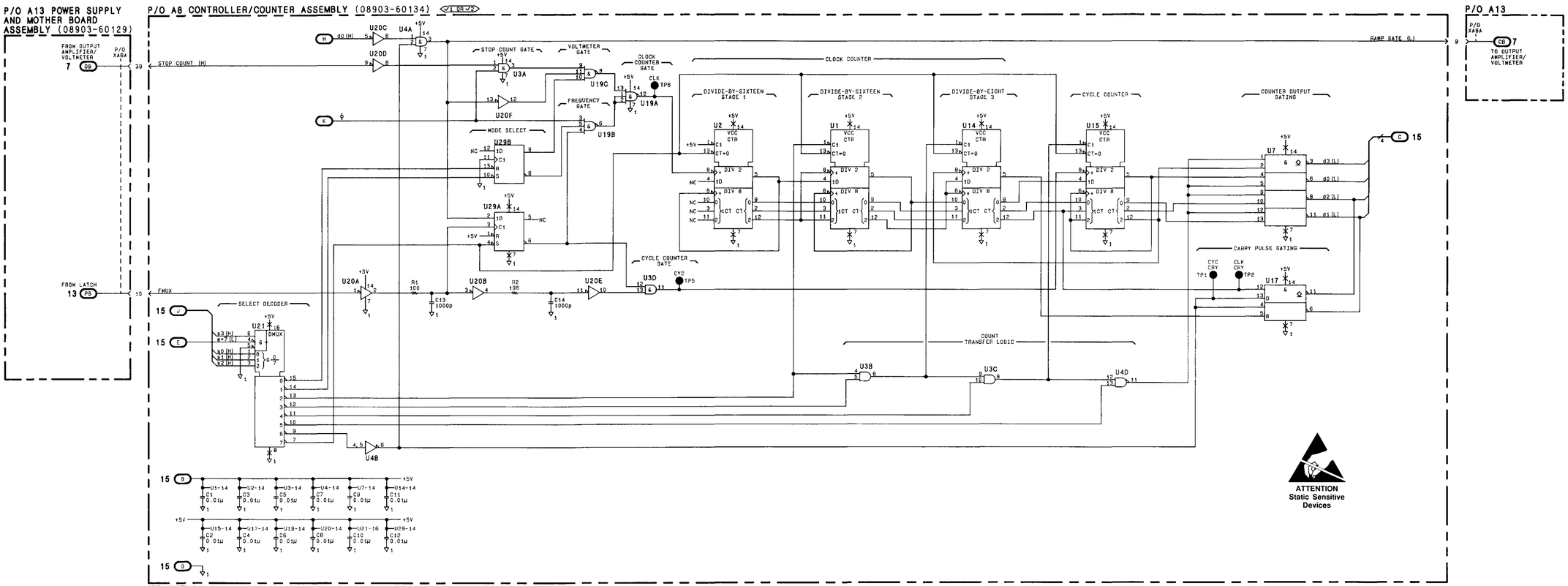
D2(L)

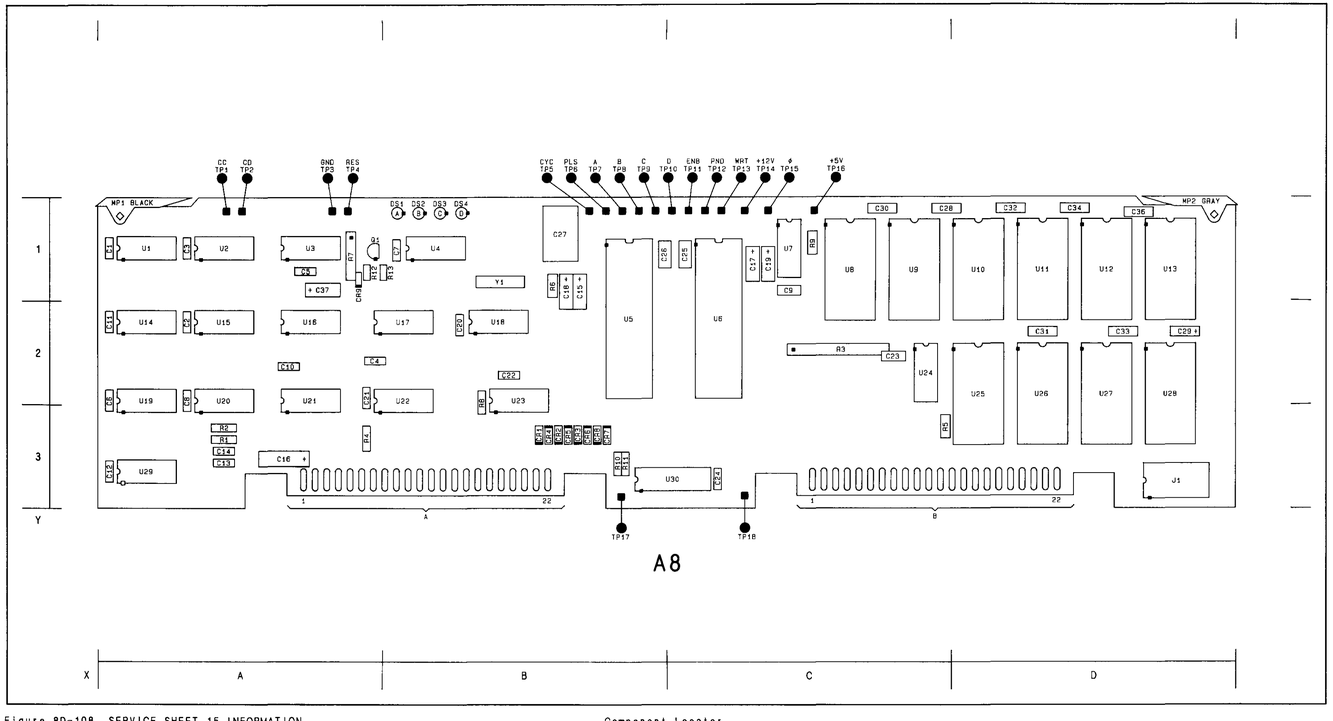
D0(L)

D1(L)

SS14

Figure 8D-106.11
(rev 01OCT89)


P/O A13 POWER SUPPLY AND MOTHER BOARD ASSEMBLY (08903-60129)
FROM OUTPUT AMPLIFIER/ VOLTMETER
7 CB
P/O XABA 1
39
STOP COUNT (H)
FROM LATCH
13 PB
10
FMUX
P/O A8 CONTROLLER/COUNTER ASSEMBLY (08903-60134) 1 OF 2
P/O A13
P/O XABA 1
CB 7
TO OUTPUT AMPLIFIER/ VOLTMETER
RAMP GATE (L)
STOP COUNT GATE
VOLTMETER GATE
FREQUENCY GATE
MODE SELECT
CLOCK COUNTER GATE
CYCLE COUNTER GATE
CLOCK COUNTER
DIVIDE-BY-SIXTEEN STAGE 1
DIVIDE-BY-SIXTEEN STAGE 2
DIVIDE-BY-EIGHT STAGE 3
CYCLE COUNTER
COUNTER OUTPUT GATING
CARRY PULSE GATING
SELECT DECODER
COUNT TRANSFER LOGIC
U20C
U20D
U4A
U3A
U19C
U19A
U20F
U19B
U29B
U29A
U2
U1
U14
U15
U7
U17
U20A
U20B
U20E
U3D
U21
U4B
U3B
U3C
U4D
R1 100
R2 196
C13 1000p
C14 1000p
TP1
TP2
TP5
TP6
CYC CRY
CLK CRY
ATTENTION Static Sensitive Devices
SERIAL PREFIX: 2450A



A8

Figure 8D-108. SERVICE SHEET 15 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C15	B1						
C16	A3						
C17	C1						
C18	B1						
C19	C1						
C20	B2						
C21	A2						
C22	B2						
C23	C2						
C24	C3						
C25	C1						
C26	B1						
C27	B1						
C37	A1						
CR1	B3						
CR2	B3						
CR3	B3						
CR4	B3						
CR5	B3						
CR6	B3						
CR7	B3						
CR8	B3						
CR9	A1						
DS1	B1						
DS2	B1						
DS3	B1						
DS4	B1						
J1	D3						
Q1	A1						
R3	C2						
R4	A3						
R5	C3						
R6	B1						
R7	A1						
R8	B2						
R9	C1						
R10	B3						
R11	B3						
R12	A1						
R13	B1						
TP3	A1						
TP4	A1						
TP7	B1						
TP8	B1						
TP9	B1						
TP10	C1						
TP11	C1						
TP12	C1						
TP13	C1						
TP14	C2						
TP15	C1						
TP16	C1						
TP17	B3						
TP18	C3						
U5	B2						
U6	C2						
U16	A2						
U18	B2						
U22	B2						
U23	B2						
U24	C2						
U30	C3						
Y1	B1						

P/O A8 Controller/Counter-Counter Circuits **SS14**

SEE REVERSE SIDE

NOTES

LOGIC LEVELS

	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN	
> IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

A8R7
TOP VIEW

PIN NO.	1	2	3	4	5	6	7	8
	+5V	A	B	C	D	E	F	G

A8R3
TOP VIEW

PIN NO.	1	2	3	4	5	6	7	8	9
	A	B	C	D	E	F	G	H	+5V

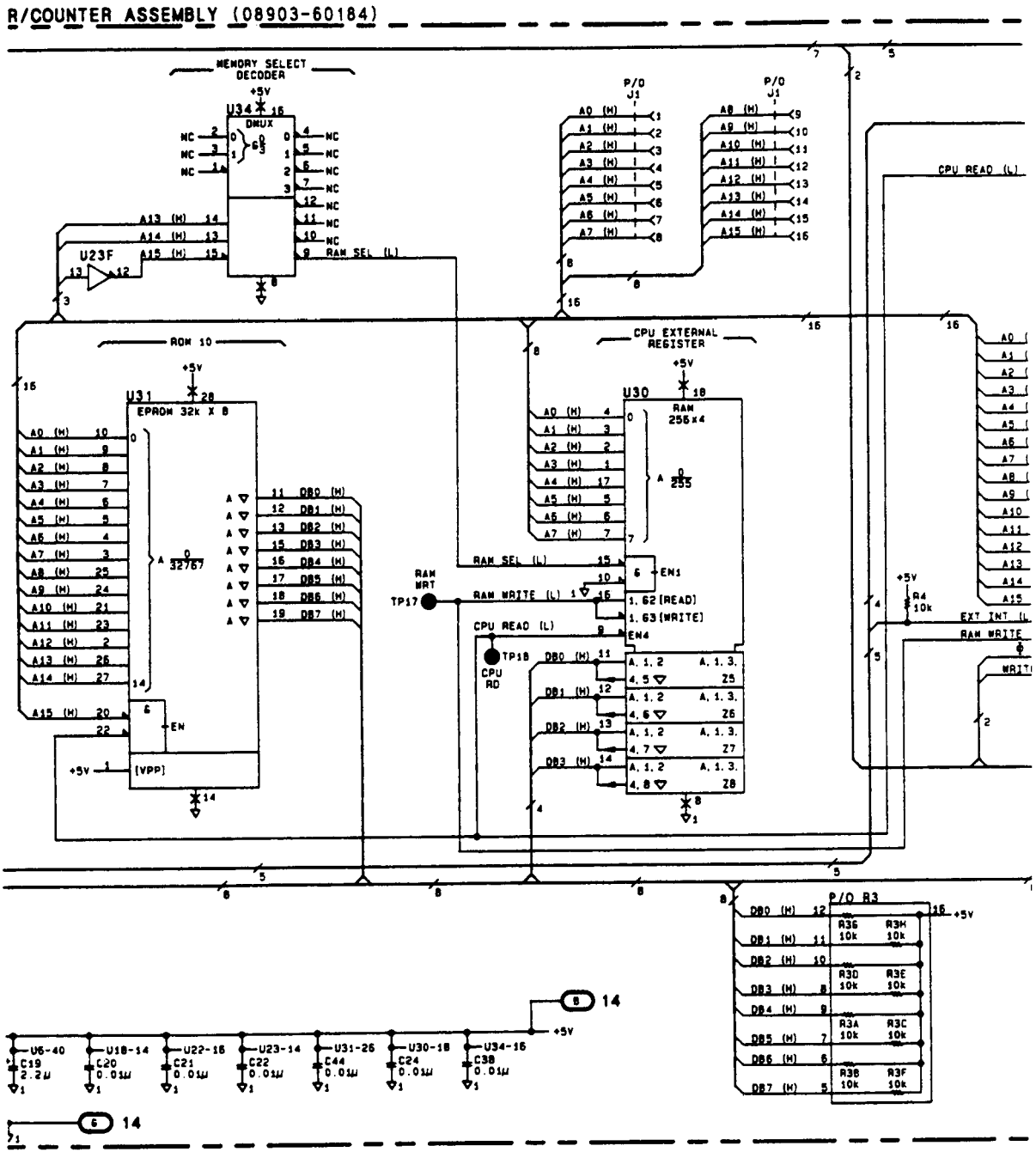
Schematic General Information

CHANGES

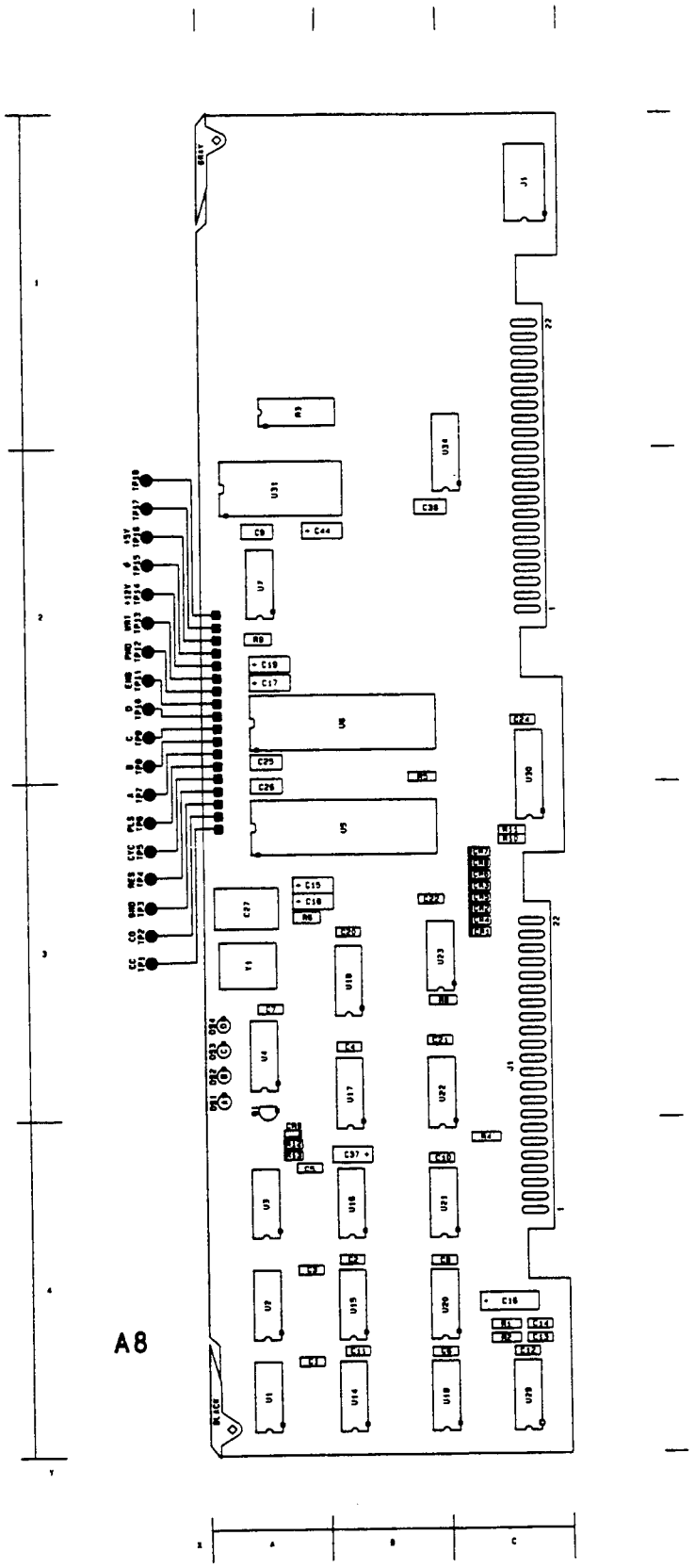
2652A only	**On the A8 schematic:** • **08903-60184** - Use the new partial schematic, P/O SS15 A8 CONTROLLER/COUNTER ASSEMBLY (2652A) on page 8D-108.3. • **R7A, R7B, R7C, R7D**- Under TEST, delete R7A through R7D. • **C44** - In the bottom left portion of the schematic change the value of C44 to 2.2uF. **On the A8 Component Locator:** • **08903-60184** - Use the new A8 component locator (2652A only) on page 8D-108.4. **On the A8 Component Coordinates:** • **08903-60184** - Use the new A8 component coordinates (2652A only) on page 8D-108.5.
2717A to 2742A	**On the A13 schematic:** • **08903-60192** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60192.
2813A to 2922A	**On the A13 schematic:** • **08903-60292** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60292.
2948A and above	**On the A8 schematic:** • **08903-60300** - Use the new schematic foldout on page 8D-108.11, SS15 with the revision date of rev.01OCT89. **On the A8 Component Locator:** • **08903-60300** - Use the new A8 Component Locator on page 8D-108.8 with the revision date of rev.01OCT89. **On the A8 Component Coordinates:** • **08903-60300** - Use the new A8 Component Coordinates on page 8D-108.9 with the revision date of rev.01OCT89.

CHANGES

2948A and above	**On the A13 schematic:** • **08903-60392** - Use the new schematic foldout on page 8D-108.11, SS15 with the revision date of rev.01OCT89.



P/O SS15, A8 Controller/Counter Assembly (2652A only)

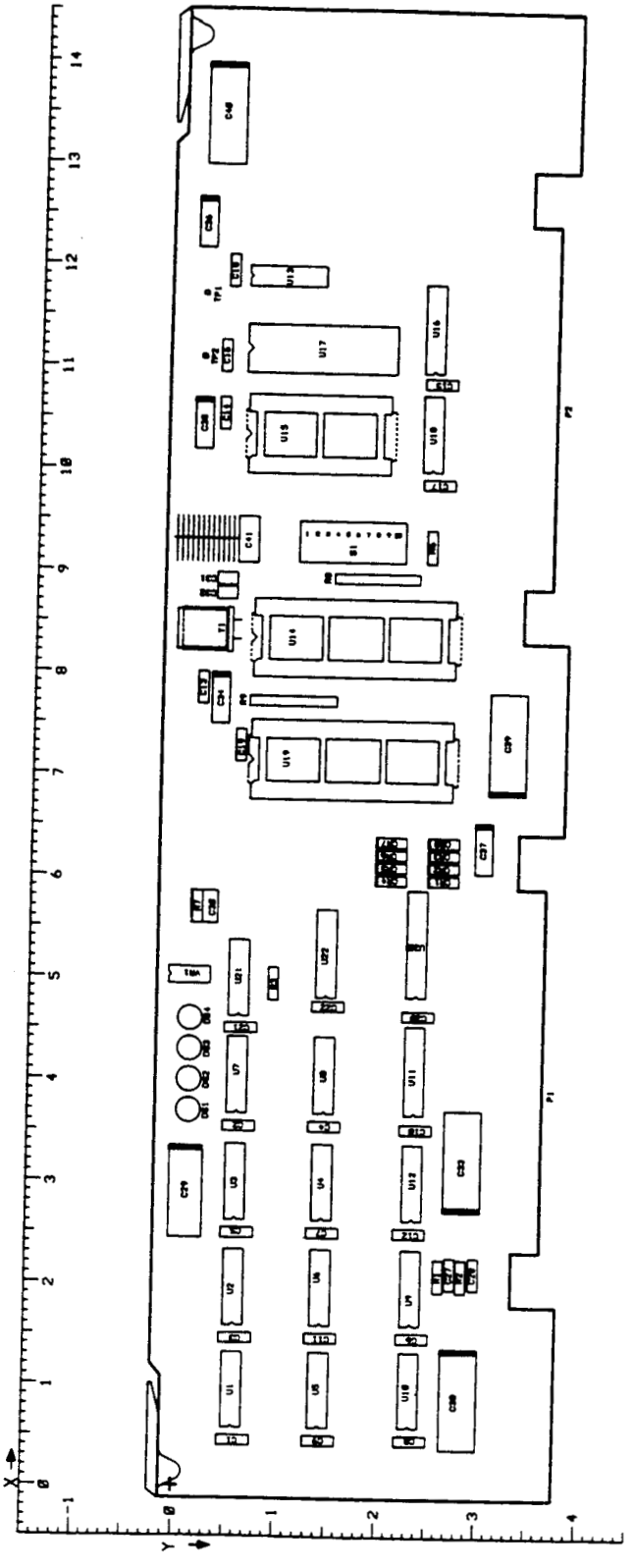


A8 Component Locator (2652A only)

A8 Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	A,4	R1	C,4	U20	B,4				
C2	B,4	R3	A,1	U21	B,4				
C3	A,4	R4	C,4	U22	B,1				
C4	B,1	R5	B,2	U23	B,1				
C5	A,4	R6	A,3	U30	C,2				
C6	B,4	R8	B,1	U31	A,2				
C7	A,3	R9	A,2	U34	C,2				
C8	B,4	R10	C,3						
C9	A,2	R11	C,3	Y1	A,3				
C10	B,4	R12	A,4						
C11	B,4	R13	A,4						
C15	A,3								
C17	A,2	TP1	A,3						
C18	A,3	TP2	A,3						
C19	A,2	TP3	A,3						
C20	B,1	TP4	A,3						
C21	B,1	TP5	A,2						
C22	B,1	TP6	A,2						
C24	C,2	TP7	A,2						
C25	A,2	TP8	A,2						
C26	A,3	TP9	A,2						
C27	A,3	TP10	A,2						
C37	B,4	TP11	A,2						
C38	B,2	TP12	A,2						
C44	B,2	TP13	A,2						
		TP14	A,2						
CR1	C,3	TP15	A,2						
CR2	C,3	TP16	A,2						
CR3	C,3	TP17	A,2						
CR4	C,3	TP18	A,2						
CR5	C,3								
CR6	C,3	U1	A,4						
CR7	C,3	U2	A,4						
CR8	C,3	U3	A,4						
CR9	A,4	U4	A,3						
		U5	B,1						
DS1	A,3	U6	B,2						
DS2	A,3	U7	A,2						
DS3	A,3	U14	B,4						
DS4	A,3	U15	B,4						
		U16	B,4						
J1	C,1	U17	B,1						
		U18	B,1						
Q1	A,3	U19	B,4						

A8 Component Coordinates (2652A only)



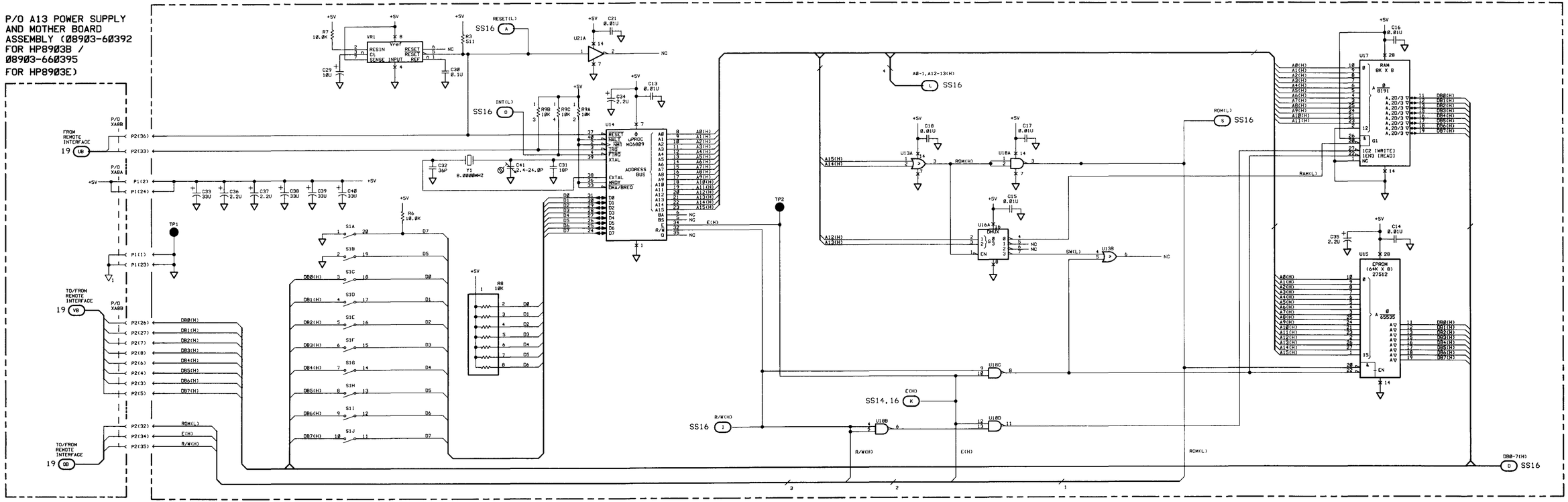
A8 Component Locator
2948A (HP8903B)
2946A (HP8903E)

COMP	X	Y	COMP	X	Y	COMP	X	Y
C1	0.5	0.4	DS1	3.7	0.1			
C2	3.6	0.4	DS2	4.0	0.1			
C3	1.5	0.4	DS3	4.3	0.1			
C4	3.6	1.2	DS4	4.6	0.1	VR1	4.9	-0.1
C5	2.5	0.4						
C6	1.5	2.1	P1	4.1	3.6	Y1	8.3	0.5
C7	2.5	1.2	P2	10.6	3.6			
C8	0.5	2.1						
C9	0.5	1.2	R1	1.8	2.6			
C10	3.5	2.1	R2	1.8	2.8			
C11	1.5	1.2	R3	4.7	0.9			
C12	2.5	2.1						
C13	7.6	0.2						
C14	10.3	0.3	R6	9.0	2.4			
C15	10.9	2.2	R7	5.5	0.1			
C16	10.9	0.3	R8	8.9	1.5			
C17	9.9	2.2	R9	7.7	0.7			
C18	11.7	0.4						
C19	7.1	0.6						
C20	4.6	2.1	S1	9.2	1.2			
C21	4.5	0.4						
C22	4.7	1.2						
			TP1	11.7	0.1			
			TP2	11.1	0.1			
C27	1.9	2.7	U1	0.7	0.7			
C28	1.9	3.0	U2	1.7	0.7			
C29	3.4	0.1	U3	2.7	0.7			
C30	5.5	0.3	U4	2.7	1.6			
C31	8.9	0.4	U5	0.7	1.6			
C32	8.8	0.4	U6	1.7	1.6			
C33	2.6	2.8	U7	3.8	0.7			
C34	8.1	0.3	U8	3.8	1.6			
C35	10.8	0.1	U9	1.7	2.5			
C36	12.8	0.1	U10	0.7	2.5			
C37	6.6	3.0	U11	3.8	2.5			
C38	1.4	2.8	U12	2.7	2.5			
C39	6.8	3.2	U13	11.8	0.6			
C40	14.1	0.3	U14	8.1	0.7			
C41	9.3	0.6	U15	10.1	0.6			
			U16	11.1	2.5			
CR1	6.0	2.4	U17	10.9	0.6			
CR2	6.1	2.4	U18	10.1	2.5			
CR3	6.2	2.4	U19	6.9	0.7			
CR4	6.0	1.9	U20	4.9	2.5			
CR5	6.1	1.9	U21	4.7	0.7			
CR6	6.2	1.9	U22	4.9	1.6			
CR7	6.4	1.9						
CR8	6.4	2.4						

A8 Component Coordinates
2948A (HP8903B)
2946A (HP8903E)

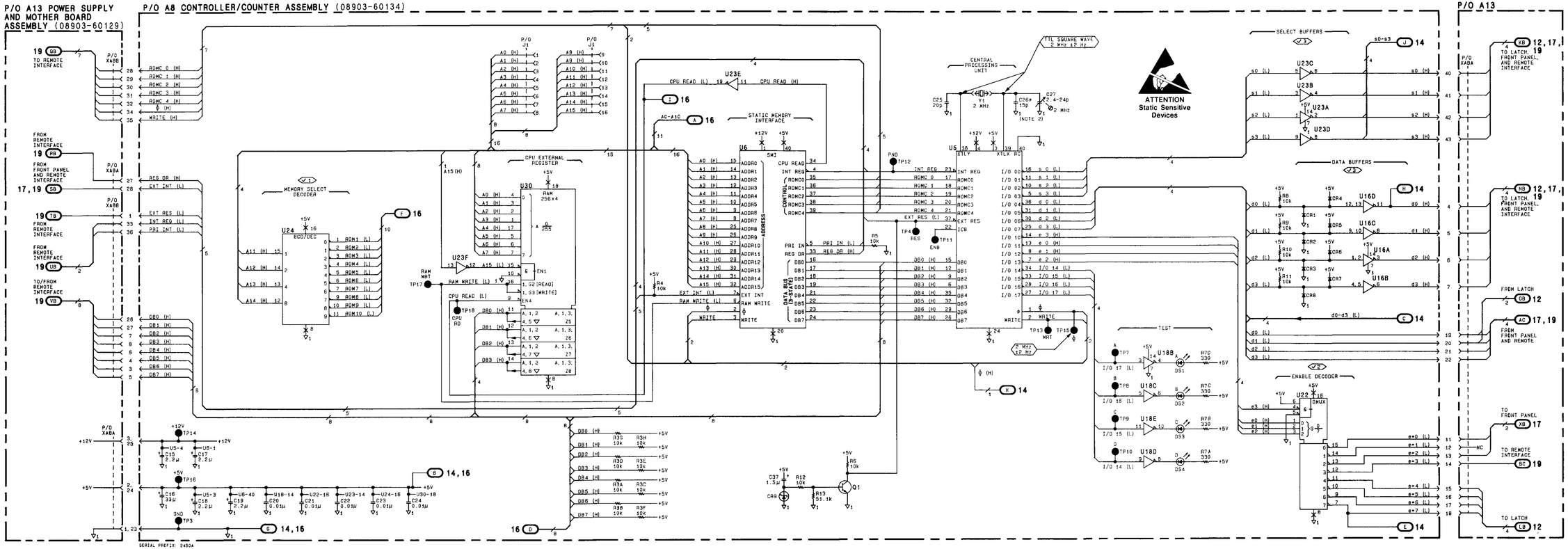
P/O A8 CONTROLLER/COUNTER ASSEMBLY (08903-60300 FOR HP8903B / 08903-60301 FOR HP8903E)

P/O A13 POWER SUPPLY AND MOTHER BOARD ASSEMBLY (08903-60392 FOR HP8903B / 08903-660395 FOR HP8903E)



SS15

Figure 8D-108.11
(rev 01OCT89)



SS15
Figure 8D-109
8D-109

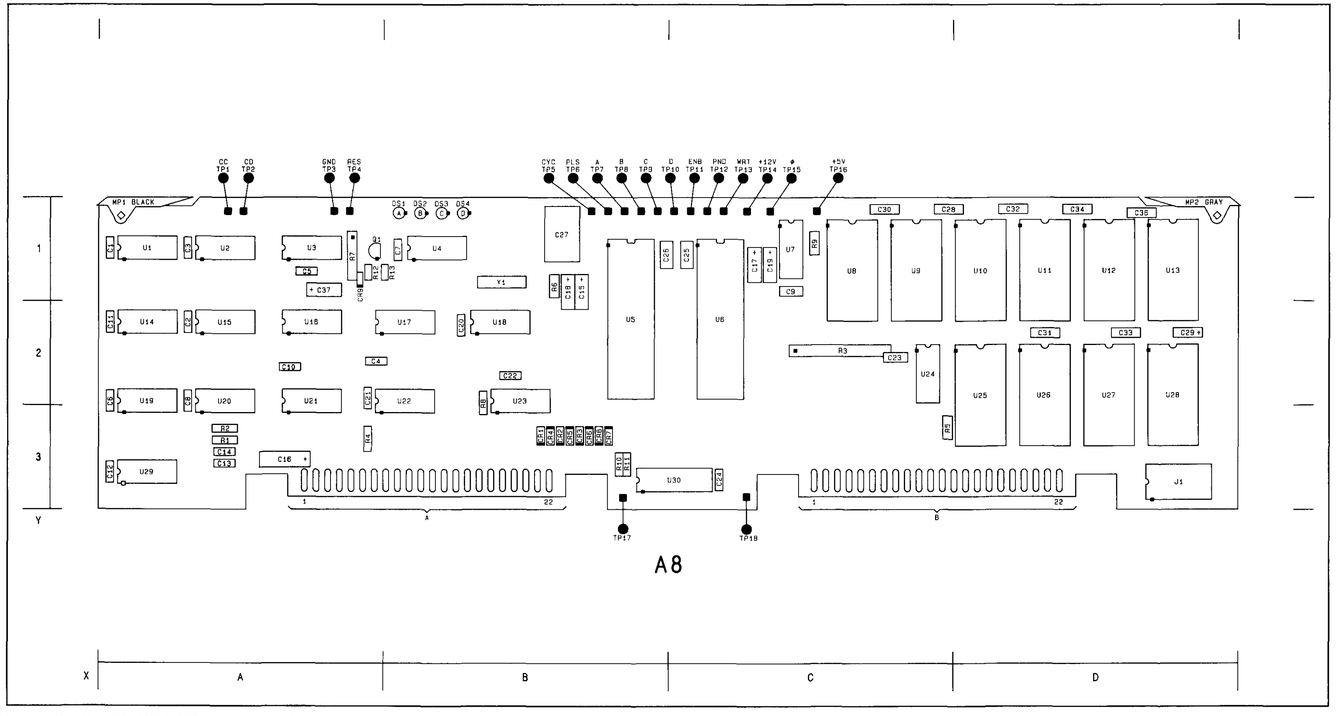


Figure 8D-110. SERVICE SHEET 16 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C28	C1						
C29	D2						
C30	C1						
C31	D2						
C32	C1						
C33	D2						
C34	C1						
C36	D1						
U8	C1						
U9	C1						
U10	B1						
U11	B1						
U12	B1						
U13	C1						
U26	D2						
U27	D2						
U28	D2						

P/O A8 SEE REVERSE SIDE

Controller/ Counter- Controller

SS15

NOTES

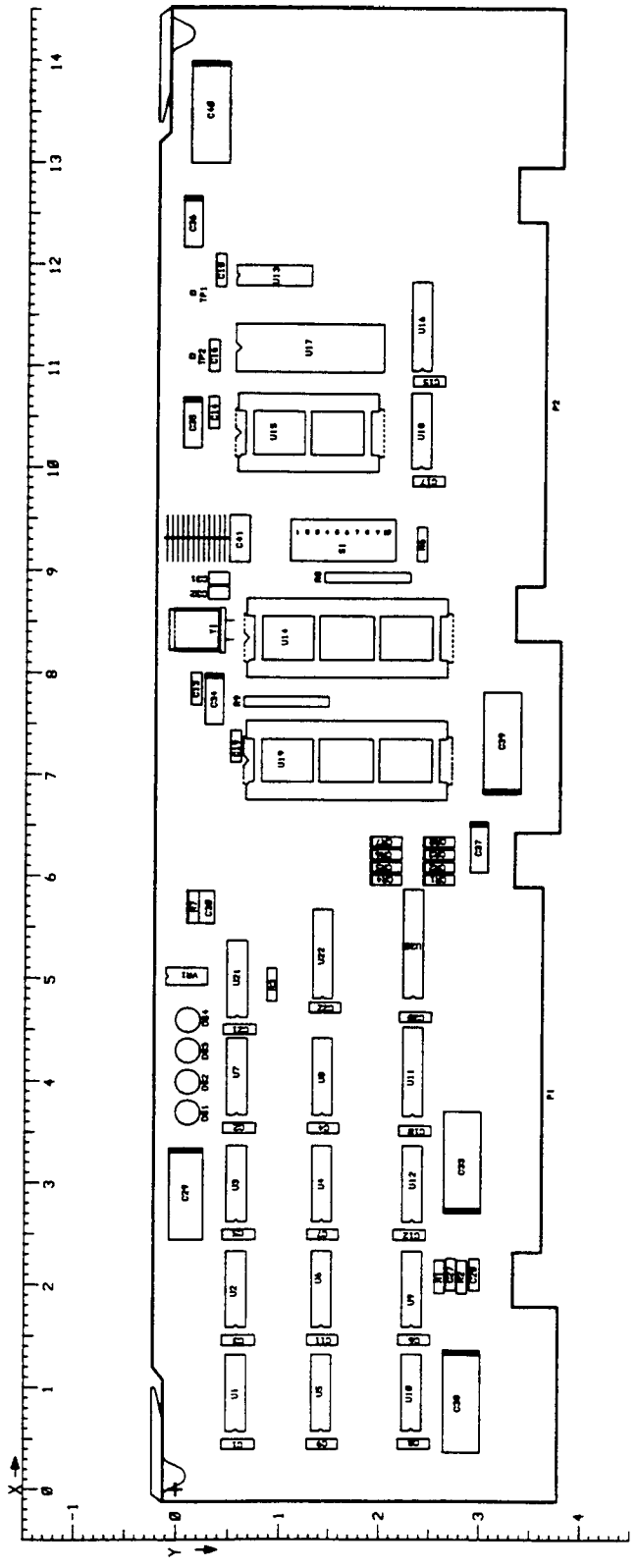
LOGIC LEVELS

	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

Schematic General Information

CHANGES

2450A to 2614A	**On the A8 schematic:** • **08903-60134** - This Service Sheet 16 applies only to the A8 CONTROLLER/COUNTER BOARD ASSEMBLY, part number 08903-60134. **On the A8 Component Locator:** • **08903-60134** - This component locator applies only to the A8 CONTROLLER/COUNTER BOARD ASSEMBLY, part number 08903-60134. **On the A8 Component Coordinates:** • **08903-60134** - This component coordinates applies only to the A8 CONTROLLER/COUNTER BOARD ASSEMBLY, part number 08903-60134.
2652A to 2922A	**On the A8 schematic:** • **08903-60184** - This Service Sheet 16 does not apply to the A8 CONTROLLER/COUNTER BOARD ASSEMBLY, part number 08903-60184.
2948A and above	**On the A8 schematic:** • **08903-60300** - Use the new schematic foldout on page 8D-110.7, SS16 with the revision date of rev.01OCT89. **On the A8 Component Locator:** • **08903-60300** - Use the new A8 component locator on page 8D-110.4 with the revision date of rev.01OCT89. **On the A8 Component Coordinates:** • **08903-60300** - Use the new A8 component coordinates on page 8D-110.5 with the revision date of rev.01OCT89. **On the A13 schematic:** • **08903-60392** - Use the new schematic foldout on page 8D-110.7, SS16 with the revision date of rev.01OCT89.



A8 Component Locator
2948A (HP8903B)
2946A (HP8903E)

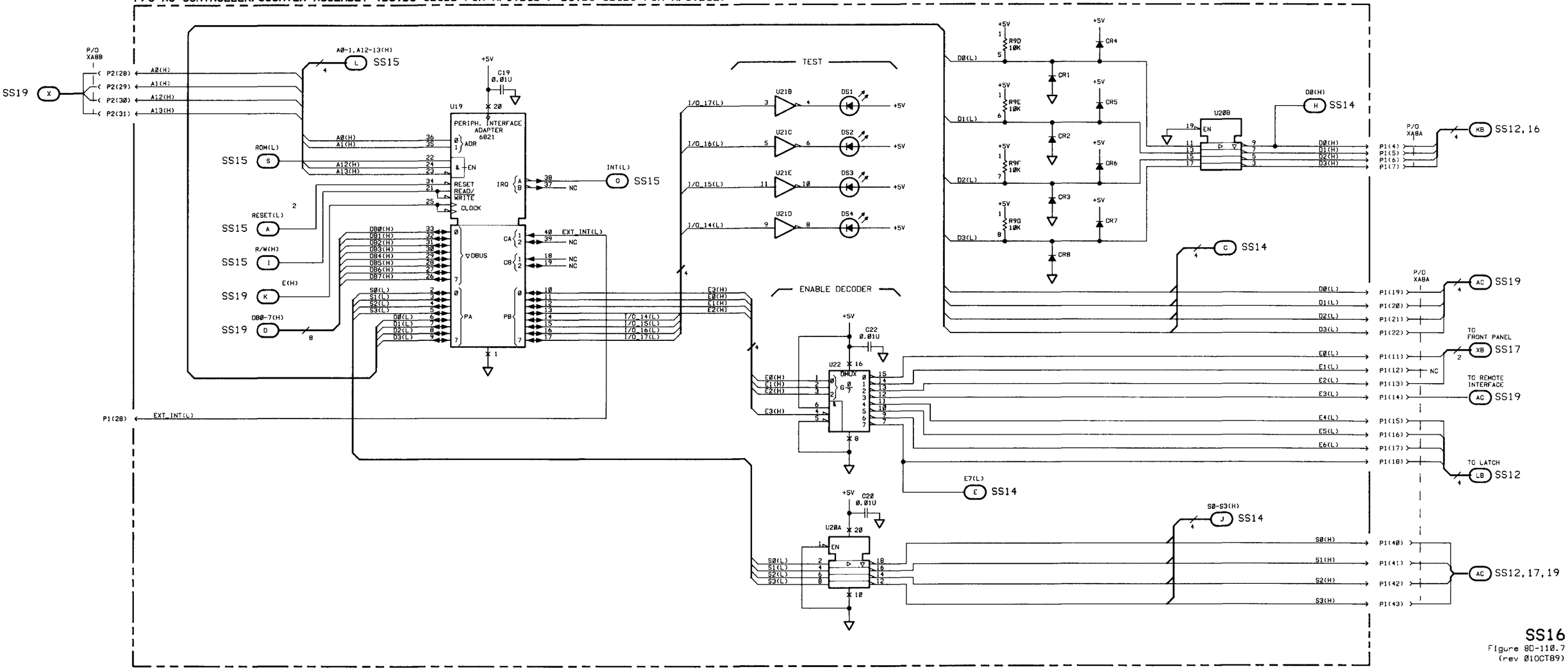
COMP	X	Y
C1	0.5	0.4
C2	3.6	0.4
C3	1.5	0.4
C4	3.6	1.2
C5	2.5	0.4
C6	1.5	2.1
C7	2.5	1.2
C8	0.5	2.1
C9	0.5	1.2
C10	3.5	2.1
C11	1.5	1.2
C12	2.5	2.1
C13	7.6	0.2
C14	10.3	0.3
C15	10.9	2.2
C16	10.9	0.3
C17	9.9	2.2
C18	11.7	0.4
C19	7.1	0.6
C20	4.6	2.1
C21	4.5	0.4
C22	4.7	1.2
C27	1.9	2.7
C28	1.9	3.0
C29	3.4	0.1
C30	5.5	0.3
C31	8.9	0.4
C32	8.8	0.4
C33	2.6	2.8
C34	8.1	0.3
C35	10.8	0.1
C36	12.8	0.1
C37	6.6	3.0
C38	1.4	2.8
C39	6.8	3.2
C40	14.1	0.3
C41	9.3	0.6
CR1	6.0	2.4
CR2	6.1	2.4
CR3	6.2	2.4
CR4	6.0	1.9
CR5	6.1	1.9
CR6	6.2	1.9
CR7	6.4	1.9
CR8	6.4	2.4

COMP	X	Y
DS1	3.7	0.1
DS2	4.0	0.1
DS3	4.3	0.1
DS4	4.6	0.1
P1	4.1	3.6
P2	10.6	3.6
R1	1.8	2.6
R2	1.8	2.8
R3	4.7	0.9
R6	9.0	2.4
R7	5.5	0.1
R8	8.9	1.5
R9	7.7	0.7
S1	9.2	1.2
TP1	11.7	0.1
TP2	11.1	0.1
U1	0.7	0.7
U2	1.7	0.7
U3	2.7	0.7
U4	2.7	1.6
U5	0.7	1.6
U6	1.7	1.6
U7	3.8	0.7
U8	3.8	1.6
U9	1.7	2.5
U10	0.7	2.5
U11	3.8	2.5
U12	2.7	2.5
U13	11.8	0.6
U14	8.1	0.7
U15	10.1	0.6
U16	11.1	2.5
U17	10.9	0.6
U18	10.1	2.5
U19	6.9	0.7
U20	4.9	2.5
U21	4.7	0.7
U22	4.9	1.6

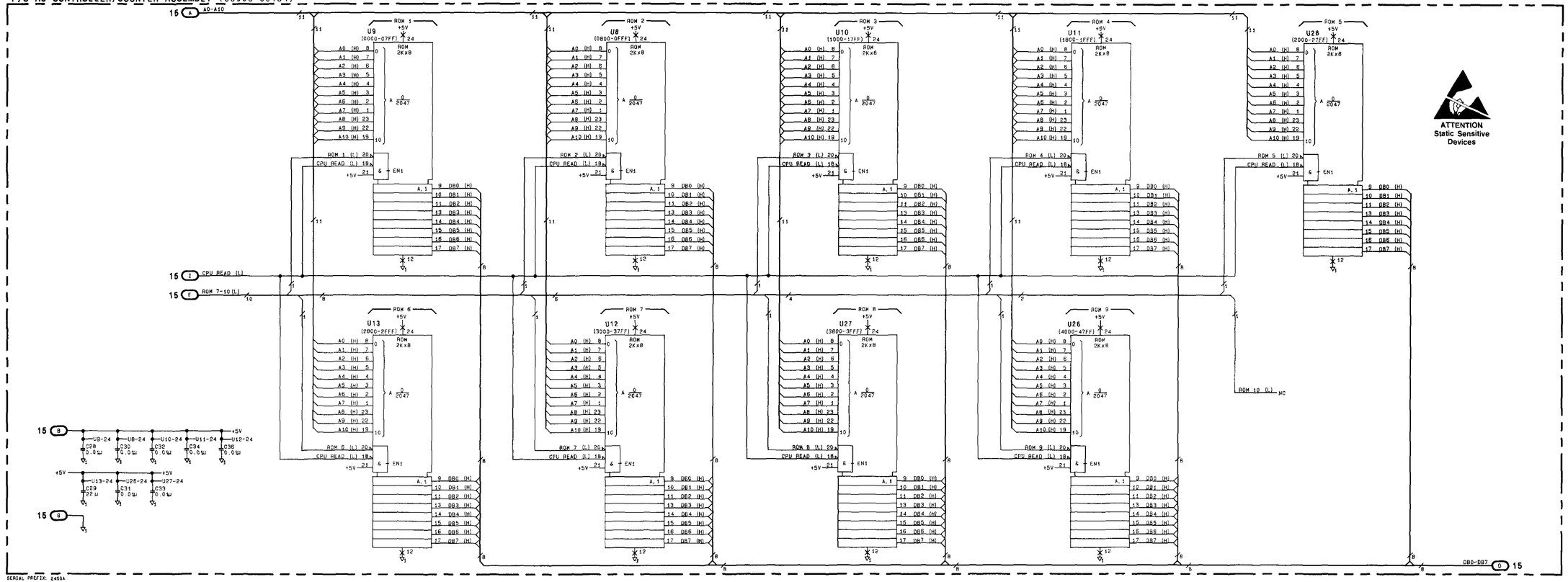
COMP	X	Y
VR1	4.9	-0.1
Y1	8.3	0.5

A8 Component Coordinates
2948A (HP8903B)
2946A (HP8903E)

P/O A8 CONTROLLER/COUNTER ASSEMBLY (08903-60300 FOR HP8903B / 08903-60301 FOR HP8903E)



SS16
Figure 8D-110.7
(rev 010CT89)



SERIAL PREFIX: 2450A

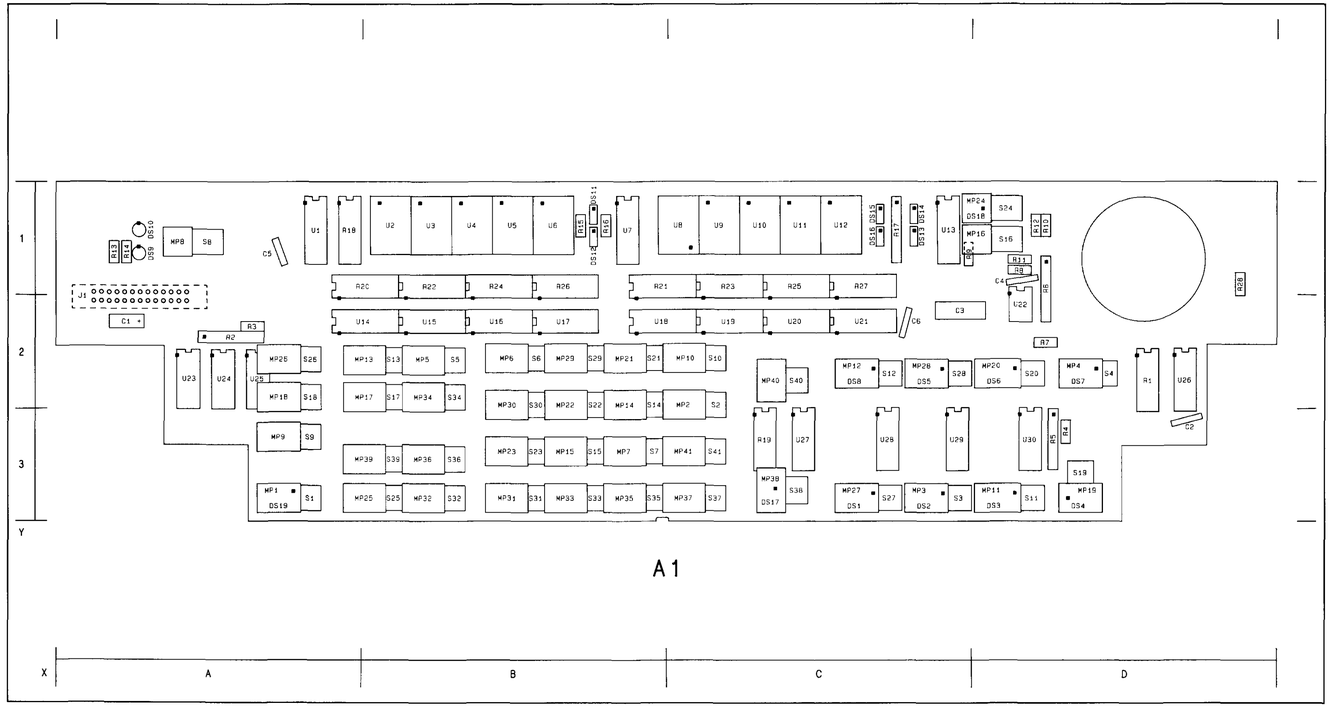


Figure 8D-112. SERVICE SHEET 17 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	A2	S18	A2				
C2	D3	S19	D3				
C3	E2	S20	D2				
C4	D1	S21	B2				
		S22	B2				
DS1	C3	S23	B3				
DS2	C3	S24	D1				
DS3	D3	S25	B3				
DS4	D3	S26	A2				
DS5	C2	S27	C3				
DS6	D2	S28	C2				
DS7	D2	S29	B2				
DS8	C2	S30	B2				
		S31	B3				
J1	A2	S32	B3				
		S33	B3				
MP1	A3	S34	B2				
MP2	C3	S35	B3				
MP3	C3	S36	B3				
MP4	D2	S37	C3				
MP5	B2	S38	C3				
MP6	B2	S39	B3				
MP7	B3	S40	C2				
MP8	A1	S41	C3				
MP9	A3						
MP10	C2	U22	D2				
MP11	D3	U23	A2				
MP12	C2	U24	A2				
MP13	B2	U25	A2				
MP14	B2	U26	D2				
MP15	B3	U28	C3				
MP16	D1	U29	C3				
MP17	A2	U30	D3				
MP18	A2						
MP19	D3						
MP20	D2						
MP21	B2						
MP22	B2						
MP23	B3						
MP24	D1						
MP25	B3						
MP26	A2						
MP27	C3						
MP28	C2						
MP29	B2						
MP30	B2						
MP31	B3						
MP32	B3						
MP33	B3						
MP34	B2						
MP35	B3						
MP36	B3						
MP37	C3						
MP38	C3						
MP39	B3						
MP40	C2						
MP41	C3						
R1	D2						
R2	A2						
R3	A2						
R4	D3						
R5	D3						
R6	D1						
R7	D2						
R8	D1						
R9	C1						
R10	D1						
R11	D1						
R12	D1						
S1	A3						
S2	C2						
S3	C3						
S4	D2						
S5	B2						
S6	B2						
S7	B3						
S8	A1						
S9	A3						
S10	C2						
S11	D3						
S12	C2						
S13	B2						
S14	B2						
S15	B3						
S16	D1						
S17	B2						

P/O A8 SEE REVERSE SIDE

Controller/ Counter-Read -Only Memory

SS16

NOTES

1. Switches S3 and S27 control the right and left HP/BP filters, respectively.

LOGIC LEVELS

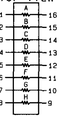
	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN	
> IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

A1R2,5,6
TOP VIEW

PIN NO.	1	2	3	4	5	6	7	8
	GND	A	B	C	D	E	F	G

A1U22
TOP VIEW

A1R1
TOP VIEW



Schematic General Information

CHANGES

All serial prefixes	**On the A1 schematic:** • **Line Labels** - In the center of the schematic to the left of U30 pin 14 and pin 15 change the line label "s2 (H)" to "e=2 (L)", and, "s=2 (L)" to "s2 (H)". To the left of U23C pin 8 locate "s=3 (H)" and change it to "s3 (H)".
2717A to 2742A	**On the A13 schematic:** • **08903-60192** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60192.
2742A and above	**On the A1 schematic:** • **08903-60166** - Use the partial schematic on page 8D-112.4. **On the A1 Component Locator:** • **08903-60166** - Use the partial component locator on page 8D-112.3. **On the A1 Component Coordinates:** • **DS20, R29** - Add DS20 A,2, and R29 A,2 to the coordinates table.
2813A and above	**On the A13 schematic:** • **08903-60292** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60292.

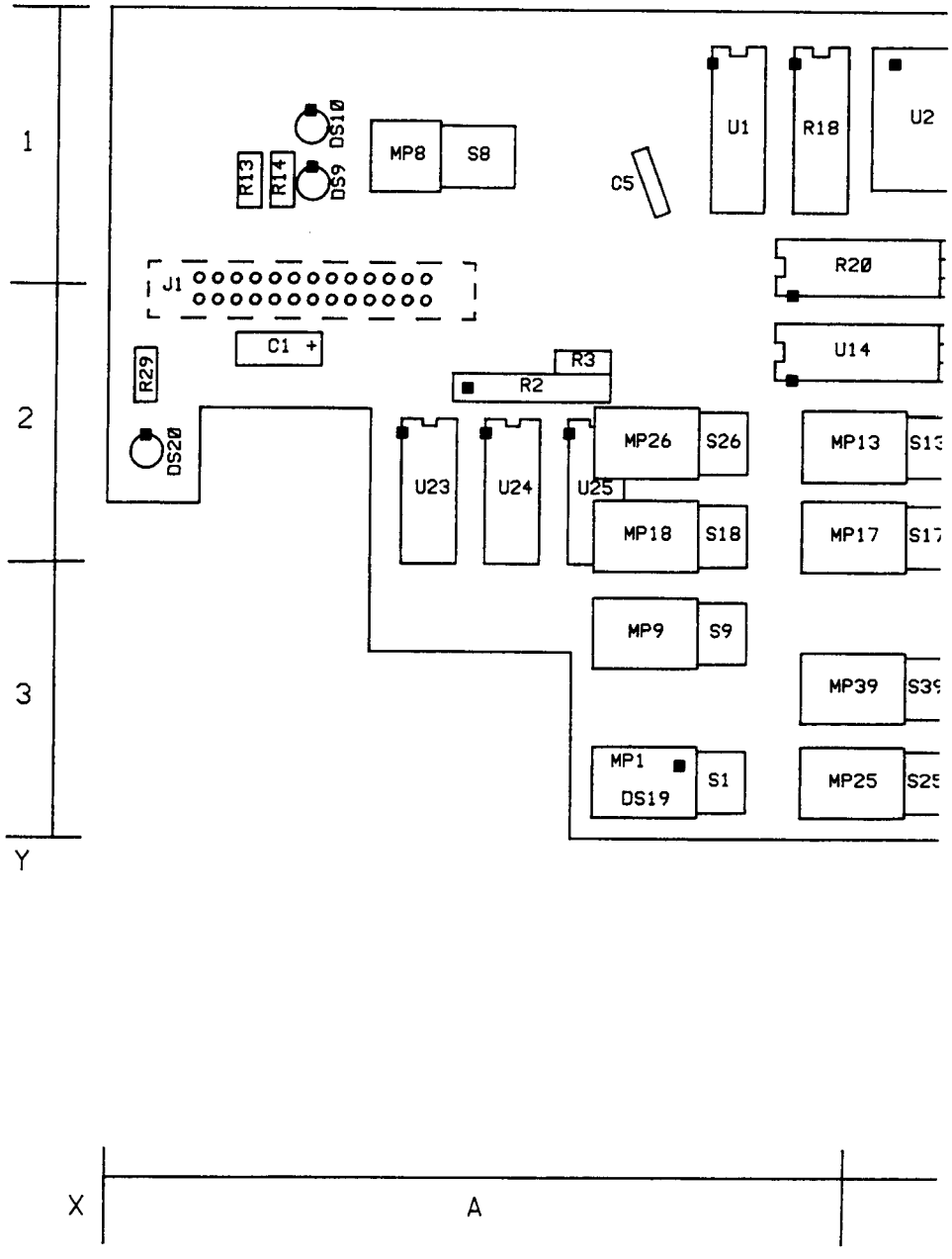


Figure 8D-112. SERVICE SHEET 17 INFORMATION

Figure 8D-112. Component Locator (2742A and above)

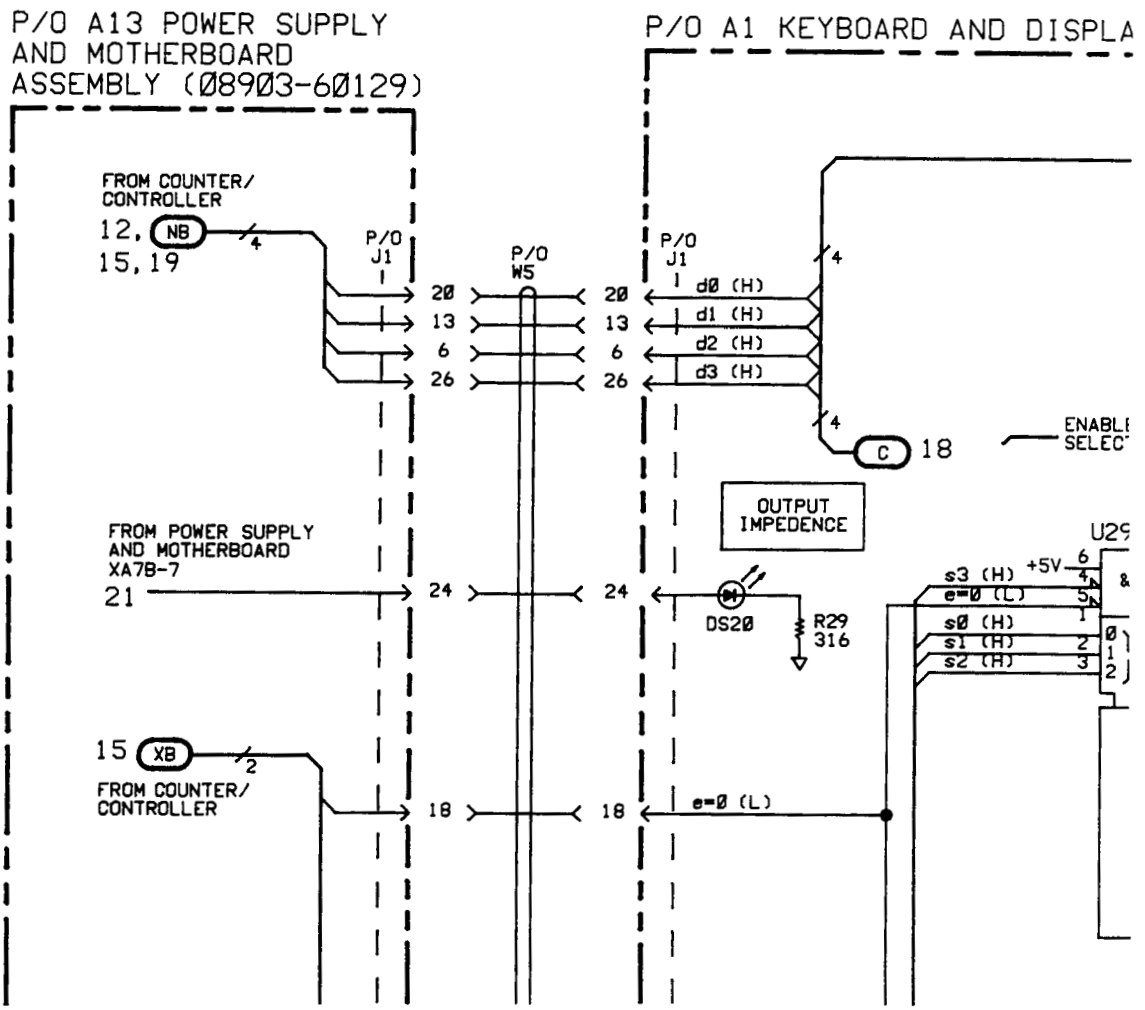
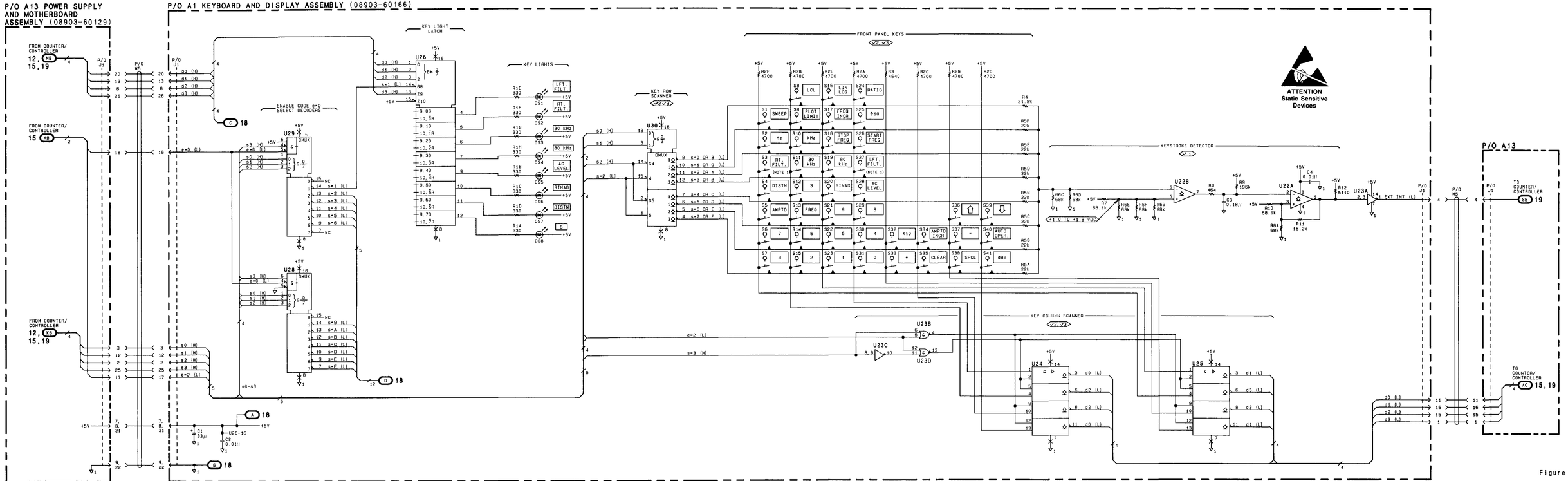


Figure 8D-112. (2742A and above)



SS17
Figure 8D-113
8D-113

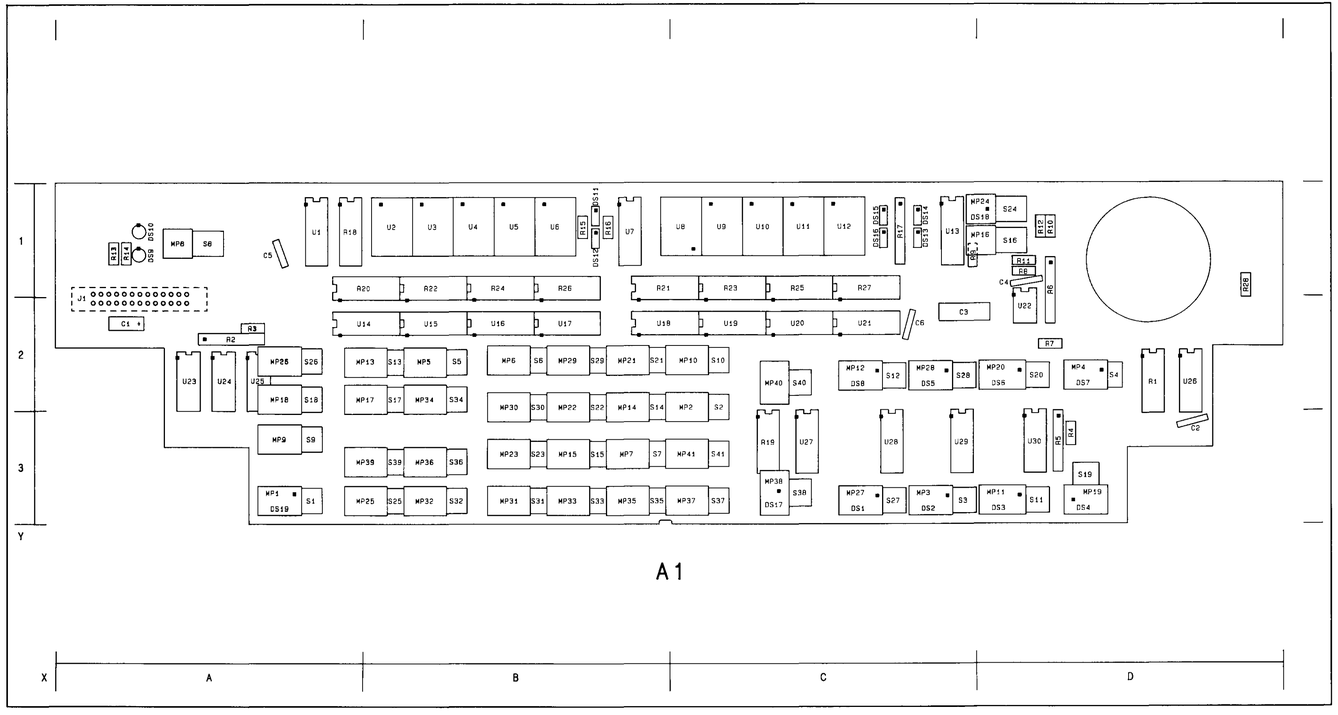


Figure 8D-114. SERVICE SHEET 18 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C5	A1						
C6	C2						
DS9	A1						
DS10	A1						
DS11	B1						
DS12	B1						
DS13	C1						
DS14	C1						
DS15	C1						
DS16	C1						
DS17	C3						
DS18	C1						
DS19	A3						
R13	A1						
R14	A1						
R15	B1						
R16	B1						
R17	C1						
R18	A1						
R19	C3						
R20	B1						
R21	B1						
R22	B1						
R23	C1						
R24	B1						
R25	C1						
R26	B1						
R27	C1						
R28	D1						
U1	A1						
U2	B1						
U3	B1						
U4	B1						
U5	B1						
U6	B1						
U7	B1						
U8	C1						
U9	C1						
U10	C1						
U11	C1						
U12	C1						
U13	C1						
U14	B2						
U15	B2						
U16	B2						
U17	B2						
U18	B2						
U19	C2						
U20	C2						
U21	C2						
U27	C3						

P/O A1 SEE REVERSE SIDE — Keyboard and Display-Keyboard Circuits — SS17

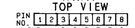
NOTES

1. Socket for U8 is upside down.

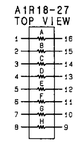
LOGIC LEVELS

	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN	
> IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

A1R17 TOP VIEW



A1R18-27 TOP VIEW



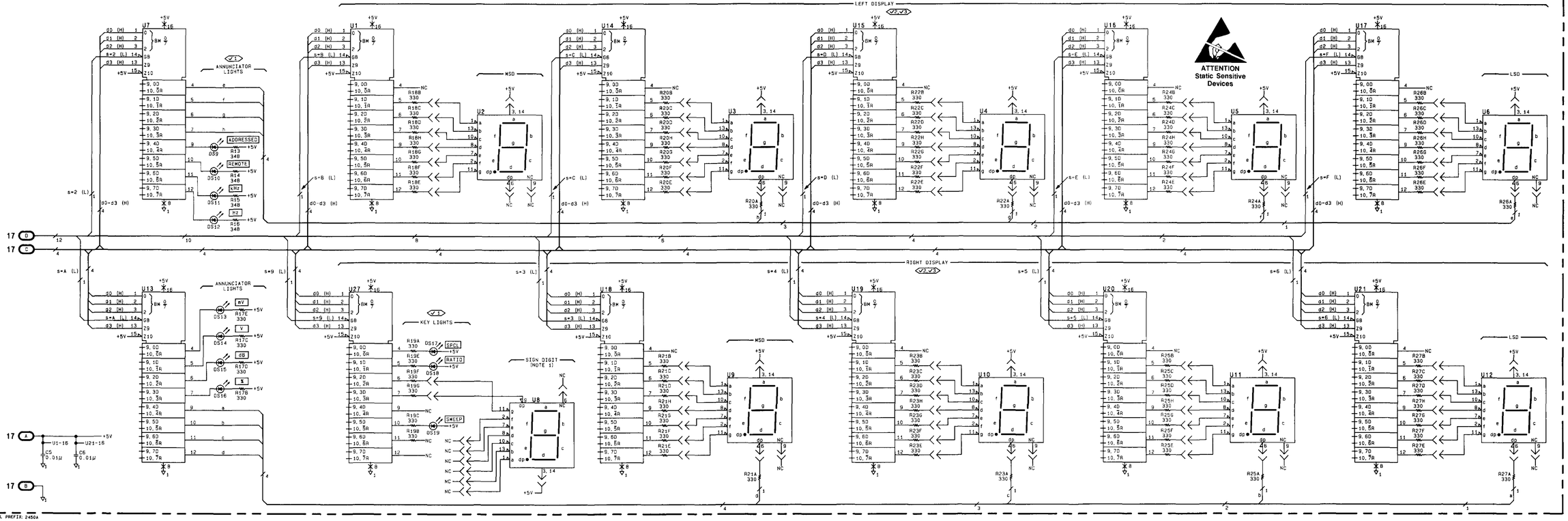
Schematic General Information

CHANGES

All Serial Prefixes

Schematic General Information:

- **Notes** - On page 8D-114, Change Note 1 to read: "Display Orientation: A1U8 (HP part 5082-7651) is part of a matched display set HP part 1990-0753. It is mounted upside down (relative to displays U2-U6 and U9-U12) with the two decimal points oriented towards the top edge of A1."


LEFT DISPLAY
RIGHT DISPLAY
ANNUNCIATOR LIGHTS
KEY LIGHTS
MSD
LSD
SIGN DIGIT (NOTE 1)
ATTENTION
Static Sensitive
Devices
ADDRESSED
REMOTE
kHz
Hz
mV
V
dB
%
SPCL
RATIO
SWEEP

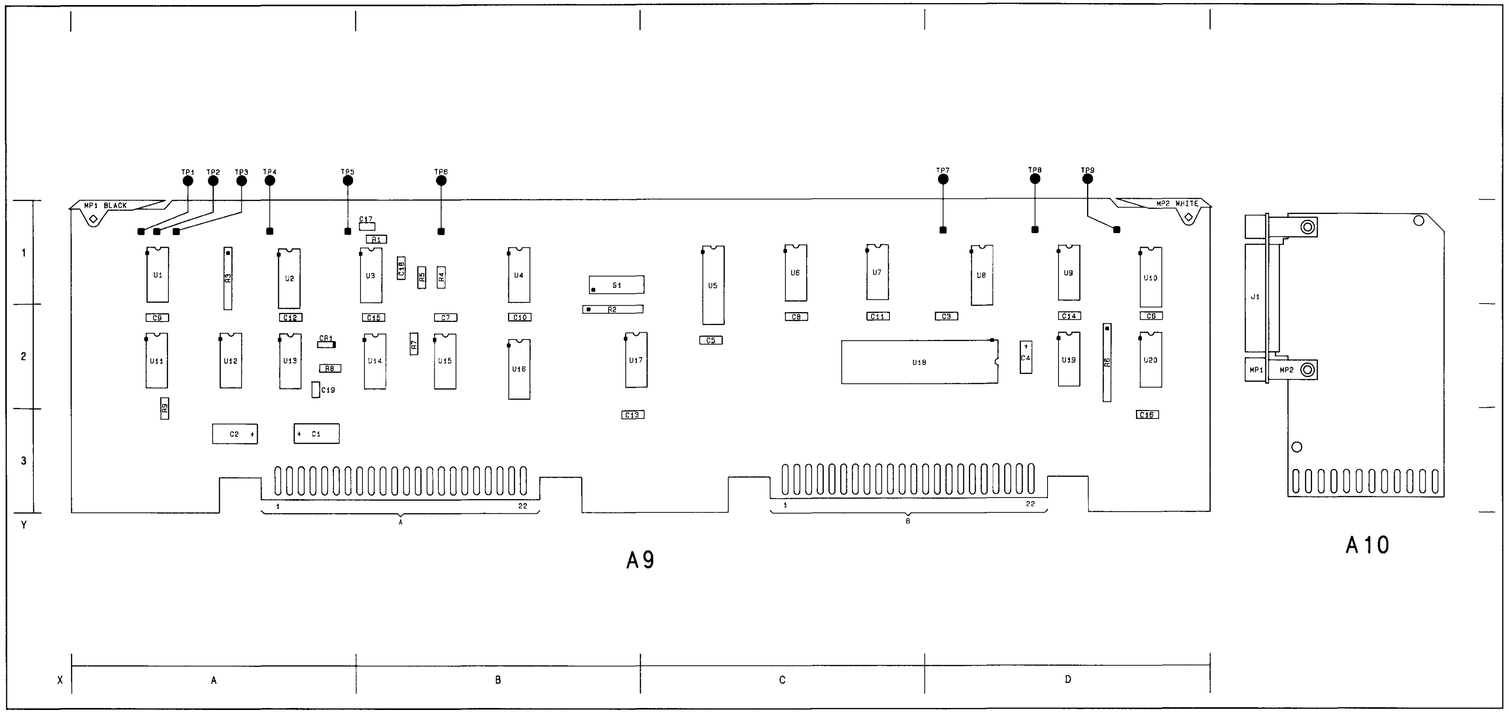


Figure 8D-116. SERVICE SHEET 19 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	A3						
C2	A3						
C3	D2						
C4	D2						
C5	C2						
C6	D2						
C7	B2						
C8	C2						
C9	A2						
C10	B2						
C11	C2						
C12	A2						
C13	B3						
C14	D2						
C15	B2						
C16	D3						
C17	B1						
C18	B1						
C19	A2						
CR1	A2						
R1	B1						
R2	B2						
R3	A1						
R4	B1						
R5	B1						
R6	D2						
R7	B2						
R8	A2						
R9	A2						
S1	B1						
TP1	A1						
TP2	A1						
TP3	A1						
TP4	A1						
TP5	A1						
TP6	B1						
TP7	D1						
TP8	D1						
TP9	D1						
U1	A1						
U2	A1						
U3	B1						
U4	B1						
U5	C1						
U6	C1						
U7	C1						
U8	D1						
U9	D1						
U10	D1						
U11	A2						
U12	A2						
U13	A2						
U14	B2						
U15	B2						
U16	B2						
U17	B2						
U18	C2						
U19	D2						
U20	D2						

P/O A1 Keyboard and Display-Display Circuits **SS18**

SEE REVERSE SIDE

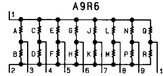
NOTES

1. Chassis ground is achieved by mechanical contact through screws holding the pc boards.

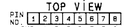
LOGIC LEVELS

	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

A9R6



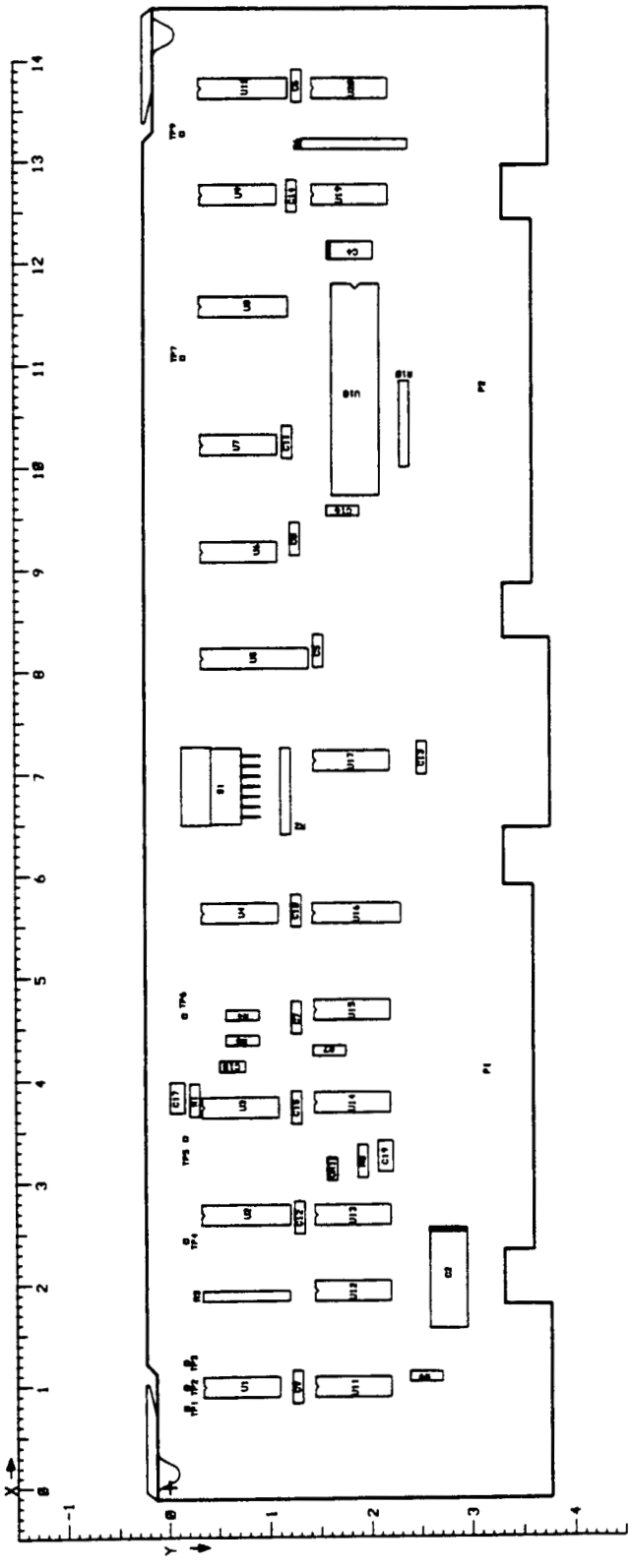
A9R2,3 TOP VIEW



Schematic General Information

CHANGES

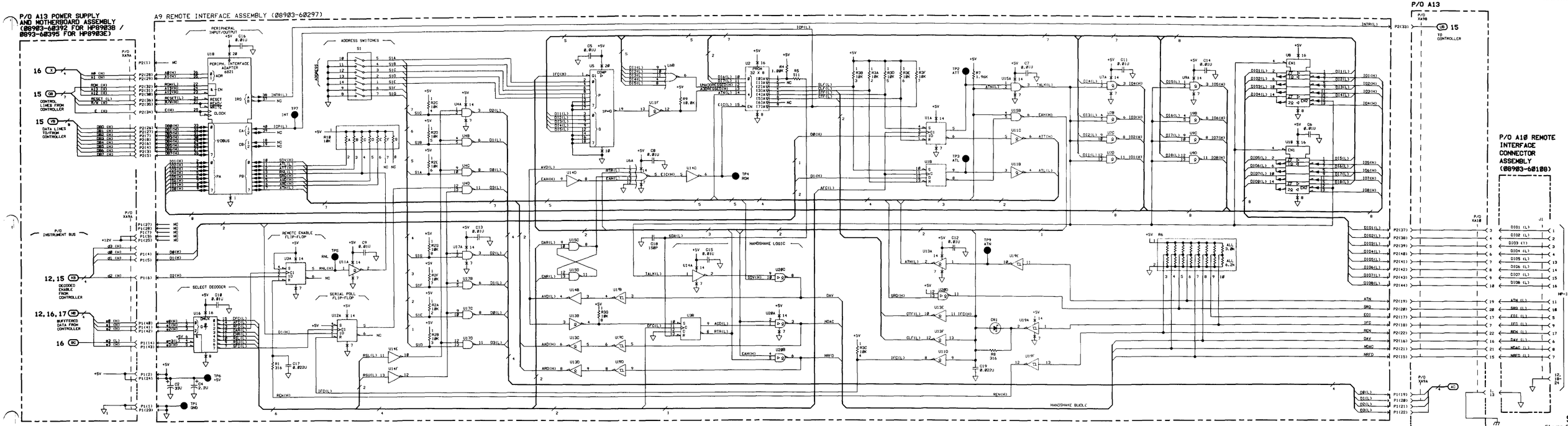
2948A and above	**On the A9 schematic:** • **08903-60297** - Use the new schematic foldout on page 8D-116.7, SS19 with the revision date of rev.01OCT89. **On the A9 Component Locator:** • **08903-60297** - Use the new A9 Component Locator on page 8D-116.4 with the revision date of rev.01OCT89. **On the A9 Component Coordinates:** • **08903-60297** - Use the new A9 Component Coordinates on page 8D-116.5 with the revision date of rev.01OCT89.



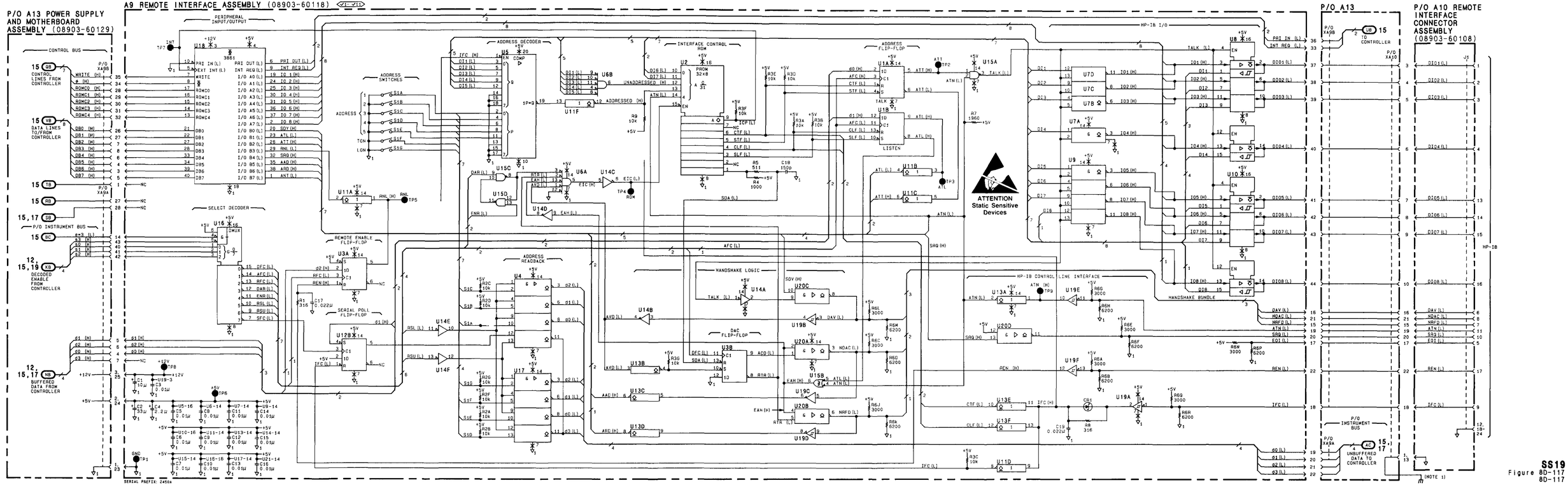
A9 Component Locator
2948A (HP8903B)
2946A (HP8903E)

COMP	X	Y	COMP	X	Y	COMP	X	Y
C2	2.6	2.8	U6	9.0	0.4			
C4	12.1	1.5	U7	10.1	0.4			
C5	8.0	1.5	U8	11.4	0.4			
C6	14.0	1.3	U9	12.5	0.4			
C7	4.8	1.3	U10	13.6	0.4			
C8	9.1	1.3	U11	0.8	1.5			
C9	0.8	1.3	U12	1.8	1.5			
C10	5.4	1.3	U13	2.5	1.5			
C11	10.0	1.2	U14	3.6	1.5			
C12	2.4	1.3	U15	4.5	1.5			
C13	6.9	2.5	U16	5.5	1.5			
C14	12.4	1.3	U17	7.0	1.5			
C15	4.0	1.3	U18	11.7	1.6			
C16	9.6	2.0	U19	12.5	1.5			
C17	3.6	0.1	U20	13.6	1.5			
C18	4.1	0.8						
C19	3.0	2.1						
CR1	3.3	1.6						
P1	4.1	3.6						
P2	10.6	3.6						
R1	3.6	0.3						
R2	6.5	1.2						
R3	1.9	0.4						
R4	4.6	0.5						
R5	4.4	0.5						
R6	13.2	1.4						
R7	4.3	1.4						
R8	3.0	1.9						
R9	1.1	2.3						
R10	10.8	2.4						
S1	6.6	0.9						
TP1	0.8	0.2						
TP2	1.0	0.2						
TP3	1.2	0.2						
TP4	2.4	0.2						
TP5	3.4	0.2						
TP6	4.6	0.2						
TP7	11.1	0.2						
TP9	13.3	0.2						
U1	0.8	0.4						
U2	2.5	0.4						
U3	3.6	0.4						
U4	5.5	0.4						
U5	8.0	0.4						

A9 Component Coordinates
2948A (HP8903B)
2946A (HP8903E)



SS19
Figure 80-116.7
(rev 010CT89)


P/O A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY (08903-60129)
A9 REMOTE INTERFACE ASSEMBLY (08903-60118)
P/O A13
P/O A10 REMOTE INTERFACE CONNECTOR ASSEMBLY (08903-60108)
CONTROL BUS
DATA LINES TO/FROM CONTROLLER
P/O INSTRUMENT BUS
BUFFERED DATA FROM CONTROLLER
DECODED ENABLE FROM CONTROLLER
CONTROL LINES FROM CONTROLLER
UNBUFFERED DATA TO CONTROLLER
HP-IB I/O
HP-IB CONTROL LINE INTERFACE
HANDSHAKE BUNDLE
PERIPHERAL INPUT/OUTPUT
ADDRESS DECODER
INTERFACE CONTROL ROM
ADDRESS FLIP-FLOP
ADDRESS SWITCHES
SELECT DECODER
REMOTE ENABLE FLIP-FLOP
SERIAL POLL FLIP-FLOP
ADDRESS READBACK
HANDSHAKE LOGIC
DAC FLIP-FLOP
TALKER
LISTENER
ATTENTION Static Sensitive Devices
SERIAL PREFIX: 2450A
SS19
Figure 8D-117
8D-117

SERVICE SHEET BD5---Power Supplies Block Diagram

PRINCIPLES OF OPERATION

Power Supplies (A11 and A13)

The four regulated supplies are: +15V, −15V, +12V, and +5V. The +15V and −15V supplies are used primarily to power the analog circuits. The +5V supply is used to power most of the relays and digital circuits. The +12V supply powers the main Controller ICs. The inputs for the +15V, −15V, and +12V supplies are obtained from one secondary winding of the power transformer, and the +5V supply (the supply drawing the most current) is obtained from another. The supplies are independently referenced except the +5V supply, which is referenced from the +15V supply and also requires the −15V supply to operate properly. Each supply has an indicator LED.

TROUBLESHOOTING

General

A procedure for checking the power supplies follows. Before performing the check, perform all the checks on Service Sheet BD1.

⟨√1⟩ Power Supply Check

1. Key in 41.0 SPCL to initialize the instrument. Key in S (Shift) DC LEVEL. Set the INPUT switch to ground. Observe the four green power supply LEDs on the A13 Power Supply and Motherboard Assembly. The LEDs should be on. If faulty, see Service Sheet 20.

CAUTION

MOS and CMOS ICs can be damaged by static charges and circuit transients. Do not remove the A8 Controller/Counter Assembly or the A9 Remote Control Interface Assembly while power is applied to the instrument.

NOTE

When removing assemblies to check for shorts, switch the instrument off before removing the assembly and back on when testing the supply. This will unlatch any crowbar SCRs that may have fired.

Hint: If a short is suspected, remove assemblies one at a time and observe the four power supply LEDs. An extinguished LED will light when the short is removed from the supply. The A1 Keyboard and Display Assembly can be disconnected by unplugging the wide ribbon cable plugged into it.

Hint: The +5V supply is referenced from the +15V supply and also depends on the −15V supply. The +15V supply and +12V supply share a common transformer and secondary fuse.

2. Connect the HIGH INPUT to A13TP3 through TP6. The amplitude display for each test point should be within the limits shown in Figure 8E-101. If faulty, see Service Sheet 20.

SERVICE SHEET 20---A13 Power Supply and Motherboard Assembly

PRINCIPLES OF OPERATION

General

The Power Supply has four outputs: +15V, −15V, +12V, and +5V. The +15V and −15V supplies are used to run all operational amplifiers and most other analog circuits. The +12V supply is used by the three microprocessor ICs (A8U5, A8U6, and A9U18). The +5V supply powers most of the digital circuits, all of the relays, and some of the analog circuits.

Transformer Primary Circuits

The input to the primary of the power transformer (chassis part T1) is through the four-voltage, filtered Line Power Module (A14) which permits operation from nominal line voltages of 100, 120, 200, and 240V at 48 to 66 Hz. (400 Hz is also permitted for 100 and 120V.) Matching of the primary winding to the input line voltage is accomplished by positioning of the printed circuit card A14TB1.

Regulators and Protection Circuits

A single, center-tapped secondary of the power transformer supplies the +15V, −15V, and +12V Regulators. The secondary is full-wave rectified and filtered by CR1, CR2, and C1 for the +15V and +12V Regulators and by CR3, CR4, and C2 for the −15V Regulator.

The Input Over-Voltage Protection circuit, consisting primarily of VR1, VR2, and Q3, protects the Power Supply and, indeed the rest of the instrument when the power line is connected to 200 or 220V and the power line printed circuit board is set for 100 or 120V. In that case VR1 and VR2 conduct, triac Q3 fires, and the primary fuse (chassis part F1) blows. C12 prevents Q3 from firing on short-duration line transients.

An independent, center-tapped secondary of the transformer supplies the +5V Regulator. The secondary is full-wave rectified and filtered by CR5A, CR5B, and C3.

All regulators are series-pass types. The +15V, −15V, and +12V Regulators (U2 and chassis parts U1 and U2) are three-terminal ICs with internal short-circuit, over-voltage, and reverse-voltage protection. All regulators, however, are further protected with input fuses. Capacitors at the inputs and outputs of the regulators (C4, C5, A11C1, A11C2, A11C3, and A11C4) prevent spurious oscillations.

The +5V Regulator is a discrete regulator. Chassis part Q1 is a Darlington, series-pass transistor pair driven by Q1. The output of the regulator is sensed by U1B and compared to a 5.2V reference derived from the +15V supply through voltage divider R12 and R13. Hence, operation of the +5V supply depends on the +15V supply. U1B drives Q1 which drives the series-pass transistor to maintain a constant +5.2V at the regulator's output.

U1A senses both the output current (through R5) and voltage for the +5V supply and folds back the supply during a fault. Foldback begins at about 4A. Short-circuit current is about 1A. C6 and R8 frequency compensate the regulator during foldback, and C7 and R11 during normal operation.

At the output of each supply is a reverse-voltage protection diode (CR11 through CR14), a supply status indicator, and an over-voltage protection circuit. The supply status indicators (DS1 through DS4) light when the voltage on the supply is high enough to cause the series reference diodes (VR3 through VR6) to conduct. Excessive output voltage will cause a reference diode (VR7 through VR10) to conduct and fire its respective SCR (Q2, Q4, Q5, or Q6). The SCR shorts the supply and initiates current foldback.

Impedence Selection Circuits

Serial prefixes 2742A and above: Special Function 47.X is used to select the output impedence of the source. When 47.0 SPCL is entered (this is the default condition at instrument turn-on or initialization via 40.0 or 41.0 SPCL) the output impedence is 600 Ω. Latch A7U26 pin 6 is low (approximately 0 Vdc) which turns off front panel LED A1DS20 (Service Sheet 17) causing the collector of A13Q7 to rise up to approximately +5 Vdc which turns off A6K4 (Service Sheet 11) adding 550 Ω to the output impedence of 50 Ω. When 47.1 SPCL is entered the output impedence is set to 50 Ω. Latch A7U26 pin 6 goes high (approximately +5 Vdc) which turns on front panel LED A1DS20 (Service Sheet 17) causing the collector of A13Q7 to go to approximately +0 Vdc which turns on A6K4 (Service Sheet 11) shorting out the 550 Ω in series with the output impedence of 50 Ω.

TROUBLESHOOTING

General

Procedures for checking the Power Supply and Motherboard Assembly are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are shown on the schematic also inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩.

Equipment

Digital Multimeter	HP 3455A
Oscilloscope	HP 1740A

⟨√1⟩ Power Supply Check—Blown Line Fuse

1. Check that the line voltage selection card (A14TB1) and line fuse (F1) are matched to the power source.

2. With LINE set to OFF, unplug the plug on the secondary of T1 which plugs into A13J2. Replace the blown fuse. Set LINE to ON. If the fuse blows, check the A14 Line Power Assembly, S1, and T1.

3. Switch LINE to OFF. Measure the resistance between pins 4 and 5 of A13J2. The resistance should be greater than 100 kΩ.

4. Measure the resistance between pins 2 and 3 of A13J2. The resistance should be greater than 100 kΩ.

5. Measure the resistance across A13C1, C2, and C3. After allowing the capacitors to be charged by the ohmmeter, the resistance should be greater than 2 kΩ in each case.

Hint: If the resistance is correct but the F1 still blows when the instrument is powered up, the fault is probably in the Input Over-Voltage Protection circuit. Check A13VR1, VR2, and Q3.

⟨√2⟩ Power Supply Check—Blown Regulator Fuses

1. With LINE set to OFF, unplug all board assemblies (including the Keyboard and Display Assembly). Replace the blown fuse. Switch LINE to ON. If the fuse (A11F1, F2, or F3) blows, the problem lies with the power supply itself.

Hint: A short on the output of the +5V, +15V, or −15V supply will blow a fuse.

Hint: If the +15V and −15V supplies work but A11F2 blows, the problem is likely caused by a fault in the Over-Current Protection circuit or shorted transistors.

2. Switch LINE to OFF. Measure the resistance from A13TP3 (+5V), A13TP4 (+12V), A13TP5 (+15V), and A13TP6 (−15V) to A13TP2 (GND A). The resistance should be greater than 3 kΩ.

⟨√3⟩ Power Supply Check—General Integrity

1. With the LINE switch ON, check the dc voltages on A13TP3 (+5V), A13TP4 (+12V), A13TP5 (+15V), and A13TP6 (−15V). The voltage should be within the limits shown on the schematic diagram.

Hint: If the +5V supply is out of limits, check pin 5 of U1B. Check that pin 1 of U1A is between +12 and +15 Vdc (over-current protection unactivated).

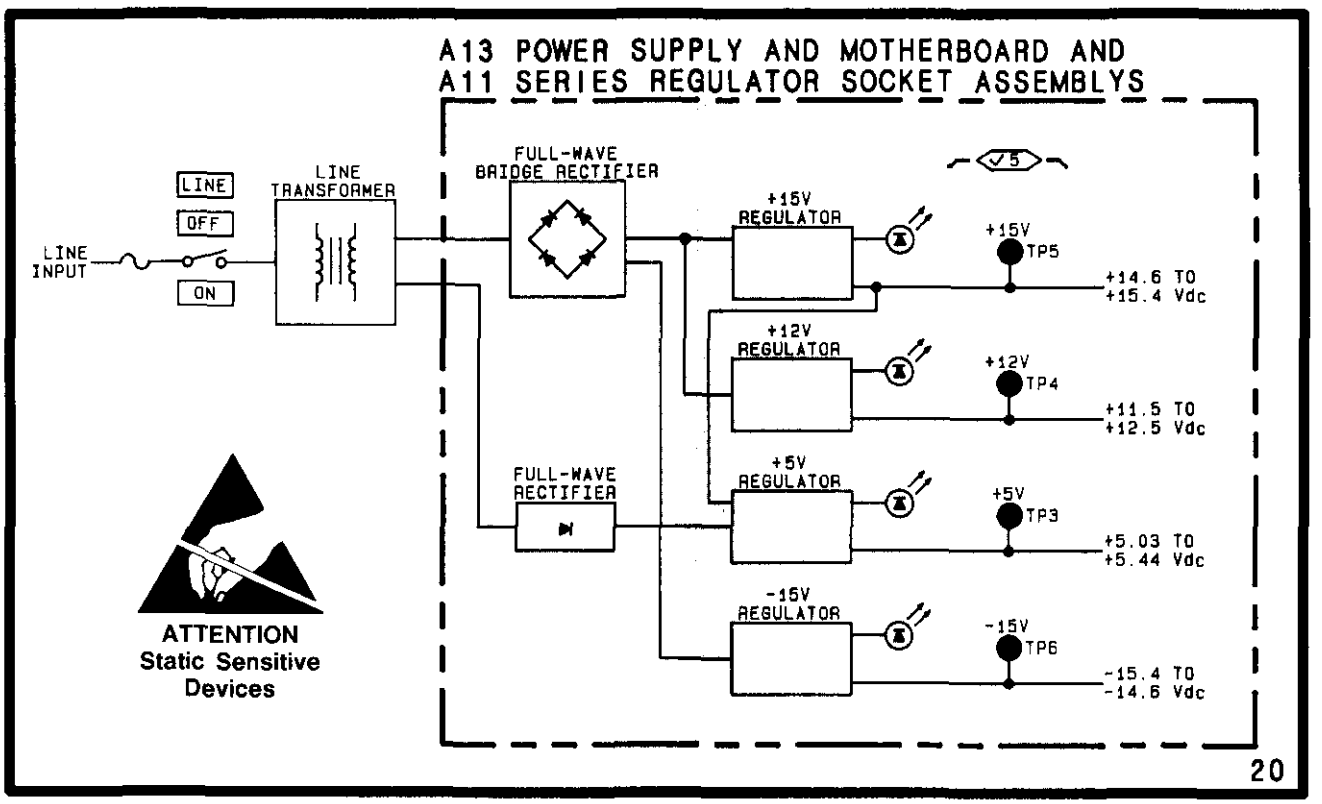
2. With an oscilloscope, measure the ripple at the outputs of the Full-Wave Rectifier. (Fuses A11F1, F2, and F3 provide convenient test points.) Ripple should be less than 1.5V and should be at double the line frequency.

Hint: For reference, typical dc level and ripple is as shown in Table 8E-1.

Table 8E-1. Typical DC Level and Ripple, ⟨√3⟩ *Step 2*

Unregulated Input	Typical Level (Vdc)	Typical Ripple (Vpp)
+15V	+23	0.6
+5V	+8	0.8
−15V	−23	0.6

3. Measure the ripple at the supply outputs. Ripple should be less than 2 mVpp.



BD5
Figure 8E-101
8E-101

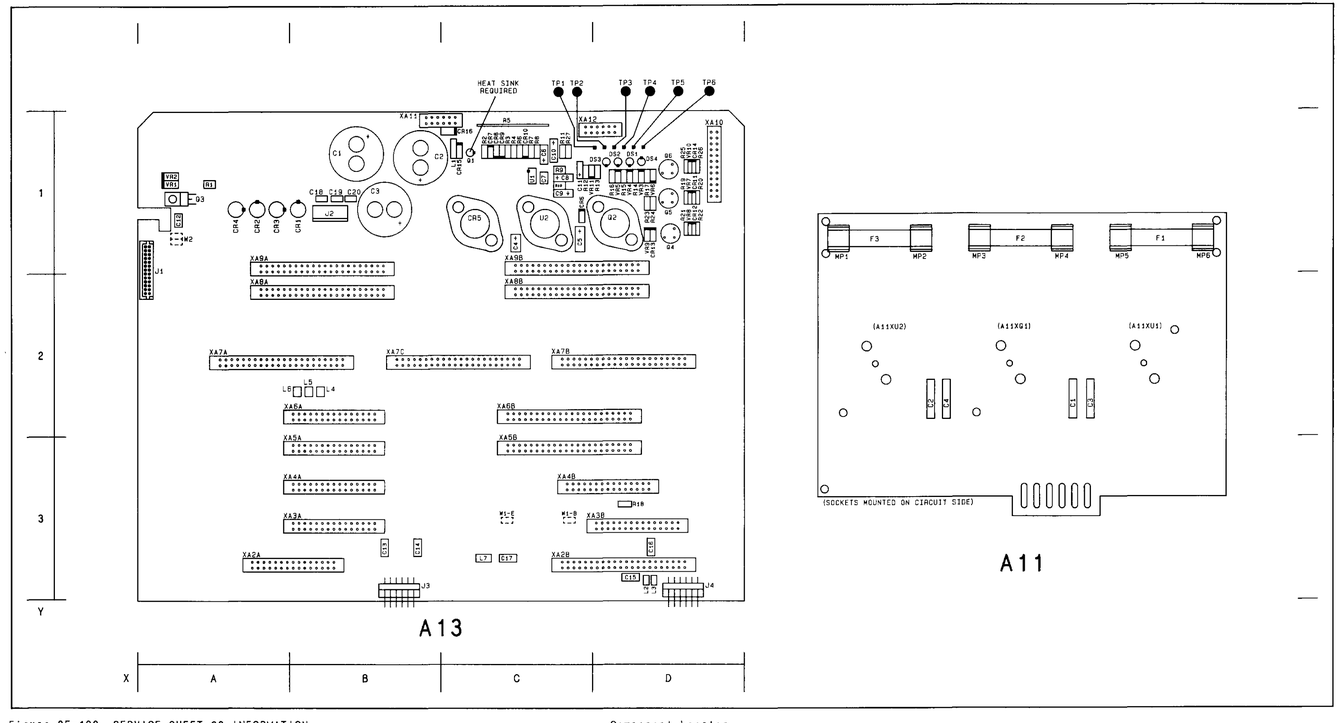


Figure 8E-102. SERVICE SHEET 20 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	B1	VR1	A1				
C2	B1	VR2	A1				
C3	B1	VR3	D1				
C4	C1	VR4	D1				
C5	C1	VR5	D1				
C6	C1	VR6	D1				
C7	C1	VR7	D1				
C8	C1	VR8	D1				
C9	C1	VR9	D1				
C10	C1	VR10	D1				
C11	C1	VR11	C1				
C12	A1						
C18	B1	XA10	D1				
C19	B1	XA11	B1				
C20	B1	XA12	C1				
CR1	B1						
CR2	A1						
CR3	A1						
CR4	A1						
CR5	C1						
CR6	C1						
CR7	C1						
CR8	C1						
CR9	C1						
CR10	C1						
CR11	D1						
CR12	D1						
CR13	D1						
CR14	D1						
CR15	C1						
CR16	C1						
DS1	D1						
DS2	D1						
DS3	D1						
DS4	D1						
J2	B1						
L1	C1						
Q1	C1						
Q2	D1						
Q3	A1						
Q4	D1						
Q5	D1						
Q6	D1						
R1	A1						
R2	C1						
R3	C1						
R4	C1						
R5	C1						
R6	C1						
R7	C1						
R8	C1						
R9	C1						
R10	C1						
R11	C1						
R12	C1						
R13	D1						
R14	D1						
R15	D1						
R16	D1						
R17	D1						
R18	D1						
R19	D1						
R20	D1						
R21	D1						
R22	D1						
R23	D1						
R24	D1						
R25	D1						
R26	D1						
R27	C1						
TP1	D1						
TP2	D1						
TP3	D1						
TP4	D1						
TP5	D1						
TP6	D1						
U1	C1						
U2	C1						

Power Supply

BD5

SEE REVERSE SIDE

NOTES

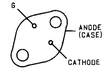
1. Value of F1 is 1.50A for 110/120V, and 0.75A for 220/240V.
2. Chassis ground is achieved through mechanical contact of the frame holding screws connected to the PC board.
3. A13R5 is a 4.8 cm (1.9 in.) strip of nickle copper.
4. Q4,5 and 6 do not have the square pad (cathode) on the actual PC motherboard. Refer to the component diagrams below.

A13Q3

U1,2,A13CR5,U2
BOTTEM VIEW

Q4,5,6
TOP VIEW

A13Q2

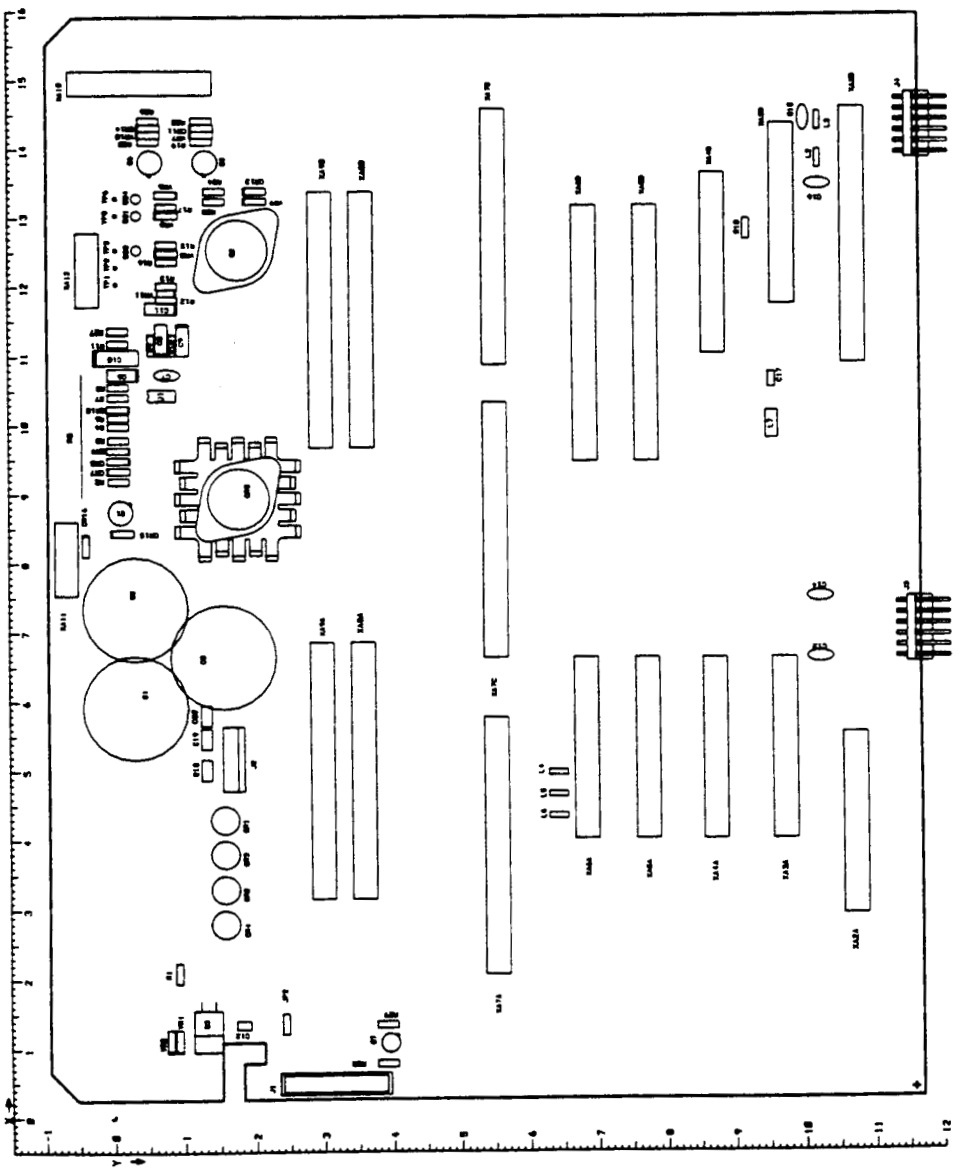


A13CR5

Schematic General Information

CHANGES

All serial prefixes	**On the A13 Component Locator:** • **C1** - Mark C1 positive on the end closest to MP4. Mark C2, C3, and, C4 positive on the end closest to the fingers of the board.
2717A to 2742A	**On the A13 schematic:** • **08903-60192** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60192. **On the A13 Component Locator:** • **J1** - In the upper left section of the component locator locate J1, then at the lower right of J1 add in order: R28, Q7, and, R29. • **JP1-B, JP1-E** - In the lower center of the component locator locate C14, then between C14 and L7 add JP1-B and JP1-E in order. **On the A13 Component Coordinates:** • **08903-60192** - In alpha numeric order add JP1-B (B-3), JP1-E (C,3), Q7 (2,A), R28 (2,A), and, R29 (2,A).
2813A and above	**On the A13 schematic:** • **08903-60292** - Change the part number of the A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY to 08903-60292.
2922A and above	**On the A13 schematic:** • **R20, R22, R26** - On the far right hand side of the schematic locate and change the value of R20, R26 to 133 ohms, and, R22 to 100 ohms.



A13 Component Locator
2948A (HP8903B)
2946A (HP8903E)

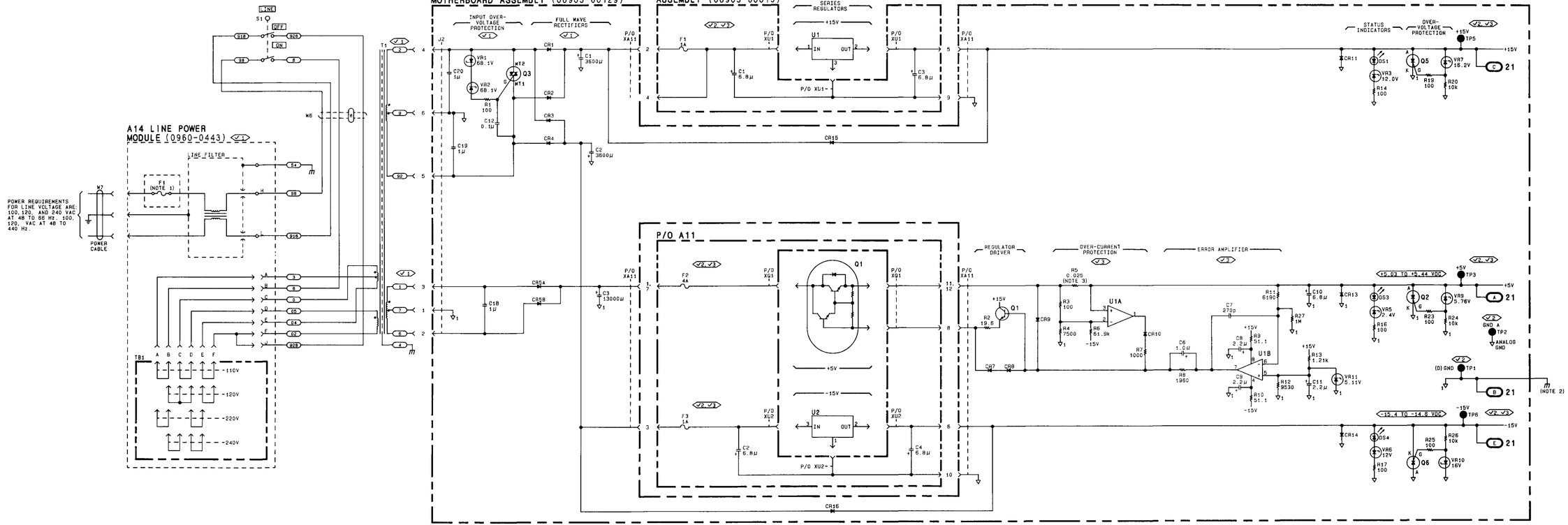
COMP	X	Y
C1	5.5	-11.5
C2	7.0	-11.0
C3	6.5	-10.0
C4	9.7	-9.6
C5	11.2	-9.8
C6	10.3	-11.1
C7	10.3	-10.7
C8	10.6	-10.8
C9	11.2	-10.6
C10	10.6	-11.9
C11	11.3	-10.6
C12	1.0	-9.8
C13	6.2	-1.2
C14	7.1	-1.2
C15	13.9	-1.5
C16	13.1	-1.2
C17	10.1	-2.0
C18	4.6	-10.3
C19	5.1	-10.3
C20	5.4	-10.3
CR1	3.9	-10.0
CR2	2.9	-10.0
CR3	3.4	-10.0
CR4	2.4	-10.0
CR5	9.0	-9.4
CR6	11.4	-10.2
CR7	9.0	-11.7
CR8	9.1	-11.3
CR9	9.3	-11.3
CR10	9.8	-11.3
CR11	13.9	-10.5
CR12	13.9	-9.8
CR13	13.0	-9.7
CR14	13.9	-11.3
CR15	8.1	-11.7
CR16	8.1	-12.0
DS1	12.7	-11.2
DS2	12.4	-11.2
DS3	12.2	-11.2
DS4	12.9	-11.2
J1	0.1	-9.0
J2	4.4	-9.9
J3	6.2	-0.2
J4	13.5	-0.2

COMP	X	Y
L1	7.9	-11.8
L2	13.4	-1.3
L3	14.0	-1.3
L4	4.6	-5.1
L5	4.3	-5.1
L6	4.0	-5.1
L7	9.3	-2.0
Q1	8.3	-11.5
Q2	12.6	-9.4
Q3	1.3	-10.2
Q4	13.4	-9.5
Q5	13.4	-10.2
Q6	13.4	-11.0
Q7	0.7	-7.6
R1	1.5	-10.7
R2	8.8	-11.7
R3	9.4	-11.7
R4	9.6	-11.7
R6	9.7	-11.7
R7	10.0	-11.7
R8	10.2	-11.7
R9	10.6	-11.0
R10	10.6	-10.7
R11	10.8	-11.7
R12	11.4	-10.6
R13	11.6	-10.6
R14	12.5	-11.0
R15	12.2	-11.0
R16	12.0	-11.0
R17	12.8	-11.0
R18	12.2	-2.4
R19	13.7	-10.1
R20	14.0	-10.1
R21	13.7	-9.8
R22	14.0	-9.8
R23	12.9	-10.3
R24	13.0	-10.3
R25	13.7	-11.3
R26	14.0	-11.3
R27	11.0	-11.7
R28	0.4	-7.9
R29	1.0	-7.9

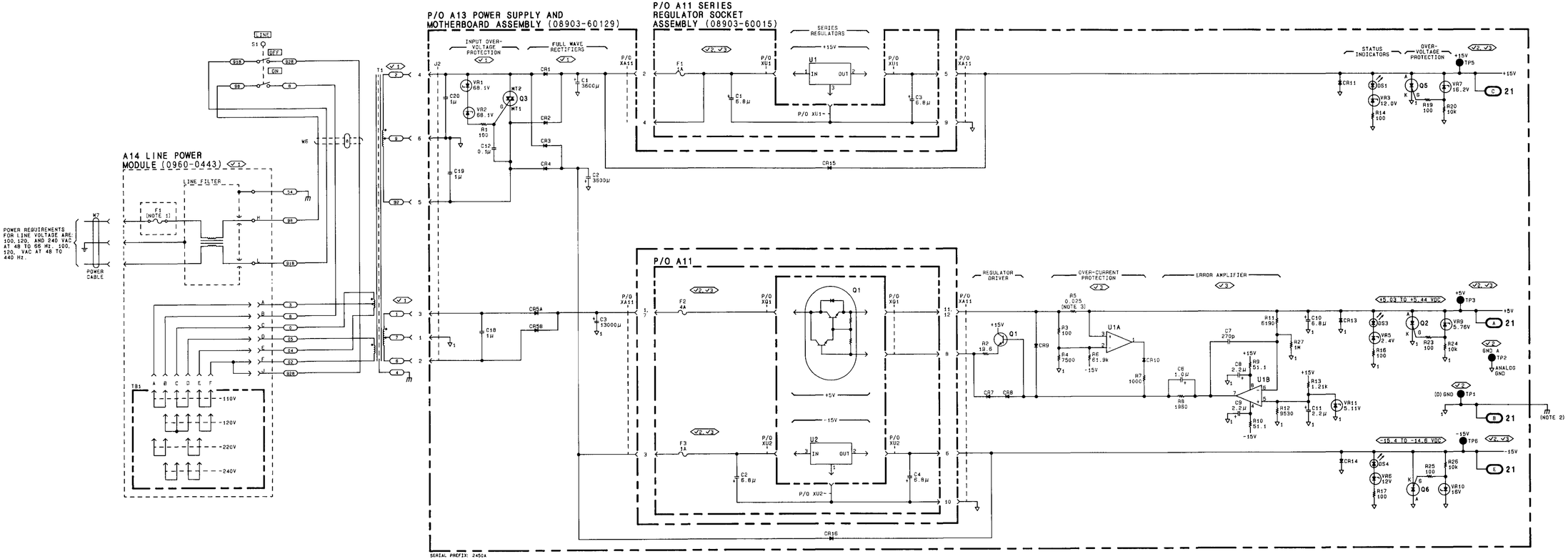
COMP	X	Y
TP1	11.7	-11.5
TP2	11.9	-11.5
TP3	12.2	-11.5
TP4	12.4	-11.5
TP5	12.7	-11.5
TP6	12.9	-11.5
U1	9.9	-11.0
U2	9.9	-10.2
VR1	0.5	-10.7
VR2	0.5	-10.8
VR3	12.7	-11.0
VR4	12.3	-11.0
VR5	12.1	-11.0
VR6	13.0	-10.6
VR7	13.8	-10.5
VR8	13.8	-9.8
VR9	12.9	-9.7
VR10	13.8	-11.3
VR11	11.5	-10.6

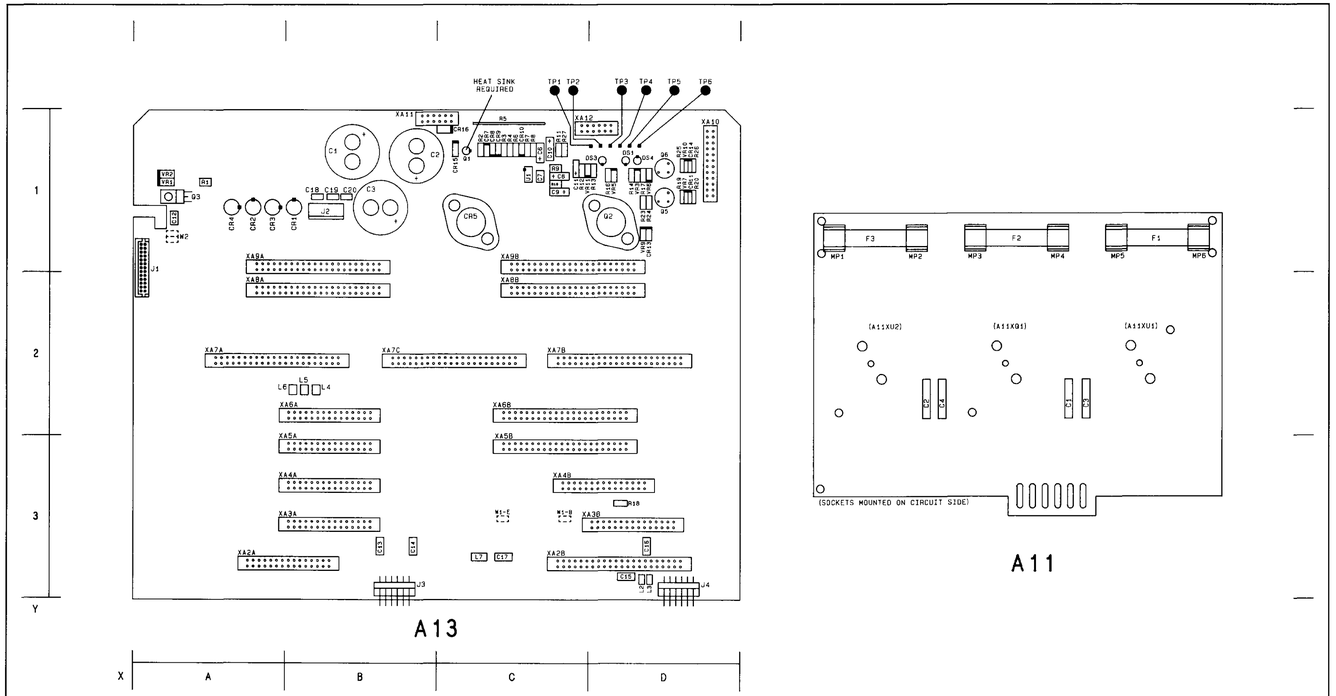
A13 Component Coordinates
2948A (HP8903B)
2946A (HP8903E)

SS20



SS20
Figure 8E-102.7
(rev 01OCT89)


P/O A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY (08903-60129)
P/O A11 SERIES REGULATOR SOCKET ASSEMBLY (08903-60015)
P/O A11
A14 LINE POWER MODULE (0960-0443)
LINE
OFF
ON
LINE FILTER
POWER REQUIREMENTS FOR LINE VOLTAGE ARE: 100, 120, AND 240 VAC AT 48 TO 66 HZ. 100, 120, VAC AT 48 TO 440 HZ.
POWER CABLE
TB1
-110V
-120V
-220V
-240V
INPUT OVER-VOLTAGE PROTECTION
FULL WAVE RECTIFIERS
SERIES REGULATORS
REGULATOR DRIVER
OVER-CURRENT PROTECTION
ERROR AMPLIFIER
STATUS INDICATORS
OVER-VOLTAGE PROTECTION
+5.03 TO +5.44 VDC
-15.4 TO -14.6 VDC
ANALOG GND
(NOTE 2)
SERIAL PREFIX: 2450A



A13

A11

Figure 8E-104. SERVICE SHEET 21 INFORMATION

Component Locator

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C13	B3						
C14	B3						
C15	D3						
C16	D3						
C17	C3						
J1	A1						
J3	B3						
J4	D3						
L2	D3						
L3	D3						
L4	B3						
L5	B2						
L6	B2						
L7	C3						
R18	D3						
W1	C3						
W2	A1						
XA2A	A3						
XA2B	C3						
XA3A	B3						
XA3B	D3						
XA4A	B3						
XA4B	C3						
XA5A	B3						
XA5B	C3						
XA6A	B2						
XA6B	C2						
XA7A	A2						
XA7B	C2						
XA7C	B2						
XA8A	A2						
XA8B	C2						
XA9A	A1						
XA9B	C1						
XA10	D1						

A11,P/O A13,A14 SEE REVERSE SIDE — Power Supply and Mother Board-Power Supply — **SS20**

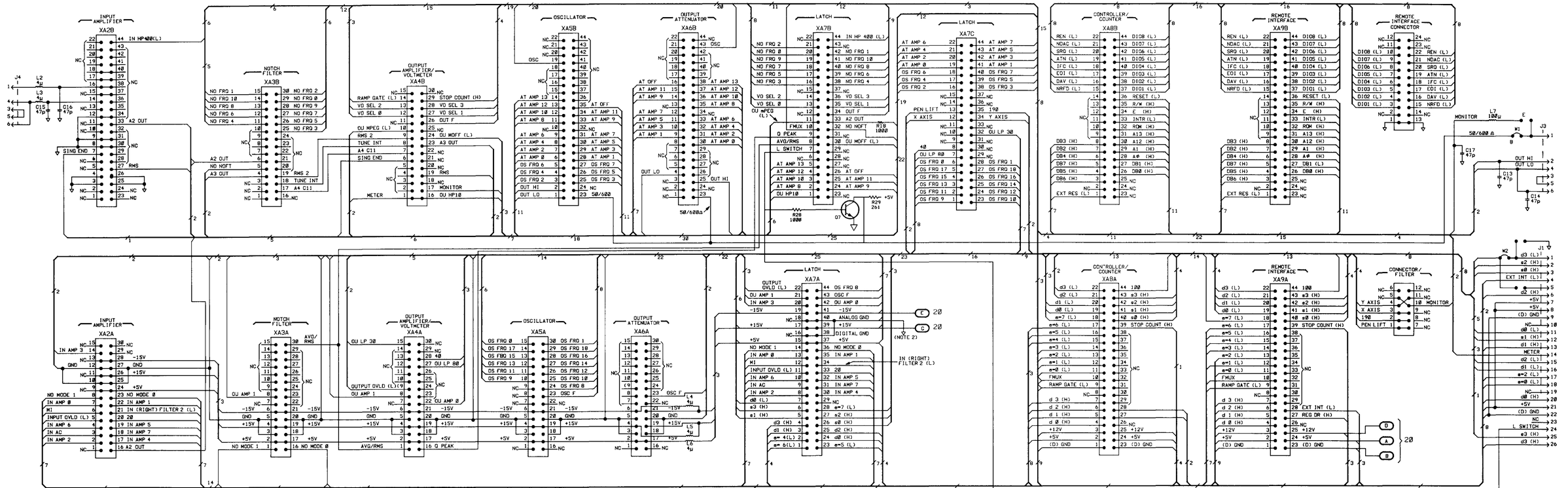
NOTES

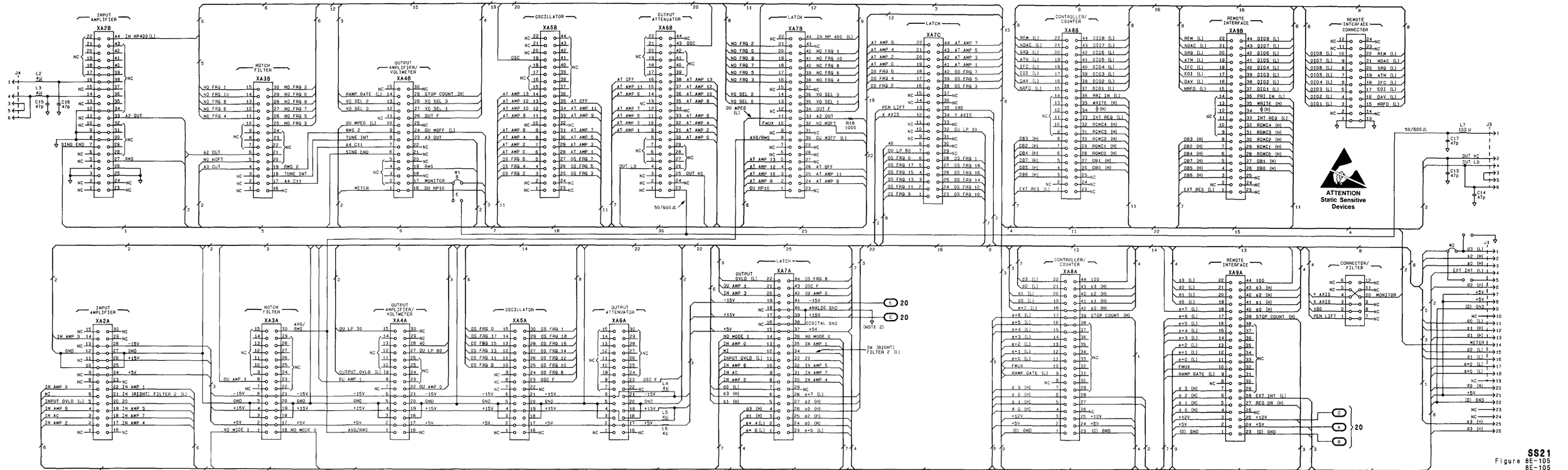
1. This wiring diagram is for (P/O) A13 POWER SUPPLY AND MOTHERBOARD ASSEMBLY (08903-60129).
2. Analog and digital ground are common to chassis ground between XA2A and XA7A.

Schematic General Information

CHANGES

2450A to 2922A	**On the A13 schematic:** • **XA4A, XA7C** - Draw a connection from XA4A pin 30 to XA7C pin 10. • **XA8A** - On the lower right half of the schematic, locate Controller/Counter XA8A and delete the connections between pins 18 and 40, 17 and 39, 16 and 38, and 15 and 37. On the line extending from pin 28 add EXT INT (L) and on the line extending from pin 27 add REG DR (H).
2717A to 2922A	**On the A13 schematic:** • **A13** - Use the new SS21, FIGURE 8E-104.3 in conjunction with SS21 on page 8E-105. • **L SWITCH** - Locate L SWITCH under XA7B and change it to Z SWITCH. Locate L SWITCH in the lower right hand corner of the schematic and change it to Z SWITCH. **On the A13 Component Locator:** • **J1** - In the upper left section of the comoponent locator, locate J1, then to the lower right of J1 add in order: R28, Q7, and R29. • **JP1-B, JP1-E** - In the lower center of the component locator locate C14, then between C14 and L7 add in order, JP1-B and JP1-E. **On the A13 Component Coordinates:** • **SS20** - In alpha numeric order add JP1-B (B,3), JP1-E (C,3), Q7 (2,A), R28 (2,A) and R29 (2,A).
2948A and above	**On the A13 Schematic:** • **SS21** - Use the new schematic foldout on page 8E-104.3, SS21 with the revision date of rev.01OCT89.


INPUT AMPLIFIER
XA2B
IN HP400(L)
NOTCH FILTER
XA3B
OUTPUT AMPLIFIER/ VOLTMETER
XA4B
OSCILLATOR
XA5B
OUTPUT ATTENUATOR
XA6B
LATCH
XA7B
LATCH
XA7C
CONTROLLER/ COUNTER
XA8B
REMOTE INTERFACE
XA9B
REMOTE INTERFACE CONNECTOR
MONITOR
50/600Ω
OUT HI
OUT LO
INPUT AMPLIFIER
XA2A
NOTCH FILTER
XA3A
AVG/ RMS
OUTPUT AMPLIFIER/ VOLTMETER
XA4A
OSCILLATOR
XA5A
OUTPUT ATTENUATOR
XA6A
LATCH
XA7A
CONTROLLER/ COUNTER
XA8A
REMOTE INTERFACE
XA9A
CONNECTOR/ FILTER
IN (RIGHT) FILTER 2 (L)
(NOTE 2)
SS21
Figure 8E-104.3
(rev 01OCT89)



SS21
Figure 8E-105
8E-105

SERVICE SHEET A---General Removal Procedures

GENERAL REMOVAL PROCEDURES

Top Cover Removal

1. Remove the two top plastic standoffs on the rear-panel by removing the Pozidriv screw from each standoff.

2. Unscrew the Pozidriv screw at the middle of the rear edge of the top cover. This is a captive screw and will cause the top cover to push away from the frame.

3. Lift the top cover off the instrument.

Bottom Cover Removal

1. Turn the instrument upside down.

2. Remove the two bottom plastic standoffs on the rear-panel by removing the Pozidriv screw from each standoff.

3. Unscrew the Pozidriv screw at the middle of the rear edge of the bottom cover. This is a captive screw and will cause the bottom cover to push away from the frame.

4. Lift the bottom cover off the instrument.

Side-Panel Removal

1. Remove the two screws holding each side-panel strap handle in place (there is one screw at either end of each strap handle).

2. Remove the strap handle caps and the strap handles.

3. Slide the side-panel toward the rear of the instrument and then pull it off.

Information Card Removal

1. Turn the instrument upside down.

2. Remove the bottom cover. (Refer to *Bottom Cover Removal* procedure above.)

3. Grasp the information cards firmly with thumb and index finger and withdraw the information cards from the information card tray.

FRONT-PANEL DISASSEMBLY PROCEDURE

Refer to Figure 8F-101.

Front-Panel Assembly Removal

1. Remove the top and bottom covers and the side-panels of the instrument. (Refer to *General Removal Procedures* above.)

2. Pry up the trim strip on the top of the instrument just above the front-panel with a small screwdriver.

3. Remove the three screws in the channel covered by the trim strip.

4. Remove the three screws from the bottom channel.

5. Pull the front-panel assembly outward.

6. Disconnect ribbon cable W5 (17) from connector A1J1 on the Keyboard and Display Assembly (16).

NOTE

Steps 7, 8 and 9 do not apply to instruments which include Option 001.

7. Remove the two screws with lock washers which secure two cable clamps MP25 to the card cage MP24 (not shown).

8. Disconnect the connector for cable W1 (13) from connector A13J3 on the motherboard.

9. Disconnect the connector for cables W4 and W5 (24) from connector A13J4 on the motherboard.

NOTE

Parts called out in steps 10, 11 and 12 are shown in Figure 8F-103, Service Sheet B.

10. Remove the two hex nuts with lock washers (21) and separate cover (22) from the transformer (18).

11. Detach the two crimp-on wire connectors (part of W6—not shown) to the line switch S1 at the Line Power Module (29) as follows:

Wire	Contact
Gray	B
White/Red/Gray	J

12. Unsolder the two wires from the Line Power Module (29) (line filter output—not shown) as follows:

Wire	Terminal
White/Gray	Front Lug
White/Brown/Gray	Rear Lug

13. Separate the front-panel assembly from the instrument by pulling the loose end of cable assembly W6 through the cut-out in the motherboard and the two polyethylene cable straps which secure W6 to the motherboard.

Separation of the A1 Keyboard and Display Assembly from the Front-Dress Panel and Sub-Panel

1. Perform steps 1 through 6 of the *Front-Panel Assembly Removal* procedure.

2. Remove the eight screws with lock washers (18), and separate the Keyboard and Display Assembly (16) from the sub-panel (6).

Meter M1 Removal

1. Perform steps 1 through 6 of the *Front-Panel Assembly Removal* procedure.

2. Remove the eight screws with lock washers (18), and separate the Keyboard and Display Assembly (16) from the sub-panel (6).

3. Remove two hex nuts on the terminals of the meter (21), and separate the white/red/orange wire and the white/brown/violet wire from the meter terminals.

4. Remove the four nuts (19) and separate the meter (21) and four spacers (20) from the Keyboard and Display Assembly (16).

Separation of the Front-Dress Panel and Display Window from the Sub-Panel

1. Remove the front-panel assembly from the instrument (refer to *Front-Panel Assembly Removal* procedure).

2. Remove the eight screws with lock washers (18), and separate the Keyboard and Display Assembly (16) from the sub-panel (6).

3. Remove the three retainers (7) from the studs on the front-dress panel (3).

NOTE

Step 4 does not apply to instruments which include Option 001.

4. Remove the four hex nuts (2 and 29) and separate the four connectors on cables W1 (15) and W2 (14) and the 12 lock washers (12) from the sub-panel (6).

5. Separate the front-dress panel (3) from the sub-panel (6) by removing two hex nuts and lock washers (10 and 9) and by separating the two binding-post terminals (1 and 30) from the sub-panel (6).

REPLACEMENT OF PUSHBUTTON KEYS AND ANNUNCIATOR LEDS

Key Cap Replacement

To replace a front-panel pushbutton key cap, pull it off and snap on a new one. You will have to either remove the Keyboard from the Front-Panel Assembly (refer to the *Front-Panel Assembly Removal* procedure) or carefully use a pair of pliers to remove the key cap.

To remove the pushbutton key cap, you will have to pull hard. Use your free hand to hold the board down as you pull.

Watch the angular position of the key cap as you snap it in place, since eight different positions for installation are possible.

Key Cap LED Replacement

Many of the front-panel pushbutton key caps have molded-in clear lenses which are illuminated by miniature LEDs located in the center portion of the switch at the circuit board. During production of the instrument, the LEDs are first soldered in place and then the switch is slid down around them and heat staked in place. If replacement of the LED becomes necessary (due to burnout), it can be replaced without having to tear out the switch. To replace a key cap LED, use the following procedure:

1. Place the Audio Analyzer on a table top. Lower the front-panel so that it is facing downward (steps 1 through 6 of the *Front-Panel Assembly Removal* procedure). Remove the pushbutton key cap (refer to *Key Cap Replacement* procedure). Unsolder the LED leads on the circuit side of the printed circuit board as you pull the LED down through the middle of the switch stem with a pair of small tweezers.

2. Clear the solder from the LED mounting holes.

3. Insert a new LED. Make sure the polarity is right. Push the leads through the circuit board and solder.

4. Put the front-panel in place. Snap on the key cap. With the instrument power on, test the switch function to make sure that the LED works.

Switch Replacement

The front-panel switches have a very high cycle life. However, if one becomes faulty and needs replacement, follow the procedure outlined below:

1. Lower the front-panel (steps 1 through 6 of the *Front-Panel Assembly Removal* procedure).

2. Remove the pushbutton key cap. You will have to pull hard. Use your free hand to hold the board down as you pull.

3. Remove the switch by chipping away or melting off the melted plastic tabs on the circuit side of the Keyboard which hold the switch in place. Refer to Figure 8F-1.

4. To assure long life and reliable electrical performance, the circuit board contact traces (which are found underneath the switch) should be clean and free of surface imperfections. Clean the switch contact pads before installing a new switch. Make sure the LEDs are not tilted and that there is no excess solder around the leads.

5. For reliable operation, any method of assembly must assure that the switch is mounted tightly against the pc board. To facilitate the heat staking operation, specially molded support anvils (HP 5040-6881) can be ordered. Refer to Figure 8F-2.

NOTE

The following operation should be done in a well ventilated area. If the heat staking tip is too hot, the plastic will vaporize and emit fumes, which may be slightly toxic.

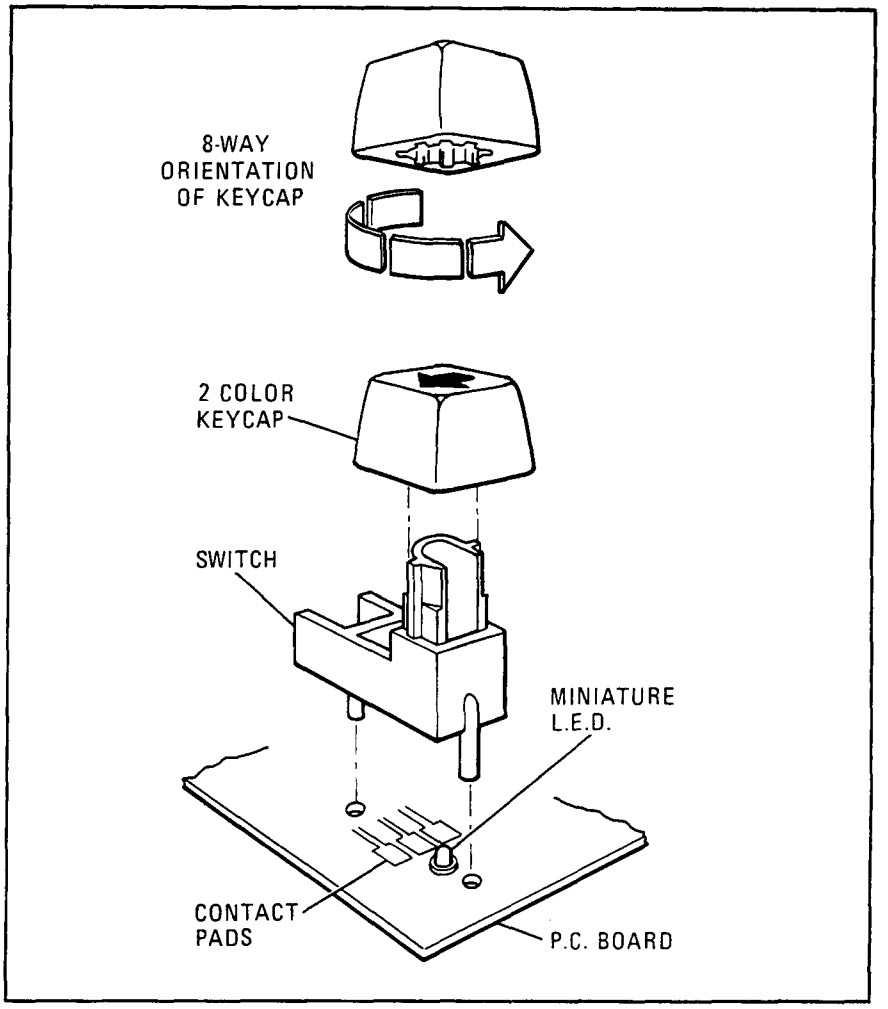


Figure 8F-1. Front-Panel Pushbutton Key Assembly

CAUTION

Do not disturb the assembly for at least 10 seconds after heat staking.

If not enough heat is applied, the plastic will tend to stick to the tip of the iron.

If too much heat is applied, the plastic will fume profusely, the "rivet" will be irregularly shaped, and the plastic will be permanently discolored.

If the staking tool is worn or flaked, it will cause a misshaped rivet and/or a contamination deposit on the surface.

6. To assure proper switch assembly, verify that the switch is pushed firmly against the circuit board and, with the hot (440°C or 825°F) staking tip, push down on each of the posts (2) of the switch. Each post should take about one second to stake. With the proper cycle, the post should turn a darker color and, in about ten seconds, return to its original bright red color. The correctly staked post should have a smooth round "rivet" like top, as shown in Figure 8F-3.

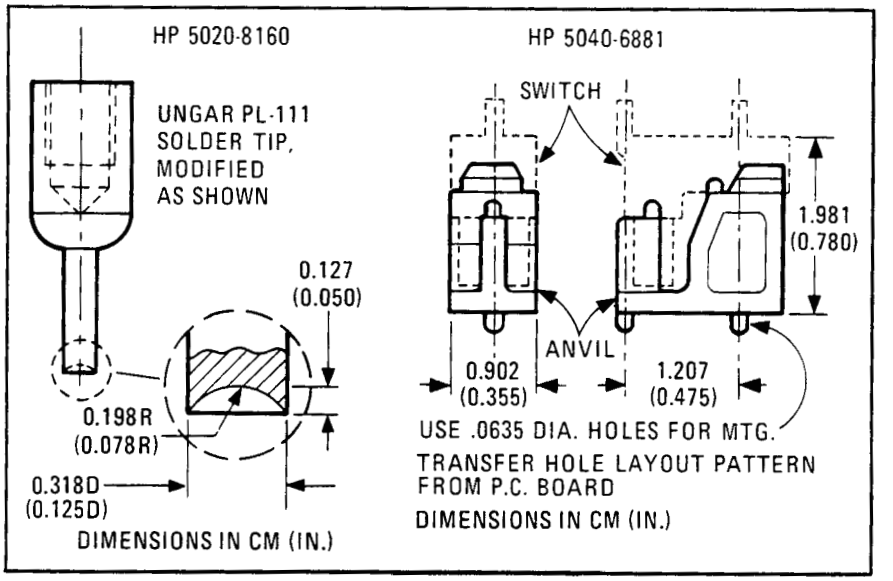


Figure 8F-2. Heat Staking Tip and Assembly Anvil

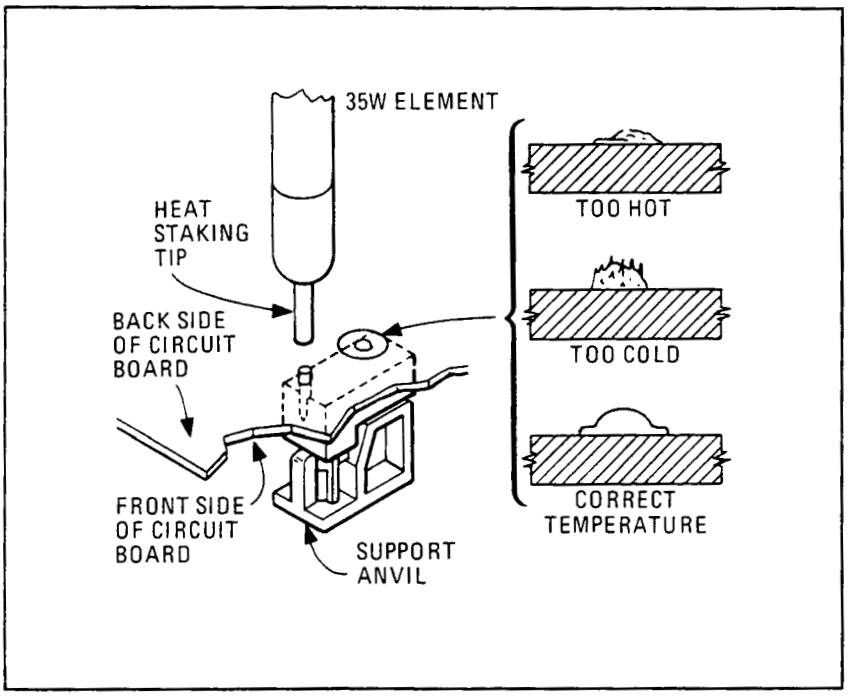


Figure 8F-3. Typical Assembly for Heat Staking Operation

SERVICE SHEET B---Rear-Panel Disassembly Procedures

REAR-PANEL DISASSEMBLY PROCEDURES

In order to remove the Power Transformer Assembly (T1) or the Connector/Filter Assembly (A12), the heatsink panel must be separated from the instrument. Refer to Figure 8F-103.

Heatsink Panel Removal

1. Remove the top cover of the instrument (refer to *General Removal Procedures,* Service Sheet A).

2. Remove the six screws and lock washers (36 and 35) and separate heatsink cover (34) from the heatsink panel (8).

3. Remove the six screws and lock washers (1 and 2) and separate the two voltage regulators (3 and 5), transistor (4), and three transistor insulators (6) from the heatsink panel (8).

4. Remove the two screws and lock washers (39 and 38) and separate rear label plate (37 or 40) if Option 001 is included.

5. Remove the four screws and lock washers (33 and 32) and separate heatsink panel (8) from rear-panel (13).

6. Separate the six insulators (7) from heatsink panel (8).

Power Transformer Assembly (T1) Removal

1. Remove the top cover and side-panels of the instrument (refer to *General Removal Procedures,* Service Sheet A).

2. Remove the instrument heatsink panel (refer to *Heatsink Panel Removal* procedure).

3. Remove the two hex nuts with lock washers (21) and separate cover (22) from the transformer (18).

4. Detach the transformer output connector (17) from connector A13J2 (not shown) in the motherboard.

5. Detach the five crimp-on wire connectors (23) from the primary side of the transformer at the Line Power Module (29) as follows:

Wire	Contact
Orange	A
Black	C
Black/Green	D
Black/Yellow	E
Black/Red	F

6. Unsolder the yellow wire (24) from ground lug on the rear panel (13).

7. Remove the four screws (27 and 28), four washers (19), and four lock nuts (20) and separate the transformer (18) and four washers (26) from the rear panel (13).

Remote Interface Connector Assembly (A10) Removal

1. Remove the top and bottom covers of the instrument (refer to *General Removal Procedures,* Service Sheet A).

2. Remove the two metric hex-head standoffs and lock washers (11 and 12) securing the HP-IB connector (14) to the rear panel (13).

3. Remove the seven screws (6-32 x 0.312) and lock washers which secure the motherboard to the chassis at the right-hand rear corner of the instrument: three from the rear edge of the motherboard and four from the right-hand edge of the motherboard.

4. Carefully move the right-hand rear corner of the motherboard no more than 0.187 inches away from instrument chassis, and remove the Remote Interface Connector Assembly (14) from its connector (A13XA10) in the motherboard.

Series Regulator Socket Assembly (A11) Removal

1. Remove the top cover of the instrument (refer to *General Removal Procedures*, Service Sheet A).

2. Remove the six screws and lock washers (36 and 35) and separate heatsink cover (34) from the heatsink panel (8).

3. Remove the six screws and lock washers (1 and 2) and separate two voltage regulators (3 and 5) and transistor (4) from the heatsink panel (8).

4. Detach the Series Regulator Socket Assembly (16) from connector A13XA11 in the motherboard.

Connector/Filter Assembly (A12) Removal

1. Remove the top and bottom covers and the side-panels of the instrument (refer to *General Removal Procedures*, Service Sheet A).

2. Remove the instrument heatsink panel (refer to *Heatsink Panel Removal* procedure).

3. Remove the two metric hex-head standoffs and lock washers (11 and 12) securing the HP-IB connector (14) to the rear panel (13).

4. Remove the two flat head screws from the rear end of each of the four corner struts (MP2, shown in Figure 6-3).

5. Remove the four screws and lock washers which secure the mother board to the rear panel (13).

NOTE

Step 6 applies only to instruments which include Option 001.

6. Remove the four hex nuts and lock washers (9 and 10) which secure connectors J7 (41), J8 (42), J9 (43), and J10 (44) to the rear panel (13).

7. Remove the four hex nuts and lock washers (9 and 10) which secure the Connector/Filter Assembly (15) to the rear-panel (13).

8. Carefully move the rear panel away from the motherboard and the corner struts until the four connectors on the Connector/Filter Assembly (15) clear the rear panel.

9. Disengage the Connector/Filter Assembly (15) from connector A13XA12 in the motherboard.

Line Power Module (A14) Removal

1. Remove the top and bottom covers and the left-hand side-panel of the instrument (refer to *General Removal Procedures*, Service Sheet A).

2. Remove the two hex nuts with lock washers (21) and separate cover (22) from the transformer (18).

3. Remove the four flat head screws and four screws and lock washers and separate lower left-hand corner strut (MP2, shown in Figure 6-2) from the instrument.

4. Remove the three screws and lock washers and separate the left frame support MP24 (not shown) from the motherboard.

5. Detach the five crimp-on wire connectors (23) from the primary side of the transformer at the Line Power Module (29) as follows:

Wire	Contact
Orange	A
Black	C
Black/Green	D
Black/Yellow	E
Black/Red	F

6. Detach the two crimp-on wire connectors (part of W6—not shown) to the line switch S1 at the Line Power Module (29) as follows:

Wire	Contact
Gray	B
White/Red/Gray	J

7. Unsolder the two wires from the Line Power Module (29) (line filter output—not shown) as follows:

Wire	Terminal
White/Gray	H
White/Brown	L

8. Unsolder the green/yellow ground wire (25) from the Line Power Module (29).

9. Depress the tabs on the top and bottom of the Line Power Module (29) and push it out through the rear panel (13).

Item Number	Reference Designator	Description
1	J3	Binding Post
2	MP40	Hex Nut
3	MP8	Front-Dress Panel
4	MP21	Not Assigned
5	See W6	Screw (4-40 x 4.6 mm)
6	MP9	Front Sub-Panel
7	S4	Not Assigned
8	W6	Line Switch Cable
9	See J3 and J6.	Lock Washer
10	See J3 and J6.	Hex Nut
11	S2	Output Float Switch
12	MP41	Lock Washer
13	P/O W1 and W2	Connector
14	W2	Output Low Cable (except Option 001)
15	W1	Output High Cable (except Option 001)
16	A1	Keyboard and Display Assembly
17	W5	Ribbon Cable
18	See MP9.	Screw (4-40 x 9.5 mm)
19	See M1.	Hex Nut with Lock Washer
20	See M1.	Spacer
21	M1	Meter
22	W4	Input High Cable (except Option 001)
23	W5	Input Low Cable (except Option 001)
24	P/O W2	Connector
25	See S2, S3, and S4.	Screw
26	See S2, S3, and S4.	Lock Washer
27	S3	Input Float Switch
28	See S2, S3, and S4.	Float Switch Lever
29	J6	Binding Post
30	A1DS20	Impedance LED

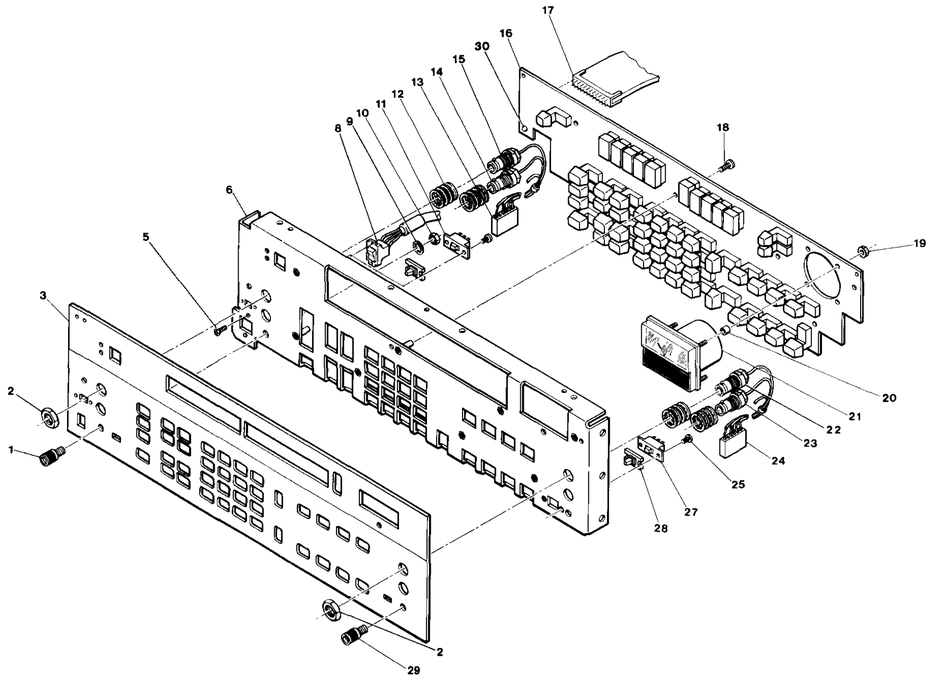


Figure 8F-101. Front-Panel Illustrated Parts Breakdown (2742A and Above)

Item Number	Reference Designator	Description
1	See Q1, U1, U2.	Tapping Screw (6-20 x 0.75)
2	See Q1, U1, U2.	Lock Washer
3	U1	Voltage Regulator 7815KC
4	Q1	Power Transistor 2N6057
5	U2	Voltage Regulator LM320K-15
6	See Q1, U1, U2	Insulator, Transistor
7	See Q1, U1, U2	Insulator, Mounting Screw
8	MP28	Heatsink Panel
9	MP42	Hex Nut
10	MP43	Lock Washer
11	See A10.	Hex Standoff
12	See A10.	Lock Washer
13	MP3	Rear Panel
14	A10	Remote Interface Connector
15	A12	Connector/Filter
16	A11	Series Regulator Socket
17	P/O T1	6-Pin Connector
18	T1	Power Transformer Assembly
19	See T1	Washer
20	See T1	Lock Nut
21	See MP30.	Hex Nut with Lock Washer
22	MP30	Cover
23	P/O T1	Primary Input Connections (5)
24	P/O T1	Primary Ground Connection
25	P/O A14	Ground Connection
26	See T1	Washer
27	See T1	Machine Screw (8-32 x 63.5 mm)
28	See T1	Machine Screw (8-32 x 57.2 mm)
29	A14	Line Power Module
30	F1	1.25 Amp Fuse (120 Vac) 0.5 Amp Fuse (220 Vac)
31	A14TB1	Line Voltage Selection Card
32	See MP28.	Lock Washer
33	See MP28.	Machine Screw (4-40 x 0.438)
34	MP29	Heatsink Cover
35	See MP29.	Lock Washer
36	See MP29.	Machine Screw (6-32 x 0.25)
37	MP31	Rear Label Plate (Except Option 001)
38	See MP31.	Lock Washer
39	See MP31.	Machine Screw (4-40 x 0.438)
40	MP31	Rear Label Plate (Option 001 Only)
41	J7	Connector (Output, High) (Option 001 Only)
42	J8	Connector (Output, Low) (Option 001 Only)
43	J9	Connector (Input, High) (Option 001 Only)
44	J10	Connector (Input, Low) (Option 001 Only)

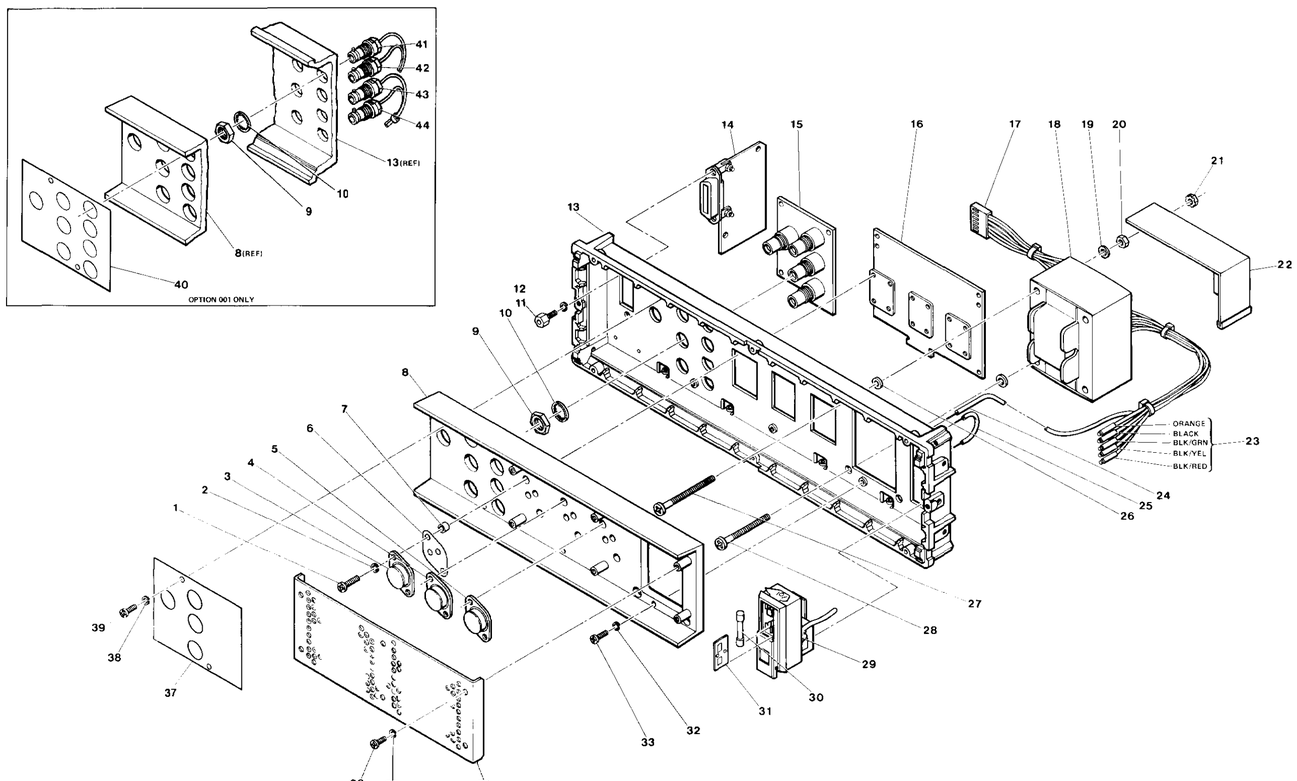


Figure 8F-103. Rear-Panel Illustrated Parts Breakdown

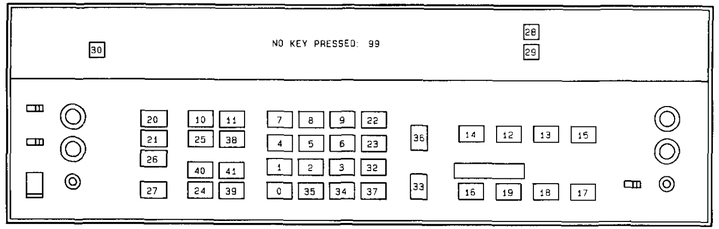


Figure 8F-105. Key Scan Codes

SERVICE SHEET C
SERVICE SPECIAL FUNCTIONS

40.0 Controller Reset

41.0 Controller Clear

42.0 Display Software Date

43.N Service Error Display Control
N=0 Disable Display of Service Errors
N=1 Enable Display of Service Errors
N=65 to N=95: Enables display of only the Service Error specified by N

44.N Notch Filter Mode Select
N=0 Notch Filter mode selected automatically as required by the measurement mode
N=1 Notch Filter in notch mode
N=2 Notch Filter in flat mode
N=3 Notch Filter in bandpass mode

45.N SINAD Meter Enable
N=0 SINAD meter enabled normally
N=1 SINAD meter enabled in all measurement modes except DC level

46.N Count Internal Signals
N=0 Oscillator Frequency
N=1 Input Frequency
N=3 Output Amplifier Frequency

48.N Defeat Output Amplifier Overdrive Protection
N=0 Output Amplifier gain determined normally
N=1 Output Amplifier gain determined by the Output RMS (Avg) Detector

49.N Display Internal Voltages
N=0 Ground
N=1 Input RMS Detector with Ripple Filter
N=2 DC Input Voltage without Filter
N=3 Output RMS (Avg) Detector with Ripple Filter
N=4 Output RMS (Avg) Detector
N=5 Output RMS (Avg) Detector with SINAD Filter
N=6 Notch Tune Voltage
N=7 DC Input Voltage with Filter

50.N Display Oscillator Frequency
N=0 Display frequency as normal
N=1 Display Oscillator frequency

52.N Read Only Memory Verification (N=ROM Number)
<Actual Checksum> . <Expected Checksum>

53.N Notch Filter Frequency Range

54.N Notch Filter Coarse Tune

55.N Oscillator Frequency Range

56.N Oscillator Coarse Tune

57.N Oscillator Fine Tune

58.N Source Fine Level

59.N Source Coarse Level

60.N Key Scan (Jumper A8U6P7 to A8TP3)
(See Figure 8F-105 for key scan codes.)

SERVICE SHEET C (Cont'd)

61.N Display HP-IB Status
N=0 <Addressed to Talk> . <Addressed to Listen> (True=1)
N=1 <DAV> . <RFD> <DAC> (True=1)
N=2 <ATN> . <REN> (True=1)
N=3 <SPM> . <SRQ> (True=1)
N=4 PIO Port A (True=1)

Display Digit	1	2	3	4	5	6	7	8
Mnemonic	IO8	IO7	IO6	IO5	IO4	IO3	IO2	IO1

N=5 PIO Port B (True=1)

Display Digit	1	2	3	4	5	6	7	8
Mnemonic	ATN	ARD	AAD	SRQ	RNL	ATT	ATL	SDV

ERROR MESSAGE SUMMARY

The error messages are grouped by error code as follows:

a. Error 10 through Error 39 and Error 90 through Error 99: these are Operating and Entry errors.

b. Error 65 through Error 89: these are Service errors.

Refer to the Error Message Summary in Section III for additional information.

NOTE

Not all of the available error message numbers are used.

Operating Errors

Error 10 — Reading too large for display.
Error 11 — Calculated value out of range.
Error 13 — Notch cannot tune to output.
Error 14 — Input level exceeds instrument specifications.

NOTE

Although error codes 17, 18 and 19 are listed as Operating Errors, they should be considered rather as diagnostic indications.

Error 17 — Internal voltmeter cannot make measurement.
Error 18 — Source cannot tune as requested.
Error 19 — Cannot confirm source frequency.
Error 25 — Top and bottom plotter limits are identical.
Error 26 — RATIO not allowed in present mode.
Error 30 — Input overload detector tripped in range hold.
Error 31 — Cannot make measurement.
Error 32 — More than 255 points total in a sweep.
Error 96 — (HP-IB only) No signal sensed at input.

SERVICE SHEET C (Cont'd)

Entry Errors

Error 20 — Entered value out of range.
Error 21 — Invalid key sequence.
Error 22 — Invalid Special Function prefix.
Error 23 — Invalid Special Function suffix.
Error 24 — Invalid HP-IB code.

Service Errors

Error 65 — Decimal point fixed too far to the left.
Error 70 — Cannot count oscillator frequency.
Error 71 — Oscillator tune abort.
Error 72 — AC input overload with input range hold.
Error 73 — Input ac level abort.
Error 74 — Output amplifier overload with output amplifier at 0 dB gain.
Error 75 — DC input overload with input range hold.
Error 76 — Too much ac for dc level measurement.
Error 77 — Output amplifier gain too high after leveling once.
Error 78 — Output amplifier overload after leveling once.
Error 79 — Output amplifier overload with no post-notch gain hold.
Error 80 — Cannot count oscillator frequency in SINAD.
Error 81 — Cannot count input frequency.
Error 82 — Notch filter does not null.
Error 83 — Cannot count input frequency (count=0).
Error 84 — Output amplifier overvoltage with no overload.
Error 85 — Period of the voltage-to-time converter 0.
Error 86 — Frequency count greater than 200 kHz.
Error 87 — Output amplifier overload with post-notch gain hold.
Error 88 — Attempt to take log of negative ratio.
Error 89 — Attempt to take log of negative number.
Error 90 — Decimal point fixed and exponent too large.
Error 91 — Decimal point fixed too far to the left (same as Error 65).
Error 92 — Decimal point fixed and unable to display.
Error 93 — Number to be displayed greater than 9999.
Error 94 — Attempt to divide by zero in ratio.
Error 95 — Signal-to-noise ratio too large to calculate.