Excerpt Edition

This PDF is an excerpt from Chapter 8
of the Parametric Measurement Handbook.

The Parametric Measurement Handbook

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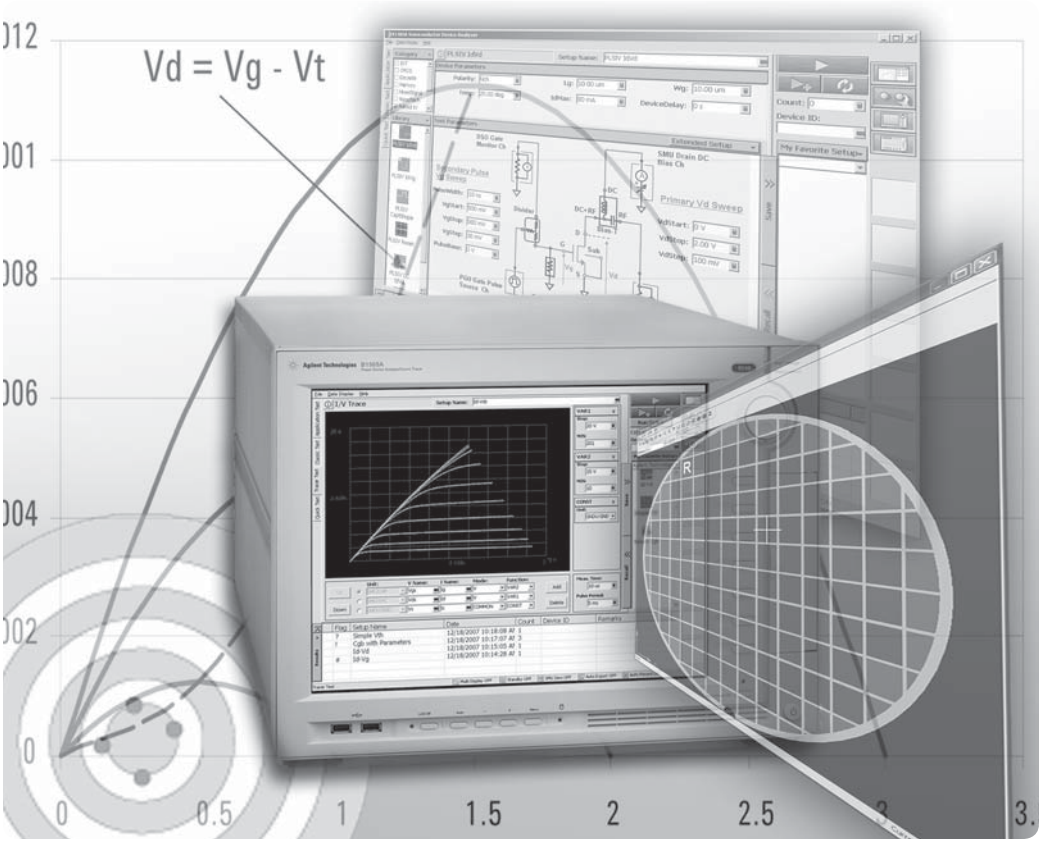

Agilent Technologies

Chapter 8: Capacitance Measurement Fundamentals

"Furious activity is no substitute for understanding." — H. H. Williams

Introduction

Capacitance measurement is one area of parametric test where many easily preventable measurement mistakes are often made. The reason for this is not lack of intelligence on the part of the user, but rather a lack of fundamental training on capacitance measurement theory and how to make good capacitance measurements. Unfortunately, this type of information is typically not taught in universities and can usually only be learned either through (rather painful) experience or by reading about it in a publication such as this.

Why do engineers make so many mistakes when measuring capacitance (especially on-wafer)? The most common reasons are:

1. Capacitance measurement requires compensation to remove parasitic inductance and capacitance from the measurement cables and fixturing, and many times this is done improperly (or not at all).
2. An induced current flows through the outer shield of the BNC connectors (if used) on a capacitance meter, and this current is necessary to balance the measurement current of the capacitance meter. If the outer shield is grounded, then the induced current flow is shorted to ground and the bridge may not be able to balance. Many users are unaware of this issue.
3. Measuring capacitance on a semiconductor wafer on a wafer chuck is very different from measuring a discrete device. The effects of the wafer prober chuck on the measurement cannot be ignored.
4. For higher measurement frequencies (> 5 MHz), structure (layout) design has a major impact on the success or failure of the measurements.

As we progress through this (rather lengthy) chapter we will cover all of these issues in detail

MOSFET capacitance measurement

Review of MOSFET capacitance behavior

Before delving into capacitance measurement theory, it is useful to first review MOSFET device operation to remind ourselves as to why we are making these measurements in the first place. While the capacitance measurement techniques discussed in this chapter are general and can be used on a variety of different device types, the dominance of MOSFETs in modern electronics elevates them enough in importance to justify devoting a section to reviewing their operating characteristics.

MOSFETs are voltage-dependent capacitors. The MOSFET gate-to-substrate capacitance depends upon the applied dc voltage (which we measure using an ac voltage of much smaller magnitude that rests on top of the dc voltage). The following set of diagrams shows the behavior of an NMOS transistor as the voltage applied to the gate is varied from negative to positive.

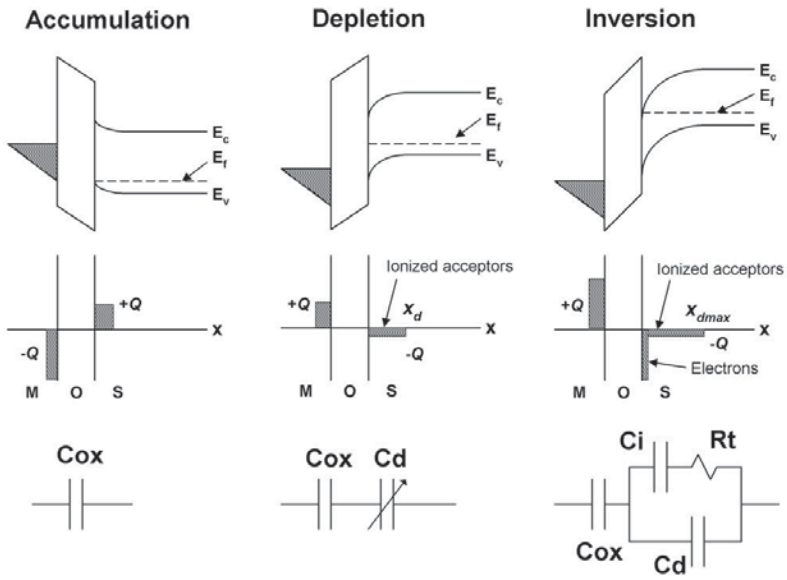

Figure 8.1. Capacitive behavior of an NMOS transistor to changes in the voltage applied to the gate.

If the silicon is held at ground and a negative voltage is applied to the gate, the MOS capacitor will begin to store positive charge at the silicon surface. The surface has a greater density of holes than Na (the acceptor density), and this condition is known as surface accumulation. In this condition the mobile charge on both sides of the oxide can respond rapidly to changes in applied voltage, and the device looks just like a parallel plate capacitor of thickness *tox*. Since it is a pure gate oxide capacitance, we denote its value as *Cox*.

If a positive gate voltage is applied to the gate relative to the silicon, the built-in positive voltage between the gate and silicon is increased. The silicon surface becomes further depleted of carriers as more acceptors become exposed at the surface, resulting in the condition known as surface depletion. In this condition electrostatic analysis shows that the total MOS capacitance consists of the series combination of Cox and the capacitance across the surface depletion region, *Cd*. Note that Cd depends upon the applied voltage.

If the positive gate voltage is further sufficiently increased, then the energy bands bend away considerably from their levels in the bulk of the silicon. The depletion region reaches a maximum width, *xdmax*, and all of the electron acceptors within this region are fully ionized. In the surface region generation of carriers exceeds recombination, and the generated electrons are swept by the electric field into the oxide-silicon interface where they remain due to the energy barrier between the conduction bands of the silicon and the oxide. Thus, the total charge in the silicon consists of the sum of these two charges. Electrostatic analysis again shows that the total MOS capacitance can be modeled as the oxide capacitance in series with the parallel combination of the depletion capacitance and the series combination of surface charge capacitance, *Ci*, and the depletion resistance, *Rt*.

Sample MOSFET parameter calculation

The reason that measurement of the gate to substrate capacitance of a MOSFET device is so important is that it is the only way to calculate many important device parameters such as substrate impurity concentration (Nsub) and flat band voltage (Vfb). It is illustrative to go through a sample parameter calculation to show how to extract these parameters from a capacitance versus voltage (CV) curve. All of the following calculations are based upon the (CV) curve shown below:

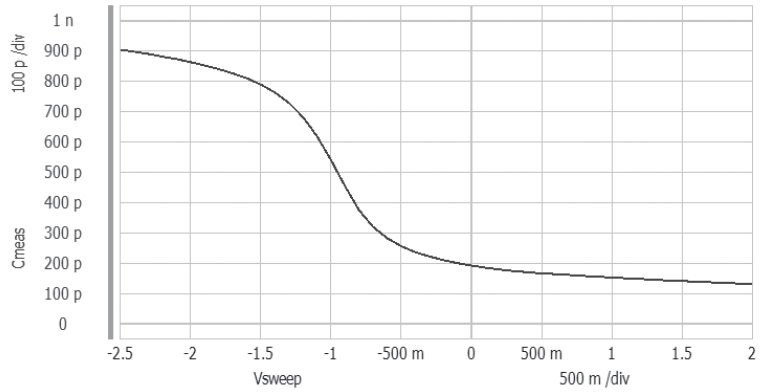

Figure 8.2. Capacitance versus voltage (CV) plot.

The gate oxide thickness of a MOSFET capacitor (t_{ox}) can be calculated from the standard equation for a parallel plate capacitor:

$$t_{ox} = \frac{A \cdot 10^8 \cdot \varepsilon_o \cdot \varepsilon_d}{Cox} \qquad \text{[Angstroms]} \qquad \textit{(Equation 8.1)}$$

Where: A is the capacitor gate area [cm^2]
ε_o is the free space permittivity (8.854×10^{-14} F/cm)
ε_d is the dielectric constant of SiO_2 (3.9)
Cox is the measured capacitance in heavy accumulation (Vg bias = Vdd) [F]

For Cox = 9.040×10^{-10} F and A = 0.001 cm^2, we have that:

t_{ox} = 37 Angstroms

The next two parameters that we must calculate are the substrate impurity concentration and the Fermi potential. These are given by the following two equations:

$$Nsub = \frac{4 \cdot |\varphi_f|}{q \cdot \varepsilon_o \cdot \varepsilon_{Si}} \left(\frac{Cs_{\min}}{A} \right)^2 \qquad [1/cm^3] \qquad \textit{(Equation 8.2)}$$

$$\varphi_f = \pm \frac{kT}{q} \cdot \ln\left(\frac{Nsub}{n_i} \right) \qquad \text{[Volts]} \qquad \textit{(Equation 8.3)}$$

Where: Nsub is the impurity concentration of the substrate
n_i is the intrinsic carrier concentration [$1/cm^3$]
Φ_f is the Fermi potential [Volts]
Cs_{min} is the minimum depletion layer capacitance [Farads]
ε_{Si} is the dielectric constant of Si (11.7)
q is the magnitude of the electron charge (1.602×10^{-19} Coulomb)
k is Boltzmann's constant (1.38×10^{-23} J/K)
T is the absolute temperature [deg K]

Note: The sign of the Fermi potential is determined by the doping in the channel. It is plus (+) for p-doped channels (NMOS transistors) and minus (-) for n-doped channels (PMOS) transistors.

These equations do not have a closed form solution; they must be solved iteratively. Using the value of $Cs_{min} = 2.01 \times 10^{-10}$ F in the above example, through repeated iterations on a computer we arrive at the values for Nsub and Φ_f shown below:

Nsub = 1.812×10^{17} cm^{-3}
Φ_f = 0.4315 V

Where A = 0.001 cm^2 and T = 300 °K

The Debye length can be calculated from the following equation:

$$\lambda = \sqrt{\frac{2k \cdot T \cdot \varepsilon_o \cdot \varepsilon_{Si}}{q^2 \cdot Nsub}} \qquad \textit{(Equation 8.4)}$$

The value of the depletion layer capacitance under flat band conditions (Csfb) is given by:

$$Csfb = \frac{\sqrt{2} \cdot A \cdot \varepsilon_o \cdot \varepsilon_{Si}}{\mathcal{A}} \qquad \textit{(Equation 8.5)}$$

Plugging the value of Nsub obtained above into these two equations yields:

Csfb = 1.0789×10^{-9} F

Since the flat band capacitance (Cfb) is the series combination of Cox and Csfb, we know that:

$$Cfb = \frac{Cox \cdot Csfb}{Cox + Csfb} \qquad \textit{(Equation 8.6)}$$

We earlier calculated the value of Cox, so combining this with the value of Csfb just calculated we arrive at a value for Cfb of:

Cfb = 4.9185×10^{-10} F

To get the value of the flat band voltage (Vfb) we need to take this value of Cfb and perform a linear interpolation on our capacitance plot. The two points on either side of the value of Cfb that we have just calculated are:

V = –0.9 V, C = 454 pF
V = –1.0 V, C = 540 pF

Thus, we can determine the value of the flat band voltage to be:

Vfb = –0.9440 V

The next useful parameter to calculate is the surface charge density (Qss). Typically, this is divided by the electron charge (q) and expressed as Qss/q:

$$\frac{Qss}{q} = \frac{Cox}{q \cdot A} \cdot \left| \Phi_{ms} - Vfb \right| \qquad [1/cm^3] \qquad \textit{(Equation 8.7)}$$

In this example,

Φ_f = 0.4315 V
Φ_{ms} = –0.6 - Φ_f = –1.032 V

where Φ_{ms} is the difference in work functions of the semiconductor (Si) and the gate poly (poly-Si). Therefore, plugging in numbers we get that:

Qss/q = 4.9375×10^{11} cm^{-3}

We can also calculate the fixed charge in the depletion layer (Q_b) and the Vth using the following equations:

$$Q_b = \pm q \cdot Nsub \cdot \frac{A \cdot \varepsilon_o \cdot \varepsilon_{Si}}{Cs_{min}} \quad \text{[Coulomb/cm}^2\text{]} \quad \textit{(Equation 8.8)}$$

$$Vth = Vfb + \left(2 \cdot \Phi_f - \frac{A \cdot Q_b}{Cox}\right) \quad \text{[Volts]} \quad \textit{(Equation 8.9)}$$

Note: The sign of Q_b is determined by the doping in the channel. It is plus (+) for n-doped channels (PMOS transistors) and minus (-) for p-doped channels (NMOS) transistors. Plugging in values previously obtained, we have that:

$Q_b = -2.2785 \times 10^{-7}$ C/cm^2

Vth = 0.1711 V

It should be obvious that it is best to create a program to automate this parameter extraction process.

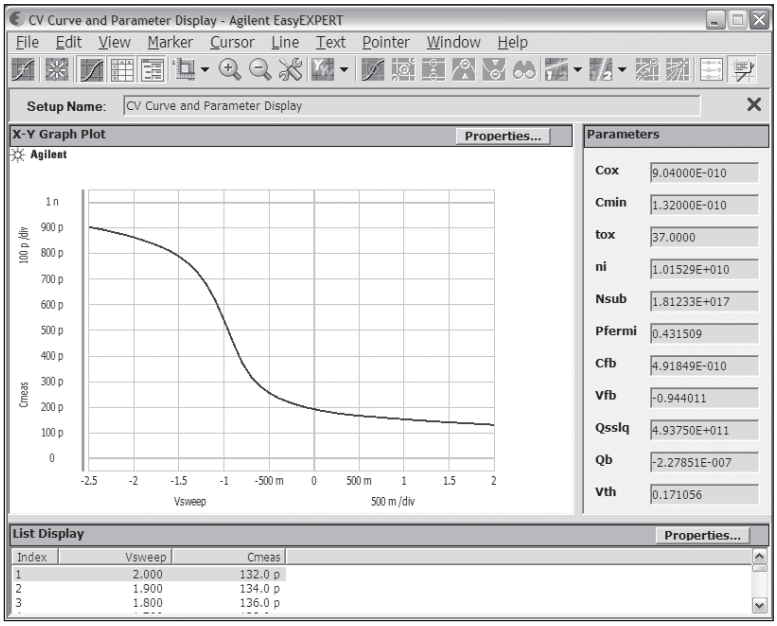

Figure 8.3. Automatic calculation of MOSFET capacitor parameters using Agilent EasyEXPERT software.

Note: The application test to perform this calculation can be downloaded from the B1500A product page on the Agilent Technologies web site.

To Get Complete Handbook

If you want to have more information, visit the following URL. You can get the complete "Parametric Measurement Handbook". This total guide contains many valuable information to measure your semiconductor devices accurately, also includes many hints to solve many measurement challenges. Now, English, Japanese, Traditional Chinese, and Simplified Chinese versions are available.

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Contents of Handbook