Digital Baseband and RF Domain Integration Challenges in Radar Systems

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Digital Baseband and RF Domain Integration Challenges in Radar Systems

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Logic analyzer measurements of FPGA hardware can be combined with IF/RF signal measurements to verify simulated performance

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Reconfigurable radar systems employ digital technology in the form of FPGAs and DSPs. That digital technology is combined with RF technology to achieve a high level of flexibility, which is required to move between different types of waveforms and configurations found in today's demanding radar applications. It is no surprise that the baseband engineering team has traditionally used different design methods and a different set of test tools than the RF team. The combined use of these different technologies has created significant system integration testing challenges.

This article describes an approach for addressing these challenges by means of a single measurement platform. Such a platform can help radar systems integrators successfully and easily validate and debug their design. This approach allows vector signal analyzer (VSA) measurements to be made all along the radar transmitter or receiver paths. Measurements can be performed with logic analyzers on FPGA hardware, with oscilloscopes at the analog IF or RF level, and with signal (spectrum) analyzers along the RF exciter and receiver chains. All three types of instruments can export captured signals into a common analysis environment to help designers pinpoint issues that might exist at any point along the mixed signal chain, ultimately speeding successful system integration.

A Chirp Radar Example Design

One of the methods to extend range and increase resolution in a radar system is to apply pulse compression. The pulse gets frequency or phase-modulated, which in turn causes each part of the pulse to have a unique frequency or phase coding. This means that reflections from a target, which normally might have had overlapping return signals in the frequency domain, now can be more easily and completely separated due to the unique frequency and phase components at hand. This enables lower peak power required for the pulse and lower probability of being detected. One type of pulse compression occurs when the frequency modulation happens in a "linear" fashion across the pulse width. This "linear" frequency modulation is also called a "chirp radar" frequency modulation.

The baseband portion of the design was created at a high level through the use of an Agilent tool called SystemVue, with a resultant design as shown in Figure 1. I and Q vector modulation chirp radar signals are created, up-sampled by a factor of four, Root-Raised-Cosine filtered, and then up-converted to digital IF. From SystemVue, hardware description language (HDL) code was generated that in turn could drive an FPGA implementation of the baseband design in a Xilinx Virtex-4 FPGA.

The digital IF signal then comes off chip and drives the input of a D/A converter. Finally, the resultant analog IF signal is up-converted to RF, where it ultimately feeds a power amplifier and drives the antenna.

Simulation of the High Level Design

The design can be simulated at a high level prior to FPGA implementation. Simulated digital IF signals can be input to the 89600 Vector Signal Analysis (VSA) tool, with results as shown in Figure 2. This example shows the desired frequency spectral content in the upper left panel, the lin-

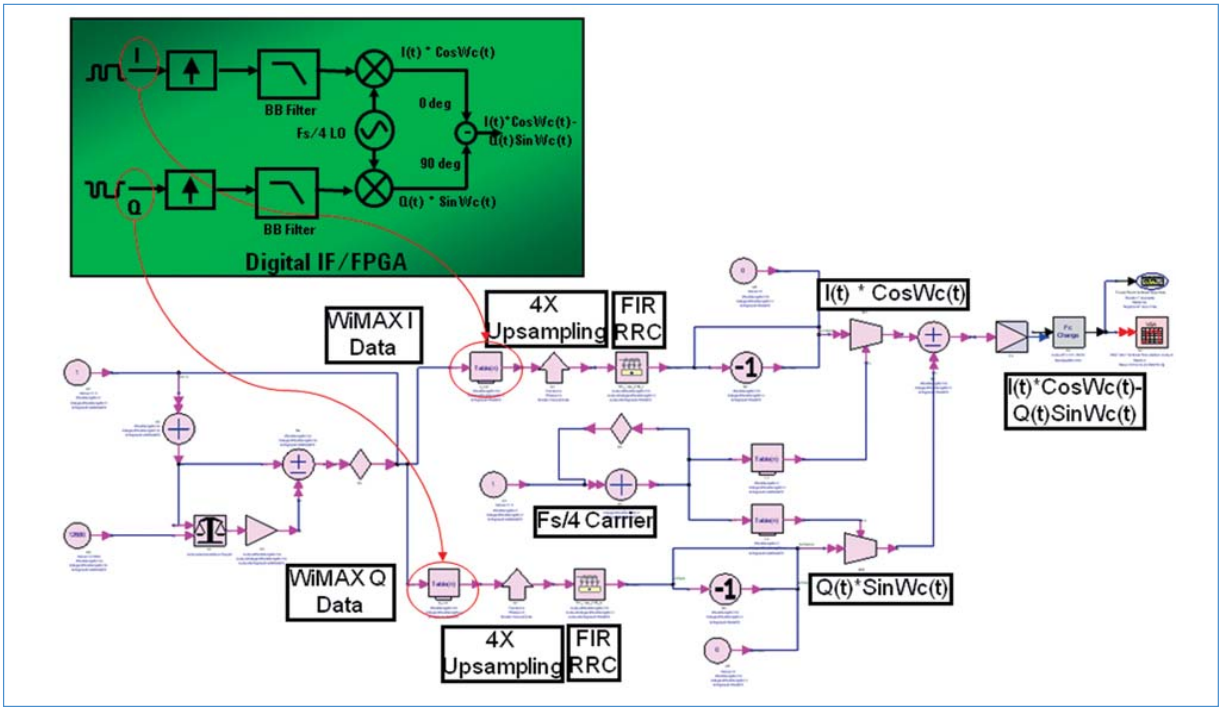

FIGURE 1
Chirp radar transmitter section with digital baseband functions.

FIGURE 2
Simulated digital IF signal demodulated in the VSA application.

ear frequency shift across the width of the radar pulse in the upper right panel, the time domain view of the radar pulse amplitude in the lower left panel, and then the classic view of the real part of the digital vector modulation in the lower right panel. These four views become our "golden standard" for comparison of measured signals on real hardware.

Taking a Look Across the Signal Path

Because the baseband portion of the design is implemented in an FPGA, it is possible to probe inside the FPGA by feeding various signals along the vector modulation path to a logic analyzer. The test setup is shown in Figure 3. The logic analyzer is on the left and has "flying lead" probes connected to 0.1 inch header pins that are on the Digitech ExtremeDSP Xilinx Virtex-4 based platform seen in the middle of the picture. Flying lead probes provide an individual coax connection for each digital data signal. A number of ground connections are made to preserve good signal integrity on the probed signals.

An oscilloscope is shown on the right, and the analog IF signal that comes out of a D/A converter on the DigiTech platform via an SMB connector is brought over to the scope with a single coax cable. Notice a Xilinx USB JTAG Programming Cable that is used to connect to the JTAG chain where the Virtex-4 FPGA is located. Ultimately, this JTAG connection will be used to switch a multiplexer inside the FPGA to reach signals of interest via internal FPGA routing resources.

In this example, the Xilinx application ChipScope Pro "Core Inserter" is used to define the probe points via an internal FPGA multiplexer measurement core and via internal routing resources of the FPGA. First, the tool allows the user to define the type of measure-

ment core, number of signal banks, how many pins will be used for debug signals, and exactly which FPGA I/O pins will be used to bring out debug signals.

FPGA signals are probed at the up-converted and filtered I and Q signal level, and also at the digital IF level where the signal drives the input to the D/A converter. Then a logic analyzer tool called the "FPGA Dynamic Probe" works with the FPGA measurement core to allow the designer to make meaningful measurements.

This logic analyzer FPGA probing tool greatly simplifies the process of making measurements. First, this tool allows the user to download the ".bit" file for the FPGA design into the FPGA directly from the logic analyzer interface via a JTAG connection.

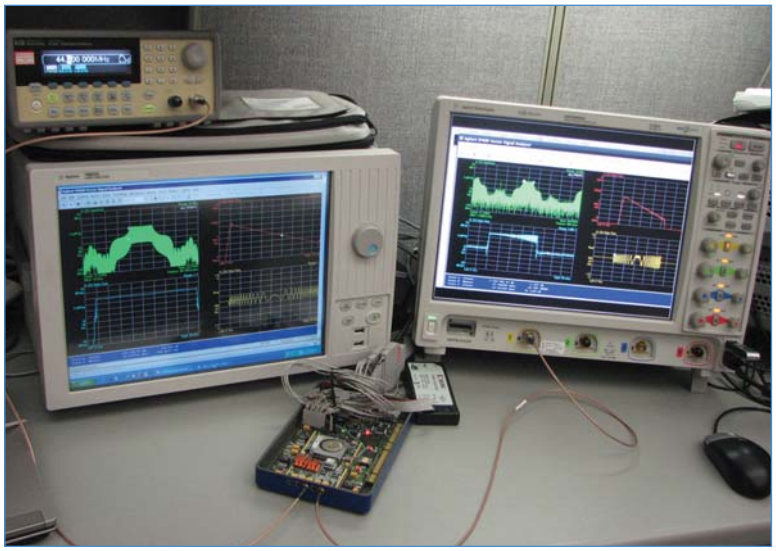

FIGURE 3
Logic analyzer probing internal FPGA signals (L) and scope probing D/A output analog IF (R), both running VSA software.

Next, the internally probed FPGA bus and signal names are imported from a Xilinx-generated file called a .cdc file that was created by the Xilinx ChipScope Pro Core Inserter application. Then a process called "automatic pin mapping" takes place where debug signals on output pins of the FPGA are discovered by the logic analyzer and "mapped" to the logic analyzer input channels automatically. The logic analyzer is set up to have the proper clock input defined, threshold levels set to match the FPGA output voltage levels, and the logic analyzer capture mode set to match the FPGA debug signal output. Designers

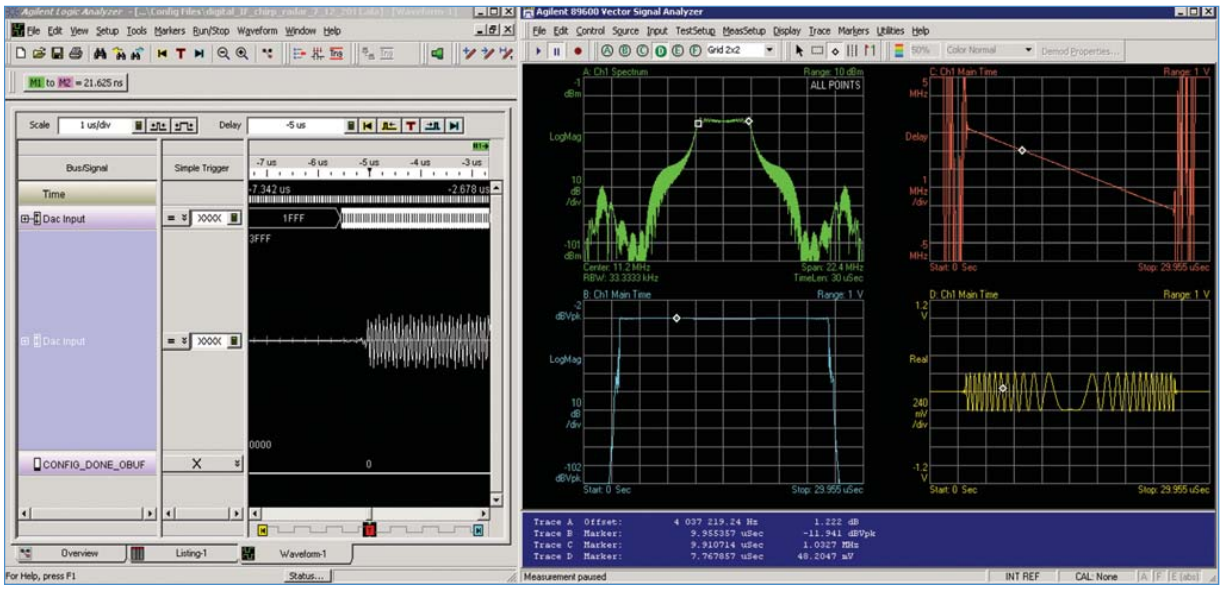

FIGURE 4
Logic analyzer measurement of the Chirp Radar digital IF signal (left) and VSA processing (right).

can select which signal bank they want to look at. In this case, it is the DAC input.

Now a digital signal trace can be taken with a logic analyzer as seen in the left side of Figure 4. The logic analyzer is displaying in "chart" mode, where hex values of the bus are converted into a waveform. We see the beginning of a digital IF pulse. The common tool, VSA software, shared between the digital baseband team and the analog/RF team, imports digital signals just captured on the logic analyzer, and processes this data into a format helpful to the designer as shown in the right side of Figure 4. But what we see now is a clear display of the linear frequency chirp modulation across the pulse, pictured in the upper right-hand side panel of the VSA software. We also see the spectral content of this digital IF signal in the upper left-hand panel. Notice these VSA panel views closely match those seen originally from "golden standard" VSA processing of simulated baseband signals back in Figure 2.

Comparing the Digital IF to the Analog IF with the Help of VSA Software

The digital IF signal that the baseband team is working with can be easily compared to the analog signal that the analog/RF team is working with. The DAC output signal is probed with a real-time oscilloscope, and this analog signal can be seen in the left side of Figure 5. This signal can be imported by the VSA software as well. The VSA software presents useful information about this analog IF signal, as shown in the VSA-processed view of that signal in the right side of Figure 5. Notice in this case, where the system is operat-

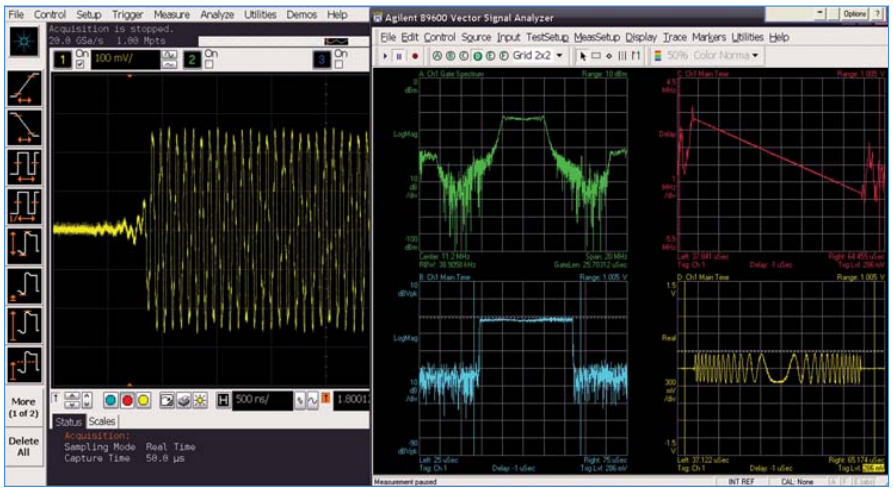

FIGURE 5
Oscilloscope measurement of the Chirp Radar analog IF signal (left) and VSA processing (right).

ing properly, we have a very similar set of data in the VSA view of processed digital IF signals seen in the four VSA panels in the right side of Figure 4, compared to the VSA view of processed analog IF signals seen in the right side of Figure 5. This side-by-side analysis can be very useful when an undesired waveform is seen along the path, and one can trace the signal back in the signal path to find the root cause of the problem.

Coordinated Debug and Validation

We have seen how the digital and analog analysis process can involve a common analysis tool called VSA that allows baseband and analog/RF teams to better work together and identify the root cause of problems in design. Whether there is an FPGA designer working with the digital baseband signals, or an RF designer focused on analog and RF stages in the system, they can jointly use one tool to pinpoint sources of error or build confidence that their radar design is ready for production.

ABOUT THE AUTHOR

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