

Product discontinued, replacement: N4960A

## Agilent N4972A Clock Synthesizer 16 GHz Data Sheet

### Key Features of N4972A-CJ0 (SCS16000)

- 0.5 to 16.0 GHz operation
- Internal calibrated sinusoidal jitter source
- Jittered, non-jittered delayed and divided outputs
- Clock output parameters independently settable on each output
- Low intrinsic jitter
- Fully supported in N4980A software
- Single port remote control through USB or GPIB
- SCPI command set for easy automation and test system integration

### N4972A-CJ1 (SCS16000J) Additionally Includes:

- Two independent sinusoidal jitter sources
- True Gaussian random jitter stress
- Spread spectrum clock - standard



### For Stressed Bit Error Rate Testing and Serial Data Device Characterization

The Agilent Technologies N4972A clock synthesizer 16 GHz (SCS16000) is a 500 MHz to 16 GHz synthesized clock generator with calibrated high-UI jitter injection capability. It is ideal as a BERT clock source or providing stressed stimulus for jitter tolerance testing and general serial data receiver characterization.



## High Performance Stressed BERT Systems

Combined with the N4965A multi-channel BERT (PCB12500), the N4972A (SCS16000) forms a high performance stressed parallel BERT. The system is ideal for performing parallel BER measurements and jitter tolerance testing in multi-lane and high SERDES count devices. The remote head architecture allows the user to select the complement of pattern generators and error detectors needed for the specific testing application.

Both parallel BER measurement and jitter tolerance testing are supported in the N4980A multi-instrument BERT software, which seamlessly scales to any number of channels as needed for multi-lane testing.

For single lane serial data applications, the N4972A (SCS16000) and N4962A serial BERT (TG1B1A) provide an affordable high performance stressed BERT that operates over the 500 Mb/s to 12.5 Gb/s range.

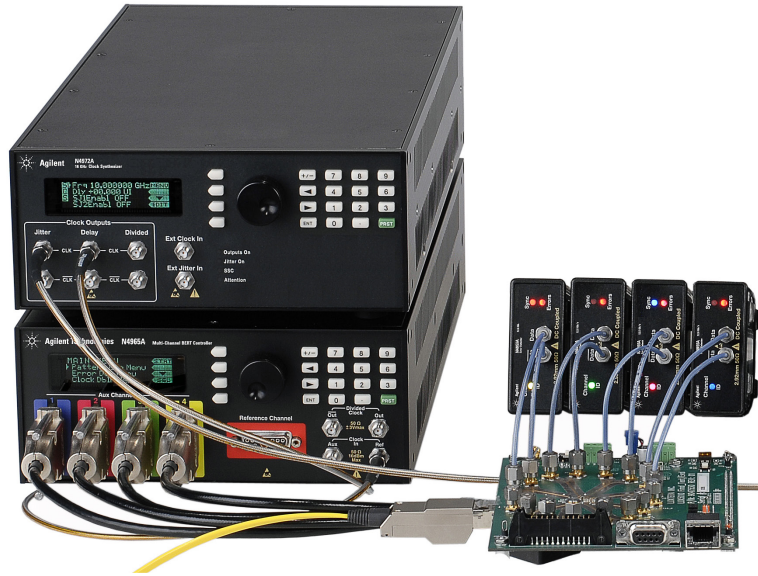


Figure 1. Stressed parallel BERT setup

## Affordable Stressed Pattern Generation

The N4972A (SCS16000) can be used to provide a clock for the Agilent Technologies N4971A pattern generator (PPG12500), creating a stressed programmable pattern generator for a fraction of the cost of a generator only version of a high performance BERT.

Many custom ICs and devices with serial data receivers lack the loop back capability required to measure BER and JTOL with a conventional BERT. Often these devices include integrated BER detectors or counters to facilitate testing. Initializing the test state in these devices requires sending a specific pattern to the device, then testing with a predefined stressed pattern. The stressed programmable pattern generation system is ideal for these applications.

With a 24 Mbit pattern memory, the N4971A pattern generator (PPG12500) can source virtually any special test pattern required for the application. The patterns can be created in the provided pattern editor utility, and quickly downloaded into the N4971A pattern generator (PPG12500).



Figure 2. Stressed pattern generation

## Repeatable Jitter Tolerance Testing

To perform jitter tolerance tests (JTOL) which can be repeated, the stressed clock source must provide jitter which is both calibrated and repeatable. The precision sources and clock modulation system used in the N4972A (SCS16000) provides this laboratory instrument grade performance.

Fully characterizing the receiver generally uses a JTOL frequency template that has high deviation at lower modulation frequencies (to test the PLL tracking in the clock data recovery circuit), then steps down to less than 1 UI stress for the remainder of the test. The N4972A (SCS16000) incorporates both a high deviation source of periodic jitter (PJ) with a modulation range up to 100 UI, and a high frequency sinusoidal jitter (SJ) source which provides up to 1 UI of stress at modulation frequencies up to 200 MHz.



Figure 3. Jitter tolerance testing

## Choose the Stress Complement You Need

The stressed clock synthesizer is available in two models. The N4972A-CJ0 (SCS16000), with single high deviation PJ and high frequency SJ source is ideal for characterizing optical communications equipment. These systems generally use only a single tone of stress for JTOL and other characterization applications.

Many serial data standards used for datacom equipment and PCs require a static base level of a mixture of stress to which the stepped SJ is added for JTOL testing. The N4972A-CJ1 (SCS16000J) adds a second independent SJ source plus a true random jitter (RJ) source to address these applications. In addition, all three of the clock outputs in the N4972A-CJ1 (SCS16000J) can be modulated with spread spectrum clock (SSC) to emulate the operating environment when SSC is employed.

Need more stress types? Both models include an external modulation input to allow the user to add an additional stress signal if required by the stress recipe. The external input can be routed to either the high deviation, low frequency modulation path, or the high frequency modulator, which operates up to 1 UI deviation and 320 MHz modulation frequency.

## Fully Integrated into N4980A Multi-Instrument BERT Software

Support for both models of the N4972A (SCS16000) is included in the N4980A multi-instrument BERT software. The base software provides an intuitive user interface for Agilent Technologies instruments. It also provides single or multi-channel BER measurement capability with an unlimited number of channels. Measurement results can be plotted or saved, as well as complete test setups.

The optional jitter tolerance package adds single and multi-channel JTOL measurements with a choice of search algorithms. Testing JTOL in multi-lane devices in parallel is much faster than testing each lane individually, and more representative of the actual operating environment with live traffic present on all lanes.



Figure 4. N4980A multi-instrument BERT software

## Three Clock Outputs

A traditional stress BERT setup uses a stressed (jittered) clock source for the pattern generator, and a clean (non-jittered) clock for the error detector. The phase delay between these clocks must be adjustable in fine resolution of time to center the error detector sample point in the eye. The N4972A (SCS16000) has dedicated outputs for both jittered and delayed signals. In addition, a clean divided clock output is provided for applications requiring a sub rate reference, or as a trigger for sampling oscilloscopes.

Each output is configured as a differential signal, but can be used single ended without the need to terminate the unused output. To address the requirements of any application, the amplitude, offset voltage, termination voltage and coupling can be independently set on each of the three outputs.



Figure 5. Clock outputs

## Block Diagram

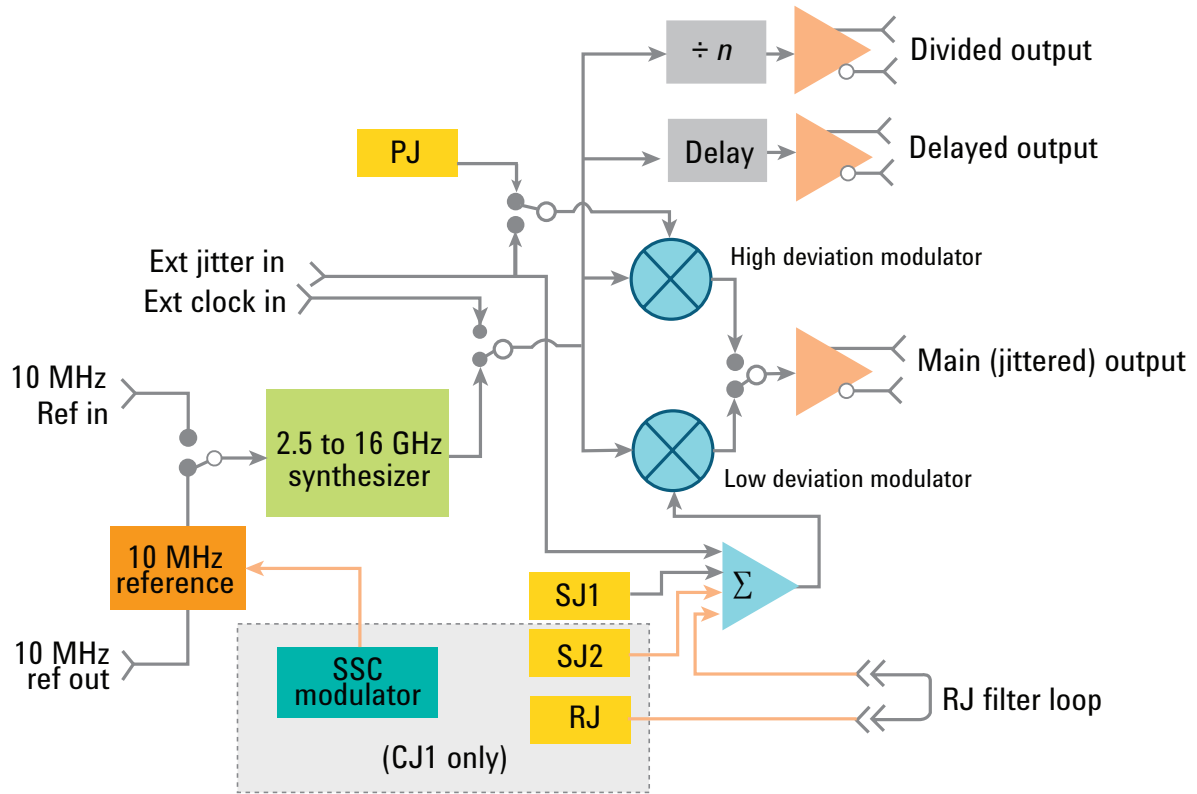


Figure 6. Block diagram

## Key Specifications

### Synthesizer

Configuration	Frequency synthesizer with three outputs: jitter (stressed), delay, and divided (both non-stressed).
Frequency range	0.5 to 16.0 GHz
Frequency resolution	1 kHz
Front panel clock outputs	
Outputs	Jitter (stressed), delay, and divided (non-stressed)
Output configuration	
All outputs	Differential, with amplitude, offset and termination voltage adjustment (can be used single ended without terminating unused output)
Amplitude range	300 mV to 1.7 V p-p single ended
Offset range	– 2.4 to +2.4 V (limited by termination voltage, see Figure 8.) On divided clock output, this is only valid when the divide ratio is a power of 2.
Termination voltage range	– 2.4 to +2.4 V (limited by offset voltage, see Figure 8.)
Rise time (20% - 80%)	< 20 ps
Intrinsic jitter	< 800 fs rms, integrated from 1 kHz to 100 MHz, for clock frequencies $\geq 1$ GHz < 1.2 ps rms for clock frequencies < 1 GHz
Duty cycle	
Jitter and delay outputs	50% $\pm$ 5%
Divided output	50% $\pm$ 5% at divide ratios which are a power of 2. Duty cycle may not be 50% at divide ratios which are not a power of 2. 50% $\pm$ 10% when divide ratio is set to 1 for amplitudes $\geq 500$ mV.
Frequency stability	0.1 ppm
Frequency accuracy	$\pm$ 20 ppm
Reference frequency	10.0 MHz, single ended output and input on rear panel
External clock	Single ended input can be substituted for internal synthesizer
External delayed clock input	Single ended input can be substituted for internal synthesizer
Spread spectrum clock (N4972A-CJ1 only)	Phase deviation appears on all outputs
Deviation range	0 – 1.0 % (10,000 ppm)
Modulation frequency range	1 Hz to 50 kHz
Modulation wave shape	Triangle
Deviation direction	Down spread, center spread, or up spread
Divided clock divide ratio	$\div 1$ to 99,999,999, with no missing integers (Waveshape of divided clocks slower than 1 MHz will be differentiated)

## Key Specifications *(Continued)*

### Synthesizer *(Continued)*

Delayed clock delay range	0 to $\pm 1,000$ UI
Delayed clock delay resolution	10 mUI
Front panel clock outputs	
Outputs	Jitter (stressed), delay, and divided (non-stressed)
Connector type	
All signals except 10 MHz ref in/out	SMA
10 MHz ref in, out	BNC

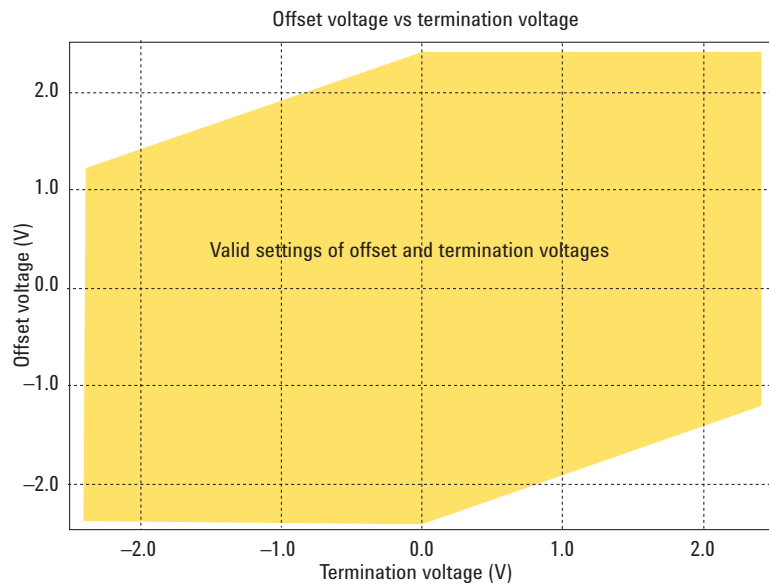


Figure 7. Maximum offset and termination voltage ranges

## Key Specifications *(Continued)*

### Stress

Configuration	Calibrated stress is added to jitter clock output through one of two modulators: A high deviation, low frequency path, or a low deviation, high frequency path.
Sources	
N4972A-CJ0 (SCS16000)	Single tone sinusoidal jitter, low and high deviation plus external input
N4972A-CJ1 (SCS16000J)	Two tone internal sinusoidal jitter, true random jitter, plus external input
SJ frequency range	1 Hz to 200 MHz
SJ modulation range (see Figure 3)	Range of SJ1 and SJ2. Also maximum combined peak jitter of SJ1 + SJ2 + RJ (peak) + external jitter applied to high frequency band modulator.
Front panel output frequency 0.5 to 1 GHz	0.01 to 1.0 UI Pk for modulation frequency 1 Hz to 10 MHz, 0.01 to 0.5 UI Pk for modulation frequency > 10 MHz to 50 MHz
Front panel output frequency > 1 to 3 GHz	0.01 to 1.0 UI Pk for modulation frequency 1 Hz to 100 MHz 0.01 to 0.5 UI Pk for modulation frequency > 100 MHz to 200 MHz
Front panel output frequency > 3 to 16 GHz	0.01 to 1.0 UI Pk for modulation frequency 1 to 100 MHz 0.01 to 0.7 UI Pk for modulation frequency > 100 MHz to 200 MHz
RJ modulation frequency contour	Flat from DC to modulator band pass: -3 dB @ 320 MHz, single pole roll off to 500 MHz. Loop through allows user to customize contour by inserting HPF or LPF in loop on rear panel. Nominal impedance is 50 Ω. Filter insertion loss will lower RJ modulation depth below calibrated value.
RJ modulation range	0 to 75 mUI rms, can be set up to 150 mUI rms, to allow for insertion loss in external filters, but is uncalibrated. For settings > 75 mUI, peak sum of all SJ, RJ and External input applied to high frequency modulation input is limited. Refer to SJ modulation range specification or Figure 9.
RJ crest factor	14 minimum (p-p to rms ratio)
External high frequency band input	
Configuration	Wide band low deviation external modulation input. External input is summed with SJ1, SJ2, and RJ. High frequency band stress is not available when either low frequency PJ or external is selected.
Modulation frequency range	DC to at least 350 MHz, determined by high frequency modulator. - 3 dB BW ≈ 320 MHz
Modulation range	Peak sum of all SJ, RJ and external input applied to high frequency modulation input is limited. Refer to SJ modulation range specification or Figure 9.
Low frequency (high deviation) modulation configuration	Periodic jitter (PJ) or external input. SJ, RJ and high frequency external modulation sources are not available when either low frequency source is enabled.
Low frequency modulation frequency range	
PJ	1 Hz to 17 MHz
External	1 Hz to 4 MHz
Low frequency PJ modulation range	0.001 to 100 UI for frequency ≤ 62.5 kHz 0.001 to (6.25E6/ PJ frequency) for frequency > 62.5 kHz to 17 MHz (see Figure 9)
Low frequency external modulation range	0.001 to 50 UI for frequency ≤ 68.4 kHz 0.001 to (3.42E6/ modulation frequency) for frequency > 68.4 kHz to 4 MHz (see Figure 9)



# Key Specifications (Continued)

## Stress (Continued)

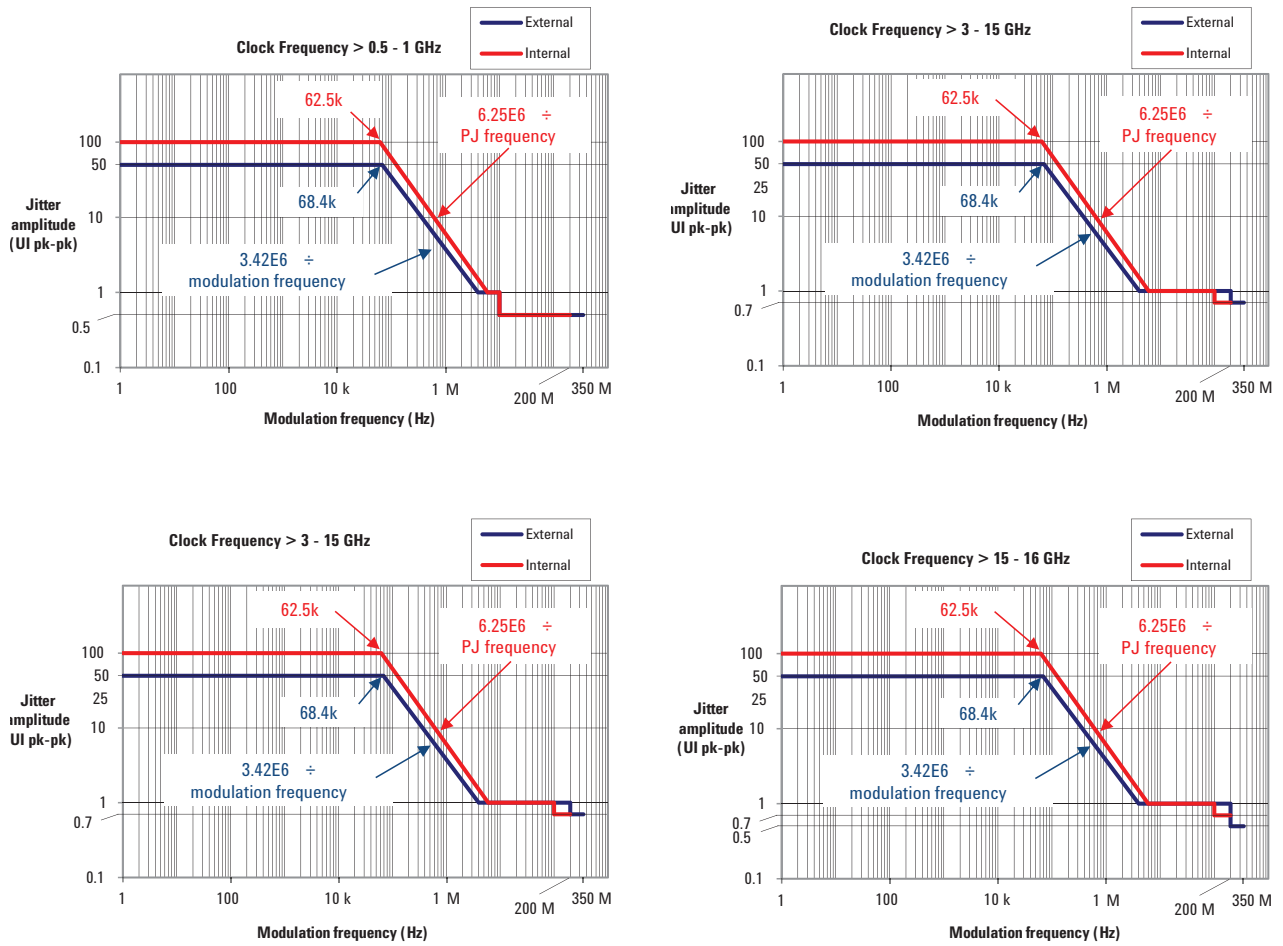


Figure 8. Modulation amplitude range graphs—internal and external front panel clock outputs

## Key Specifications *(Continued)*

### General

Remote control interface	USB 2.0 and IEEE-488 (GPIB)
Power requirements	
Voltage	100 to 240 VAC, auto ranging
Frequency	50 to 60 Hz
Power consumption	170 W maximum
Temperature, operating	+10 to +40 °C
Temperature, non-operating	– 40 to +70 °C
Dimensions (H x W x D)	
N4972A-CJ0 (SCS16000), N4972A-CJ1 (SCS16000J)	100 mm (3.9 in) x 214 mm (8.4 in) x 425 mm (16.7 in)
Mass	
N4972A-CJ0 (SCS16000)/N4972A-CJ1 (SCS16000J)	3.2 kg (7.0 lbs)

## Regulatory Standards

### EMC

Complies with European EMC Directive 2004/108/EC

- IEC/EN 61326-1
- CISPR Pub 11 Group 1, class A
- AS/NZS CISPR 11
- ICES/NMB-001

This ISM device complies with Canadian ICES-001.  
Cet appareil ISM est conforme a la norme NMB-001  
du Canada.

### Safety

Complies with European Low Voltage Directive 2006/95/EC

- IEC/EN 61010-1, 2<sup>nd</sup> Edition
- Canada: CSA C22.2 No. 61010-1
- USA: UL std no. 61010-1, 2<sup>nd</sup> Edition
- German Acoustic statement

Acoustic noise emission	Geraeuschemission
LpA < 70 dB	LpA < 70 dB
Operator position	Am Arbeitsplatz
Normal position	Normaler Betrieb
Per ISO 7779	Nach DIN 45635 t.19

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