

HP 3588A Service Manual

Serial Number 3005A00647 and greater.

Manual Backdating adapts this manual
to instruments with earlier serial numbers.



HP Part Number: 03588-90017
Microfiche Part Number: 03588-90217
Printed in U.S.A.

Print Date: February 1995

© Hewlett-Packard Company, 1990, 1
3500 Super Hill Road, Everett, WA 98203

rights reserved.
U.S.A.



SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements. This is a Safety Class 1 instrument.

GROUND THE INSTRUMENT

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure the safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

Warning



Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SAFETY SYMBOLS

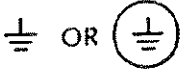
General Definitions of Safety Symbols Used On Equipment or In Manuals.



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.



Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line.)



Direct current (power line.)



Alternating or direct current (power line.)

Warning

The **WARNING** sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which if not correctly performed or adhered to, could result in injury or death to personnel.

Caution

The **CAUTION** sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

Note

The **NOTE** sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

Table of Contents

Section I Adjustments

| | |
|---|------|
| Introduction | 1-1 |
| Safety Considerations | 1-3 |
| Equipment Required | 1-3 |
| Remote Operation | 1-4 |
| 1. Oven Shutdown | 1-5 |
| 2. 80 MHz Reference VCXO | 1-6 |
| 3. 300 MHz Reference VCO | 1-7 |
| 4. Interpolation VCO | 1-9 |
| 5. Single Loop Control Voltage Clamps | 1-11 |
| 6. 100 kHz and API Spurs | 1-12 |
| 7. Sum VCO Filter | 1-15 |
| 8. Multiple Loop Control Voltage Clamps | 1-17 |
| 9. Step VCO Filter | 1-18 |
| 10. Pretune Offset and Slope | 1-20 |
| 11. ADC Gain, Offset, and Reference | 1-22 |
| 12. Second IF Bandpass Filter | 1-28 |
| 13. Source Bandpass Filter | 1-31 |
| 14. First IF Bandpass Filter | 1-34 |
| 15. Autorange Thresholds and 1 Meg Ohm Flatness | 1-37 |
| 16. Oven Frequency | 1-40 |
| 17. Calibrator Flatness and Level | 1-42 |
| 18. Display | 1-44 |

Section II Replaceable Parts

| | |
|-------------------------------|------|
| Introduction | 2-1 |
| Ordering Information | 2-2 |
| Ordering Non-Listed Parts | 2-2 |
| Direct Mail Order System | 2-2 |
| Assemblies | 2-6 |
| Replacing the CPU Assembly | 2-7 |
| Replacing the Memory Assembly | 2-7 |
| Cables | 2-8 |
| Hardware | 2-10 |
| Disassembly/Assembly | 2-13 |

Table of Contents (Continued)

Section III Manual Backdating

Introduction 3-1
Manual Changes Supplement 3-1
Manual Changes Instructions 3-2

Section IV Circuit Descriptions

Introduction 4-1
Overall Instrument Description 4-1
 Overall Block Diagram 4-2
 Assemblies 4-5
A11 Input 4-9
A12 First Conversion 4-11
A13 Second Conversion 4-12
A21 Sum VCO 4-13
A22 Sum Phase Detector 4-19
A23 Step Phase Detector 4-21
A24 Step VCO 4-23
A31 Reference/Calibrator 4-24
A32 300 MHz 4-26
A33 Trigger 4-27
A41 Source Amplifier 4-29
A42 Source Conversion 4-31
A51 Interpolation VCO 4-33
A52 Fractional-N 4-35
A61 IF 4-37
A62 ADC/Digital Filter 4-38
A81 CPU 4-40
A87 Memory and A88 Expanded Memory 4-46
A90 Fan Power and A91 Fan Power/Oven 4-47
A99 Motherboard 4-47
Front Panel 4-47
Power Supply 4-48
Disk Drive 4-48
Display 4-48
Voltage and Signal Distribution 4-49
W1 Memory Cable Signals 4-61
W2 CPU Power Cable Signals 4-63
W3 Display Cable Signals 4-64
W4 Disk Drive Cable Signals 4-64
W5 Front Panel Cable Signals 4-66
W11 Fast Bus Cable Signals 4-66
W12 Motherboard Power Cable Signals 4-68
RF Cable Signals 4-69

| | |
|---|------|
| Motherboard Signals | 4-73 |
| HP-IB Connector Signals | 4-76 |
| Calibration Routine | 4-77 |
| Calibration Error Message | 4-78 |
| Calibration Correction Curves | 4-79 |
| Fault Log Messages | 4-82 |
| Power-On and Preset States | 4-84 |
| Power-On States | 4-86 |
| Nonvolatile States | 4-86 |

Section V Service

| | |
|--|------|
| Introduction | 5-1 |
| Safety Considerations | 5-1 |
| Equipment Required | 5-2 |
| How to Use This Section | 5-2 |
| Troubleshooting Hints | 5-3 |
| Choosing a Troubleshooting Test | 5-4 |
| What to Do After an Assembly Is Replaced | 5-5 |
| Initial Verification | 5-8 |
| Test 1. Initial Verification | 5-8 |
| Troubleshooting Using the Power-On Test | 5-14 |
| Test 2. Power-on | 5-14 |
| Test 3. CPU, Memory, and Buses | 5-17 |
| Test 4. Memory | 5-19 |
| Test 5. Display | 5-20 |
| Test 6. IIC Bus (Inter-IC Bus) | 5-23 |
| Test 7. Fast Bus | 5-26 |
| Test 8. Control Lines | 5-28 |
| Troubleshooting Using the Self Tests | 5-30 |
| Test 9. Self Test | 5-31 |
| Test 10. ALL Locks Analyzer | 5-36 |
| Test 11. Disk Drive | 5-38 |
| Test 12. HP-IB/RS-232 | 5-41 |
| Test 13. Digital Filter | 5-42 |
| Test 14. Source | 5-43 |
| Test 15. Local Oscillator | 5-46 |
| Test 16. Interpolation Loop | 5-47 |
| Test 17. Single Loop | 5-49 |
| Test 18. Input Conversion | 5-52 |
| Test 19. Sum Loop | 5-58 |
| Test 20. Step Loop | 5-61 |
| Test 21. Reference | 5-63 |
| Test 22. Intermittent Failures | 5-66 |

Table of Contents (Continued)

| | |
|---|------|
| Troubleshooting Failing Performance Tests | 5-68 |
| Test 23. Local Oscillator Feedthrough | 5-70 |
| Test 24. Phase Noise | 5-71 |
| Test 25. Residual Responses | 5-75 |
| Test 26. Noise Level | 5-76 |
| Test 27. Frequency Accuracy | 5-78 |
| Test 28. Spurious Responses | 5-79 |
| Test 29. Input Harmonic Distortion | 5-80 |
| Test 30. Intermodulation Distortion | 5-82 |
| Test 31. Source Amplitude Accuracy and Frequency Response | 5-84 |
| Test 32. Log Scale Accuracy | 5-85 |
| Troubleshooting Miscellaneous Failures | 5-88 |
| Test 33. Memory Battery | 5-88 |
| Test 34. Fan Power | 5-89 |
| Test 35. Trigger | 5-90 |
| Power-on Test Descriptions | 5-91 |
| Low-level Tests | 5-91 |
| High-level Test | 5-91 |
| Power-on Test Messages | 5-92 |
| Self-Test Descriptions | 5-94 |
| Self Tests that Perform a Measurement | 5-96 |
| Individual Self-Test Descriptions | 5-97 |

Index

Adjustments

Introduction

This section contains the adjustment procedures for the HP 3588A Spectrum Analyzer. Use these adjustments if the analyzer does not meet its specifications or if instructed in section V, "Service," to perform these adjustments. These adjustments are not required for routine maintenance. Table 1-1 lists all the adjustments.

The top cover must be removed to perform all adjustments except "1. Oven Shutdown" and "16. Oven Frequency." For information on top cover removal, see "Disassembly/Assembly" in section II, "Replaceable Parts."

Note



Allow the HP 3588A Spectrum Analyzer to warm up for at least an hour. This is critical for adjustment "2. 80 MHz Reference VCXO." Analyzers with the oven option (option 001) must cool off for at least 8 hours before doing adjustment "1. Oven Shutdown" and warm up for at least 48 hours before doing adjustment "16. Oven Frequency."

During many of these adjustment procedures, an adjustment message appears on the screen. The instructions on the screen are not as complete as the instructions in this manual. When an adjustment message appears on the screen, continue to follow the instructions in this manual. Failure to follow the instructions in this manual may result in an incorrect adjustment, which would appear as a hardware failure.

Table 1-1. Adjustments

| Adjustment Procedure | Assembly | Component |
|---|----------|---|
| 1. Oven Shutdown | A91 | R2 |
| 2. 80 MHz Reference VCXO | A31 | C6, R13 |
| 3. 300 MHz Reference VCO | A32 | L506, L508 |
| 4. Interpolation VCO | A51 | L101 |
| 5. Single Loop Control Voltage Clamps | A52 | R423, R422 |
| 6. 100 kHz and API Spurs | A52 | R416, R518, R521, R533 |
| 7. Sum VCO Filter | A21 | L106, L107 |
| 8. Multiple Loop Control Voltage Clamps | A23 | R463, R461 |
| 9. Step VCO Filter | A24 | L506, 507 |
| 10. Pretune Offset and Slope | A23 | R452, R457 |
| 11. ADC Gain, Offset, and Reference | A62 | R407, R405, R431 |
| 12. Second IF Bandpass Filter | A61 | L3-L6, L8-L10, C30, R11 |
| 13. Source Bandpass Filter | A42 | CAV ADJ 1-CAV ADJ4 |
| 14. First IF Bandpass Filter | A12 | CAV ADJ 1-CAV ADJ4 |
| 15. Autorange Thresholds and 1 Meg Ohm Flatness | A11 | C413, R624, R626 |
| 16. Oven Frequency | A91 | U3, R12 |
| 17. Calibrator Flatness and Level | A31 | R322, C330 |
| 18. Display | Display | VR31-VR34, VR41, VR42, VR64, VR67, L403 |

Note

If an assembly is replaced, see table 5-2 for required adjustments and performance tests.

Safety Considerations

Although the HP 3588A Spectrum Analyzer is designed in accordance with international safety standards, this manual contains information, cautions, and warnings that must be followed to ensure safe operation and to keep the unit in safe condition. Adjustments in this section are performed with power applied and protective covers removed. These adjustments must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Warning



Any interruption of the protective (grounding) conductor inside or outside the unit, or disconnection of the protective earth terminal can expose operators to potentially dangerous voltages.

Under no circumstances should an operator remove any covers, screws, shields or in any other way access the interior of the HP 3588A Spectrum Analyzer. There are no operator controls inside the analyzer.

Equipment Required

See chapter 1, "General Information," in the *HP 3588A Performance Test Guide* for tables listing recommended test equipment. Any equipment which meets the critical specifications given in the tables may be substituted for the recommended model.

Remote Operation

Adjustments can be set up using the remote operation capability of the HP 3588A Spectrum Analyzer. See table 1-2 for a list of adjustments and corresponding HP-IB codes. See the *HP 3588A HP-IB Programming Reference* for general information on remote operation.

Table 1-2. HP-IB Codes to Set Up Adjustments

| Adjustments | HP-IB Codes |
|---|--|
| 4. Interpolation VCO | DIAG:FRAC:VCO:ADJ |
| 5. Single Loop Control Voltage Clamps | DIAG:FRAC:SLO:CHIG DIAG:FRAC:SLO:CLOW |
| 6. 100 kHz and API Spurs | DIAG:FRAC:SPUR:NULL DIAG:FRAC:SPUR:API:ONE DIAG:FRAC:SPUR:API:TWO DIAG:FRAC:SPUR:API:FOUR |
| 7. Sum VCO Filter | DIAG:FRAC:SUMV:LPF |
| 8. Multiple Loop Control Voltage Clamps | DIAG:FRAC:MLO:CHIG DIAG:FRAC:MLO:CLOW |
| 9. Step VCO Filter | DIAG:FRAC:SVCO:LPF |
| 10. Pretune Offset and Slope | DIAG:FRAC:PRET:OFFS DIAG:FRAC:PRET:SLOP |
| 11. ADC Gain, Offset, and Reference | DIAG:ADJ:ADC:GAIN DIAG:ADJ:ADC:OFFS |
| 12. Second IF Bandpass Filter | DIAG:REC:TWO:ONE DIAG:REC:TWO:TWO DIAG:REC:TWO:THR DIAG:REC:TWO:FOUR DIAG:REC:TWO:FIVE |
| 13. Source Bandpass Filter | DIAG:ADJ:SOUR:RES |
| 14. First IF Bandpass Filter | DIAG:REC:HRES |
| 15. Autorange Thresholds and 1 Meg Ohm Flatness | DIAG:REC:MOHM:FLAT DIAG:REC:RANG:UP DIAG:REC:RANG:DOWN |
| 17. Calibrator Flatness and Level | DIAG:CAL:EREF DIAG:CAL:FLAT DIAG:CAL:HFR DIAG:CAL:LEV |
| 18. Display | TEST:DISP:PATT |

2. 80 MHz Reference VCXO

This procedure adjusts the control voltage for the 80 MHz reference VCXO on the A31 Reference/Calibrator assembly. The 80 MHz reference is the primary frequency reference for the analyzer.

Equipment Required: Frequency Counter
 BNC(m)-to-SMB(f) Cable
 Flat-Edge Adjustment Tool

Note



Before doing this adjustment, make sure the HP 3588A Spectrum Analyzer has been ON (1) for approximately one hour to allow the 80 MHz reference VCXO to reach a stable operating temperature.

-
1. Disconnect the rear panel jumper (OVEN REF OUT to EXT REF IN) on analyzers with the optional oven.
 2. Disconnect the cable from A31 J3, and connect the frequency counter to A31 J3 using a BNC-to-SMB cable.
 3. Adjust FREQ ADJ FINE (A31 R13) to the center of its adjustment range.
 4. Adjust FREQ ADJ CRS (A31 C6) for $10 \text{ MHz} \pm 10 \text{ Hz}$ using the flat-edge adjustment tool in the service kit.
 5. Adjust FREQ ADJ FINE for $10 \text{ MHz} \pm 1 \text{ Hz}$.
 6. Disconnect the frequency counter from A31 J3, and reconnect the cable from A61 J2 to A31 J3.
 7. Reconnect the rear panel jumper on analyzers with the optional oven.

3. 300 MHz Reference VCO

4. Set the power switch to ON (I). Through the holes in shield can, alternately adjust A32 L506 and L508 for $-7.00 \pm 0.25V$.
5. Set the power switch to STANDBY (O). Place the 300 MHz assembly into the card nest and replace the screws.
6. Reconnect the following using original cables:
 - A32 J1 to A31 J9
 - A32 J2 to A33 J1
 - A32 J3 to A42 J3
 - A32 J4 to A23 J2
 - A32 J5 to A13 J1

4. Interpolation VCO

This procedure adjusts the frequency range of the interpolation VCO on the A51 Interpolation VCO assembly.

Equipment Required: Frequency Counter
 Extender Board
 BNC(m)-to-SMB(f) Cable

1. Set the power switch to STANDBY (⊖). Remove the screw at each end of the A51 Interpolation VCO assembly, and remove the assembly from the card nest.
2. Move the jumper on A51 J101 to its test position (see figure 1-2). Place the assembly on an extender board.

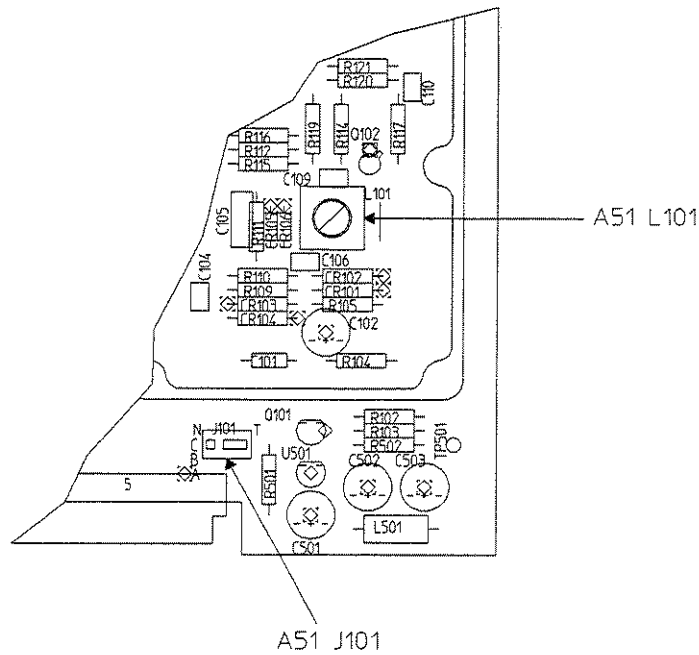


Figure 1-2. A51 Interpolation VCO Component Locator

4. Interpolation VCO

3. Connect the frequency counter to A51 J4 using a BNC-to-SMB cable.

4. Set the power switch to ON (I), then press the following keys:

[Spcl Fctn]

[] (second softkey from bottom)

- 99

[] (second softkey from bottom)

[SERVICE FUNCTIONS]

[ADJUSTMTS]

[LOCAL OSC]

[INTRPL VCO]

5. Through the hole in the shield can, adjust A51 L101 for 55 ± 0.5 MHz using a plastic tuning tool.

6. Set the power switch to STANDBY (O). Move the jumper back to its normal position, and place the Interpolation VCO assembly into the card nest. Replace the screws.

7. Reconnect the following using original cables:

A51 J1 to A22 J3

A51 J2 to A21 J1

A51 J3 to A52 J1

A51 J4 (no connection)

6. 100 kHz and API Spurs

This procedure attenuates the 100 kHz sample and hold spur, and the API spurs on the A52 Fractional-N assembly.

Equipment Required:

- Spectrum Analyzer
- Extender Board
- Extender Cables
- BNC(m)-to-SMB(f) Cable
- BNC Cable

1. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A52 Fractional-N assembly, and place the assembly on an extender board.

Caution



To avoid damaging the cables connected to A33 J5 and J6, disconnect and position the cables away from the A52 Fractional-N assembly before removing or inserting the A52 Fractional-N assembly.

2. Reconnect the following using extender cables:

- A52 J1 to A51 J3
- A52 J2 to A33 J4
- A62 J1 to A33 J3
- A62 J2 to A31 J8

3. Disconnect the cable from A21 J2, and connect the spectrum analyzer to A21 J2 using a BNC-to-SMB cable. Connect the spectrum analyzer's 10 MHz reference output to EXT REF IN (on rear panel) using a BNC cable.
4. Press the [Preset] hardkey, then set the spectrum analyzer as follows:

| | |
|------------------|---------|
| Center Frequency | 400 MHz |
| Frequency Span | 500 kHz |
| Reference Level | 10 dBm |
| Res BW | 10 kHz |
| Video BW | 1 kHz |

5. Set the power switch to ON (⏻), then press the following keys:

[Spcl Fctn]

[] (second softkey from bottom)

– 99

[] (second softkey from bottom)

[SERVICE FUNCTIONS]

[ADJUSTMTS]

[LOCAL OSC]

[SPURS]

[100 kHz]

6. Adjust A52 R416 (see figure 1-3) for a minimum spur level at approximately 400.2 MHz (figure 1-4 shows the spurs out of adjustment).

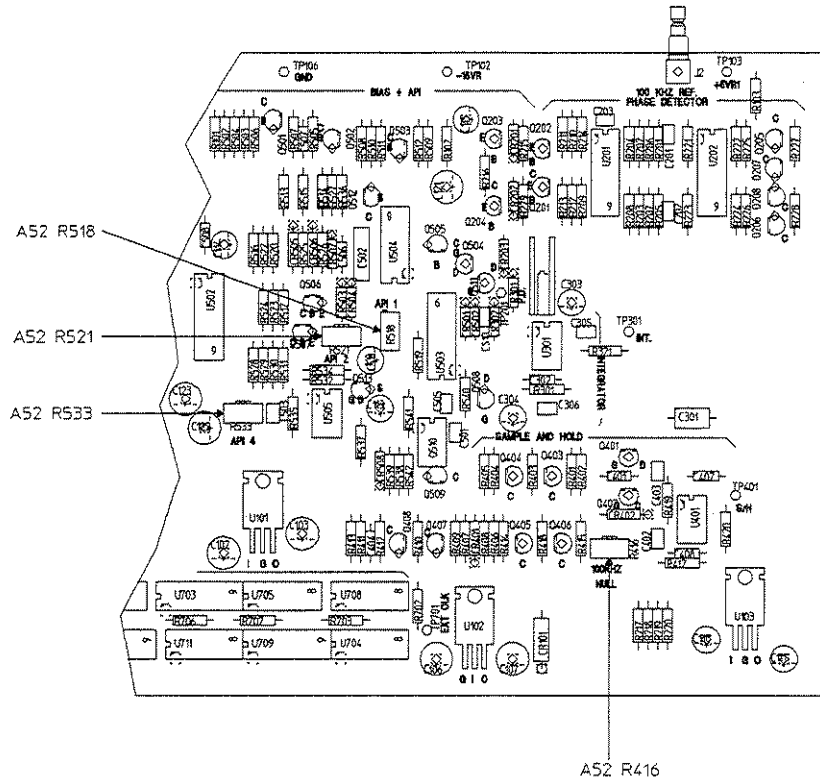


Figure 1-3. A52 Fractional-N Component Locator

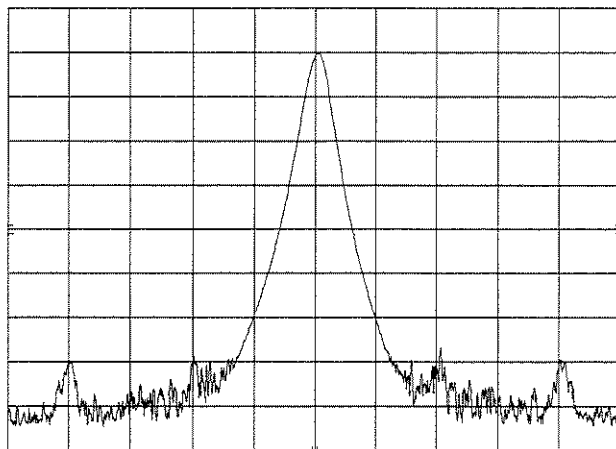


Figure 1-4. Spurs Out of Adjustment

6. 100 kHz and API Spurs

7. Set the spectrum analyzer as follows:

| | |
|------------------|------------|
| Center Frequency | 400.03 MHz |
| Frequency Span | 25 kHz |
| Res BW | 300 Hz |
| Video BW | 300 Hz |
| Sweeptime | 1 sec |

8. Press the [API 1] softkey.
9. Adjust API 1 (A52 R518) for a minimum spur level at 400.033 MHz.
10. Change the spectrum analyzer's center frequency to 400.003 MHz.
11. Press the [API 2] softkey.
12. Adjust API 2 (A52 R521) for a minimum spur level at 400.006 MHz.
13. Change the spectrum analyzer's center frequency to 400.0001 MHz.
14. Press the [API 4] softkey.
15. Adjust API 4 (A52 R533) for a minimum spur level at 400.00303 MHz.
16. Set the power switch to STANDBY (⓪). Place the Fractional-N assembly into the card nest, and replace the screws.
17. Reconnect the following using original cables:
 - A52 J1 to A51 J3
 - A52 J2 to A33 J4
 - A62 J1 to A33 J3
 - A62 J2 to A31 J8
 - A21 J2 to A42 J2
 - A33 J5 to TRIG OUT (white cable)
 - A33 J6 to EXT TRIG (black cable)

7. Sum VCO Filter

This procedure adjusts the low pass filter on the A21 Sum VCO assembly. This filter improves spectral purity of the VCO.

Equipment Required:

- Spectrum Analyzer
- Extender Board
- Extender Cable
- BNC(m)-to-SMB(f) Cable

1. Set the power switch to STANDBY (⓪). Remove the screw at each end of the A21 Sum VCO assembly, and place the assembly on an extender board.
2. Reconnect A21 J1 to A51 J2 using an extender cable. (A11 J2 to A31 J1 may be left unconnected.)
3. Connect the spectrum analyzer to A21 J2 using a BNC-to-SMB cable.
4. Set the power switch to ON (I), then press the following keys:
 - [**Spcl Fctn**]
 - [] (second softkey from bottom)
 - 99
 - [] (second softkey from bottom)
 - [SERVICE FUNCTIONS]
 - [ADJUSTMTS]
 - [LOCAL OSC]
 - [SUM VCO LOW PASS]
5. Press the [**Preset**] hardkey, then set the spectrum analyzer as follows:

| | |
|------------------|---------|
| Center Frequency | 380 MHz |
| Frequency Span | 200 MHz |
| Reference Level | – 5 dBm |
| dB per Division | 1 dB |
| Maximum Hold | On |
6. Through the holes in the shield can, alternately adjust A21 L106 and L107 (see figure 1-5) for a flatness (maximum amplitude minus minimum amplitude) of less than 3 dB(p-p). During this adjustment, periodically clear the spectrum analyzer's maximum hold function.

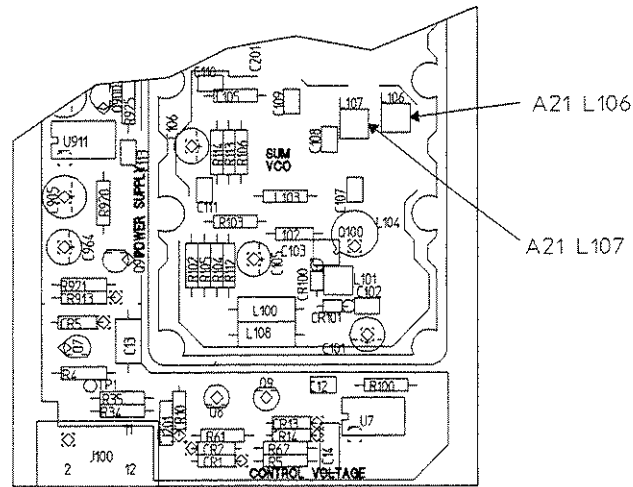


Figure 1-5. A21 Sum VCO Component Locator

7. Set the power switch to STANDBY (ϕ). Place the Sum VCO assembly into the card nest, and replace the screws.
8. Reconnect the following using original cables:
 - A21 J1 to A51 J2
 - A21 J2 to A42 J2
 - A21 J3 to A12 J1
 - A21 J4 to A22 J1
 - A11 J2 to A31 J1

9. Step VCO Filter

This procedure adjusts the low pass filter on the A24 Step VCO assembly. This filter improves the spectral purity of the VCO.

Equipment Required:

- Spectrum Analyzer
- Extender Board
- Extender Cable
- BNC(m)-to-SMB(f) Cable

1. Connect the spectrum analyzer to A24 J2 using a BNC-to-SMB cable.
2. Set the power switch to ON (1), then press the following keys:

[Spcl Fctn]

[] (second softkey from bottom)

– 99

[] (second softkey from bottom)

[SERVICE FUNCTIONS]

[ADJUSTMTS]

[LOCAL OSC]

[STEP VCO LOW PASS]

3. Press the [Preset] hardkey, then set the spectrum analyzer as follows:

| | |
|------------------|----------|
| Center Frequency | 380 MHz |
| Frequency Span | 200 MHz |
| Reference Level | – 20 dBm |
| dB per Division | 1 dB |
| Maximum Hold | On |

4. If the flatness (maximum amplitude minus minimum amplitude) of the displayed signal is less than 3 dB(p-p), the step VCO filter is within tolerance and should not be adjusted. Disconnect the spectrum analyzer from A24 J2.
5. If the flatness (maximum amplitude minus minimum amplitude) of the displayed signal is larger than 3 dB(p-p), do the following:
 - a. Set the power switch to STANDBY (0). Remove the screw at each end of the A24 Step VCO assembly, and place the assembly on an extender board.
 - b. Reconnect A24 J3 to A23 J1 using an extender cable.
 - c. Reconnect the spectrum analyzer to A24 J2 using a BNC-to-SMB cable.

d. Set the power switch to ON (I), then press the following keys:

[Spcl Fctn]

[] (second softkey from bottom)

- 99

[] (second softkey from bottom)

[SERVICE FUNCTIONS]

[ADJUSTMTS]

[LOCAL OSC]

[STEP VCO LOW PASS]

e. Through the holes in the shield can, alternately adjust A24 L506 and L507 (see figure 1-6) for a flatness (maximum amplitude minus minimum amplitude) of less than 3 dB(p-p). During this adjustment, periodically clear the spectrum analyzer's maximum hold function.

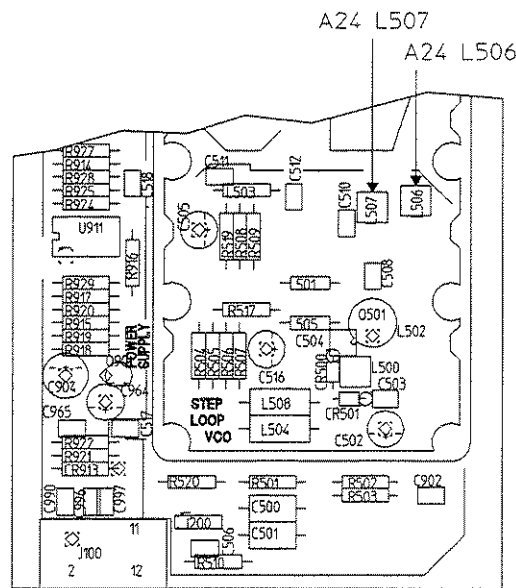


Figure 1-6. A24 Step VCO Component Locator

f. Set the power switch to STANDBY (O). Place the Step VCO assembly into the card nest, and replace the screws.

g. Reconnect the following using original cables:

A24 J1 to A22 J2

A24 J2 (no connection)

A24 J3 to A23 J1

10. Press the following keys:

[**Preset**]
[**Sweep**]
[SWEEP AUTO **MAN**]
[MANUAL FREQ]
30
[MHz]

11. The counter readout should be 336 ± 1 MHz. If the counter readout is not within tolerance, do the following:

a. Press the following keys:

[**Spcl Fctn**]
[SERVICE FUNCTIONS]
[ADJUSTMTS]
[LOCAL OSC]
[PRETUNE SLOPE]

b. Adjust PRETUNE SLOPE (A23 R457) for 305.6 ± 0.1 MHz.

c. Repeat steps 5 through 11 until all are within tolerance without adjustment.

d. Press the [**Preset**] hardkey to exit the adjustment mode.

12. Disconnect the frequency counter from A21 J3.

13. Reconnect A21 J3 to A12 J1 and A22 J3 to A51 J1.

11. ADC Gain, Offset, and Reference

This procedure adjusts the second-pass gain, the first-pass offset, and the reference voltage for the ADC on the A62 ADC/Digital Filter assembly.

| | |
|---------------------|------------------------|
| Equipment Required: | Oscilloscope |
| | 1:1 Oscilloscope Probe |
| | Synthesizer |
| | Extender Board |
| | Extender Cables |
| | BNC(m)-to-SMB(f) Cable |
| | Capacitive Load |
| | BNC Cable |

Note



Although a digital oscilloscope is listed in the recommended equipment list, this adjustment may be easier using an analog oscilloscope.

-
1. Set the power switch to STANDBY (ϕ). Remove the screw at each end of the A62 ADC/Digital Filter assembly, and place the assembly on an extender board.
 2. Reconnect A62 J1 to A33 J3 and A62 J2 to A31 J8 using extender cables. Reconnect the fast bus cable to A62 J5 using the fast bus extender cable.
 3. Connect the oscilloscope to A62 TP400 (see figure 1-7) using a capacitive load and a 1:1 oscilloscope probe. Connect the probe ground clip to TP 505 (AGND).

11. ADC Gain, Offset, and Reference

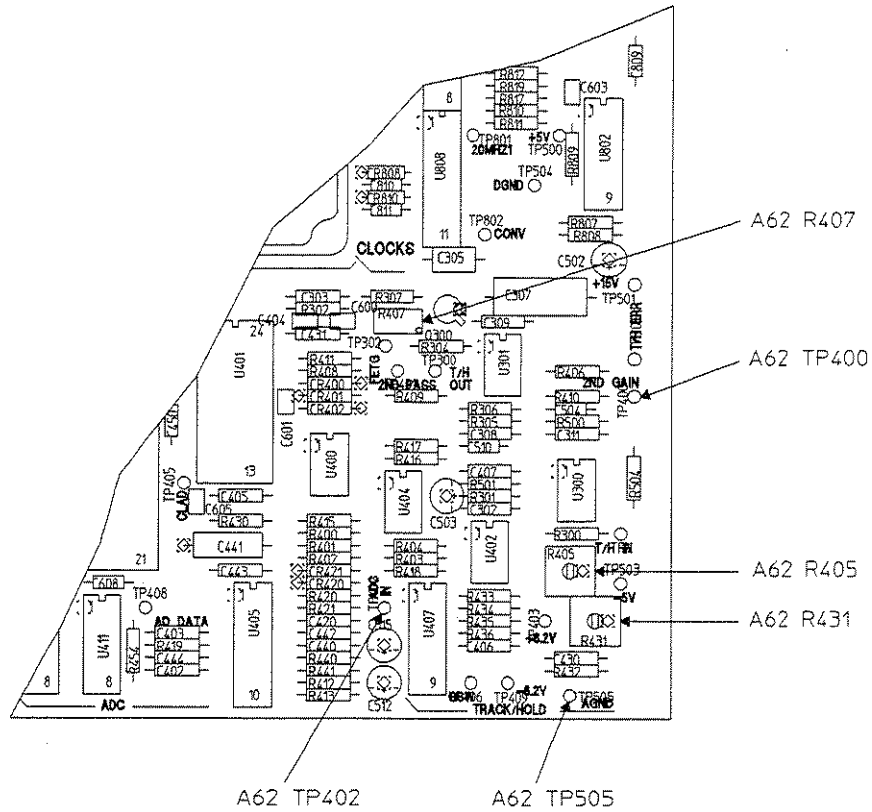


Figure 1-7. A 62 ADC/Digital Filter Component Locator

4. Connect the synthesizer to A62 J3 using a BNC-to-SMB cable.

Note



A 50Ω termination is required for synthesizers with 50Ω output impedance.

5. Connect the synthesizer's synchronous output to either the oscilloscope's channel 2 input or external trigger input using a BNC cable.
6. Set the synthesizer as follows:

| | |
|-----------|-----------|
| Function | Sine Wave |
| Frequency | 1 kHz |
| Amplitude | 10 mVrms |

11. ADC Gain, Offset, and Reference

7. Set the oscilloscope as follows:

| | | |
|-----------|------------|--------------------------|
| Channel 1 | Volts/Div | 20 mV/div |
| | Offset | 0V |
| | Coupling | 1 M Ω ac |
| Channel 2 | Volts/Div | 500 mV/div |
| | Offset | 0V |
| | Coupling | 1 M Ω ac |
| Time Base | Time/Div | 1.0 ms/div |
| | Sweep | Triggered |
| | Level | 500 mV |
| Trigger | Slope | Positive |
| | Mode | Edge |
| | Source | Channel 2 or Ext Trigger |
| Display | Mode | Repetitive |
| | Averaging | On |
| | No. of Avg | 8 |
| | Screen | Single |

8. Set the power switch to ON (1), then press the following keys:

[Spcl Fctn]

[] (second softkey from bottom)

- 99

[] (second softkey from bottom)

[SERVICE FUNCTIONS]

[ADJUSTMTS]

[ADC]

[ADC 2ND PASS GAIN]

9. Adjust A62 R407 for a flat trace on the oscilloscope display.

10. Remove the capacitive load from the oscilloscope, and connect the oscilloscope probe to A62 TP402.

11. Change the set up for the oscilloscope as follows:

| | | |
|-----------|-------------|-----------------|
| Channel 1 | Volts/Div | 100 mV/div |
| | Coupling | 1 M Ω dc |
| Channel 2 | Coupling | 1 M Ω dc |
| | Time Base | Time/Div |
| Display | Averaging | Off |
| | Persistence | 2.00s |

12. Increase the synthesizer's amplitude to 400 mVrms.

13. Press the [ADC OFFSET & REFERNC] softkey.

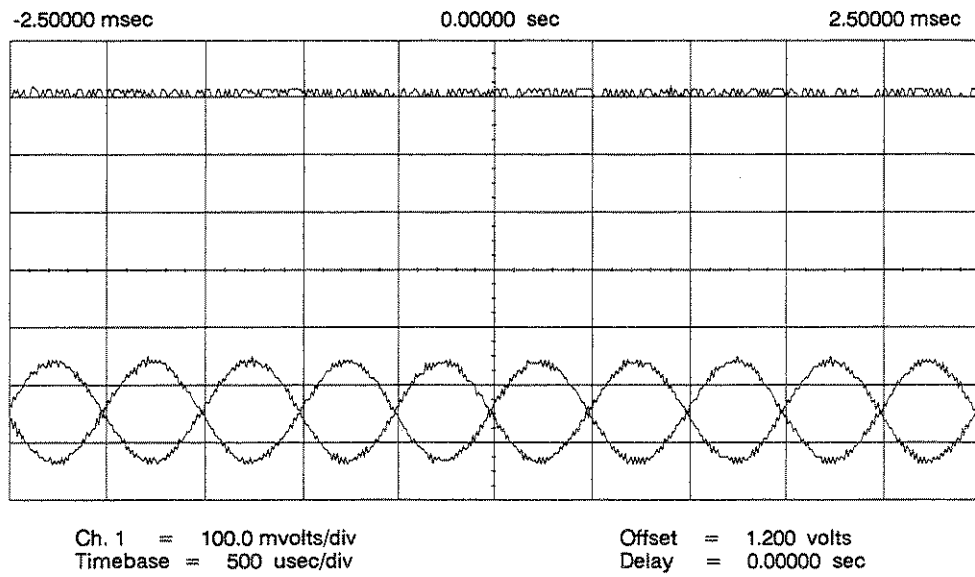


Figure 1-9. R431 and R405 Incorrectly Adjusted

b. If the oscilloscope display looks like figure 1-10, adjust A62 R405 to position the flat trace at the center of the sine wave trace as shown in figure 1-8.

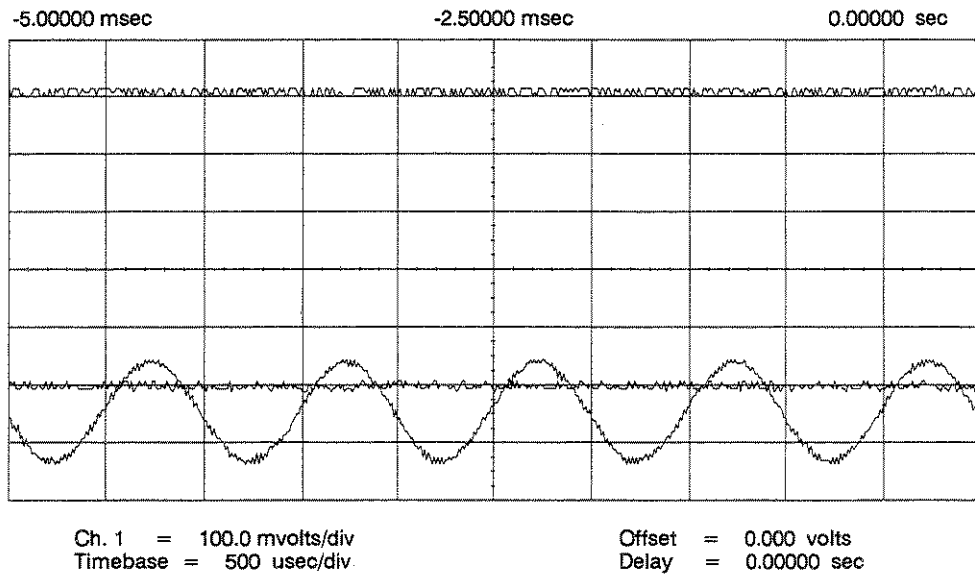


Figure 1-10. R405 Incorrectly Adjusted

15. Set the power switch to STANDBY (0). Place the ADC/Digital Filter assembly into the card nest, and replace the screws.
16. Reconnect the following using original cables:
 - A62 J1 to A33 J3
 - A62 J2 to A31 J8
 - A62 J3 to A61 J3

12. Second IF Bandpass Filter

This procedure adjusts the second IF bandpass filter on the A61 IF assembly. This 10.1875 MHz bandpass filter attenuates signals outside the passband.

Equipment Required:

- Spectrum Analyzer
- Extender Board
- Extender Cables
- BNC Cable
- SMB(m)-to-SMB(m) Adapter

1. Set the power switch to STANDBY (ϕ). Remove the screw at each end of the A61 IF assembly, and place the assembly on an extender board.
2. Reconnect the following using extender cables (connecting A61 J1 to A13 J3 requires using two extender cables and an adapter):

- A61 J1 to A13 J3
- A61 J2 to A31 J3
- A61 J3 to A62 J3

3. Set the power switch to ON (1), then press the following keys:

[Spcl Fctn]
[] (second softkey from bottom)
– 99
[] (second softkey from bottom)
[SERVICE FUNCTIONS]
[ADJUSTMTS]
[RECEIVER IF]
[2nd IF1]

Note



During this adjustment, the reference level automatically changes when the signal reaches the top or bottom of the displayed range. The analyzer beeps to indicate that the reference level changed.

4. Adjust A61 L3, L4, L5, L6, L8, L9, and L10 from the circuit side of the board (see figure 1-11 for component location) for a maximum **Man** readout (approximately – 20 dBm). Continue adjusting until no further improvement can be made.

Note

If the signal is below the displayed range, continue to adjust. The signal is not seen when the filter is too far out of adjustment.

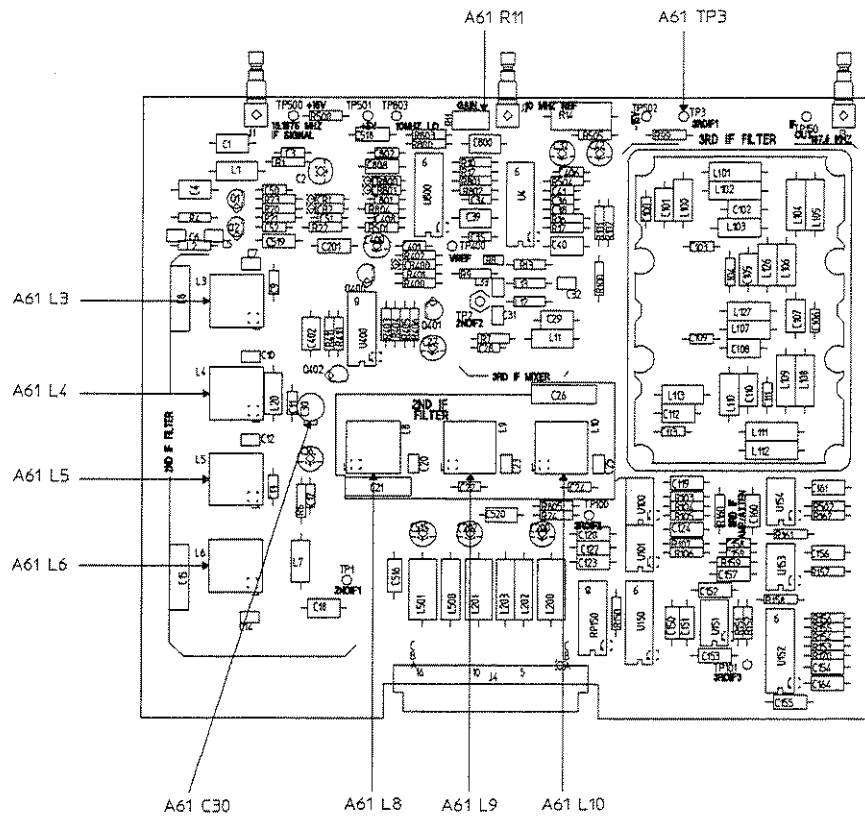


Figure 1-11. A61 IF Component Locator

5. Press the [2nd IF2] softkey.
6. Connect REF OUT (10 MHz) on the rear panel to INPUT on the front panel using a BNC cable.
7. Adjust A61 C30 for a minimum **Man** readout.
8. Press the [2nd IF3] softkey.
9. Alternately adjust A61 L4 and L5 for a maximum **Man** readout.
10. Press the [2nd IF4] softkey.

12. Second IF Bandpass Filter

11. Alternately adjust A61 L4 and L5 to center the peak and equalize the level of the sides (see figure 1-12).

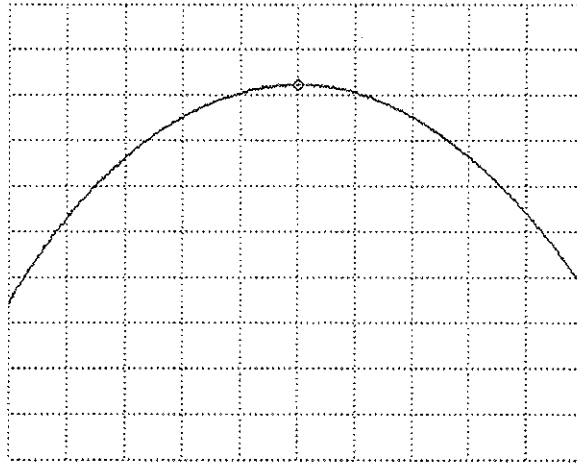


Figure 1-12. Second IF Adjustment

12. Set the spectrum analyzer as follows:

| | |
|------------------|--------------|
| Input | 1 M Ω |
| Center Frequency | 187.5 kHz |
| Span | 10 kHz |
| Scale | 0 dBV |

13. Connect the spectrum analyzer to A61 TP3 using a 1:1 oscilloscope probe.
14. Press the [2nd IF5] softkey.
15. Adjust A61 R11 for -32.0 ± 0.1 dBV.
16. Set the power switch to STANDBY (ϕ). Place the IF assembly into the card nest, and replace the screws.
17. Reconnect the following using original cables:
 - A61 J1 to A13 J3
 - A61 J2 to A31 J3
 - A61 J3 to A62 J3

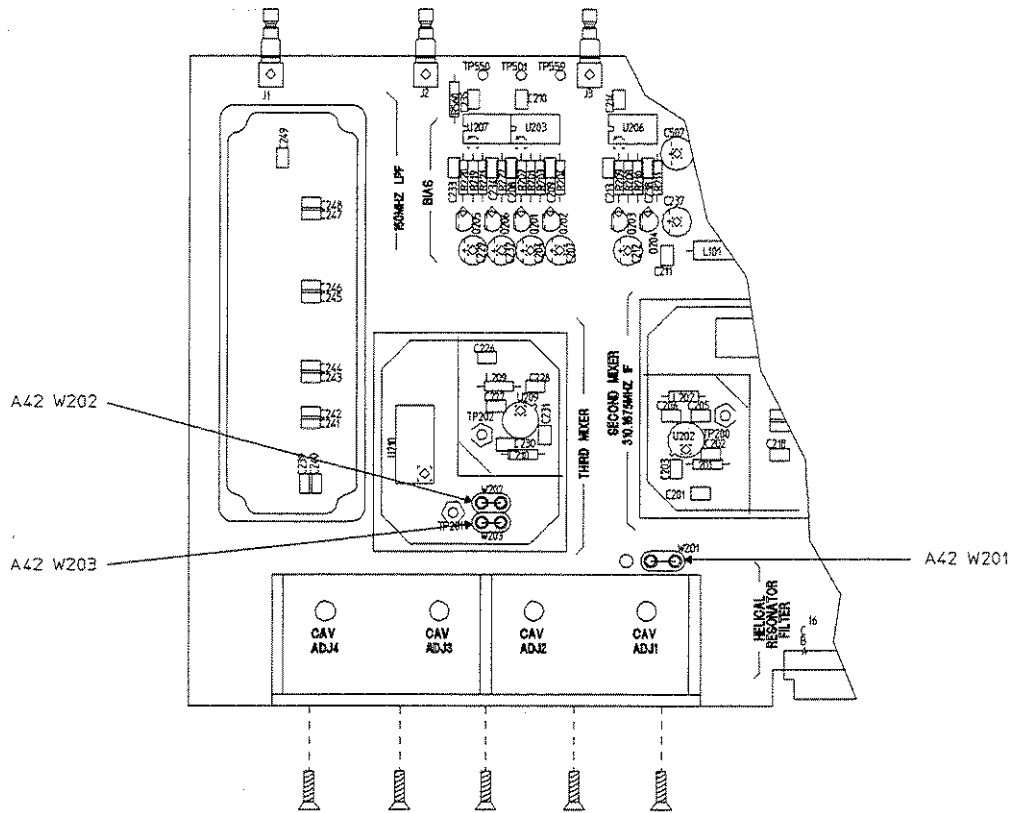


Figure 1-13. A42 Source Conversion Component Locator

3. Remove the plate covering the helix cavity. Then using a ball driver hex tool, turn all four tuning screws (CAV ADJ 1, 2, 3, and 4) clockwise until the screws just contact the helix structure inside the cavity (see caution below). Replace the plate covering the helix cavity.

Caution



The helix structure will be damaged if the tuning screws are turned in too far. Be careful to only turn the screws until they just touch the helix structure inside the cavity.

4. Place the A42 Source Conversion assembly on an extender board.
5. Reconnect the following using extender cables:

- A42 J1 to A41 J3
- A42 J2 to A21 J2
- A42 J3 to A32 J3
- A42 J4 to A31 J5
- A42 J6 to A33 J2
- A52 J2 to A33 J4
- A62 J1 to A33 J3

6. Set the power switch to ON (1), then press the following keys:

[Spcl Fctn]

[] (second softkey from bottom)

– 99

[] (second softkey from bottom)

[SERVICE FUNCTIONS]

[ADJUSTMTS]

[SOURCE]

[HELICAL RESONATOR]

Note



During this adjustment, the reference level automatically changes when the signal reaches the top or bottom of the displayed range. The analyzer beeps to indicate that the reference level changed.

7. Adjust CAV ADJ 1 counterclockwise for a maximum signal level.
8. Adjust CAV ADJ 2 counterclockwise for a minimum signal level. (The minimum level should be about 15 dB smaller than the maximum level achieved in the previous step.)
9. Adjust CAV ADJ 3 counterclockwise for a maximum signal level.
10. Adjust CAV ADJ 4 counterclockwise for a minimum signal level.
11. Set the power switch to STANDBY (⓪). Return W201, W202, and W203 to their original positions. Replace the shield can.
12. Place the Source Conversion assembly into the card nest, and replace the screws.
13. Reconnect the following using original cables:
 - A42 J1 to A41 J3
 - A42 J2 to A21 J2
 - A42 J3 to A32 J3
 - A42 J4 to A31 J5
 - A42 J6 to A33 J2
 - A52 J2 to A33 J4
 - A62 J1 to A33 J3
 - A33 J5 to TRIG OUT (white cable)
 - A33 J6 to EXT TRIG (black cable)

3. Remove the plate covering the helix cavity. Then using a ball driver hex tool, turn all four tuning screws (CAV ADJ 1, 2, 3, and 4) clockwise until the screws just contact the helix structure inside the cavity (see caution below). Replace the plate covering the helix cavity.

Caution

The helix structure will be damaged if the tuning screws are turned in too far. Be careful to only turn the screws until they just touch the helix structure inside the cavity.

4. Place the assembly on an extender board.
5. Reconnect the following using extender cables:
 - A12 J1 to A21 J3
 - A12 J2 to A11 J3
 - A12 J3 to A13 J2
6. Set the power switch to ON (1), then press the following keys:

[Spcl Fctn]

[] (second softkey from bottom)

– 99

[] (second softkey from bottom)

[SERVICE FUNCTIONS]

[ADJUSTMNTS]

[RECEIVER IF]

[HELICAL RESONATOR]

Note

During this adjustment, the reference level automatically changes when the signal reaches the top or bottom of the displayed range. The analyzer beeps to indicate that the reference level changed.

7. Adjust CAV ADJ 1 counterclockwise for a maximum signal level.
8. Adjust CAV ADJ 2 counterclockwise for a minimum signal level. (The minimum level should be about 15 dB smaller than the maximum level achieved in the previous step.)
9. Adjust CAV ADJ 3 counterclockwise for a maximum signal level.
10. Adjust CAV ADJ 4 counterclockwise for a minimum signal level.

14. First IF Bandpass Filter

11. Set the power switch to STANDBY (⓪). Return W801, W802, and W803 to their original positions.
12. Place the First Conversion assembly into the card nest, and replace the screws.
13. Reconnect the following using original cables:
 - A12 J1 to A21 J3
 - A12 J2 to A11 J3
 - A12 J3 to A13 J2

15. Autorange Threshold Adjustment

Equipment Required:

- Frequency Synthesizer
- Extender Board
- Extender Cables
- BNC(m) to SMB(f) Cable
- SMB(m) to SMB(m) Adapter

1. Set the power switch to STANDBY (⓪). Remove the screw at each end of the A11 Input assembly, and remove the assembly from the cardnest
2. Using the BNC-to-SMB cable and adapter, connect the frequency synthesizer to A11 J4 (SMB connector at the bottom of the A11 assembly). Place the assembly on an extender board.
3. Turn A11 R626 fully counterclockwise.
4. Reconnect the following using extender cables:
 - A11 J1 to A41 J1
 - A11 J2 to A31 J1
 - A11 J3 to A12 J2
5. Set the power switch to ON (I), wait for the calibration to complete, then press the following keys:
 - [Spcl Fctn]
 - [AUTO CAL OFF]
 - [Range/Input]
 - [RANGE]
 - 20
 - [dBm]
6. Set the frequency synthesizer for a 10 MHz, - 18.5 dBm sine wave output.
7. Adjust A11 R624 so that A11 CR606 just lights up, indicating that the upper threshold trip point was reached. (Turn A11 R624 counterclockwise to light A11 CR606.)
8. Change the frequency synthesizer amplitude to - 31.5 dBm.
9. Adjust A11 R626 so that A11 CR607 just lights up, indicating that the lower threshold trip point was reached. (Turn A11 R626 clockwise to light A11 CR607.)
10. Set the power switch to STANDBY (⓪). Place the A11 Input assembly into the cardnest, and replace the screws.
11. Reconnect the following using the original cables:
 - A11 J1 to A41 J1
 - A11 J2 to A31 J1
 - A11 J3 to A12 J2

16. 1 Meg Ohm Flatness

This procedure adjusts the flatness of the frequency response of the 1 M Ω buffer on the A11 Input assembly.

Equipment Required:

- Extender Board
- Extender Cables
- Small Adjustment Tool
- 50 Ω Feedthrough Termination
- BNC(m)-to-SMB(f) Cable
- SMB(m)-to-SMB(m) Adapter

1. Set the power switch to STANDBY (ϕ). Remove the screw at each end of the A11 Input assembly, and remove the assembly from the card nest.
2. Connect the 50 Ω feedthrough termination to the SOURCE connector. Using the BNC-to-SMB cable and adapter, connect the feedthrough termination to A11 J4 (SMB connector at bottom of A11 Input assembly). Place the assembly on an extender board.
3. Reconnect the following using extender cables:
 - A11 J1 to A41 J1
 - A11 J2 to A31 J1
 - A11 J3 to A12 J2
4. Set the power switch to ON (1), then press the following keys:
 - [Spcl Fctn]
 - [] (second softkey from bottom)
 - 99
 - [] (second softkey from bottom)
 - [SERVICE FUNCTIONS]
 - [ADJUSTMTS]
 - [RECEIVER INPUT]
 - [1 MOHM FLATNESS]

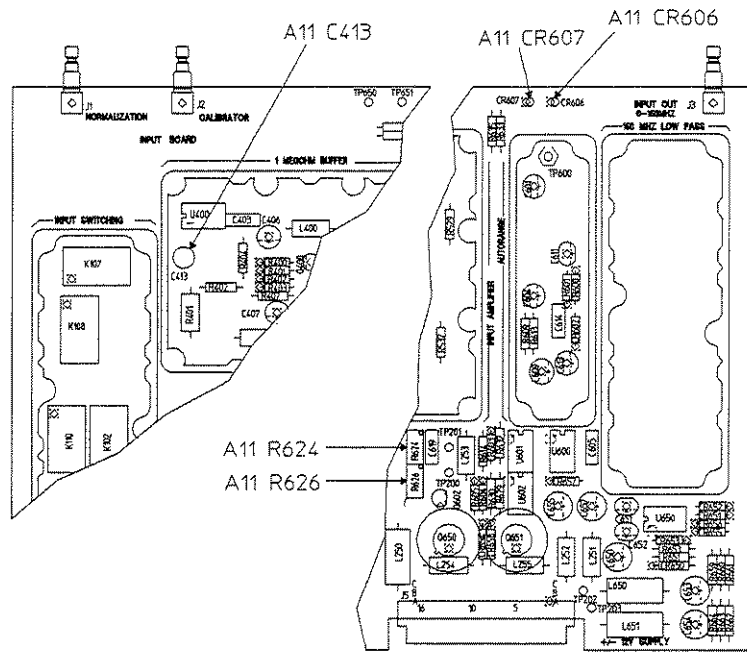


Figure 1-15. A11 Input Component Locator

5. Using the small adjustment tool in the service kit, adjust A11 C413 through a hole in the shield can so the displayed waveforms are as close as possible without the ends crossing (see figure 1-16).

Adjustments
16. 1 Meg Ohm Flatness

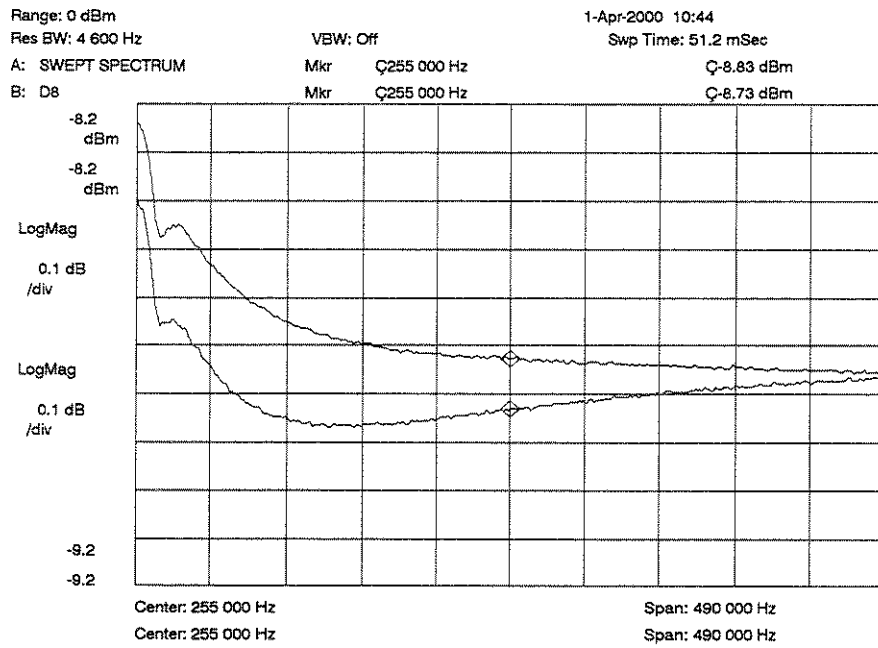


Figure 1-16. 1 Meg Ohm Flatness Adjustment

6. Set the power switch to STANDBY (⓪). Place the Input assembly into the card nest, and replace the screws.
7. Reconnect the following using original cables:
 - A11 J1 to A41 J1
 - A11 J2 to A31 J1
 - A11 J3 to A12 J2

17. Oven Frequency

6. Remove the oven screw and adjust COARSE FREQUENCY ADJUST (A91 U3) for a stable (not moving) display on the oscilloscope.
7. Change the oscilloscope timebase to 10 ns per division.
8. Adjust FINE FREQUENCY ADJUST for a stable (not moving) display on the oscilloscope.
9. Return the oven screw, oven-adjustment cover and screw, and rear panel jumper (OVEN REF OUT to EXT REF IN) to their original positions.

18. Calibrator Flatness and Level

7. While monitoring the **Man** readout, adjust CAL LEVEL (A31 R322) for the value indicated in the message on the display.
8. Disconnect the BNC cable from the INPUT connector and reconnect to the power meter (SOURCE connected to power meter).

Note

If you are using a standard power meter, set its calibration factor for 120 MHz to improve the accuracy of this adjustment.

9. Press the [CAL FLATNESS] softkey.
10. After the message appears on the screen, press the [SRCE DAC ATTEN] softkey and adjust the attenuation level for a 0 dBm \pm 0.01 dB readout on the power meter.
11. Press the [NEXT STEP] softkey.
12. Disconnect the BNC cable from the power meter and reconnect to the INPUT connector (SOURCE connected to INPUT).
13. After the **Man** readout is stable, press the [NEXT STEP] softkey.
14. While monitoring the **Man** readout, adjust CAL FLAT (A31 C330) for the value indicated in the message on the display.
15. Disconnect the cable connected between the SOURCE connector and INPUT connector.
16. Press the [**Preset**] hardkey to exit the adjustment mode.

19. Display

This procedure adjusts the focus, intensity, and alignment of the Display assembly.

Equipment Required: None

Note



If the Display assembly needs to be adjusted, adjust only the components that apply to the problem.

1. Press the following keys to view the test pattern:

[Spcl Fctn]

[] (second softkey from bottom)

– 99

[] (second softkey from bottom)

[SERVICE FUNCTIONS]

[SELF TEST]

[FUNCTIONL TESTS]

[DISPLAY]

[TEST PATTERN]

2. Compare the test pattern to figure 1-17 and adjust as indicated in table 1-3.

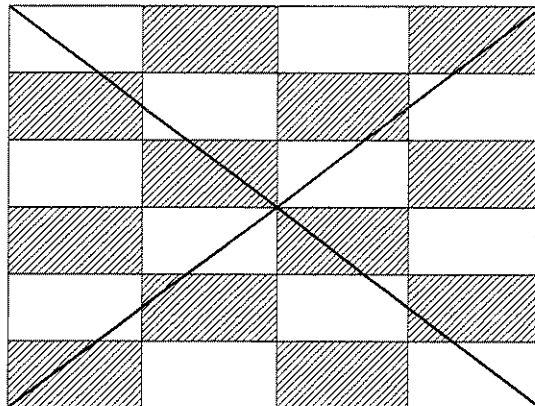


Figure 1-17. Center Portion of Display Test Pattern

Table 1-3. Display Adjustments

| Adjustment Name | Adjust for... |
|---------------------|---|
| Focus | Optimum focus |
| Brightness | Optimum intensity |
| Horizontal Width † | Test pattern width of 6.89 ± 0.06 inches (175 ± 1.5 mm) |
| Vertical Hold | Vertically stable display |
| Vertical Linearity | Uniform height of blocks in test pattern |
| Vertical Position | Vertically centered test pattern |
| Vertical Size | Test pattern height of 4.92 ± 0.06 inches (128 ± 1.5 mm) |
| Horizontal Position | Horizontally centered test pattern |
| Horizontal Hold | Horizontally stable display |

† Adjust using non-metallic hexagonal tuning tool.

Note



If Vertical Linearity is adjusted, check Vertical Size and Vertical Position, and adjust if necessary.

-
3. Press the [**Preset**] hardkey to exit the adjustment mode.

Replaceable Parts

Introduction

This section contains information for ordering replacement parts for the HP 3588A Spectrum Analyzer. This section also contains illustrations showing how to disassembly and assembly the analyzer. These illustrations also show reference designator numbers for the hardware.

Replacement parts are listed in the following three tables:

- Assemblies
- Cables
- Hardware

Caution



Many of the parts listed in this section are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unnecessary damage.

Ordering Information

Note



See the final pages in the back of this manual for a list of Hewlett-Packard sales and service office locations and addresses.

Ordering Non-Listed Parts

To order a part that is NOT listed in the replaceable parts tables, indicate the instrument model number, instrument serial number, description and function of the part, and the quantity of the part required. Address the order to the nearest Hewlett-Packard sales and service office.

Direct Mail Order System

Within the U.S.A., Hewlett-Packard can supply parts through a direct mail order system. Advantages of the Direct Mail Order System are:

- Direct ordering and shipment from the HP Parts Center.
- No maximum or minimum on any mail order. There is a minimum order for parts ordered through a local HP sales and service office when the orders require billing and invoicing.
- Transportation charges are prepaid. A small handling charge is added to each order.
- No invoicing. A check or money order must accompany each order.
- Mail order forms and specific ordering information are available through your local Hewlett-Packard sales and service office.

Table 2-1. Abbreviations Used

| Abbreviations | |
|------------------|---|
| Ag | silver |
| Al | aluminum |
| A | ampere(s) |
| Au | gold |
| cer | ceramic |
| coef | coefficient |
| com | common |
| conn | connection |
| dep | deposited |
| DPDT | double-pole double-throw |
| DPST | double-pole single-throw |
| elect | electrolytic |
| encap | encapsulated |
| F | farad(s) |
| FET | field effect transistor |
| fxd | fixed |
| GaAs* | gallium arsenide |
| GHz | gigahertz = 10^{+9} hertz |
| Gd | guard(ed) |
| Ge | germanium |
| gnd | ground(ed) |
| H | henry(ies) |
| Hg | mercury |
| Hz | hertz (cycle(s) per second) |
| ID | inside diameter |
| impgr | impregnated |
| incd | incandescent |
| ins | insulation(ed) |
| k Ω | kilohm(s) = 10^{+3} ohms |
| kHz | kilohertz = 10^{+3} hertz |
| L | inductor |
| lin | linear taper |
| log | logarithmic taper |
| mA | milliamper(s) = 10^{-3} amperes |
| MHz | megahertz = 10^{+6} hertz |
| M Ω | megohms(s) = 10^{+6} ohms |
| met flm | metal film |
| mfr | manufacturer |
| ms | microsecond |
| mtg | mounting |
| mV | millivolt(s) = 10^{-6} volts |
| μ F | microfarad(s) |
| μ s | microsecond(s) |
| μ V | microvolt(s) = 10^{-6} volts |
| my | Mylar® |
| nA | nanoampere(s) = 10^{-9} amperes |
| NC | normally closed |
| Ne | neon |
| NO | normally open |
| NPO | negative positive zero (zero temperature coefficient) |
| ns | nanosecond(s) = 10^{-9} seconds |
| nsr | not separately replaceable |
| obd | order by description |
| OD | outside diameter |
| p | peak |
| pc | printed circuit |
| pF | picofarad(s) 10^{-12} farads |
| piv | peak inverse voltage |
| p/o | part of |
| pos | position(s) |
| poly | polystyrene |
| pot | potentiometer |
| p-p | peak-to-peak |
| ppm | parts per million |
| prec | precision (temperature coefficient long term stability and/or tolerance) |
| R | resistor |
| Rh | rhodium |
| rms | root-mean-square |
| rot | rotary |
| Se | selenium |
| sect | section(s) |
| Si | silicon |
| sl | slide |
| SPDT | single-pole double-throw |
| SPST | single-pole single-throw |
| Ta | tantalum |
| TC | temperature coefficient |
| TiO ₂ | titanium dioxide |
| tog | toggle |
| tol | tolerance |
| trim | trimmer |
| TSTR | transistor |
| V | volt(s) |
| vacw | alternating current working voltage |
| var | variable |
| vdcw | direct current working voltage |
| W | watts |
| w/ | with |
| wiv | working inverse voltage |
| w/o | without |
| ww | wirewound |

* optimum value selected at factory average value shown (part may be omitted)

**no standard type assigned selected or special type

® Dupont de Nemours

Table 2-1. Abbreviations Used (continued)

| Designators | | | |
|-------------|----------------------|-----|------------------|
| A | assembly | Q | transistor |
| B | motor | QCR | transistor-diode |
| BT | battery | R | resistor |
| C | capacitor | RT | thermistor |
| CR | diode or thyristor | S | switch |
| DL | delay line | T | transformer |
| DS | lamp | TB | terminal board |
| E | misc electronic part | TC | thermocouple |
| F | fuse | TP | test point |
| FL | filter | TS | terminal strip |
| HR | heater | U | microcircuit |
| IC | integrated circuit | V | vacuum tube |
| J | jack | W | cable jumper |
| K | relay | X | socket |
| L | inductor | XDS | lampholder |
| M | meter | XF | fuseholder |
| MP | mechanical part | Y | crystal |
| P | plug | Z | network |

Table 2-2. Manufacturers' Code Numbers

| Mfr No. | Mfr Name | Address |
|----------------|---------------------------------|-------------------------|
| 01075 | ITT Pomona Electronics | Pomona, CA 91766 |
| 01125 | Lewis Screw Co | Chicago, IL 60609 |
| 01440 | Pool Machine Co Inc | Denver, CO 80223 |
| 01642 | Sons Tool Inc | Woodville, WI 55412 |
| 01808 | Small Parts Inc | Costa Mesa, CA 92626 |
| 03316 | Specialty Connector Co | Franklin, IN 46131 |
| 03480 | Heyco Molded Products | Kentworth, NJ 07033 |
| 05030 | Barry Div Barry Wright Corp | Watertown, MA 02172 |
| 05502 | Connor Springs and Mfg Co | San Francisco, CA 94101 |
| 05791 | Griffith Rubber Mills | Portland, OR 97210 |
| 06915 | Pan Asian Paper Product Mfg | Pinang, MA |
| 06916 | Sony Corp | Toyko, JP |
| 08709 | Panasonic Industrial Co | Secaucus, NJ 07094 |
| 08891 | Power Conversion Inc | Mt Vernon, NY 10551 |
| 09328 | Dreefs Switch Inc | Waukegan, IL 60087 |
| 09441 | Applied Engineering Product Co | Hamden CT 06514 |
| 09655 | Chomerics Shielding Technology | Carson, CA 90749 |
| 12136 | Solitec Inc | Santa Clara, CA 95054 |
| 28480 | Hewlett-Packard Company | Palo Alto, CA 94304 |
| 30817 | Instrument Specialties Co Inc | Del Water Gap, PA 07424 |
| 34785 | Dek Inc | Chicago, IL 60185 |
| 3U116 | TRW Electronic Components Group | Marshall, IL 62441 |
| 46384 | Penn Engineering and Mfg Corp | Doylestown, PA 18901 |
| 73734 | Federal Screw Products Co | Chicago, IL 60618 |
| 75915 | Littelfuse Inc | Des Plaines, IL 60016 |
| 76381 | 3M Co | St Paul, MN 55144 |
| 83486 | Elco Industries Inc | Rockford, IL 61125 |

Assemblies

To order an assembly listed in table 2-3, quote the Hewlett-Packard part number, the check digit (CD), indicate the quantity required, and address the order to the nearest Hewlett-Packard sales and service office. The check digit verifies that an order has been transmitted correctly, ensuring accurate and timely processing of the order. The first time a part is listed in the table, the quantity column lists the total quantity of the part used in the analyzer. See table 2-2 for a table listing the manufacturers' code numbers and the corresponding names and addresses.

Table 2-3. Assemblies

| Ref.Des. | HP Part Number | CD | Qty | Description | Mfr. Code | Mfr. Part Number |
|----------|----------------|----|-----|---|-----------|------------------|
| A11 | 03588-69511 | 3 | 1 | EXCHANGE PCBD ASSY-INPUT † | 28480 | 03588-69511 |
| A12 | 03588-69512 | 4 | 1 | EXCHANGE PCBD ASSY-FIRST CONVERSION † | 28480 | 03588-69512 |
| A13 | 03588-69513 | 5 | 1 | EXCHANGE PCBD ASSY-SECOND CONVERSION † | 28480 | 03588-69513 |
| A21 | 03588-69521 | 5 | 1 | EXCHANGE PCBD ASSY-SUM VCO † | 28480 | 03588-69521 |
| A22 | 03588-69522 | 6 | 1 | EXCHANGE PCBD ASSY-SUM PHASE DETECTOR † | 28480 | 03588-69522 |
| A23 | 03588-69523 | 7 | 1 | EXCHANGE PCBD ASSY-STEP PHASE DETECTOR † | 28480 | 03588-69523 |
| A24 | 03588-69524 | 8 | 1 | EXCHANGE PCBD ASSY-STEP VCO † | 28480 | 03588-69524 |
| A31 | 03588-69531 | 7 | 1 | EXCHANGE PCBD ASSY-REFERENCE/CALIBRATOR † | 28480 | 03588-69531 |
| A32 | 03588-69532 | 8 | 1 | EXCHANGE PCBD ASSY-300 MHz † | 28480 | 03588-69532 |
| A33 | 03588-69533 | 9 | 1 | EXCHANGE PCBD ASSY-TRIGGER † | 28480 | 03588-69533 |
| A41 | 03588-69541 | 9 | 1 | EXCHANGE PCBD ASSY-SOURCE AMPLIFIER † | 28480 | 03588-69541 |
| A42 | 03588-69542 | 0 | 1 | EXCHANGE PCBD ASSY-SOURCE CONVERSION † | 28480 | 03588-69542 |
| A51 | 03588-69551 | 1 | 1 | EXCHANGE PCBD ASSY-INTERPOLATION VCO † | 28480 | 03588-69551 |
| A52 | 03588-69552 | 2 | 1 | EXCHANGE PCBD ASSY-FRACTIONAL-N † | 28480 | 03588-69552 |
| A61 | 03588-69561 | 3 | 1 | EXCHANGE PCBD ASSY-IF † | 28480 | 03588-69561 |
| A62 | 03588-69562 | 4 | 1 | EXCHANGE PCBD ASSY-ADC/DIGITAL FILTER † | 28480 | 03588-69562 |
| A81 | 35672-69581 | 7 | 1 | EXCHANGE PCBD ASSY-CPU ‡ | 28480 | 35672-69581 |
| A87 | 35672-69587 | 3 | 1 | EXCHANGE PCBD ASSY-MEMORY ‡‡ | 28480 | 35672-69587 |
| A88 | 35672-69588 | 4 | 1 | EXCHANGE PCBD ASSY-EXPANDED MEMORY OPT 003 ‡‡ | 28480 | 35672-69588 |
| A90 | 03588-66590 | 2 | 1 | PCBD ASSY-FAN POWER | 28480 | 03588-66590 |
| A91 | 03588-66591 | 9 | 1 | PCBD ASSY-OVEN/FAN POWER OPT 001 † | 28480 | 03588-66591 |
| A99 | 03588-66599 | 1 | 1 | PCBD ASSY-MOTHERBOARD | 28480 | 03588-66599 |
| MP805 | 5080-8600 | 7 | 1 | EXCHANGE DISK DRIVE 3.5" FLEXIBLE Δ | 06916 | MP-F52W-30 |
| MP841 | 35672-67501 | 7 | 1 | POWER SUPPLY CUSTOM 180W-7 OUTPTS | 3U116 | 095-10097-00 |
| MP842 | 35672-69301 | 9 | 1 | DISPLAY 9" RASTER GRN 576X400 | 08709 | TR-94S1A |
| MP859 | 03588-60214 | 1 | 1 | FRONT PANEL ASSY (INCLUDES KEYBOARD) Δ | 28480 | 03588-60214 |
| | 03561-68501 | 8 | 1 | FAN-ASSY | 28480 | 03561-68501 |

† After replacing the assembly, see table 5-2 for required adjustments and performance tests.

‡ See "Replacing the CPU Assembly."

‡‡ See "Replacing the Memory Assembly."

Δ See section 3, "Manual Backdating."

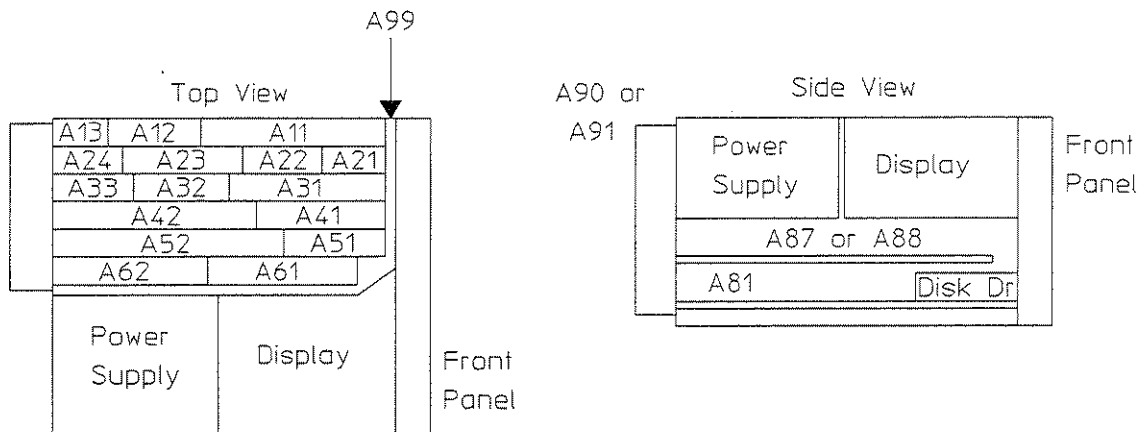


Figure 2-1. Assembly Locations

Replacing the CPU Assembly

The analyzer's serial number and IBASIC option are stored in EEPROM on the CPU assembly. Therefore, when the CPU assembly is replaced, IBASIC must be reinstalled and the analyzer's serial number must be entered in EEPROM. For information on loading IBASIC, see *Using Instrument BASIC with the HP 3588A*. To store the analyzer's serial number, use the HP-IB command, `SYST:EEROM:SNUM 'serial number'`.

For example, if your computer has HP BASIC and the analyzer's HP-IB address is set to 19, enter the following command:

```
OUTPUT 719;"SYST:EEROM:SNUM 'serial number'"
```

Replacing the Memory Assembly

The HP-IB address may need to be reset after replacing the Memory assembly or battery. Press the following keys to reset the HP-IB address:

```
[ Local/HP-IB ]
[ SYSTEM CONTROLLR ]
[ ANALYZER ADDRESS ]
11
[ ENTER ]
```

Cables

To order a part listed in table 2-4, quote the Hewlett-Packard part number, the check digit (CD), indicate the quantity required, and address the order to the nearest Hewlett-Packard sales and service office. The check digit verifies that an order has been transmitted correctly, ensuring accurate and timely processing of the order. The first time a part is listed in the table, the quantity column lists the total quantity of the part used in the analyzer. See table 2-2 for a table listing the manufacturers' code numbers and the corresponding names and addresses.

Table 2-4. Cables

| Ref.Des. | HP Part Number | CD | Qty | Description | Mfr. Code | Mfr. Part Number |
|----------|----------------|----|-----|---|-----------|------------------|
| MP701 | 03586-61677 | 4 | 4 | CBL-ASM CXL FSMB/FSMB 265MM BLUE | 28480 | 03586-61677 |
| MP703 | 03577-61621 | 7 | 2 | CBL-ASM CXL FSMB/FSMB 220MM WHITE | 28480 | 03577-61621 |
| MP705 | 03577-61622 | 8 | 1 | CBL-ASM CXL FSMB/FSMB 160MM YELLOW | 28480 | 03577-61622 |
| MP706 | 03577-61641 | 1 | 6 | CBL-ASM CXL FSMB/FSMB 135MM ORANGE | 28480 | 03577-61641 |
| MP712 | 03585-61602 | 4 | 10 | CBL-ASM CXL FSMB/FSMB 76MM RED | 28480 | 03585-61602 |
| MP723 | 03585-61605 | 7 | 2 | CBL-ASM CXL FSMB/FSMB 330MM GREEN | 28480 | 03585-61605 |
| MP725 | 03585-61606 | 8 | 1 | CBL-ASM CXL FSMB/FSMB 406MM BLUE | 28480 | 03585-61606 |
| MP765 | 03588-61602 | 7 | 1 | EXT TRIG CBL-ASMCXLBNC/FHSH 200 MM BLACK | 28480 | 03588-61602 |
| MP766 | 03588-61603 | 8 | 1 | TRIG OUT CBL-ASMCXLBNC/FHSG 200MM WHITE | 28480 | 03588-61603 |
| MP767 | 03588-61604 | 9 | 1 | EXT REF IN CBL-ASMCXLBNC/MSMB 578MM BLUE | 28480 | 03588-61604 |
| MP768 | 03588-61605 | 0 | 1 | REF OUT CBL-ASMCXLBNC/MSMB 478MM GREEN | 28480 | 03588-61605 |
| MP770 | 03588-61660 | 7 | 1 | SOURCE CBL-ASM RGD MBNC/MSMB | 09441 | |
| MP771 | 03588-61670 | 9 | 1 | INPUT CBL-ASM RGD MBNC/MSMB | 09441 | |
| MP773 | 03588-61699 | 2 | 1 | W12 MOTHER BRD PWR CBL-ASM RBN FSKT/FSKT 360MM GY | L1624 | |
| MP817 | 35660-61611 | 4 | 1 | W11 FAST BUS CABLE-ASM RBN FHDR/FHDR 350MM GY | 76381 | |
| MP836 | 35672-61601 | 6 | 1 | W1 MEMORY CABLE-ASM RBN FHDR/FHDR 40MM GY | 76381 | |
| MP837 | 35672-61602 | 7 | 1 | W2 CPU POWER CABLE-ASM RBN FHDR/FHDR 290MM GY | 76381 | |
| MP838 | 35672-61603 | 8 | 1 | W3 DISPLAY CABLE-ASM RBN FHDR/FHDR 325MM GY | 76381 | |
| MP839 | 35672-61604 | 9 | 1 | W4 DISK DRIVE CABLE-ASM RBN FHDR/FHDR 35MM GY | 76381 | |
| MP840 | 35672-61605 | 0 | 1 | W5 FRONT-PANEL CABLE-ASM RBN FHDR/FHDR 450MM GY | 76381 | |
| MP861 | 03588-61607 | 2 | 1 | CBL-ASM CXL FSMB/FSMB 85MM BLACK | 28480 | 03588-61607 |
| MP862 | 03588-61608 | 3 | 1 | CBL-ASM CXL FSMB/FSMB 270MM GRAY | 28480 | 03588-61608 |
| MP877 | 35672-61617 | 4 | 1 | W7 POWER ON/OFF CABLE-ASM JKT FCRP/FHSG 615MM GY | 28480 | 35672-61607 |
| | 03588-61606 | 1 | 1 | FAN/OVEN POWER CBL-ASMDSCFHSG/STRP 494MM ML | 28480 | 03588-61606 |
| | 03588-61696 | 9 | 1 | POWER PROBE CBL-ASMDSCFCON/CRMP 65MM ML | 28480 | 03588-61696 |
| | 8120-6495 | 3 | 1 | SWITCH/CABLE ASSEMBLY | 28480 | 8120-6495 |

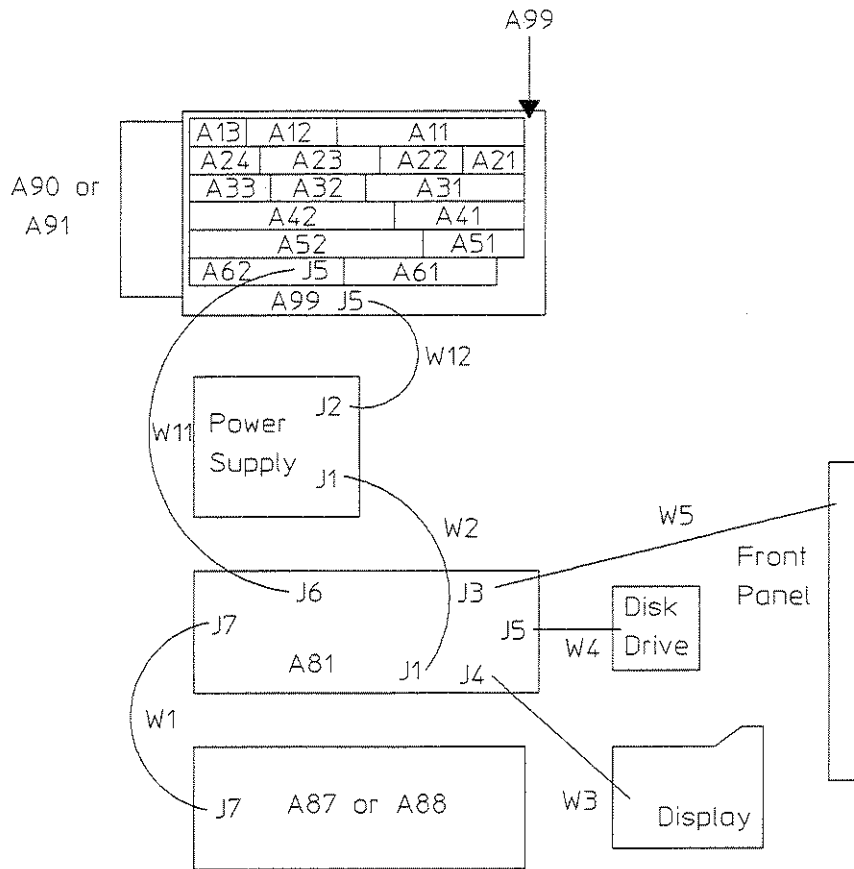


Figure 2-2. Cable Locations

Hardware

To order a part listed in table 2-5, quote the Hewlett-Packard part number, the check digit (CD), indicate the quantity required, and address the order to the nearest Hewlett-Packard sales and service office. The check digit verifies that an order has been transmitted correctly, ensuring accurate and timely processing of the order. The first time a part is listed in the table, the quantity column lists the total quantity of the part used in the analyzer. See table 2-2 for a table listing the manufacturers' code numbers and the corresponding names and addresses. For hardware reference designator numbers, see the disassembly/assembly illustrations following this table.

Table 2-5. Hardware

| Ref.Des. | HP Part Number | CD | Qty | Description | Mfr. Code | Mfr. Part Number |
|----------|----------------|----|-----|--|-----------|----------------------|
| MP700 | 0340-0881 | 7 | 1 | GROMMET-SNAP BUSHING SHORTY | 03480 | 2850 BLK (B-875-750) |
| MP729 | 03588-00219 | 4 | 1 | SHTF BRKT-FOOT AL | 28480 | 03588-00219 |
| MP730 | 03588-01204 | 9 | 1 | STMP BE/CU GROUND BRKT | 28480 | 03588-01204 |
| MP731 | 03588-01206 | 1 | 2 | SHTF BRKT-CONN AL | 28480 | 03588-01206 |
| MP733 | 03588-04101 | 1 | 1 | SHTF HOUSING-INPUT | 28480 | 03588-04101 |
| MP751 | 03588-21703 | 5 | 2 | BSHG-BRASS 5MM ID 3.2MM THK | 05791 | |
| MP753 | 03588-23201 | 2 | 2 | MCHD CONNECTOR GUIDE | 28480 | 03588-23201 |
| MP763 | 03588-60101 | 9 | 1 | CARD SUPPORT ASSY | 28480 | 03588-60101 |
| MP764 | 03588-60201 | 0 | 1 | SHTF ASSY-RR PNL/FAN HSNG ALSK | 28480 | 03588-60201 |
| MP806 | 1400-0611 | 0 | 2 | CLAMP-FL-CA 1-WD | 76381 | 3484-1000 |
| MP809 | 1400-1122 | 0 | 2 | CLAMP-CABLE .187-DIA .735-WD NYL | 34785 | 021-0188 |
| MP810 | 1460-1345 | 5 | 2 | TILT STAND SST | 05502 | |
| MP812 | 1520-0247 | 2 | 1 | MOLD FAN MOUNT | 05030 | FM-450-1 |
| | | 8 | 1 | | | |
| MP818 | 35672-00211 | 6 | 1 | SHTF PNL-REAR ALSK | 28480 | 35672-00211 |
| MP819 | 35672-01202 | 7 | 2 | MCHD SS STRAP SS-HANDLE | 28480 | 35672-01202 |
| MP821 | 35672-01211 | 8 | 1 | SHTF BRKT-DISK DRIVE AL | 28480 | 35672-01211 |
| MP822 | 35672-04111 | 3 | 1 | SHTF COVER AL | 28480 | 35672-04111 |
| MP823 | 35672-21703 | 5 | 4 | MCHD RETAINER SS-HANDLE | 28480 | 35672-21703 |
| MP828 | 35672-41201 | 0 | 2 | MOLD VINYL EXTRUSION-HANDLE | 12136 | 35672-41201 |
| MP831 | 35672-45004 | 9 | 4 | MOLD ENDCAP-HANDLE | 28480 | 35672-45004 |
| MP835 | 35672-60111 | 1 | 1 | SHTF ASSY-CHASSIS AL | 28480 | 35672-60111 |
| MP843 | 5041-8801 | 8 | 2 | MOLD FOOT II + | 28480 | 5041-8801 |
| MP845 | 5041-8822 | 3 | 2 | MOLD FOOT-NON SKID II + | 28480 | 5041-8822 |
| MP848 | 8160-0634 | 4 | 2 | STMP BE/CU GROUND STRIP | 30817 | 0097-0611-17 |
| MP850 | 8160-0636 | 6 | 3 | STMP GROUND STRIP BE/CU .156H | 30817 | 0786-0162-00 |
| MP852 | 1250-2275 | 7 | 2 | BNC FEED THRU SERIES RESISTOR | 01075 | 4391-25 |
| MP854 | 03588-01210 | 7 | 2 | SHTF BRKT-CSS TO WALL AL | 01642 | |
| MP854 | 0380-1630 | 0 | 2 | SPACER-PRESS-IN 10.00 MM LG; 3.6 MM ID | 46384 | KFSE-3.6-10 |
| MP857 | 03588-34311 | 4 | 1 | OVRL ASSY-DRS PLT PLCR Δ | 22670 | |

Δ See section 3, "Manual Backdating."

Table 2-5. Hardware (continued)

| Ref.Des. | HP Part Number | CD | Qty | Description | Mfr. Code | Mfr. Part Number |
|----------|----------------|----|-----|--|-----------|------------------|
| MP863 | 0400-0002 | 2 | 1 | GROMMET-RND .188-IN-ID .312-IN-GRV-OD | 73734 | 1656 |
| MP864 | 0400-0009 | 9 | 2 | GROMMET-RND .125-IN-ID .25-IN-GRV-OD | 01808 | G250 |
| MP873 | 5060-0467 | 6 | 1 | CON-LF PROBE POWER 3PIN | 28480 | 5060-0467 |
| MP874 | 1400-1356 | 2 | 2 | CLP-CABLE .469-.562DIA NYLON | 06915 | |
| MP879 | 8160-0329 | 4 | 1 | RFI STRIP MNL/NPRN .375-IN-WD .25-IN-THK | 09655 | 01-0401-0888 |
| MP880 | 8160-0636 | 6 | | STMP GROUND STRIP BE/CU .156H | 30817 | 0786-0162-00 |
| MP882 | 8160-0683 | 3 | 3 | SPRING FILTER GROUNDING STRIP | 30817 | 0097-551-17-X |
| | 03588-00604 | 1 | 4 | SHTF SHIELD-WALL BTM AL | 01642 | |
| | 03588-00605 | 2 | 4 | SHTF SHIELD-WALL TOP AL | 01642 | |
| | 03588-40607 | 8 | 3 | CSTG-FILTER CANTOP | 28480 | 03588-40607 |
| | 03588-40608 | 9 | 3 | CSTG-FILTER CANBTM | 28480 | 03588-40608 |
| | 35660-40601 | 8 | 2 | CSTG SHIELD CAN (TOP) AL | 01440 | |
| | 35660-40602 | 9 | 2 | CSTG SHIELD CAN (BOTTOM) AL | OBV87 | 35660-40602 |
| | 0380-0003 | 9 | 1 | SPCR-RD .18ID.25D .12LG BRNSI | 28480 | 0380-0003 |
| | 6960-0041 | 1 | 1 | PLUG-HOLE FL-HD FOR .5-D-HOLE NYL | 03480 | 2643 (BLACK) |
| | 03588-40605 | 6 | 1 | CSTG-RF SHIELDTOP | 28480 | 03588-40605 |
| | 03588-40606 | 7 | 1 | CSTG-RF SHIELDBTM | 28480 | 03588-40606 |
| | 03588-04111 | 3 | 1 | A11 SHTF ASSY-COVER TOP ALSK | 28480 | 03588-04111 |
| | 03588-04112 | 4 | 1 | A12 SHTF ASSY-COVER TOP | 28480 | 03588-04112 |
| | 03588-04113 | 5 | 1 | A13 SHTF ASSY-COVER TOP | 28480 | 03588-04113 |
| | 03588-04121 | 5 | 1 | A21 SHTF ASSY-COVER TOP | 28480 | 03588-04121 |
| | 03588-04122 | 6 | 1 | A22 SHTF ASSY-COVER TOP | 28480 | 03588-04122 |
| | 03588-04123 | 7 | 1 | A23 SHTF ASSY-COVER TOP | 28480 | 03588-04123 |
| | 03588-04124 | 8 | 1 | A24 SHTF ASSY-COVER TOP | 28480 | 03588-04124 |
| | 03588-04131 | 7 | 1 | A31 SHTF ASSY-COVER TOP ALSK | 28480 | 03588-04131 |
| | 03588-04132 | 8 | 1 | A32 SHTF ASSY-COVER TOP ALSK | 28480 | 03588-04132 |
| | 03588-04133 | 9 | 1 | A33 SHTF ASSY-COVER TOP ALSK | 28480 | 03588-04133 |
| | 03588-04141 | 9 | 1 | A41 SHTF ASSY-COVER TOP ALSK | 28480 | 03588-04141 |
| | 03588-04142 | 0 | 1 | A42 SHTF ASSY-COVER TOP ALSK | 28480 | 03588-04142 |
| | 03588-04151 | 1 | 1 | A51 SHTF ASSY-COVER TOP ALSK | 28480 | 03588-04151 |
| | 03588-04152 | 2 | 1 | A52 SHTF ASSY-COVER TOP ALSK | 28480 | 03588-04152 |
| | 03588-04161 | 3 | 1 | A61 SHTF ASSY-COVER TOP ALSK | 28480 | 03588-04161 |
| | 03588-04162 | 4 | 1 | A62 SHTF ASSY-COVER TOP ALSK | 28480 | 03588-04162 |
| | 03588-05002 | 3 | 11 | A11 HANDLE-BAIL | 05502 | |
| | 03588-05002 | 3 | | A12 HANDLE-BAIL | 05502 | |
| | 03588-05001 | 2 | 4 | A13 HANDLE-BAIL | 05502 | |
| | 03588-05001 | 2 | | A21 HANDLE-BAIL | 05502 | |
| | 03588-05001 | 2 | | A22 HANDLE-BAIL | 05502 | |
| | 03588-05002 | 3 | | A23 HANDLE-BAIL | 05502 | |
| | 03588-05001 | 2 | | A24 HANDLE-BAIL | 05502 | |

Table 2-5. Hardware (continued)

| Ref.Des. | HP Part Number | CD | Qty | Description | Mfr. Code | Mfr. Part Number |
|----------|----------------|----|-----|---------------------------------------|-----------|------------------|
| | 03588-05002 | 3 | | A31 HANDLE-BAIL | 05502 | |
| | 03588-05002 | 3 | | A32 HANDLE-BAIL | 05502 | |
| | 03588-05002 | 3 | | A33 HANDLE-BAIL | 05502 | |
| | 03588-05002 | 3 | | A41 HANDLE-BAIL | 05502 | |
| | 03588-05002 | 3 | | A42 HANDLE-BAIL | 05502 | |
| | 03588-05002 | 3 | | A51 HANDLE-BAIL | 05502 | |
| | 03588-05002 | 3 | | A52 HANDLE-BAIL | 05502 | |
| | 03588-05002 | 3 | | A61 HANDLE-BAIL | 05502 | |
| | 03588-05003 | 4 | 1 | A62 HANDLE-BAIL | 05502 | |
| | 1420-0336 | 8 | 1 | BATTERY | 08891 | T06/46 |
| | 5061-2819 | 8 | 1 | BLANK PLASTIC DISK FOR TRANSPORTATION | | |
| | 2110-0056 | 3 | 1 | 6A 250V FAST ACTING FUSE | 75915 | 312 006 |
| | 2110-0003 | 0 | 1 | 3A 250V FAST ACTING FUSE | 75915 | 312 003 |
| | 35672-05011 | 4 | 3 | FRONT PANEL MOUNTING CLIP | 28480 | 35672-05011 |
| | 03588-47401 | 4 | 1 | MOLD KNOB-RPG II+ | 28480 | 03588-47401 |
| | 0570-1378 | 6 | 14 | SCREEN SCREWS | 83486 | 276-000-0000-7N |
| | 35672-49301 | 7 | 1 | LNZ-CURVED RFI WINDOW | 09655 | |
| | 03588-04103 | 3 | 1 | SHTF CVR-OVEN TWEAK ALSK | 28480 | 3588-04103 |
| | 7204-0009 | 0 | 1 | SHT-AL 1.0MM/.040TK AA5052- | 28480 | 7204-0009 |
| | 0515-1954 | 8 | 11 | SCR-MCH M4.0 20MMLG PHPZ SSTWX | 01125 | 13149-437 |
| | 7204-0003 | 4 | | SHT-AL 1.6MM/.063TK AA5052- | 28480 | 7204-0003 |
| | 0590-1368 | 6 | 2 | PEM PRESS-IN NUT | 46384 | CLS-M3-2 |
| | 1250-2062 | 1 | 1 | OVEN BNC CONNECTOR | 03316 | 28JR175-9 |
| | 1250-1499 | 5 | 1 | COAX BNC(M) TO COAX BNC(M) | 03316 | 28AU100-1 |
| | 0515-0456 | 3 | 3 | TOP COVER SCREWS M4X16MMLG | 28480 | 0515-0456 |
| | 8160-0683 | 3 | 2 | SPRING GROUND CLIP | 28480 | 8160-0683 |
| | 03588-80401 | 4 | 1 | LABEL-CABLING (OVER CRT) | 28480 | 03588-80401 |
| | 1252-0268 | 8 | 1 | HP-IB CONNECTOR | 28480 | 1252-0268 |
| | 1000-0888 | 5 | 1 | RPG | 28480 | 1000-0888 |
| | 0590-1196 | 8 | 1 | PEM CENTER/REAR FRAME P/O 35672-66501 | 28480 | 0590-1196 |

Disassembly/Assembly

Use the following illustrations to disassemble and assemble the HP 3588A Spectrum Analyzer.

Warning



Disconnect the power cord from the rear panel before disassembly or assembly of the HP 3588A Spectrum Analyzer.

Caution



Do not connect or disconnect ribbon cables from circuit assemblies with the line power turned ON (I).
To protect circuits from static discharge, remove or replace HP 3588A Spectrum Analyzer assemblies only at static-protected work stations.

Warning



When replacing the handle assemblies, be careful to position properly and attach firmly. If improperly attached, the handles could come off when lifting the analyzer, causing personal injury.

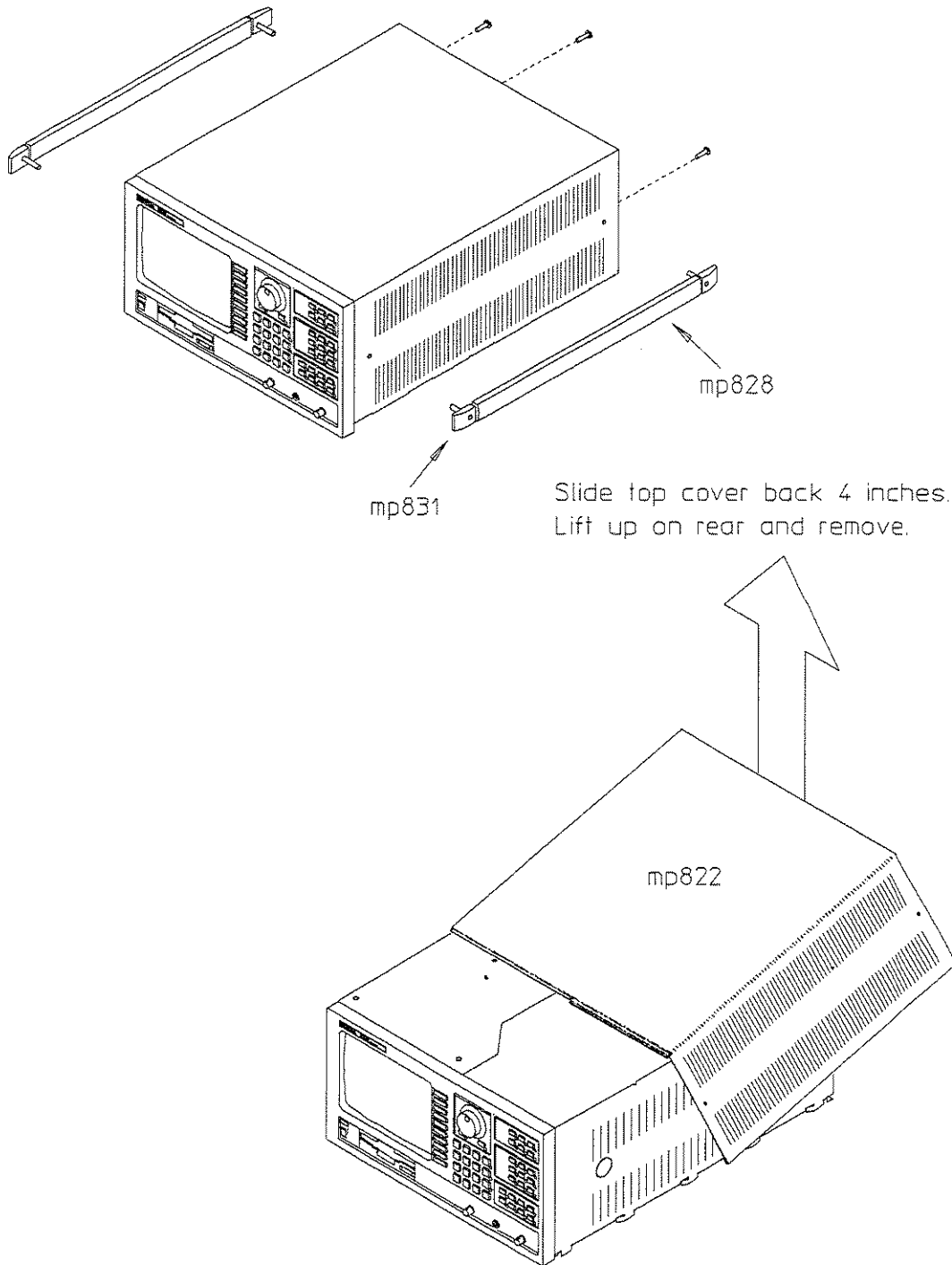


Figure 2-3. Top Cover

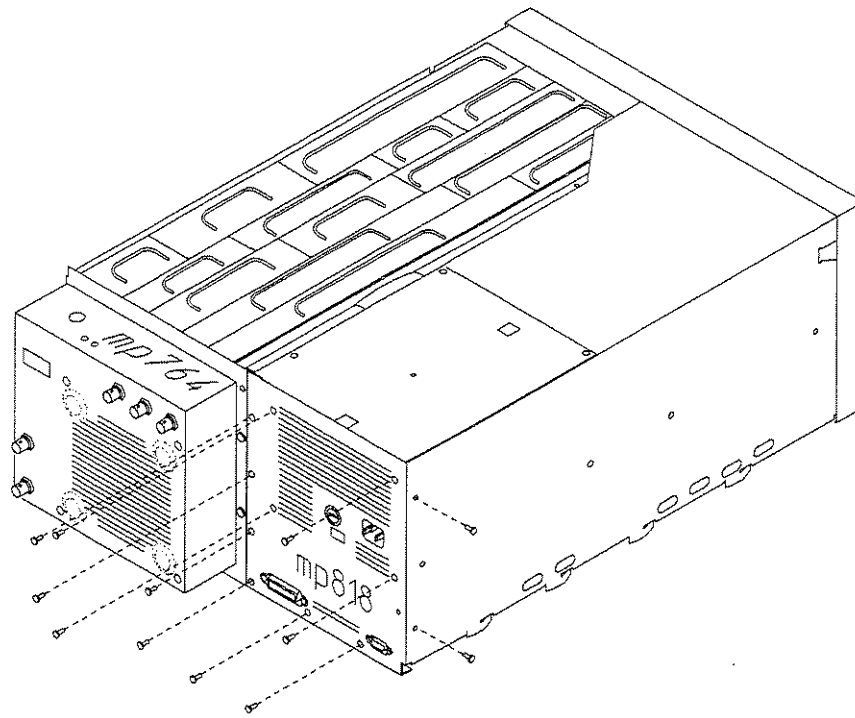


Figure 2-4. Rear Panel

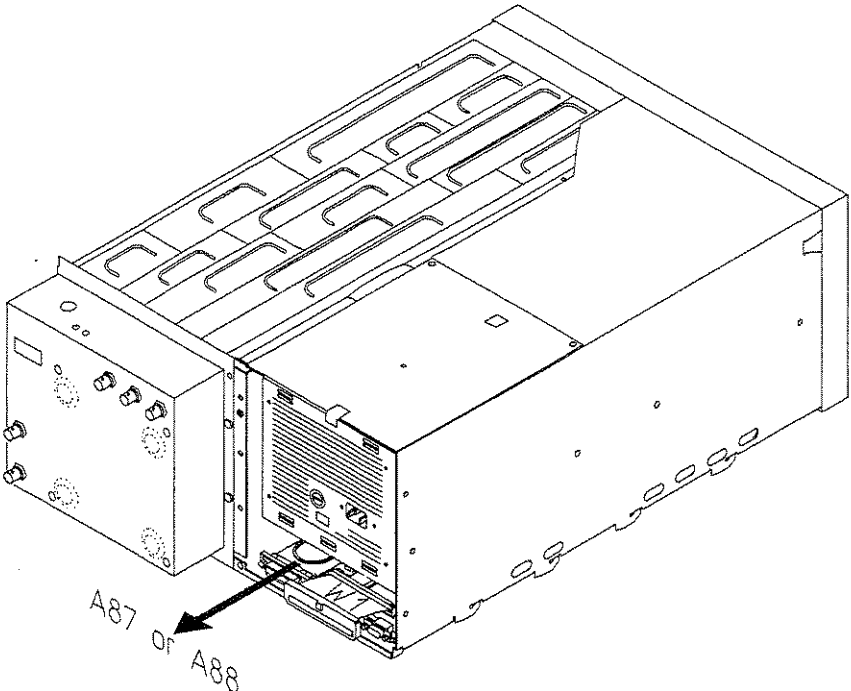


Figure 2-5. Memory

Caution

Do NOT remove the 3 screws that are marked with an X on the illustration. The Power Supply assembly will be damaged if the center screw is removed.
Do NOT remove the earth ground (green/yellow wire) from the Power Supply assembly or the analyzer's chassis.

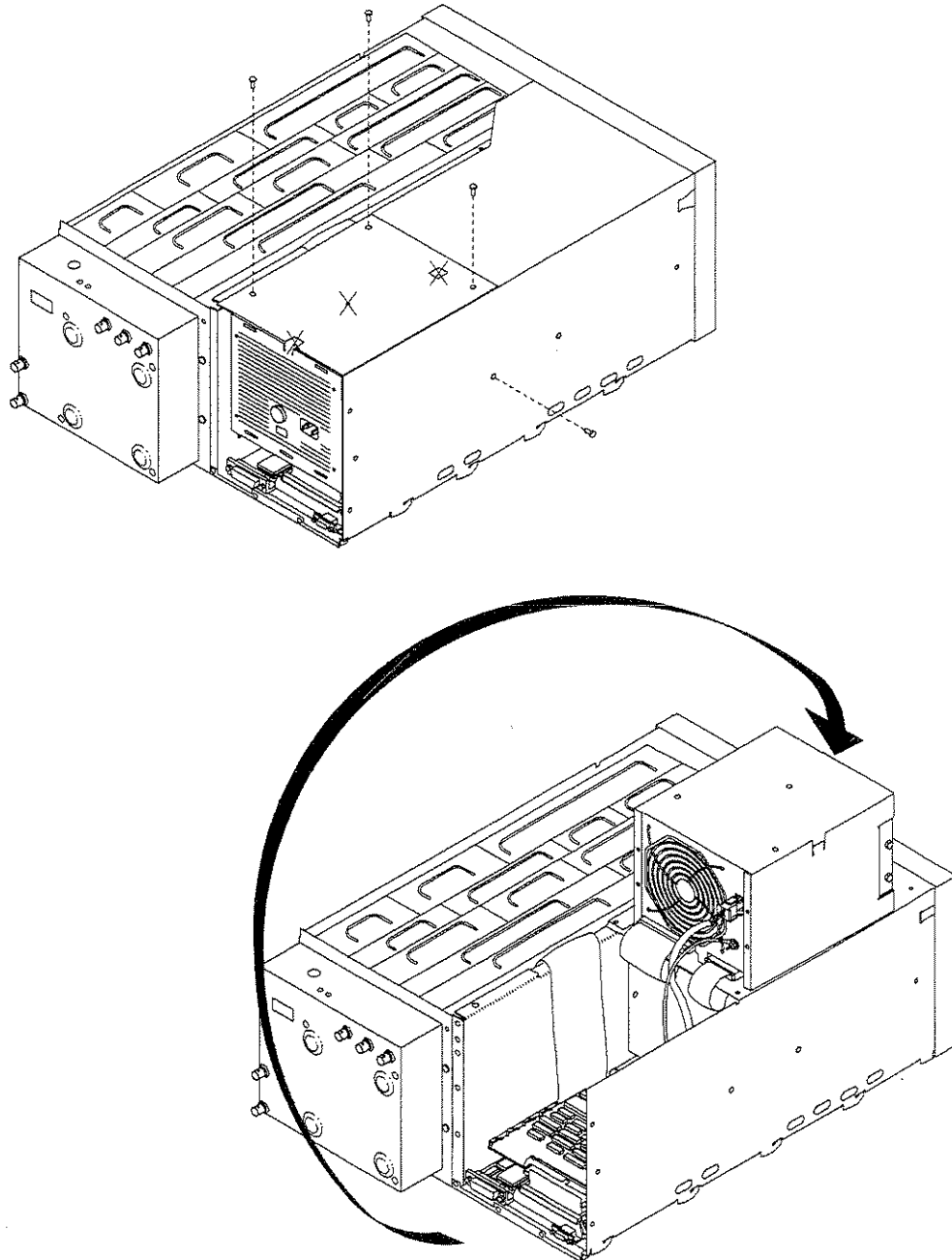


Figure 2-6. Power Supply

Note



Follow these steps when replacing the Front Panel assembly:
Connect the power cable and front-panel cable to the Front Panel assembly.
With the top of the Front Panel assembly tilted away from the analyzer, align the 3 plastic flanges (on the bottom of the Front Panel assembly) with the slots in the chassis.
Align the BNC dress plate with the BNC connectors.
Align the disk drive slot on the Front Panel assembly with the disk drive bezel.
Push the top of the Front Panel assembly back, snapping the 3 clips into place.

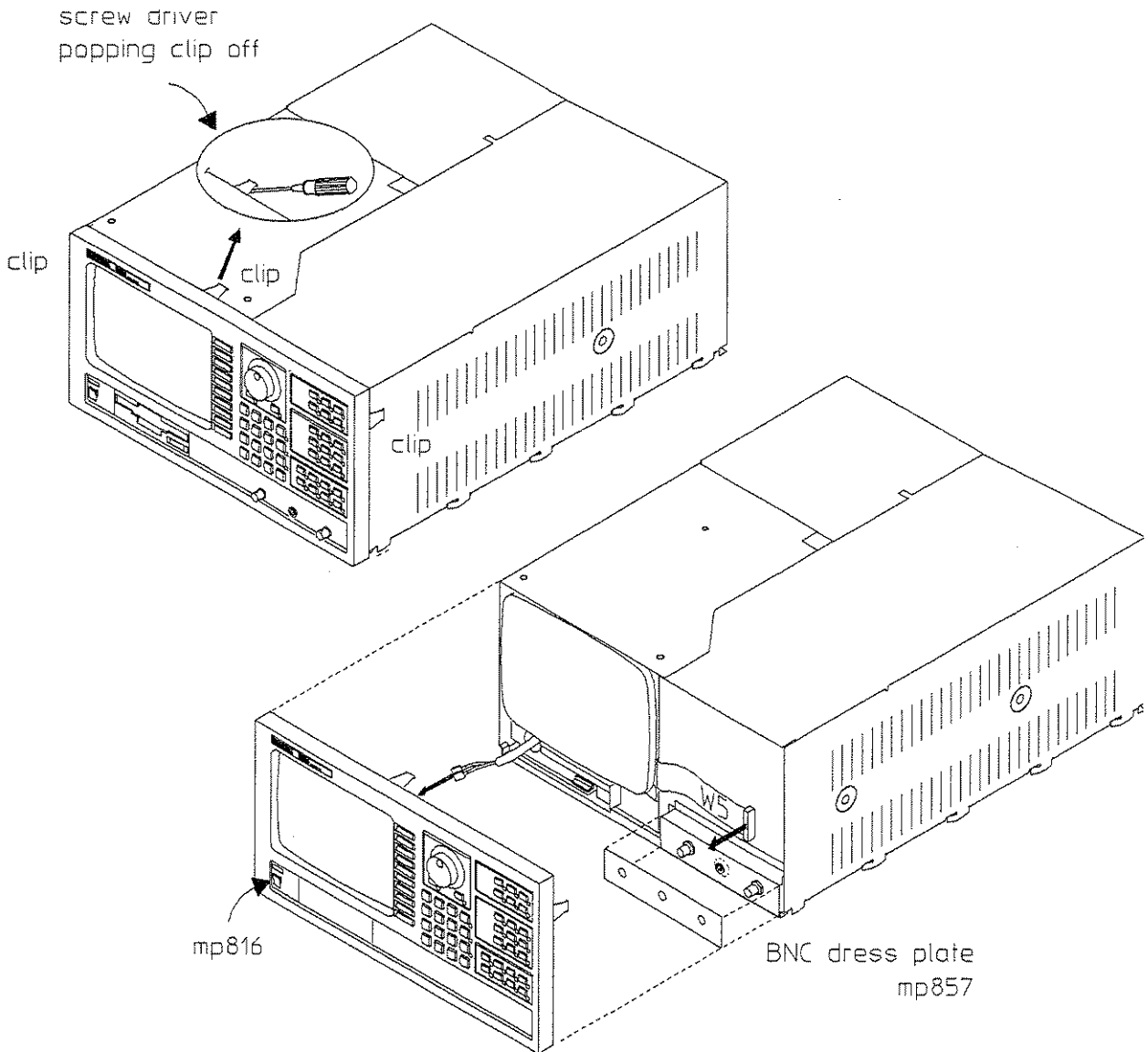


Figure 2-7. Front Panel

Note



When reinstalling the CPU assembly, connect the display cable before placing the CPU assembly in position.

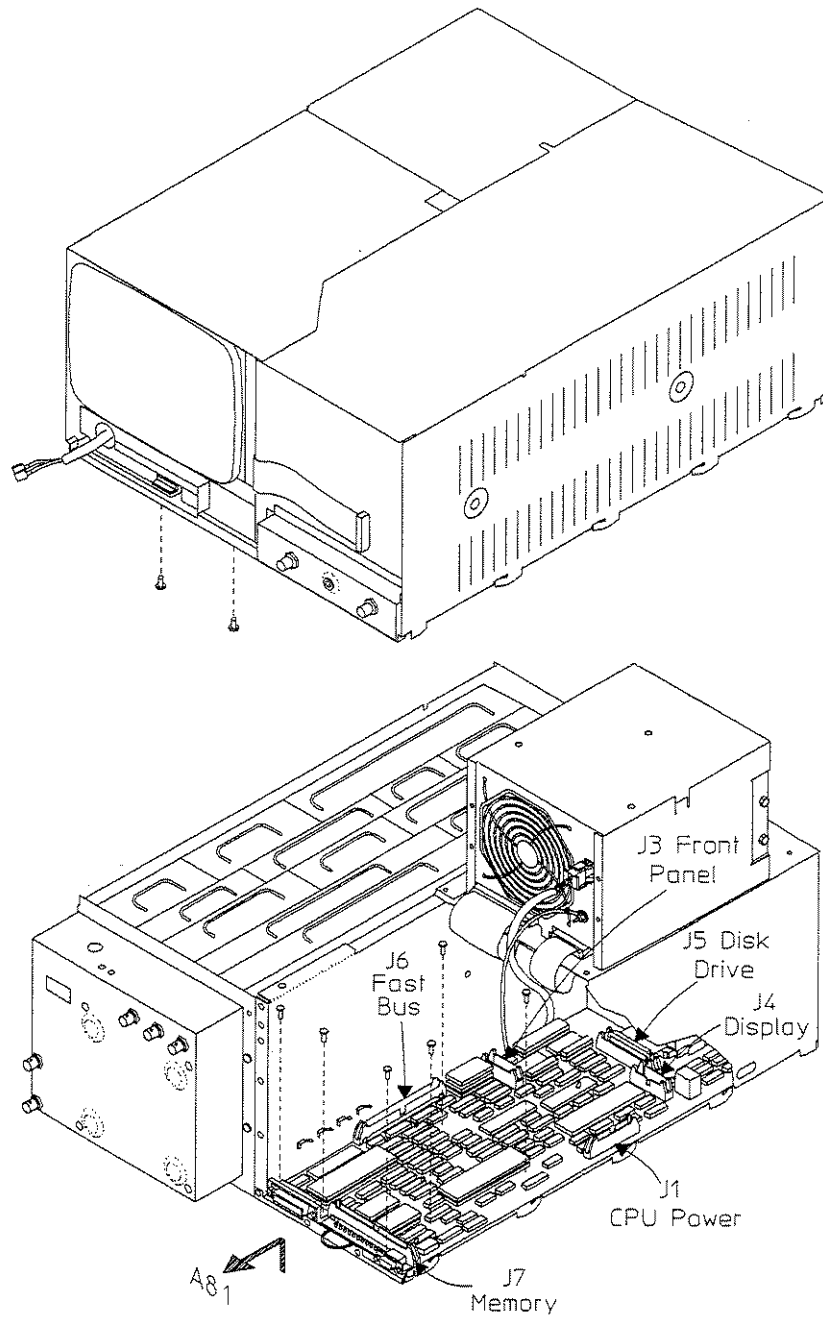


Figure 2-8. CPU

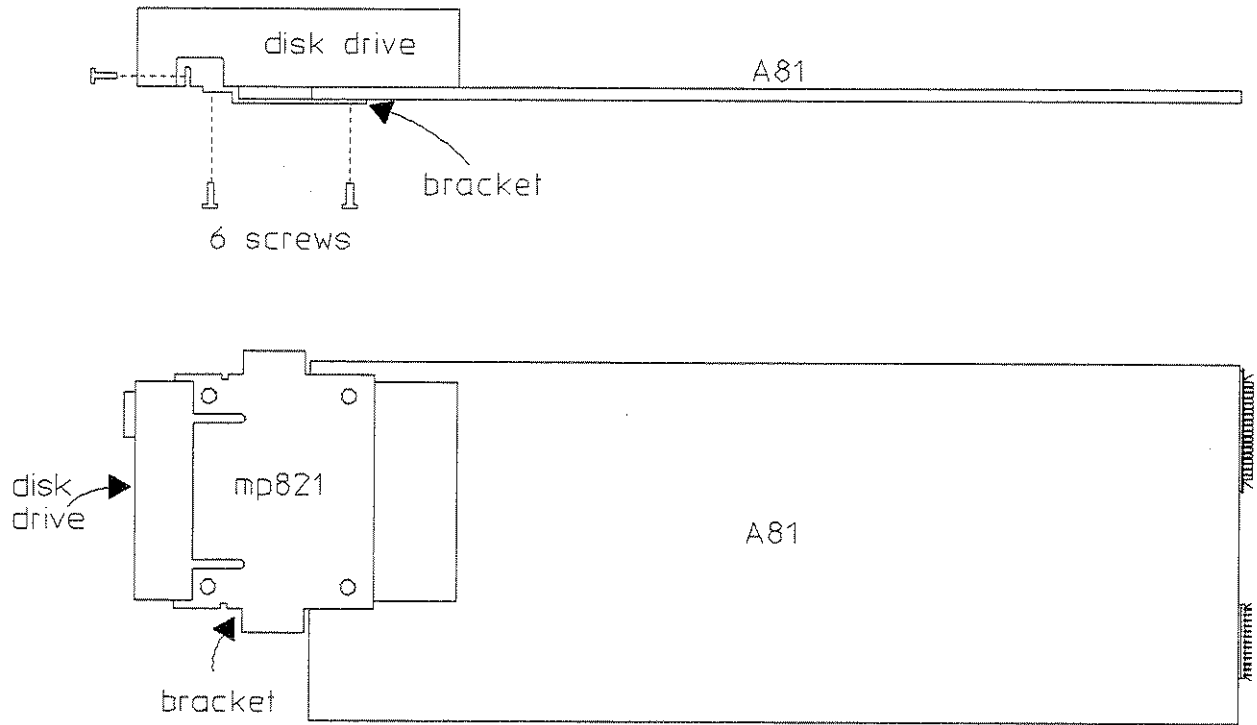


Figure 2-9. Disk Drive

Caution



When replacing the Display assembly, be careful to keep the front-panel cable flat against the inside center wall.

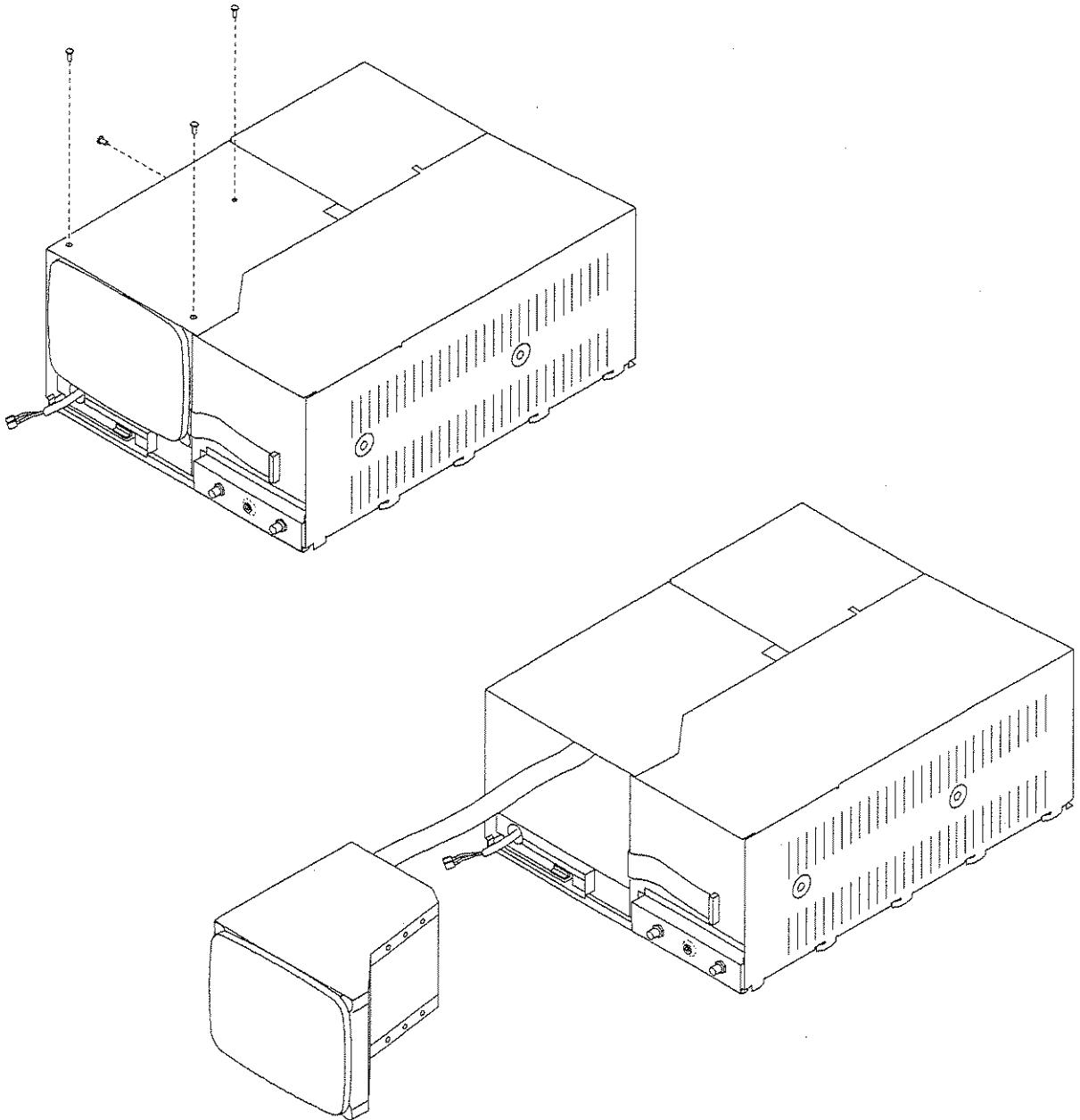


Figure 2-10. Display

Caution



Before positioning the fan/oven housing against the chassis, connect the cable from the motherboard to the assembly, and carefully route the cable from the motherboard around the fan and the RF cables through the slots in the chassis.

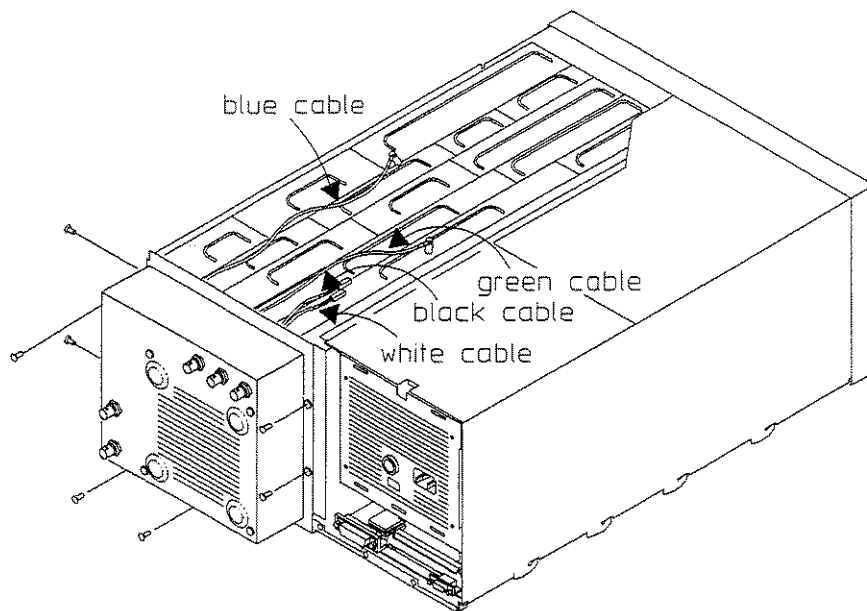


Figure 2-11. Fan/Oven Housing

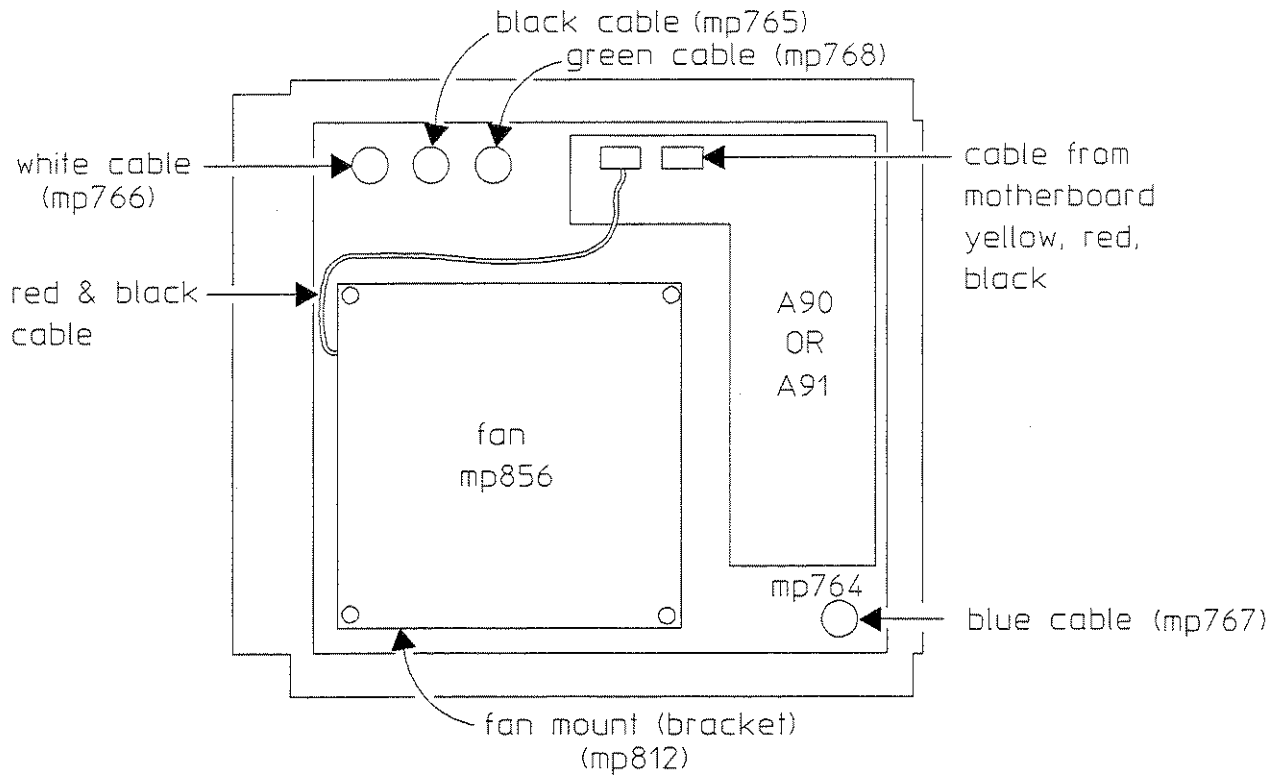


Figure 2-12. Fan/Oven

Note

Connect motherboard power cable before placing card nest in chassis.

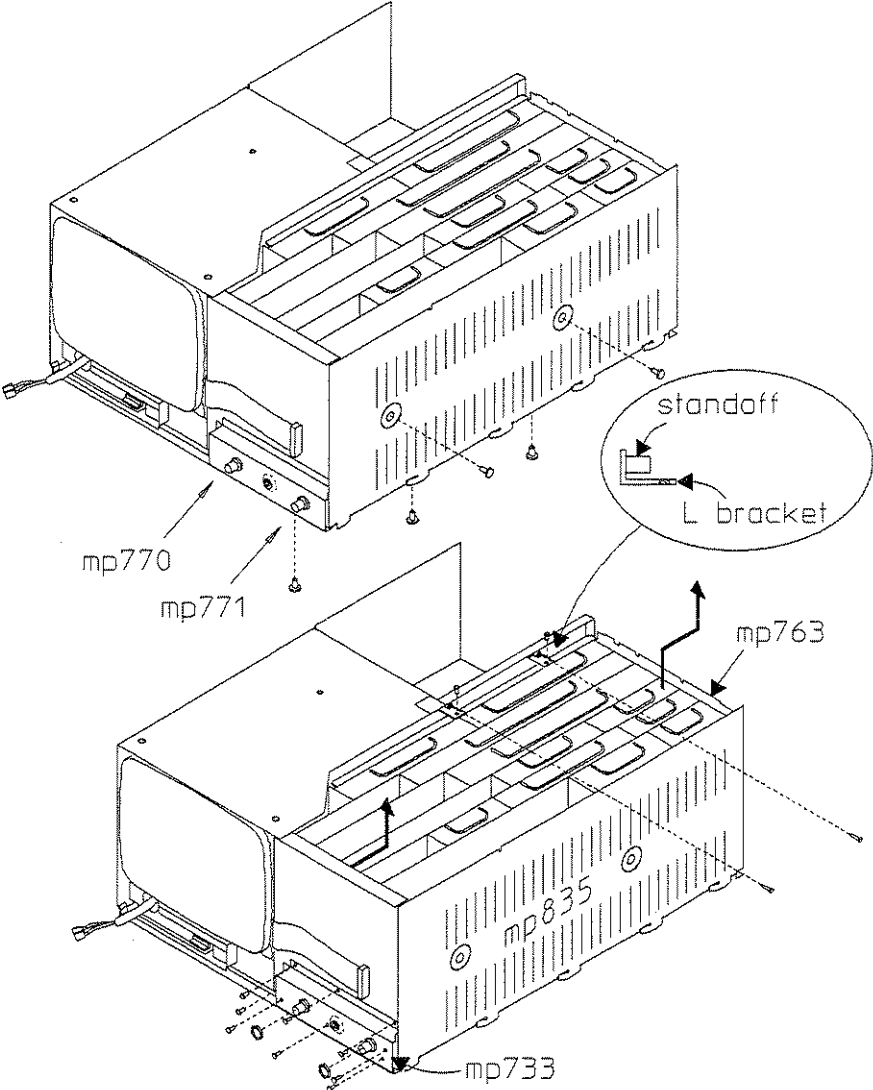


Figure 2-13. Card Nest

Manual Backdating

Introduction

This section provides information necessary to modify this manual for instruments that differ from those currently being produced. The information in this section documents earlier instrument configurations and associated servicing procedures.

With the information provided in this section, this manual can be corrected so that it applies to any earlier version or configuration of the instrument. To adapt this manual to your instrument, see table 3-1 and make all the changes listed opposite your instrument serial number. Later versions of the instrument are documented in the Manual Changes Supplement.

Manual Changes Supplement

As Hewlett-Packard continues to improve the performance of the HP 3588A, corrections and modifications to the manual may be required. Required changes are documented by a yellow Manual Changes supplement and/or revised pages. To keep the manual up-to-date, periodically request the most recent supplement, available from the nearest Hewlett-Packard sales and service office (for office locations, see the listing at the back of this manual).

Manual Changes Instructions

Table 3-1. Manual Changes

| Instrument Serial Number | Make Manual Changes |
|--------------------------|---------------------|
| 3005A00100 to 3005A00647 | A |

Change A

Page 2-6, Table 2-3. Assemblies:

Change the HP part number for MP859 to 03588-60204.

Page 2-10, Table 2-5. Hardware:

Change the part number for MP857 to 03588-34301 and add MP834, Mold Disk Eject Button, HP part number 35672-47401.

Circuit Descriptions

Introduction

This section contains the overall instrument description and individual assembly descriptions for the HP 3588A Spectrum Analyzer. The overall instrument description lists the assemblies in the HP 3588A and describes the instrument's overall block diagram. The assembly descriptions give additional information for each assembly. This section also contains the following:

- Voltage and signal distribution tables
- Signal descriptions
- Calibration routine descriptions
- Power-on and preset states

Overall Instrument Description

The HP 3588A Spectrum Analyzer is a high performance, 10 Hz to 150 MHz, synthesized spectrum analyzer offering swept spectrum and narrow-band zoom measurements. Swept spectrum mode uses digital IF filters that allow increased measurement speed (up to four times faster than conventional swept-tuned analyzers for comparable measurements) with no additional amplitude error or resolution loss. Narrow-band zoom uses an implementation of the Fast Fourier Transform to provide even faster measurements (up to 350 times faster than conventional swept-tuned analyzers for comparable measurements) with even greater resolving power. Narrow-band zoom mode can be used for spans of 40 kHz and less.

The HP 3588A Spectrum Analyzer also has a built-in source with programmable amplitude that allows scalar network measurements. Measurements can be saved using the optional internal 3.5-inch flexible disk drive or the internal non-volatile memory. Plots and prints of the measurements can be made directly to HP-IB printers and plotters. The HP 3588A Spectrum Analyzer also supports the HP Instrument BASIC programming language (IBASIC).

Overall Block Diagram

Figure 4-1 shows the overall block diagram for the analyzer. Each block in the diagram represents a functional block in the instrument. The assembly (or assemblies) that performs the function is listed in the block.

The **Input/Conversion** and **IF/ADC** together function as the analyzer's receiver. Input/Conversion prepares the input signal for analog-to-digital conversion. Figure 4-2 shows the signal flow to and from each assembly in the Input/Conversion block. The IF further prepares the input signal and then the ADC converts the signal from analog to digital. Figure 4-3 shows the signal flow to and from each assembly in the IF/ADC block.

The **Sum/Step Loop** and **Fractional-N** together function as the analyzer's local oscillator. The Sum/Step Loop provides the Fractional-N, Input/Conversion, and Source blocks with a signal that can sweep from 310.1875 to 460.1875 MHz. Figure 4-4 shows the signal flow to and from each assembly in the Sum/Step Loop block. The Fractional-N provides the Sum/Step Loop block with a signal that can sweep from 3 to 11 MHz and the single loop control voltage. Figure 4-5 shows the signal flow to and from each assembly in the Fractional-N block.

The **Frequency Reference** provides both high and low frequency reference signals, a sweep synchronization signal, a trigger signal, and a precision amplitude signal for calibration. Figure 4-6 shows the signal flow to and from each assembly in the Frequency Reference block.

The **Source** provides the tracking source output for the analyzer. Its frequency tracks the tuned receiver frequency, providing an output signal that can sweep from 10 Hz to 150 MHz. Its amplitude can be adjusted from +10 to -59.9 dBm. The Source also provides the normalization signal to the Input/Conversion block and the calibration signal to the Frequency Reference block. Figure 4-7 shows the signal flow to and from each assembly in the Source block.

The optional **Oven** provides a stable 10 MHz frequency reference. A BNC-to-BNC jumper from OVEN REF OUT to EXT REF IN (on the rear panel) connects this signal to the Frequency Reference block.

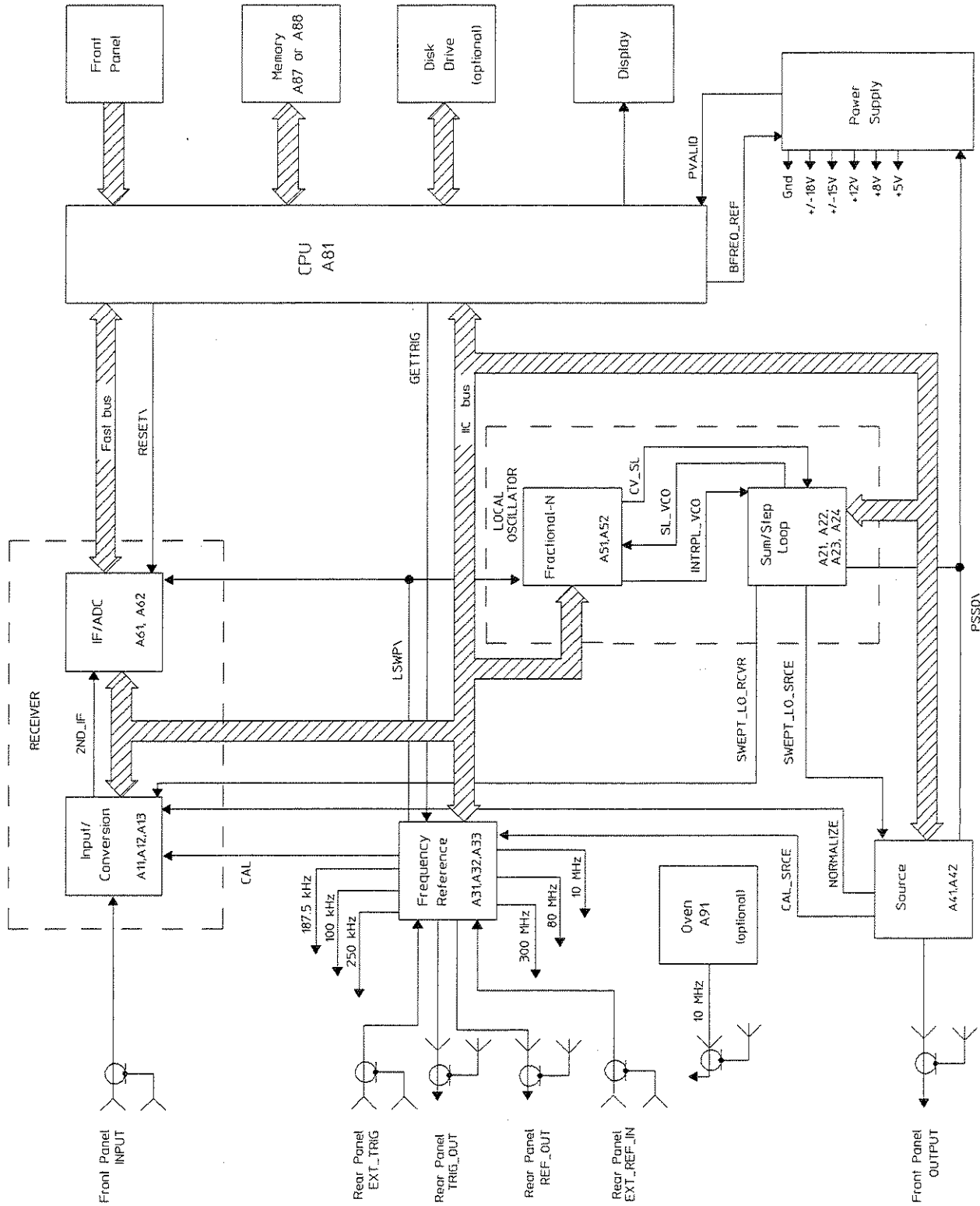


Figure 4-1. Overall Block Diagram

The **CPU** controls the analyzer. The following is a partial list of the operations it performs:

- Configures the assemblies
- Controls the Disk Drive assembly
- Controls the Display assembly
- Controls the HP-IB interface
- Initiates the power-up sequence and calibration routine
- Processes digital data from the ADC/Digital Filter assembly
- Computes the Fast Fourier Transform (FFT)
- Monitors for a front panel keystroke
- Monitors the assemblies for overloads or other error conditions
- Runs the self tests

The optional **Disk Drive** stores and retrieves information on 3.5-inch flexible disks.

The **Memory** contains RAM, NVRAM, and ROM for the CPU. The RAM is dynamic and all refresh circuitry is located with the RAM.

The **Display** offers a view of the processed data. It is controlled by the CPU. See the description of the Display Controller for the "A81 CPU" later in this section for further details.

The **Front Panel** allows interaction with the analyzer. It consists of hardkeys, softkeys, an RPG, an Inter-IC (IIC) interface, and a plastic diffuser-screen for the Display.

The **Power Supply** provides the dc voltages shown in figure 4-1. See "Voltage and Signal Distribution" later in this section for further information.

Assemblies

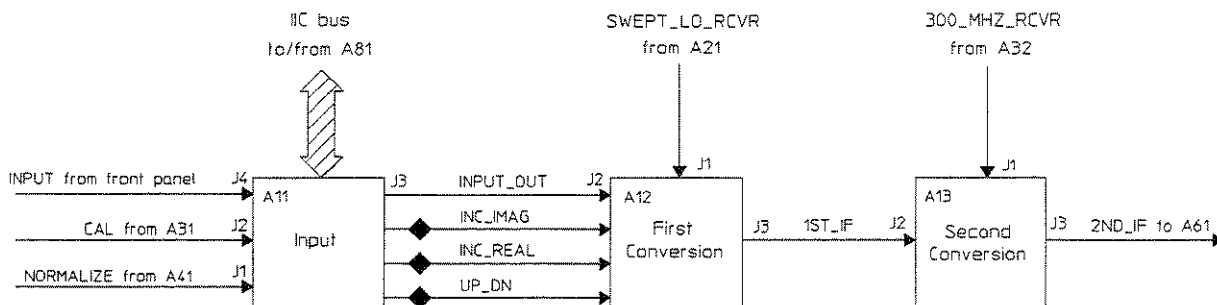
The HP 3588A Spectrum Analyzer consists of the assemblies shown below.

- A11 Input
- A12 First Conversion
- A13 Second Conversion
- A21 Sum VCO
- A22 Sum Phase Detector
- A23 Step Phase Detector
- A24 Step VCO
- A31 Reference/Calibrator
- A32 300 MHz
- A33 Trigger
- A41 Source Amplifier
- A42 Source Conversion
- A51 Interpolation VCO
- A52 Fractional-N
- A61 IF
- A62 ADC/Digital Filter
- A81 CPU
- A87 Memory
- A88 Expanded Memory (optional)
- A90 Fan Power
- A91 Fan Power/Oven (optional)
- A99 Motherboard
- Power Supply
- Disk Drive
- Display
- Front Panel

Note

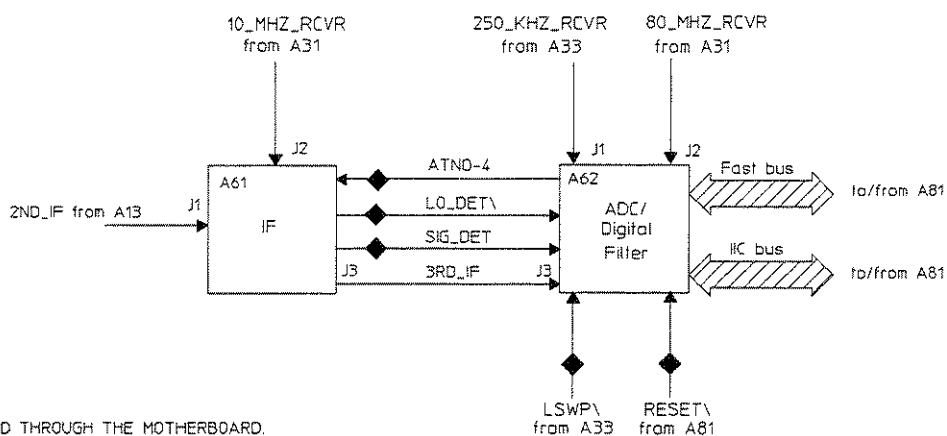


In this section, the block diagrams show the connector numbers for signals routed through RF cables. The block diagrams do *not* show connector numbers for signals routed through the Motherboard assembly.



◆ ROUTED THROUGH THE MOTHERBOARD.

Figure 4-2. Input Conversion Block Diagram



◆ ROUTED THROUGH THE MOTHERBOARD.

Figure 4-3. IF/ADC Block Diagram

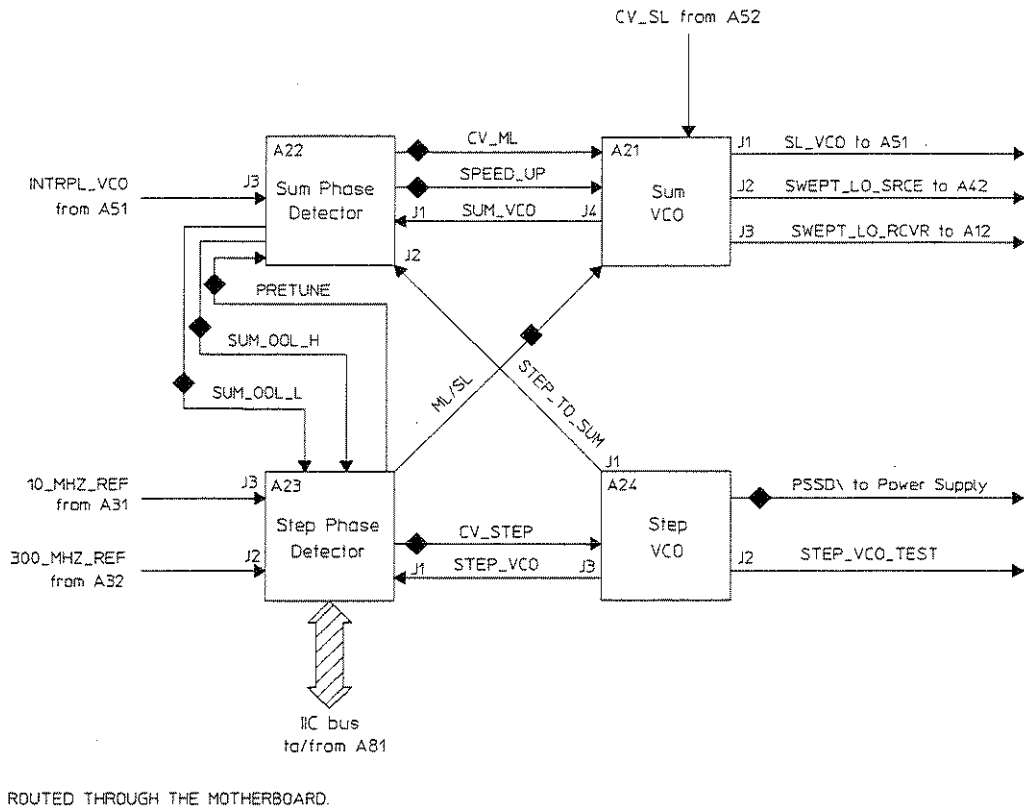


Figure 4-4. Sum and Step Loop Block Diagram

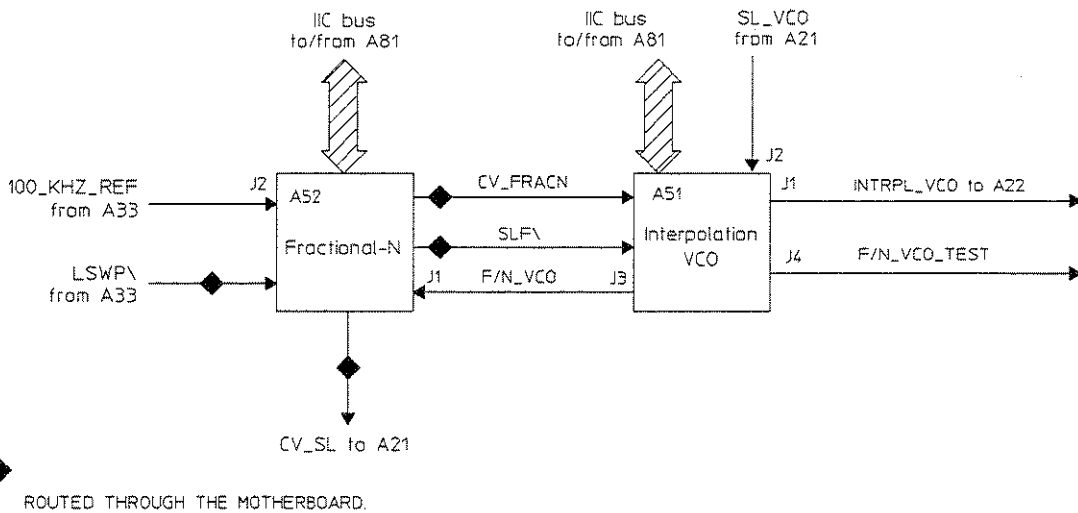


Figure 4-5. Fractional-N Block Diagram

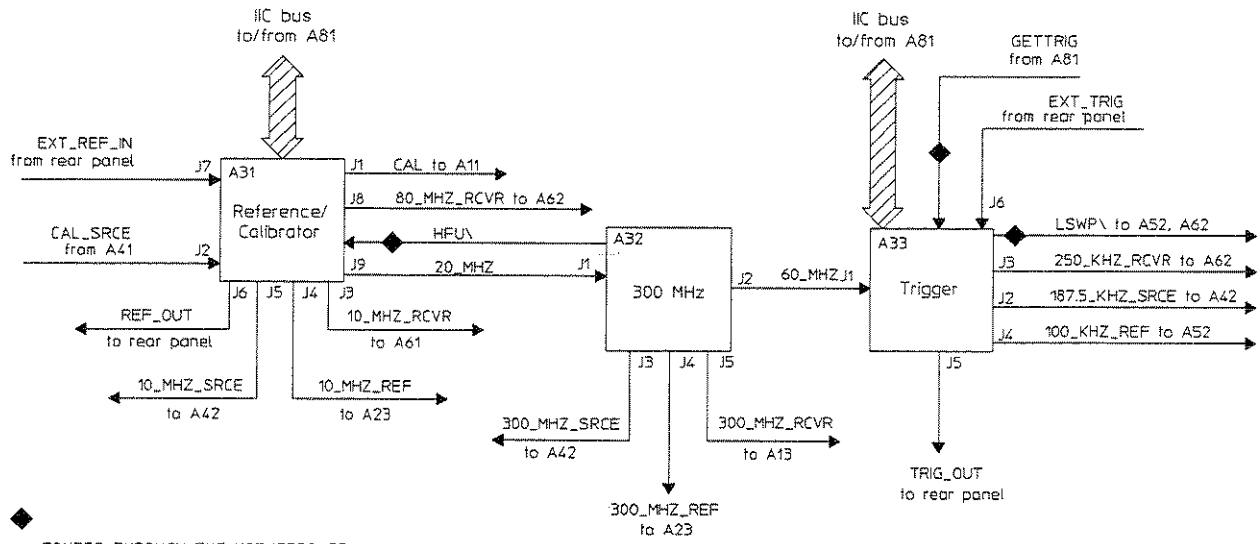


Figure 4-6. Frequency Reference Block Diagram

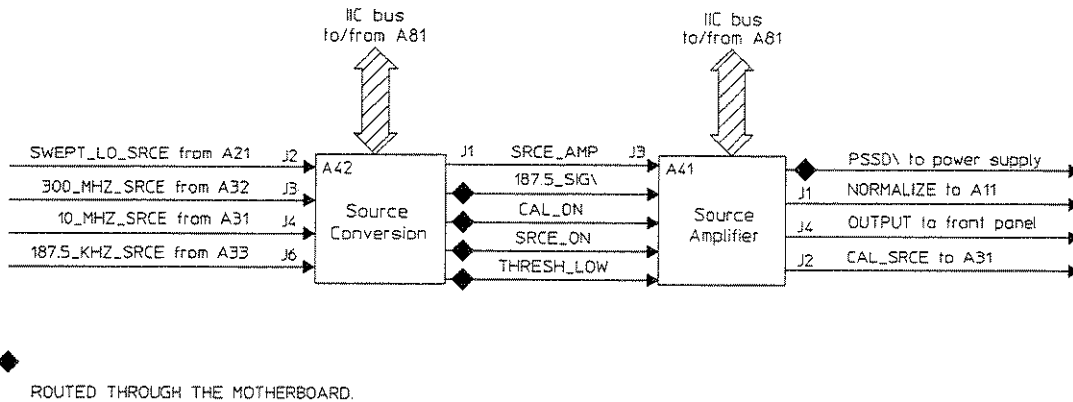


Figure 4-7. Source Block Diagram

A11 Input

The Input assembly is the first of five assemblies that condition the input signal before it is sent to the CPU assembly in digital form. The input signal can be a signal (10 Hz to 150 MHz) that is connected to the front-panel input connector, the normalization signal from the Source Amplifier assembly, or the calibration signal from the Reference/Calibrator assembly. Figure 4-8 shows the Input assembly's block diagram.

The **Input Switching** circuit selects either the signal connected to the front-panel input connector, the calibration signal from the Reference/Calibrator assembly, or the normalization signal from the Source Amplifier assembly. It then routes the selected signal to either the 50 Ω or the 1 M Ω input impedance path.

The **1M Ohm Buffer** provides a 1 M Ω impedance path for the input signal. This circuit conditions the input signal using a 20 dB attenuator pad, a flatness service adjustment, and a 1M Ω input amplifier. Its maximum input level is -13 dBV and its output impedance is 50 Ω .

The **50 Ohm Attenuator** provides a 50 Ω impedance path for the input signal. This circuit attenuates the input signal using one 10 dB and two 20 dB attenuator pads. Its maximum input level is +20 dBm and its output impedance is 50 Ω .

The **Input Amplifier** increases the input signal's amplitude by 5 dB and provides 50 Ω output impedance to both the 150 MHz Low Pass Filter and the Autorange Detector.

The **150 MHz Low Pass Filter** attenuates signals greater than 150 MHz.

The **Autorange Detection** circuit compares the input signal to a service adjustable "range up" and "range down" threshold. The CPU assembly monitors the result of this comparison and then sets the 50 Ω attenuators so the largest signal amplitude is at a level that displays maximum dynamic range.

The **Overload Protection** circuit monitors the 50 Ω impedance path. If an overload occurs, this circuit causes the relays in Input Switching to disconnect the input signal.

The **IIC Interface** provides the interface between the CPU assembly and the Input assembly, and it provides the control lines that null local oscillator feedthrough on the First Conversion assembly. It also interrupts the CPU assembly if a range up, range down, or overload condition is detected.

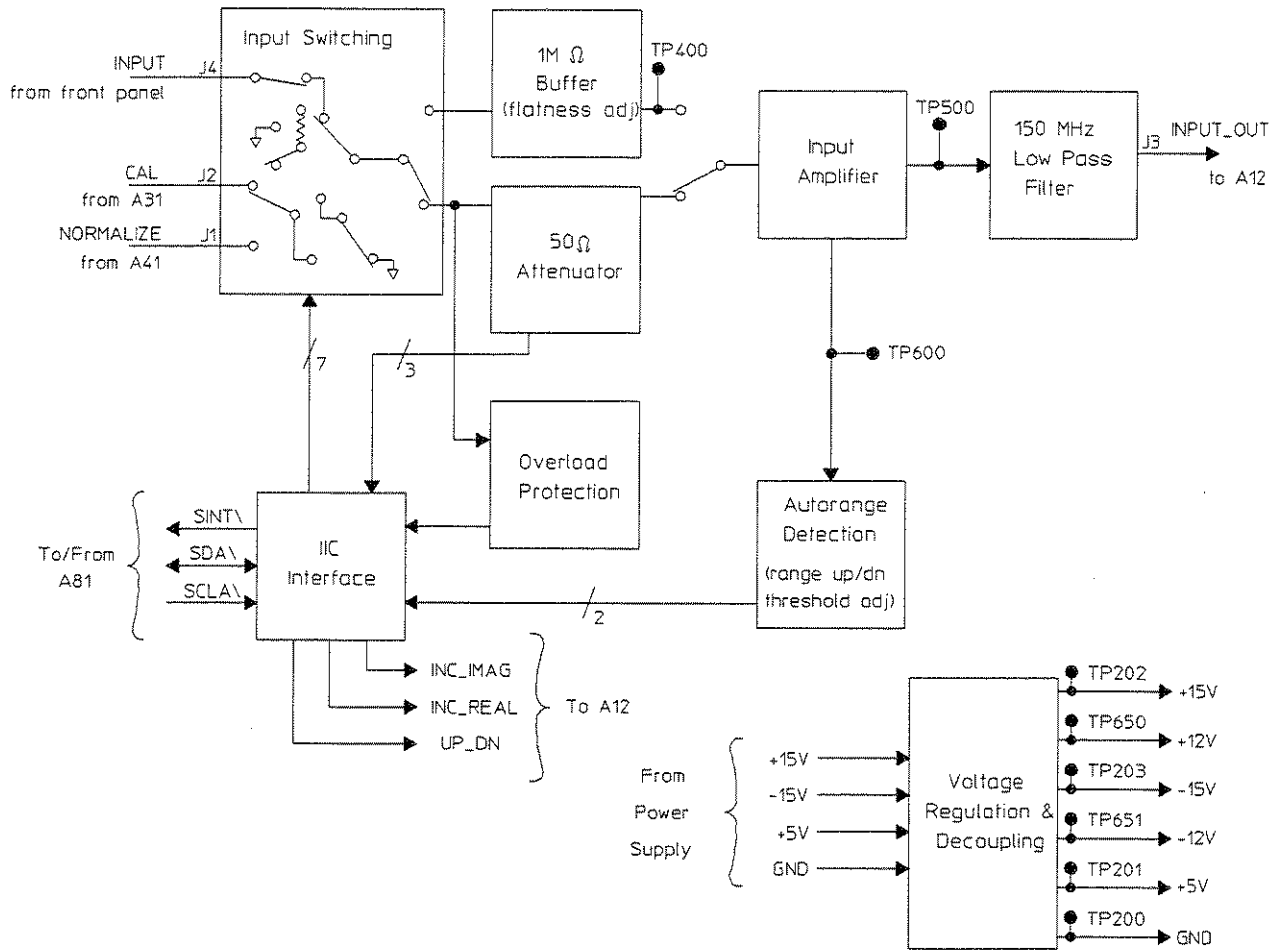


Figure 4-8. A11 Input Block Diagram

A12 First Conversion

The First Conversion assembly is the second of five assemblies that condition the input signal. This assembly mixes the swept LO signal with the signal from the Input assembly. The resulting 310.1875 MHz signal is routed to the Second Conversion assembly. Figure 4-9 shows the First Conversion assembly's block diagram.

The **First Conversion Mixer/Driver** first increases the amplitude of the swept LO signal (310.1875 to 460.1875 MHz) to +17 dBm at the mixer input. It then mixes the swept signal with the input signal. At the output of this circuit, a bandpass diplexer attenuates signals away from the 310.1875 MHz IF signal.

The **LO Feedthrough Cancellation** circuit generates a signal that reduces LO feedthrough. During calibration, LO feedthrough is measured and the information is sent to the CPU assembly. The CPU assembly then adjusts the amplitude and phase of the LO feedthrough cancellation signal using three control lines from the Input assembly.

The **First IF Amplifier** increases the amplitude of the 310.1875 MHz signal by approximately 15 dB. Between this circuit's two gain stages, it adds the LO feedthrough cancellation signal to the input signal. At the output of this circuit, a low pass filter attenuates signals greater than 350 MHz.

The **First IF Bandpass Filter** (a service adjustable helical resonator filter) attenuates signals out of the passband centered at 310.1875 MHz.

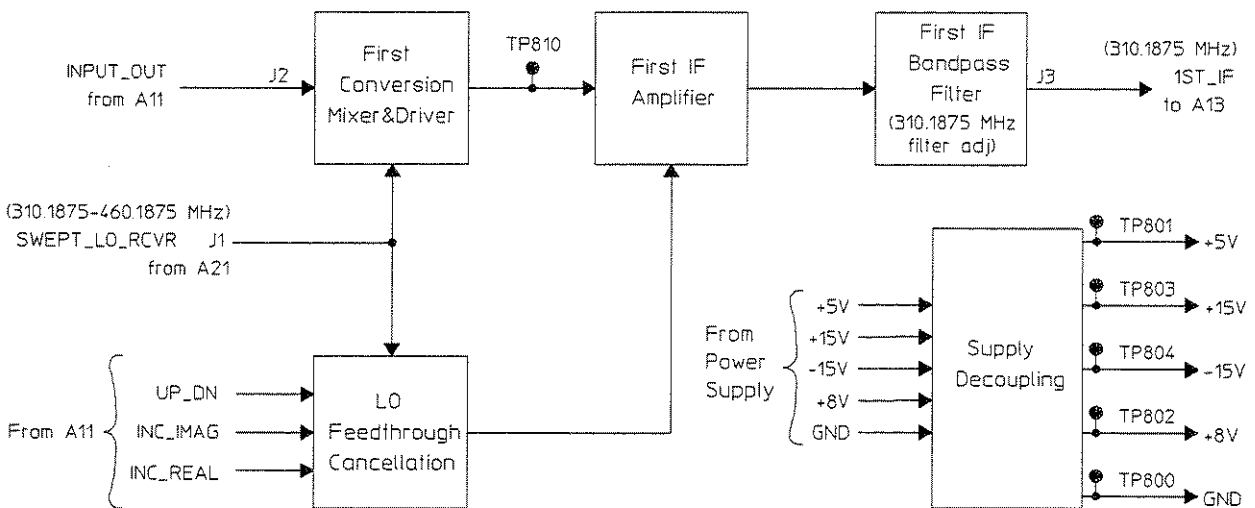


Figure 4-9. A12 First Conversion Block Diagram

A13 Second Conversion

The Second Conversion assembly is the third of five assemblies that condition the input signal. This assembly mixes a 300 MHz frequency reference with the 310.1875 MHz signal from the First Conversion assembly. The resulting 10.1875 MHz signal is routed to the IF assembly. Figure 4-10 shows the Second Conversion assembly's block diagram.

The **350 MHz Low Pass Filter** attenuates signals greater than 350 MHz.

The **Second Conversion Mixer/Driver** increases the amplitude of the 300 MHz reference signal to +17 dBm at the mixer input. It then mixes the reference signal with the 310.1875 MHz IF signal.

The **12 MHz Low Pass Filter** attenuates signals above the 10.1875 MHz second IF frequency.

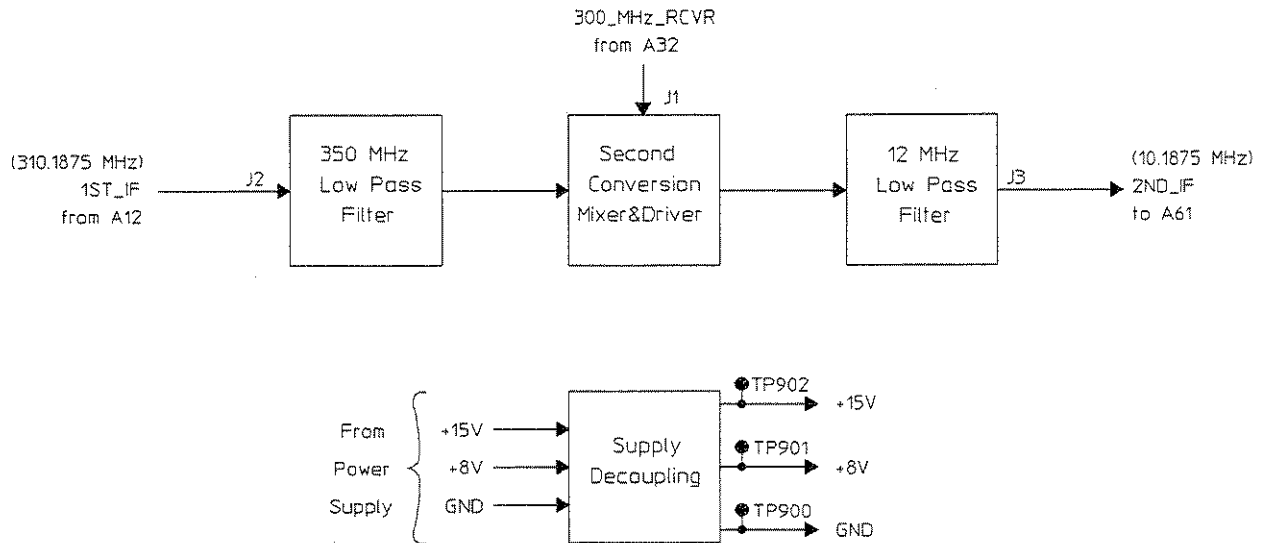


Figure 4-10. A13 Second Conversion Block Diagram

A21 Sum VCO

The Sum VCO assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used when the local oscillator operates in either single loop mode or multiple loop mode (see figures 4-12 and 4-13). The Sum VCO assembly provides four signals that can sweep from 310.1875 to 460.1875 MHz. Two of these signals provide feedback — one to close the single loop mode's single loop and another to close the multiple loop mode's sum loop. The other two signals provide the swept LO signal for the First Conversion assembly and the Source Conversion assembly. Figure 4-11 shows the Sum VCO assembly's block diagram.

In single loop mode, the **Control Voltage Switch** connects the single loop control voltage to the Sum Loop VCO. In multiple loop mode, this switch connects the multiple loop control voltage to the Sum Loop VCO. If multiple loop mode's sum loop is unlocked, the Out of Lock Detector on the Sum Phase Detector assembly provides a control line to this circuit that speeds up the sum loop's settling time. The IIC Interface on the Step Phase Detector assembly provides the control line that selects multiple or single loop mode. This switch also provides the control line for the Single Loop Bias Shutdown Switch.

The **Sum Loop VCO** generates a signal that can sweep from 310.1875 to 460.1875 MHz. The multiple or single loop control voltage controls the VCO's frequency. This circuit also contains two service adjustments — one to improve the spectral purity of the VCO and the other to improve the tracking of the sum loop VCO and step loop VCO to each other.

The **Sum Loop Buffers** route the swept signal through four buffered signal paths that are current biased by the **Amplifier Current Sources**.

In multiple loop mode, the **Single Loop Bias Shutdown Switch** turns off the current biasing for the single loop VCO signal path.

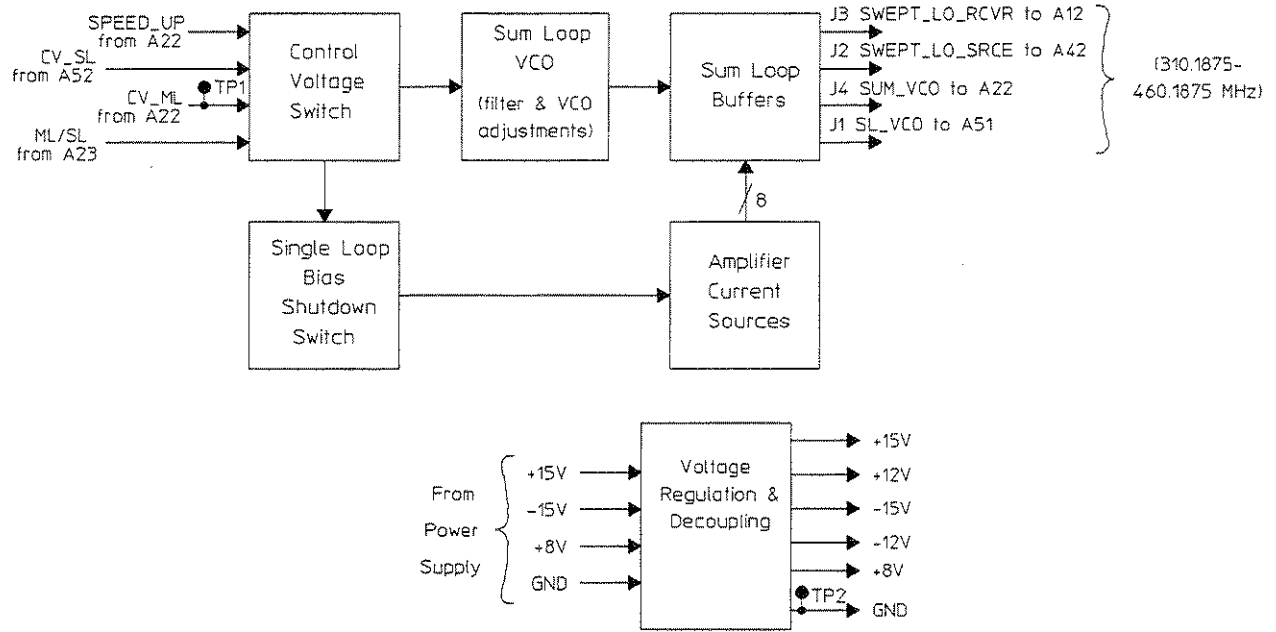


Figure 4-11. A21 Sum VCO Block Diagram



The analyzer's local oscillator operates in either single loop mode or multiple loop mode. The CPU assembly selects which mode based on the frequency span, resolution bandwidth, and sweep time of the measurement. Single loop mode allows the fastest sweep time, and multiple loop mode provides better phase noise and spurious performance. Therefore, the local oscillator uses multiple loop mode for all narrow-band zoom measurements and for swept spectrum measurements with slow sweep time, narrow frequency span, and narrow resolution bandwidth, and single loop mode for all other swept spectrum measurements.

In single loop mode, the local oscillator uses one PLL (phase-locked loop) — single loop (see figure 4-12). In multiple loop mode, the local oscillator uses three PLLs — step loop, interpolation loop, and sum loop (see figure 4-13).

In the single loop, the feedback signal (SL_VCO) is divided by ten. The resulting signal (F/N_VCO) is then divided down to 100 kHz. The phases of the divided signal and the 100 kHz reference signal (100_KHZ_REF) are compared and integrated by the integrator. The output voltage of the integrator becomes the control voltage (CV_SL) for the sum VCO. The output of the sum VCO is routed to three signal paths — one provides feedback (SL_VCO) for the single loop, and the other two provide the swept LO for the source and receiver (SWEPT_LO_SRCE and SWEPT_LO_RCVR).

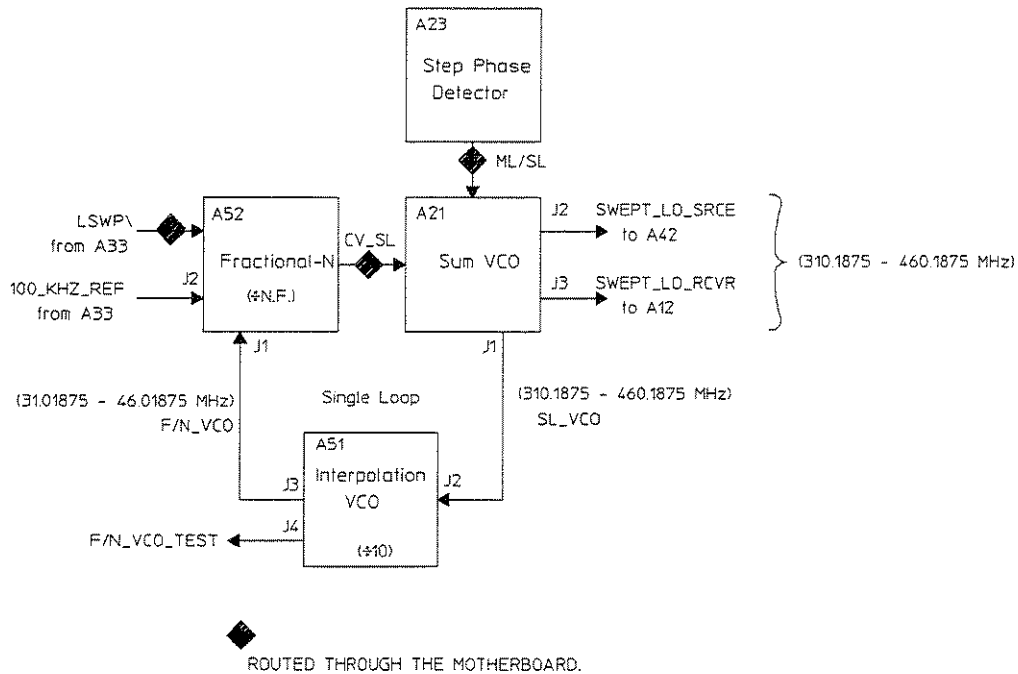


Figure 4-12. Local Oscillator in Single Loop Mode

Note



In the interpolation loop (see figure 4-13), the feedback signal (F/N_VCO) is divided down to 100 kHz. The phases of the divided feedback signal and the 100 kHz reference signal (100_KHZ_REF) are then compared, and integrated by the integrator. The output voltage of the integrator becomes the control voltage (CV_FRACN) for the interpolation VCO. The output of the interpolation VCO is routed to two signal paths — one provides feedback (F/N_VCO) to close the interpolation loop, and the other provides a signal that is divided by 5 or 10, then sent to the sum loop for fine frequency tuning (INTRPL_VCO).

In the step loop, the feedback signal (STEP_VCO) is mixed with the 300 MHz frequency reference (300_MHZ_REF). The difference frequency is divided down to 2 or 5 MHz. The 10 MHz frequency reference (10_MHZ_REF) is also divided down to 2 or 5 MHz. The phases of the two signals are compared, and integrated by the integrator. The output voltage of the integrator becomes the control voltage (CV_STEP) for the step VCO and the pretune voltage (PRETUNE) for the sum loop. The output of the step VCO is routed to two signal paths — one provides feedback (STEP_VCO) to close the step loop, and the other provides the sum loop with a phase reference (STEP_TO_SUM).

In the sum loop, the feedback signal (SUM_VCO) is mixed with the step signal (STEP_TO_SUM). The phases of the difference frequency and the interpolation VCO (INTRPL_VCO) are then compared, and integrated by the integrator. Pretune voltage (PRETUNE) is added to the output voltage of the integrator (to ensure that the sum loop can phase lock), and the resulting voltage becomes the control voltage (CV_ML) for the sum VCO. The output of the sum VCO is routed to three signal paths — one provides feedback to close the sum loop (SUM_VCO), and the other two provide the swept LO for the source and receiver (SWEPT_LO_SRCE and SWEPT_LO_RCVR).

The divide by numbers and frequencies that generate the lower swept LO frequencies (310.1875 to 341 MHz) are labeled L. The divide by numbers and frequencies that generate the higher swept LO frequencies (341 to 460.1875 MHz) are labeled H. See table 4-1 for a matrix of frequencies when the local oscillator is in multiple loop mode.

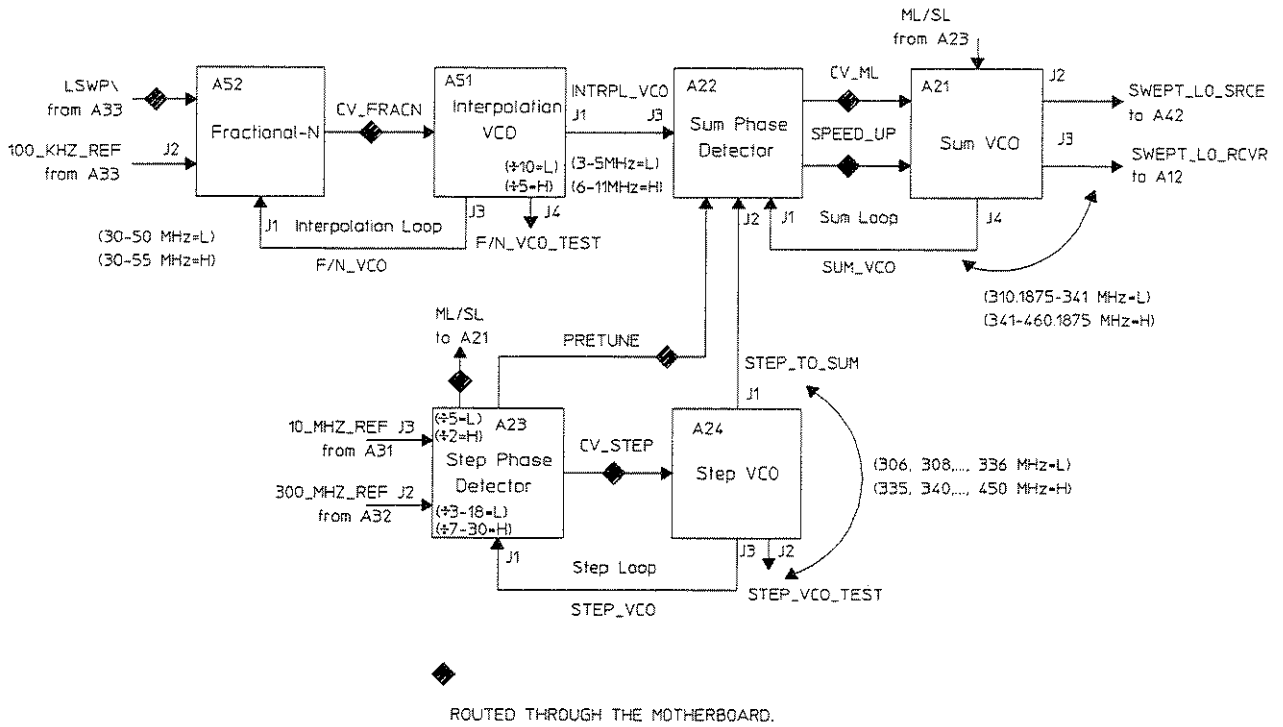


Figure 4-13. Local Oscillator in Multiple Loop Mode

Table 4-1. Multiple Loop Mode Frequency Matrix

| Measurement Freq | | Sum VCO | | Step VCO | | F/N VCO | | Intrpl VCO | |
|-----------------------|-----------------|----------------|---------------|---------------|----------------|----------------|---------------|----------------|---------------|
| Start \geq (MHz) | Stop < (MHz) | Start (MHz) | Stop (MHz) | Freq (MHz) | Divide By N | Start (MHz) | Stop (MHz) | Start (MHz) | Stop (MHz) |
| 0.0 | 0.8125 | 310.1875 | 311.0 | 306 | 3 | 41.875 | 50.0 | 4.1875 | 5.0 |
| 0.8125 | 2.8125 | 311.0 | 313.0 | 308 | 4 | 30.0 | 50.0 | 3.0 | 5.0 |
| 2.8125 | 4.8125 | 313.0 | 315.0 | 310 | 5 | 30.0 | 50.0 | 3.0 | 5.0 |
| 4.8125 | 6.8125 | 315.0 | 317.0 | 312 | 6 | 30.0 | 50.0 | 3.0 | 5.0 |
| 6.8125 | 8.8125 | 317.0 | 319.0 | 314 | 7 | 30.0 | 50.0 | 3.0 | 5.0 |
| 8.8125 | 10.8125 | 319.0 | 321.0 | 316 | 8 | 30.0 | 50.0 | 3.0 | 5.0 |
| 10.8125 | 12.8125 | 321.0 | 323.0 | 318 | 9 | 30.0 | 50.0 | 3.0 | 5.0 |
| 12.8125 | 14.8125 | 323.0 | 325.0 | 320 | 10 | 30.0 | 50.0 | 3.0 | 5.0 |
| 14.8125 | 16.8125 | 325.0 | 327.0 | 322 | 11 | 30.0 | 50.0 | 3.0 | 5.0 |
| 16.8125 | 18.8125 | 327.0 | 329.0 | 324 | 12 | 30.0 | 50.0 | 3.0 | 5.0 |
| 18.8125 | 20.8125 | 329.0 | 331.0 | 326 | 13 | 30.0 | 50.0 | 3.0 | 5.0 |
| 20.8125 | 22.8125 | 331.0 | 333.0 | 328 | 14 | 30.0 | 50.0 | 3.0 | 5.0 |
| 22.8125 | 24.8125 | 333.0 | 335.0 | 330 | 15 | 30.0 | 50.0 | 3.0 | 5.0 |
| 24.8125 | 26.8125 | 335.0 | 337.0 | 332 | 16 | 30.0 | 50.0 | 3.0 | 5.0 |
| 26.8125 | 28.8125 | 337.0 | 339.0 | 334 | 17 | 30.0 | 50.0 | 3.0 | 5.0 |
| 28.8125 | 30.8125 | 339.0 | 341.0 | 336 | 18 | 30.0 | 50.0 | 3.0 | 5.0 |
| 30.8125 | 35.8125 | 341.0 | 346.0 | 335 | 7 | 30.0 | 55.0 | 6.0 | 11.0 |
| 35.8125 | 40.8125 | 346.0 | 351.0 | 340 | 8 | 30.0 | 55.0 | 6.0 | 11.0 |
| 40.8125 | 45.8125 | 351.0 | 356.0 | 345 | 9 | 30.0 | 55.0 | 6.0 | 11.0 |
| 45.8125 | 50.8125 | 356.0 | 361.0 | 350 | 10 | 30.0 | 55.0 | 6.0 | 11.0 |
| 50.8125 | 55.8125 | 361.0 | 366.0 | 355 | 11 | 30.0 | 55.0 | 6.0 | 11.0 |
| 55.8125 | 60.8125 | 366.0 | 371.0 | 360 | 12 | 30.0 | 55.0 | 6.0 | 11.0 |
| 60.8125 | 65.8125 | 371.0 | 376.0 | 365 | 13 | 30.0 | 55.0 | 6.0 | 11.0 |
| 65.8125 | 70.8125 | 376.0 | 381.0 | 370 | 14 | 30.0 | 55.0 | 6.0 | 11.0 |
| 70.8125 | 75.8125 | 381.0 | 386.0 | 375 | 15 | 30.0 | 55.0 | 6.0 | 11.0 |
| 75.8125 | 80.8125 | 386.0 | 391.0 | 380 | 16 | 30.0 | 55.0 | 6.0 | 11.0 |
| 80.8125 | 85.8125 | 391.0 | 396.0 | 385 | 17 | 30.0 | 55.0 | 6.0 | 11.0 |
| 85.8125 | 90.8125 | 396.0 | 401.0 | 390 | 18 | 30.0 | 55.0 | 6.0 | 11.0 |
| 90.8125 | 95.8125 | 401.0 | 406.0 | 395 | 19 | 30.0 | 55.0 | 6.0 | 11.0 |
| 95.8125 | 100.8125 | 406.0 | 411.0 | 400 | 20 | 30.0 | 55.0 | 6.0 | 11.0 |
| 100.8125 | 105.8125 | 411.0 | 416.0 | 405 | 21 | 30.0 | 55.0 | 6.0 | 11.0 |
| 105.8125 | 110.8125 | 416.0 | 421.0 | 410 | 22 | 30.0 | 55.0 | 6.0 | 11.0 |
| 110.8125 | 115.8125 | 421.0 | 426.0 | 415 | 23 | 30.0 | 55.0 | 6.0 | 11.0 |
| 115.8125 | 120.8125 | 426.0 | 431.0 | 420 | 24 | 30.0 | 55.0 | 6.0 | 11.0 |
| 120.8125 | 125.8125 | 431.0 | 436.0 | 425 | 25 | 30.0 | 55.0 | 6.0 | 11.0 |
| 125.8125 | 130.8125 | 436.0 | 441.0 | 430 | 26 | 30.0 | 55.0 | 6.0 | 11.0 |
| 130.8125 | 135.8125 | 441.0 | 446.0 | 435 | 27 | 30.0 | 55.0 | 6.0 | 11.0 |
| 135.8125 | 140.8125 | 446.0 | 451.0 | 440 | 28 | 30.0 | 55.0 | 6.0 | 11.0 |
| 140.8125 | 145.8125 | 451.0 | 456.0 | 445 | 29 | 30.0 | 55.0 | 6.0 | 11.0 |
| 145.8125 | 150.0 | 456.0 | 460.1875 | 450 | 30 | 30.0 | 50.9375 | 6.0 | 10.1875 |

A22 Sum Phase Detector

The Sum Phase Detector assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used only when the local oscillator operates in multiple loop mode (see figure 4-13). The Sum Phase Detector assembly generates the multiple loop control voltage for the sum loop. If the control voltage is out of range, this assembly clamps the voltage and tells the CPU assembly. Figure 4-14 shows the Sum Phase Detector assembly's block diagram.

The **Offset Mixer** mixes the sum VCO signal with the step signal. When the sum VCO signal sweeps from 310.1875 to 341 MHz, the step signal steps from 306 to 336 MHz in 2 MHz increments. When the sum VCO signal sweeps from 341 to 460.1875 MHz, the step signal steps from 335 to 450 MHz in 5 MHz increments.

The **Sum Loop Phase Detector** compares the phase of the signal from the Offset Mixer to the phase of the interpolation VCO and generates a voltage relative to the phase difference. When the sum VCO signal is in the range from 310.1875 to 341 MHz, the interpolation signal sweeps from 3 to 5 MHz, and when the sum VCO signal is in the range from 341 to 460.1875 MHz, the interpolation signal sweeps from 6 to 11 MHz.

The **Sum Loop Integrator** integrates the phase difference of the two signals. To ensure that the sum loop can phase lock, pretune voltage is added to the output of the integrator. This voltage provides the control voltage for the multiple loop.

The **Out-of-Lock Detector** clamps the output of the integrator (before the pretune voltage is added) if the amplitude is not within the range of -0.6 to $+0.15$ V. It then tells the CPU assembly that the amplitude is too high or too low, which means the sum loop is unlocked. The Out-of-Lock Detector also provides a control signal, which speeds up the sum loop's settling time when the sum loop is unlocked.

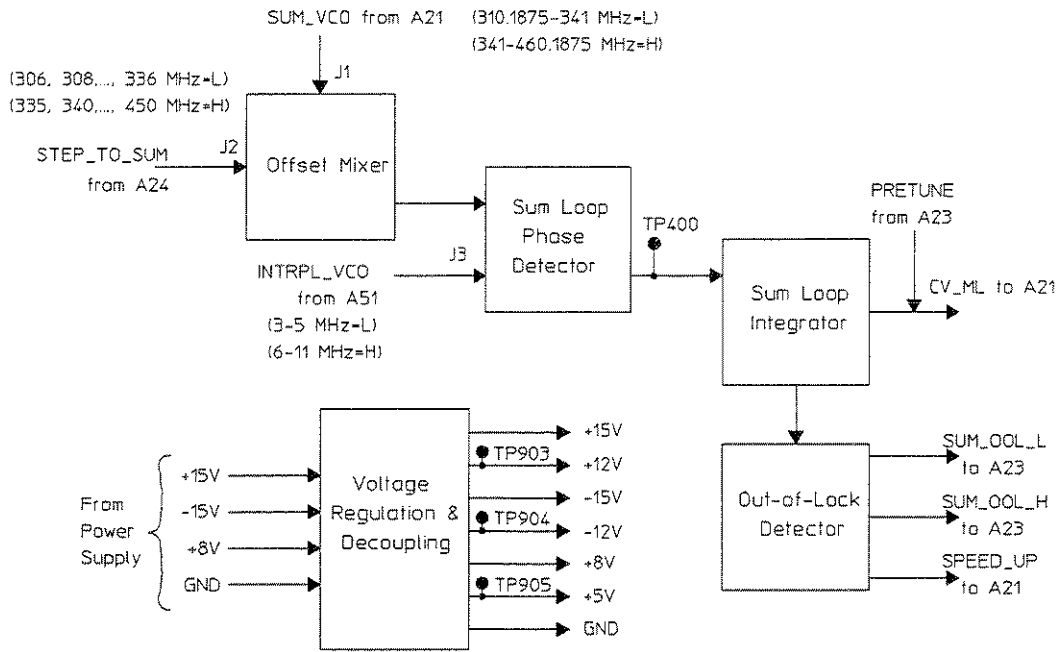


Figure 4-14. A22 Sum Phase Detector Block Diagram

A23 Step Phase Detector

The Step Phase Detector assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used when the local oscillator operates in either single loop mode or multiple loop mode (see figures 4-12 and 4-13). In single loop mode, the Step Phase Detector assembly provides only the loop mode control line. In multiple loop mode, this assembly provides the loop mode control line, the control voltage for the step loop, and the pretune voltage for the sum loop. Figure 4-15 shows the Step Phase Detector assembly's block diagram.

The **Step Loop Offset Mixer** mixes the 300 MHz frequency reference with the stepped VCO signal. It then filters and amplifies the resulting 6 to 150 MHz difference frequency.

The **Divide-by-N Counter** produces either a 2 or 5 MHz signal by dividing the 6 to 150 MHz difference frequency with a number between 3 and 30. When the step VCO signal steps from 306 to 336 MHz in 2 MHz increments, this circuit divides by a number (between 3 and 18) that produces a 2 MHz signal. When the step VCO signal steps from 335 to 450 MHz in 5 MHz increments, this circuit divides by a number (between 7 and 30) that produces a 5 MHz signal.

The **Step Size Divider** divides the 10 MHz frequency reference by 5 when the Divide-by-N Counter selects a number that produces a 2 MHz signal, or by 2 when the Divide-by-N Counter selects a number that produces a 5 MHz signal.

The **Step Loop Phase Detector** compares the phase of the signal from the Step Size Divider to the phase of the signal from the Divide-by-N Counter. It then generates a voltage proportional to the phase difference.

The **Step Loop Integrator** amplifies and integrates the phase difference voltage, creating the step loop control voltage.

The **VCO Clamps** compare the control voltage to service adjustable out-of-limit voltages. This circuit clamps the control voltage if its amplitude is not within the approximate range of -2 to $+7$ V. It also tells the CPU assembly that the amplitude is too high or too low, which means the step loop is unlocked.

The **Pretune** circuit adds a service adjustable dc offset level to the control voltage, then amplifies it by a service adjustable gain. The resulting voltage coarsely adjusts the sum VCO's frequency to ensure that the sum loop can phase lock.

The **IIC Interface** provides the interface between the CPU assembly and the Step Phase Detector assembly, and it provides the loop mode control line to the Sum VCO assembly. It also interrupts the CPU assembly if either the sum loop or the step loop is unlocked.

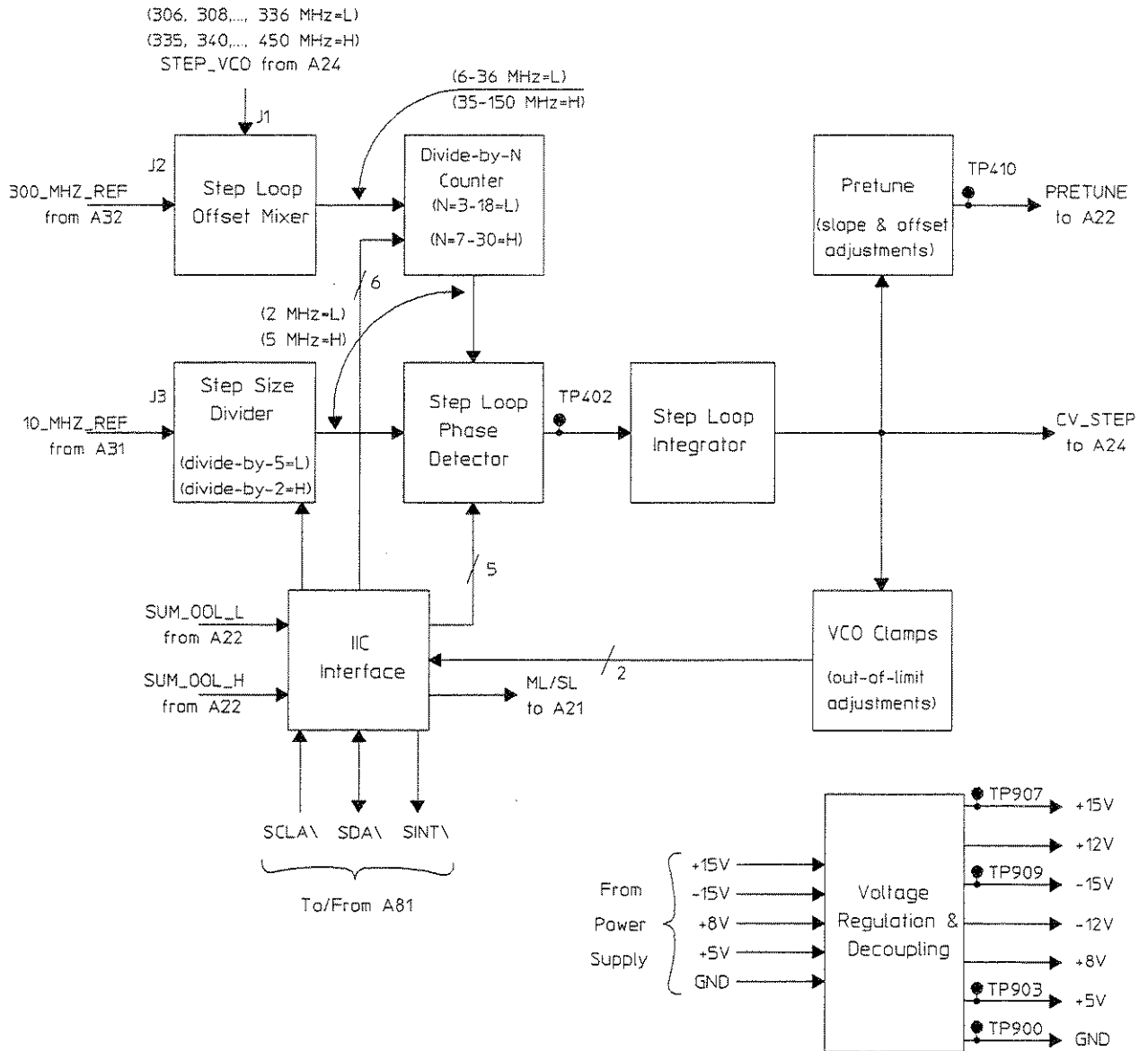


Figure 4-15. A23 Step Phase Detector

A24 Step VCO

The Step VCO assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used only when the local oscillator operates in multiple loop mode (see figure 4-13). The Step VCO assembly generates a 306 to 450 MHz signal that provides feedback for the step loop and an offset frequency reference for the sum loop. Figure 4-16 shows the Step VCO assembly's block diagram.

The **Step Loop VCO** generates a signal that steps from 306 to 336 MHz in 2 MHz increments or from 335 to 450 MHz in 5 MHz increments. In single loop mode, this VCO generates a 306 MHz signal even though the signal is not used. The step loop control voltage controls the VCO's frequency. This circuit also contains two service adjustments — one to improve the spectral purity of the VCO and the other to improve the tracking of the sum loop VCO and step loop VCO to each other.

The **Step Loop Buffers** route the signal into three separate signal paths that filter and amplify each signal. One signal provides feedback to close the step loop. Another signal provides an offset frequency reference for the sum loop. The third signal provides a test port to check the sum loop.

The **Thermal Switch** shuts down the Power Supply assembly if it senses an over-temperature condition.

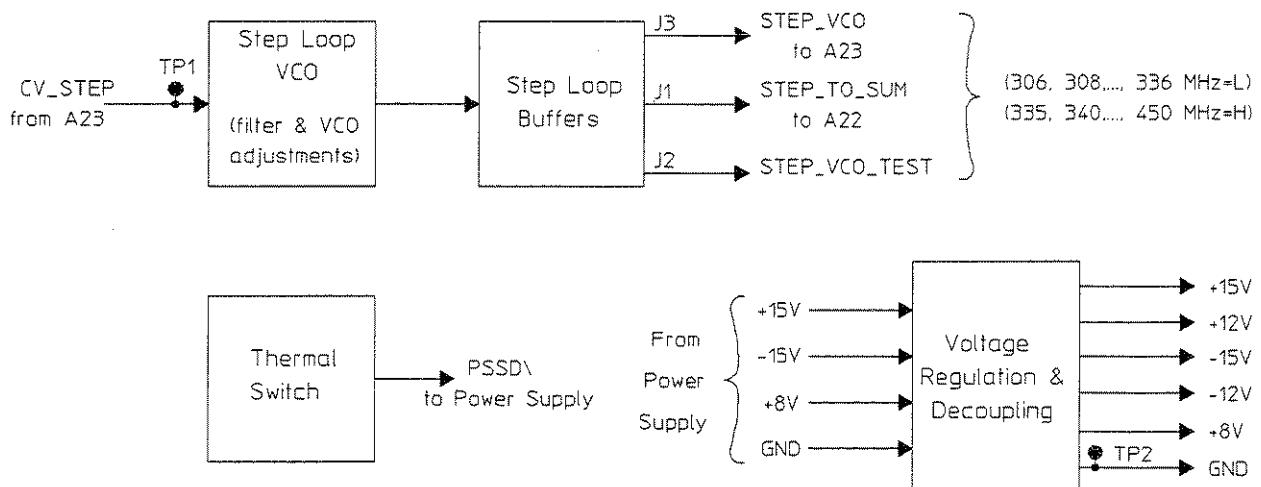


Figure 4-16. A24 Step VCO Block Diagram

A31 Reference/Calibrator

The Reference/Calibrator assembly provides three frequency references (80, 20, and 10 MHz) to various assemblies. It also provides a precision amplitude calibration signal to the Input assembly. This precision amplitude calibration signal is actually one of two signals — a precision leveled signal derived from the Source Amplifier assembly or a precision leveled fixed 10 MHz frequency reference. Figure 4-17 shows the Reference/Calibrator assembly's block diagram.

The **80 MHz VCXO** generates an 80 MHz signal, which is the analyzer's primary frequency reference. When an external frequency reference is present, feedback phase-locks the 80 MHz VCXO to the external reference. A service adjustment is provided to adjust the VCXO's frequency.

The **Divide-by-4** circuit divides the 80 MHz signal down to 20 MHz. The **Divide-by-2** circuit divides the 20 MHz signal down to 10 MHz.

The **Input Protection/Signal Conditioning** circuit limits and conditions the external frequency reference. The optional Fan Power/Oven assembly can supply the external frequency reference if a rear panel BNC-to-BNC jumper connects the oven output to the external frequency reference input.

The **External Reference Detector** detects the presence of the external reference, and tells both Tune Enable/Loop Filter/Integrator and the CPU assembly.

The **Sampling Phase Detector** compares the phase of the signal from the Divide-by-2 with the phase of the signal from Input Protection/Signal Conditioning and generates a voltage equal to the phase difference. This circuit can phase lock to an external frequency reference of 1, 2, 5, or 10 MHz.

The **Tune Enable/Loop Filter/Integrator** amplifies and filters the phase-difference voltage from the Sampling Phase Detector. It then routes the voltage to the 80 MHz VCXO as feedback to close the external reference phase-locked loop (PLL). If an external reference is not present, this circuit opens the PLL and routes zero volts to the 80 MHz VCXO. If the Beatnote Detector indicates that the loop is unlocked, this circuit selects a wider loop bandwidth in an attempt to lock.

The **Beatnote Detector** monitors the feedback voltage to the 80 MHz VCXO. If the feedback voltage is either too high or too low (approx $\pm 10V$), indicating that the external reference PLL is unlocked, this circuit tells the Tune Enable/Loop Filter/Integrator and the CPU assembly.

During swept mode calibration, **Swept Cal** amplifies and conditions the swept 200 kHz to 150 MHz, approximate -11 dBm signal to a square wave with a -3 dBm fundamental. During fixed mode calibration, **Fixed 10 MHz Cal** conditions the 10 MHz signal to a square wave with a -3 dBm fundamental.

The **Precision Square Wave Generator** attenuates and conditions the -3 dBm swept or fixed calibration signal to a square wave with a -20 dBm precision amplitude fundamental. This circuit contains both a flatness and a level service adjustment.

The **IIC Interface** provides the interface between the CPU assembly and the Reference/Calibrator assembly. It also interrupts the CPU assembly if the Beatnote Detector indicates that the external reference PLL is unlocked or if the high frequency PLL on the 300 MHz assembly is unlocked.

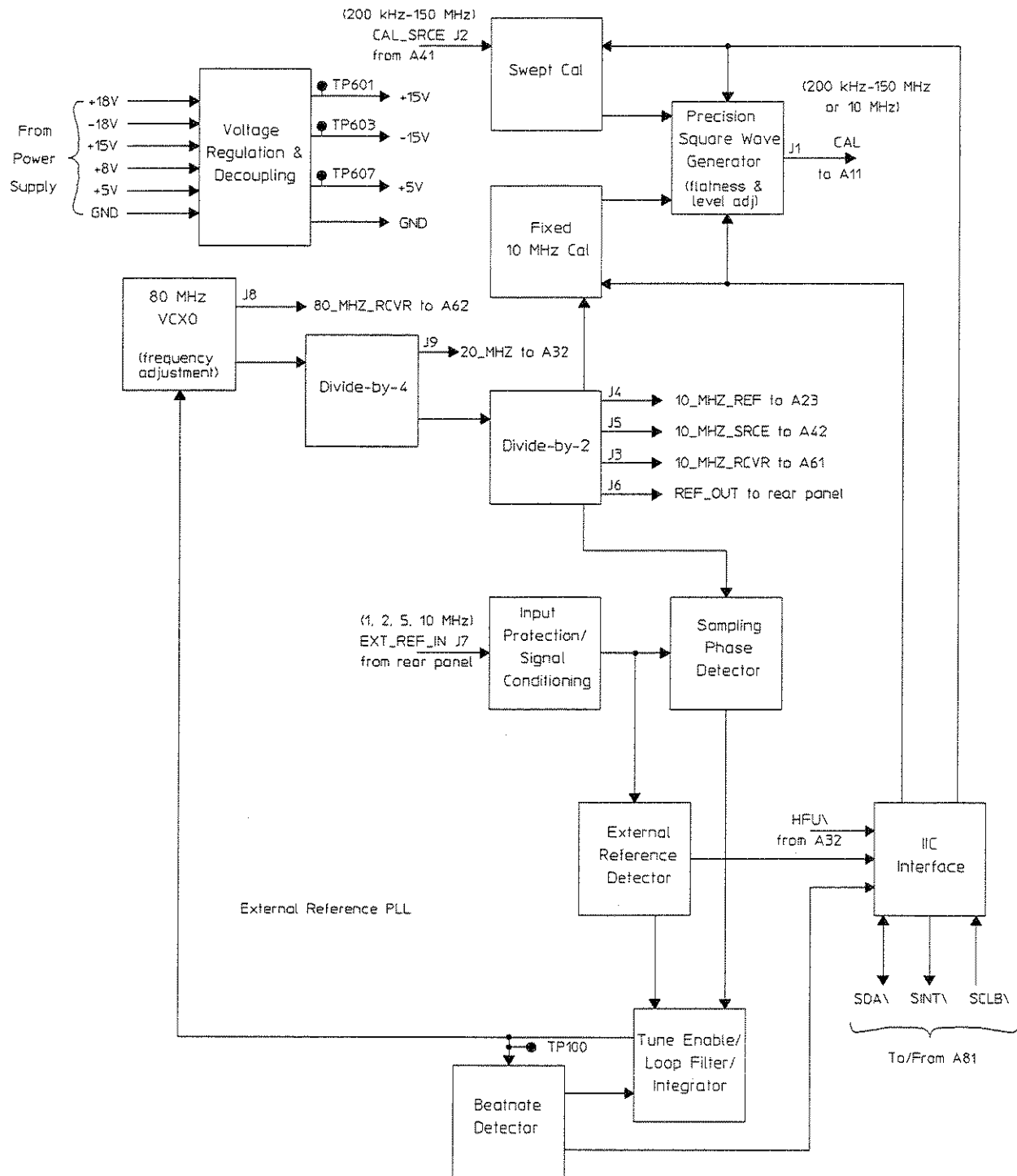


Figure 4-17. A31 Reference/Calibrator Block Diagram

A32 300 MHz

The 300 MHz assembly provides high-frequency references to various assemblies. The high-frequency references are 300 MHz and 60 MHz. These frequency references are phase locked to the Reference/Calibrator assembly at 20 MHz. Figure 4-18 shows the 300 MHz assembly's block diagram.

The **300 MHz VCO** generates a 300 MHz signal. A service adjustment sets the frequency of this VCO. Feedback from the Loop Filter/Integrator adjusts the frequency to keep this VCO phase locked with the 20 MHz reference signal.

The **300 MHz Amplifier** routes the 300 MHz signal to four signal paths and amplifies each signal.

The **Divide-by-5** circuit divides the 300 MHz signal down to 60 MHz and routes the signal to two signal paths. The **Divide-by-3** circuit divides the 60 MHz signal down to 20 MHz.

The **Digital Phase Detector** compares the phase of the 20 MHz signal to the 20 MHz reference signal and generates a voltage equal to the phase difference.

The **Loop Filter/Integrator** filters the phase difference voltage and sends it to the 300 MHz VCO as the control voltage.

The **PLL Unlocked Detector** monitors the voltage from the Loop Filter/Integrator. If the voltage goes too high or too low, the high-frequency PLL unlocks and the Reference/Calibrator assembly interrupts the CPU assembly.

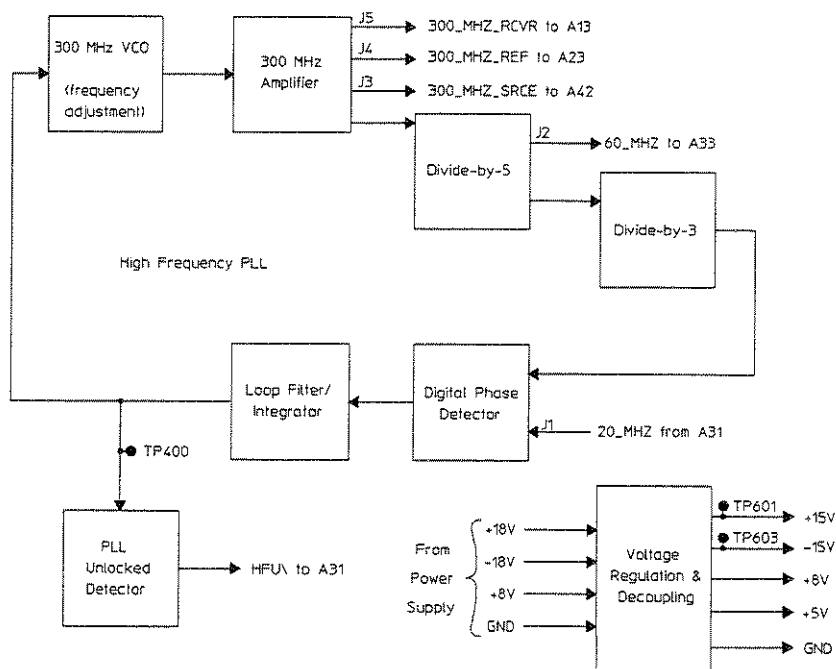


Figure 4-18. A32 300 MHz Block Diagram

A33 Trigger

The Trigger assembly provides low-frequency reference signals, the sweep synchronization signal (LSWP), and the trigger signal. The low frequency reference signals are 100 kHz, 187.5 kHz, and 250 kHz. Figure 4-19 shows the Trigger assembly's block diagram.

The **Divide-by-4** circuit divides the 60 MHz signal down to 15 MHz. The **Divide-by-10** circuit divides the 15 MHz signal down to 1.5 MHz.

The **Clock Synchronization** circuit resets all low-frequency references at instrument power-up and provides the 1.5 MHz signal as a common clock.

The **Divide-by-6** circuit divides the 1.5 MHz signal down to a 250 kHz, TTL-level signal. The **Divide-by-8** circuit divides the 1.5 MHz signal down to a 187.5 kHz, 600 mVp-p, ac-coupled square wave. The **Divide-by-15** circuit reduces the 1.5 MHz signal to a 100 kHz, 1 Vp-p pulse, with an approximate 1% duty cycle.

The **Divide-by-2ⁿ** circuit divides the 100 kHz signal by 2ⁿ, generating the Slow Clock. The CPU assembly provides the decimating number **n**.

The **Trigger Logic** circuit selects internal trigger, external trigger, or HP-IB trigger (GETTRIG). Internal trigger is self-enabling. External trigger and HP-IB trigger, however, must be enabled by the CPU assembly.

When the selected trigger occurs, Trigger Logic holds the trigger and, after receiving a negative edge from the Slow Clock, outputs it as the sweep synchronization signal (LSWP). Following a change in resolution bandwidth or an instrument power-up or preset, the negative edge of the sweep synchronization signal resets the phase of the digital filters on the ADC/Digital Filter assembly. On subsequent negative edges, the sweep synchronization signal is the sweep signal for the analyzer. The sweep synchronization signal is also sent to the rear panel as the trigger output.

The **IIC Interface** provides the interface between the CPU assembly and the Trigger assembly.

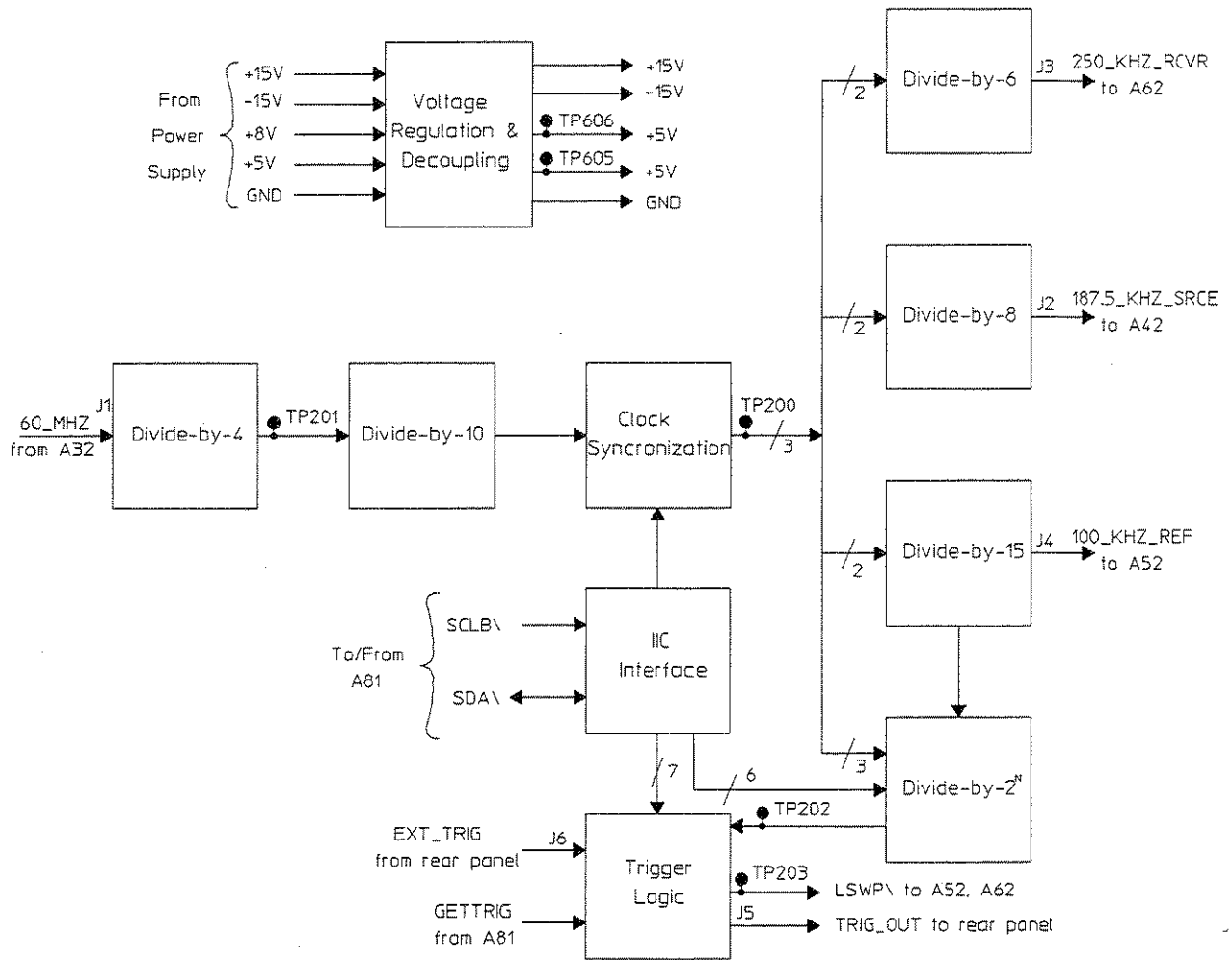


Figure 4-19. A33 Trigger Block Diagram

A41 Source Amplifier

The Source Amplifier assembly is one of two assemblies that together function as the analyzer's source. This assembly amplifies the signal generated by the Source Conversion assembly. It then routes this signal to either the Front Panel assembly, the Input assembly, or the Reference/Calibrator assembly. The output of the Source Amplifier assembly can sweep from 10 Hz to 150 MHz and its amplitude can be adjusted from +10 to -59.9 dBm. Figure 4-20 shows the Source Amplifier assembly's block diagram.

The two **20 dB Amplifiers** and the one **15 dB Amplifier** provide 55 dB of gain to the signal from the Source Conversion assembly.

The **DC Servo** provides feedback to drive the dc voltage to zero volts at the output of the 15 dB Amplifier.

The **Attenuator** provides from 0 to 50 dB of attenuation, in 10 dB increments.

The **Output Switching** circuit routes the source signal to either the front panel or the Input assembly (for normalized measurements). During calibration, this circuit also routes the source signal to the Reference/Calibrator assembly.

The **Overload Detector/Threshold Set** monitors the voltage at the output of the Source Amplifier assembly. If the voltage exceeds the threshold set by the Source Conversion assembly, this circuit tells the IIC Interface, which in turn, disconnects the output from the front panel and interrupts the CPU assembly.

The **IIC Interface** provides the interface between the CPU assembly and the Source Amplifier assembly. It also provides control logic for the signals from the Source Conversion assembly.

The **Thermal Switch** shuts down the Power Supply assembly if it senses an over-temperature condition.

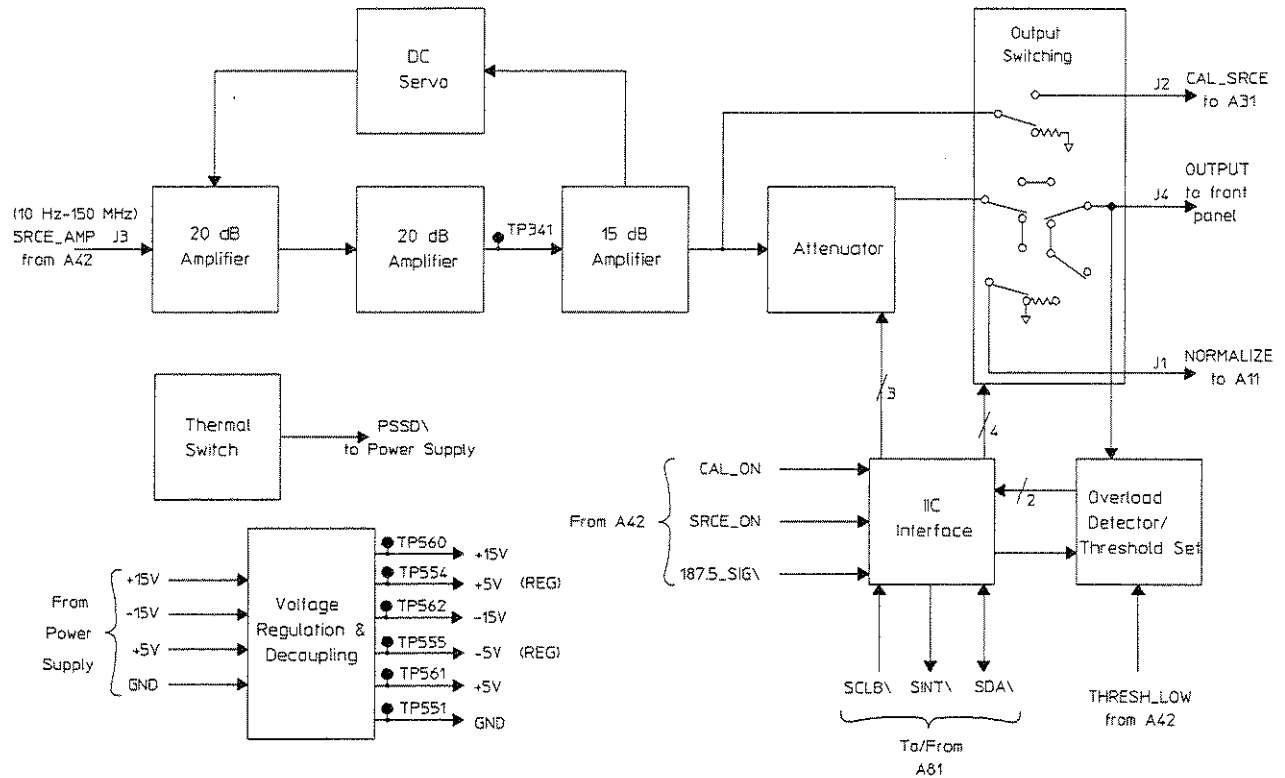


Figure 4-20. A41 Source Amplifier Block Diagram

A42 Source Conversion

The Source Conversion assembly is one of two assemblies that together function as the analyzer's source. The Source Conversion assembly generates the source signal, and the Source Amplifier assembly provides the final amplification for the source signal. Figure 4-21 shows the Source Conversion assembly's block diagram.

The **187.5 kHz Limiter** limits the amplitude of the 187.5 kHz square wave, providing the Gilbert Cell Multiplier with a constant-amplitude square wave. It also provides the dc bias voltage to the Gilbert Cell Multiplier.

The **187.5 kHz Detector** can check for the presence of the signal in one of two places — either at the input of the 187.5 kHz Limiter or the output of the Gilbert Cell Multiplier.

The **Amplitude Control** circuit converts digital data to the differential control signal.

The **Gilbert Cell Multiplier** generates a 187.5 kHz square wave with an amplitude proportional to the amplitude of the differential control signal. The square wave amplitude may be controlled over a 19.9 dB range.

The **190 kHz Low Pass Filter** attenuates signals above 190 kHz (harmonic energy of the 187.5 kHz square wave).

The **10 MHz Limiter/First Mixer** limits the amplitude of the 10 MHz reference signal. It then mixes the 10 MHz signal with the 187.5 kHz signal, producing a 10.1875 MHz signal.

The **10.1875 MHz Filter/Amplifier** filters and amplifies the 10.1875 MHz signal.

The **300 MHz LO Driver** amplifies the 300 MHz reference to +7 dBm at the input to the second mixer.

The **Second Mixer** mixes the 300 MHz signal with the 10.1875 MHz signal, producing a 310.1875 MHz signal.

The **310.1875 MHz Filter/Amplifier** filters and amplifies the 310.1875 MHz signal. This circuit contains a service-adjustable helical resonator filter.

The **LO Driver** amplifies the swept LO signal to +7 dBm at the input of the Third Mixer.

The **Third Mixer** mixes the swept LO signal (310.1875 to 460.1875 MHz) with the 310.1875 MHz signal, producing a frequency that tracks the tuned receiver frequency.

The **150 MHz Low Pass Filter** attenuates all signals above 150 MHz and routes the 10 Hz to 150 MHz swept signal to the Source Amplifier assembly.

The IIC Interface provides control lines from the CPU assembly to both the Source Conversion assembly and the Source Amplifier assembly.

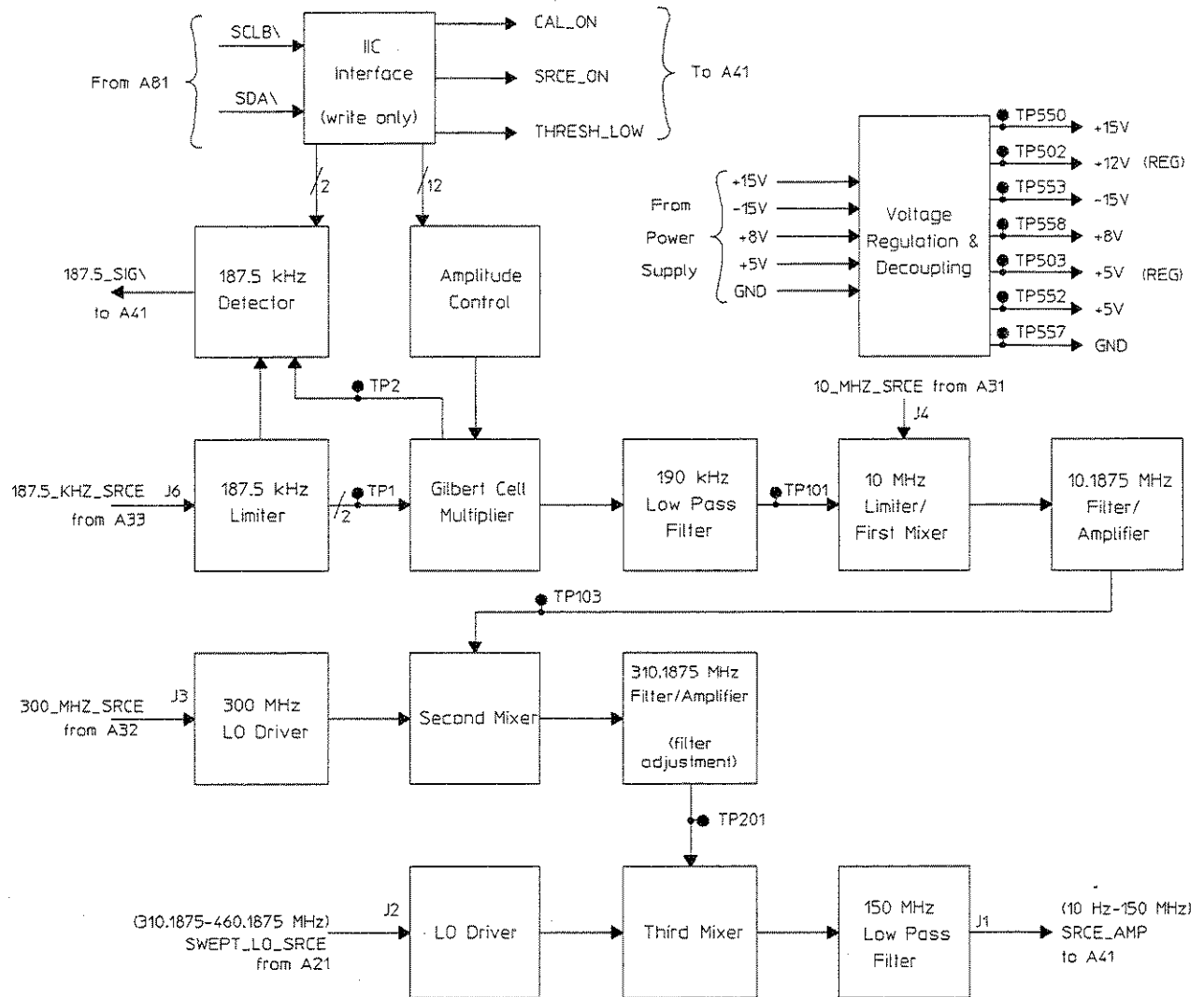


Figure 4-21. A42 Source Conversion Block Diagram

A51 Interpolation VCO

The Interpolation VCO assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used when the local oscillator operates in either single loop mode or multiple loop mode (see figures 4-12 and 4-13). In multiple loop mode, this assembly provides the interpolation VCO and feedback to close the interpolation loop. In single loop mode, this assembly provides feedback to close the single loop. Figure 4-22 shows the Interpolation VCO assembly's block diagram.

In multiple loop mode, the **Interpolation VCO** generates a signal that sweeps from 30 to 50 MHz or from 30 to 55 MHz. The fractional-N control voltage determines the frequency. There's also a service adjustment to control the frequency range. In single loop mode, this VCO is disabled.

The **VCO Buffer Amplifier** conditions the signal and routes it through two signal paths.

The **Divide-by-10/Divide-by-5** circuit divides the signal from the VCO Buffer by 10 or 5. For output frequencies lower than 341 MHz, the VCO sweeps from 30 to 50 MHz and this circuit divides it by 10 (providing a 3 to 5 MHz signal). For output frequencies higher than 341 MHz, the VCO sweeps from 30 to 55 MHz and this circuit divides it by 5 (providing a 6 to 11 MHz signal).

In single loop mode, the **Divide-by-10** circuit divides the single loop VCO signal by 10, resulting in a 31 to 46 MHz signal. In multiple loop mode, this circuit is disabled.

In single loop mode, the **Single/Multiple Loop Switch** sends the signal from the Divide-by-10 to the Fractional-N assembly to close the single PLL. In multiple loop mode, this circuit sends the signal from the VCO Buffer Amplifier to the Fractional-N assembly to close the interpolation PLL.

The **Control Voltage Detector** monitors the amplitude of the fractional-N control voltage, in both multiple and single loop mode. The fractional-N control voltage is the same as the single loop control voltage that is sent to the Sum VCO assembly, except the single loop control voltage is clamped. Therefore, checking the fractional-N control voltage is essentially the same as checking the single loop control voltage.

The **IIC Interface** provides the interface between the CPU assembly and the Interpolation VCO assembly. This circuit interrupts the CPU assembly if the control voltage (from the Control Voltage Detector) is too high or too low — a situation that will occur if the interpolation loop or the single loop is unlocked. The IIC Interface also interrupts the CPU assembly if the fractional-N signal on the Fractional-N assembly reaches the end of its sweep.

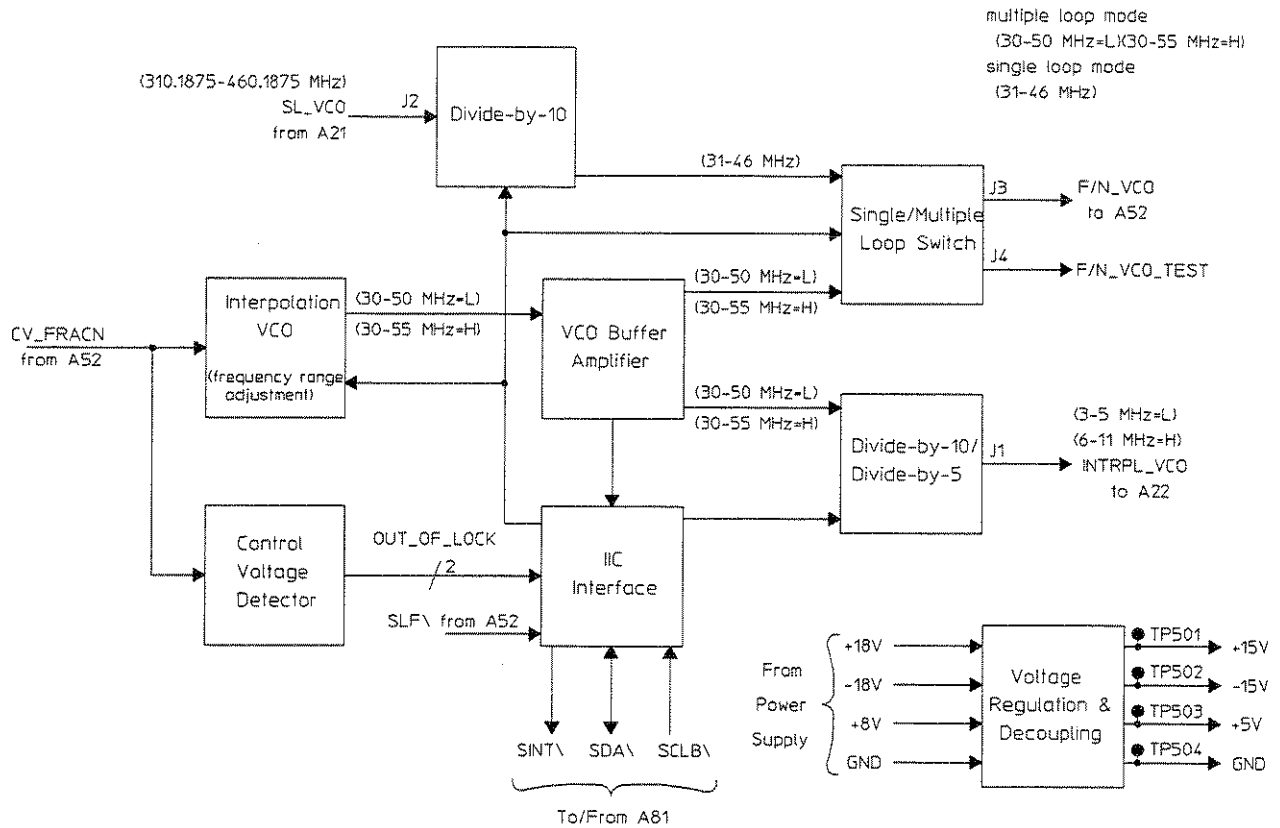


Figure 4-22. A51 Interpolation VCO Block Diagram

A52 Fractional-N

The Fractional-N assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used when the local oscillator operates in either multiple loop mode or single loop mode (see figures 4-12 and 4-13). In single loop mode, this assembly provides the control voltage for the single loop. In multiple loop mode, this assembly provides the control voltage for the interpolation loop. Figure 4-23 shows the Fractional-N assembly's block diagram.

The **Divide-by-N** circuit divides the fractional-N VCO signal down to 100 kHz.

The **Phase Comparator** compares the signal from the Divide-by-N with the 100 kHz reference signal and generates a pulse equal to the phase difference.

The **Integrator** and **Sample and Hold** circuits convert the phase-difference pulses to a dc voltage. A service adjustment minimizes the 100 kHz sample and hold spur.

The **API (Analog Phase Interpolation) Current Control** discharges the Integrator to help maintain a steady dc state. There are also service adjustments to minimize API spurs.

The **Multiple Loop Buffer** conditions the dc voltage and provides it as the control voltage for the interpolation loop.

The **Single Loop Buffer** conditions the dc voltage and provides it as the control voltage for the single loop. The Single Loop Buffer also clamps the control voltage if its amplitude is not within the approximate range of -2 to $+7V$. A service adjustment sets the range of the voltage clamps.

The **Fractional-N** integrated circuit controls the Divide-by-N, API Current Control, and Sample and Hold. The negative edge of the sweep synchronization signal (LSWP\) causes this circuit to start a sweep. If this circuit reaches the end of its frequency sweep, the IIC Interface on the Interpolation VCO assembly can interrupt the CPU assembly.

The **IIC Interface** provides the interface between the CPU assembly and the Fractional-N assembly. After a change in resolution bandwidth or an instrument preset, the IIC Interface also routes the LSWP\ signal to the Fractional-N circuit.

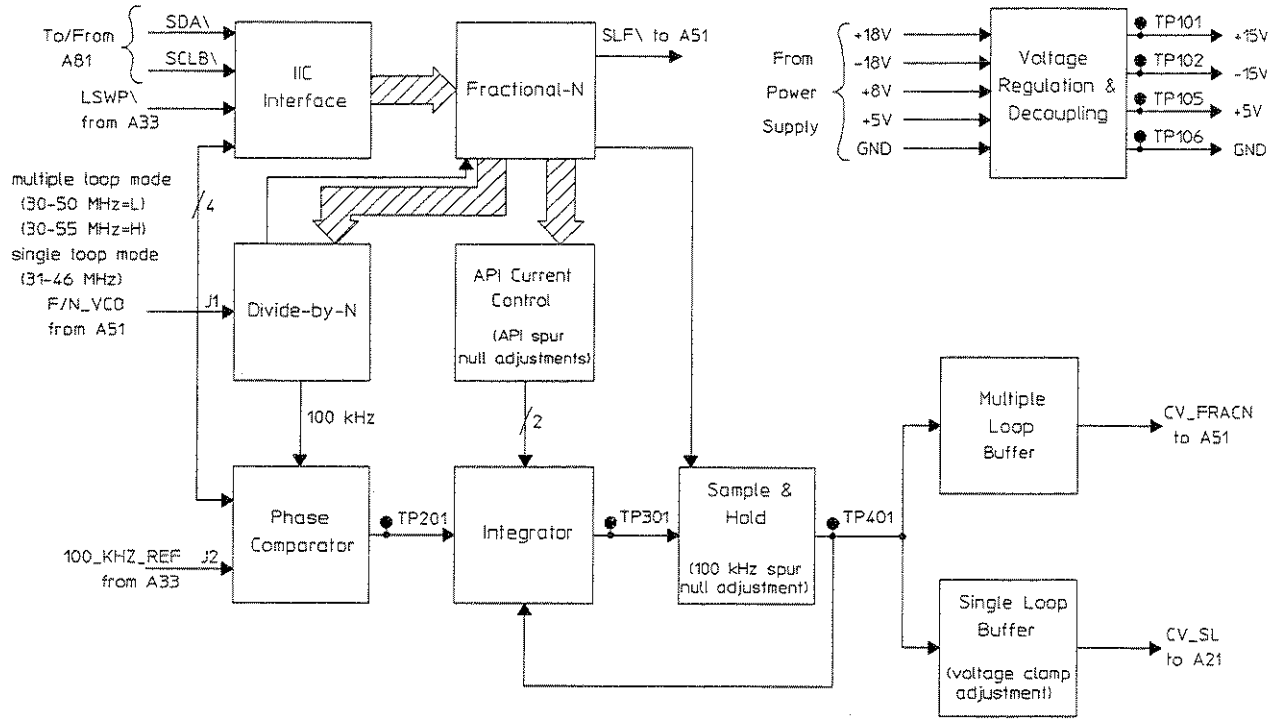


Figure 4-23. A52 Fractional-N Block Diagram

A61 IF

The IF assembly is the fourth of five assemblies that condition the input signal. This assembly converts the output of the Second Frequency Conversion assembly to the third IF signal. Figure 4-24 shows the IF assembly's block diagram.

The **Second IF Amplifier/Filter** amplifies and filters the second IF signal. Also, the analyzer's internal self-test routines use this circuit to detect if the second IF signal is approximately 15 dB over full scale. The filter in this circuit is service-adjustable.

The **10 MHz Reference Receiver** buffers the 10 MHz reference signal. If the 10 MHz reference signal is not present, the Fault Detector on the ADC/Digital Filter assembly interrupts the CPU assembly.

The **Third Conversion Mixer** mixes the second IF signal with the 10 MHz reference signal. This circuit contains a service adjustment to set the gain of the second IF signal.

The **Third IF Filter** then amplifies and filters the resulting 187.5 kHz signal.

The **Third IF Amplifier/Attenuator** amplifies and, under CPU control, subsequently attenuates the signal so that the maximum signal possible (without causing an overload) is available at the analog-to-digital converter (ADC) on the ADC/Digital Filter assembly.

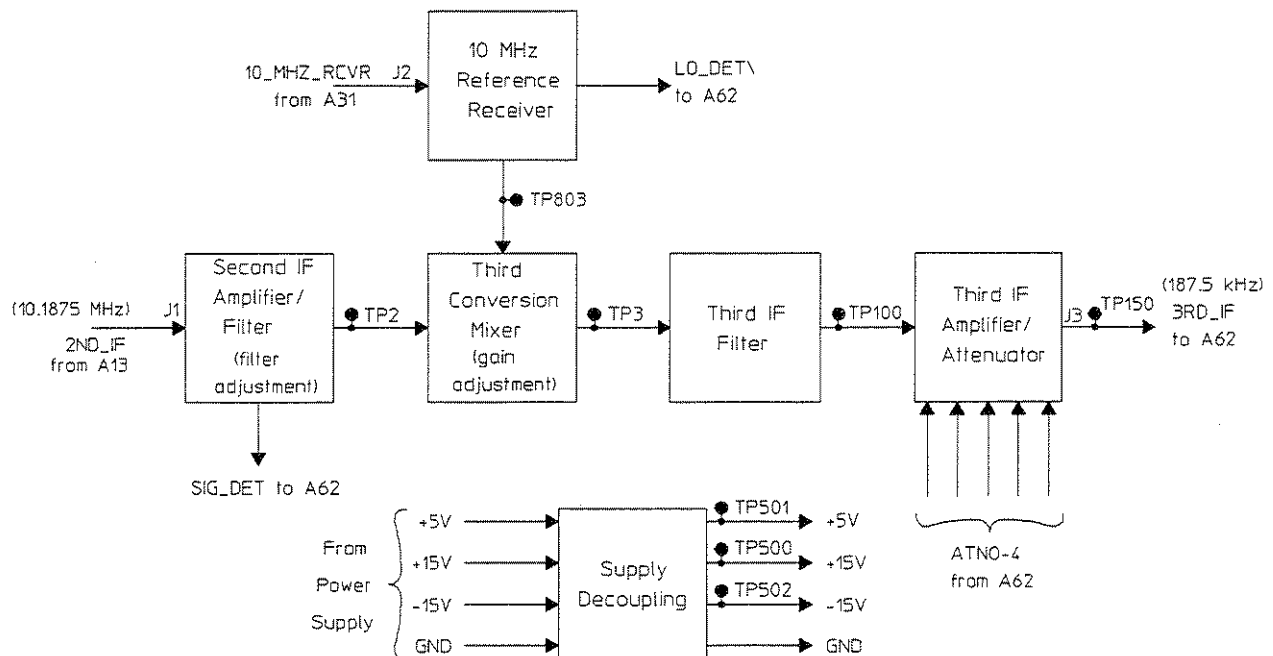


Figure 4-24. A61 IF Block Diagram

A62 ADC/Digital Filter

The ADC/Digital Filter assembly is the last of five assemblies to condition the input signal. This assembly converts the output of the IF assembly to digital data. The digital data is then digitally filtered and detected, then sent to the CPU assembly over the fast bus. Figure 4-25 shows the ADC/Digital Filter assembly's block diagram.

The **Track and Hold** circuit holds a voltage sample of the 187.5 kHz IF signal for the period of time required by the ADC to digitize the voltage.

The **ADC** circuit converts the voltage to a 13-bit digital word at a 250 kHz sample rate. After a complete conversion cycle, the ADC serially transfers the digital word to the Digital Filter.

The ADC circuit converts the voltage to a 13-bit digital word by passing the signal through an 8-bit A/D converter twice. On the first pass, the voltage is divided by four, then level shifted. Then dither (noise) is added to increase the accuracy of the analog-to-digital conversion. The 8-bit A/D converter converts the voltage to an 8-bit digital word. This first-pass word is converted back to a voltage and compared with the original voltage. A difference voltage is generated and converted to an 8-bit word. The second-pass word is added to the first-pass word, resulting in a 13-bit digital word that represents the IF signal.

The ADC circuits contain three service adjustments — one to null dc offset, one to set the reference voltage, and one to match the gain between the two conversion passes.

The **Digital Filter** circuit digitally mixes the 13-bit word with a 62.5 kHz sine wave and a 62.5 kHz cosine wave. (The 62.5 kHz signals result from dividing the 250 kHz sample clock by four.) The result of this digital mixing is two data streams — one representing the real part of the IF signal and the other representing the imaginary part of the IF signal. This circuit also provides the final resolution bandwidth filtering for each data stream.

The **Detector** sends the data streams from the Digital Filter to the CPU assembly over the fast bus. The Detector also squares the output of both digital filters, adds the squared values together, and sends the result to the CPU assembly.

The **Reset Receivers** buffer the reset signal and the sweep synchronization signal. The reset signal (RESET) resets the ADC, Digital Filter, and Detector. The sweep synchronization signal (LSWP) resets the phase of the gate arrays in the Digital Filter and the Detector.

The **Sample Clock Receiver** buffers the 250 kHz reference signal and sends it to the ADC as the sample rate.

The **20 MHz Clock** divides the 80 MHz reference signal by four, creating two 20 MHz signals in quadrature (90 degree phase relationship). These signals provide the clock signals for the ADC, Digital Filter, Detector and the external clock signal for the CPU assembly. The external clock signal is sent to the CPU assembly over the fast bus. If this external clock signal is not present, the fast bus is disabled.

The **Fault Detection** circuit detects the presence of the 10 MHz reference and the input signal at the IF assembly. It also detects the presence of the 250 kHz reference and the 20 MHz clocks. This information is sent to the IIC Interface.

The **IIC Interface** provides the interface between the CPU assembly and the ADC/Digital Filter assembly. It also provides the interface between the CPU assembly and the IF assembly. If the 10 MHz reference, 250 kHz reference, or 20 MHz clock is not present, the IIC Interface interrupts the CPU assembly.

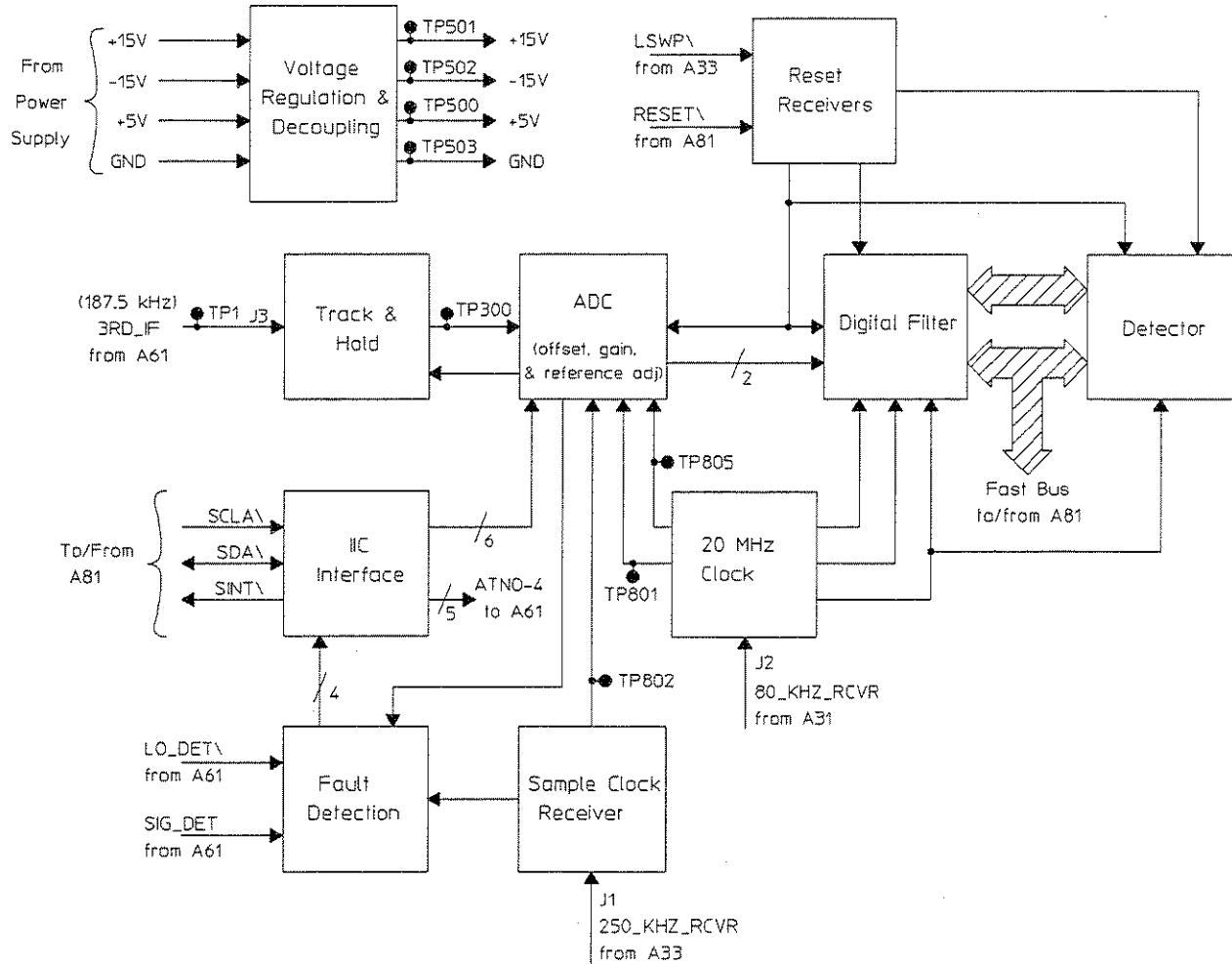


Figure 4-25. A62 ADC/Digital Filter Block Diagram

A81 CPU

The CPU assembly controls the entire analyzer. It performs multiple tasks, such as:

- Initiating the power-up sequence and calibration routines
- Capturing front panel keystrokes
- Configuring the measurement hardware
- Processing input data from the ADC/Digital Filter assembly
- Controlling the display
- Monitoring the hardware for faults or overloads
- Running the self tests
- Handling all data transfers for the fast bus, HP-IB, and Disk Drive assembly

Figure 4-26 shows the CPU assembly's block diagram. Figure 4-27 shows the CPU interface's block diagram.

The **MPU (Microprocessor)** controls the processor address bus and the buffered processor data bus. At power-up, this circuit initializes the analyzer from the information stored in the Monitor ROM. This circuit also processes interrupts from the Interrupt Handler and synchronizes data transfers on the processor data bus with the Data Transfer Handler. The MPU also has access to battery-backed-up SRAM on the Memory assembly. This allows the CPU assembly to store and update information such as the analyzer's address, default disk, and peripheral addresses.

The **DMA (Direct Memory Access) Controller** handles all DMA data transfers and controls the fast bus that connects the ADC/Digital Filter assembly to the CPU assembly. When a DMA data transfer occurs, the DMA Controller circuit takes control of the processor address and data busses. When the DMA data transfer is finished, the DMA Controller returns control of the busses to the MPU. Throughput from the ADC/Digital Filter assembly to the Memory assembly or to the Disk Drive assembly are examples of DMA data transfers.

The **TMS320** relieves the MPU of math intensive-tasks by supplying the computational power needed for accurate, high-speed signal processing operations — for example, windowing and Fast Fourier Transform (FFT) for the analyzer's narrow-band zoom mode. The TMS320 is a high speed (40 MHz) math co-processor that performs complex mathematical operations. It works as a slave co-processor to the MPU (68000), and it has its own Program RAM and Data RAM. This arrangement leaves the MPU free to perform other functions while the TMS320 performs math-intensive operations.

The **Interrupt Handler** processes interrupts for the MPU. It sets the interrupt priority level and returns an interrupt acknowledge to the circuit that generated the interrupt. If the MFP controller causes an interrupt, the MPU reads a status byte from the MFP controller to determine the circuit that caused the interrupt.

The **Data Transfer Handler** synchronizes data transfers in the analyzer with the MPU. When a data transfer occurs, the Data Transfer Handler notifies the MPU when the transfer is complete.

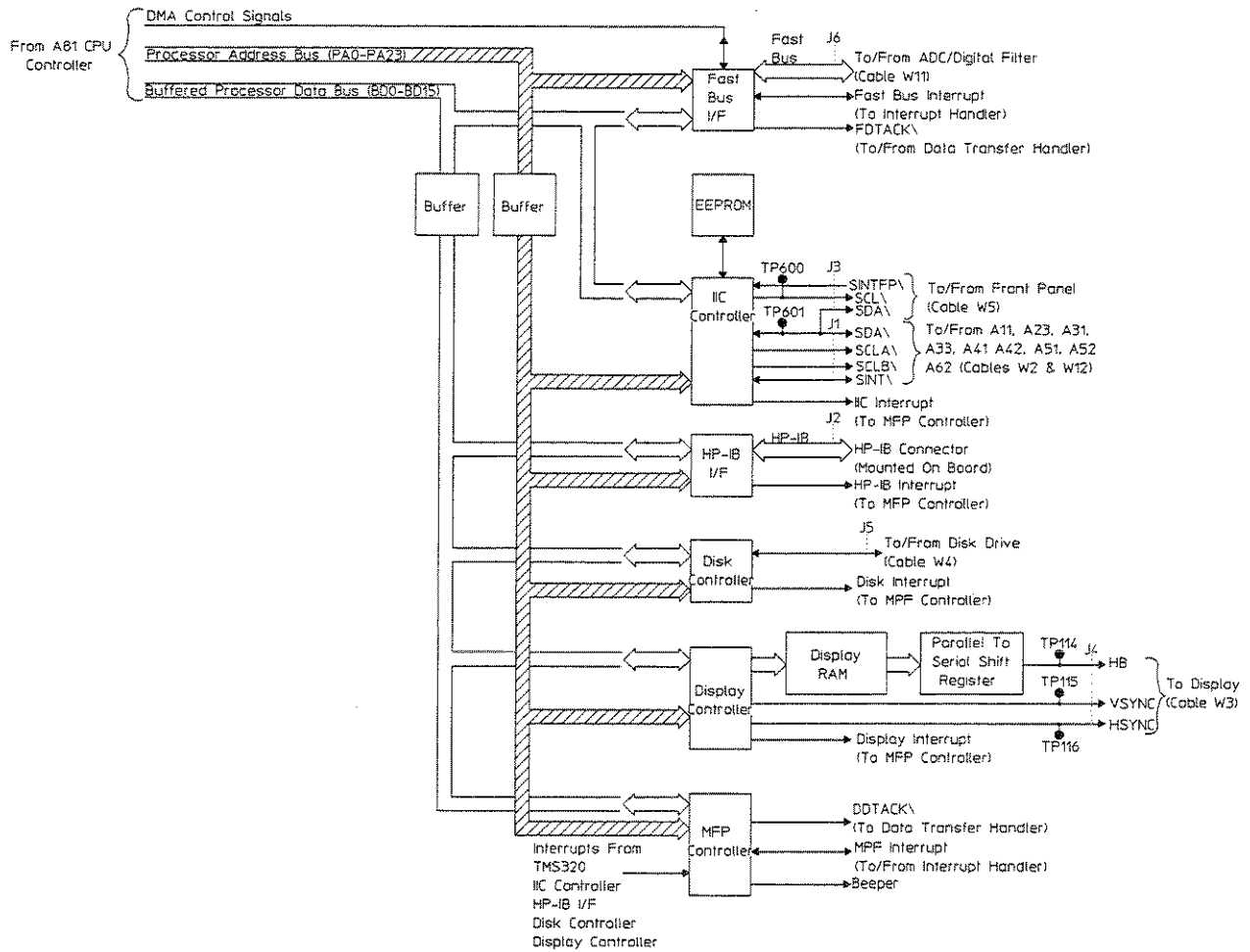


Figure 4-27. A81 CPU Interface Block Diagram

The **Clock Circuits** provide the clocks for the CPU, Disk Drive, and Memory assemblies. If the external clock from the ADC/Digital Filter assembly is present, this circuit synchronizes the CPU assembly with the rest of the analyzer.

The **MFP (Multiple-Function Peripheral) Controller** handles interrupts and handshaking during data transfers for the following circuits:

- TMS320
- IIC Controller
- HP-IB Interface
- Disk Controller
- Display Controller

Interrupts from these circuits are sent to the MFP Controller. When the MFP Controller receives an interrupt, it interrupts the Interrupt Handler, which in turn interrupts the MPU. The MPU then reads a status byte from the MFP Controller to determine the cause of the interrupt. The MFP Controller also tells the Data Transfer Handler if any data transfers occurred for these circuits.

The **Reset Logic** puts the analyzer into a known state (see figure 4-28). A reset occurs at power up (PVALID from the Power Supply assembly goes high), when the reset switch SW101 (located on the CPU assembly) is pressed, or when the MPU receives a reset instruction.

A low-to-high transition on pin 18 of the MPU causes the MPU to execute its reset routine (stored in ROM). When the MPU completes its reset routine, it forces RST\ high (notice that pin 18, RST\, of the MPU is bidirectional). This in turn forces RESET\ high, which tells the other assemblies that the reset routine is finished.

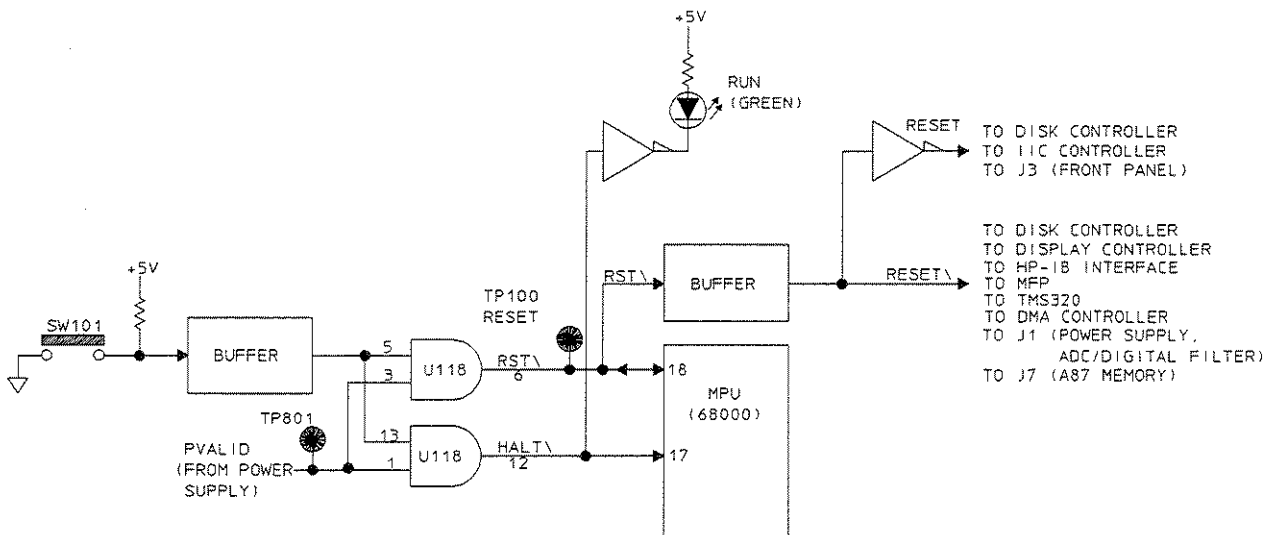


Figure 4-28. Reset Logic

The **Fast Bus Interface** connects the CPU assembly to the fast bus. All data transfers between the ADC/Digital Filter assembly and the CPU assembly occur over the fast bus. The fast-bus address lines (FA0 through FA5) and data lines (FD0 through FD15) are simply extensions of the processor address and data busses. This allows fast DMA transfers between the two assemblies. See “W11 Fast Bus Cable Signals” (later in this section) for a description of the fast bus signals.

The **IIC (Inter-IC) Controller** manages the IIC bus. It allows direct communication between the CPU assembly and the following assemblies via the IIC bus:

- Front Panel
- Input
- Step Phase Detector
- Reference/Calibrator
- Trigger
- Source Amplifier
- Source Conversion
- Interpolation VCO
- Fractional-N
- ADC/Digital Filter
- Memory

All of these assemblies appear as slaves to the IIC Controller. The IIC Controller has access to an EEPROM, which allows the CPU assembly to store information such as the analyzer’s serial number and IBASIC option. If the CPU assembly is replaced, the analyzer’s serial number and IBASIC option must be stored in EEPROM on the new assembly (see “Replacing CPU Assembly” in section II). The IIC Controller also has access to a battery backed real-time clock on the Memory assembly.

The IIC bus consists of the following six signal lines:

- SCL\ (serial clock)
- SCLA\ (serial clock)
- SCLB\ (serial clock)
- SDA\ (serial data)
- SINT\ (serial interrupt)
- SINTFP\ (serial interrupt for Front Panel assembly)

Pull-up resistors connect these signals to logic high (all six lines are open collector or open drain). See “W5 Front Panel Cable Signals” and “W12 Motherboard Power Cable Signals” (later in this section) for descriptions of the IIC signals.

The **HP-IB Interface** allows the analyzer to communicate with other devices such as plotters, printers, or a host computer via an HP-IB cable. This circuit handles all HP-IB functions for the analyzer. The analyzer’s HP-IB connector is located on the CPU assembly.

The **Disk Controller** allows the analyzer to store or retrieve data from the optional internal 3.5-inch flexible Disk Drive assembly. It provides all the control signals necessary to operate the Disk Drive assembly. The Disk Controller performs the following functions:

- Turns on the disk drive motor
- Selects the disk drive head
- Turns on the disk drive LED
- Selects a track on the flexible disk
- Writes or reads serial data from the flexible disk

The Disk Controller puts data on the flexible disk in a bit stream that consists of data and clock bits. When data is read from the disk, this circuit separates the data bits from the clock bits, converts the serial data bits to an 8-bit parallel word, and puts the data word on the processor data bus. The operation is reversed when data is written to the disk.

The **Display Controller** positions information on the analyzer's display. The Display Controller takes parallel data from the processor data bus and places the data in display RAM (four 64K × 4-bit RAM chips). One bit in display RAM corresponds to one pixel on the display. The data in display RAM is then sent to a parallel-to-serial shift register. The shift register continuously updates the display with the contents of display RAM. The Display Controller also supplies the horizontal and vertical sync signals for the display, and it determines if the data on the display is full bright or half bright.

A87 Memory and A88 Expanded Memory

The Memory assembly provides the CPU assembly with ROM, dynamic RAM, static RAM, and a real-time clock (see figure 4-29). The Memory assembly also provides battery backup for the static RAM and real-time clock. Memory is divided into 16-bit words. To access a memory location, the CPU assembly puts the address of the desired 16-bit word on the processor address bus. The CPU assembly can then read from (or write to) this memory location.

The optional Expanded Memory assembly replaces the Memory assembly, plus provides an additional two megabytes of RAM.

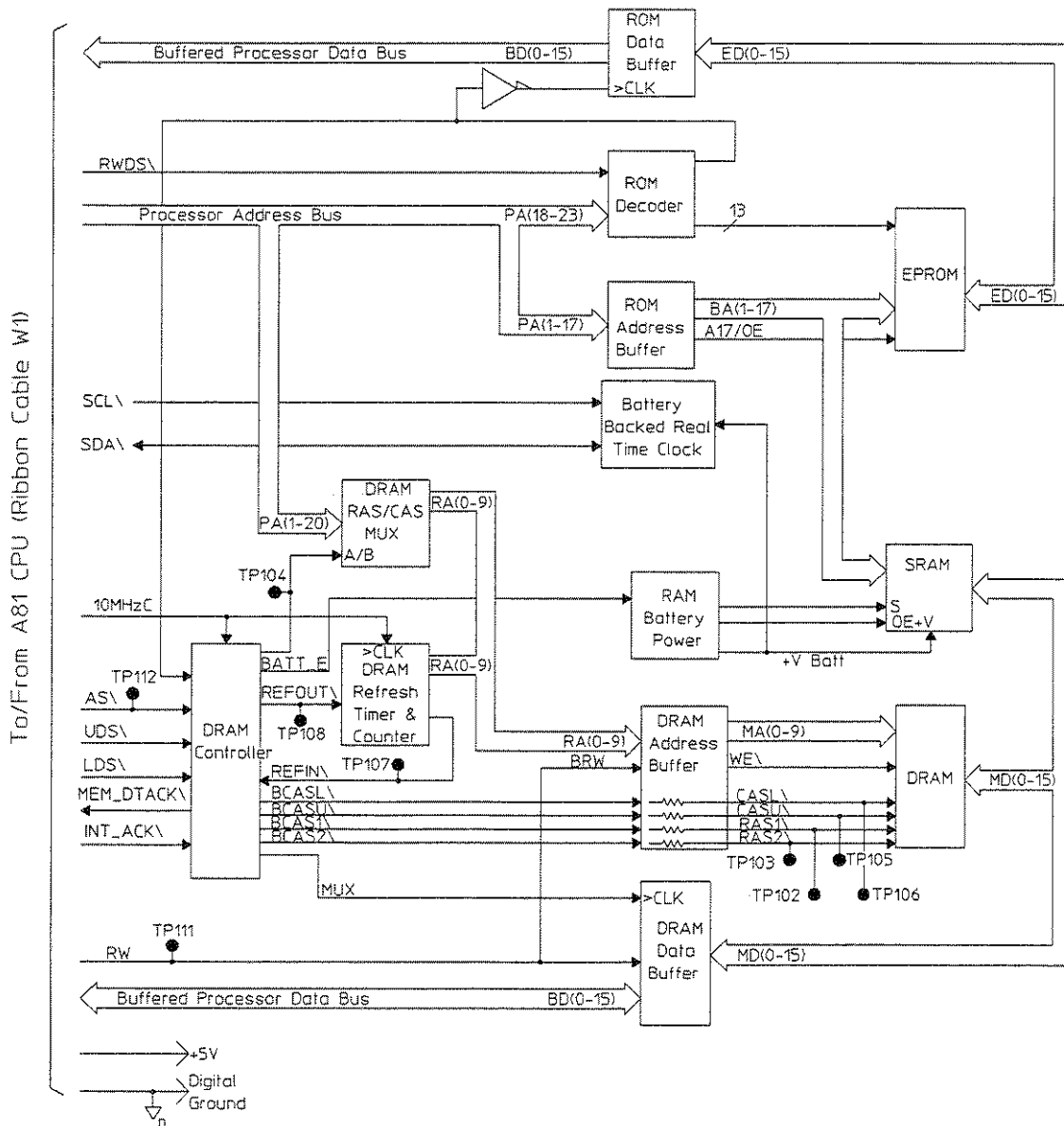


Figure 4-29. Memory and Expanded Memory Block Diagram

A90 Fan Power and A91 Fan Power/Oven

The Fan Power assembly provides power to the fan, which cools the card-nest side of the analyzer.

The optional Fan Power/Oven assembly provides power to the fan, which cools the card-nest side of the analyzer, and provides a stable 10 MHz frequency reference to the rear panel (OVEN REF OUT). During the oven warm-up cycle, oven reference output is disabled and the analyzer uses its internal crystal reference. When the oven reaches the proper operating temperature (about 10 minutes after power-up), oven reference output is automatically enabled. A BNC-to-BNC jumper connects the OVEN REF OUT connector to the EXT REF IN connector on the rear panel.

A99 Motherboard

The Motherboard assembly provides a common point of contact for voltage and signal distribution. This assembly filters some voltages and signals, and also provides power for the active probe connector on the front panel (+15V and -13V, derived from the analyzer's $\pm 15V$ supply). See "Motherboard Signals" (later in this section) for a list of all signals that are distributed via the Motherboard assembly.

Front Panel

The Front Panel assembly sends information to the analyzer. This assembly consists of all the keys on the instrument's front panel (except for the power switch), the RPG, and an IIC interface. When a front panel key is pressed or the RPG is turned, the IIC interface interrupts the CPU assembly. The CPU assembly then addresses the IIC interface and reads an 8-bit frame of data from the IIC bus to determine which key was pressed (for information about the IIC bus, see the description of the IIC Controller in the "CPU Assembly" earlier in this section).

Power Supply

The Power Supply assembly is a switching power supply that provides the voltages for all the assemblies in the analyzer. See “Voltage and Signal Distribution” (later in this section) for a list of these voltages and the assemblies that use each voltage.

Disk Drive

The optional internal Disk Drive assembly stores and retrieves information from 3.5-inch flexible disks. This assembly is mounted on (and controlled by) the CPU assembly. See the description of the Disk Controller in the “CPU Assembly” (earlier in this section) for further details.

Display

The Display assembly shows processed data sent by the CPU assembly. See the description of the Display Controller for the “CPU Assembly” (earlier in this section) for further details.

Voltage and Signal Distribution

This section shows where the signals and voltages are used in the analyzer. See figure 4-30 for assembly locations, and figure 4-31 for ribbon cable connections.

Assemblies

- | | |
|--------------------------|------------------------|
| A11 Input | A42 Source Conversion |
| A12 First Conversion | A51 Interpolation VCO |
| A13 Second Conversion | A52 Fractional-N |
| A21 Sum VCO | A61 IF |
| A22 Sum Phase Detector | A62 ADC/Digital Filter |
| A23 Step Phase Detector | A81 CPU |
| A24 Step VCO | A87 Memory |
| A31 Reference/Calibrator | A88 Expanded Memory |
| A32 300 MHz | A90 Fan Power |
| A33 Trigger | A91 Fan Power/Oven |
| A41 Source Amplifier | A99 Motherboard |

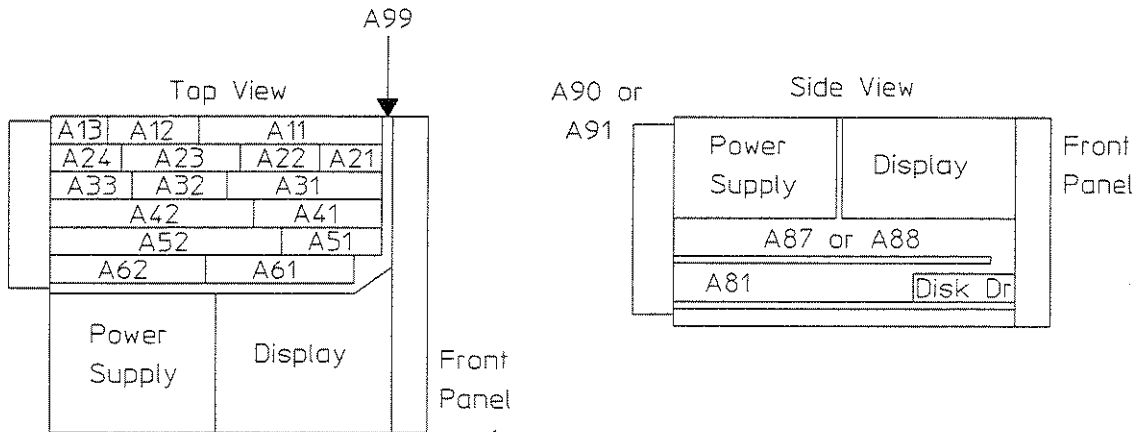


Figure 4-30. Assembly Locations

Cables

- W1 Memory
- W2 CPU Power
- W3 Display
- W4 Disk Drive
- W5 Front Panel
- W11 Fast Bus
- W12 Motherboard Power

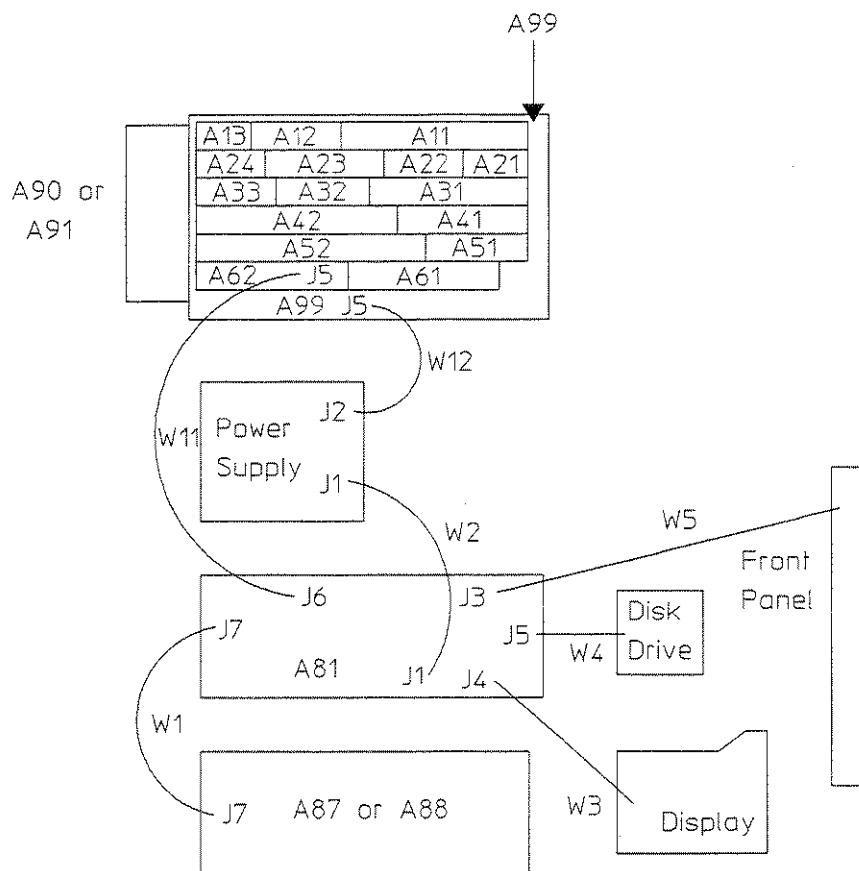


Figure 4-31. Ribbon Cable Connections

Note

Signals with a mnemonic that ends with a “\” are active low.

Table 4-2 shows the power supply voltages used by each assembly in the analyzer. In addition, the table also shows the path taken by these voltages and the location of individual test points. Some assemblies use the power supply voltages as supplied by the Power Supply assembly. However, most assemblies contain voltage regulation and voltage decoupling circuits to provide additional regulation and decoupling for their own use.

Table 4-2. Power Supply Voltage Distribution

| From | Path | To | Voltages | | | | | | | |
|---------------|-----------|-------------|----------|-------|------|-------|-------|-------|------|-------|
| | | | +18V | +15V | +12V | +8V | +5V | -15V | -18V | Gnd |
| Pwr Supply J1 | W2 | A81 J1 | | | ✓ | | TP102 | | ✓ | TP101 |
| | W2/A81/W1 | A87/A88 J7 | | | | | TP100 | | | TP101 |
| | W2/A81/W3 | Display | | | ✓ | | ✓ | | | ✓ |
| | W2/A81/W4 | Disk Drive | | | ✓ | | ✓ | | | ✓ |
| | W2/A81/W5 | Front Panel | | | | | ✓ | | | ✓ |
| Pwr Supply J2 | W12 | A99 J5 | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ |
| | W12/A99 | A11 J5 | | TP202 | | | TP201 | TP203 | | TP200 |
| | | A12 J4 | | TP803 | | TP802 | TP801 | TP804 | | TP800 |
| | | A13 J4 | | TP901 | | TP900 | | | | TP903 |
| | | A21 J100 | | ✓ | | ✓ | | ✓ | | ✓ |
| | | A22 J100 | | ✓ | | ✓ | | ✓ | | ✓ |
| | | A23 J100 | | TP907 | | ✓ | TP903 | TP909 | | TP900 |
| | | A24 J100 | | ✓ | | ✓ | | ✓ | | ✓ |
| | | A31 J10 | ✓ | ✓ | | ✓ | ✓ | | ✓ | ✓ |
| | | A32 J32 | ✓ | | | ✓ | ✓ | | ✓ | ✓ |
| | | A33 J7 | | ✓ | | ✓ | ✓ | ✓ | | ✓ |
| | | A41 J41 | | TP560 | | | TP561 | TP562 | | TP551 |
| | | A42 J42 | | TP550 | | TP558 | TP552 | TP553 | | TP559 |
| | | A51 J5 | ✓ | | | ✓ | | | ✓ | TP504 |
| | | A52 J3 | ✓ | | | ✓ | ✓ | | ✓ | TP106 |
| | | A61 J4 | | TP500 | | | TP501 | TP502 | | ✓ |
| | | A62 J4 | | TP501 | | | TP500 | TP502 | | TP504 |
| A90/91 J3 | | | | | | | ✓ | ✓ | | |
| A91 J2 | ✓ | | | | | | ✓ | ✓ | | |
| Probe Power | | ✓ | | | | | ✓ † | ✓ | | |

† A circuit on the Motherboard assembly reduces this voltage to -13V.

Table 4-3 lists the pin numbers of the voltages and signals at the power supply connectors, J1 (connects to CPU) and J2 (connects to Motherboard). For a description of these signals, see “W2 CPU Power Cable Signals” and “W12 Motherboard Power Cable Signals” later in this section. For voltage tolerances and troubleshooting information, see “Initial Verification” in section V, “Service.”

Table 4-3. Power Supply Connectors J1 and J2

| Signal Name | J1 Pin(s) | J2 Pin(s) |
|-------------|-----------------|---|
| PSSD\ | — | 50 |
| LSWP\† | — | 37 |
| BFREQ_REF | 3 | — |
| PVALID | 13 | — |
| SDA\‡ | 15 | 11 |
| SCLB\‡ | 17 | 9 |
| SCLA\‡ | 19 | 7 |
| RESET\‡ | 21 | 5 |
| SINT\‡ | 23 | 3 |
| GETTRIG‡ | 25 | 1 |
| +5V | 5-10 | 15-20 |
| +8V | — | 45-49 |
| +12V | 1,2,4 | — |
| +15V | — | 41, 42 |
| -15V | — | 27, 29 |
| +18V | — | 33 |
| -18V | 26 | 23 |
| Gnd | 11,12-24 (even) | 2-12 (even), 13, 14, 21, 22, 24-26, 28, 30-32, 34-36, 38-40, 43, 44 |

† This signal is not used by the Power Supply assembly.

‡ This signal passes directly from J1 to J2 and is not used by the Power Supply assembly.

Tables 4-4 through 4-10 list signals routed through ribbon cables. These tables show several things — which assembly generates each signal, which assemblies use the signals, if a signal is bidirectional, and if a signal is not connected to an assembly.

Table 4-4. Memory Cable

| Signal Name | Pin(s) | A81J7 | A87/A88 J7 |
|-------------|-----------------------------|-------|------------|
| PA1 — PA23 | 1-23 | S | ● |
| BDO — BD15 | 25-40 | ↔ | ↔ |
| UDS\ | 44 | S | ● |
| LDS\ | 46 | S | ● |
| AS\ | 48 | S | ● |
| INT_ACK\ | 50 | S | ● |
| RW | 52 | S | ● |
| MEM_DTACK\ | 54 | ● | S |
| RWDS\ | 56 | S | ● |
| AS_DEL | 58 | S | ● |
| 10MHZ | 60 | S | ● |
| SCL\ | 62 | S | ● |
| SDA\ | 64 | S | ● |
| +5V | 42,45,49,53,57,61 | ● | ● |
| Gnd | 24,41,43,47,51,55, 59,63 | ● | ● |

- S This assembly is the source of the signal.
- This assembly uses the signal.
- ↔ This signal is bidirectional.
- This assembly does not use this signal.

Table 4-5. W2 CPU Power Cable

| Signal Name | Pin(s) | A81J1 | PwrJ1 |
|-------------|-----------------------------|-------|-------|
| BFREQ_REF | 3 | S | ● |
| PVALID | 13 | ● | S |
| SDA\ | 15 | ↔ | — |
| SCLB\ | 17 | S | — |
| SCLA\ | 19 | S | — |
| RESET\ | 21 | S | — |
| SINT\ | 23 | ● | — |
| GETTRIG | 25 | S | — |
| +5V | 5-10 | ● | S |
| +12V | 1,2,4 | ● | S |
| -18V | 26 | ● | S |
| Gnd | 11,12,14,16,18,20, 22,24 | ● | ● |

- S This assembly is the source of the signal.
- This assembly uses the signal.
- ↔ This signal is bidirectional.
- This assembly does not use this signal.

Table 4-6. W3 Display Cable

| Signal Name | Pin(s) | A81J4 | Display |
|-------------|----------------|-------|---------|
| HSYNC | 5 | S | ● |
| VSYNC | 7 | S | ● |
| HB | 13 | S | ● |
| FB | 15 | S | ● |
| +12V | 9,11 | ● | ● |
| +5V | 10 | ● | ● |
| Gnd | 4,6,8,12,14,16 | ● | ● |
| Not Used | 1-3 | — | — |

- S This assembly is the source of the signal.
- This assembly uses the signal.
- ↔ This signal is bidirectional.
- This assembly does not use this signal.

Table 4-7. W4 Disk Drive Cable

| Signal Name | Pin(s) | A81J5 | Disk Drive |
|---|--------------------------|-------|------------|
| DCR\ | 1 | S | ● |
| DISK_CHANGE\ IN_USE\ | 2 | ● | S |
| DRIVE_SELECT_3 | 4 | S | ● |
| INDEX\ DRIVE_SELECT_0 | 6 | S | ● |
| DRIVE_SELECT_1 | 8 | ● | S |
| DISK_IN\ DRIVE_SELECT_2 | 10 | S | ● |
| MOTOR_ON\ DIRECTION | 12 | S | ● |
| STEP\ WRITE_DATA\ WRITE_GATE\ TOO\ WRITE_PROT\ READ_DATA\ HEAD_SELECT | 13 | ● | S |
| DISK_READY\ +5V +12V | 14 | S | ● |
| Gnd | 16 | S | ● |
| | 18 | S | ● |
| | 20 | S | ● |
| | 22 | S | ● |
| | 24 | S | ● |
| | 26 | ● | S |
| | 28 | ● | S |
| | 30 | ● | S |
| | 32 | S | ● |
| | 34 | ● | S |
| | 3,5,7,9,11 | ● | ● |
| | 29,31,33 | ● | ● |
| | 15,17,19,21,23,25, 27 | ● | ● |

- S This assembly is the source of the signal.
- This assembly uses the signal.
- ↔ This signal is bidirectional.
- This assembly does not use this signal.

Table 4-8. W5 Front Panel Cable

| Signal Name | Pin(s) | A81J3 | Front Panel |
|-------------|--------------|-------|-------------|
| RESET | 5 | S | ● |
| SINTFP\ | 7 | ● | S |
| SDA\ | 13 | ↔ | ↔ |
| SCL\ | 15 | S | ● |
| +5V | 10 | ● | ● |
| Gnd | 6,8,12,14,16 | ● | ● |
| Not Used | 1,2,3,4,9,11 | — | — |

- S This assembly is the source of the signal.
- This assembly uses the signal.
- ↔ This signal is bidirectional.
- This assembly does not use this signal.

Table 4-9. W11 Fast Bus Cable

| Signal Name | Pin(s) | A81J6 | A62J5 |
|-------------|-------------|-------|-------|
| FD0 — FD15 | 1-31 (odd) | ↔ | ↔ |
| FA1 — FA5 | 33-41 (odd) | S | ● |
| FIRQ\ | 43 | ● | S |
| FRW | 45 | S | ● |
| SELA\ | 47 | S | ● |
| SELS\ | 49 | S | ● |
| FDTACK\ | 51 | ● | S |
| ECLK | 53 | S | — |
| REQO\ | 55 | ● | S |
| ACKO\ | 57 | S | ● |
| PCL0\ | 59 | ● | S |
| DTC\ | 61 | ● | S |
| EXT_CLK | 63 | ● | S |
| Gnd | 2-64 (even) | ● | ● |

- S This assembly is the source of the signal.
- This assembly uses the signal.
- ↔ This signal is bidirectional.
- This assembly does not use this signal.

Table 4-10. W12 Motherboard Power Cable

| Signal Name | PWRJ2 Pin(s) | Power Supply | A99J5 Pin(s) | Motherboard |
|---|---|--|---|--|
| PSSD\ LSWP\ SDA\ SCLB\ SCLA\ RESET\ SINT\ GETTRIG +8V +15V +18V -15V -18V +5V Gnd | 50 37 11 9 7 5 3 1 45-49 41, 42 33 27, 29 23 15-20 2-12(even), 13, 14, 21, 22, 24-26, 28, 30-32, 34-36, 38-40, 43, 44 | ● — — — — — — — S S S S S S S S | 1 14 40 42 44 46 48 50 2-6 9,10 18 22, 24 28 31-36 7, 8, 11-13, 15-17, 19-21, 23, 25-27, 29, 30, 37, 38, 39-49(odd) | S S ↔ ● ● ● S ● ● ● ● ● ● ● ● ● |

- S This assembly is the source of the signal.
- This assembly uses the signal.
- ↔ This signal is bidirectional.
- This assembly does not use this signal.

Table 4-11 lists all signals routed through RF cables. The table shows where the cables are connected and which assembly generates the signal.

Table 4-12 lists all signals routed through the Motherboard. The table shows the first place a signal appears or could appear on the Motherboard.

Table 4-13 lists voltages routed through the Motherboard (see table 4-2 for a complete list of assemblies using each voltage).

Table 4-14 lists signals at the HP-IB connector (A81 J2).

Table 4-11. RF Cables †

| Signal Name | Assembly & Connectors | | | | | | | | | | | | | | | | Cable Color | |
|----------------|-----------------------|-----------|-----------|-----------|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----|-----------|-----|-------------------|------------|
| | A11 | A12 | A13 | A21 | A22 | A23 | A24 | A31 | A32 | A33 | A41 | A42 | A51 | A52 | A61 | A62 | | Rear Panel |
| 100_KHZ_REF | | | | | | | | | | J4 | | | | J2 | | | | red |
| 187.5_KHZ_SRCE | | | | | | | | | | J2 | | J6 | | | | | | red |
| 250_KHZ_RCVR | | | | | | | | | | J3 | | | | | | J1 | | orange |
| 10_MHZ_RCVR | | | | | | | | J3 | | | | | | | J2 | | | yellow |
| 10_MHZ_REF | | | | | | J3 | | J4 | | | | | | | | | | blue |
| 10_MHZ_SRCE | | | | | | | | J5 | | | | J4 | | | | | | green |
| 20_MHZ | | | | | | | | J9 | J1 | | | | | | | | | red |
| 60_MHZ | | | | | | | | | J2 | J1 | | | | | | | | orange |
| 80_MHZ_RCVR | | | | | | | | J8 | | | | | | | | J2 | | green |
| 300_MHZ_RCVR | | | J1 | | | | | | J5 | | | | | | | | | orange |
| 300_MHZ_REF | | | | | | J2 | | | J4 | | | | | | | | | red |
| 300_MHZ_SRCE | | | | | | | | | J3 | | | J3 | | | | | | red |
| 1ST_IF | | J3 | J2 | | | | | | | | | | | | | | | red |
| 2ND_IF | | | J3 | | | | | | | | | | | | J1 | | | lt blue |
| 3RD_IF | | | | | | | | | | | | | | | J3 | J3 | | white |
| CAL | J2 | | | | | | | J1 | | | | | | | | | | red |
| CAL_SRCE | | | | | | | | J2 | | | J2 | | | | | | | red |
| EXT_REF_IN | | | | | | | | J7 | | | | | | | | | EXT REF IN | blue |
| EXT_TRIG | | | | | | | | | | J6 | | | | | | | EXT TRIG | black |
| F/N_VCO | | | | | | | | | | | | | J3 | J1 | | | | orange |
| INPUT_OUT | J3 | J2 | | | | | | | | | | | | | | | | black |
| INTRPL_VCO | | | | | J3 | | | | | | | | J1 | | | | | white |
| NORMALIZE | J1 | | | | | | | | | | J1 | | | | | | | orange |
| REF_OUT | | | | | | | | J6 | | | | | | | | | REF OUT | lt green |
| SL_VCO | | | | J1 | | | | | | | | | J2 | | | | | orange |
| SRCE_AMP | | | | | | | | | | | J3 | J1 | | | | | | red |
| STEP_TO_SUM | | | | | J2 | | J1 | | | | | | | | | | | blue |
| STEP_VCO | | | | | | J1 | J3 | | | | | | | | | | | blue |
| SUM_VCO | | | | J4 | J1 | | | | | | | | | | | | | red |
| SWEPT_LO_RCVR | | J1 | | J3 | | | | | | | | | | | | | | gray |
| SWEPT_LO_SRCE | | | | J2 | | | | | | | | J2 | | | | | | blue |
| TRIG_OUT | | | | | | | | | | J5 | | | | | | | TRIG OUT | white |

† The signal source is shown in boldface type.

Table 4-12. Motherboard Signals †

| Signal Name | Assembly Using Signal | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------------|-----------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|------------|--|--|--|--|----|------------|----|------------|----|------------|
| | PWR | A11 | A12 | A21 | A22 | A23 | A24 | A31 | A32 | A33 | A41 | A42 | A51 | A52 | A61 | A62 | | | | | | | | | | | | |
| | Motherboard Connector | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | J5 | J11 | J12 | J21 | J22 | J23 | J24 | J31 | J32 | J33 | J41 | J42 | J51 | J52 | J61 | J62 | | | | | | | | | | | | |
| Connector Pin Number | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 187.5_SIG\ ATN0 ATN1 | | | | | | | | | | | | | | | | | 1A | 16A | | | | | 1A | 16A | | | | |
| ATN2 ATN3 ATN4 | | | | | | | | | | | | | | | | | | | | | | | 1C | 16C | 2A | 15A | 2B | 15B |
| CAL_ON CV_FRACN CV_ML | | | | | | | | | | | | | | | | | | | | | | | 2A | 15A | 1B | 16B | | |
| CV_SL CV_STEP GETTRIG | | | | | | | | | | | | | | | | | | | | | | | | | | 16A | | |
| HFU\ INC_IMAG INC_REAL | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LO_DET\ LSWP\ ML/SL | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PRETUNE PSSD\ RESET | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SCLA\ SCLB\ SDA | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SIG_DET SINT\ SLF | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SPEED_UP SRCE_ON SUM_OOL_H | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SUM_OOL_L THRESH_LO UP_DN | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

† The first place on the Motherboard that the signal appears (or could appear) is shown in boldface type.

Table 4-13. Motherboard Voltages

| Voltage | Assembly Using Voltage | | | | | | | | | | | | | | | | | | | | | |
|------------------------------------|--|--|-------------|-------------|--------|--------|--|-------------|-------------|-------------|-------------|--|--|--|--|--|--|--|--|--|-----|-----|
| | PWR | A11 | A12 | A13 | A21 | A22 | A23 | A24 | A31 | A32 | A33 | A41 | A42 | A51 | A52 | A61 | A62 | A90/91 | P PWR | | | |
| | Motherboard Connector | | | | | | | | | | | | | | | | | | | | | |
| | J5 | J11 | J12 | J13 | J21 | J22 | J23 | J24 | J31 | J32 | J33 | J41 | J42 | J51 | J52 | J61 | J62 | W1 | W2 | | | |
| Connector Pin Number or Wire Color | | | | | | | | | | | | | | | | | | | | | | |
| +18V | 18 | | | | | | | | 1 | 1 | | | | 7A 7B 7C | 7A 7B 7C | | | | Red | | | |
| +15V | 9 10 | 4A 4B 4C | 1 | 1 | 1 | 1 | 4A 4B 4C | 1 | 3 | | 1 | 4A 4B 4C | 4A 4B 4C | | | 4A 4B 4C | 4A 4B 4C | | | Red | | |
| +8V | 2-6 | | 5 6 | 5 6 | 5 6 | 5 6 | 10A 10B 10C | 5 6 | 5 6 | 5 6 | 5 6 | | 10A 10B 10C | 10A 10B 10C | 10A 10B 10C | | | | | | | |
| +5V | 31- 36 | 12A 12B 12C | 10 | | | | 12A 12B 12C | | 10 | 10 | 10 | 12A 12B 12C | 12A 12B 12C | | 12A 12B 12C | 12A 12B 12C | 12A 12B 12C | | | | | |
| -15V | 22 24 | 5A 5B 5C | 2 | | 2 | 2 | 5A 5B 5C | 2 | | | 2 | 5A 5B 5C | 5A 5B 5C | | | 5A 5B 5C | 5A 5B 5C | | | Yel† | | |
| -18V | 28 | | | | | | | | 2 | 2 | | | | 8A 8B 8C | 8A 8B 8C | | | | | Yel | | |
| Gnd | 7-8 11- 13 15- 17 19- 21 23 25- 27 29 30 37- 39 41 43 45 47 49 | 6A 6B 6C 9A 9B 9C 11A 11B 11C 13A 13B 13C | 4 7 9 | 4 7 9 | 4 9 | 4 | 3A 3B 3C 6A 6B 6C 9A 9B 9C 11A 11B 11C 13A 13B 13C | 4 7 9 | 4 7 7 | 4 7 7 | 4 7 7 | 6A 6B 6C 9A 9B 9C 11A 11B 11C 13A 13B 13C | 6A 6B 6C 9A 9B 9C 11A 11B 11C 13A 13B 13C | 1A 1C 2A 2B 2C 3A 3C 6A 6B 6C 9A 9B 9C 11A 11B 11C 13A 13B 13C | 6A 6B 6C 9A 9B 9C 11A 11B 11C 13A 13B 13C | 6A 6B 6C 9A 9B 9C 11A 11B 11C 13A 13B 13C | 6A 6B 6C 9A 9B 9C 11A 11B 11C 13A 13B 13C | 6A 6B 6C 9A 9B 9C 11A 11B 11C 13A 13B 13C | 6A 6B 6C 9A 9B 9C 11A 11B 11C 13A 13B 13C | 6A 6B 6C 9A 9B 9C 11A 11B 11C 13A 13B 13C | Blk | Blk |

† A circuit on the Motherboard reduces this voltage to -13V before it is routed to the front panel for probe power.

Table 4-14. HP-IB Connector (A81 J2)

| Signal Name | Pin | Signal Name | Pin |
|--------------------|------------|--------------------|------------|
| DIO1 | 1 | DIO5 | 13 |
| DIO2 | 2 | DIO6 | 14 |
| DIO3 | 3 | DIO7 | 15 |
| DIO4 | 4 | DIO8 | 16 |
| EOI | 5 | REN | 17 |
| DAV | 6 | GND6 | 18 |
| NRFD | 7 | GND7 | 19 |
| NDAC | 8 | GND8 | 20 |
| IFC | 9 | GND9 | 21 |
| SRQ\ | 10 | GND10 | 22 |
| ATN | 11 | GND11 | 23 |
| Shield | 12 | Logic Gnd | 24 |

W1 Memory Cable Signals

Note

Signals with a mnemonic that ends with a “\” are active low.

| | |
|------------|---|
| 10MHZ | 10 MHz Clock — This is a 50% duty cycle, 10 MHz clock. It refreshes the dynamic RAM and synchronizes data transfers on the Memory assembly. |
| AS_DEL | Delayed Address Strobe — This is a delayed version of AS\ (Address Strobe). A high on this line generates a data transfer acknowledge for memory that requires 1 or more wait states. |
| AS\ | Address Strobe — This line pulses low when a valid address is on the processor address bus (PA1 — PA23). |
| BD0 — BD15 | Buffered Data Bus — This is the buffered processor data bus from the CPU assembly. It is further buffered on the Memory assembly. Most data transfers between the two assemblies occur on this bus. |
| INT_ACK\ | Interrupt Acknowledge — This line goes low when the CPU assembly receives an interrupt. A low on this line prevents the Memory assembly from starting another memory cycle. |
| LDS\ | Lower Data Strobe — During a write cycle, this line pulses low when valid data is on BD0 through BD7. During a read cycle, this line pulses low when data should be placed onto BD0 through BD7. |
| MEM_DTACK\ | Memory Data Transfer Acknowledge — This line pulses low after the Memory assembly places RAM or ROM data on the Buffered Data Bus. |
| PA1 — PA23 | Processor Address Bus — This is the processor address bus from the CPU assembly. It is buffered on the Memory assembly. |

- RW** Read/Write — This line is high when the current memory cycle is a read. It goes low when the current memory cycle is a write.
- RWDS** Read/Write & Data Strobe — A low on this line synchronizes access to ROM. This signal goes low during a read cycle when the upper or lower data strobe goes low.
- SCL** Serial Clock — This is the serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock to synchronize the transfer of data on the IIC bus.
- SDA** This is the IIC bus bidirectional data line. This line transmits real-time clock data between the CPU assembly and the Memory assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus.
- UDS** Upper Data Strobe — During a write cycle, this line goes low when data is valid on BD8 — BD15. During a read cycle, this line goes low when data should be placed onto BD8 — BD15.

W2 CPU Power Cable Signals

Note

GETTRIG, SCLA\, SCLB\, SINT\, SDA\, and RESET\ are not used by the Power Supply assembly. Instead, these signals are routed between the CPU assembly and the Motherboard assembly by the CPU power cable, the Power Supply assembly, and the motherboard power cable. LSWP\ is present on the motherboard power cable but is not used by either the Power Supply assembly or the CPU assembly.

| | |
|-----------|--|
| BFREQ_REF | Buffered Frequency Reference — This is a 50% duty cycle, 35.714 kHz clock generated by the CPU assembly to reduce noise and ripple from the Power Supply assembly. The Power Supply assembly phase locks its switching frequency to this clock. |
| GETTRIG | Group Execute Trigger — This is the group-execute trigger line from the HP-IB interface on the CPU assembly. When the analyzer is under HP-IB control, the Trigger assembly uses this line to trigger the analyzer. |
| PVALID | Power Valid — This line is high when the +5V supply from the Power Supply assembly is stabilized. |
| RESET\ | System Reset — A low on this line resets the digital logic on the ADC/Digital Filter assembly. This line pulses low during power-up and power-down, when the processor is externally reset, and when the processor executes the RESET instruction. |
| SCLA\ | Serial Clock A — This is a serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock to synchronize the transfer of data on the IIC bus. |
| SCLB\ | Serial Clock B — This is another serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock to synchronize the transfer of data on the IIC bus. |
| SDA\ | Serial Data — This is the IIC bus bidirectional data line. This line transmits data to or from the CPU assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus. |
| SINT\ | Serial Interrupt — This is the IIC bus interrupt line. A low on this line interrupts the CPU assembly. |

W3 Display Cable Signals

| | |
|-------|--|
| FB | Full Bright — A high on this line sets the Display assembly's electron beam to full bright. |
| HB | Half Bright — A high on this line sets the Display assembly's electron beam to half bright. |
| HSYNC | Horizontal Synchronization — A high on this line causes the Display assembly to do a horizontal retrace. |
| VSYNC | Vertical Synchronization — A high on this line causes the Display assembly to do a vertical retrace. |

W4 Disk Drive Cable Signals

| | |
|----------------------------|--|
| DCR\ | Disk Change Reset — A low on this line resets DISK_CHANGE\. This line goes low when DISK_READY\ is low. |
| DIRECTION | Direction — This line sets the direction for the disk head. A high on this line sets the direction away from the spindle. A low on this line sets the direction toward the spindle. |
| DISK_CHANGE\ | Disk Change — This line goes low when a flexible disk is removed from the Disk Drive assembly. This line remains low until a flexible disk is installed and either DCR\ or STEP\ goes low. |
| DISK_IN\ | Disk In — This line goes low when a flexible disk is inserted in the Disk Drive assembly. |
| DISK_READY\ | Disk Ready — This line goes low when a flexible disk is inserted and the index period of the disk motor is stable. A low on this line causes DCR\ to go low, which resets DISK_CHANGE\. |
| DRIVE_SELECT 0, 1, 2, 3 | Drive Select — A low on DRIVE_SELECT 0 selects the Disk Drive assembly. DRIVE_SELECT 0 is connected to ground and DRIVE_SELECT 1, 2 and 3 are connected to +5V. |

| | |
|-------------|--|
| HEAD_SELECT | Head Select — A low on this line selects the lower disk drive head. A high on this line selects the upper disk drive head. |
| INDEX\ | Index — This line pulses low with each revolution of the flexible disk. |
| IN_USE\ | In Use — A low on this line turns on the disk drive LED. This line is low during disk access. |
| MOTOR_ON\ | Motor On — A low on this line turns on the disk drive motor. This line goes low when a flexible disk is inserted. |
| READ_DATA\ | Read Data — This line pulses low for each bit detected on the flexible disk. |
| STEP\ | Step — A low on this line moves the disk drive head. When STEP\ and DIRECTION are low, the head moves toward the disk spindle. When STEP\ is low and DIRECTION is high, the head moves away from the disk spindle. |
| T00\ | Track 00 — This line is low when the head is positioned over track 0 on the flexible disk. |
| WRITE_DATA\ | Write Data — When WRITE_GATE\ is low, a low pulse on this line writes a bit to the disk. |
| WRITE_GATE\ | Write Gate — When this line is low, information may be written to the Disk Drive assembly under control of the WRITE_DATA\ line. |
| WRITE_PROT\ | Write Protect — This line is low when a write-protected disk is installed in the Disk Drive assembly. |

W5 Front Panel Cable Signals

| | |
|---------|---|
| RESET | System Reset — A high on this line resets the digital logic on the Front Panel assembly. This line pulses high during power-up and power-down, when the processor is externally reset, and when the processor executes the RESET instruction. |
| SCL\ | Serial Clock — This is the serial clock for the front panel IIC bus. The IIC controller on the CPU assembly generates this clock to synchronize the transfer of data from the Front Panel assembly. |
| SDA\ | Serial Data — This is the front panel IIC bus. When a front panel key is pressed or the RPG is turned, SINTFP\ interrupts the CPU assembly and this line transmits data to the CPU assembly in 8-bit frames. |
| SINTFP\ | Serial Interrupt from the Front Panel — A low on this line interrupts the CPU assembly. This line goes low when a front-panel key is pressed or when the RPG is turned. |

W11 Fast Bus Cable Signals

| | |
|-----------|--|
| ACK0\ | DMA Acknowledge — This line pulses low in response to a low on REQ0\ when the CPU assembly is ready for data. |
| DTC\ | Data Transfer Complete — This line goes low after the CPU assembly successfully reads the data from the ADC/Digital Filter assembly. When this line goes low, PCL0\ goes high to prevent the CPU assembly from trying another read cycle until the ADC/Digital Filter assembly is ready. |
| ECLK | Enable Clock — This is a 60% duty cycle, 1 MHz clock. The ADC/Digital Filter assembly does not use this clock or route it to any other assembly. |
| EXT_CLK | External Clock — This is a TTL level, 20 MHz clock that locks the system clock to the reference clock. It synchronizes the CPU assembly with the rest of the instrument. |
| FA1 — FA5 | Fast Bus Address Lines — These lines are a buffered form of the CPU assembly's processor address bus. The CPU assembly uses these lines to address different circuits on the ADC/Digital Filter assembly. |

| | |
|------------|--|
| FD0 — FD15 | Fast Bus Data Lines — These bidirectional data lines are an extension of the CPU assembly's buffered processor data bus. |
| FDTACK\ | Fast Bus Data Transfer Acknowledge — A low on this line terminates asynchronous bus cycles. |
| FIRQ\ | Fast Bus Interrupt Request — A low on this line interrupts the CPU assembly. |
| FRW | Fast Bus Read/Write — This line is high during a read cycle and low during a write cycle. This line is an extension of the read/write line (RW). |
| PCL0\ | DMA Programmable Control Line — This line goes low in response to a low on ACK0\ when the ADC/Digital Filter assembly is ready to send data. This line goes high when DTC\ goes low. |
| REQ0\ | DMA Request — This line goes low after the ADC/Digital Filter assembly collects a block of data and is ready to have the CPU assembly read the data. |
| SELA\ | Asynchronous Select — A low on this line enables asynchronous circuits on the ADC/Digital Filter assembly. |
| SELS\ | Synchronous Select — This line is low when a synchronous bus cycle is in operation. The ADC/Digital Filter assembly does not use this line or route it to any other assembly. |

W12 Motherboard Power Cable Signals

Note



GETTRIG, SCLA\, SCLB\, SINT\, SDA\, and RESET\ are not used by the Power Supply assembly. Instead, these signals are routed between the CPU assembly and Motherboard assembly by the CPU power cable, the Power Supply assembly, and the motherboard power cable.

| | |
|---------|---|
| GETTRIG | Group Execute Trigger — This is the group execute trigger line from the HP-IB interface on the CPU assembly. When the analyzer is under HP-IB control, the Trigger assembly uses this line to trigger the analyzer. |
| PSSD\ | Power Supply Shut Down — A short circuit to ground on this line forces all Power Supply output voltages to zero. This line is normally an open circuit, but becomes a short circuit to ground if the analyzer's internal temperature becomes excessive. |
| RESET\ | System Reset — A low on this line resets the digital logic on the ADC/Digital Filter assembly. This signal is pulsed low during power-up and power-down, when the processor is externally reset, and when the processor executes the RESET instruction. |
| SCLA\ | Serial Clock A — This is the serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock. This clock synchronizes the transfer of data on the IIC bus. |
| SCLB\ | Serial Clock B — This is another serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock. This clock synchronizes the transfer of data on the IIC bus. |
| SDA\ | Serial Data — This is the IIC bus bidirectional data line. This line transmits data to or from the CPU assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus. |
| SINT\ | Serial Interrupt — This is the IIC bus interrupt line. A low on this line interrupts the CPU assembly. |

RF Cable Signals

| | |
|----------------|--|
| 100_KHZ_REF | 100 kHz Reference — This is a 100 kHz, 1 Vp-p, approximate 1% duty cycle pulse. This signal provides a phase reference for the Fractional-N assembly. |
| 187.5_KHZ_SRCE | 187.5 kHz to Source — This is a 187.5 kHz, 600 mVp-p, ac-coupled square wave. The Source Conversion assembly mixes this signal with 10_MHZ_SRCE. |
| 250_KHZ_RCVR | 250 kHz to Receiver — This is a 250 kHz, TTL-level signal. The ADC on the ADC/Digital Filter assembly samples on the rising edge of this signal. |
| 10_MHZ_RCVR | 10 MHz to Receiver — This is a 10 MHz, -2 dBm, ac-coupled sine wave. The IF assembly mixes this signal with 2ND_IF. |
| 10_MHZ_REF | 10 MHz Reference — This is a 10 MHz, -2 dBm, ac-coupled sine wave. This signal is divided by 5 or 2, then used as a phase reference on the Step Phase Detector assembly. |
| 10_MHZ_SRCE | 10 MHz to Source — This is a 10 MHz, -2 dBm, ac-coupled sine wave. The Source Conversion assembly mixes this signal with 187.5_KHZ_SRCE. |
| 20_MHZ | 20 MHz — This is a 20 MHz, ECL level, ac-coupled square wave. This signal provides the 300 MHz assembly with a phase reference. |
| 60_MHZ | 60 MHz — This is a 60 MHz, ECL level, ac-coupled signal. The Trigger assembly divides this signal to generate 250_KHZ_RCVR, 187.5_KHZ_SRCE, and 100_KHZ_REF. |
| 80_MHZ_RCVR | 80 MHz to Receiver — This is an 80 MHz, 50% duty cycle, ECL level signal. The ADC/Digital Filter assembly divides this signal by four to generate 20 MHz clock signals. |
| 300_MHZ_RCVR | 300 MHz to Receiver — This is a 300 MHz, 0 dBm, ac-coupled sine wave. The Second Conversion assembly mixes this signal with 1ST_IF. |
| 300_MHZ_REF | 300 MHz Reference — This is a 300 MHz, -2 dBm, ac-coupled sine wave. The Step Phase Detector assembly mixes this signal with STEP_VCO. |
| 300_MHZ_SRCE | 300 MHz to Source — This is a 300 MHz, -10 dBm, ac-coupled sine wave. The Source Conversion assembly mixes this signal with a 10.1875 MHz signal. |
| 1ST_IF | First Intermediate Frequency — This is a 310.1875 MHz signal with a nominal full-scale amplitude of -30 dBm. This signal is the input signal for the Second Conversion assembly. |

| | |
|------------|--|
| 2ND_IF | Second Intermediate Frequency — This is a 10.1875 MHz signal with a nominal full-scale amplitude of -37 dBm signal. This signal is the input signal for the IF assembly. |
| 3RD_IF | Third Intermediate Frequency — This is a 187.5 kHz signal with a nominal full-scale amplitude of 3 dBV. This signal is the input signal for the ADC/Digital Filter assembly. |
| CAL | Calibration — This is a square wave with a -20 dBm precision-amplitude fundamental. The Reference/Calibrator assembly attenuates either CAL_SRCE or a fixed 10 MHz signal. The calibration and self-test routines use this signal at various times. |
| CAL_SRCE | Calibration Source — During calibration of the input path, this is a 200 kHz to 150 MHz, approximate -11 dBm signal. The Source Amplifier assembly routes this signal to the Reference/Calibrator assembly. The calibration, adjustment-setup, and self-test routines use this signal path at various times. |
| EXT_REF_IN | External Reference — This is the analyzer's external reference input from the optional Fan Power/Oven assembly or an external source. The signal can be a 1 MHz, 2 MHz, 5 MHz, or 10 MHz sine or square wave with an amplitude between 5 dBm and $+10$ dBm. This signal is routed from a BNC connector on the rear panel. |
| EXT_TRIG | External Trigger — This is the analyzer's external trigger input. When the CPU assembly enables external trigger mode, a TTL low on this line triggers the analyzer. This signal is routed from a BNC connector on the rear panel. |
| F/N_VCO | Fractional-N Voltage Controlled Oscillator — When the local oscillator is operating in single loop mode, this is a 31 to 46 MHz, dc-coupled, ECL level, square wave derived from dividing SL_VCO by 10. In multiple loop mode, this is a 30 to 55 MHz, dc-coupled, ECL level, square wave controlled by CV_FRACN. The Fractional-N assembly divides this signal down to 100 kHz. |

Note



For information on the local oscillator's single and multiple loop modes, see figures 4-12 and 4-13.

| | |
|-----------|---|
| INPUT_OUT | Input Out — This signal's frequency range is 10 Hz to 150 MHz and its full-scale amplitude is approximately -28 dBm ± 1 dB. This signal is the input signal after it is buffered or attenuated, then amplified and filtered. This signal is the input signal for the First Conversion assembly. |
|-----------|---|

| | |
|-------------|---|
| INTRPL_VCO | Interpolation Voltage Controlled Oscillator — This is either a 3 to 5 MHz or a 6 to 11 MHz, ac-coupled, ECL level, square wave. The frequency range depends on whether F/N_VCO is divided by ten or by five. The Sum Phase Detector uses this signal for a phase comparison. This signal is only present when the local oscillator is operating in multiple loop mode. |
| NORMALIZE | Normalize — The analyzer's calibration and self-test routines use this signal path at various times. During calibration of the source, this is a 300 kHz signal routed to the Input assembly. |
| REF_OUT | Reference Out — This is a 10 MHz, 50% duty cycle, ECL level, ac-coupled sine wave derived by dividing 20_MHZ by two. This signal is routed to a BNC connector on the rear panel. |
| SL_VCO | Single Loop Voltage Controlled Oscillator — This signal can sweep from 310.1875 to 460.1875 MHz. It is a +3 dBm signal controlled by CV_SL. The Interpolation VCO assembly divides this signal by 10 and routes it to the Fractional-N assembly as F/N_VCO. This signal is only present when the local oscillator is operating in single loop mode. |
| SRCE_AMP | Source Amplifier — This is a 10 Hz to 150 MHz, -41 to -60.9 dBm signal. This signal is the input for the Source Amplifier. |
| STEP_TO_SUM | Step to Sum Voltage Controlled Oscillator — When the local oscillator is operating in multiple loop mode, this is a 306 to 450 MHz, -8 dBm signal controlled by CV_STEP. This signal steps from 306 to 336 MHz in 2 MHz steps and from 335 to 450 MHz in 5 MHz steps. The Sum Phase Detector mixes this signal with SUM_VCO. When the local oscillator is operating in single loop mode, this is a 306 MHz signal that is not used. |
| STEP_VCO | Step Voltage Controlled Oscillator — When the local oscillator is operating in multiple loop mode, this is a 306 to 450 MHz, +10 dBm signal controlled by CV_STEP. This signal steps from 306 to 336 MHz in 2 MHz steps and from 335 to 450 MHz in 5 MHz steps. The Step Phase Detector mixes this signal with 300_MHZ_REF. When the local oscillator is operating in single loop mode, this is a 306 MHz signal that is not used. |
| SUM_VCO | Sum Voltage Controlled Oscillator — This signal can sweep from 310.1875 to 460.1875 MHz. Its amplitude is typically +8 dBm, and it is controlled by CV_ML. The Sum Phase Detector mixes this signal with STEP_TO_SUM. This signal is only used when the local oscillator is operating in multiple loop mode. |

SWEPT_LO_RCVR Swept Local Oscillator to Receiver — This signal can sweep from 310.1875 to 460.1875 MHz. When the local oscillator is operating in single loop mode, this signal is controlled by CV_SL, and in multiple loop mode, this signal is controlled by CV_ML. This signal's amplitude is typically +4 dBm. The First Conversion assembly mixes this signal with INPUT_OUT.

SWEPT_LO_SRCE Swept Local Oscillator to Source — This signal can sweep from 310.1875 to 460.1875 MHz. When the local oscillator is operating in multiple loop mode, this signal is controlled by CV_SL, and in multiple loop mode, this signal is controlled by CV_ML. This signal's amplitude is typically -10 dBm. The Source Conversion assembly mixes this signal with 310.1875 MHz.

TRIG_OUT Trigger Output — If the trigger is in slave mode, this is a buffered version of EXT_TRIG; otherwise, this is a buffered version of LSWP. This signal is routed to a BNC connector on the rear panel.

Motherboard Signals

| | |
|-------------|--|
| 187.5_SIG\ | 187.5 kHz Signal — This line is used during self tests and disabled during normal operation. This line goes low if the 187.5 kHz reference is present when a self test checks for the presence of the reference. This line also goes low if the output of the gilbert cell multiplier is present when a self test checks for the presence of the output. |
| ATN0 — ATN4 | Attenuator Control — These lines provide attenuator control for the IF assembly. |
| CAL_ON | Calibration Path Enable — A high on this line enables the calibration path from the Source Amplifier assembly to the Reference/Calibrator assembly. |
| CV_FRACN | Control Voltage to Fractional-N — This is the control voltage for the Interpolation VCO assembly. Its amplitude is between approximately $-3V$ and $+11.5V$. This signal is only used when the local oscillator is operating in multiple loop mode. |

Note



For information on the local oscillator's single and multiple loop modes, see figures 4-12 and 4-13.

| | |
|---------|---|
| CV_ML | Control Voltage Multiple Loop — This is the control voltage for the Sum VCO assembly. Its amplitude is between approximately $-2V$ and $+7V$. This signal is only used when the local oscillator is operating in multiple loop mode. |
| CV_SL | Control Voltage Single Loop — This is the control voltage for the Sum VCO assembly. Its amplitude is between approximately -2 and $+7V$. This signal is only used when the local oscillator is operating in single loop mode. |
| CV_STEP | Control Voltage Step — This is the control voltage for the Step VCO assembly. When the local oscillator is operating in multiple loop mode, this signal's level is between approximately $-2V$ and $+7V$. When the local oscillator is operating in single loop mode, this signal's level is approximately $+7V$. |
| GETTRIG | Group Execute Trigger — This is the group execute trigger from the HP-IB interface on the CPU assembly. When the analyzer is under HP-IB control, the Trigger assembly uses this line to trigger the analyzer. |

| | |
|----------|--|
| HFU\ | High Frequency Unlocked — This line is low when the 300 MHz phase-lock loop on the 300 MHz assembly is unlocked. A low on this line forces SINT\ low. |
| INC_IMAG | Increment Imaginary — This is the increment pulse for local oscillator feedthrough null imaginary axis control. UP_DN sets the increment direction. INC_IMAG, INC_REAL, and UP_DN interact to null the local oscillator feedthrough circuit on the First Conversion assembly. |
| INC_REAL | Increment Real — This is the increment pulse for local oscillator feedthrough null real axis control. UP_DN sets the increment direction. INC_IMAG, INC_REAL, and UP_DN interact to null the local oscillator feedthrough circuit on the First Conversion assembly. |
| LO_DET\ | Local Oscillator Detector — This line is low when the 10 MHz reference is not present on the IF assembly. A low on this line forces SINT\ low. |
| LSWP\ | Sweep Synchronization — This is the TTL sweep synchronization signal. After a change in resolution bandwidth or an instrument preset, the negative edge of this signal resets the digital filters on the ADC/Digital Filter assembly. On subsequent negative edges, this signal is the sweep signal for the analyzer. |
| ML/SL | Multiple Loop/Single Loop — This line is low when the local oscillator is in multiple loop mode and high when the local oscillator is in single loop mode. This line controls a switch on the Sum VCO assembly. |
| PRETUNE | Pretune — This signal coarsely adjusts the sum VCO. It is a scaled version of CV_STEP. When the local oscillator is operating in multiple loop mode, this signal's amplitude is between -2V and +7V. This voltage is added to the output of the integrator on the Sum Phase Detector assembly and becomes CV_ML. When the local oscillator is operating in single loop mode, this signal's amplitude is about +7V. |
| PSSD\ | Power Supply Shut Down — A short circuit to ground on this line forces all Power Supply output voltages to zero. This line is normally an open circuit, but becomes a short circuit to ground if the analyzer's internal temperature becomes excessive. |
| RESET\ | System Reset — A low on this line resets the digital logic on the ADC/Digital Filter assembly. This line is pulsed low during power-up and power-down, when the processor is externally reset, and when the processor executes the RESET instruction. |
| SCLA\ | Serial Clock A — This is a serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock. This clock synchronizes the transfer of data on the IIC bus. |

| | |
|------------|---|
| SCLB\ | Serial Clock B — This is another serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock. This clock synchronizes the transfer of data on the IIC bus. |
| SDA\ | Serial Data — This is the IIC bus bidirectional data line. This line transmits data to or from the CPU assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus. |
| SIG_DET | Signal Detection — This line is high when the signal at the 10.1875 MHz input of the IF assembly is approximately 15 dB over full scale. |
| SINT\ | Serial Interrupt — This is the IIC bus interrupt line. A low on this line interrupts the CPU assembly. |
| SLF\ | Sweep Limit Flag — This line goes low if the fractional-N integrated circuit on the ADC/Digital Filter assembly reaches the end of its frequency sweep. A low on this line can force SINT\ low. |
| SPEED_UP | Speed Up — When the sum loop is unlocked, this line is +15V and it speeds up the settling time of the sum loop. When the sum loop is locked, this line is -15V. This line controls a switch on the Sum VCO assembly. This line is only used when the local oscillator is operating in multiple loop mode. |
| SRCE_ON | Source On — This line is high when the source is on and low when the source is off. |
| SUM_OOL_H | Sum Out of Lock High — This line is high when the sum loop is unlocked because the frequency of the sum loop circuit is too high. |
| SUM_OOL_L | Sum Out of Lock Low — This line is high when the sum loop is unlocked because the frequency of the sum loop circuit is too low. |
| THRESH_LOW | Threshold Low — This line sets the overload detector threshold for the Source Amplifier assembly. |
| UP_DN | Up or Down — This line sets the increment direction for INC_IMAG and INC_REAL. When this line is low the increment direction is down. When this line is high the increment direction is up. INC_IMAG, INC_REAL, and UP_DN interact to null the local oscillator feedthrough circuit on the First Conversion assembly. |

HP-IB Connector Signals

Note



The descriptions that follow for the HP-IB lines are general descriptions only. For a detailed description of how the analyzer interprets the HP-IB lines, see the *HP 3588A HP-IB Programming Reference*.

| | |
|-------------|---|
| ATN | Attention — This line is controlled by the controller in charge. When this line is low, the DIO lines contain interface commands. When this line is high, the DIO lines contain data. |
| DAV | Data Valid — This line goes high when valid data is on the bus. This line is controlled by the HP-IB controller. |
| DIO1 — DIO8 | Data Input/Output — These are inverted data lines that conform to IEEE specification IEEE-488. When ATN is low, these lines contain interface commands. When ATN is high, these lines contain data. |
| EOI | End or Identify — If ATN is high, a high on this line marks the end of a message block. If ATN is low, a high on this line requests a parallel poll. |
| IFC | Interface Clear — This line goes high to set the interface system to a known state. The system controller becomes the controller in charge. |
| NDAC | Not Data Accepted — This line goes high when the DIO lines have been latched by the acceptor. |
| NRFD | Not Ready for Data — This line goes high when the acceptor is ready for more data. |
| REN | Remote Enable — This line is high when the HP-IB has control, and low when the Front Panel assembly has control. |
| SRQ\ | Service Request — This line is low when a device on the HP-IB needs service. |

Calibration Routine

The calibration routine minimizes the receiver's LO feedthrough, and also provides amplitude correction for both the receiver and the source. The receiver's amplitude corrections are stored in memory as vectors. All measurements are multiplied by these vectors before being displayed (the vectors become part of the measurement). The calibration routine occurs immediately following the power-on tests and periodically afterwards to compensate for any drift. To manually start the calibration routine, press the [Spcl Fctn] hardkey followed by the [SINGLE CAL] softkey.

First, the calibration routine nulls the receiver's LO feedthrough. The receiver measures the LO feedthrough (response at 0 Hz input frequency) and sends the results to the CPU assembly. The CPU then sends control data to the Input assembly. The Input assembly decodes the control data and sends three control lines to the First Conversion assembly (see figure 4-32). These control lines adjust the real and imaginary components of the LO feedthrough cancellation signal. The LO cancellation signal then is added to the LO feedthrough. This process continues until a satisfactory null is achieved.

The calibration routine then produces amplitude correction for the IF assembly's attenuators. The calibrator generates a 10 MHz square wave with a -20 dBm precision-amplitude fundamental. This signal is sent to the receiver through the CAL path. Measurements are taken for all 32 attenuator settings, and the results are stored in memory.

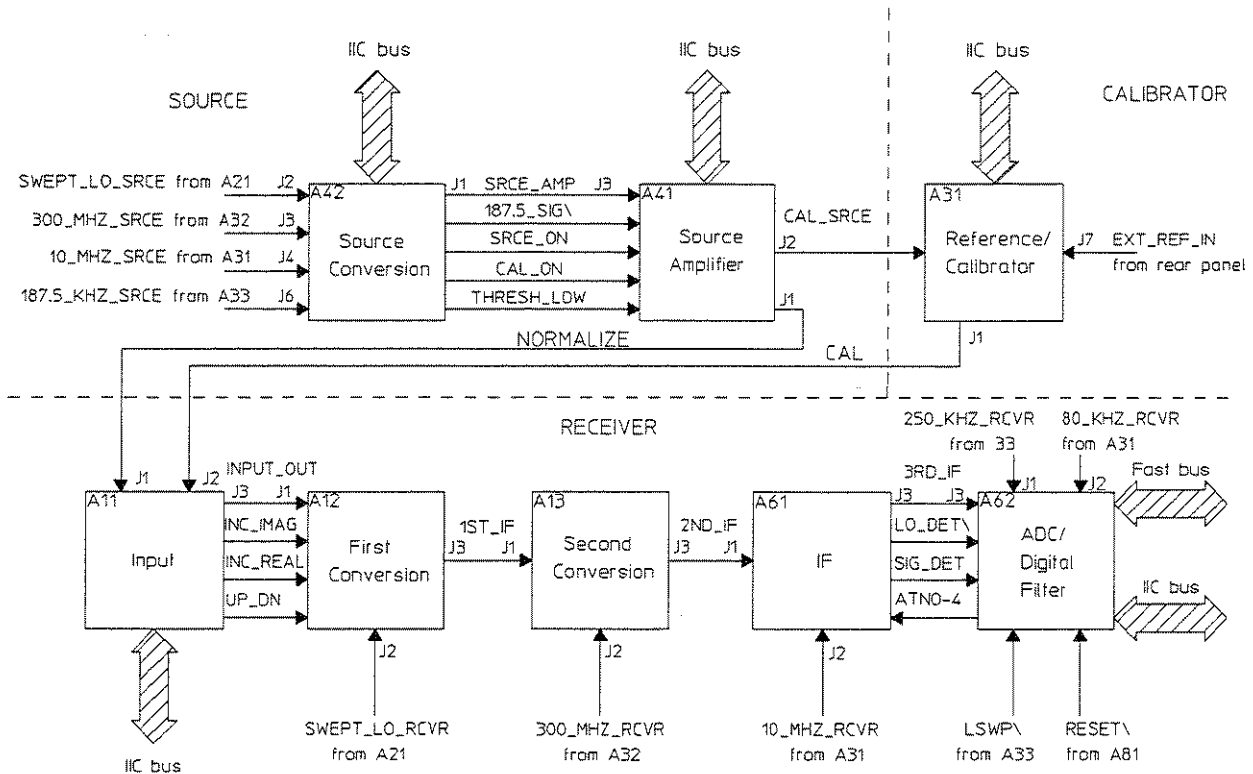


Figure 4-32. Calibration Block Diagram

Next, the calibration routine produces correction curves for the Input assembly's input paths. The source generates a swept 200 kHz to 150 MHz signal. This swept signal is sent to the calibrator through the CAL_SRCE path. The calibrator uses the swept signal to generate a swept 200 kHz to 150 MHz square wave with a -20 dBm precision-amplitude fundamental. This precision signal is sent to the receiver through the CAL path. Measurements are taken with the signal routed through the Input assembly's 50Ω input path (for all attenuators) and through the 1 MΩ input path. The measurement results are stored in memory as vectors.

The calibration routine then produces a correction curve for the shape of the 3rd IF filter. This correction curve is used in only narrow-band zoom measurements. The calibrator generates a 10 MHz square wave with a -20 dBm precision-amplitude fundamental. This precision signal is sent to the receiver through the CAL path. As the local oscillator sweeps, tracing out the shape of the 3rd IF, measurements are taken. The measurement result is stored in memory as a vector.

Last, the calibration routine produces amplitude correction data for the source. The source generates a 300 kHz signal. This signal is sent to the receiver through the NORMALIZE path. The receiver measures the signal at two different amplitudes and sends the measurement results to the CPU assembly. The CPU assembly then uses the measurement results to calculate the correction data for the source.

Calibration Error Message

Calibration correction vectors are compared with a set of maximum allowable error vectors. If any correction vector exceeds the maximum allowable error, the **Calibration failure** error message is displayed on the screen (for approximately 5 seconds) and placed in the Fault Log. To view the Fault Log, press the following keys:

```
[ Spcl Fctn ]  
  [ +/- ] (second softkey from bottom)  
  - 99  
  [ +/- ] (second softkey from bottom)  
  [ SERVICE FUNCTIONS ]  
  [ FAULT LOG ]
```

Note



Pressing the [Spcl Fctn] hardkey followed by the second softkey from the bottom, [+/-], [9], [9], and the second softkey from the bottom, enables and displays the [SERVICE FUNCTIONS] softkey. The [SERVICE FUNCTIONS] softkey remains enabled until power to the analyzer is removed.

Calibration Correction Curves

The calibration correction curves can be viewed for any input range or frequency span in the 50 Ω input path. Calibration fails if a correction curve for the 50 Ω input path varies by more than ± 10 dB from 0 dBV². Figure 4-33 shows a typical calibration curve for the following instrument set up:

```
[ Preset ]
[ Range/Input ]
  [ AUTORANGE ON OFF ]
  [ RANGE ] (any range from -20 to +20 dBm)
[ Meas Type ]
  [ LOW DIST ON OFF ] (low distortion mode can be on or off)
[ Scale ]
  [ REF TRACK ON OFF ]
  [ REFERENCE LEVEL ]
  6.5
  [ dBm ]
  [ VERTICAL /DIV ]
  1
  [ dB ]
[ Spcl Fctn ]
  [ AUTO CAL ON OFF ]
  [   ] (second softkey from bottom)
  -99
  [   ] (second softkey from bottom)
  [ SERVICE FUNCTIONS ]
  [ CAL OPTIONS ]
  [ CAL TRC ON OFF ]
  [ IF ATTEN ON OFF ] (IF attenuation corrections can be on or off)
  [ IF SHAPE ON OFF ] (IF shape corrections can be on or off)
  [ SOURCE ON OFF ] (source corrections can be on or off)
```

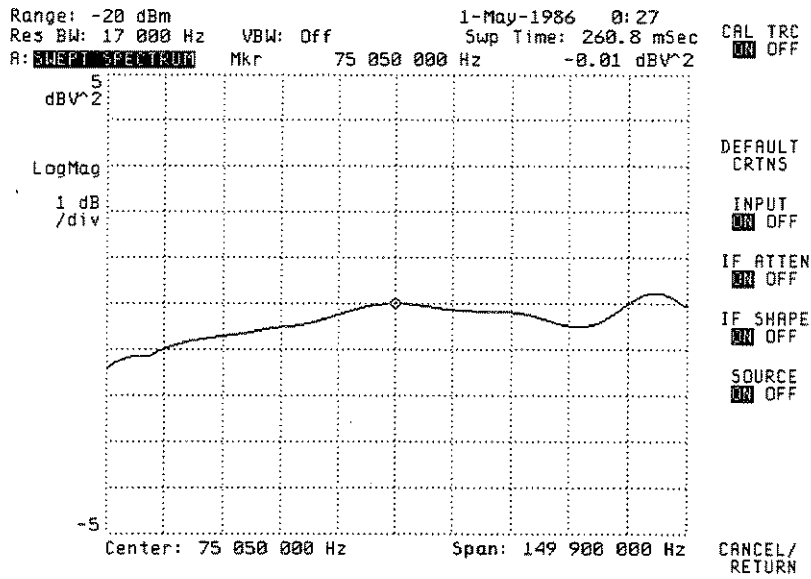


Figure 4-33. Typical 50 Ohm Input Calibration Curve

The calibration correction curves can be viewed for any frequency span in the 1 MΩ input path. Calibration fails if a correction curve for the 1 MΩ input path, from 10 Hz to 40 MHz, varies by more than ± 10 dB from 0 dBV². Figure 4-34 shows a typical calibration curve for the following instrument set up:

- [Preset]
- [Range/Input]
 - [1 MEGOHM]
- [Freq]
 - [STOP]
 - 40
 - [MHz]
- [Scale]
 - [REF TRACK ON OFF]
 - [REFERENCE LEVEL]
 - 5
 - [dBm]
 - [VERTICAL /DIV]
 - 1
 - [dB]

[Spcl Fctn]

- [AUTO CAL ON OFF]
- [] (second softkey from bottom)
- 99
- [] (second softkey from bottom)
- [SERVICE FUNCTIONS]
- [CAL OPTIONS]
- [CAL TRC ON OFF]
- [IF ATTN ON OFF] (IF attenuation corrections can be on or off)
- [IF SHAPE ON OFF] (IF shape corrections can be on or off)
- [SOURCE ON OFF] (source corrections can be on or off)

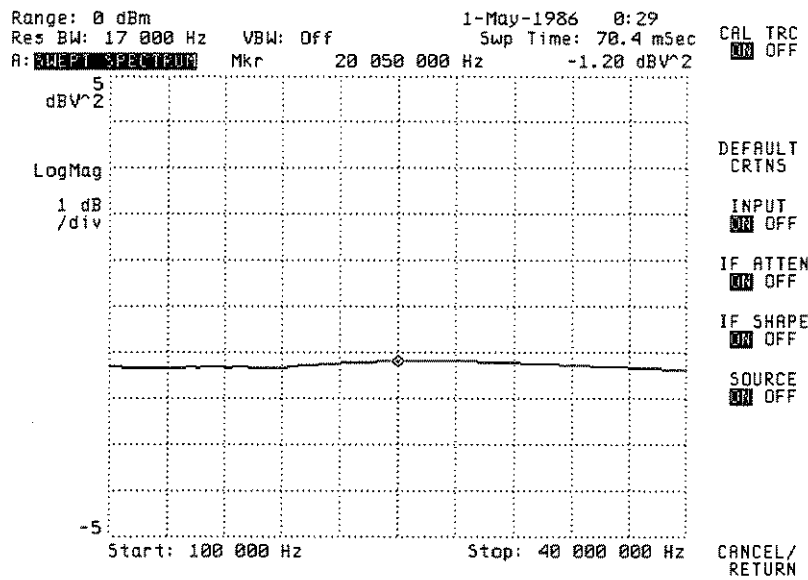


Figure 4-34. Typical 1 Meg Ohm Input Calibration Curve

Fault Log Messages

| | |
|--------------------------------------|--|
| 250 kHz Sample Clock failure | This error message occurs if a circuit on the ADC/Digital Filter assembly does not detect the 250 kHz reference signal from the Trigger assembly. |
| 10 MHz third LO failure | This error message occurs if a circuit on the IF assembly does not detect the 10 MHz reference signal from the Reference/Calibrator assembly. |
| 80 MHz clock failure | This error message occurs if a circuit on the ADC/Digital Filter assembly does not detect the 20 MHz clock signals. The 20 MHz clock signals are derived from dividing the 80 MHz reference signal by four. Since the Reference/Calibrator assembly's 80 MHz reference is the analyzer's primary frequency reference, many failures occur if the 80 MHz reference is not present. |
| 300 MHz Ref Unlocked | This error message occurs if the control voltage for the 300 MHz VCO is too high or too low, indicating that the 300 MHz VCO is unlocked. Since the 300 MHz VCO is the analyzer's high frequency reference, many failures occur if it is unlocked. If the primary frequency reference from the Reference/Calibrator assembly is not present, the 300 MHz VCO unlocks. |
| Calibration failure | This error message occurs if the calibration routine generates correction vectors that exceed the maximum allowable error vectors. |
| Detector Gate Array DMA over-run | This error message occurs if the ADC/Digital Filter assembly's detector gate array detects an acknowledge signal from the CPU assembly's DMA controller when a request is not pending. |
| Detector Gate Array illegal input | This error message occurs if the ADC/Digital Filter assembly's digital filter gate array sends data to the detector gate array in an illegal format. |
| Filter Gate Array always busy | This error message occurs if the ADC/Digital Filter assembly's gate array takes too long to change out of "run" mode. |
| Filter Gate Array input over-sample | This error message occurs if the ADC/Digital Filter assembly's sample time is too short. |
| Frac N unlocked - frequency too high | This error message occurs if a circuit on the Interpolation VCO assembly detects that the amplitude of the fractional-N control voltage is too low (frequency too high). The fractional-N control voltage is monitored when the local oscillator is in multiple loop mode or single loop mode even though the Interpolation VCO is not used in single loop mode. Since the fractional-N control voltage is the same as the single loop control voltage, checking the fractional-N control voltage is essentially the same as checking the single loop control voltage. |

| | |
|-------------------------------------|--|
| Frac N unlocked - frequency too low | This error message occurs if a circuit on the Interpolation VCO assembly detects that the amplitude of the fractional-N control voltage is too high (frequency too low). The fractional-N control voltage is monitored when the local oscillator is in multiple loop mode or single loop mode even though the Interpolation VCO is not used in single loop mode. Since the fractional-N control voltage is the same as the single loop control voltage, checking the fractional-N control voltage is essentially the same as checking the single loop control voltage. |
| I2C: No Device Acknowledge | This error message occurs if the CPU assembly's IIC controller does not sense the acknowledge part of the formal handshake used to transmit data over the IIC bus. |
| I2C: Timeout | This error message occurs if the CPU assembly's IIC controller takes too long to tell the MPU that it is ready for a new command. |
| Input Tripped | This error message occurs if an overload occurs in the Input assembly's 50 Ω impedance path. When this occurs, relays disconnect the input signal from the front panel. |
| LSWEEP timed-out | This error message occurs if the ADC/Digital Filter assembly does not sense an LSWP\ signal from the Trigger assembly during the time expected. |
| Power-on ROM Checksum error | This error message occurs if a power-on test detects a ROM checksum error. |
| Power-on test failure | This error message occurs if a power-on test fails. |
| Source Tripped | This error message occurs if the voltage at the output of the Source Amplifier assembly exceeds the threshold set by the Source Conversion assembly. When this occurs, the source output is disconnected from the front panel. |
| Step Loop unlocked | This error message occurs if a circuit on the Step Phase Detector assembly detects that the step loop control voltage is too high or too low, indicating that the step loop is unlocked. The control voltage is clamped to service adjustable limits when the step loop is unlocked. |
| Sum Loop unlocked | This error message occurs if a circuit on the Sum Phase Detector assembly detects that the amplitude of the integrator output is too high or too low, indicating that the sum loop is unlocked. The integrator output is clamped when the sum loop is unlocked. |

Power-On and Preset States

The analyzer is in a known state after power up or after pressing the [**Preset**] key. Pressing the [**Preset**] key resets the analyzer as close to the power-on state as possible. To view the power-on state, press [**Format**] [**SETUP STATE**] immediately after power up or after pressing the [**Preset**] key. States that are reset by power up, but not by pressing the [**Preset**] key, are listed in "Power-On States" later in this section. States that are stored in battery-backed-up SRAM are listed in "Nonvolatile States" later in this section.

Note



The following lists only the power-on and preset state values that are NOT displayed after pressing [**Format**] [**SETUP STATE**].

| | |
|------------------------|---|
| [Disk Util] | [FORMAT DISK] [FORMAT OPTION] 0 [INTRLEAVE FACTOR] 1 [CATALOG ON OFF] |
| [Format] | [SINGLE] [GRATICULE ON OFF] |
| [Freq] | [STEP SIZE AUTO USER] [USER STEP SIZE] 1 kHz [SIGNL TRK ON OFF] |
| [Local/HP-IB] | [ECHO ON OFF] |
| [Marker] | [MARKER X ENTRY] 75.05 MHz [OFFSET ON OFF] [MARKER ON OFF] |
| [Marker Fctn] | [PEAK TRK ON OFF] [FREQ CNTR ON OFF] [NOISE LVL ON OFF] [LIMIT TEST] [LINES ON OFF] [TEST EVAL ON OFF] [FAIL BEEP ON OFF] [ABSOLUTE LIMIT] |
| [Meas Type] | [PEAK DET ON OFF] |

| | |
|-----------------|---|
| [Plot/Print] | [DEFINE PLOT] [DEFINE PLOT PENS] [TRACE A PEN] 2 [TRACE B PEN] 3 [MARKER A PEN] 5 [MARKER B PEN] 6 [ALPHA PEN] 4 [GRATICULE PEN] 1 [TRACE A LINE TYPE] [SOLID] [TRACE B LINE TYPE] [SOLID] [PLOT SPEED] [FAST (50 cm/s)] [PAGE EJCT ON OFF] |
| [Range/Input] | [1 MEG REF IMPEDANCE] 50 Ω |
| [Res BW] | [HI ACCRCY ZOOM] |
| [Save/Recall] | [CATALOG ON OFF] |
| [Scale] | [VERTICAL /DIV] 10 dB [REF TRACK ON OFF] [REFERENCE LEVEL] -20 dBm |
| [Source] | [AMPLITUDE STEP] 0.1 dBm [COUPLE TO INPUT Z] |
| [Spcl Fctn] | [AUTO CAL ON OFF] [BEEPER ON OFF] [PRFM TESTS] [SRCE 10dB IN OUT] [SRCE 20dB A IN OUT] [SRCE 20dB B IN OUT] [SRCE DAC ATTEN] 0 dB |
| [Sweep] | [MANUAL FREQ] 75.05 MHz [SAMPLE TIME] 4 μ s [OVERSWEEP ON OFF] |
| [Trace Type] | [LOG MAGNITUDE] |
| [Trace Data] | [INPUT SPECTRUM] |

Service

Introduction

This section contains troubleshooting tests that isolate failures to the assembly. These tests include initial verification, power-on test, self tests, and tests for miscellaneous failures and failing performance tests. This section also contains self-test descriptions and HP-IB command list.

Safety Considerations

The HP 3588A Spectrum Analyzer is a Safety Class 1 instrument (provided with a protective earth terminal). Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings that must be followed to ensure safe operation and retain the HP 3588A Spectrum Analyzer in safe operating condition. Service must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Warning



Any interruption of the protective (grounding) conductor inside or outside the analyzer, or disconnection of the protective earth terminal can expose operators to potentially dangerous voltages.

Under no circumstances should an operator remove any covers, screws, shields or in any other way access the interior of the HP 3588A Spectrum Analyzer. There are no operator controls inside the analyzer.

Only fuses with the required current rating and of the specified type should be used for replacement. The use of repaired fuses or short circuiting the fuse holder is not permitted. Whenever it is likely that the protection offered by the fuse has been impaired, the analyzer must be made inoperative and secured against any unintended operation.

When power is removed from the analyzer, +11000 volts are present in the CRT for approximately 3 seconds. Be extremely careful when working in proximity to this area during this time. The high voltage can cause serious personal injury if contacted.

Caution



Do not connect or disconnect ribbon cables with the power switch set to ON (I). Power transients caused by connecting or disconnecting a cable can damage circuit assemblies.

Equipment Required

See chapter 1, “General Information,” in the *HP 3588A Performance Test Guide* for a table of recommended equipment for troubleshooting. Any equipment which meets the critical specifications given in the table may be substituted for the recommended model.

How to Use This Section

Use the following steps to isolate failures to the assembly. See the disassembly/assembly illustrations in section II, “Replaceable Parts,” to determine how to disassemble and assemble the analyzer.

1. Review “Safety Considerations” and “Troubleshooting Hints.”
2. Determine which troubleshooting test to start with by comparing your analyzer’s symptoms to the symptoms in “Choosing a Troubleshooting Test.”
3. Follow the recommended troubleshooting procedure until you locate the faulty assembly.
4. Replace the faulty assembly, and do the required adjustments and tests listed in “What to Do After an Assembly Is Replaced.”

Troubleshooting Hints

- Incorrect bias supply voltages can cause false diagnostic messages. In most troubleshooting procedures, the power supply voltages are not checked through the motherboard. If you suspect incorrect supply voltages to an assembly, use table 4-13 on page 4-59 and an extender board to check the voltages at the assembly.
- Cables can cause intermittent hardware failures.
- Noise or spikes in the power supply can cause the analyzer to fail.
- Measurements in this section are only approximate (usually ± 1 dB or 10%) unless stated otherwise.
- Use chassis ground for all measurements in this section unless stated otherwise.
- Logic levels in this section are either TTL level high or TTL level low unless stated otherwise. Toggling signal levels continually change from one TTL level to the other.

Choosing a Troubleshooting Test

Use table 5-1 to determine which troubleshooting test to begin with. Test 1. Initial Verification checks the basics: power supply voltages, reset signals, and clocks. It then uses tests 2 through 8 to further isolate the failure. Test 9. Self Test runs all the analyzer's self tests. It then uses tests 10 through 32 to further isolate the failure. Test 33. Memory Battery checks the battery on the Memory assembly. Test 34. Fan Power determines if the fan is faulty. Test 35. Trigger determines the cause of HP-IB trigger and external trigger failures.

Note



If you abort a self test before the self test is finished, the analyzer may fail its calibration routine. To prevent this from happening press [**Preset**] or cycle power after you abort the self test.

The troubleshooting tests in this section assume only one independent failure. Multiple failures can cause false results.

Table 5-1. Troubleshooting Guide

| Symptom | Troubleshooting Test |
|--|------------------------------|
| Screen blank Screen defective After power-on, >3 minutes before keys active No response when key is pressed Incorrect response when key is pressed | Test 1. Initial Verification |
| Calibration fails Performance test fails Local oscillator unlocked Intermittent failure HP-IB fails | Test 9. Self Test |
| Nonvolatile states not saved after power cycled | Test 33. Memory Battery |
| Fan not running | Test 34. Fan Power |
| HP-IB trigger fails External trigger fails | Test 35. Trigger |

What to Do After an Assembly Is Replaced

After replacing an assembly, do the following:

1. Reinstall all assemblies and cables that were removed during troubleshooting.
2. On the CPU assembly, check that SW100 pin 4 is set to 1 and all other pins are set to zero (see figure 5-1).
3. Do the required adjustments listed in table 5-2 (the adjustments are in section I of this manual).
4. Do Test 9. Self Test in this section.
5. Do the required performance tests listed in table 5-2 (the performance tests are in chapter 3 of the *HP 3588A Performance Test Guide*).

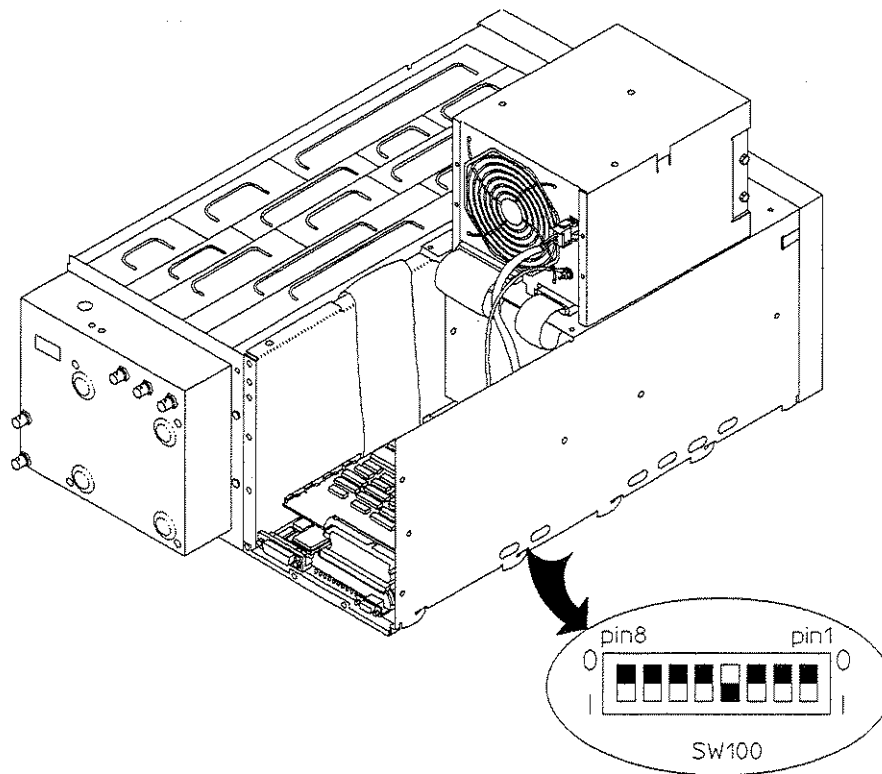


Figure 5-1. Normal Setting for A81 SW100

Table 5-2. Required Adjustments and Performance Tests

| Assembly Replaced | Adjustments | Performance Tests |
|--------------------------|---|--|
| A11 Input | 15. Second IF Bandpass Filter | 1. Local Oscillator Feedthrough 3. Residual Responses 4. Noise Level 8. Input Harmonic Distortion 9. Intermodulation Distortion 11. Frequency Response 12. Reference Level Accuracy 13. Log Scale Accuracy 15. Input Return Loss |
| A12 First Conversion | 12. Second IF Bandpass Filter 14. First IF Bandpass Filter | 1. Local Oscillation Feedthrough 3. Residual Responses 4. Noise Level 7. Image Responses 8. Input Harmonic Distortion 9. Intermodulation Distortion 12. Reference Level Accuracy 13. Log Scale Accuracy |
| A13 Second Conversion | 12. Second IF Bandpass Filter | 3. Residual Responses 12. Reference Level Accuracy 13. Log Scale Accuracy |
| A21 Sum VCO | 4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope | 2. Phase Noise 6. Spurious Responses |
| A22 Sum Phase Detector | 4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope | 2. Phase Noise 6. Spurious Responses |
| A23 Step Phase Detector | 4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope | 2. Phase Noise 6. Spurious Responses |
| A24 Step VCO | 4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope | 2. Phase Noise 6. Spurious Responses |
| A31 Reference/Calibrator | 2. 80 MHz Reference VCXO 3. 300 MHz Reference VCO 17. Calibrator Flatness and Level | 2. Phase Noise 5. Frequency Accuracy 11. Frequency Response |

Table 5-2. Required Adjustments and Performance Tests (continued)

| Assembly Replaced | Adjustments | Performance Tests |
|------------------------|---|---|
| A32 300 MHz | 3. 300 MHz Reference VCO | 2. Phase Noise |
| A33 Trigger | | 2. Phase Noise |
| A41 Source Amplifier | | 10. Source Amplitude Accuracy and Frequency Response 14. Source Dynamic Accuracy 16. Source Return Loss 17. Source Harmonic Distortion 19. Source Noise |
| A42 Source Conversion | 13. Source Bandpass Filter | 10. Source Amplitude Accuracy and Frequency Response 14. Source Dynamic Accuracy 18. Source Spurious Responses |
| A51 Interpolation VCO | 4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope | 2. Phase Noise 6. Spurious Responses |
| A52 Fractional-N | 4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope | 2. Phase Noise 6. Spurious Responses |
| A61 IF | 12. Second IF Bandpass Filter | 3. Residual Responses 4. Noise Level 7. Image Responses 9. Intermodulation Distortion 12. Reference Level Accuracy 13. Log Scale Accuracy |
| A62 ADC/Digital Filter | 11. ADC Gain, Offset, and Reference | 4. Noise Level 12. Reference Level Accuracy 13. Log Scale Accuracy |
| A81 CPU | | |
| A87 Memory | | |
| A88 Expanded Memory | | |
| A90 Fan Power | | |
| A91 Fan Power/Oven | 1. Oven Shutdown 16. Oven Frequency | 2. Phase Noise 5. Frequency Accuracy |
| A99 Motherboard | | |
| Power Supply | | |
| Disk Drive | | |
| Display | | |
| Front Panel | | |

Initial Verification

Before starting Test 1. Initial Verification, check that the voltage selector switch on the rear of the analyzer is set for the local line voltage. Also check that the correct line fuse is installed in the rear panel fuse holder. For information on the voltage selector switch and the line fuse, see chapter 2, "Installation," in the *HP 3588A Performance Test Guide*.

Test 1. Initial Verification

Use this test to check signals that are vital to the operation of the analyzer.

1. If the graticule appears after power-on but there is no response when keys are pressed, do the following:
 - a. Set the power switch to STANDBY (⓪).
 - b. Set the power switch to ON (I) and as soon as the graticule appears, disable the calibration routine by pressing the following keys:
 - [] second softkey from the bottom
 - [] second softkey from the bottom
 - [Spcl Fctn]
 - [AUTO CAL ON OFF]
 - c. If the keys responded correctly, go to Test 10. All Locks Analyzer.
2. Set the power switch to STANDBY (⓪) and disconnect the power cord from the rear panel. Remove the top cover, place the Power Supply assembly in its test position, and remove the Memory assembly (see figures 2-3 through 2-6 in section II, "Replaceable Parts").

Caution



Do NOT remove earth ground (green/yellow wire) from the Power Supply assembly or the analyzer's chassis.

-
3. Disconnect the CPU power cable (W2) from J1 on the CPU assembly. Disconnect the motherboard power cable (W12) from J2 on the Power Supply assembly (see figure 5-2).

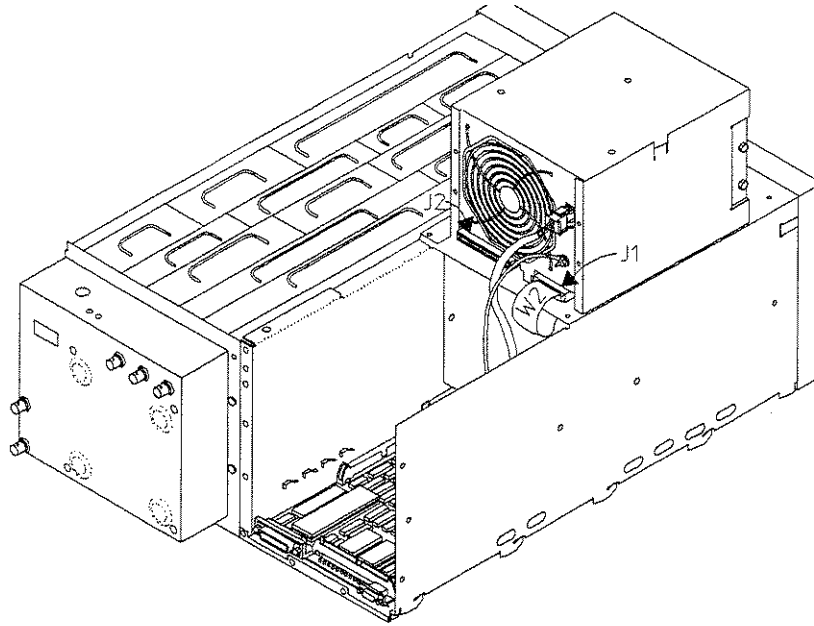


Figure 5-2. Connecting Test Board

4. Connect the power supply test board (from the service kit) to the CPU power cable (W2) and to J2 on the Power Supply assembly. Be careful not to short the test board to the analyzer's chassis.

Warning



The power supply test board dissipates high power from the Power Supply assembly. Be careful of the heat from the shield.

-
5. Connect the power cord and set the power switch to ON (1). Check the voltages in table 5-3. There are no adjustments in the Power Supply assembly; therefore, if any of the voltages are incorrect replace the entire assembly.

Warning



To assure shock protection for the user, reattach the earth ground (green/yellow wire) from the supply to the instrument chassis.

Table 5-3. Test Board Nominal Voltage Values

| Test Location | Nominal Voltage | Minimum Voltage | Maximum Voltage | Ripple Tolerance |
|---------------|-----------------|-----------------|-----------------|------------------|
| TP1 | +8.4V | +7.9V | +10.5V | 84 mVpp |
| TP2 | +15V | +14.55V | +15.45V | 30 mVpp |
| TP3 | +18V | +18V | +27V | 180 mVpp |
| TP4 | -15V | -14.55V | -15.45V | 30 mVpp |
| TP5 | -18V | -18V | -27V | 180 mVpp |
| TP6 | +12V | +11.4V | +12.6V | 120 mVpp |
| TP7 | +5.1V | +4.84V | +5.36V | 51 mVpp |

- Set the power switch to STANDBY (⓪). Disconnect the power supply test board. Reconnect the CPU power cable (W2) to J1 on the CPU assembly and the motherboard power cable (W12) to the Power Supply assembly. Replace the Memory assembly.
- Set the power switch to ON (I). Check the voltages in table 5-4 (see figure 5-3).

Table 5-4. Initial Verification Nominal Voltage Values

| Test Location | Signal Name | Nominal Voltage | Minimum Voltage | Maximum Voltage |
|---------------|-------------|-----------------|-----------------|-----------------|
| A81 TP102 | +5V | +5.1V | +4.845V | +5.355V |
| A81 TP103 | +12V | +12V | +11.4V | +12.6V |
| A81 TP104 | -11V | -11V | -10.45V | -11.55V |

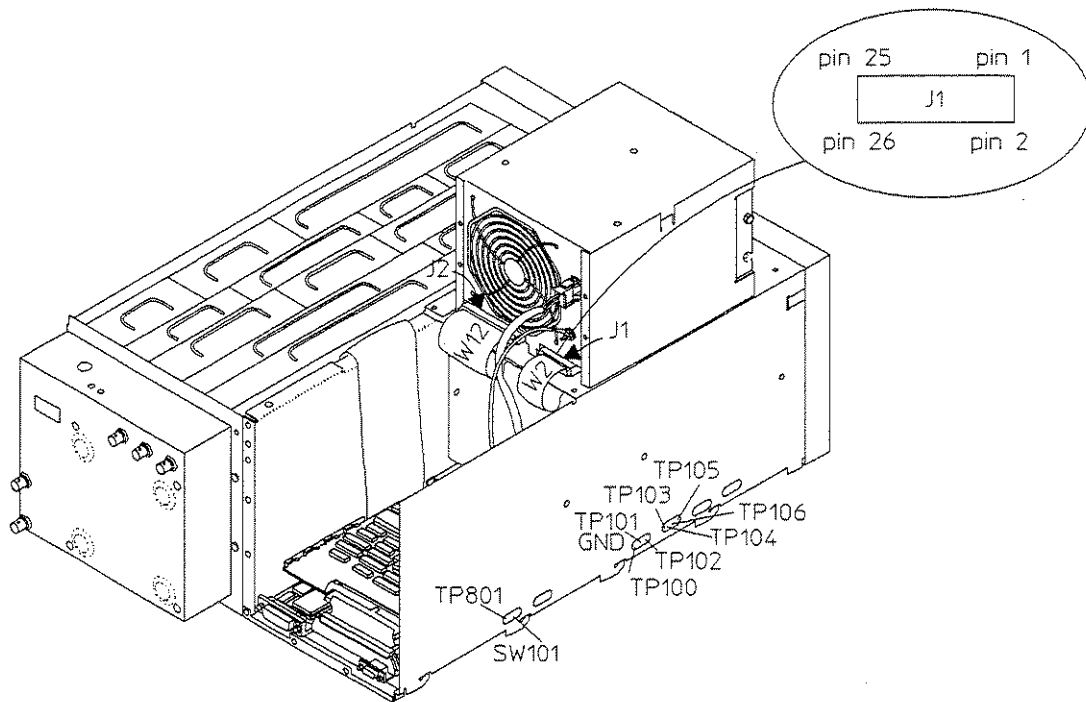


Figure 5-3. Initial Verification Test Locations

8. If the voltages are correct, go to step 9. If the voltages are incorrect, do the following:
 - a. Set the power switch to STANDBY (ϕ). Remove the Memory assembly.
 - b. Disconnect all cables from the CPU assembly except the CPU power cable (W2). Disconnect the motherboard power cable (W12) from the Power Supply assembly.
 - c. Set the power switch to ON (1). Check the voltages in table 5-4. If the voltages are incorrect, the CPU assembly is probably faulty.
 - d. If the voltages are correct, set the power switch to STANDBY (ϕ), reconnect one cable, set the power switch to ON (1), and check the voltages in table 5-4 again. Repeat this step until the faulty assembly or assemblies are located.
 - e. If the failure occurs when the motherboard power cable (W12) is reconnected, set the power switch to STANDBY (ϕ), remove one assembly from the card nest, set the power switch to ON (1), and check the voltages in table 5-4. If the voltages are still incorrect, repeat this step until the faulty assembly is located.

Note

Table 4-2, Power Supply Voltage Distribution, lists which assemblies use each voltage. Use the table to determine which assembly could be causing the failure.

Note

Both the A24 Step VCO assembly and the A41 Source Amplifier assembly have over-temperature protection circuits. These circuits force the power supply output voltages to zero if the analyzer's internal temperature becomes excessive. Before replacing either of these assemblies, make sure both fans are working properly and that the air flow is not restricted (cooling air enters from both sides and exhausts through the rear panel).

9. On the CPU assembly, attach a logic probe to TP100 (RST).

10. While monitoring TP100, press SW101 (reset switch). If the logic level at TP 100 went from high to low, go to step 11. If the logic level at TP100 did not go from high to low, do the following:
 - a. Set the power switch to STANDBY (⓪). Disconnect the CPU power cable (W2) from J1 on the Power Supply assembly.
 - b. Set the power switch to ON (I). With a logic probe, check J1 pin 13 (PVALID) on the Power Supply assembly for a TTL logic high (see figure 5-3). If the signal is incorrect, the Power Supply assembly is faulty.
 - c. Set the power switch to STANDBY (⓪). Reconnect the CPU power cable. On the CPU assembly, attach a logic probe to TP100, and attach a jumper to TP801 (PVALID).
 - d. Set the power switch to ON (I). While monitoring TP100, momentarily connect TP801 to chassis ground. If the logic level at TP100 did not go from high to low, the CPU assembly is probably faulty.
11. Using an oscilloscope and a 10:1 probe, check the clock signals in figure 5-4.

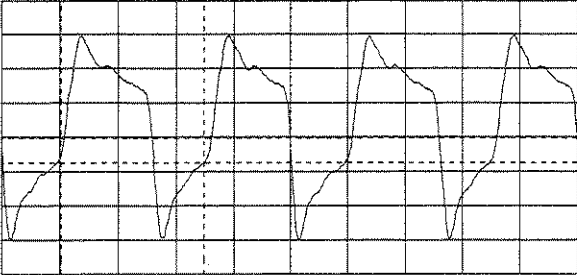
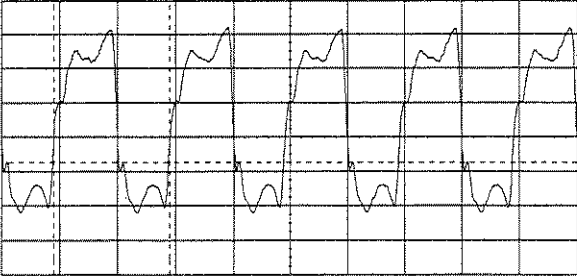
| Oscilloscope Setup | Parameters | Waveform |
|--|--------------------|---|
| Connect CH1 to A81 TP105 Connect GND to A81 TP101 CH1 V/div 200 mV/div CH1 Coupling dc Time/div 20 ns/div Trigger CH1 | Time Duty Cycle |  <p style="text-align: center;">20 MHz (A81 OUT)</p> |
| Connect CH1 to A81 TP106 CH1 V/div 200 mV/div CH1 Coupling dc Time/div 50 ns/div Trigger CH1 | Time Duty Cycle |  <p style="text-align: center;">10 MHz (A81 OUT)</p> |

Figure 5-4. A81 CPU Clock Signals

12. Using an oscilloscope and a 10:1 resistive divider probe with input capacitance of <math><0.7\text{ pF}</math> and input resistance of

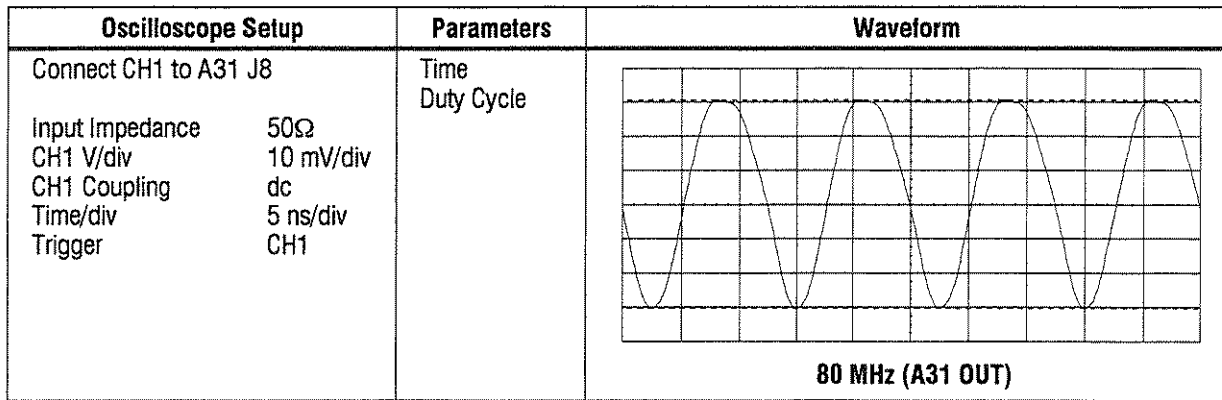


Figure 5-5. 80 MHz Reference Signal

13. If the clock signals are correct, go to Test 2. Power-on.
14. Set the power switch to STANDBY (ϕ). Disconnect the fast bus cable (W11) from J5 on the A62 ADC/Digital Filter assembly.
15. Set the power switch to ON (1). Check the signals in figure 5-5 again. If the signals are now correct, the ADC/Digital Filter assembly's EXT_CLK signal is probably faulty. If the signals are still incorrect, the CPU assembly is probably faulty.

Troubleshooting Using the Power-On Test

Note



Test 1. Initial Verification must be done before the power-on test messages are valid.

Use the power-on test when the screen is defective, when the analyzer does not respond correctly to the keyboard, or when it takes more than 3 minutes for the keyboard to become active. Any of the following conditions may cause a power-on failure:

- A defective CPU or Memory assembly.
- A defective assembly connected to the CPU assembly causing a bus failure.
- A defective cable between the CPU assembly and another assembly.
- A defective control line.

Test 2. Power-on

If Test 1. Initial Verification did not detect any problems, use this test to continue troubleshooting. This test points you to one of the following tests:

- Test 3. CPU, Memory, and Buses
- Test 5. Display
- Test 6. IIC Bus
- Test 7. Fast Bus

Note



The Power Supply assembly is in its test position.

1. Set the power switch to STANDBY (⓪). On the CPU assembly, set SW100 pin 6 to one and pin 4 to zero. Check that the other pins are set to zero (see figure 5-6).

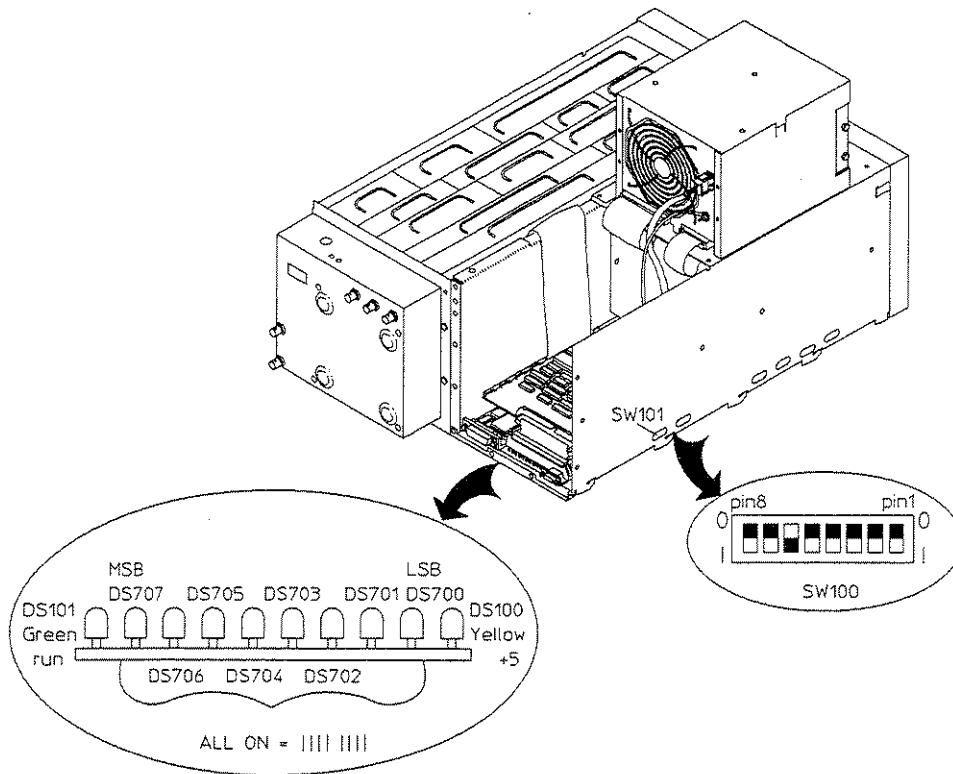


Figure 5-6. Power-on Test LEDs

2. Set the power switch to ON (I). On the CPU assembly, press SW101 (reset switch) while watching the power-on test LEDs (see figure 5-6). The power-on test LEDs pass sequence occurs if the LEDs respond as follows:
 - All power-on test LEDs are on momentarily.
 - DS100 (yellow, +5 LED) remains on as long as power is applied to the assembly.
 - DS101 (green, run LED) comes on as soon as SW101 is released.
 - DS707 through DS700 sequence through the codes listed in the table 5-5.

Table 5-5. Power-on Test Pass Sequence

| Binary 0 = LED off 1 = LED on (DS707) (DS700) | Hexadecimal | ~ Time LEDs Visible | Description |
|--|-------------|-------------------------|--------------------------------------|
| 1111 1111 0000 0000 | FF 00 | 200 ms on 200 ms off | A81 flashes LEDs |
| 0000 0101 | 05 | * | starting A81 test |
| 1001 0000 | 90 | * | A81 monitor ROM test |
| 0000 1000 | 08 | * | starting A81 display controller test |
| 1111 0000 | F0 | 5s | starting A87 program ROM test |
| 0000 1011 | 0B | * | get RAM size |
| 0000 1111 | 0F | 30 - 45s | starting A87 RAM test |
| 1000 0000 | 80 | 6s | starting A87 RAM refresh test |
| 0000 0000 | 00 | Remain off | clear LEDs |

* When no failure occurs, these codes appear for only a very short time and probably won't be visible.

- If a failure occurs in the core assemblies or on the buses, the power-on test pauses and LEDs DS707 through DS700 show a fail code for approximately 10 seconds. Compare your power-on test results to table 5-6 and follow the recommended troubleshooting test.

Table 5-6. Power-on Test Results

| LEDs Sequence Results | Troubleshooting Test |
|---|--------------------------------|
| LEDs show a fail code. A81 DS101 (green run LED) is off. | Test 3. CPU, Memory, and Buses |
| LEDs pass sequence occurs, but the screen is defective. | Test 5. Display |
| LEDs pass sequence occurs, but it takes more than 3 minutes before the keys are active. | Test 6. IIC Bus |
| LEDs pass sequence occurs and screen appears normal, but keys do not function. | |

Note



See table 5-29 on page 5-92 for binary to hexadecimal conversion. For a complete list of the power-on test messages, see table 5-30 on page 5-93.

Test 3. CPU, Memory, and Buses

Use this test to isolate the failure when the power-on test LEDs show a fail code.

Note

The Power Supply assembly is in its test position. On the CPU assembly, SW100 pin 6 is set to one and all other pins are set to zero.

1. Set the power switch to STANDBY (⓪). Remove the Memory assembly.
2. Disconnect the display cable (W3), front-panel cable (W5), and fast bus cable (W11) from J4, J3 and J6 on the CPU assembly. Disconnect the motherboard power cable (W12) from J2 on the Power Supply assembly.

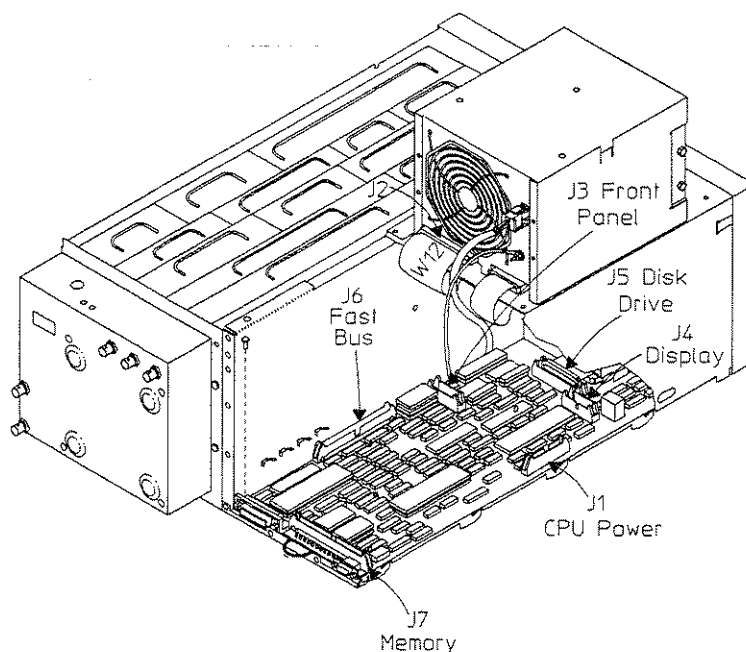


Figure 5-7. Cable Locations

3. Set the power switch to ON (I). On the CPU assembly, press SW101 (reset switch) while monitoring the power-on test LEDs (see figure 5-6). The LEDs display fail code hexadecimal F3 (1111 0011) for 10 seconds, then flash hexadecimal 0F. If the LEDs do not respond correctly, the CPU assembly is faulty.

Troubleshooting Using the Power-On Test

4. Set the power switch to STANDBY (⓪). Reconnect the Memory assembly with the assembly upside-down and outside the chassis. Be careful not to short the pins on back of the assembly.
5. Set the power switch to ON (I). Press SW101 while monitoring the power-on test LEDs.
6. If the LEDs pass sequence does not occur, go to Test 4. Memory.
7. Set the power switch to STANDBY (⓪). Connect the display cable (W3) to J4 on the CPU assembly.
8. Set SW100 pin 6 to zero and pin 4 to one. All other pins are set to zero.
9. Set the power switch to ON (I). Press SW101 while monitoring the power-on test LEDs.
10. The LEDs pass sequence occurs and Testing Memory... is displayed on the screen. About 15 seconds after pressing SW101, the LEDs show fail code hexadecimal A1 (10100001). If the analyzer did not respond correctly, go to Test 5. Display.
11. Set the power switch to STANDBY (⓪). Connect the front-panel cable (W5) to J3 on the CPU assembly and the motherboard power cable (W12) to J2 on the Power Supply assembly.
12. Set the power switch to ON (I). Press SW101 while monitoring the power-on test LEDs.
13. If the LEDs show a fail code other than hexadecimal A1, go to Test 6. IIC Bus.
14. Set the power switch to STANDBY (⓪). Connect the fast bus cable (W11) to J6 on the CPU assembly.
15. Set the power switch to ON (I), and monitor the power-on test LEDs.
16. If the LEDs show fail code hexadecimal A1, go to Test 7. Fast Bus.
17. If the failure still is not isolated, go to Test 6. IIC Bus.

Test 4. Memory

Use this test to separate Memory assembly failures from CPU assembly failures.

Note



The Power Supply assembly is in its test position. The motherboard power cable (W12) is disconnected from J2 on the Power Supply assembly. The Memory assembly is upside-down and outside the chassis. On the CPU assembly, the display cable (W3), front-panel cable (W5), and the fast bus cable (W11) are disconnected. Also, SW100 pin 6 is set to one and all other pins are set to zero.

1. Set the power switch to STANDBY (o). Disconnect the memory cable (W1) from J7 on the CPU assembly.
2. Set the power switch to ON (I). Using a logic probe, check that the signals listed in table 5-7 are toggling (see figure 5-8). If the signals are toggling, the Memory assembly is probably faulty.

Table 5-7. Memory Signals

| Test Location | Signal Name | In/Out |
|---------------|-------------|---------|
| A81 TP107 | AS | A81 Out |
| A81 TP108 | UDS | A81 Out |
| A81 TP109 | LDS | A81 Out |
| A81 TP110 | RW | A81 Out |

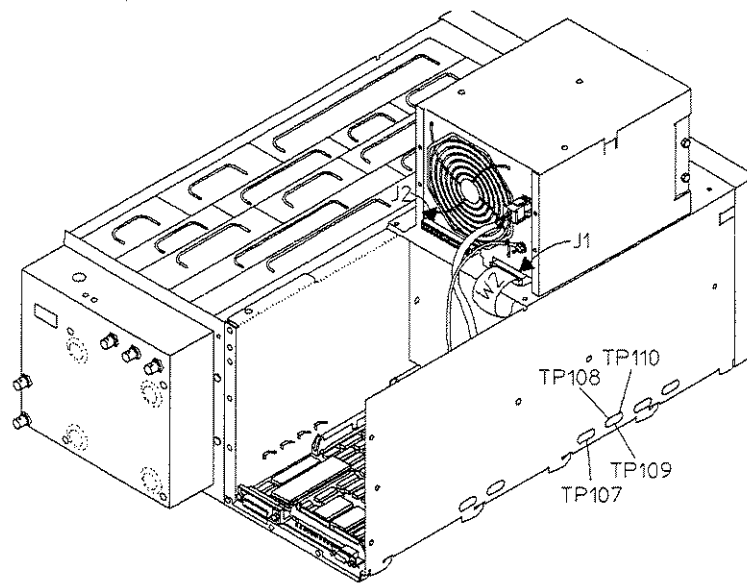


Figure 5-8. Memory Test Locations

Test 5. Display

Use this test to separate Display assembly failures from CPU assembly failures.

Note



The Power Supply assembly is in its test position. The motherboard power cable (W12) is disconnected from J2 on the Power Supply assembly. The Memory assembly is upside-down and outside the chassis. On the CPU assembly, the front-panel cable (W5) and the fast bus cable (W11) are disconnected. Also, SW100 pin 6 is set to one and all other pins are set to zero.

1. Set the power switch to ON (I). Using an oscilloscope and 10:1 probes, check the signals in figure 5-9 (see figure 5-10).

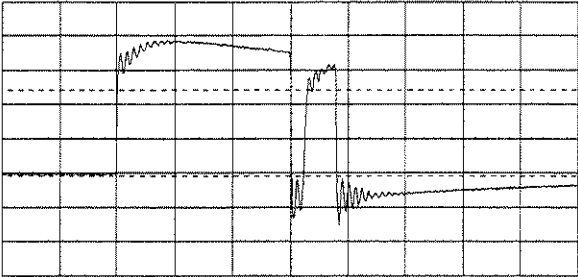
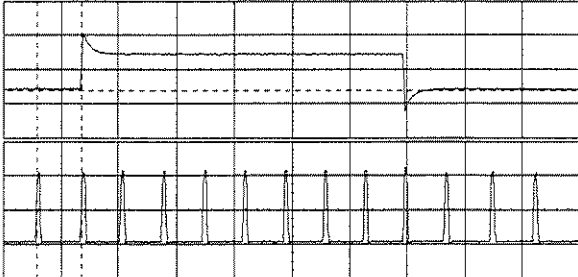
| Oscilloscope Setup | Parameters | Waveform |
|---|---|---|
| Connect CH1 to A81 TP114 CH1 V/div 800 mV/div CH1 Coupling dc Time/div 1 ms/div Trigger CH1 | Active TTL Levels |  HB (A81 OUT) |
| Connect CH1 to A81 TP115 Connect CH2 to A81 TP116 CH1 V/div 200 mV/div CH2 V/div 200 mV/div CH1 Coupling dc CH2 Coupling dc Time/div 50 μs/div Trigger CH1 | Time Time Relationship Duty Cycle |  VSYNC & HSYNC (A81 OUT) |

Figure 5-9. Display Signals

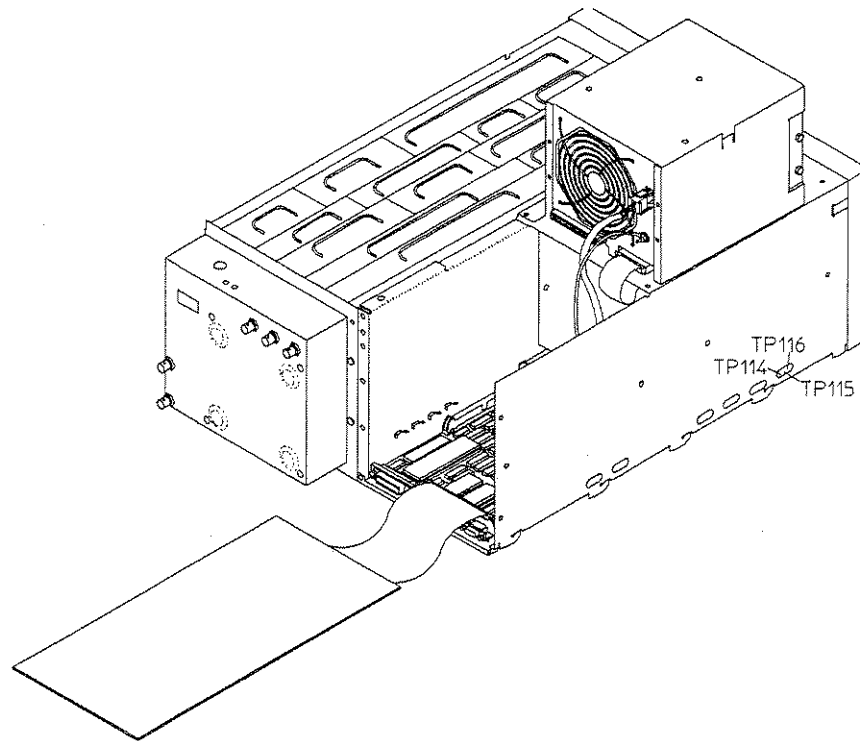


Figure 5-10. Display Controller Test Locations

2. If the signals are incorrect, do the following:
 - a. Set the power switch to STANDBY (ϕ). Disconnect the display cable (W3) from J4 on the CPU assembly.
 - b. Set the power switch to ON (1). Check the signals again. If all the signals are now correct, the Display assembly is probably faulty.

3. Compare your screen to the typical symptoms listed in table 5-8.

Table 5-8. Display Test Troubleshooting Guide

| Symptom | Probable Cause |
|---|--|
| Vertical and horizontal scanning is occurring. Part of information is missing, for example only half letters. Blocks of information are missing. Information on the screen is scrambled or mixed up. Vertical or horizontal stripes appear across the screen. | DRAM sub-block is failing on the CPU assembly. |
| Screen is blank. Screen is tilted, compressed, or distorted. Line across the screen. | Display assembly is failing. |

Note



Before replacing the Display assembly, try the adjustments in section I, "Adjustments."

4. If the failure still is not isolated, check the CPU assembly's control signals in Test 8. Control Lines.

Test 6. IIC Bus (Inter-IC Bus)

Use this test to isolate IIC bus failures to one of the following assemblies:

- Front Panel
- A11 Input
- A23 Step Phase Detector
- A31 Reference/Calibrator
- A33 Trigger
- A41 Source Amplifier
- A42 Source Conversion
- A51 Interpolation VCO
- A52 Fractional-N
- A62 ADC/Digital Filter
- A81 CPU

Note



The Power Supply assembly is in its test position. The Memory assembly is upside-down and outside the chassis. On the CPU assembly, the fast bus cable (W11) is disconnected. Also, SW100 pin 4 is set to one and all other pins are set to zero.

1. Set the power switch to STANDBY (⓪). Connect the fast bus cable (W11) to the CPU assembly.
2. Disconnect the front-panel cable (W5) from J3 on the CPU assembly and the motherboard power cable (W12) from J2 on the Power Supply assembly.
3. On the CPU assembly, attach a logic probe to TP600 (IIC Serial Clock).
4. Set the power switch to ON (I). Press SW101 (reset switch) while monitoring TP600 (SCL) and the power-on test LEDs (see figure 5-11). If the CPU assembly is operating correctly, the TTL logic level at TP600 toggles once when 00 is displayed and again when A1 is displayed.
5. Attach the logic probe to TP601 (IIC Serial Data). Press SW101 while monitoring TP601 (SDA) and the power-on test LEDs. If the CPU assembly is operating correctly, the logic level at TP601 toggles once as SW101 is released (when 00 is displayed) and again when A1 is displayed.
6. Set the power switch to STANDBY (⓪). Connect the front-panel cable (W5) to J3 on the CPU assembly.

7. Set the power switch to ON (I). Repeat steps 3, 4, and 5 to check that the front panel is not causing the failure.
8. Set the power switch to STANDBY (⓪). Connect the motherboard power cable (W12) to J2 on the Power Supply assembly.

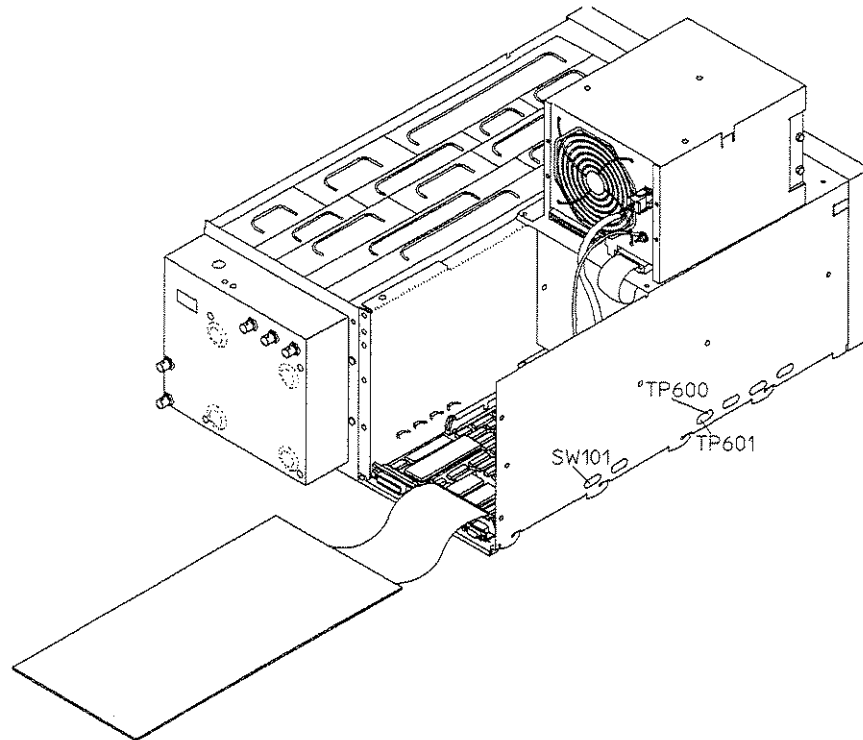


Figure 5-11. IIC Bus Test Locations

9. Set the power switch to ON (I). Press any key. If the analyzer did not respond, do the following:
 - a. Set the power switch to STANDBY (⓪) and remove one of the following assemblies:
 - A11 Input
 - A23 Step Phase Detector
 - A31 Reference/Calibrator
 - A33 Trigger
 - A41 Source Amplifier
 - A42 Source Conversion
 - A51 Interpolation VCO
 - A52 Fractional-N
 - b. Set the power switch to ON (I), then press any key. If the analyzer responds, the assembly just removed is probably faulty.

Note

Press a key before the calibration routine starts. The calibration routine may lock the front panel when an assembly is removed.

- c. If the analyzer did not respond, repeat steps a and b until the faulty assembly is located.
10. If the failure still is not isolated, go to Test 7. Fast Bus.

Test 7. Fast Bus

Use this test to isolate fast bus failures to the CPU assembly, the ADC/Digital Filter assembly, or the fast bus cable.

Note



The Power Supply assembly is in its test position. The Memory assembly is upside-down and outside the chassis. On the CPU assembly, SW100 pin 4 is set to one and all other pins are set to zero. The motherboard power cable (W12) is disconnected from the Power Supply assembly.

1. Set the power switch to STANDBY (⓪). Disconnect the fast bus cable (W11) from J5 on the ADC/Digital Filter assembly.
2. On the CPU assembly, set SW100 pin 6 to one (see figure 5-12).
3. Set the power switch to ON (I). The screen displays Fast Bus Diagnostic Test Also the power-on test LEDs alternately flash hexadecimal AA (DS707, DS705, DS703, and DS701 are on) and hexadecimal 55 (DS706, DS704, DS702, and DS700 are on). If the analyzer did not respond correctly, the CPU assembly is probably faulty.
4. Using a logic probe, check the signals in table 5-9 at the fast bus cable. If the signals are correct, the ADC/Digital Filter assembly is probably faulty.
5. If any of the signals are incorrect, disconnect the fast bus cable from the CPU assembly. Check the failing signals at J6 on the CPU assembly. If the signals are still incorrect, the CPU assembly is faulty.

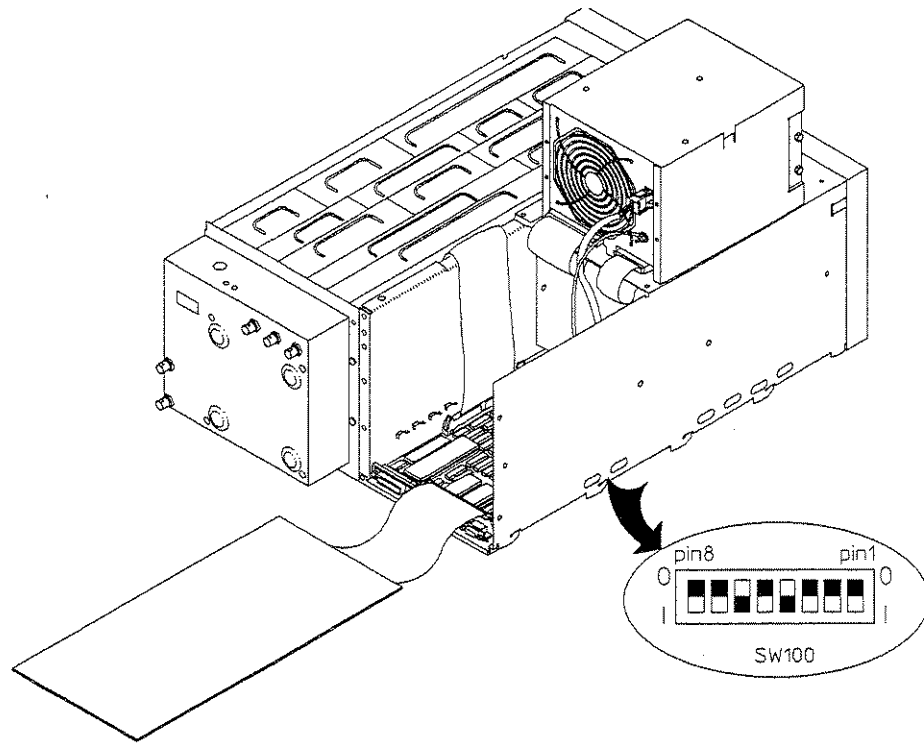


Figure 5-12. Switch Setting for Fast Bus Test

Table 5-9. Fast Bus Lines

| Pin | Signal Name | TTL Logic State In Test Mode |
|--------------|-------------|------------------------------|
| 1 to 31 odd | FD0 - FD15 | Toggling |
| 33 to 41 odd | FA1 - FA5 | Toggling |
| 43 | FIRQ\ | High |
| 45 | FRW | Toggling |
| 47 | SELA\ | High |
| 49 | SELS\ | Toggling |
| 51 | FDTACK\ | High |
| 53 | ECLK | Toggling |
| 55 | REQ\ | High |
| 57 | ACKO\ | High |
| 59 | PCLO\ | High |
| 61 | DTC\ | High |
| 63 | EXT_CLK | High |
| 2 to 64 even | GND | Low |

Test 8. Control Lines

Control line failures can cause false error codes and multiple failure messages. Table 5-10 lists the active state for each control line. The assembly listed in the table as the “Probable Faulty Assembly” is listed with the assumption that no other assembly is loading the line.

1. Set the power switch to STANDBY (⓪). Reinstall all assemblies and cables that were removed during troubleshooting. On the CPU assembly, check that SW100 pin 4 is set to one and all others are set to zero (0000 1000).
2. Set the power switch to ON (I). Check the signals in table 5-10 with a logic probe or oscilloscope (see figure 5-13).

Table 5-10. Data and Control Lines

| Test Location | Signal Name | In/Out | Logic Level During Power-on | Logic Level After Power-on | Probable Faulty Assembly |
|---------------|-------------|--------------|-----------------------------|----------------------------|--------------------------|
| A81 TP107 | AS\ | A81 Out | Toggling | Toggling | A81 |
| A81 TP108 | UDS\ | A81 Out | Toggling | Toggling | A81 |
| A81 TP109 | LDS\ | A81 Out | Toggling | Toggling | A81 |
| A81 TP110 | FRW | A81 Out | Toggling | Toggling | A81 |
| A81 TP111 | DTACK | A62, A87 | Toggling | Toggling | A62, A81, A87 |
| A81 TP112 | BGACK\ | A81 Internal | High | Toggling | A81 |
| A81 TP113 | BERR\ | A81 Internal | Toggle once | High | Any |
| A87 TP102 | RAS1\ | A87 Internal | Toggling | Toggling | A87 |
| A87 TP103 | RAS2\ | A87 Internal | Toggling | Toggling | A87 |
| A87 TP104 | MUX\ | A87 Internal | Toggling | Toggling | A87 |
| A87 TP105 | CASU\ | A87 Internal | Toggling | Toggling | A87 |
| A87 TP106 | CASL\ | A87 Internal | Toggling | Toggling | A87 |
| A87 TP107 | REFIN\ | A87 Internal | Toggling | Toggling | A87 |
| A87 TP108 | REFOUT\ | A87 Internal | Toggling | Toggling | A87 |
| A87 TP109 | ROMSEL\ | A87 Internal | High | Toggling | A87 |
| A87 TP110 | MEM_DTACK\ | A87 Out | Toggling | Toggling | A87 |
| A87 TP111 | RW | A81 Out | Toggling | Toggling | A81 |
| A87 TP113 | DS | A87 Internal | Toggling | Toggling | A87 |
| A81 TP600 | SCL | A81 Out | High | Toggling | A81 |

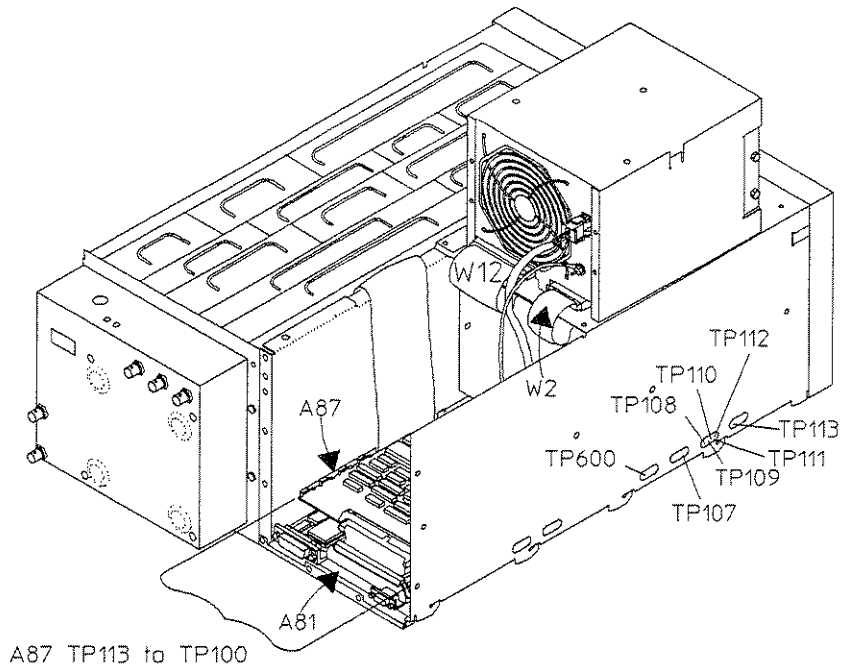


Figure 5-13. Control Lines Test Location

Troubleshooting Using the Self Tests

Use the self tests when one of the following occurs:

- Calibration fails
- Performance test fails
- Local oscillator unlocked
- Failure is intermittent
- HP-IB fails

Test 9. Self Test thoroughly exercises the digital and analog circuits in the analyzer. However, some circuits are not tested, but they are used and can cause tests to fail. Other circuits are neither tested nor used. If you suspect that one of these circuits is faulty, see table 5-11 and follow the recommended troubleshooting test.

Table 5-11. Circuits Not Tested by Test 9. Self Test

| Used But Not Tested: | Troubleshooting Test |
|---|--------------------------------|
| Power Supply assembly | Test 1. Initial Verification |
| Ribbon cable | Test 3. CPU, Memory, and Buses |
| Control lines | Test 8. Control Lines |
| Not Used or Tested: | |
| HP-IB connector | Test 12. HP-IB/RS-232 |
| Source BNC connector and last relay | Test 14. Source |
| Input protection circuits Input BNC and first relay | Test 18. Input Conversion |
| Rear panel oven output Rear panel reference output Rear panel reference input | Test 21. Reference |
| Memory battery Real-time clock | Test 33. Memory Battery |
| Rear panel fan | Test 34. Fan Power |
| Rear panel external trigger Rear panel trigger output | Test 35. Trigger |

Test 9. Self Test

Use this test if the analyzer fails a calibration or performance test.

1. Disconnect all cables connected to the front panel, and set the power switch to STANDBY (0). Remove the top cover (see the disassembly/assembly illustrations in section II, "Replaceable Parts").
2. Set the power switch to ON (1).
3. If a disk drive failure is suspected, install a LIF disk in the disk drive. If a disk drive failure is not suspected, do not install a disk in the disk drive.

Note

The analyzer uses Logical Interchange Format (LIF), option 0-4. This is the same format used by the Series 200/300 BASIC system. To format a disk, press the following keys:

[Disk Util]

[FORMAT DISK]

It takes about 1.5 minutes to format a disk.

4. Press the following keys:

[Spcl Fctn]

[] (second softkey from bottom)

— 99

[] (second softkey from bottom)

[SERVICE FUNCTIONS]

[SELF TEST]

[FUNCTIONL TESTS]

[ALL]

Note

With a disk in the disk drive, this test takes approximately 22 minutes.

Without a disk in the disk drive, this test takes approximately 2 minutes. Also, the disk drive self tests respond with the message, test ABORTED.

5. When the tests have finished running, press the following keys:

[**Spcl Fctn**]
[SERVICE FUNCTIONS]
[SELF TEST]
[TEST LOG]

Note



To print the test log to a HP-IB printer, press the analyzer keys as follows:

[**Local/HP-IB**]
[SYSTEM CONTROLLER]
[**Spcl Fctn**]
[SERVICE FUNCTIONS]
[SELF TEST]
[TEST LOG]
[**Plot/Print**]
[PRINT ALL]

6. If the analyzer did not complete the tests (analyzer locks up), go to Test 10. ALL Locks Analyzer.
 7. If the analyzer completes the tests, compare table 5-12 to the analyzer's test log. If the analyzer's test log matches more than one entry on the table, use the entry closest to the beginning of the table. The table lists the probable faulty assembly or assemblies and any recommended adjustment or troubleshooting procedure to do before replacing the assembly. If both an adjustment and a test are recommended, do the adjustment first.
-

Note



For the complete list of assemblies used in each self test, see table 5-31 on page 5-95. For additional information on the self tests, see "Self Test Descriptions" at the end of this section.

8. If the analyzer passed all but the Quick confidence self test, see table 5-27 in "Troubleshooting Failing Performance Tests."
9. If the problem is intermittent and the analyzer passed all self tests, go to Test 22. Intermittent Failures.

Table 5-12. Self-Test Troubleshooting Guide

| Failing Self Test | Probable Faulty Assembly | Adjustment | Troubleshooting Test |
|---|--|------------|--------------------------------|
| Processor | A81 CPU | | Test 3. CPU, Memory, and Buses |
| ROM | A87/A88 Memory | | Test 3. CPU, Memory, and Buses |
| RAM | A87/A88 Memory | | Test 3. CPU, Memory, and Buses |
| Interrupt | A81 CPU | | Test 3. CPU, Memory, and Buses |
| Mult fctn peripheral | A81 CPU | | |
| Display digital | A81 CPU | | |
| DMA | A81 CPU | | |
| Math coprocessor | A81 CPU | | |
| HP-IB | A81 CPU A87/A88 Memory | | Test 33. Memory Battery |
| Disk controller | A81 CPU | | |
| IIC bus | see test log | | Test 6. IIC Bus |
| Fast bus | A81 CPU A62 ADC/Digital Filter | | Test 7. Fast Bus |
| Front panel | Front Panel | | |
| Disk motor [MOTOR] | A81 CPU Disk Drive | | Test 11. Disk Drive |
| Disk restore [RESTORE] | A81 CPU Disk Drive | | Test 11. Disk Drive |
| Disk random seek [RANDOM SEEK] | A81 CPU Disk Drive | | Test 11. Disk Drive |
| Disk sector seek [SEEK SECTOR] | A81 CPU Disk Drive | | Test 11. Disk Drive |
| Disk read [READ] | A81 CPU Disk Drive | | Test 11. Disk Drive |
| Disk read/write [READ/WRITE] | A81 CPU Disk Drive | | Test 11. Disk Drive |
| Disk read/write all [READ/WRITE ALL] | A81 CPU Disk Drive | | Test 11. Disk Drive |
| Digital filter gate array | A62 ADC/Digital Filter A32 300 MHz A33 Trigger | | Test 13. Digital Filter |
| Detector gate array | A62 ADC/Digital Filter A33 Trigger | | Test 13. Digital Filter |
| Source 187.5 kHz [187.5 kHz REFERENCE] | A42 Source Conversion A33 Trigger | | Test 14. Source |
| Source gilbert cell [GILBERT CELL] | A42 Source Conversion | | Test 14. Source |

Table 5-12. Self-Test Troubleshooting Guide (continued)

| Failing Self Test | Probable Faulty Assembly | Adjustment | Troubleshooting Test |
|---|---|--|-----------------------------|
| Mult loop tuning range | A51 Interpolation VCO A52 Fractional-N A33 Trigger | 4. Interpolation VCO | Test 16. Interpolation Loop |
| Single loop tuning range | A 21 Sum VCO A51 Interpolation VCO A52 Fractional-N A23 Step Phase Detector | 5. Single Loop Control Voltage Clamps | Test 17. Single Loop |
| "Local Oscillator Unlocked" message displayed | A51 Interpolation VCO A52 Fractional-N A21 Sum VCO A22 Sum Phase Detector A23 Step Phase Detector A24 Step VCO | | Test 15. Local Oscillator |
| Source output level [OUTPUT CKTS] | A41 Source Amplifier A42 Source Conversion A21 Sum VCO A22 Sum Phase Detector A23 Step Phase Detector A24 Step VCO A31 Reference/Calibrator A32 300 MHz | 10. Pretune Offset and Slope 13. Source Bandpass Filter | Test 14. Source |
| Receiver 2nd If [2ND IF LEVEL] | A61 IF A11 Input A12 First Conversion A13 Second Conversion A21 Sum VCO A32 300 MHz A41 Source Amplifier | 14. First IF Bandpass Filter | Test 18. Input Conversion |
| Receiver ADC [ADC] | A62 ADC/Digital Filter A24 Step VCO A31 Reference/Calibrator A51 Interpolation VCO A61 IF | 3. 300 MHz Reference VCO 12. Second IF Bandpass Filter 11. ADC Gain, Offset, and Reference | Test 18. Input Conversion |
| Post divider | A51 Interpolation VCO A21 Sum VCO | | Test 19. Sum Loop |
| Receiver autorange [AUTO RNG TRIP PTS] | A11 Input A41 Source Conversion | 15. Autorange Thresholds and 1 Meg Ohm Flatness 17. Calibrator Flatness and Level | Test 18. Input Conversion |
| Receiver 10 MHz [10 MHz LOCAL OSC] | A31 Reference/Calibrator A32 300 MHz A33 Trigger A21 Sum VCO A22 Sum Phase Detector A23 Step Phase Detector A24 Step VCO A51 Interpolation VCO A52 Fractional-N | 3. 300 MHz Reference VCO 14. First IF Bandpass Filter 12. Second IF Bandpass Filter | Test 21. Reference |
| Source flatness [FLATNESS] | A41 Source Amplifier A42 Source Conversion | | Test 14. Source |

Table 5-12. Self-Test Troubleshooting Guide (continued)

| Failing Self Test | Probable Faulty Assembly | Adjustment | Troubleshooting Test |
|--------------------------|---------------------------------|---|--|
| Quick confidence | | 3. 300 MHz Reference VCO 5. Single Loop Control Voltage Clamps 10. Pretune Offset and Slope 13. Source Bandpass Filter 14. First IF Bandpass Filter 12. Second IF Bandpass Filter 11. ADC Gain, Offset, and Reference | See "Troubleshooting Failing Performance Tests " |

Test 10. ALL Locks Analyzer

Use this test to continue troubleshooting if the analyzer locked up while running the functional test ALL.

1. Set the power switch to ON (I) and as soon as the graticule appears, disable the calibration routine by pressing the following keys:
 - [] (second softkey from bottom)
 - [] (second softkey from bottom)
 - [Spcl Fctn]
 - [AUTO CAL ON OFF]
2. Press the following keys (allow enough time for each test to complete before pressing the next key) until a test fails or the analyzer locks up:

Note



A failure may cause the self tests to run very slow. Wait one minute before assuming the analyzer is locked up.

[] (second softkey from bottom)
- 99
[] (second softkey from bottom)
[SERVICE FUNCTIONS]
[SELF TEST]
[TEST LOG]
[CANCEL/RETURN]
[FUNCTIONL TESTS]
[CPU]
[PROCESSOR]
[ROM]
[RAM]
[INTERRUPT]
[MULT FCTN PERIPHERL]
[DISPLAY DGTL HW]
[Spcl Fctn]
[SERVICE FUNCTIONS]
[SELF TEST]
[TEST LOG]
[CANCEL/RETURN]
[FUNCTIONL TESTS]
[DMA]
[MATH COPROC SSR]
[I/O]
[HP-IB]
[HP-IB FUNC TEST]
[ABORT/RETURN]

[INTERNAL DISK]
[DISK CONTROLLER]
[ABORT/RETURN]
[IIC BUS]
[FAST BUS]
[FRONT PANEL]
[ABORT/RETURN]
[RECEIVER]
[DIGITAL FILTER]
[DETECTOR]
[ABORT/RETURN]
[SOURCE]
[187.5 kHz REFERENCE]
[GILBERT CELL]
[ABORT/RETURN]
[LOCAL OSC]
[MULT-LOOP TUN RANGE]
[SNGL LOOP TUN RANGE]
[ABORT/RETURN]
[SOURCE]
[OUTPUT CKTS]
[ABORT/RETURN]
[RECEIVER]
[2ND IF LEVEL]
[ADC]
[ABORT/RETURN]
[LOCAL OSC]
[POST DIVIDER]
[ABORT/RETURN]
[RECEIVER]
[AUTO RNG TRIP PTS]
[10 MHz LOCAL OSC]
[ABORT/RETURN]
[SOURCE]
[FLATNESS]
[ABORT/RETURN]
[ABORT/RETURN]
[QUICK CONF TEST]

3. Locate the test that failed or locked up the analyzer in table 5-12. The table lists the probable faulty assembly and any recommended adjustment or troubleshooting procedure to do before replacing the assembly.

Test 11. Disk Drive

Use this test to isolate disk drive failures to the CPU assembly, the Disk Drive assembly, or the flexible disk.

Note



The assembly uses Logical Interchange Format (LIF), option 0-4. This is the same format used by the Series 200/300 BASIC system. To format a disk, press the following keys:

[Disk Util]
[DEFAULT DISK]
[INTERNAL DISK]
[CANCEL/RETURN]
[FORMAT DISK]

It takes about 1.5 minutes to format a disk.

1. Set the power switch to ON (I). Insert a formatted disk into the Disk Drive assembly and press the following keys:

[Spcl Fctn]
[] (second softkey from bottom)
- 99
[] (second softkey from bottom)
[SERVICE FUNCTIONS]
[SELF TEST]
[TEST LOG]
[CANCEL/RETURN]
[FUNCTIONL TESTS]
[I/O]
[INTERNAL DISK]
[ALL]

Note



This test takes about 20 minutes to complete if there are no failures.

2. If the Motor and Restore self tests pass and the Random Seek and Read self tests fail, the flexible disk is probably unformatted or faulty. If this occurs, use a different formatted disk and repeat step 1 to see if the error clears. Following is the typical error message when the disk is unformatted or faulty:

```
Seek to n went to n
rd data verify err sctr n
```

Where n is a sector number from 1 to 2464.

3. If the Disk Controller self test fails, the Disk Drive assembly or the CPU's disk drive controller is probably faulty. Before replacing the Disk Drive assembly, do the following to verify that the CPU's disk drive controller is operating correctly:
- Disconnect the power cord from the rear panel and place the Power Supply assembly in its test position. Remove the Memory assembly. See the disassembly/assembly illustrations in section II, "Replaceable Parts."
 - With the Memory assembly upside-down and outside the chassis, connect the memory cable. Be careful not to short the pins on back of the assembly.
 - Disconnect the disk drive cable (W4).
 - Connect the power cord and set the power switch to ON (I). Press the analyzer keys as follows:

[Spcl Fctn]

[] (second softkey from bottom)

- 99

[] (second softkey from bottom)

[SERVICE FUNCTIONS]

[SELF TEST]

[TEST LOG]

[CANCEL/RETURN]

[LOOP MODE ON OFF]

[FUNCTIONL TESTS]

[I/O]

[INTERNAL DISK]

[ALL]

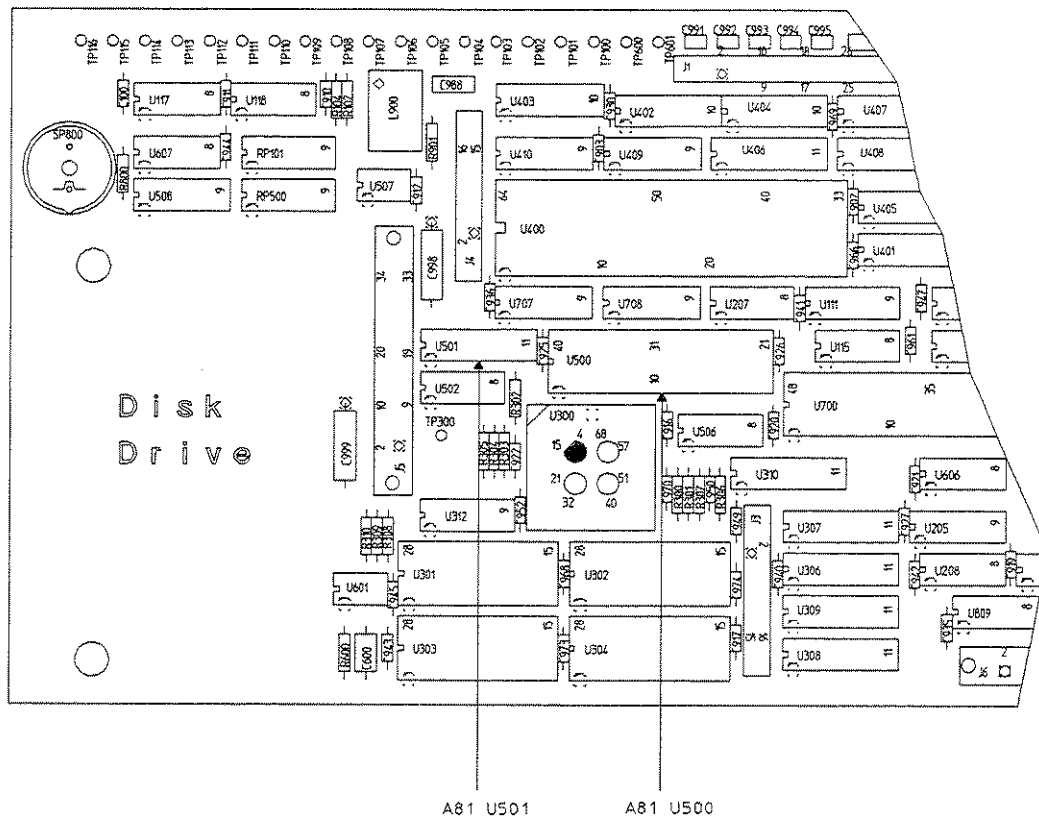
- e. Using a logic probe, check that the TTL signals in table 5-13 are toggling (see figure 5-14 for test locations).

Table 5-13. Disk Drive Control Signals

| Test Location | Signal Name | In/Out |
|---------------|-------------|--------------|
| A81 U500(19) | 8 MHz | A81 Internal |
| A81 U500(21) | 1 MHz | A81 Internal |
| A81 U500(28) | DS0 | A81 Internal |
| A81 U500(29) | DS1 | A81 Internal |
| A81 U500(22) | DW | A81 Internal |
| A81 U501(5) | MOTOR_ON\ | A81 Out |
| A81 U501(12) | WRITE_DATA\ | A81 Out |

- f. After checking the signals, press the following keys:

[ABORT/RETURN]
 [ABORT/RETURN]
 [ABORT/RETURN]
 [LOOP MODE ON OFF]



Test 12. HP-IB/RS-232

Use this test to separate HP-IB sub-block failures from HP-IB connector failures.

Note

The HP 3588A Spectrum Analyzer has an RS-232 connector, but it does not function.

1. Set the power switch to STANDBY (⓪) and remove the top cover (see the disassembly/assembly illustrations in section II, "Replaceable Parts").
2. Set the power switch to ON (I), then press the following keys:
 - [Spcl Fctn]
 - [] (second softkey from bottom)
 - 99
 - [] (second softkey from bottom)
 - [SERVICE FUNCTIONS]
 - [SELF TEST]
 - [FUNCTIONL TESTS]
 - [I/O]
 - [HP-IB]
 - [HP-IB FUNC TEST]
3. If the HP-IB self test fails, the HP-IB sub-block on the CPU assembly is probably faulty.
4. Press the [HP-IB CONNECTOR] softkey.
5. Using a small jumper, short each HP-IB connector pin to the HP-IB connector ground while watching the display. When a pin is grounded, the corresponding pin in the display should have a dot in it. If this test fails, the HP-IB connector is probably faulty.

Note

When pin 11 is grounded, the display should have a dot in ATN and may also have a dot in NDAC.

Test 13. Digital Filter

Use this test if the receiver is suspected of failing and all self tests listed before the Digital filter gate array in table 5-12 passed.

1. Using a spectrum analyzer (with frequency span set to ≤ 1 MHz) or an oscilloscope, check the signals in table 5-14 in the order listed. At the first incorrect signal, go to step 6.

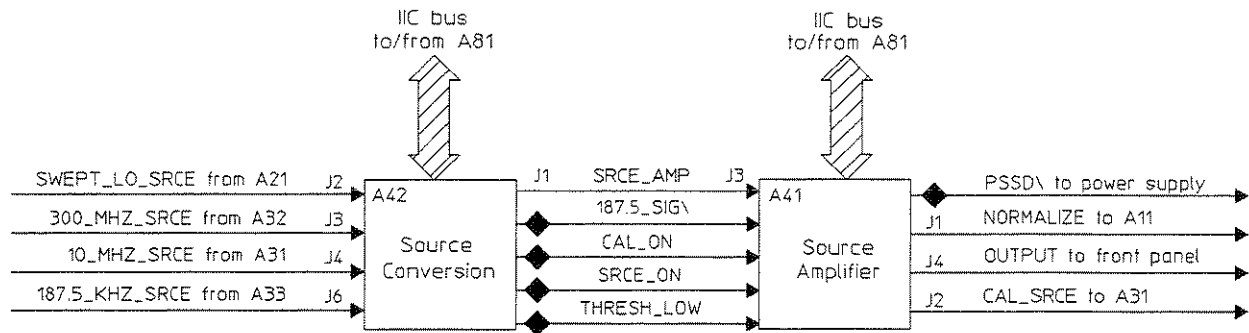
Table 5-14. ADC/Digital Filter Frequency Reference

| Test Location | Frequency | Amplitude | Output Impedance | Probable Faulty Assembly |
|---------------|-----------|-----------------|------------------|--------------------------|
| A31 J8 | 80 MHz | - 5 dBm (ECL) | 50 Ω | A31 Reference/Calibrator |
| A32 J2 | 60 MHz | - 2.5 dBm (ECL) | 50 Ω | A32 300 MHz |
| A33 J3 | 250 kHz | 3.3 Vp-p (TTL) | 1 M Ω | A33 Trigger |

2. Set the power switch to STANDBY (ϕ), and reconnect all cables.
3. Set the power switch to ON (1), and check that A62 DS804 (LSWP – yellow LED) is on and briefly blinking off.
4. If the LED is not blinking and the message dma ok using internal test mode was included in the self-test message, the A33 Trigger assembly is probably faulty. If the message was not included, the A62 Digital/Filter assembly is probably faulty. Before replacing an assembly, go to step 6 to check the voltages at the connector.
5. If the LED is blinking, the A62 ADC/Digital Filter assembly is probably faulty. Do the next step before replacing the assembly.
6. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:
 - a. Set the power switch to STANDBY (ϕ). Remove the suspected assembly and place an extender board in the card nest.
 - b. Set the power switch to ON (1), then check the pins of the extender board for correct voltages (see table 4-13 on page 4-59).

Test 14. Source

Use this test when the source is suspected of failing and all self tests listed before Source 187.5 kHz in table 5-12 passed.



ROUTED THROUGH THE MOTHERBOARD.

Figure 5-15. Source Block Diagram

Note

If a particular amplitude or frequency is failing, set the HP 3588A Spectrum Analyzer to the failing amplitude or frequency.

1. Press the following keys:

[**Preset**]

[**Sweep**]

[SWEEP AUTO **MAN**]

[MANUAL FREQ]

10 (or to the failing frequency)

[MHz]

[**Source**]

[SOURCE **ON** OFF]

[SOURCE AMPLITUDE]

10 (or to the failing amplitude)

[dBm]

2. Set the spectrum analyzer as follows:

| | |
|------------------|--------------------------------------|
| Center Frequency | 10 MHz (or to the failing frequency) |
| Frequency Span | 1 MHz |
| Input Impedance | 50Ω |

3. Connect the spectrum analyzer to A42 J1 using a BNC-to-SMB cable and compare the amplitude to table 5-15.

Table 5-15. Amplitude Settings and A42 J1 Amplitudes

| Amplitude Setting (dBm) | A42 J1 Amplitude (dBm ± 3 dB) |
|--------------------------------|-------------------------------|
| 10, 0, - 10, - 20, - 30, - 40 | - 41 |
| 9, - 1, - 11, - 21, - 31, - 41 | - 42 |
| 8, - 2, - 12, - 22, - 32, - 42 | - 43 |
| 7, - 3, - 13, - 23, - 33, - 43 | - 44 |
| 6, - 4, - 14, - 24, - 34, - 44 | - 45 |
| 5, - 5, - 15, - 25, - 35, - 45 | - 46 |
| 4, - 6, - 16, - 26, - 36, - 46 | - 47 |
| 3, - 7, - 17, - 27, - 37, - 47 | - 48 |
| 2, - 8, - 18, - 28, - 38, - 48 | - 49 |
| 1, - 9, - 19, - 29, - 39, - 49 | - 50 |
| - 50 | - 51 |
| - 51 | - 52 |
| - 52 | - 53 |
| - 53 | - 54 |
| - 54 | - 55 |
| - 55 | - 56 |
| - 56 | - 57 |
| - 57 | - 58 |
| - 58 | - 59 |
| - 59 | - 60 |
| - 59.9 | - 61 |

4. If the amplitude at A42 J1 is correct, do the following:

a. Set the power switch to STANDBY (⓪). Remove the screw at each end of the A41 Source Amplifier assembly, and place an extender board in the card nest.

b. Set the power switch to ON (I), and press the following keys:

[**Source**]

[SOURCE **ON** OFF]

- c. Check that pin 16B (SRCE_ON) on the extender board is a TTL level high. If pin 16B is a TTL high, the A41 Source Amplifier assembly is probably faulty. If pin 16B is not a TTL high, the A42 Source Conversion assembly is probably faulty. Before replacing the assembly, go to step 6 to check the voltages at the connector.
5. If the amplitude at A42 J1 is incorrect, do the following:
- Press the [**Preset**] hardkey.
 - Using a spectrum analyzer (with frequency span set to ≤ 1 MHz) or an oscilloscope, check the signals in table 5-16 in the order listed. At the first incorrect signal, go to step 6 if a probable faulty assembly is listed or to the recommended troubleshooting test.

Table 5-16. Source Reference Frequencies

| Test Location | Frequency | Amplitude | Output Impedance | Probable Faulty Assembly or Troubleshooting Test |
|---------------|--------------------------|-----------------------|------------------|--|
| A31 J4 | 10 MHz | - 3 dBm (ECL) | 50 Ω | A31 Reference/Calibrator |
| A31 J5 | 10 MHz | - 3 dBm (ECL) | 50 Ω | A31 Reference/Calibrator |
| A31 J9 | 20 MHz | - 3 dBm (ECL) | 50 Ω | A31 Reference/Calibrator |
| A32 J3 | 300 MHz | - 10 dBm | 50 Ω | A32 300 MHz |
| A32 J4 | 300 MHz | - 2 dBm | 50 Ω | A32 300 MHz |
| A33 J2 | 187.5 kHz | 600 mVp-p square wave | 50 Ω | A33 Trigger |
| A21 J2 | 310.1875 to 460.1875 MHz | - 10 dBm | 50 Ω | Test 17. Single Loop |

- c. If all the signals are correct, the A42 Source Conversion assembly is probably faulty. Before replacing the assembly, do the next step.
6. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:
- Set the power switch to STANDBY (⓪). Remove the screw at each end of the suspected assembly. Remove the assembly and place an extender board in the card nest.
 - Set the power switch to ON (I), then measure the pins of the extender board for correct voltages (see table 4-13 on page 4-59).

Test 15. Local Oscillator

Use this test when the “Local Oscillator Unlock” message appears on the screen and the following self tests passed:

- Digital filter gate array
- Detector gate array
- Mult loop tuning range
- Single loop tuning range

Note



The following procedure checks frequencies with a spectrum analyzer. However, if the failure mode requires more exact frequency measurements, use a frequency counter with $\pm 25 \times 10^{-3}$ Hz frequency accuracy.

1. Press the following keys:

```
[ Preset ]  
[ Freq ]  
  [ FULL SPAN ]  
[ Sweep ]  
  [ SWEEP AUTO MAN ]  
  [ MANUAL FREQ ]  
  0  
  [ Hz ]
```

2. Using a spectrum analyzer with 50 Ω input impedance, set its span to 50 MHz and connect to A51 J4. The signal at A51 J4 should be 41.875 MHz, -24 dBm \pm 3 dB. If the signal is incorrect, go to Test 16. Interpolation Loop.

3. Press the following keys:

```
[ Sweep ]  
  [ MANUAL FREQ ]  
  50  
  [ MHz ]
```

4. Connect the spectrum analyzer to A24 J2. The signal at A24 J2 should be 350 MHz, -24 dBm \pm 5 dB. If the signal at A24 J2 is incorrect, go to Test 20. Step Loop.
5. Connect the spectrum analyzer to A21 J3. The signal at A21 J3 should be 360.1875 MHz, 4 dBm \pm 3 dB. If the signal at A21 J3 is incorrect, go to Test 19. Sum Loop.

Test 16. Interpolation Loop

Use this test when the local oscillator's interpolation loop is suspected of failing and the following self tests passed:

- Digital filter gate array
- Detector gate array

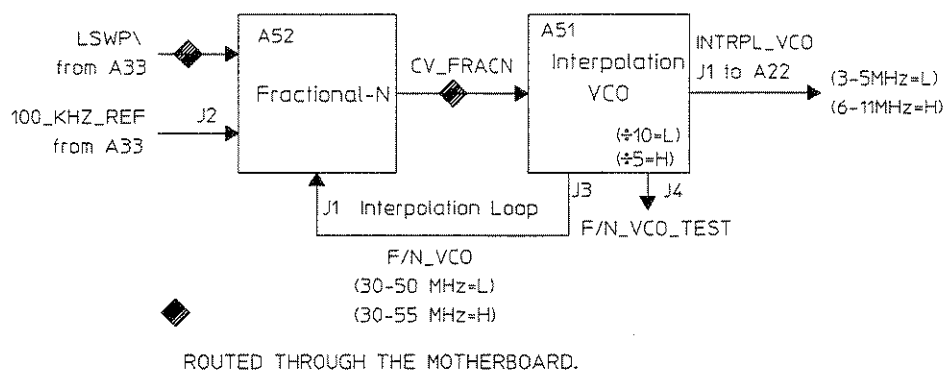


Figure 5-16. Local Oscillator Interpolation Loop

1. Using an oscilloscope with a 50 Ω input impedance, check that A33 J4 is a 100 kHz, TTL pulse.
2. If the signal at A33 J4 is incorrect, the A33 Trigger assembly is probably faulty. Before replacing the assembly, go to step 12 to check the voltages at the connector.
3. Set the power switch to STANDBY (ϕ). Remove the screw at each end of the A51 Interpolation VCO assembly, and remove the assembly. Move A51 J101 to its test position, and place the assembly on an extender board.
4. Set the power switch to ON (I), then press the following keys:

```

[ Freq ]
  [ FULL SPAN ]
[ Sweep ]
  [ SWEEP AUTO MAN ]
  [ MANUAL FREQ ]
  0
  [ Hz ]
  
```

5. Using a spectrum analyzer with 50Ω input impedance and the frequency span set to 50 MHz, check that A51 J4 is $55\text{ MHz} \pm 0.5\text{ MHz}$ with an output level of $-24\text{ dBm} \pm 3\text{ dB}$.
6. If the signal at A51 J4 is incorrect, the A51 Interpolation VCO assembly is probably faulty. Before replacing the assembly, go to step 12 to check the voltages at the connector.
7. Set the power switch to STANDBY (⓪). Remove the test jumper and connect a $\pm 10\text{ Vdc}$ supply to the center pin of A51 J101.
8. Connect a spectrum analyzer to A51 J4. Set it to a start frequency of 30 MHz and stop frequency of 55 MHz.
9. Set the power switch to ON (I), then press the following keys:
 - [Freq]
 - [FULL SPAN]
 - [Sweep]
 - [SWEEP AUTO **MAN**]
 - [MANUAL FREQ]
 - 0
 - [Hz]
10. Vary the dc voltage from +10V to 0V while monitoring A51 J4. The frequency should vary between 30 MHz and 55 MHz as the dc voltage is varied. The output level should be $-24\text{ dBm} \pm 3\text{ dB}$.
11. If the signal at A51 J4 is correct, the A52 Fractional-N assembly is probably faulty. If the signal at A51 J4 is incorrect, the A51 Interpolation VCO assembly is probably faulty. Before replacing the assembly, go to step 12 to check the voltages at the connector.
12. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:
 - a. Set the power switch to STANDBY (⓪). Remove the suspected assembly and place an extender board in the card nest.
 - b. Set the power switch to ON (I), then check the pins of the extender board for correct voltages (see table 4-13 on page 4-59).

Test 17. Single Loop

Use this test when the local oscillator is suspected of failing in single loop mode and the following self tests passed:

- Digital filter gate array
- Detector gate array
- Mult loop tuning range

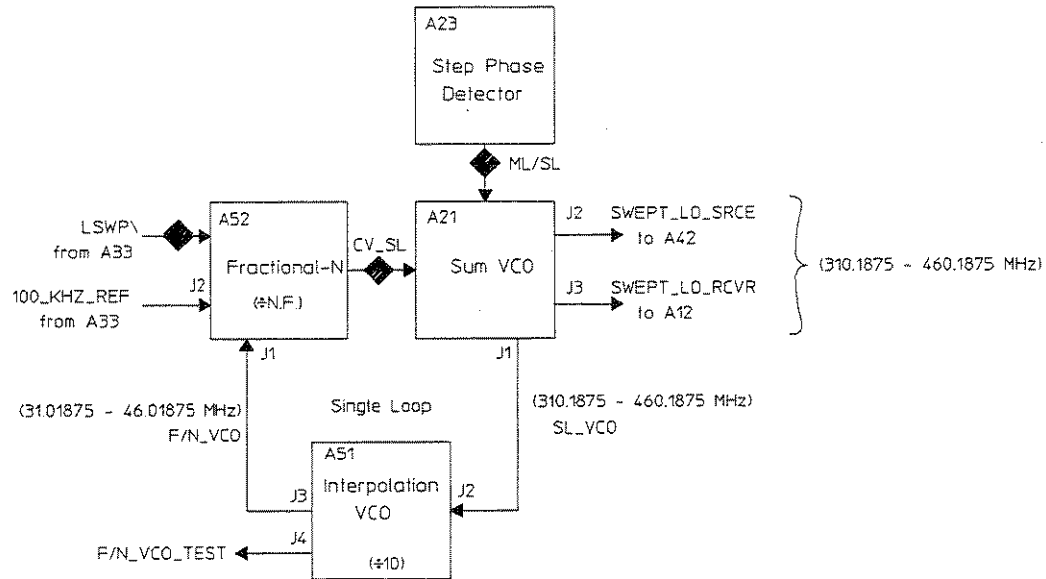


Figure 5-17. Local Oscillator in Single Loop Mode

1. Press the [Preset] key, then check the signals in table 5-17 using a spectrum analyzer.

Table 5-17. Single Loop Output Frequencies

| Test Location | Frequency | Amplitude (± 3 dBm) | Output Impedance |
|---------------|----------------|--------------------------|------------------|
| A21 J2 | 310 to 460 MHz | - 10 dBm | 50 Ω |
| A21 J3 | 310 to 460 MHz | + 4 dBm | 50 Ω |
| A51 J4 | 31 to 46 MHz | - 24 dBm | 50 Ω |

2. If all the signals are correct, the local oscillator is operating correctly in single loop mode. Go to Test 19. Sum Loop.

3. If the signal at A51 J4 is 31 to 46 MHz, but the signal at A21 J2 or A21 J3 is incorrect, the A21 Sum VCO assembly is probably faulty. Before replacing the assembly, go to step 16 to check the loop mode control signal.
4. Set the power switch to STANDBY (⓪). Remove the screw at each end of the A21 Sum VCO assembly, and remove the assembly. Move A21 J201 to its test position, and place the assembly on an extender board.
5. Set the power switch to ON (I). Check the signals in table 5-18 using a spectrum analyzer with the frequency span set to 50 MHz.

Table 5-18. Single Loop Output Frequencies in Test Mode

| Test Location | Frequency (± 10 MHz) | Amplitude (± 3 dBm) | Output Impedance | Probable Faulty Assembly |
|---------------|----------------------|---------------------|------------------|--------------------------|
| A21 J1 | 445 MHz | +3 dBm | 50Ω | A21 Sum VCO |
| A21 J2 | 445 MHz | - 10 dBm | 50Ω | A21 Sum VCO |
| A21 J3 | 445 MHz | +4 dBm | 50Ω | A21 Sum VCO |

6. If a signal is incorrect, go to step 16 to check the loop mode control signal.
7. Set the power switch to STANDBY (⓪). Remove the jumper from A21 J201, and connect a ± 10 Vdc supply to the center pin of A21 J201.
8. Connect a spectrum analyzer to A21 J1 and set its frequency span for 300 to 470 MHz.
9. Set the power switch to ON (I). While monitoring A21 J1, vary the dc voltage from +7V to - 1V. The signal at A21 J1 should vary between 310 and 460 MHz as the dc voltage is varied.
10. If the signal is correct, check that A21 J2 and A21 J3 vary between 310 and 460 MHz as the dc voltage is varied. The amplitudes should be the same as listed in the previous table.
11. If the signal at A21 J1, J2, or J3 is incorrect, the A21 Sum VCO assembly is probably faulty. Before replacing the assembly, go to step 16 to check the loop mode control signal.
12. Using an extender cable, connect A21 J1 to A51 J2.
13. Connect the spectrum analyzer to A51 J4 and change its start frequency to 30 MHz and its stop frequency to 50 MHz.
14. Vary the dc voltage while monitoring A51 J4. The signal should vary between 31 and 46 MHz as the dc voltage is varied. The output level should be - 24 dBm ± 3 dB.
15. If the signal at A51 J4 is correct, the A52 Fractional-N assembly is probably faulty. If the signal is incorrect, the A51 Interpolation VCO assembly is probably faulty. Before replacing the assembly, go to step 17 to check the voltages at the connector.

16. Before replacing the A21 Sum VCO assembly, do the following:
 - a. Set the power switch to STANDBY (⓪). Remove the screws at each end of the A21 Sum VCO assembly and remove the assembly. Place an extender board in the card nest.
 - b. Set the power switch to ON (1), then check that A21 J100 pin 8 (ML/SL) is a TTL level high. If it is not, the A23 Step Phase Detector assembly is probably faulty. Before replacing the assembly, do the next step.
17. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:
 - a. Set the power switch to STANDBY (⓪). Remove the suspected assembly and place an extender board in the card nest.
 - b. Set the power switch to ON (1), then check the pins of the extender board for correct voltages (see table 4-13 on page 4-59).

Test 18. Input Conversion

Use this test when the receiver is suspected of failing and all self tests listed before the Receiver 2nd If in table 5-12 passed.

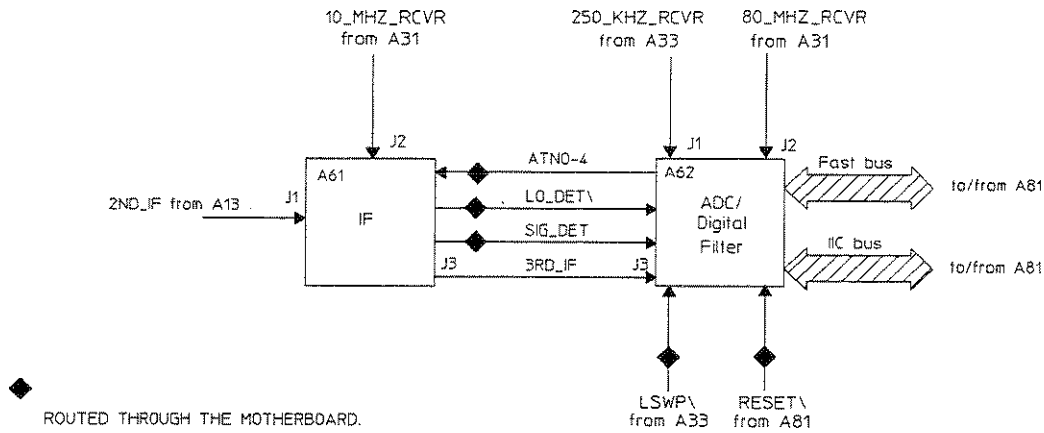


Figure 5-18. IF/ADC Block Diagram

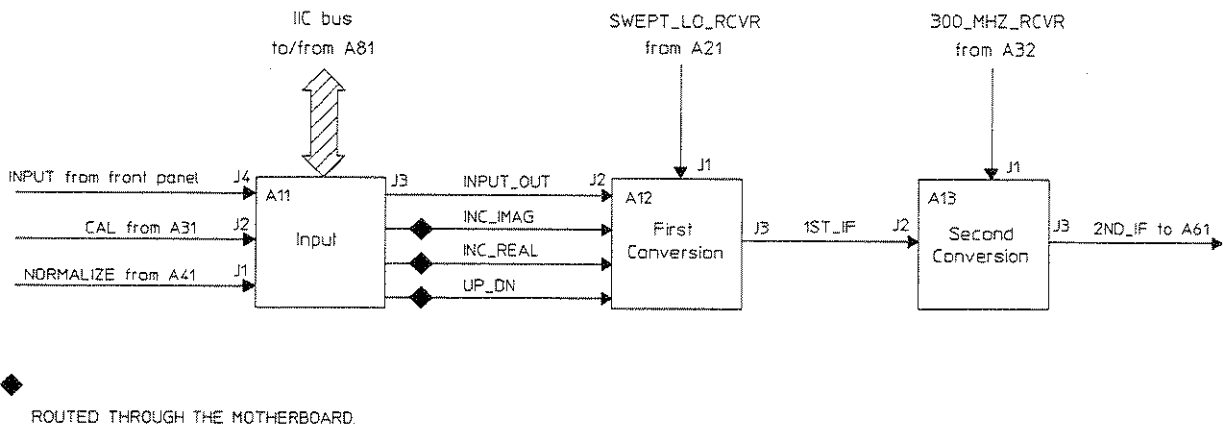


Figure 5-19. Input Conversion Block Diagram

1. Connect the signal generator to the front panel INPUT connector using a BNC cable.
2. Set the signal generator as follows:

| | |
|-----------|----------|
| Frequency | 10 MHz |
| Amplitude | - 20 dBm |
3. Press the following keys:
 - [Preset]
 - [Spcl Fctn]
 - [AUTO CAL ON **OFF**]
 - [Range/Input]
 - [RANGE]
 - 20
 - [dBm]
 - [Sweep]
 - [SWEEP AUTO **MAN**]
 - [MANUAL FREQ]
 - 10
 - [MHz]
4. Check the signals in table 5-19 using a spectrum analyzer with the frequency span set to ≤ 1 MHz. After checking a signal, reconnect the disconnected cable before checking the next signal. At the first incorrect signal, go to the recommended test or to step 34 if an assembly is listed as faulty.

Table 5-19. Input Conversion References and Signals

| Test Location | Frequency | Amplitude (± 3 dB) | Output Impedance | Probable Faulty Assembly or Next Test |
|---------------|--------------|-------------------------|------------------|---------------------------------------|
| A11 J3 | 10 MHz | - 28 dBm | 50 Ω | A11 Input |
| A21 J3 | 320.1875 MHz | 4 dBm | 50 Ω | Test 19. Sum Loop |
| A12 J3 | 310.1875 MHz | - 30 dBm | 50 Ω | A12 First Conversion |
| A32 J5 | 300 MHz | 0 dBm | 50 Ω | A32 300 MHz |
| A13 J3 | 10.1875 MHz | - 37 dBm | 50 Ω | A13 Second Conversion |
| A31 J3 | 10 MHz | - 3 dBm | 50 Ω | A31 Reference/Calibrator |
| A61 J3 | 187.5 kHz | +7 dBm | 50 Ω | Step 20 |
| A51 J1 | 4.1875 MHz | - 5 dBm | 50 Ω | A51 Interpolation VCO |

5. If the signals in step 4 were correct and the Receiver 2nd IF self test passed, go to step 25.
6. Change the signal generator's amplitude to 0 dBm.
7. Press the following keys:
 - [Range/Input]
 - [1 MEGOHM]

22
8. Connect the spectrum analyzer to A11 J3. The signal at A11 J3 should be 10 MHz, $-28 \text{ dBm} \pm 3 \text{ dB}$. If the signal is incorrect, the A11 Input assembly is probably faulty. Before replacing the assembly, go to step 34 to check the voltages at the connector.

9. Press the following keys:

[Range/Input]
[50 OHMS]
[RANGE]
- 10
[dBm]

10. Change the signal generator's amplitude to -10 dBm .

286
11. The signal at A11 J3 should be 10 MHz, $-28 \text{ dBm} \pm 3 \text{ dB}$. If the signal is incorrect, the A11 Input assembly is probably faulty. Before replacing the assembly, go to step 34 to check the voltages at the connector.

12. Change the signal generator's amplitude to 10 dBm .

13. Press the following keys:

[RANGE]
10
[dBm]

297
14. The signal at A11 J3 should be 10 MHz, $-28 \text{ dBm} \pm 3 \text{ dB}$. If the signal is incorrect, the A11 Input assembly is probably faulty. Before replacing the assembly, go to step 34 to check the voltages at the connector.

15. Change the signal generator's amplitude to 5 dBm .

16. Connect the spectrum analyzer to A61 J3 and reconnect A11 J3 to A12 J2 using the original cable.

17. Press the following keys:

[Spcl Fctn]
[] (second softkey from bottom)
- 99
[] (second softkey from bottom)
[SERVICE FUNCTIONS]
[SPCL TEST MODES]
[IF ATTEN]
16
[dB]

18. Adjust the signal generator's amplitude for a spectrum analyzer readout of $6.00 \text{ dBm} \pm 0.05 \text{ dB}$ at 187.5 kHz (spectrum analyzer's frequency span is 20 kHz).

19. Press the following keys:

[IF ATTEN]
15
 [dB]

20. The spectrum analyzer should now read $7.0 \text{ dBm} \pm 0.3 \text{ dB}$. If the signal at A61J3 is correct, go to step 21. If the signal at A61J3 is incorrect, do the following to check the A31 10 MHz Cal signal:

- a. Press the following keys:

[Preset]
 [Spcl Fctn]
 [PRFM TESTS]
 [CALIBRATR TO INPUT]

- b. Check the signal at A31 J1 for 10 MHz, $-20 \text{ dBm} \pm 3 \text{ dB}$ using a spectrum analyzer. If the signal is incorrect, the A31 Reference/Calibrator assembly is probably faulty, go to step 34 to check the voltages at the connector.

21. Do the following to check the attenuator control from the A62 ADC/Digital Filter assembly:

- a. Set the power switch to STANDBY (ϕ). Remove the screws at each end of the A61 IF assembly and remove the assembly. Place an extender board in the card nest.

- b. Set the power switch to ON (I), then press the following keys:

[Range]
 [AUTORANGE ON **OFF**]
 [Spcl Fctn]
 [] (second softkey from bottom)
 - 99
 [] (second softkey from bottom)
 [AUTO CAL ON **OFF**]
 [SERVICE FUNCTIONS]
 [SPCL TEST MODES]
 [IF ATTEN]
0
 [dB]

- c. Check that pins 1A, 1B, 1C, 2A, and 2B on the extender board are a TTL level low. If they are incorrect, the A62 ADC/Digital Filter assembly is probably faulty. Before replacing the assembly, go to step 34 to check the voltages at the connector.

- d. Press the following keys:

[IF ATTEN]
31
 [dB]

- e. Check that pins 1A, 1B, 1C, 2A, and 2B on the extender board are a TTL level high. If they are incorrect, the A62 ADC/Digital Filter assembly is probably faulty. If they are correct,

the A61 IF assembly is probably faulty. Before replacing the assembly, go to step 34 to check the voltages at the connector.

22. Disconnect the cable connecting the signal generator to the INPUT connector.

23. Press the following keys:

[Preset]
[Range/Input]
[AUTORANGE ON **OFF**]
[Spcl Fctn]
[AUTO CAL ON **OFF**]
[SERVICE FUNCTIONS]
[SPCL TEST MODES]
[RECEIVER INPUT]
[CONNCT TO SOURCE]
[Sweep]
[SWEEP AUTO **MAN**]
[MANUAL FREQ]
10
[MHz]

24. Connect the spectrum analyzer to A41 J1 and reconnect A61 J3 to A62 J3 using the original cable.

25. The signal at A41 J1 should be 10 MHz, $-10 \text{ dBm} \pm 3 \text{ dB}$. If the signal is incorrect, the A41 Source Amplifier assembly is probably faulty. Before replacing the assembly, go to step 34 to check the voltages at the connector.

26. Press the following keys:

[Preset]
[Spcl Fctn]
[]
-99
[]
[AUTO CAL ON **OFF**]
[SERVICE FUNCTIONS]
[SPCL TEST MODES]
[RECEIVER INPUT]
[CONNCT TO CALIBRATR]

27. Connect the spectrum analyzer to A31 J1 and reconnect A41 J1 to A11 J1 using the original cable.

28. The signal at A31 J1 should be 10 MHz, $-20 \text{ dBm} \pm 3 \text{ dB}$. If the signal is incorrect, the A31 Reference/Calibrator assembly is probably faulty. Before replacing the assembly, go to step 34 to check the voltages at the connector.

29. Press the following keys:
 - [CANCEL/RETURN]
 - [CALIBRATR SWPT]
30. Connect the spectrum analyzer to A41 J2 and reconnect A31 J1 to A11 J2 using the original cable.
31. The signal at A41 J2 should be 200 kHz to 150 MHz, – 12 dBm. If the signal is incorrect, the A41 Source Amplifier assembly is probably faulty. Before replacing the assembly, go to step 34 to check the voltages at the connector.
32. Connect the spectrum analyzer to A31 J1 and reconnect A41 J2 to A31 J2 using the original cable.
33. The signal at A31 J1 should be 200 kHz to 150 MHz, – 20 dBm. If the signal is incorrect, the A31 Reference/Calibrator assembly is probably faulty. Before replacing the assembly, go to step 34 to check the voltages at the connector.
34. If all the signals in the previous steps are correct, the A62 ADC/Digital Filter assembly is probably faulty. Do the next step before replacing the assembly.
35. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:
 - a. Set the power switch to STANDBY (0). Remove the screw at each end of the suspected assembly. Remove the assembly and place an extender board in the card nest.
 - b. Set the power switch to ON (1), then measure the pins of the extender board for correct voltages (see table 4-13 on page 4-59).

Test 19. Sum Loop

Use this test when the local oscillator is suspected of failing in multiple loop mode and the following self tests passed.

- Digital filter gate array
- Detector gate array
- Mult loop tuning range

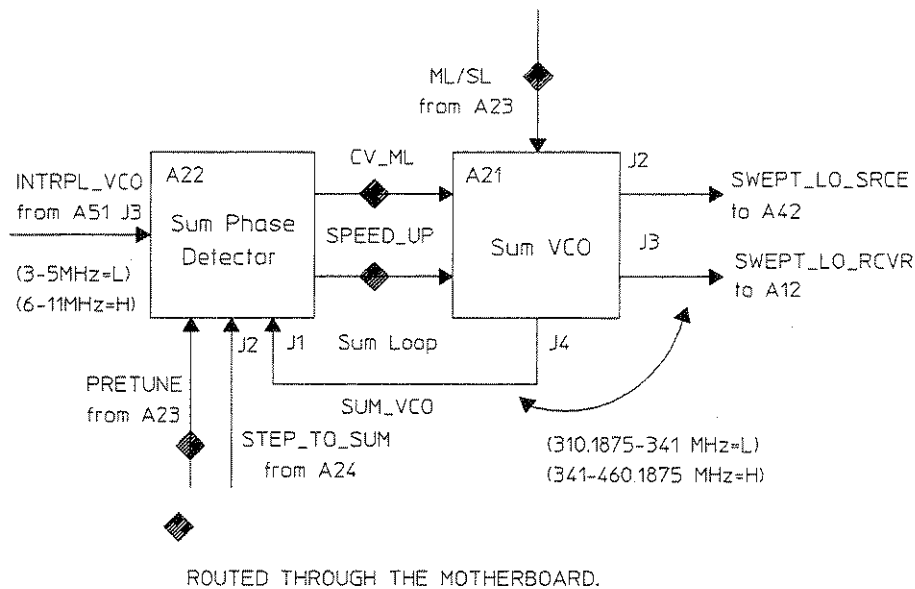


Figure 5-20. Local Oscillator Sum Loop

1. Set the power switch to ON (1), then press the following keys:

```
[ Spcl Fctn ]
[ SINGLE CAL ]
[ AUTO CAL ON OFF ]
[   ] (second softkey from bottom)
- 99
[   ] (second softkey from bottom)
[ SERVICE FUNCTIONS ]
[ SPCL TEST MODES ]
[ LOCAL OSC CONFIG ]
[ LOCAL OSC SNGL MULT ]
```

- Using a spectrum analyzer, check the signals in table 5-20 in the order listed. At the first incorrect signal, go to the recommended test or to step 14 if an assembly is listed as faulty.

Table 5-20. Sum Loop Reference Frequencies

| Test Location | Frequency | Amplitude (± 3 dB) | Output Impedance | Probable Faulty Assembly or Next Test |
|---------------|--------------------------|-------------------------|------------------|---------------------------------------|
| A24 J2 | 306 to 450 MHz | - 24 dBm | 50 Ω | Test 20. Step Loop |
| A24 J1 | 306 to 450 MHz | - 8 dBm | 50 Ω | A24 Step VCO |
| A51 J1 | 3 to 11 MHz ¹ | - 3 dBm (ECL) | 50 Ω | A51 Interpolation VCO |

¹ There is a noticeable jump in the sweep between 5 and 6 MHz as the signal changes between 'L' and 'H' settings. This occurs at an input frequency of approximately 30.8125 MHz.

- Set the power switch to STANDBY (ϕ). Remove the screw at each end of the A22 Sum Phase Detector assembly, and lift the assembly up about one inch.
- Remove the screw at each end of the A21 Sum VCO, and place the assembly on an extender board.
- Connect a ± 10 V dc supply to A21 CVML (ground is at TP2).
- Set the spectrum analyzer's frequency span to 300 MHz to 470 MHz and connect its 50 Ω input to A21 J4.
- Set the power switch to ON (I), then press the following keys:
 - [Spcl Fctn]
 - [SINGLE CAL]
 - [AUTO CAL ON **OFF**]
 - [] (second softkey from bottom)
 - 99
 - [] (second softkey from bottom)
 - [SERVICE FUNCTIONS]
 - [SPCL TEST MODES]
 - [LOCAL OSC CONFIG]
 - [LOCAL OSC SNGL **MULT**]
- Vary the dc voltage from +7V to - 1V while monitoring A21 J4. The frequency should vary between 310 MHz to 460 MHz as the dc voltage is varied. The output level should be +8 dBm ± 3 dB.
- If the signal at A21 J4 is correct, the A22 Sum Phase Detector assembly is probably faulty. Before replacing the assembly, go to step 14 to check the voltages at the connector. If the signal at A21 J4 is incorrect, the A21 Sum VCO assembly is probably faulty. Before replacing the assembly, go to step 13 to check control signals.

10. Remove the dc supply from A21 TP1.
11. Set the power switch to STANDBY (⓪), then push the A22 Sum Phase Detector assembly back into the card nest.
12. Set the power switch to ON (|), then press the following keys:
 - [Spcl Fctn]
 - [SINGLE CAL]
 - [AUTO CAL ON **OFF**]
 - [] (second softkey from bottom)
 - 99
 - [] (second softkey from bottom)
 - [SERVICE FUNCTIONS]
 - [SPGL TEST MODES]
 - [LOCAL OSC CONFIG]
 - [LOCAL OSC SNGL **MULT**]
13. Before replacing the A21 Sum VCO assembly, check the signals in table 5-21.

Table 5-21. Sum Loop Control Signals

| Signal Name | Test Location | Amplitude | Probable Faulty Assembly |
|-------------|----------------|----------------------|--------------------------|
| ML/SL | A21 J100 pin 8 | TTL Low | A23 Step Phase Detector |
| SPEED-UP | A21 J100 pin 7 | TTL Low ¹ | A22 Sum Phase Detector |

¹ The signal occasionally pulses high. In manual sweep the signal is always low.

14. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:
 - a. Set the power switch to STANDBY (⓪). Remove the suspected assembly and place an extender board in the card nest.
 - b. Set the power switch to ON (|), then check the pins of the extender board for correct voltages (see table 4-13 on page 4-59).

Test 20. Step Loop

Use this test when the local oscillator is suspected of failing in multiple loop mode and the following self tests passed.

- Digital filter gate array
- Detector gate array
- Mult loop tuning range

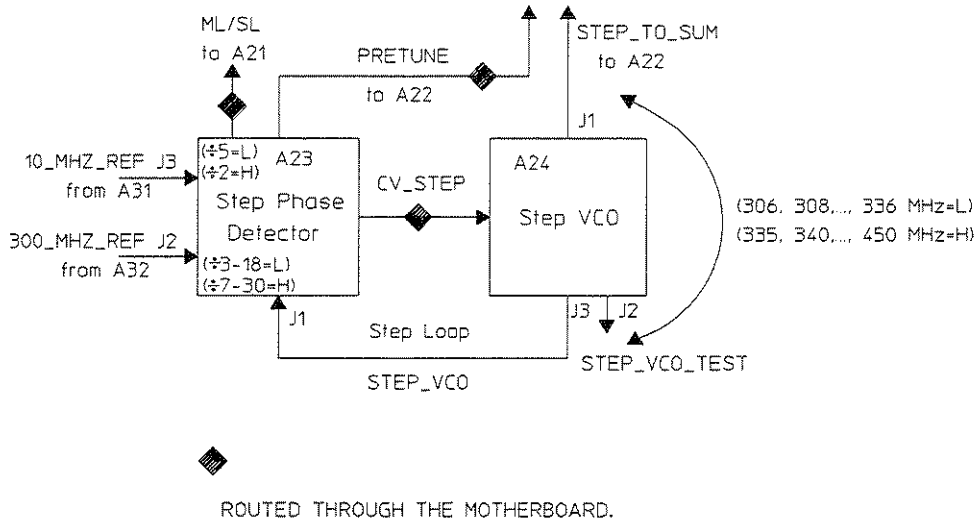


Figure 5-21. Local Oscillator Step Loop

1. Using a spectrum analyzer with the frequency span set to ≤ 1 MHz, check the signals in table 5-22 in the order listed. At the first incorrect signal, go to step 10.

Table 5-22. Step Loop Reference Frequencies

| Test Location | Frequency | Amplitude (± 3 dB) | Output Impedance | Probable Faulty Assembly |
|---------------|-----------|-------------------------|------------------|--------------------------|
| A31 J9 | 20 MHz | - 3 dBm (ECL) | 50 Ω | A31 Reference/Calibrator |
| A31 J4 | 10 MHz | - 3 dBm (ECL) | 50 Ω | A31 Reference/Calibrator |
| A32 J4 | 300 MHz | - 2 dBm | 50 Ω | A32 300 MHz |

2. Set the power switch to STANDBY (ϕ). Remove the screw at each end of the A24 Step VCO assembly, and remove the assembly. Move A24 J200 to its test position, and place the assembly on an extender board.

3. Set the power switch to ON (I), then press the following keys:
 - [Freq]
 - [FULL SPAN]
 - [Sweep]
 - [SWEEP AUTO **MAN**]
 - [MANUAL FREQ]
 - 0
 - [Hz]
4. Using a spectrum analyzer with 50Ω input impedance and the frequency span set to 50 MHz, check that A24 J3 is about 450 MHz ± 40 MHz and its output level is about +10 dBm ± 5 dB.
5. If the signal at A24 J3 is incorrect, the A24 Step VCO assembly is probably faulty. Before replacing the assembly, go to step 10 to check the voltages at the connector.
6. Set the power switch to STANDBY (⓪). Remove the test jumper and connect a ± 10V dc supply to the center pin of A24 J200.
7. Set the spectrum analyzer's frequency span to 300 MHz to 470 MHz and connect its 50Ω input to A24 J3.
8. Set the power switch to ON (I). Vary the dc voltage from +7V to - 1V while monitoring A24 J3. The frequency should vary between 306 MHz and 450 MHz as the dc voltage is varied. The output level should be +10 dBm ± 5 dB.
9. If the signal at A24 J3 is correct, the A23 Step Phase Detector assembly is probably faulty. If the signal at A24 J3 is incorrect, the A24 Step VCO assembly is probably faulty. Do the next step before replacing the assembly.
10. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector.
 - a. Set the power switch to STANDBY (⓪). Remove the suspected assembly and place an extender board in the card nest.
 - b. Set the power switch to ON (I), then check the pins of the extender board for correct voltages (see table 4-13 on page 4-59).

Test 21. Reference

Use this test when reference signals are suspected of failing and the following self tests passed:

- Receiver 2nd If
- Receiver ADC
- Post divider
- Receiver autorange

Note



The following procedure checks frequencies with a spectrum analyzer. However, if the failure mode requires more exact frequency measurements, use a frequency counter with $\pm 25 \times 10^{-3}$ Hz frequency accuracy.

1. If the analyzer has option 001 (Precision Frequency Reference), do the following:
 - a. Remove the rear panel jumper connecting OVEN REF OUT to EXT REF IN.
 - b. Connect the spectrum analyzer's 50 Ω input to OVEN REF OUT and check that it is 10 MHz, +3 dBm \pm 3 dB. If the signal is incorrect, do the following:
 - i. Set the power switch to STANDBY (ϕ), and disconnect the power cord from the rear panel. Remove the rear panel and fan/oven housing (see figures 2-4 and 2-11 in section II, "Replaceable Parts").
 - ii. Disconnect the connector with the yellow, red, and black wires from the A91 Fan Power/Oven assembly (see figure 2-12).
 - iii. Set the power switch to ON (I). Check that the voltage at the yellow wire is $-18 \pm 2V$ and the voltage at the red wire is $+18 \pm 2V$. If either voltage is incorrect, the motherboard or the wire is probably faulty. If the voltages are correct, the A91 Fan Power/Oven assembly is probably faulty.
2. Set the synthesizer as follows:

| | |
|-----------|--------|
| Frequency | 10 MHz |
| Amplitude | 5 dBm |
3. Connect the synthesizer to the rear panel EXT REF IN connector.
4. Using a spectrum analyzer with the frequency span set to ≤ 1 MHz, check the signals in table 5-23 in the order listed. At the first incorrect signal, go to step 15.

Table 5-23. Reference/Calibrator Signals

| Test Location | Frequency | Amplitude (± 3 dB) | Output Impedance | Probable Faulty Assembly |
|---------------|-----------|-------------------------|------------------|----------------------------|
| A31 J8 | 80 MHz | - 5 dBm | 50 Ω | A31 Reference/Calibrator † |
| A31 J6 | 10 MHz | +3 dBm | 50 Ω | A31 Reference/Calibrator |
| A31 J9 | 20 MHz | - 3 dBm | 50 Ω | A31 Reference/Calibrator |

† Before replacing this assembly, check adjustment 2. 80 MHz Reference VCXO.

- Repeatedly check the signals in table 5-23 but set the synthesizer's frequency to 1 MHz, then 2 MHz, and finally 5 MHz.

Note



The analyzer may not be able to lock to a low frequency signal connected to EXT REF IN.

- Again check the signals in table 5-23 but set the synthesizer's amplitude to - 5 dBm, then to +10 dBm.
- Disconnect the synthesizer from the EXT REF IN connector and on analyzer's with option 001, reconnect the rear panel jumper (EXT REF IN to OVEN REF OUT).
- Using a BNC cable, connect REF OUT to the spectrum analyzer's 10 MHz reference input.
- Press the following keys:
 - [Spcl Fctn]
 - [PRFM TESTS]
 - [CALIBRATR TO INPUT]
- Using a spectrum analyzer with the frequency span set to ≤ 1 MHz, check the signals in table 5-24 in the order listed. At the first incorrect signal, go to step 15.

Table 5-24. 300 MHz, Calibrator and Trigger Signals

| Test Location | Frequency | Amplitude (± 3 dB) | Output Impedance | Probable Faulty Assembly |
|---------------|-----------|-------------------------|------------------|--------------------------|
| A32 J4 | 300 MHz | - 2 dBm | 50 Ω | A32 300 MHz |
| A32 J5 | 300 MHz | 0 dBm | 50 Ω | A32 300 MHz |
| A31 J1 | 10 MHz | - 20 dBm | 50 Ω | A31 Reference/Calibrator |
| A32 J2 | 60 MHz | - 3 dBm | 50 Ω | A32 300 MHz |
| A33 J3 | 250 kHz | 13 dBm | 50 Ω | A33 Trigger |

11. Press the following keys:

- [Preset]
- [Freq]
- [FULL SPAN]
- [Sweep]
- [SWEEP AUTO MAN]

12. For each of the following manual frequencies in table 5-25, set [MANUAL FREQ] to the frequency in the table and check the signal at A21 J3 using a spectrum analyzer.

Table 5-25. Sum VCO Frequencies

| Manual Frequency | A21 J3 Frequency | A21 J3 Amplitude |
|------------------|------------------|-------------------|
| 0 Hz | 310.1875 MHz | +4 dBm \pm 3 dB |
| 30.8125 MHz | 341.0 MHz | +4 dBm \pm 3 dB |
| 150 MHz | 460.1875 MHz | +4 dBm \pm 3 dB |

13. If the frequency at A21 J3 was incorrect for all manual frequencies, go to Test 17. Single Loop.

14. If the frequency at A21 J3 was correct for some manual frequencies and incorrect for others, do the following:

- a. Set [MANUAL FREQ] to a frequency that produced an incorrect frequency at A21 J3.
 - b. In table 4-1 on page 4-18, locate the manual frequency in the Measurement Freq column. (Table 4-1 lists the frequencies of the different loops for all measurement frequencies.)
 - c. Check the frequency of A51 J1 and compare to the Intrpl VCO frequency in table 4-1.
 - d. If the frequency at A51 J1 is incorrect, go to Test 16. Interpolation Loop.
 - e. Check the frequency of A24 J2 and A24 J1, and compare to the Step VCO frequency in table 4-1.
 - f. If the frequency at A24 J2 or A24 J1 is incorrect, go to Test 20. Step Loop.
15. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector.
- a. Set the power switch to STANDBY (⓪). Remove the suspected assembly and place an extender board in the card nest.
 - b. Set the power switch to ON (I), then check the pins of the extender board for correct voltages (see table 4-13 on page 4-59).

Test 22. Intermittent Failures

Use this test to isolate intermittent failures to the assembly.

1. Check the common reasons for intermittent failures in table 5-26. If it's possible that your intermittent failure is caused by one of the common reasons given in the table, then follow the recommended troubleshooting procedure.

Table 5-26. Common Reasons for Intermittent Failures

| Common Reasons | Troubleshooting Procedure |
|-------------------------|--|
| Loose screws and cables | Check that the screws in the analyzer are tight and that the cables are firmly in their sockets. This is especially important since grounding for the analyzer depends on the cables and screws. |
| Power supply voltages | Check for correct power-supply voltages. See Test 1. Initial Verification |
| Out-of-adjustment | Do the adjustments for the analyzer in section I |
| Air flow restricted | The analyzer cools by drawing air from both side and blowing it out the back panel. Check that the air flow was not restricted in these areas when the failure occurred. |
| External voltage | Verify that the line voltage is within the electrical specification for the analyzer. See chapter 2 in the <i>HP 3588A Performance Test Guide</i> . |

Caution



Do not install a disk in the Disk Drive assembly. Running the disk in loop mode will wear out the disk drive head.

2. Set the power switch to ON (I), then press the following keys:

[Spcl Fctn]

[] (second softkey from bottom)

– 99

[] (second softkey from bottom)

[SERVICE FUNCTIONS]

[SELF TEST]

[LOOP MODE **ON** OFF]

[FUNCTIONL TESTS]

[ALL]

3. After this test detects a failure, press the following keys:

[ABORT/RETURN]

[LOOP MODE ON **OFF**]

4. Compare table 5-12 on page 5-33 to the test log. If the analyzer's test log matches more than one entry on the table, use the entry closest to the beginning of the table. The table lists the probable faulty assembly or assemblies and any recommended adjustment or troubleshooting procedure to do before replacing the assembly. If both an adjustment and a test are recommended, do the adjustment first.

Note

All pass, fail, and abort messages are displayed on the test log along with the number of times a test passes, fails, or aborts.

When loop mode is activated, the analyzer continually repeats a test until power is cycled or loop mode is aborted by pressing [ABORT/RETURN]. If the power is cycled, the information in the test log is lost.

During some tests the keyboard is not active and loop mode cannot be aborted. If this occurs, wait for the test to finish.

If you abort a self test before the self test is finished, the analyzer may fail its calibration routine. To prevent this from happening, press [**Preset**] or cycle power after you abort a self test.

To run a specific self test in loop mode, press the analyzer keys as follows and then select the self test:

[**Preset**]

[**Spcl Fctn**]

[SERVICE FUNCTIONS]

[SELF TEST]

[LOOP MODE **ON** OFF]

[FUNCTIONL TESTS]

Troubleshooting Failing Performance Tests

Note



With the exception of the Quick Confidence test, all functional self tests in Test 9. Self Test must pass before table 5-27 is valid.

Use table 5-27 to determine which assembly is causing a performance test to fail. The table lists the assembly or assemblies most likely to cause the failure. In some cases, the failure can be isolated to one assembly based on the exact failure. When the cause of the failure cannot be isolated to one assembly, an additional test is provided to help isolate the faulty assembly. Multiple probable faulty assemblies are listed in order of probability.

Table 5-27. Failing Perf. Test Troubleshooting Guide

| Failing Performance Test | Probable Faulty Assembly (in order of probability) | Troubleshooting Test |
|---------------------------------|---|---------------------------------------|
| 1. Local Oscillator Feedthrough | A12 First Conversion A11 Input | Test 23. Local Oscillator Feedthrough |
| 2. Phase Noise | A51 Interpolation VCO A52 Fractional-N A21 Sum VCO A22 Sum Phase Detector A23 Step Phase Detector A24 Step VCO A31 Reference/Calibrator A32 300 MHz A33 Trigger A91 Fan Power/Oven | Test 24. Phase Noise |
| 3. Residual Responses | A12 First Conversion A13 Second Conversion A11 Input A61 IF | Test 25. Residual Responses |
| 4. Noise Level | A61 IF A62 ADC/Digital Filter A12 First Conversion A11 Input A13 Second Conversion | Test 26. Noise Level |
| 5. Frequency Accuracy | A31 Reference Calibrator A91 Fan Power/Oven | Test 27. Frequency Accuracy |
| 6. Spurious Responses | A52 Fractional-N A51 Interpolation VCO A22 Sum Phase Detector A21 Sum VCO A24 Step VCO A23 Step Phase Detector | Test 28. Spurious Responses |

Table 5-27. Failing Perf. Test Troubleshooting Guide (continued)

| Failing Performance Test | Probable Faulty Assembly (in order of probability) | Troubleshooting Test |
|--|---|---|
| 7. Image Responses 40.85956 MHz fails 60.85956 MHz fails 61.35956 MHz fails | A12 First Conversion A61 IF A61 IF | |
| 8. Input Harmonic Distortion | A11 Input A12 First Conversion | Test 29. Input Harmonic Distortion |
| 9. Intermodulation Distortion | A61 IF A12 First Conversion A11 Input | Test 30. Intermodulation Distortion |
| 10. Source Amplitude Accuracy and Frequency Response | A42 Source Conversion A41 Source Amplifier | Test 31. Source Amplitude Accuracy and Frequency Response |
| 11. Input Amplitude Accuracy and Flatness | A31 Reference/Calibrator ¹ A11 Input ² | |
| 12. Reference Level Accuracy | A11 Input ³ | |
| 13. Log Scale Accuracy | A62 ADC/Digital Filter ⁴ | Test 32. Log Scale Accuracy |
| 14. Source Dynamic Accuracy DAC attenuation fails pad attenuation fails | A42 Source Conversion A41 Source Amplifier | |
| 15. Input Return Loss | A11 Input | |
| 16. Source Return Loss | A41 Source Amplifier | |
| 17. Source Harmonic Distortion | A41 Source Amplifier | |
| 18. Source Spurious Responses | A42 Source Conversion ⁵ | |
| 19. Source Noise | A41 Source Amplifier ⁵ | |

¹ Provided performance test 10 (Source Amplitude Accuracy and Frequency Response) passed.

² Provided performance test 10 (Source Amplitude Accuracy and Frequency Response) passed and failures only occurred in the 1 MΩ input impedance path.

³ If all ranges failed, the following assemblies could cause the failure:

- A12 First Conversion
- A13 Second Conversion
- A61 IF
- A62 ADC/Digital Filter

⁴ Use the recommended test to verify that the A62 ADC/Digital Filter assembly is faulty and not one of the following assemblies:

- A61 IF
- A13 Second Conversion
- A12 First Conversion
- A11 Input

⁵ Provided the receiver passed all performance tests.

Test 23. Local Oscillator Feedthrough

Use this test to determine if the A11 Input assembly or the A12 First Conversion assembly is causing the Local Oscillator Feedthrough performance test to fail.

Note



If local oscillator feedthrough null passes the Quick Confidence test and fails the performance test, the A12 First Conversion assembly is probably faulty.

1. Set the power switch to STANDBY (⓪). Remove the screw at each end of the A11 Input assembly, and place the assembly on an extender board.
 2. Reconnect the following using extender cables:
 - A11 J1 to A41 J1
 - A11 J2 to A31 J1
 - A11 J3 to A12 J2
 3. Set the power switch to ON (I). Using an oscilloscope, monitor J11 pin 1A (INC_IMAG), pin 3A (INC_REAL), and pin 2A (UP_DN). During the calibration routine, narrow pulses are on pins 1A and 3A, and the signal on pin 2A toggles between high and low TTL levels.
-

Note



The calibration routine occurs during power up. To repeat the calibration routine, press the following keys:

[Spcl Fctn]
[SINGLE CAL]

4. If the signals are correct, the A12 First Conversion assembly is probably faulty. If the signals are incorrect, the A11 Input assembly is probably faulty.

Test 24. Phase Noise

Use this test to determine which of the following assemblies is causing the Phase Noise performance test to fail:

- A51 Interpolation VCO
- A52 Fractional-N
- A21 Sum VCO
- A22 Sum Phase Detector
- A23 Step Phase Detector
- A24 Step VCO
- A31 Reference/Calibrator
- A32 300 MHz
- A33 Trigger
- A91 Fan Power/Oven

Note

If you have the optional A91 Fan Power/Oven assembly, remove the rear panel jumper (OVEN REF OUT to EXT REF IN), and repeat the Phase Noise performance test. If the test now passes, the A91 Fan Power/Oven assembly is probably faulty.

1. Set the signal generator for a 10 MHz, -20 dBm signal and connect to the front panel INPUT connector.
2. Press the following keys:
 - [Preset]
 - [Spcl Fctn]
 - [SINGLE CAL]
 - [AUTO CAL ON **OFF**]
 - [Sweep]
 - [OVERSWEEP ON **OFF**]
 - [Freq]
 - [CENTER]
 - 10
 - [MHz]
 - [SPAN]
 - 5
 - [kHz]
 - [Marker]
 - [MARKER X ENTRY]
 - 10.001
 - [MHz]
 - [Marker Fctn]
 - [NOISE LEVEL **ON OFF**]

3. Record the **Mkr** readout (dBm/Hz).
4. Change the signal generator's frequency to 100 MHz.
5. Press the following keys:

[NOISE LEVEL ON **OFF**]
[**Freq**]
[CENTER]
100
[MHz]
[**Marker**]
[MARKER X ENTRY]
100.001
[MHz]
[**Marker Fctn**]
[NOISE LEVEL **ON** OFF]

6. If the **Mkr** readout is more than approximately 10 dB above the level recorded in step 3, then the A31 Reference/Calibrator assembly is probably faulty.
7. Set a spectrum analyzer's center frequency to 300 MHz and connect to A32 J4. If the noise level is > -95 dBc/Hz for offsets > 1 kHz, the A32 300 MHz assembly is probably faulty.
8. Connect an oscilloscope to A33 J4. The signal should be a 100 kHz, 1 Vp-p, approximate 1% duty cycle pulse. If the signal is not correct, the A33 Trigger assembly is probably faulty.
9. Reconnect the following using original cables.
 - A31 J4 to A23 J3
 - A32 J4 to A23 J2
 - A33 J4 to A52 J2

10. Press the following keys:

[NOISE LEVEL ON **OFF**]
 [**Spcl Fctn**]
 [PRFM TESTS]
 [CALIBRATR TO INPUT]
 [**Freq**]
 [CENTER]
10
 [MHz]
 [**Spcl Fctn**]
 [] (second softkey from bottom)
- 99
 [] (second softkey from bottom)
 [SERVICE FUNCTIONS]
 [SPCL TEST MODES]
 [LOCAL OSC CONFIG]
 [LOCAL OSC **SNGL** MULT]
 [**Marker**]
 [MKR --> PEAK]
 [ZERO OFFSET]
 [MARKER X ENTRY]
10.001
 [MHz]
 [**Marker Fctn**]
 [NOISE LEVEL **ON** OFF]

11. Phase noise fails in single loop mode if the Δ **Mkr** readout is > -105 dB/Hz. If single loop phase noise is failing, the A21 Sum VCO assembly or the A52 Fractional-N assembly is probably faulty.

12. Press the following keys:

[**Preset**]
 [**Sweep**]
 [SWEEP AUTO **MAN**]
 [MANUAL FREQ]
10
 [MHz]

13. Set the spectrum analyzer's center frequency to 316 MHz and connect to A24 J2. Measure and record the noise level at offsets >1 kHz.
14. Press the following keys:
 [MANUAL FREQ]
 100
 [MHz]
15. Change the spectrum analyzer's center frequency to 400 MHz and measure the noise level for offsets >1 kHz. If the noise level changed when the frequency changed, the A23 Step Phase Detector assembly or the A24 Step VCO assembly is probably faulty.
16. Change the spectrum analyzer's center frequency to 10.1875 MHz and connect to A51 J1. If the noise level is > -110 dBc/Hz for offset frequencies >100 Hz, the A51 Interpolation VCO assembly is probably faulty.
17. Reconnect A51 J1 to A22 J3.
18. Change the spectrum analyzer's center frequency to 410.1875 MHz and span to 5 kHz. Connect the spectrum analyzer to A21 J3. If the shape of the noise peaks excessively (>5 dB), the A22 Sum Phase Detector assembly is probably faulty.

Test 25. Residual Responses

Use this test to determine which of the following assemblies is causing the Residual Responses performance test to fail:

- A12 First Conversion
- A13 Second Conversion
- A11 Input
- A61 IF

1. Press the following keys:

```
[ Preset ]
[ Spcl Fctn ]
  [ SINGLE CAL ]
  [ AUTO CAL ON OFF ]
[ Range/Input ]
  [ RANGE ]
  -20
  [ dBm ]
[ Meas Type ]
  [ NARROW BAND ZOOM ]
[ Avg/Pk Hld ]
  [ VIDEO AVERAGE ]
[ Freq ]
  [ SPAN ]
  36.0625
  [ Hz ]
  [ CENTER ] (to failing frequency)
```

2. After measurement averaging is complete (10 averages), press the following keys:

```
[ Marker ]
  [ ZERO OFFSET ]
```

3. Disconnect the cable connected to A11 J3 and press [**Meas Restart**]. After measurement averaging is complete, the Δ **Mkr** readout should be > -2 dB. If the readout dropped more than approximately 4 dB when A11 J3 is disconnected, the A11 Input assembly is probably faulty.
4. Disconnect the cable connected to A12 J3 and press [**Meas Restart**]. After measurement averaging is complete, the Δ **Mkr** readout should be > -2 dB. If the readout drops more than approximately 4 dB when A12 J3 is disconnected, the A12 First Conversion assembly is probably faulty.
5. Disconnect the cable connected to A13 J3 and press [**Meas Restart**]. After measurement averaging is complete, the Δ **Mkr** readout should be > -2 dB. If the readout drops more than approximately 4 dB when A13 J3 is disconnected, the A13 Second Conversion assembly is probably faulty. If the readout is correct, A61 IF assembly is probably faulty.

Test 26. Noise Level

Use this test to determine which of the following assemblies is causing the Noise Level performance test to fail:

- A61 IF
- A62 ADC/Digital Filter
- A12 First Conversion
- A11 Input
- A13 Second Conversion

Note



The A11 Input assembly dominates the low frequency noise level. Therefore, if the failing frequencies are below 30 kHz, the A11 Input assembly is probably faulty.

If failures only occurred using the 1 MΩ input impedance, the A11 Input assembly is probably faulty.

1. Press the following keys:

- [Preset]
- [Spcl Fctn]
 - [SINGLE CAL]
 - [AUTO CAL ON **OFF**]
- [Range/Input]
 - [RANGE]
 - 20
 - [dBm]
- [Freq]
 - [ZERO SPAN]
- [Marker Fctn]
 - [NOISE LVL **ON** OFF]
- [Meas Type]
 - [LOW DIST ON OFF] (to distortion mode of failing frequency)
- [Res BW]
 - [RES BW] (to resolution bandwidth of failing frequency)
- [Freq]
 - [CENTER] (to failing frequency)
- [Marker]
 - [ZERO OFFSET]

2. Disconnect the cable connected to A11 J3. The Δ Mkr readout should be > -2 dB/Hz. If the readout dropped more than approximately 4 dB when A11 J3 is disconnected, the A11 Input assembly is probably faulty.
3. Disconnect the cable connected to A12 J3. The Δ Mkr readout should be > -2 dB/Hz. If the readout drops more than approximately 4 dB when A12 J3 is disconnected, the A12 First Conversion assembly is probably faulty.
4. Disconnect the cable connected to A13 J3. The Δ Mkr readout should be > -2 dB/Hz. If the readout drops more than approximately 4 dB when A13 J3 is disconnected, the A13 Second Conversion assembly is probably faulty.
5. Disconnect the cable connected to A61 J3 and terminate A62 J3 into 50Ω . The Δ Mkr readout should be > -4 dB/Hz. If the readout drops more than approximately 6 dB when A61 J3 is disconnected, the A61 IF assembly is probably faulty. If the readout is correct, A62 ADC/Digital Filter assembly is probably faulty.

Test 27. Frequency Accuracy

Use this test to determine if the A31 Reference/Calibrator assembly or the optional A91 Fan Power/Oven assembly is causing the Frequency Accuracy performance test to fail.

Note



If the frequency accuracy performance test failed without option 001, the A31 Reference/Calibrator assembly is probably faulty.

The calculated frequency specification is based on the number of months since the last frequency adjustment. If unsure of the date, do the adjustment and repeat the performance test. If the performance test is done immediately after the adjustment, use zero for the number of months, otherwise use one.

1. Remove the rear panel jumper (OVEN REF OUT to EXT REF IN) and connect OVEN REF OUT to a frequency counter.
2. Divide the lower and upper frequency limit specifications calculated in the performance test by ten and compare to OVEN REF OUT.
3. If OVEN REF OUT is within specification, the A31 Reference/Calibrator assembly is probably faulty. If OVEN REF OUT is not within specification, the A91 Fan Power/Oven assembly is probably faulty.

Test 28. Spurious Responses

Table 5-28 lists spur types and the assembly or assemblies most likely to cause the failure.

If the A52 Fractional-N assembly is listed as the probable faulty assembly but the performance test still fails after replacing the assembly and doing the required adjustments (see table 5-2), the probable faulty assembly is listed below in order of probability:

- A51 Interpolation VCO
- A21 Sum VCO
- A22 Sum Phase Detector
- A24 Step VCO
- A23 Step Phase Detector

If the A22 Sum Phase Detector assembly is listed as the probable faulty assembly but the performance test still fails after replacing the assembly, the probable faulty assembly is listed below in order of probability:

- A21 Sum VCO
- A24 Step VCO
- A23 Step Phase Detector
- A52 Fractional-N
- A51 Interpolation VCO

Table 5-28. Spur Types

| Source Frequency (MHz) | Spur Frequency (MHz) | Spur Type | Probable Faulty Assembly |
|------------------------|----------------------|-------------------------------|---------------------------------------|
| 7.8125 | 10.8428 | sum reference | A22 Sum Phase Detector A21 Sum VCO |
| 9.8125 | 9.8248 | step comb | A22 Sum Phase Detector |
| 149.8125 | 149.8248 | step comb | A22 Sum Phase Detector |
| 95.81274 | 95.81254 | API 1 | A52 Fractional-N † |
| 95.8149 | 95.8129 | API 1 | A52 Fractional-N † |
| 100.79274 | 100.79254 | API 1 | A52 Fractional-N † |
| 100.7949 | 100.7929 | API 1 | A52 Fractional-N † |
| 100.79454 | 100.79254 | API 2 | A52 Fractional-N † |
| 100.794504 | 100.792504 | API 3 | A52 Fractional-N |
| 100.7945004 | 100.7925004 | API 4 | A52 Fractional-N † |
| 1.8125 | 4.81373 | 3 MHz sideband on sum loop | A22 Sum Phase Detector A21 Sum VCO |
| 7.81496 | 4.81373 | 3 MHz sideband on sum loop | A22 Sum Phase Detector A21 Sum VCO |
| 144.8125 | 144.822623 | 10.123 kHz sideband on signal | A22 Sum Phase Detector A21 Sum VCO |
| 144.832746 | 144.822623 | 10.123 kHz sideband on signal | A22 Sum Phase Detector A21 Sum VCO |
| 89.9125 | 89.8125 | 100 kHz sideband | A52 Fractional-N † |

† Before replacing the A52 Fractional-N assembly, go to section I and do adjustment 6. 100 kHz and API Spurs. Do not try to adjust the spurs using the performance test setup. The setup in the performance test is not the same as the setup for the adjustment. After replacing the assembly, do adjustment 6. 100 kHz and API Spurs before repeating the performance test.

Test 29. Input Harmonic Distortion

Use this test to determine if the A11 Input assembly or the A12 First Conversion assembly is causing the Input Harmonic Distortion performance test to fail.

Note



If failures only occurred in the 1 M Ω input impedance path, the A11 Input assembly is probably faulty.

If failures only occurred with low distortion mode on or off, but not both, the A11 Input assembly is probably faulty.

1. Press the following keys:

[Preset]
[Spcl Fctn]
[SINGLE CAL]
[AUTO CAL ON **OFF**]
[Range/Input]
[RANGE]
0
[dBm]
[Res BW]
[RES BW]
4.5
[Hz]
[Sweep]
[SWEEP AUTO **MAN**]
[Avg/Pk Hld]
[VIDEO AVERAGE]
[Meas Type]
[LOW DIST ON OFF] (to failing mode)

2. Connect the test equipment as shown in figure 5-22.

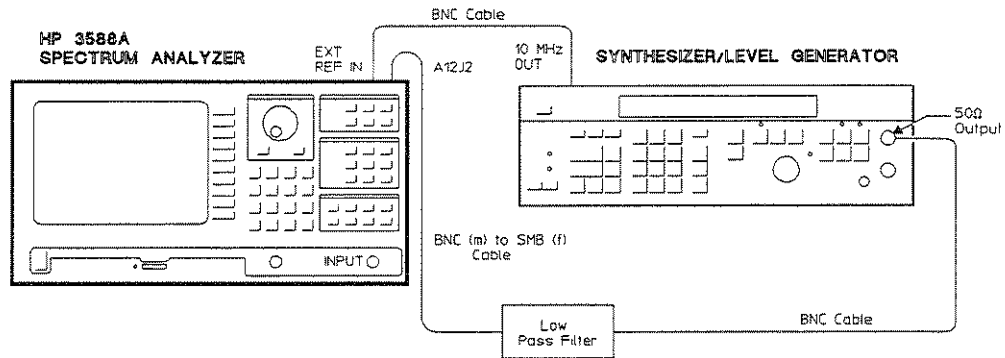


Figure 5-22. Troubleshooting Input Harmonic Distortion

3. Set the synthesizer/level generator as follows:

| | |
|-----------|--|
| Amplitude | -28 dBm |
| Frequency | (to fundamental frequency of failing harmonic) |
4. Press the following keys:
 - [Sweep]
 - [MANUAL FREQ] (to fundamental frequency of failing harmonic)
 - [Marker]
 - [ZERO OFFSET]
 - [Sweep]
 - [MANUAL FREQ] (to failing harmonic)
5. If the Δ Man readout is now within specification, the A11 Input assembly is probably faulty. If the Δ Man readout is still failing, the A12 First Conversion assembly is probably faulty.

Test 30. Intermodulation Distortion

Use this test to determine which of the following assemblies is causing the Intermodulation Distortion performance test to fail:

- A61 IF
- A12 First Conversion
- A11 Input

Note



If failures only occurred using the 1 M Ω input impedance path or the 50 Ω input impedance path, but not both, the A11 Input assembly is probably faulty.
If failures only occurred at 23.634734 MHz or 23.640148 MHz, the A61 IF assembly is probably faulty.

1. Press the following keys:

[Preset]
[Spcl Fctn]
 [SINGLE CAL]
 [AUTO CAL ON **OFF**]
[Range/Input]
 [RANGE]
 -20
 [dBm]
[Freq]
 [FULL SPAN]
[Res BW]
 [RES BW]
 1.1
 [Hz]
[Sweep]
 [SWEEP AUTO **MAN**]
 [MANUAL FREQ]
 23.634466

2. Connect the test equipment as shown in figure 5-23.
3. Set the signal generator's frequency to 23.634466 MHz, and adjust its amplitude for a **Man** readout of $-26.0 \text{ dBm} \pm 0.1 \text{ dB}$ (approximately -27 dBm).
4. Press the following keys:
 [Sweep]
5. [MANUAL FREQ] (to source frequency of failing frequency)
6. Set the synthesizer/level generator's frequency to the source frequency of the failing frequency, and adjust its amplitude for a **Man** readout of $-26.0 \text{ dBm} \pm 0.1 \text{ dB}$ (approximately -27 dBm).

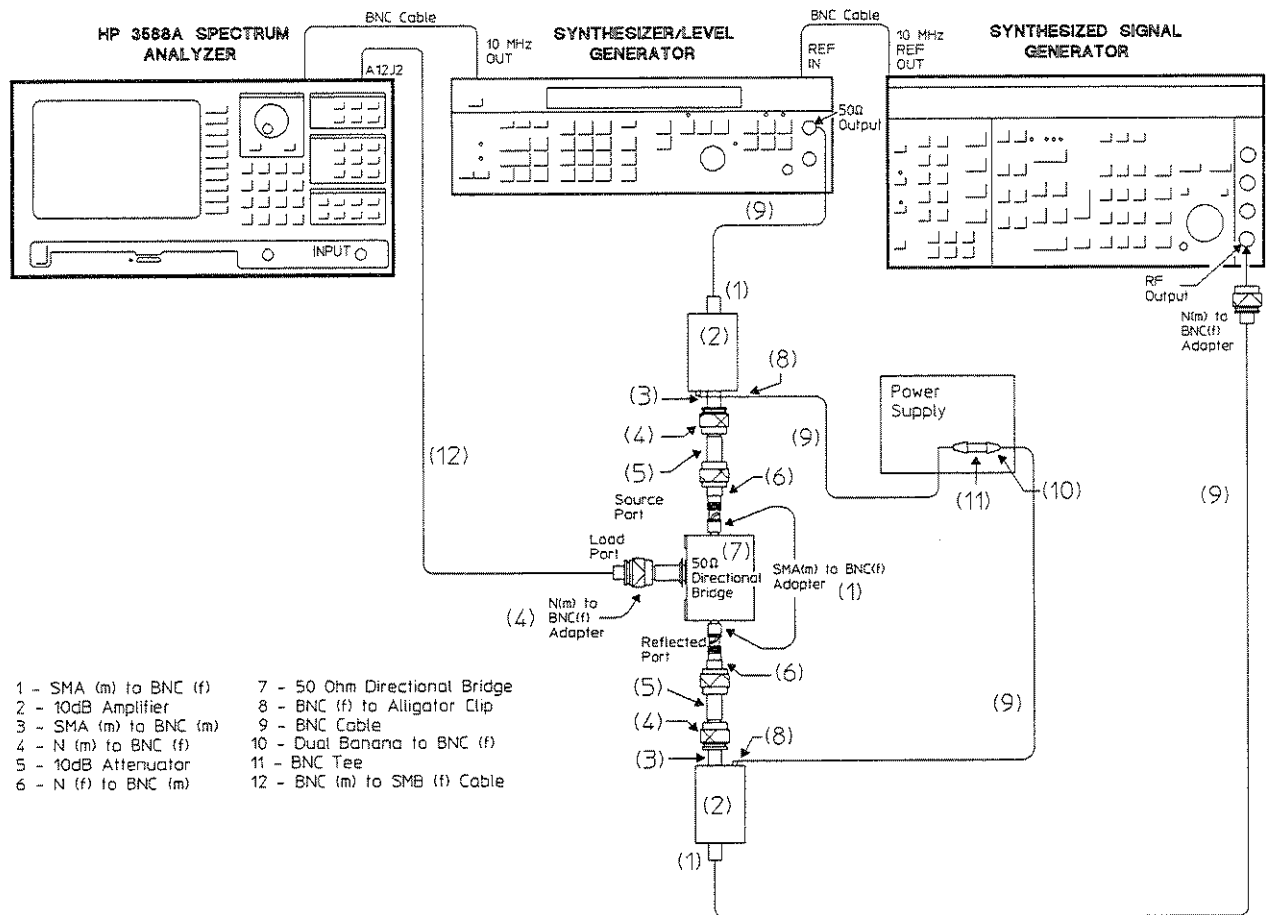


Figure 5-23. Troubleshooting Intermodulation Distortion

7. Press the following keys:

- [Marker]
- [ZERO OFFSET]
- [Avg/Pk Hld]
- [VIDEO AVERAGE]
- [Sweep]
- [MANUAL FREQ] (to failing frequency)

8. If the Δ Man readout is now within specification, the A11 Input assembly is probably faulty. If the Δ Man readout is still failing, the A12 First Conversion assembly is probably faulty.

Test 31. Source Amplitude Accuracy and Frequency Response

Use this test to determine if the A42 Source Conversion assembly or the A41 Source Amplifier assembly is causing the Source Amplitude Accuracy and Frequency Response performance test to fail.

Note



If the Source Dynamic Accuracy performance test also fails, the A42 Source Conversion assembly is probably faulty.

Before replacing the A42 Source Conversion assembly, check the Source Bandpass Filter adjustment.

1. Connect A42 J1 to the front panel INPUT connector using an SMB-to-BNC cable.
2. Press the following keys:
 - [Preset]
 - [Source]
 - [SOURCE ON OFF]
 - [Scale]
 - [REFERENCE LEVEL]
 - 36
 - [dBm]
 - [VERTICAL/DIV]
 - 1
 - [dB]
3. The signal's amplitude should be $-41 \text{ dBm} \pm 3 \text{ dB}$, and its flatness should be $\pm 1 \text{ dB}$ relative to the amplitude at 300 kHz. If the signal is correct, the A41 Source Amplifier is probably faulty. If the signal is incorrect, the A42 Source Conversion assembly is probably faulty. Before replacing the A42 Source Conversion assembly, check the Source Bandpass Filter adjustment.

Test 32. Log Scale Accuracy

If the Log Scale Accuracy performance test fails, the most likely cause is the A62 ADC/Digital Filter assembly. Use this test to verify that the A62 ADC/Digital Filter assembly is faulty and not one of the following:

- A61 IF
- A13 Second Conversion
- A12 First Conversion
- A11 Input

Note

Before replacing the A62 ADC/Digital Filter assembly, check the ADC Gain, Offset, and Reference adjustment.

1. Connect the 50Ω feedthrough termination to the multimeter using the adapter.
2. Measure the resistance of the feedthrough termination and enter as the reference impedance for dBm operation (RES). Then set the multimeter's function to ac volts (most accurate mode). For an HP 3458A Digital Multimeter, press the following keys:

| | |
|----------------|-------------------------|
| blue shift key | Reset |
| OHM | |
| blue shift key | S |
| Menu Scroll ↓ | (until SMATH is shown) |
| 10 (RES) | ENTER |
| ACV | |
| blue shift key | S |
| Menu Scroll ↓ | (until SETACV is shown) |
| 3 (SYNC) | ENTER |

Note

If your digital multimeter does not have dBm math capability, record the resistance of the feedthrough termination (RES) for later calculations.

3. Connect the test equipment as shown in figure 5-24.

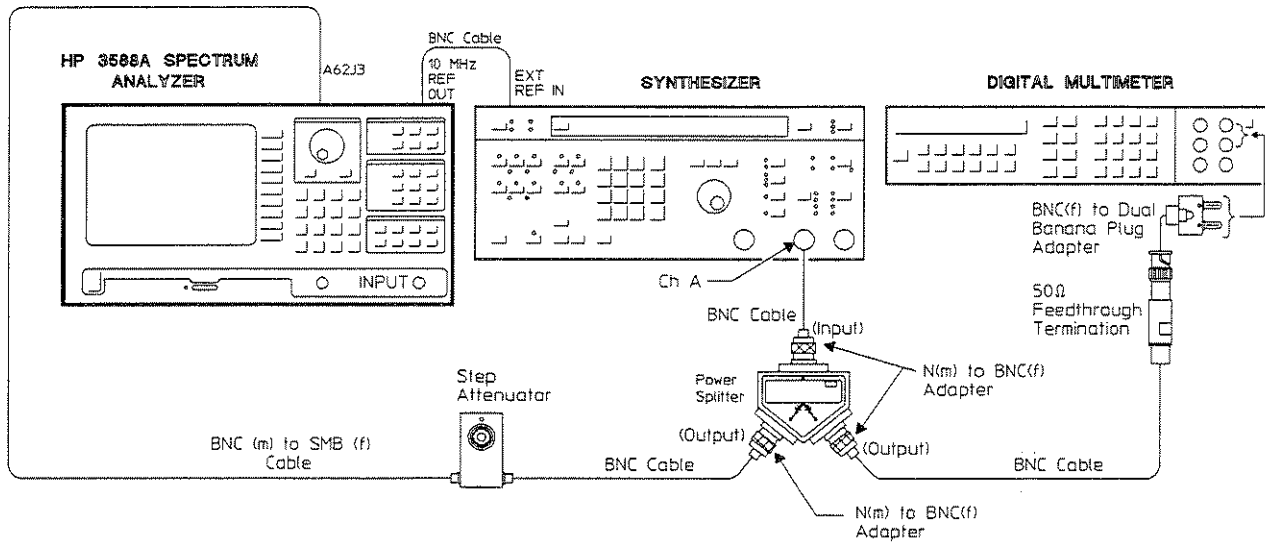


Figure 5-24. Troubleshooting Log Scale Accuracy

4. Press the following keys:

- [Preset]
- [Spcl Fctn]
 - [SINGLE CAL]
 - [AUTO CAL ON **OFF**]
- [Freq]
 - [CENTER]
 - 100**
 - [kHz]
 - [SPAN]
 - 1**
 - [kHz]
- [Sweep]
 - [SWEEP AUTO **MAN**]
- [Range/Input]
 - [RANGE]
 - 10**
 - [dBm]

5. Set the step attenuator to 0 dB.

6. Set the synthesizer as follows:

- | | |
|-----------|---|
| Frequency | 187.5 kHz |
| Amplitude | (adjust for Man readout of 10 dBm \pm 0.01 dB) |

7. Press the following keys:

[Marker]
 [ZERO OFFSET]
 [Avg/Pk Hld]
 [VIDEO AVERAGE]

8. Set the multimeter's math mode to dBm and null. For an HP 3458A Digital Multimeter, press the following keys:

| | |
|------------------|-----------------------|
| blue shift key | L |
| Menu Scroll ↓ | (until MATH is shown) |
| 5, 9 (dBm, NULL) | ENTER |

Note



If your digital multimeter does not have math null capability, record the multimeter readout in dBm for later calculations.

If your digital multimeter does not have dBm math capability, use the following formula to convert your measurement results to dBm.

$$10 \times \log_{10} (\text{readout}^2 / \text{RES} / 1 \text{ mW}) = \text{dBm}$$

readout = multimeter's readout in volts

RES = measured resistance of the feedthrough termination

9. Adjust the synthesizer's amplitude down from the reference amplitude (set in step 6) by the level that failed the performance test.

Note



If your digital multimeter does not have math null capability, subtract the multimeter readout in step 8 from the current multimeter readout.

10. Press [Meas Restart].

11. If the Δ Man readout is still out of specification, the A62 ADC/Digital Filter assembly is probably faulty.

Troubleshooting Miscellaneous Failures

The following tests provide troubleshooting information for miscellaneous failures that are not detected by the self tests.

Test 33. Memory Battery

Use this test when battery-backed-up memory is suspected of failing. This test separates Memory assembly failures from memory battery failures.

1. Press the following keys:

[Preset]
[Spcl Fctn]
[DATE MMDDYY]
010101
[ENTER]

2. Set the power switch to STANDBY (⓪), then to ON (I).
3. Press the following keys:
[Spcl Fctn]
[DATE MMDDYY]
4. If the date is 01/01/01, the battery-backed-up memory is functioning correctly, go to Test 9. Self Test to continue troubleshooting.
5. If the date is incorrect, remove the Memory assembly (see figures 2-3, 2-4, and 5-0 in section II, "Replaceable Parts").
6. Check the voltage at B402. If the voltage is $3.7 \pm 1V$, the Memory assembly is probably faulty. If the battery voltage is incorrect, replace the battery.

Note



Set the analyzer's HP-IB address after replacing the battery or the Memory assembly (see "Replacing the Memory Assembly" in section II, "Replaceable Parts").

Test 34. Fan Power

Use this test when the analyzer is operating correctly, but the fan on the BNC connector side of the analyzer is not working. This test determines which of the following is faulty:

- Motherboard
 - A90 Fan Power assembly or optional A91 Fan Power/Oven assembly
 - Fan
1. Set the power switch to STANDBY (⓪), and disconnect the power cord from the rear panel. Remove the top cover, rear panel, and fan/oven housing (see figures 2-3, 2-4, and 2-11 in section II, "Replaceable Parts").
 2. Disconnect the connector with the yellow, red, and black wires from the A90 Fan Power assembly or the optional A91 Fan Power/Oven assembly (see figure 2-12).
 3. Set the power switch to ON (I). Check that the voltage at the yellow wire is $-18 \pm 2V$ and the voltage at the red wire is $+18 \pm 2V$. If either voltage is incorrect, the motherboard or the wire is probably faulty.
 4. Set the power switch to STANDBY (⓪). Reconnect the connector with yellow, red, and black wires, and disconnect the connector with the red and black wires.
 5. Set the power switch to ON (I) and check that J3 pin 2 is $-18 \pm 2V$. If the voltage is correct, the fan is probably faulty. If this voltage is incorrect, the A90 Fan Power assembly or the optional A91 Fan Power/Oven assembly is probably faulty.

Test 35. Trigger

Use this test when the analyzer is operating correctly, but the HP-IB trigger or external trigger is not functioning. This test determines if the A33 Trigger assembly or A81 CPU assembly is faulty.

Note



If the analyzer triggers using external trigger and does not trigger using HP-IB trigger, the A81 CPU assembly is probably faulty.

1. Set a synthesizer for a 2 Hz, 5 Vp-p square wave.
2. Using a BNC cable, connect the synthesizer's output to EXT TRIG on the rear panel.
3. Press the following keys:
 - [Preset]
 - [Trigger]
 - [EXTERNAL TRIGGER]
4. The analyzer should briefly display WAITING FOR TRIGGER between each sweep. If this did not occur, the A33 Trigger assembly is probably faulty. Before replacing the assembly, go to step 6 to check the voltages at the connector.
5. Using a logic probe, check that TRIG OUT on the rear panel toggles between a TTL high and TTL low level. If this did not occur, the A33 Trigger assembly is probably faulty. Do the next step before replacing the assembly.
6. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:
 - a. Set the power switch to STANDBY (⓪). Remove the screw at each end of the suspected assembly. Remove the assembly and place an extender board in the card nest.
 - b. Set the power switch to ON (1), then measure the pins of the extender board for correct voltages (see table 4-13 on page 4-59).

Power-on Test Descriptions

A portion of the self tests listed in table 5-31 are run when the analyzer is powered up. These self tests are the power-on tests and are divided into low-level and high-level tests (as indicated in the table).

Note



The calibration routine is run immediately following the power-on tests. If an error occurs during the calibration routine, a failure message is recorded in the fault log.

Low-level Tests

The low-level power-on tests exercise the core of the CPU assembly and, depending on the position of A81 SW100(6), run the short or long RAM test. If an error occurs during the low-level tests, the tests pause for 10 seconds and display an error code on the CPU assembly's power-on test LEDs (see Test 2. Power-on for details on decoding the power-on test LEDs).

The short RAM test does one read and write test of RAM plus a RAM refresh test. If the short RAM test fails, the only error code displayed on the CPU's power-on test LEDs is the RAM refresh error code (81 hexadecimal). The long RAM test does eight passes of RAM plus the RAM refresh test. The long RAM test displays the RAM specific bit errors on the CPU's power-on test LEDs. Set SW100(6) to zero (factory setting) to run the short RAM test and to one to run the long RAM test.

Note



If A81 SW100 switch 4 is set to 0, the CPU determines the installed RAM size and bypasses the high-level tests. The factory setting for A81 SW100(4) is 1.

High-level Test

The high-level power-on test exercises the fast bus. If an error occurs during the fast bus test, the analyzer locks up and the power-on LEDs display the fast bus error code (A1 hexadecimal).

Power-on Test Messages

Table 5-30 provides additional information for interpreting the power-on test LEDs. Using table 5-29, translate the power-on test LEDs to their equivalent hexadecimal code. Table 5-30 describes the power-on subtests in the order they are run. Table 5-30 also shows the relationship between a failing power-on subtest and the assemblies or sub-blocks.

Note



False error codes can be caused by shorts on the buses, reset line, or interrupt line. If an error code is caused by the last bus connected, it is probably the source of the failure.

Table 5-29. Binary to Hexadecimal

| Binary 1 = LED on 0 = LED off | Hexadecimal |
|-------------------------------------|-------------|
| 0000 | 0 |
| 0001 | 1 |
| 0010 | 2 |
| 0011 | 3 |
| 0100 | 4 |
| 0101 | 5 |
| 0110 | 6 |
| 0111 | 7 |
| 1000 | 8 |
| 1001 | 9 |
| 1010 | A |
| 1011 | B |
| 1100 | C |
| 1101 | D |
| 1110 | E |
| 1111 | F |

Table 5-30. Power-on Test Messages

| Hexadecimal Code | Message | Assembly/Sub-block (Chart Below) | | | | | | |
|------------------|-------------------------------------|----------------------------------|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Undefined | Initial power-on | x | x | x | | | | |
| FF* | CPU flashes LEDs | 0 | x | x | x | | | |
| 05 | Start CPU test | 0 | x | x | x | | | |
| 06 | CPU test failure | 0 | x | x | x | | | |
| 90 | Start monitor ROM test | 0 | 0 | 0 | x | | | |
| 91 | Monitor ROM failure, low byte | 0 | 0 | 0 | x | | | |
| 92 | Monitor ROM failure, high byte | 0 | 0 | 0 | x | | | |
| 93 | Monitor ROM failure, both bytes | 0 | 0 | 0 | x | | | |
| 08 | Start display controller test | 0 | 0 | 0 | 0 | x | | |
| 09 | Display controller test fails | 0 | 0 | 0 | 0 | x | | |
| 0A | Display control didn't return DTACK | 0 | 0 | 0 | 0 | x | | |
| F0 | Start program ROM test | 0 | 0 | 0 | 0 | 0 | x | |
| F1, D0 to DF | Program ROM failure, low byte | 0 | 0 | 0 | 0 | 0 | x | |
| F2, E0 to EF | Program ROM failure, high byte | 0 | 0 | 0 | 0 | 0 | x | |
| F3, C0 to CF | Program ROM failure, both bytes | 0 | 0 | 0 | 0 | 0 | x | |
| F4 | Number of ROMs out of range | 0 | 0 | 0 | 0 | 0 | x | |
| 0B | RAM size test | 0 | 0 | 0 | 0 | 0 | x | |
| 0F | Start RAM test | 0 | 0 | 0 | 0 | 0 | x | |
| 0F flash | Memory did not return MEM DTACK | 0 | 0 | 0 | 0 | 0 | x | |
| 10, 11 | RAM test failure, low byte | 0 | 0 | 0 | 0 | 0 | x | |
| 20, 21 | RAM test failure, high byte | 0 | 0 | 0 | 0 | 0 | x | |
| 30, 31 | RAM test failure, both bytes | 0 | 0 | 0 | 0 | 0 | x | |
| 40 to 7F | RAM test, chip failure | 0 | 0 | 0 | 0 | 0 | x | |
| 80 | Start RAM refresh test | 0 | 0 | 0 | 0 | 0 | x | |
| 81 | RAM refresh failure | 0 | 0 | 0 | 0 | 0 | x | |
| A1 | Fast bus test | 0 | 0 | 0 | 0 | 0 | 0 | x |
| 00 | Clear (passed power-on sequence) | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Assembly/Sub-block Chart

- 1 = Power Supply
- 2 = A81 MPU (6800) & Address Decoder
- 3 = A81 MPU Buses
- 4 = A81 Monitor EPROM
- 5 = A81 Display Controller
- 6 = A87 Memory
- 7 = A81 Fast Bus

0 Assembly or sub-block is used but is probably not the cause of the failure message.

X Assembly or sub-block is probably the cause of the failure message.

(blank) Assembly or sub-block is not used in the test.

FF* If the area of failure is unclear, all LEDs flash continuously.

Self-Test Descriptions

Thirty-six self tests are available that can be run in groups or individually. Table 5-31 lists the assemblies used by the self tests and shows the assembly that would be the most likely cause of a self-test failure. To run these self tests in the order shown, press the following keys:

```
[ Spcl Fctn ]  
  [      ] (second softkey from bottom)  
  - 99  
  [      ] (second softkey from bottom)  
  [ SERVICE FUNCTIONS ]  
  [ SELF TEST ]  
  [ FUNCTIONL TESTS ]  
  [ ALL ]
```

To run a single self test, press the softkey shown in the table instead of [ALL]. To determine the key path for the self-test softkeys, see table 5-32, "Self-Test Menu Map and HP-IB Commands."

Note



Certain instrument malfunctions cause multiple self-test failures. Therefore, to determine the most likely cause when more than one self test fails, look in table 5-31 for assemblies common to all failing self tests.

Table 5-31. Assemblies Used in Self Tests

| Self Test Softkey | Assembly | | | | | | | | | | | | | | | | | | | | |
|--------------------------|----------|-----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| | A81 | A87 | FP | DD | A62 | A61 | A13 | A12 | A11 | A42 | A41 | A33 | A32 | A31 | A52 | A51 | A24 | A23 | A22 | A21 | |
| [PROCESSOR]† | X | 0 | | | 0 | | | | | | | | | 0 | | | | | | | |
| [RAM]† | 0 | X | | | 0 | | | | | | | | | 0 | | | | | | | |
| [ROM]† | 0 | X | | | 0 | | | | | | | | | 0 | | | | | | | |
| [INTERRUPT] | X | 0 | | | 0 | | | | | | | | | 0 | | | | | | | |
| [MULTI FCTN PERIPHERL] | X | 0 | | | 0 | | | | | | | | | 0 | | | | | | | |
| [FRONT PANEL] | 0 | 0 | X | | 0 | | | | | | | | | 0 | | | | | | | |
| [DISPLAY DGTL HW] | X | 0 | | | 0 | | | | | | | | | 0 | | | | | | | |
| [HP-IB FUNC TEST] | X | 0 | | | 0 | | | | | | | | | 0 | | | | | | | |
| [DISK CONTRLLR] | X | 0 | | | 0 | | | | | | | | | 0 | | | | | | | |
| [MOTOR] | 0 | 0 | | X | 0 | | | | | | | | | 0 | | | | | | | |
| [RESTORE] | 0 | 0 | | X | 0 | | | | | | | | | 0 | | | | | | | |
| [RANDOM SEEK] | 0 | 0 | | X | 0 | | | | | | | | | 0 | | | | | | | |
| [SEEK SECTOR] | 0 | 0 | | X | 0 | | | | | | | | | 0 | | | | | | | |
| [READ] | 0 | 0 | | X | 0 | | | | | | | | | 0 | | | | | | | |
| [READ/WRITE] | 0 | 0 | | X | 0 | | | | | | | | | 0 | | | | | | | |
| [READ/WRITE ALL] | 0 | 0 | | X | 0 | | | | | | | | | 0 | | | | | | | |
| [IIC BUS] | X | 0 | X | | X | | | | X | X | X | X | | X | X | X | | | X | | |
| [FAST BUS]‡ | X | 0 | | | X | | | | | | | | | 0 | | | | | | | |
| [DMA] | X | 0 | | | 0 | | | | | | | | | 0 | | | | | | | |
| [MATH COPROC SSR] | X | 0 | | | 0 | | | | | | | | | 0 | | | | | | | |
| [SNGL LOOP TUN RANGE] | 0 | 0 | | | 0 | | | | | | | 0 | 0 | 0 | X | X | | 0 | | | X |
| [MULT-LOOP TUN RANGE] | 0 | 0 | | | 0 | | | | | | | 0 | 0 | 0 | X | X | | 0 | | | |
| [POST DIVIDER] | 0 | 0 | | | 0 | 0 | 0 | 0 | 0 | | | 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 0 |
| [AUTO RNG TRIP PTS] | 0 | 0 | | | 0 | 0 | 0 | 0 | X | 0 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| [10 MHz LOCAL OSC] | 0 | 0 | | | 0 | 0 | 0 | 0 | 0 | | | X | X | X | X | X | X | X | X | X | X |
| [2ND IF LEVEL] | 0 | 0 | | | 0 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| [ADC] | 0 | 0 | | | X | 0 | 0 | 0 | 0 | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| [DIGITAL FILTER] | 0 | 0 | | | X | | | | | | | 0 | 0 | 0 | | | | | | | |
| [DETECTOR] | 0 | 0 | | | X | | | | | | | 0 | 0 | 0 | | | | | | | |
| [187.5 kHz REFERENCE] | 0 | 0 | | | 0 | | | | | X | 0 | 0 | 0 | 0 | | | | | | | |
| [GILBERT CELL] | 0 | 0 | | | 0 | | | | | X | 0 | 0 | 0 | 0 | | | | | | | |
| [OUTPUT CKTS] | 0 | 0 | | | 0 | | | | | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| [FLATNESS] | 0 | 0 | | | 0 | 0 | 0 | 0 | 0 | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| [QUICK CONF TEST] | 0 | 0 | | | X | X | X | X | X | X | X | 0 | 0 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

X This assembly could be the cause of the failure message.
 0 This assembly is probably not the cause of the failure message but could be.
 No symbol means that the assembly is not used by the self test.
 † Low-level power-on tests
 ‡ High-level power-on tests
 The motherboard, power supply, and display are used in every test.

Self Tests that Perform a Measurement

The following self tests perform measurements:

- ADC
- POST DIVIDER
- AUTO RNG TRIP PTS
- 10 MHz LOCAL OSC
- FLATNESS
- QUICK CONF TEST

The measurements bypass any standard corrections and do not perform calibration data corrections. Therefore, all self-test measurements using analog data have limits larger than the standard calibration tolerances.

Some hardware setup modes used in these self tests are not used by normal measurements and cannot be accessed from the front panel. Once the hardware is set up, data is taken and time records are processed according to the needs of the specific test. Some tests monitor overloads, others require spectrum data, and others require time record data. After the data is collected, it is compared to an internal reference specification to determine if the self test passed or failed. The pass or fail information along with any additional information is placed in the Test Log.

Individual Self-Test Descriptions

- [187.5 kHz REFERENCE]
(Source 187.5 kHz) This test verifies that the reference signal is present at the input of the 187.5 kHz limiter on the Source Conversion assembly. In this test, a detector forces 187.5_SIG\ low if the 187.5_KHZ_SRCE signal is present. The Source Amplifier assembly provides control logic for 187.5_SIG\ and sends this information to the CPU assembly over the IIC bus.
- [10 MHz LOCAL OSC]
(Receiver 10 MHz) This test verifies that the swept LO signal, 300 MHz, 10 MHz, and 250 kHz reference signals are at the proper frequency. In this test, the 10 MHz calibration signal from the Reference/Calibrator assembly is connected to the receiver (the Input, First Conversion, Second Conversion, IF, and ADC/Digital Filter assemblies). This test then checks the output frequency of the ADC on the ADC/Digital Filter assembly.
- [2ND IF LEVEL]
(Receiver 2nd IF) This test verifies the integrity of the signal path through the Input, First Conversion, and Second Conversion assemblies up to the IF assembly. In this test the receiver's range is set to -20 dBm and a 0 dBm signal (NORMALIZE) from the Source Amplifier assembly is connected to the Input assembly. The detector on the IF assembly forces SIG_DET high. The receiver's range is changed to 0 dBm, and SIG_DET returns to a logic low. The ADC/Digital Filter assembly provides the control logic for the SIG_DET signal and sends this information to the CPU assembly over the IIC bus.
- [ADC]
(Receiver ADC) This test verifies that the ADC on the ADC/Digital Filter assembly is functioning correctly. This test consists of 7 tests – positive overflow, negative overflow, positive limit, negative limit, 1st pass, 2nd pass, and zero. The positive and negative overflow tests set up the ADC test mode to cause positive and negative overflows, then checks the digital filter for interrupt flags. The positive and negative limit tests check the ADC's positive and negative limits. The 1st and 2nd pass tests connect the 10 MHz calibration signal from the Reference/Calibrator assembly to the Input assembly. The 1st pass test sets the 2nd pass result to zero and checks the signal into the ADC for the proper value and the gate array for interrupts or overloads. The 2nd pass test sets the 1st pass result to zero and checks the signal into the ADC for the proper value and the gate array for interrupts or overloads. The zero test checks for minimal output when the signal is removed.
- [AUTO RNG TRIP PTS]
(Receiver autorange) This test verifies that the receiver's auto range trip points are set correctly. This test calibrates the source at -20 dBm, then connects the NORMALIZE signal from the Source Amplifier assembly to the Input assembly. The NORMALIZE signal is increased until the range up trip point is found, then decreased until the range down trip point is found. This test compares the trip points to acceptable levels.

- [DETECTOR]
(Detector gate array) This test verifies that the detector on the ADC/Digital Filter assembly is operating correctly. The microprocessor on the CPU assembly writes data to the detector over the fast bus. The microprocessor then reads the data and compares it to the data sent.
- [DIGITAL FILTER]
(Digital filter gate array) This test verifies that the digital filter's gate array on the ADC/Digital Filter assembly is operating correctly. The CPU assembly's microprocessor configures the digital filter's gate array over the fast bus. The microprocessor then reads the control lines to check circuits internal to the gate array and verify correct configuration. This test also writes to and reads from the gate array's RAM, checking for stuck bits.
- [DISK CONTROLLER]
(Disk controller) This test verifies that the disk controller on the CPU assembly is operating correctly. In this test, the microprocessor sends an invalid command to the disk controller, and the disk controller reports the command as invalid.
- [DISPLAY DIGITAL HW]
(Display digital) This test checks that the display controller on the CPU assembly is operating correctly. In this test, the microprocessor writes a pattern to the display controller, then reads the pattern checking for errors.
- [DMA]
(DMA) This test checks the DMA controller on the CPU assembly. In this test, the microprocessor writes to the DMA controller, then reads the registers checking for errors.
- [FAST BUS]
(Fast bus) This test verifies that the fast bus is operating correctly. In this test, the microprocessor on the CPU assembly writes data to the detector gate array on the ADC/Digital Filter assembly over the fast bus. The microprocessor then reads data.
- [FLATNESS]
(Source flatness) This test verifies the flatness of the source (Source Conversion and Source Amplifier assemblies) for all attenuator settings (10 dBm to - 50 dBm in 10 dB steps) from 200 kHz to 150 MHz. This test connects the NORMALIZE signal from the Source Amplifier assembly to the Input assembly. The receiver (the Input, First Conversion, Second Conversion, IF, and ADC/Digital Filter assemblies) measures the signal, and the microprocessor on the CPU assembly compares the results to acceptable levels.
- [FRONT PANEL]
(Front panel) This test verifies that the IIC controller on the Front Panel assembly is operating correctly. In this test, the microprocessor on the CPU assembly reads the IIC controller on the Front Panel assembly and verifies that no front-panel keys are held down.
- [GILBERT CELL]
(Source gilbert cell) This test verifies that the gilbert cell multiplier on the Source Conversion assembly is operating correctly. In this test, the gilbert cell generates a full scale signal and a detector forces 187.5_SIG\ low. The gilbert cell reduces its amplitude and 187.5_SIG\ returns to a logic high. The Source Amplifier assembly provides control logic for 187.5_SIG\ and sends this information to the CPU assembly over the IIC bus.

[HP-IB CONNECTOR]

This is a user-interactive test of the HP-IB connector on the CPU assembly. In this test, a diagram of the HP-IB connector is displayed on the screen. The user then connects an HP-IB pin to ground, and the pin is highlighted on the screen. See Test 12. HP-IB/RS-232 for the procedure to use with this softkey.

[HP-IB FUNC TEST]
(HP-IB)

This test verifies that the HP-IB interface on the CPU assembly is operating correctly. In this test, the microprocessor sets the HP-IB interface to a listen only state, then tests for a listen only state.

[IIC BUS]
(IIC bus)

This test verifies that the CPU assembly can write to and read from all assemblies with IIC interfaces. This test also checks the CPU assembly's EEROM. The following assemblies have IIC interfaces:

- Front Panel
- A11 Input
- A23 Step Phase Detector
- A31 Reference/Calibrator
- A33 Trigger
- A41 Source Conversion
- A42 Source Amplifier (write only)
- A51 Interpolation VCO
- A52 Fractional-N
- A62 ADC/Digital Filter

[INTERRUPT]
(Interrupt)

This test verifies that the interrupt circuits on the CPU assembly are operating correctly. In this test, the microprocessor writes to the interrupt registers and reads the registers for verification.

[LONG CONF TEST]

This test performs most of the self tests. The tests are performed in the following order:

[PROCESSOR]
[RAM]
[ROM]
[INTERRUPT]
[MULTI FCTN PERIPHERL]
[DISPLAY DGTL HW]
[FRONT PANEL]
[HP-IB FUNC TEST]
[IIC BUS]
[FAST BUS]
[DMA]
[MATH COPROC SSR]
[SNGL LOOP TUN RANGE]
[MULT-LOOP TUN RANGE]
[POST DIVIDER]
[AUTO RNG TRIP PTS]
[10 MHz LOCAL OSC]
[2ND IF LEVEL]
[ADC]
[DIGITAL FILTER]
[DETECTOR]
[187.5 kHz REFERENCE]
[GILBERT CELL]
[OUTPUT CKTS]
[FLATNESS]
[QUICK CONF TEST]

[MATH COPROC SSR]
(Math coprocessor)

This test verifies the processing capability of the TMS320 signal processor on the CPU assembly. In this test, the microprocessor reads from and writes to the TMS320's SRAM. This test also does two cyclic redundancy checks on the TMS320's SRAM contents.

[MOTOR]
(Disk motor)

This test verifies that the Disk Drive assembly's motor is operating correctly. In this test, the CPU assembly's disk controller instructs the Disk Drive assembly to turn its motor on and off. While the motor is turning on and off, the disk controller monitors the DISK_READY\ signal. This test requires a flexible disk.

[MULT FCTN PERIPHERL]
(Mult fctn peripheral)

This test verifies that the MFP (multi-function peripheral) on the CPU assembly is operating correctly. In this test, the microprocessor writes to the MFP, then reads the registers checking for errors.

- [MULT-LOOP TUN RANGE] This test checks the tuning range of the local oscillator's interpolation loop
(Mult loop tuning range) (Interpolation VCO and Fractional-N assemblies). In this test, the local oscillator is in multiple loop mode and the Interpolation VCO's frequency is set to a minimum locking value. Then while monitoring the interpolation loop for an unlock condition, the Interpolation VCO's frequency is decreased until the loop unlocks. This test then sets the Interpolation VCO's frequency to a valid locking value and checks that the loop locked. Next this test sets the Interpolation VCO's frequency to a maximum locking value. Then while monitoring the interpolation loop for an unlock condition, the Interpolation VCO's frequency is increased until the loop unlocks. This test then sets the Interpolation VCO's frequency to a valid locking value and checks that the loop locked.
- [OUTPUT CKTS] This test checks the output of the Source Amplifier assembly and verifies that the
(Source output level) source can reduce its amplitude. In this test, the overload threshold is lowered and the overload detection circuit detects an overload. Then the source amplitude is reduced, and the overload detection circuit verifies that the overload is gone.
- [POST DIVIDER] This test checks for proper operation of the divide-by-10/divide-by-5 circuit on the
(Post divider) Interpolation VCO assembly. In this test, the local oscillator is in multiple loop mode, and the 10 MHz calibration signal is connected to the receiver. While the receiver is measuring the signal, the divide by number is changed from 10 to 5. This causes the frequency the receiver is measuring to change, indicated by the receiver unable to measure the calibration signal.
- [PROCESSOR] This test verifies that the microprocessor on the CPU assembly is operating
(Processor) correctly. In this test, the following microprocessor operations are tested:
 Immediate move and compare instructions
 Data and address registers
 Data direct and address direct addressing modes
 AND, EOR, OR, multiply, divide, shift, and rotate

[QUICK CONF TEST]
(Quick confidence)

This test calibrates the analyzer and checks the calibration limits. See "Calibration Routine Description" in section IV, "Circuit Descriptions," for a description of the calibration routine. This test lists the following calibration correction information in the test log:

LO null real: n, imag: n
1 MOhm nominal crtn: n
50 Ohm nominal crtn: n
src crtn: gain: n, offset: n

The **LO null real** and **imag** numbers are the calibration correction numbers to null the receiver's LO feedthrough. These numbers can range from 1 to 100, but typically range from 40 to 90. The nominal number is 50. This test fails if either the real or the imaginary number is 1 or 100.

The **1 MOhm** and **50 Ohm nominal crtn** numbers are the calibration correction numbers for the receiver's 1 M Ω input path and 50 Ω input path (– 20 dBm range, no attenuators engaged). The nominal number is 1.0 with typical numbers ranging from 0.4 to 2.5. When either the 1 M Ω or the 50 Ω input path can not be calibrated, this test fails and the correction number is set to 1.000 (no correction applied).

The **src crtn gain** and **offset** numbers are the calibration gain and offset correction numbers for the source. The nominal number for gain is 1.00 with typical numbers ranging from 0.7 to 1.4. The nominal number for offset is 0 with typical numbers ranging from – 5 to 7.

[RAM]
(RAM)

This test checks the RAM on the Memory assembly. Before writing to a memory location, this test stores the memory contents in a register. The memory location is restored after the memory is tested. This test disables the keyboard and all interrupts.

[RANDOM SEEK]
(Disk random seek)

This test verifies that the Disk Drive assembly's head can move to a random sector on the flexible disk. In this test, the disk controller on the CPU assembly instructs the disk-drive head to move to a random sector. This test requires a flexible disk that is not write protected.

[READ]
(Disk read)

This test verifies that the Disk Drive assembly can read a flexible disk. In this test, the CPU assembly's disk controller instructs the Disk Drive assembly to read the current sector on the flexible disk. While the current sector is being read, the disk controller monitors the READ_DATA\ signal to verify the read operation. The current sector is set by the [SEEK SECTOR] test. This test requires a flexible disk that is not write protected.

[READ/WRITE]
(Disk read/write)

This test verifies that the Disk Drive assembly can read and write to a flexible disk. In this test, the CPU assembly's disk controller instructs the Disk Drive assembly to read the current sector on the flexible disk. While the current sector is being read, the disk controller monitors the READ_DATA\ signal to verify the read operation. The disk controller then instructs the Disk Drive assembly to write to the current sector. While the current sector is being written to, the disk controller monitors the WRITE_DATA\ signal to verify the write operation. The current sector is set by the [SEEK SECTOR] test. This test requires a flexible disk that is not write protected.

[READ/WRITE ALL]
(Disk read/write all)

This test verifies that the Disk Drive assembly can read and write to all sectors of a flexible disk. In this test, the CPU assembly's disk controller instructs the Disk Drive assembly to read every available sector on the flexible disk (excluding privileged tracks). While the flexible disk is being read, the disk controller monitors the READ_DATA\ signal to verify the read operation. The disk controller then instructs the Disk Drive assembly to write to every available sector on the flexible disk (excluding privileged tracks). While the flexible disk is being written to, the disk controller monitors the WRITE_DATA\ signal to verify the write operation. This test stops on the first error. If there are no errors, this test takes approximately 20 minutes to complete. This test requires a flexible disk that is not write protected.

[RESTORE]
(Disk restore)

This test verifies that the Disk Drive assembly's head can move away from track 0, then back to track 0. In this test, the CPU assembly's disk controller instructs the disk-drive head to move away from track 0, then back to track 0. The disk controller monitors the T00\ signal to verify the move operation. This test requires a flexible disk that is not write protected.

[ROM]
(ROM)

This test calculates and verifies checksums for all ROMs on the Memory assembly.

[SEEK SECTOR]
(Disk sector seek)

This test verifies that the Disk Drive assembly's head can move to a user specified sector on the flexible disk. In this test, the disk controller on the CPU assembly instructs the disk-drive head to move to a user specified sector. The user specified sector number must be in the range of valid sector numbers. The default sector number is 1. This test requires a flexible disk that is not write protected.

[SNGL LOOP TUN RANGE]
(Single loop tuning range)

This test checks the tuning range of the local oscillator's single loop (Sum VCO, Interpolation VCO, and Fractional-N assemblies). In this test, the local oscillator is in single loop mode and the Sum VCO's frequency is set to a minimum locking value. Then while monitoring the single loop for an unlock condition, the Sum VCO's frequency is decreased until the loop unlocks. This test then sets the Sum VCO's frequency to a valid locking value and checks that the single loop locked. Next this test sets the Sum VCO's frequency to a maximum locking value. Then while monitoring the single loop for an unlock condition, the Sum VCO's frequency is increased until the loop unlocks. This test then sets the Sum VCO's frequency to a valid locking value and checks that the single loop locked.

[TEST PATTERN]

This is a user-interactive test of the Display assembly and the CPU assembly's display controller. In this test, a test pattern is displayed on the screen. See adjustment "18. Display," in section I, "Adjustments," for more information.

Table 5-32. Self Test Menu Map and HP-IB Commands

| Self Test | HP-IB Command |
|-------------------------|--------------------|
| [SELF TEST] | |
| [QUICK CONF TEST] | TEST:SHOR |
| [LONG CONF TEST] | TEST:LONG |
| [FUNCTIONL TESTS] | |
| [CPU] | |
| [PROCESSOR] | TEST:PROC:CPU |
| [RAM] | TEST:PROC:RAM |
| [ROM] | TEST:PROC:ROM |
| [INTERRUPT] | TEST:PROC:INT |
| [MULT FCTN PERIPHERL] | TEST:PROC:MFP |
| [DISPLAY DGTL HW] | TEST:PROC:DISP |
| [ALL] | TEST:PROC:ALL |
| [DISPLAY] | |
| [TEST PATTERN] | TEST:DISP:PATT |
| [DMA] | TEST:PROC:DMA |
| [I/O] | |
| [FRONT PANEL] | TEST:IO:FPAN |
| [HP-IB] | |
| [HP-IB FUNC TEST] | TEST:IO:GPIB |
| [HP-IB CONNECTOR] | |
| [INTERNAL DISK] | |
| [DISK CONTROLLR] | TEST:IO:DISK:CONT |
| [MOTOR] | TEST:IO:DISK:MOT |
| [RESTORE] | TEST:IO:DISK:REST |
| [RANDOM SEEK] | TEST:IO:DISK:RAND |
| [SEEK SECTOR] | TEST:IO:DISK:SEEK |
| [READ] | TEST:IO:DISK:READ |
| [READ/WRITE] | TEST:IO:DISK:WRIT |
| [READ/WRITE ALL] | TEST:IO:DISK:RWR |
| [ALL] | TEST:IO:DISK:ALL |
| [IIC BUS] | TEST:IO:IIC |
| [FAST BUS] | TEST:IO:FBUS |
| [ALL] | TEST:IO:ALL |
| [MATH COPROCSSR] | TEST:MATH |
| [LOCAL OSC] | |
| [SNGL LOOP TUN RANGE] | TEST:LOSC:SLO:TRAN |
| [MULT-LOOP TUN RANGE] | TEST:LOSC:MLO:TRAN |
| [POST DIVIDER] | TEST:LOSC:PDIV |
| [ALL] | TEST:LOSC:ALL |

Table 5-32. Self Test Menu Map and HP-IB Commands (continued)

| Self Test | HP-IB Command |
|-------------------------|-------------------------------|
| [RECEIVER] | |
| [AUTO RNG TRIP PTS] | TEST:REC:AUT |
| [10 MHz LOCAL OSC] | TEST:LOCS:TENM |
| [2ND IF LEVEL] | TEST:IF:LEV |
| [ADC] | TEST:REC:GARR |
| [DIGITAL FILTER] | TEST:DFIL:GARR |
| [DETECTOR] | TEST:DET:GARR |
| [ALL] | TEST:REC:ALL |
| [SOURCE] | |
| [FLATNESS] | TEST:SOUR:FLAT |
| [187.5 kHz REFERENCE] | TEST:SOUR:REF |
| [GILBERT CELL] | TEST:SOUR:GILB |
| [OUTPUT CKTS] | TEST:SOUR:DAC:ATT † |
| [ALL] | TEST:SOUR:ALL |
| [ALL] | TEST:ALL |
| [LOOP MODE ON OFF] | TEST:LOOP ON TEST:LOOP OFF |
| [TEST LOG] | TEST:LOG:DATA? |
| [CLEAR TEST LOG] | TEST:LOG:CLE |
| [NEXT PAGE] | |
| [PREVIOUS PAGE] | |

† This test will fail if the Source Amplifier assembly detects a voltage at its front-panel connector. Therefore, before running this test, disconnect any cable connected to the SOURCE connector.

Note

To view the analyzer's fault log via HP-IB, send SYST:FLOG:DATA?. To clear the fault log send SYST:FLOG:CLE.

Index

A

ADC

- adjustments 1-22
- circuit description 4-38
- adjustments
 - HP-IB commands for setup 1-4
 - required after replacing assembly 5-6
- amplitude accuracy troubleshooting 5-68
- API spurs adjustment 1-12
- assembly part numbers and locations 2-6
- attenuation
 - source DAC 4-31
 - source pads 4-29
- autorange
 - circuit description 4-9
 - threshold adjustment 1-37

B

- battery part number 2-12
- battery-backed-up memory
 - circuit description 4-46
 - states stored in 4-86
 - troubleshooting 5-88
- binary to hexadecimal conversion 5-92
- bus
 - See fast bus
 - See IIC bus

C

- cable part numbers 2-8
- cables
 - See RF cables
 - See ribbon cables
- calibration routine
 - correction curves 4-79
 - description 4-77
 - swept and fixed mode 4-24
 - troubleshooting failing 5-30
- calibrator flatness and level adjustment 1-42
- card nest removal 2-24
- coax cables
 - See RF cables

connector

- external reference 4-24
- external trigger 4-27
- input 4-9
- probe power 4-51
- source 4-29

correction curves

- See calibration routine

CPU

- circuit description 4-40
- removal 2-19
- replacing 2-7
- See also disk drive cable
- See also display cable
- See also front panel cable
- See also memory cable
- CPU power cable
 - signal connections 4-53
 - signal descriptions 4-63

CRT

- See display

D

- disassembly 2-13
- disk drive
 - circuit description 4-48
 - controller 4-45
 - removal 2-20
- disk drive cable
 - signal connections 4-54
 - signal descriptions 4-64
- display
 - adjustment 1-44
 - circuit description 4-48
 - controller 4-45
 - removal 2-21
 - troubleshooting 5-8
- display cable
 - signal connections 4-54
 - signal descriptions 4-64
- distortion troubleshooting
 - input harmonic 5-68, 5-80
 - intermodulation 5-68, 5-82
 - source harmonic 5-68

Index (Continued)

E

- equipment required
 - See HP 3588A Performance Test Guide
- error messages
 - See fault log
 - See test log
- exchange assembly part numbers 2-6
- expanded memory circuit description 4-46
- external frequency reference 4-24, 4-70
- external trigger
 - signal description 4-70
 - See also trigger

F

- fan
 - circuit description 4-47
 - removal 2-22
 - troubleshooting 5-89
- fast bus
 - ADC/Digital Filter 4-38
 - CPU 4-40
 - interface 4-44
 - troubleshooting 5-8
- fast bus cable
 - signal connections 4-55
 - signal descriptions 4-66
- fault log
 - messages 4-82
 - to display 4-78
- first IF bandpass filter adjustment 1-34
- flatness adjustment
 - calibrator 1-42
 - receiver 1 meg ohm 1-37
- frequency accuracy troubleshooting 5-68, 5-78
- frequency reference
 - block diagram 4-8
 - IIC controller 4-44
- frequency reference adjustments
 - calibrator flatness and level 1-42
 - high frequency 1-7
 - oven frequency 1-40
 - oven shutdown 1-5
 - primary frequency reference 1-6
- frequency reference circuit description
 - A31 Reference/Calibrator 4-24
 - A32 300 MHz 4-26
 - A33 Trigger 4-27
 - overall 4-2
- frequency response troubleshooting 5-68

- front panel
 - circuit description 4-47
 - IIC controller 4-44
 - removal 2-18
 - troubleshooting 5-8
- front panel cable
 - signal connections 4-55
 - signal descriptions 4-66
- fuse 2-12

H

- hardware part numbers 2-10
- harmonic distortion troubleshooting
 - input 5-68, 5-80
 - source 5-68
- high-frequency reference adjustment 1-7
- HP-IB
 - circuit description 4-44
 - setting address 2-7
 - troubleshooting 5-30
- HP-IB commands
 - for adjustment setup 1-4
 - for self tests 5-104
- HP-IB connector
 - signal descriptions 4-76
 - signals 4-60
- HP-IB trigger
 - signal description 4-68
 - See also trigger

I

- IBASIC 4-1
- IIC bus
 - signals 4-44
 - See also CPU power cable
 - See also front panel cable
 - See also motherboard power cable
 - See also motherboard, signals
- image responses troubleshooting 5-68
- initial verification 5-8
- input
 - See receiver
- input connector 4-9
- input harmonic distortion troubleshooting 5-68, 5-80
- input return loss troubleshooting 5-68
- installation
 - See HP 3588A Performance Test Guide
- intermittent failures 5-30
- intermodulation distortion troubleshooting 5-68, 5-82
- interpolation VCO adjustment 1-9

K

keyboard
See front panel

L

local oscillator
 block diagram 4-7
 IIC controller 4-44

local oscillator adjustments
 100 kHz and API spurs 1-12
 interpolation VCO 1-9
 multiple loop clamps 1-17
 pretune offset and slope 1-20
 single loop clamps 1-11
 step VCO filter 1-18
 sum VCO filter 1-15

local oscillator circuit description
 A21 Sum VCO 4-13
 A22 Sum Phase Detector 4-19
 A23 Step Phase Detector 4-21
 A24 Step VCO 4-23
 A51 Interpolation VCO 4-33
 A52 Fractional-N 4-35
 multiple loop mode 4-15 - 4-16
 overall 4-2
 single loop mode 4-15

local oscillator feedthrough
 troubleshooting 5-68, 5-70
 See also calibration routine, description

local oscillator unlocked 5-30

log scale accuracy troubleshooting 5-68, 5-85

M

memory
 circuit description 4-46
 removal 2-16
 replacing 2-7

memory cable
 signal connections 4-53
 signal descriptions 4-61

miscellaneous failures, troubleshooting 5-88

motherboard
 circuit description 4-47
 signal connections 4-58
 signal descriptions 4-73
 voltage connections 4-59

motherboard power cable
 signal connections 4-56
 signal descriptions 4-68

multiple loop
 control voltage clamps adjustment 1-17
 frequency matrix 4-18

N

narrow-band zoom 4-1, 4-15

noise troubleshooting
 input level 5-68, 5-76
 phase 5-68, 5-71
 source 5-68

nonvolatile states 4-86

nonvolatile states not saved
 See battery-backed-up memory

O

oven
 circuit description 4-47
 frequency adjustment 1-40
 removal 2-22
 shutdown adjustment 1-5

overall instrument description 4-1

P

part numbers
 assemblies 2-6
 cables 2-8
 hardware 2-10

performance tests
 required after replacing assembly 5-6
 troubleshooting failing 5-30
 See also HP 3588A Performance Test Guide
 See also HP 3588A Semiautomated Performance Test Guide

phase noise troubleshooting 5-68, 5-71

power supply
 circuit description 4-48
 connectors 4-52
 test board nominal voltage values 5-10
 test position 2-17
 troubleshooting 5-8
 voltage distribution 4-51
 See also CPU power cable
 See also motherboard power cable

power-on states 4-84

power-on test
 descriptions 5-91
 messages 5-93
 troubleshooting using 5-14

preset states 4-84

pretune offset and slope adjustment 1-20

primary frequency reference adjustment 1-6

probe power voltages 4-51

Index (Continued)

R

- rear panel removal 2-15
- receiver
 - block diagram 4-6
 - IIC controller 4-44
- receiver adjustments
 - first IF filter 1-34
 - flatness and autorange 1-37
 - second IF bandpass filter 1-28
- receiver circuit description
 - A11 Input 4-9
 - A12 First Conversion 4-11
 - A13 Second Conversion 4-12
 - A61 IF 4-37
 - A62 ADC/Digital Filter 4-38
 - overall 4-2
- recommended test equipment
 - See HP 3588A Performance Test Guide
- reference level accuracy troubleshooting 5-68
- reference output 4-71
- replaceable part numbers
 - assemblies 2-6
 - cables 2-8
 - hardware 2-10
- residual responses troubleshooting 5-68, 5-75
- return loss troubleshooting
 - input 5-68
 - source 5-68
- RF cables
 - signal connections 4-57
 - signal descriptions 4-69
- ribbon cables
 - signal connections 4-50
 - signal descriptions 4-61

S

- safety 5-1
 - See front matter
- sample and hold spur adjustment 1-12
- screen
 - See display
- second IF bandpass filter adjustment 1-28
- self tests
 - assemblies used in 5-95
 - circuits not tested by 5-30
 - descriptions 5-94
 - HP-IB commands 5-104
 - troubleshooting guide 5-33
 - troubleshooting using 5-30
- serial number
 - entering after replacing CPU 2-7
- service functions softkey 4-78

- signal descriptions 4-61
- single loop control voltage clamps adjustment 1-11
- SMB cables
 - See RF cables
- source
 - bandpass filter adjustment 1-31
 - block diagram 4-8
 - connector 4-29
 - IIC controller 4-44
- source circuit description
 - A41 Source Amplifier 4-29
 - A42 Source Conversion 4-31
 - overall 4-2
- source troubleshooting
 - amplitude accuracy and frequency response 5-68, 5-84
 - dynamic accuracy 5-68
 - harmonic distortion 5-68
 - noise 5-68
 - return loss 5-68
 - spurious responses 5-68
- specifications
 - See HP 3588A Performance Test Guide
- spurious responses troubleshooting 5-68, 5-79
- states
 - nonvolatile 4-86
 - power-on 4-84
 - preset 4-84
- step VCO filter adjustment 1-18
- sum VCO filter adjustment 1-15
- swept spectrum 4-1, 4-15

T

- test log 5-32
- top cover removal 2-14
- tracking generator
 - See source
- trigger
 - circuit description 4-27
 - output signal 4-72
 - troubleshooting 5-90
- troubleshooting
 - fan power 5-89
 - guide 5-4
 - hints 5-3
 - memory battery 5-88
 - trigger 5-90

V

voltages

motherboard 4-59

power supply distribution 4-51

power supply test board nominal values 5-10

