OPERATING AND SERVICE MANUAL

HP 436A
POWER METER
(Including Options 003, 004 and 022)

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed 2410A and 2410U.

With changes described in Section VII, this manual also applies to instruments with serial numbers prefixed 1447A, 1448A, 1451A, 1501A, 1503A, 1504A, 1505A, 1538A, 1550A, 1606A, 1611A, 1629A, 1713A, 1725A, 1746A, 1803A, 1908A, 1911A, 1917A, 1918A, 1930A, 2008A, 2016A, 2101A, 2236A, 2330A, 2347A and 2347U.

For additional important information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section I.

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SECTION VIII
SERVICE

8-1. INTRODUCTION

8-2. This section provides principles of operation, troubleshooting procedures, and general service information for the Power Meter. The specific content and arrangement of this section is outlined below.

a. **Safety Considerations:** Provides general safety precautions that should be observed when working on the Power Meter.

b. **Recommended Test Equipment:** Defines the test equipment and accessories required to maintain the Power Meter.

c. **Service Aids:** Provides general information useful in servicing the Power Meter.

d. **Repair:** Provides general information for replacing factory selected components and instrument disassembly procedures.

e. **Basic Circuit Descriptions:** Describes the functional operation of linear and digital integrated circuits used in the Power Meter.

f. **Troubleshooting:** Provides step-by-step procedures for checkout and troubleshooting of a standard instrument, and a verification program for checkout and troubleshooting of an HP-IB equipped instrument. (Additional circuit troubleshooting data is provided as required on the individual service sheets located at the end of the section.)

g. **Principles of Operation:** Principles of operation are provided on two levels in this section. The first level is a block diagram description which covers the overall operation of the Power Meter in detail and is located at the end of the section just before the service sheets. The second level consists of detailed circuit theory descriptions which are provided as required on the individual service sheets with the appropriate schematics.

h. **Service Sheets:** Foldout service sheets are provided at the end of the section. Service Sheet 1 is an overall block diagram which illustrates major signal flow and circuit dependency and is keyed, by the numbers in the lower, right-hand corners of the individual blocks on the diagram, to the detailed block diagrams. The detailed block diagrams provide an assembly-by-assembly description of instrument operation and are keyed to the service sheets containing schematics which follow them.

NOTE

Figure 8-1, Schematic Diagram Notes, explains any unusual symbols that appear on the schematics and the switch-wafer numbering system.

8-3. SAFETY CONSIDERATIONS

8-4. Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition (see Sections II, III, and V). Service and adjustments should be performed only by qualified service personnel.

WARNING

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnection of the protective earth terminal is likely to make the instrument dangerous. Intentional interruption is prohibited.

8-5. Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

8-6. Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

8-7. Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement.

SCHEMATIC DIAGRAM NOTES

Resistance in ohms, capacitance in picofarads, inductance in millihenries unless otherwise noted.

* Asterisk denotes a factory-selected value. Value shown is typical. Part may be omitted.

Tool-aided adjustment. Manual control.

Encloses front-panel designation.

Encloses rear-panel designation.

Circuit assembly borderline.

Other assembly borderline. Also used to indicate mechanical interconnection (ganging).

Heavy line with arrows indicates path and direction of main signal.

Heavy dashed line with arrows indicates path and direction of main feedback.

CW — Wiper moves toward CW with clockwise rotation of control (as viewed from shaft or knob).

Numbered Test Point. Measurement aid provided.

Lettered Test Point. No measurement aid provided.

Encloses wire color code. Code used is the same as the resistor color code. First number identifies the base color, second number identifies the wider stripe, third number identifies the narrower stripe. E.g., (947) denotes white base, yellow wide stripe, violet narrow stripe.

A direct conducting connection to the earth, or a conducting connection to a structure that has a similar function (e.g., the frame of an air, sea, or land vehicle).

A conducting connection to a chassis or frame.

Common connections. All like-designated points are connected.

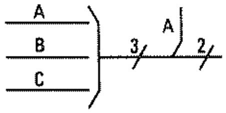
Letter = off-page connection.
Number = Service Sheet number for off-page connection.

THIS PAGE — Number (only) = on page connection.

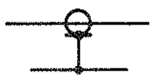
Figure 8-1. Schematic Diagram Notes (1 of 3)

Service Model 436A

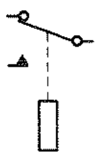
SCHEMATIC DIAGRAM NOTES



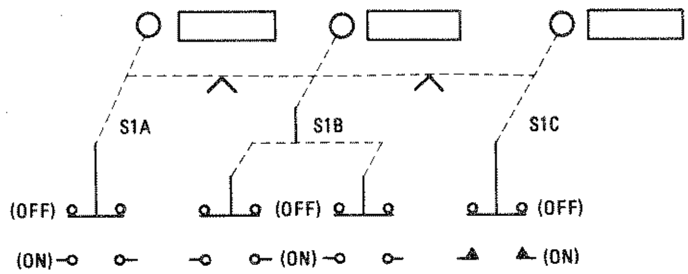
Indicates multiple paths represented by only one line. Letters or names identify individual paths. Numbers indicate number of paths represented by the line.



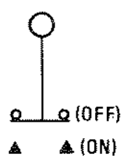
Coaxial or shielded cable.



Relay contact moves in direction of arrow when energized.



Indicates interlocked pushbutton switches with one momentary switch section. Only one switch section can be (ON) at a time. Depressing one switch section releases any other switch section.



Indicates a pushbutton switch with a momentary (ON) position.

SWITCH DESIGNATIONS

EXAMPLE: A3S1AR(2-1/2)

A3S1 = SWITCH S1 WITHIN ASSEMBLY A3

A = 1ST WAFER FROM FRONT (A=1ST, ETC)

R = REAR OF WAFER (F=FRONT)

(2-1/2) = TERMINAL LOCATION (2-1/2) (VIEWED FROM FRONT)

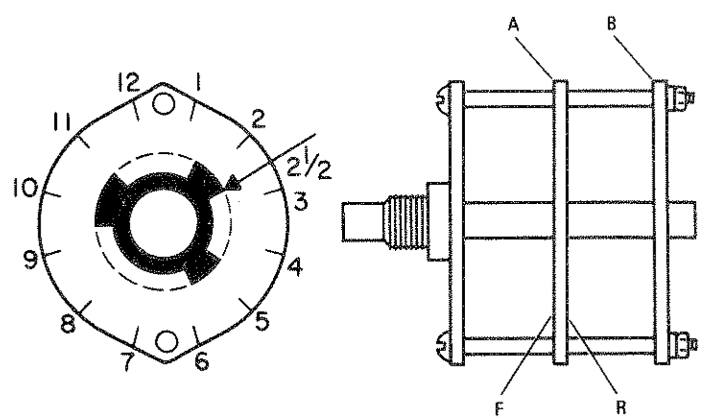


Figure 8-1. Schematic Diagram Notes (2 of 3)

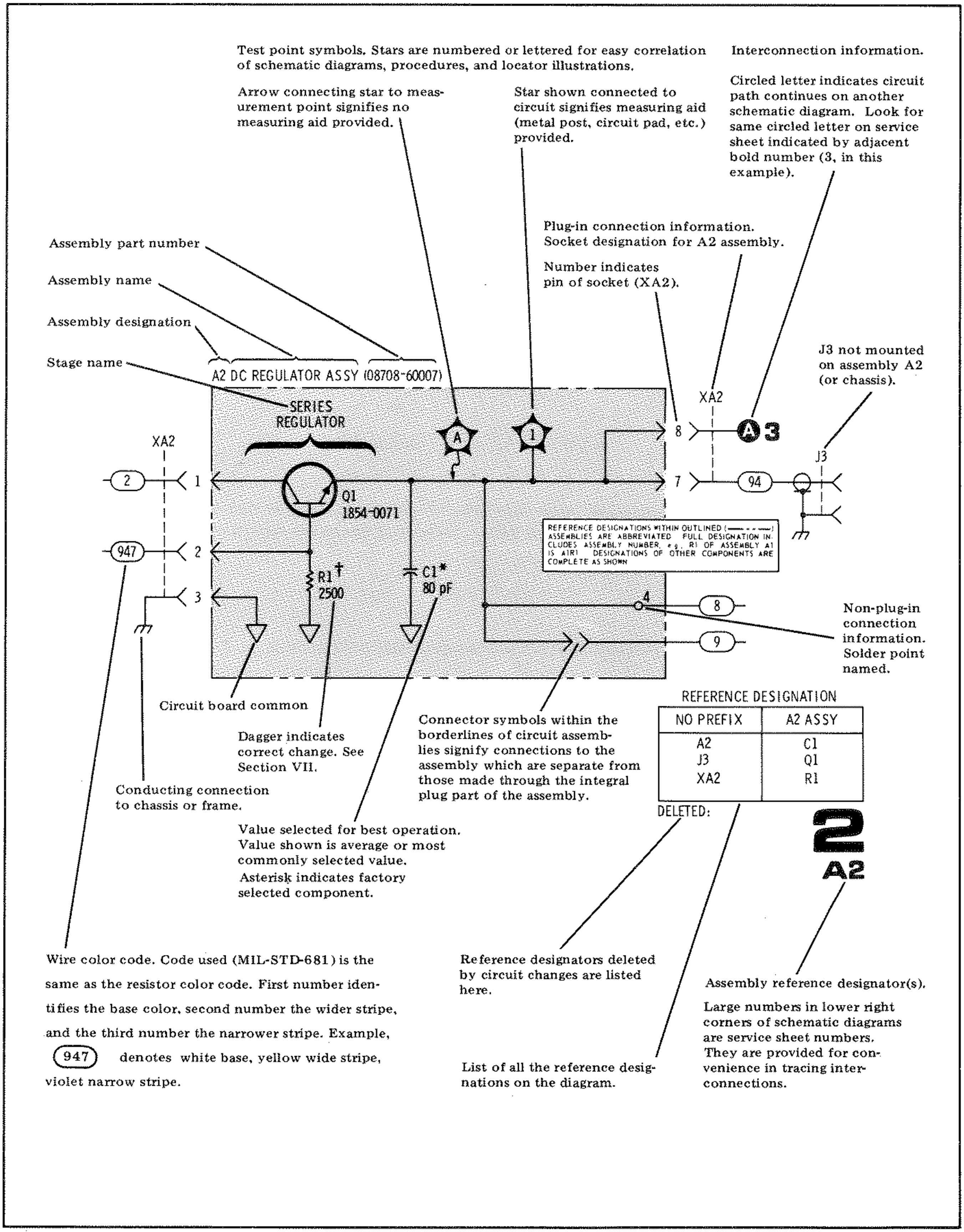


Figure 8-1. Schematic Diagram Notes (3 of 3)

Safety Considerations (cont'd)
The use of repaired fuses and the short-circuiting of fuseholders must be avoided.

8-8. Whenever it is likely that this protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

WARNING

The service information is often used with power supplied and protective covers removed from the instrument. Energy available at many points may, if contacted, result in personal injury.

8-9. RECOMMENDED TEST EQUIPMENT

8-10. Test equipment and test equipment accessories required to maintain the Power Meter are listed in Table 1-2. Equipment other than that listed may be used if it meets the listed critical specifications.

8-11. SERVICE AIDS

8-12. Pozidriv Screwdrivers. Many screws in the instrument appear to be Phillips, but are not. To avoid damage to the screw slots, Pozidriv screwdrivers should be used.

8-13. Blade Tuning Tools. For adjustment of the front panel CAL ADJ control a special tuning tool is provided (HP Part Number 8710-0630). In situations not requiring non-metallic tuning tools, an ordinary small screwdriver or other suitable tool is sufficient. No matter what tool is used, never try to force any adjustment control in this instrument. This is especially critical when adjusting variable inductors or capacitors.

8-14. Part Location Aids. The locations of some chassis-mounted parts and the major assemblies are shown on the last foldout in this manual. The locations of individual components mounted on printed circuit boards or other assemblies are shown on the appropriate schematic diagram page or on the page opposite it. The part reference designator is the assembly designator plus the part designator (for example, A2R9 is R9 on the A2 assembly). For specific component description and ordering information refer to the parts list in Section VI.

8-15. Servicing Aids on Printed Circuit Boards. The servicing aids include test points, transistor and integrated circuit designations, adjustment callouts and assembly stock numbers.

8-16. REPAIR

8-17. Factory Selected Components

8-18. Some component values are selected at the time of final checkout at the factory (see Table 5-1). Usually these values are not extremely critical; they are selected to provide optimum compatibility with associated components. These components are identified on individual schematics by an asterisk (*). The recommended procedure for replacing a factory-selected part is as follows:

a. Try the original value, then perform the calibration test specified for the circuit in the performance and adjustment sections of this manual.

b. If calibration cannot be accomplished, try the typical value shown in the parts list and repeat the test.

c. If the test results are still not satisfactory, substitute various values within the tolerances specified in Table 5-1 until the desired result is obtained.

8-19. Disassembly and Reassembly Procedures

WARNINGS

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, if inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

8-20. Before performing any of the following disassembly or reassembly procedures, the following steps must be performed.

a. Set POWER ON-OFF switch to OFF position.

b. Remove Line Power Cable (W8) from Line Power Module (A11).

Disassembly and Reassembly Procedures (cont'd)

8-21. Top Cover Removal. To remove the top cover from the Power Meter follow the steps as listed below:

a. Remove Pozidriv screw from rear edge of top cover.

b. Slide top cover back until free from front frame and lift off. Reverse the procedure to replace the top cover.

8-22. Bottom Cover Removal. To remove the bottom cover from the Power Meter follow the steps as listed below:

a. Place Power Meter with bottom cover facing up.

b. Remove four plastic feet from bottom cover. Lift up on back edge of plastic foot and push back on front edge of plastic foot to free foot from bottom cover.

c. Remove captive Pozidriv screw from rear edge of bottom cover.

d. Slide bottom cover back until it clears rear frame. Reverse the procedure to replace the bottom cover.

8-23. Front Panel Removal. To remove the front panel from the Power Meter follow the steps as listed below:

a. Remove top and bottom covers.

b. Remove side trim strips from front frame.

c. Remove two Pozidriv screws from both sides of front frame.

d. Carefully push front panel from behind to free it from the front frame (see Figure 8-2).

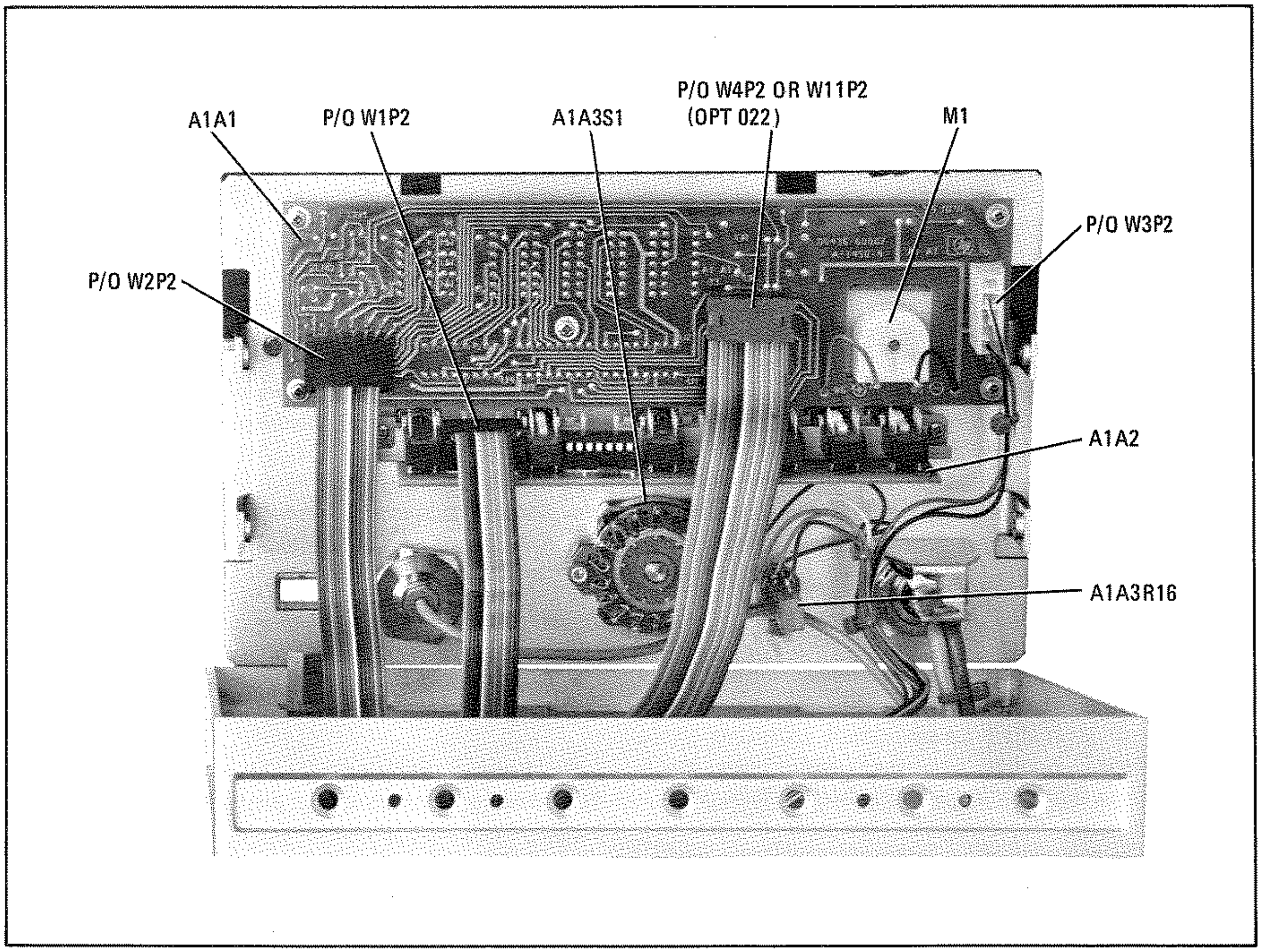


Figure 8-2. Front Panel Removal

Disassembly and Reassembly Procedures (cont'd)

e. Disconnect cables as necessary for access to front panel assemblies and components. Reverse the procedure to replace the front panel.

8-24. BASIC CIRCUIT DESCRIPTIONS

8-25. Linear Integrated Circuits

8-26. Operational Amplifiers. Operational amplifiers are used to provide such functions as summing and offsetting voltages, as buffer amplifiers, detectors, and in power supplies. The particular function is determined by the external circuit connections. Equivalent circuit and functional diagrams for typical operational amplifiers are contained in Figure 8-3. Circuit A is a non-inverting buffer amplifier with gain of one. Circuit B is a non-inverting amplifier with gain determined by the resistance of R1 and R2. Circuit C is an inverting amplifier with gain determined by R1 and R2, with the input impedance equal to R2. Circuit D shows the equivalent circuit and typical parameters for an operational amplifier.

NOTE

It is assumed that the amplifier has high gain, low output impedance and high input impedance.

8-27. Troubleshooting. An operational amplifier can be characterized as an ideal voltage amplifier having low output impedance, high input impedance, and very high gain. Also the output voltage is proportional to the difference in the voltages *applied* to the input terminals. In use, the amplifier drives the input voltage difference close to zero.

8-28. When troubleshooting an operational amplifier, measure the voltages at the two inputs with no signal applied; the difference between these voltages should be less than 10 mV. A difference voltage much greater than 10 mV indicates trouble in the amplifier or its external circuitry. Usually this difference will be several volts and one of the inputs will be very close to an applied circuit operating voltage (for example, +20V, −12V).

8-29. Measure the amplifier's output voltage. It will probably be close to one of the supply voltages or ground. Verify that the output voltage follows the input voltages, i.e., if the non-inverting input voltage is more positive than normal and/or if the inverting input voltage is more negative than normal, then the change in output voltage should be more positive. If the non-inverting input is less positive and/or the inverting input voltage is less negative, the change in output voltage should be less positive. The preceding symptoms indicate the defective component is in the external circuitry. If the symptoms as stated are absent, the operational amplifier is probably defective.

8-30. Digital Integrated Circuits and Symbols

8-31. Introduction. Except for two Read Only Memory (ROM) devices, all digital circuits used in this instrument belong to the TTL family. The two ROMs belong to the MOS family and are made TTL compatible via the use of pull-up resistors attached to the input/output ports. Refer to Table 8-1 for TTL and MOS input/output voltage level specifications, and for MOS input power requirements.

8-32. The symbols used in this manual conform to the requirements of American National Standard ANSI Y32.14-1973, "Graphic Symbols for Logic Diagrams (Two-State Devices)". Unless otherwise specified all symbols and signal mnemonics should be interpreted according to the following general rules:

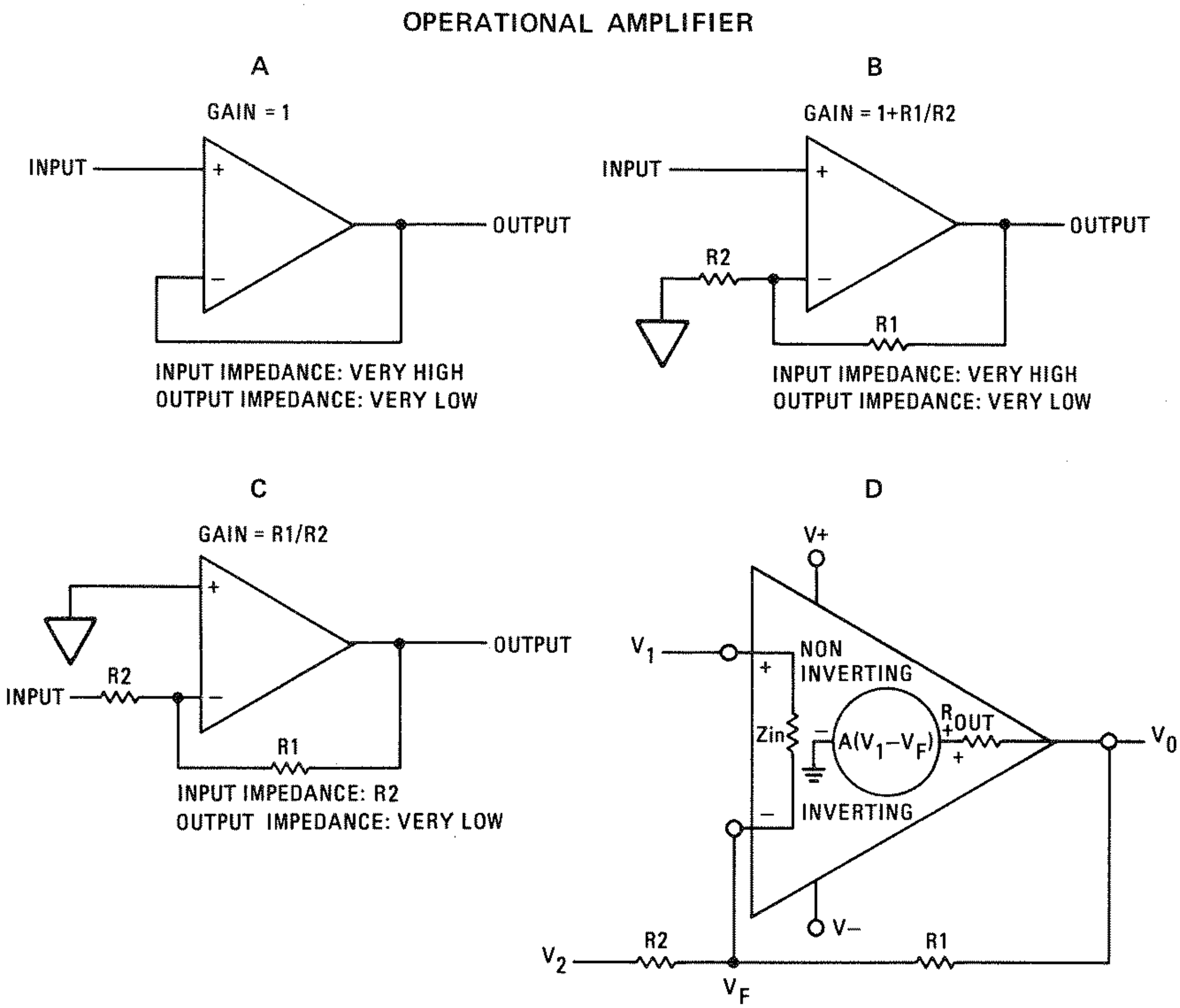
a. Signals that are active-low are identified by the letter L or N followed by the signal mnemonic (e.g., LQT).

b. Signals that are active-high are identified by the letter H or Y followed by the signal mnemonic (e.g., HLLD).

c. A polarity indicator symbol (◺) at an input indicates that it is active-low or triggers on a low going edge; a polarity indicator symbol at an output indicates inversion or that the output is active-low. Active-high inputs or inputs which trigger on a high going edge; and active-high outputs are shown without the polarity indicator symbol.

d. A dynamic indicator symbol (-▷) at an input indicates that the input triggers (is active) only on the leading or trailing edge of an input signal. If a polarity indicator symbol is present with the dynamic indicator symbol, then the input triggers on the negative edge of the input signal. Inputs that are not edge sensitive are referred to as level sensitive and are shown without the dynamic indicator symbol.

e. The output-delay indicator symbol (┐) indicates that the output is effective at the time



IF "A" IS LARGE, $V_F = V_1$

(1) $$V_0 = V_1\left(1+\frac{R1}{R2}\right) - V_2\left(\frac{R1}{R2}\right)$$

(2) IF $V_2 = 0$ (⏚), THEN $$V_0 = V_1\left(1+\frac{R1}{R2}\right)$$

(3) IF $V_1 = 0$ (⏚), THEN $$V_0 = -V_2\left(\frac{R1}{R2}\right)$$

Figure 8-3. Operational Amplifier Functional Circuits

Digital Integrated Circuits and Symbols (cont'd)

that the signal which initiates the change returns to its opposite state.

f. The inhibiting-input indicator symbol (+) indicates that the output is prevented from going to its indicated state as long as the inhibiting-input remains high. If an inhibiting-input indicator and a polarity indicator symbols are used together, the output will be inhibited as long as the inhibiting-input remains low. The inhibiting-input symbol is used mainly with three-state logic devices to allow the use of the "wired OR" connection of the outputs.

NOTE

The term "binary coded decimal" (BCD) refers to four-bit binary circuits that range from decimal 0 to 9 in an 8421 code.

The term "binary", when applied to four-bit binary circuits, refers to circuits that range from decimal 0 to 15 in an 8421 code.

Table 8-1. Logic Levels and Power Requirements

Logic	High =	Low =	Power Requirements
TTL	⩾2V	⩽0.8V	Gnd, +5V
MOS	Input ⩾4V Output ⩾2V	Input and output ⩽0.8V	Gnd V_{DD} +5V V_{GG} +12V V_{EE} −2V

8-33. Dual D-Type Flip-Flop. The dual D-type flip-flop shown in Figure 8-4 consists of two independent D-type flip-flops. The information present at the data (D_C) input is transferred to the active-high and active-low outputs on a low-to-high transition of the clock (C) input. The data input is then locked out and the outputs do not change again until the next low-to-high transition of the clock input.

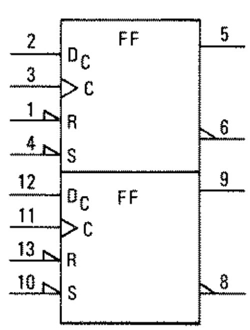


Figure 8-4. Dual D-Type Flip-Flop

8-34. The set (S) and reset (R) inputs override all other input conditions: when set (S) is low, the active-high output is forced high; when reset (R) is low, the active-high output is forced low. Although normally the active-low output is the complement of the active-high output, simultaneous low inputs at the set and reset will force both the active-low and active-high outputs to go high at the same time on some D-type flip-flops. This condition will exist only for the length of time that both set and reset inputs are held low. The flip-flop will return to some indeterminate state when both the set and reset inputs are returned to the high state.

8-35. Four-Bit Bistable Latch. The four-bit bistable latch shown in Figure 8-5 consists of four independent D-type flip-flops. The flip-flops (FF1 and FF2) are controlled by the C1 clock input and the flip-flops (FF3 and FF4) are controlled by the C2 clock input. Information present at a data (D_C) input is transferred to the active-high and active-low outputs when the associated clock input is high; the outputs will follow the data as long as the clock remains high. When the clock goes low, the information that was present at the data input when the transition occurred is retained at the outputs until the clock returns high.

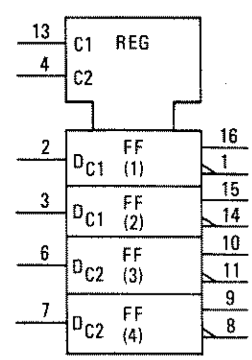


Figure 8-5. Four-Bit Bistable Latch

8-36. Dual J-K Master/Slave Flip-Flop. The dual J-K Master/Slave Flip-Flop shown in Figure 8-6 consists of two independent J-K flip-flops. Inputs to the master section is controlled by the gate (G)

Digital Integrated Circuits and Symbols (cont'd)

pulse. The gate pulse also controls the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

a. T1 — Isolate slave from master.

b. T2 — Enter information from J and K inputs to master.

c. T3 — Disable J and K inputs.

d. T4 — Transfer information from master to slave.

8-37. Flip-flop response is determined by the levels present at the J and K inputs at time T2. The four possible combinations are as follows:

a. When J and K are low, the outputs will not change state.

b. When J is high and K is low, the active-high output will go high, unless it is already high.

c. When J is low and K is high, the active-high output will go low, unless it is already low.

d. When J and K are both high, the flip-flop will toggle. That is, the active-high and active-low outputs will change states for each gate pulse.

8-38. The set (S) and reset (R) inputs override all other input conditions: when set (S) is low, the active-high output is forced high; when reset (R) is low, the active-high output is forced low. Although normally the active-low output is the complement of the active-high output, simultaneous low inputs to both S and R will force both outputs high on some J/K flip-flops. This forced high on both outputs will exist only for as long as both R and S are held low. The flip-flop will return to some indeterminate state when both R and S go high.

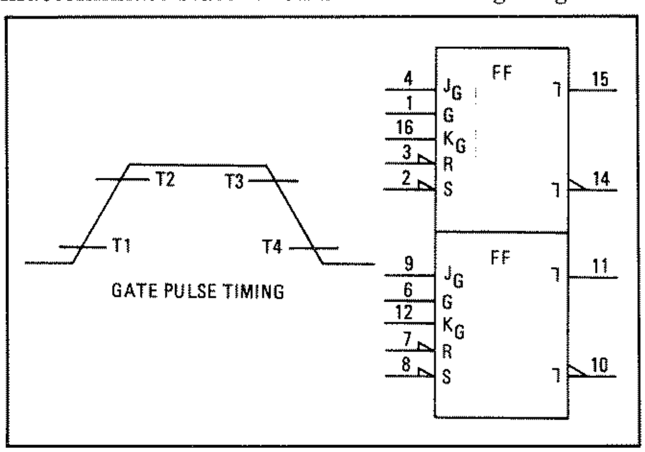


Figure 8-6. Dual J-K Master/Slave Flip-Flop and Gate Pulse Timing

8-39. **Dual J-K Edge-Triggered Flip-Flop.** The dual J-K edge-triggered flip-flop shown in Figure 8-7 is functionally identical to the master/slave flip-flop described previously except for gate pulse timing. The edge-triggered flip-flop response is determined by the levels present at the J and K inputs at the instant that a negative gate transition (high-to-low) occurs.

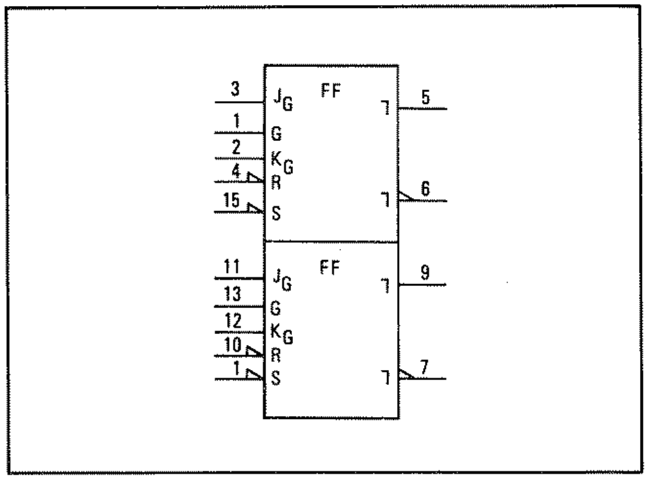
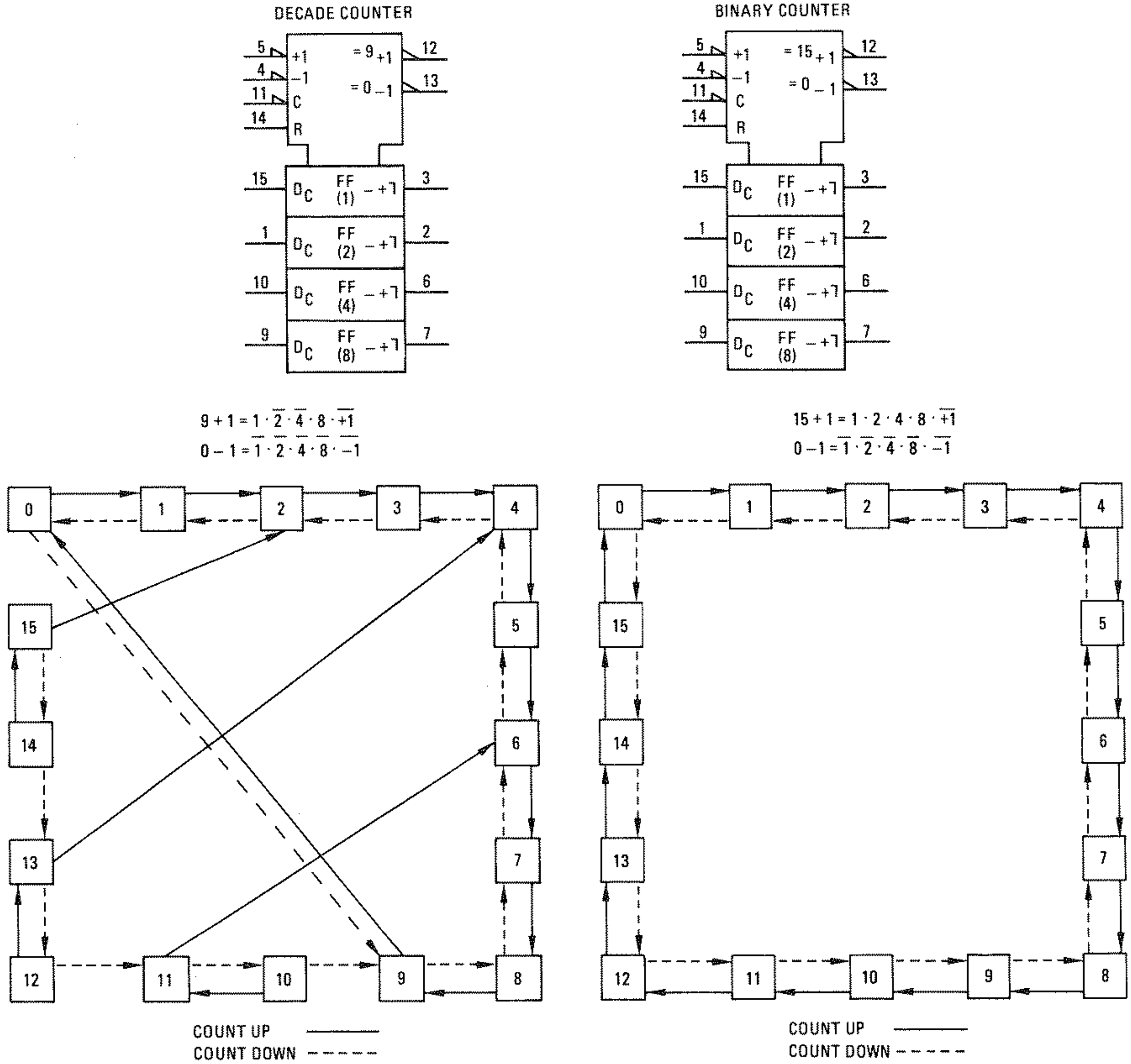


Figure 8-7. Dual J-K Edge-Triggered Flip-Flop

8-40. **Programmable Counters.** Programmable binary and decade counters used in the Power Meter are shown in Figure 8-8. The operating modes for both counters are identical. The only differences in operation are in the count sequences.

8-41. Operation of the counters is synchronous, with the outputs changing state after the high-to-low transistion of either the Count-Up Clock (+1) or the Count-Down Clock (−1). The direction of counting is determined by which clock input is pulsed while the other clock is high. Incorrect counting will occur if both clock inputs are low simultaneously. Both counters will respond to a clock pulse on either input by changing to the next appropriate state of the count sequence. The state diagram for the decade counter (Figure 8-8) shows both the regular sequence and the sequence if a code greater than nine is present in the counter.

8-42. Both counters have a parallel load (asynchronous) facility which permits the counters to be preset. Whenever the Parallel Load input (C) and Master Reset (R) are low, the information present on the D_C inputs will be loaded into the counters and appear at the outputs independently of the conditions of the clocks. When the Parallel Load (C) input goes high, this information is stored in the counters. When the counters are clocked they will change to the next



MODE SELECTION SUMMARY (Both Counters)

R	C	+1	−1	Mode
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H		H	Count Up
L	H	H		Count Down

H = HIGH Level X = Don't Care Condition
L = LOW Level = Clock Pulse

Figure 8-8. Programmable Counters

Digital Integrated Circuits and Symbols (cont'd)

appropriate state in the count sequence. The D_C inputs are inhibited when C is held high and have no effect on the counters.

8-43. The Terminal Count-Up (9_{+1} or 15_{+1}) or Terminal Count-Down (0_{-1}) outputs (carry and borrow respectively) allow multidecade counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and terminal count-down output to the count-down clock input.

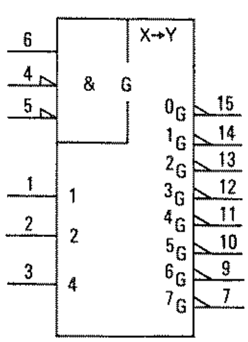
8-44. The Terminal Count-Up outputs of the decade and binary counters are low when their count-up clock inputs are low and the counters are in state nine and fifteen respectively. Similarly, the Terminal Count-Down outputs are low when their count-down clock inputs are low and both counters are in state zero. Thus, when the decade counter is in state nine and the binary counter is in state fifteen and both are counting up, or both are in state zero and counting down, a clock pulse will change the counter's state on the rising edge and simultaneously clock the following counter through the appropriate active low terminal count output. There are two gate delays per state when these counters are cascaded.

8-45. The asynchronous Master Reset (R) input, when high, overrides all other inputs and clears the counters. Master Reset (R) overrides Parallel Load (C) input so that when both are activated the counters will be reset.

8-46. Decoder. There are two types of decoders used in the Power Meter: a 3-line to 8-line and a 4-line to 16-line decoder. Operation of both decoders is identical except for the number of input and output lines. Therefore only the operation of the 3-line to 8-line decoder is shown in the truth table in Figure 8-9.

8-47. Data Selector (Multiplexer). There are two types of data selectors used in the Power Meter: an 8-input data selector and a 16-input data selector. The operation of both data selectors are identical except for the number of inputs. Therefore only the operation of the 8-input data selector is described and the symbol shown in Figure 8-10. One of the 8-input lines (0 through 7) is selected by the SEL output (G0 through 7). The strobe input (G8) must be low in order to enable the output lines. If the strobe input is high, the output lines are inhibited and present a high impedance. This circuit uses Three State logic so that the outputs may be connected into a "wired OR" configuration.

8-48. Display Driver. The display driver (Figure 8-11) accepts a 4-bit binary code and provides output drive to light the appropriate segments of a 7-segment numeric display. The decode format employed allows generation of numeric codes 0 through 9 as well as other codes shown in the truth table in Figure 8-11.

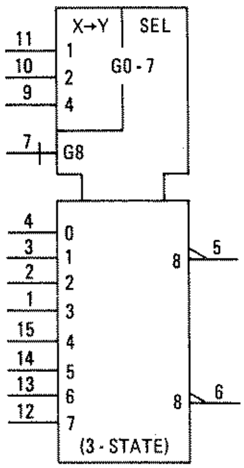


Truth Table

Inputs						Outputs							
Gate Enable			Select Code										
PIN 6	PIN 4	PIN 5	1	2	4	7	6	5	4	3	2	1	0
X	H	L	X	X	X	H	H	H	H	H	H	H	H
X	L	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H	L
H	L	L	L	L	H	H	H	H	H	H	H	L	H
H	L	L	L	H	L	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	L	H	H	H
H	L	L	H	L	L	H	H	H	L	H	H	H	H
H	L	L	H	L	H	H	H	L	H	H	H	H	H
H	L	L	H	H	L	H	L	H	H	H	H	H	H
H	L	L	H	H	H	L	H	H	H	H	H	H	H

H = High, L = Low, X = Don't care condition.

Figure 8-9. 3-Line to 8-Line Decoder



Truth Table

Inputs		Data Input Selected	Outputs	
X→Y Sel 1 2 4	Strobe (G_8)		PIN 5	PIN 6
X X X	H	X	Z	Z
L L L	L	0	0	0
L L H	L	1	1	1
L H L	L	2	2	2
L H H	L	3	3	3
H L L	L	4	4	4
H L H	L	5	5	5
H H L	L	6	6	6
H H H	L	7	7	7

H = High; L = Low; X = Don't care condition; Z - High impedance.

Figure 8-10. 8-Input Data Selector (Multiplexer)

8-49. Latches on the four data inputs are controlled by the gate (G2) input. When G2 is low, the states of the outputs are determined by the input data code. When G2 goes high, the last data code present at the input to the latches is stored and the output remains stable.

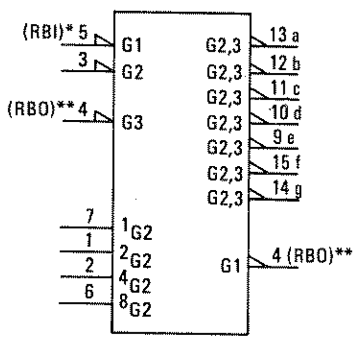
8-50. The display driver also has provision for automatic blanking and zero suppression via the ripple blanking input, RBI, (G1) and the ripple blanking output (RBO), respectively. The G1 line always serves as an input; the RBO line typically serves as an output but it can also be configured as an input (G3) by connecting it to an external drive source. When G3 is held low by an external source, it overrides all other inputs to the display driver and causes the display driver to provide blanking outputs to all segments of the associated display.

8-51. When the RBO line is not connected to an external drive source it serves as a blanking output which is controlled by G1. As shown on the truth table in Figure 8-11, the combination of a low G1 and a binary 0 code causes the display driver to set the RBO low and to provide blanking outputs to all segments of the associated display. For zero suppression, the RBI (G1) input associated with the most significant digit is grounded and the RBO output is connected to the G1 input of the next significant digit. Using this configuration a number such as 0010 would be displayed as 10.

8-52. Numeric Display. The numeric display consists of eight individual light emitting diodes (LED) which share a common anode input. Seven of the LEDs, designated a through g, are arranged to form a seven-segment display as shown in Figure 8-12. The eighth LED, designated dp, provides a left-hand decimal point display. Each segment is lighted individually by a low input to the cathode pin (a through g and dp) of the LEDs.

8-53. Read Only Memories (ROMs). The Read Only Memories (ROMs) used in the Power Meter fall into two separate logic families: TTL and MOS. As shown in Figure 8-13, the only significant differences between the two types of ROMs are the power requirements and the amount of program storage. The power requirements for each family are provided in Table 8-1. Storage capacity for the TTL ROM is 32 8-bit words (256 bits); for the MOS ROM, storage capacity increases to 256 16-bit words (4096 bits).

8-54. When the ROMs are initially programmed, each 8- or 16-bit word is stored at a predetermined address. During subsequent operation, selection of the desired word is accomplished by applying the appropriate address code to the X→Y inputs. (In the Power Meter, the gate (G) input on the TTL ROMs is not used; it is tied to ground to keep the ROMs continuously enabled.) The specific program associated with each ROM is listed adjacent to the Service Sheet schematic on which the ROM is shown.



Truth Table

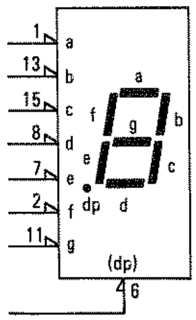
Binary Data Input	Inputs							Outputs								Display
	Control			Data												
	G1	G2	G3	8	4	2	1	a	b	c	d	e	f	g	RBO	
–	*	H	**	X	X	X	X	←STABLE→							H	STABLE
0	L	L	**	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	H	L	**	L	L	L	L	L	L	L	L	L	L	H	H	0
1	X	L	**	L	L	L	H	H	L	L	H	H	H	H	H	1
2	X	L	**	L	L	H	L	L	L	H	L	L	H	L	H	2
3	X	L	**	L	L	H	H	L	L	L	L	H	H	L	H	3
4	X	L	**	L	H	L	L	H	L	L	H	H	L	L	H	4
5	X	L	**	L	H	L	H	L	H	L	L	H	L	L	H	5
6	X	L	**	L	H	H	L	L	H	L	L	L	L	L	H	6
7	X	L	**	L	H	H	H	L	L	L	H	H	H	H	H	7
8	X	L	**	H	L	L	L	L	L	L	L	L	L	L	H	8
9	X	L	**	H	L	L	H	L	L	L	H	H	L	L	H	9
10	X	L	**	H	L	H	L	H	H	H	H	H	H	L	H	– (dash)
11	X	L	**	H	L	H	H	L	H	H	L	L	L	L	H	E
12	X	L	**	H	H	L	L	H	L	L	H	L	L	L	H	H
13	X	L	**	H	H	L	H	H	H	H	L	L	L	H	H	L
14	X	L	**	H	H	H	L	L	L	H	H	L	L	L	H	P
15	X	L	**	H	H	H	H	H	H	H	H	H	H	H	H	BLANK
X	X	X	L	X	X	X	X	H	H	H	H	H	H	H	**	BLANK

H= HIGH; L = LOW; X = DON'T CARE CONDITION

*The G1 input will blank the display only if a binary zero is stored in the latches.

**The RBO output (pin 4) when used as an input (G3) overrides all other input conditions.

Figure 8-11. LED Display Driver



Truth Table

Inputs								Display
a	b	c	d	e	f	g	dp	
L	L	L	L	L	L	H	X	0
H	L	L	H	H	H	H	X	1
L	L	H	L	L	H	L	X	2
L	L	L	L	H	H	L	X	3
H	L	L	H	H	L	L	X	4
L	H	L	L	H	L	L	X	5
L	H	L	L	L	L	L	X	6
L	L	L	H	H	H	H	X	7
L	L	L	L	L	L	L	X	8
L	L	L	H	H	L	L	X	9
H	H	H	H	H	H	H	X	BLANK
X	X	X	X	X	X	X	L	•

H = high; L = low; X = Don't care condition.

Figure 8-12. Numeric Display

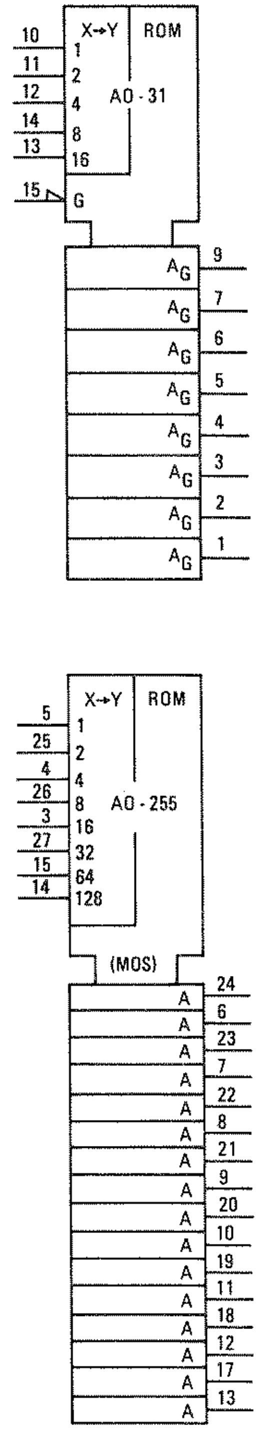


Figure 8-13. MOS and TTL ROMs

8-55. TROUBLESHOOTING

8-56. Since the Power Meter is a software controlled instrument, effective troubleshooting requires a thorough knowledge of both hardware operation and program execution. As an aid to this understanding, a general overview of Power Meter operation and troubleshooting rationale is provided in the Block Diagram Description associated with Service Sheets 1 through 5, detailed descriptions of the operating program are provided in Tables 8-3 and 8-6 and Figure 8-15, and circuit descriptions and troubleshooting data are provided as required on Service Sheets 6 through 15.

8-57. In addition to the information referenced above, this section also contains step-by-step verification procedures for a standard instrument, an HP-IB equipped instrument, and a BCD equipped instrument. Each of these procedures are designed to accomplish three major purposes. The first purpose is to exercise the stored program and the hardware circuits in a known sequence so that a fault condition can be readily isolated to a circuit group or to a segment of the stored program. The second purpose is to describe each check in sufficient detail to familiarize a maintenance technician with overall Power Meter operation. The third and most significant purpose is to indicate a logical troubleshooting entry point for program verification and signal tracing.

8-58. When the verification procedures are used as a basis for troubleshooting instruments equipped with either the HP-IB or BCD option, it is necessary that the standard instrument verification procedure be performed first to ascertain that the fault is not in the standard instrument circuits. After the standard instrument circuits are known to be operating properly, a fault can be readily isolated to a remote option circuit group, or to that segment of the operating program associated with remote operation.

8-59. Standard Instrument Checkout

8-60. A step-by-step procedure for verifying the operation of a standard instrument is provided in Table 8-3. Each step of the procedure directs that a specific function be verified and summarizes the program execution and/or circuit operation associated with the function. Each summary, in turn, is based on normal indications previously obtained. Thus, if the steps are performed in the order listed, an abnormal indication is directly related to a small segment of the operating program or to a specific circuit group. The information contained on the Service Sheets and in the Operating Program Flow Chart (Figure 8-15) can then be used to further isolate the problem. Typical examples of using the checkout procedure as a basis for troubleshooting are listed below.

8-61. Example 1: Abnormal Indication is Observed for Step 1. For this example, it is assumed that the power supplies are operating normally since troubleshooting of these circuits is straightforward (refer to Service Sheet 15). The first step in isolating any other type of fault is to determine whether the fault is in the ROM which contains the operating program, or whether it is one of the major circuit groups shown on Service Sheet 1. To isolate the fault, proceed as follows:

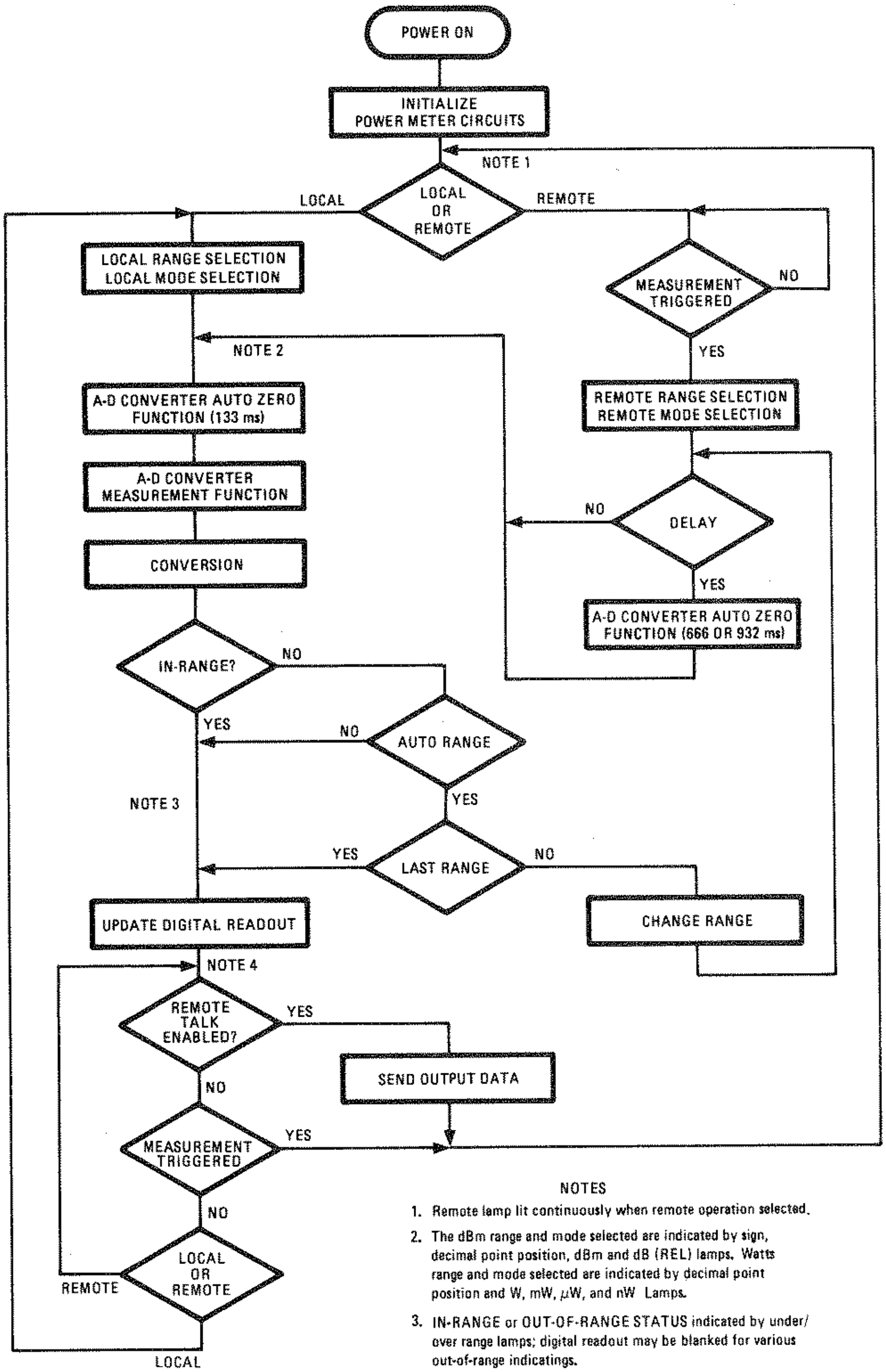
a. Look at the front-panel display while referrring to Figure 8-14 and try to determine what portion of the operating program that the fault is associated with. Note that the range and mode indications are generated at the start of the program cycle, the in-range/out-of-range status indications are generated next, then the digital readout is updated at the end of the program cycle. (When autoranging is enabled and an out-of-range conversion is detected, additional measurements are taken until an in-range conversion is detected, or until an out-of-range conversion is detected on the last range. Thus, the digital readout is not updated until after the last conversion of the program cycle.)

b. If the mode and range indications are abnormal, the fault occurs early in the program cycle and will affect circuit operation for the remainder of the cycle. Thus, the abnormal indication should be remedied before attempting any further analysis of Power Meter operation. To isolate the fault, proceed as follows:

1) Connect the logic analyzer (HP 1600A or equivalent) to the Power Meter as follows:

NOTE

Unless otherwise indicated, the logic analyzer is always connected



NOTES

1. Remote lamp lit continuously when remote operation selected.
2. The dBm range and mode selected are indicated by sign, decimal point position, dBm and dB (REL) lamps. Watts range and mode selected are indicated by decimal point position and W, mW, μW, and nW Lamps.
3. IN-RANGE or OUT-OF-RANGE STATUS indicated by under/over range lamps; digital readout may be blanked for various out-of-range indicatings.
4. Input power level measured is clocked into digital readout. (If digital was blanked previously, it will remain blanked.)

Figure 8-14. Power Meter Operating Cycle

TROUBLESHOOTING

Standard Instrument Checkout (cont'd)

Note cont'd)
as specified below for verifying program execution.

Logic Analyzer Input	Connect to:
DATA INPUTS BIT 0	A5TP1
DATA INPUTS BIT 1	A5TP2
DATA INPUTS BIT 2	A5TP3
DATA INPUTS BIT 3	A5TP4
DATA INPUTS BIT 4	A5TP5
DATA INPUTS BIT 5	A5TP6
DATA INPUTS BIT 6	A5TP7
DATA INPUTS BIT 7	A5TP8
DATA INPUTS GND	A5TP11
CLOCK INPUT	A5TP10

2) Set the logic analyzer controls as indicated below.

NOTE

Unless otherwise indicated, the logic analyzer controls are always set as specified below for verifying program execution.

DISPLAY	CLOCK: ⎍ (rising edge)	THRESHOLD: TTL
LOGIC: POS	DISPLAY TIME: as desired.	
MARK: OFF BYTE: 3 BIT	COLUMN BLANKING: to display Bits 0 through 7.	

3) Observe the logic analyzer NO CLOCK indicators to verify that a Ø1 clock input is applied to the Controller. If either indicator is lit, refer to Service Sheet 9 for information covering checkout and troubleshooting of the Clock Generator Circuits. (Service Sheet 1 indicates that Program Clocks are applied to the Controller from the Counter and Clock Generator Circuits and that a detailed block diagram of these circuits is provided on Service Sheet 3. Service Sheet 3, in turn, indicates that a schematic of the Clock Generator Circuits is provided on Service Sheet 9.)

4) Move the logic analyzer CLOCK probe from A5TP10 to A4TP2 and observe the NO CLOCK indicators to verify that a Ø2 clock is applied to the Controller. If either indicator is lit, refer to Service Sheet 9 for information covering checkout and troubleshooting of the Clock Generator Circuits.

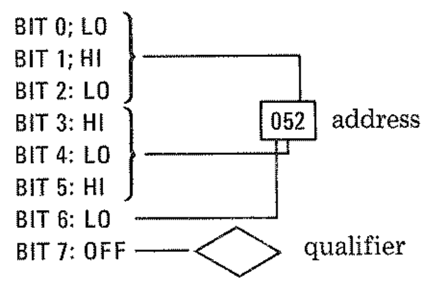
5) Return logic analyzer CLOCK probe to A5TP10 and set remaining logic analyzer controls as indicated below. These controls select the triggering of the logic analyzer and are adjusted as required to verify Power Meter program execution.

DELAY SET: 00000

SAMPLE MODE: REPET

TRIGGER MODE: START DISPLAY

TRIGGER WORD: (switch settings specified select address 052_8; qualifier =1 or 0)



6) If the operating program is cycling normally, the NO TRIG indicator will be off and the logic analyzer will provide a 16-line display starting at address 052_8. The first two lines of the display should indicate that the YR3 qualifier associated with address 052_8 is a logic 1, and that the YR2 qualifier associated with address 055_8 is a logic 0. An explanation of how this status indication is derived can be found in Table 8-3 and 8-6 and in Figure 8-15. Table 8-6 indicates that the range counter was counted down to range 7 at address 034_8 of the Power Up subroutine, and to range 5 at address 035_8. Figure 8-15 shows the qualifiers associated with these addresses and how the qualifiers are processed to control address branching and instruction generation. Table 8-2

TROUBLESHOOTING

Standard Instrument Checkout (cont'd)

describes the purpose and function of each qualifier and instruction. Thus, from the information contained in the tables and on the figure, it can be determined that after the Range Counter is counted down from range 5, the Mode Register is loaded, then the program branches to the Local/Remote Subroutine. Since Local operation is automatically selected when power is turned on, the next branch is to address 052_8 of the Local Initialize subroutine. The Range Counter was counted down properly, the range qualifiers should be set to the following logic states: YR3 = H, YR2 = L, YR1 = H.

7) If a display is present on the logic analyzer, it verifies that the operating program is cycling normally and branching to address 052_8 to initiate each cycle. With this fact established, its just a matter of signal tracing to find out exactly where the problem is. Refer to Service Sheet 3 and check the outputs of the Mode Register and Range Counter. If they're normal, trace out the signal lines to the Display Assembly to isolate the problem to a circuit. If the outputs of the Mode Register are abnormal, use the logic analyzer and an oscilloscope to isolate the problem to the ROM containing the program, the Instruction Register, the Front-Panel Switches, the Buffers, or the Mode Register and Gates (Service Sheet 3). If the outputs of the Range Counter are abnormal, turn power on and off while using the logic analyzer to check program execution and Range Counter operation during the Power Up Subroutine.

8) If no display is present on the logic analyzer, turn power on and off as required to verify program execution starting at address 000_8 of the Power Up Subroutine.

c. If the mode and range indications are normal, check the output of the Amplifier, Demodulator, and Filter circuits at DC test point A3TP4. If it is abnormal, refer to Service Sheet 2 and check the YLOG and range select inputs to the circuit. If the YLOG and Range Select inputs are normal, use standard signal tracing techniques to isolate the problem. If they're abnormal, refer back to step b.

d. If the output of the Amplifier, Demodulator, and Filter circuit is normal, sync the logic analyzer on address 071_8 and check whether the A-D Converter-qualifier goes to logic 0 at 633 ± 160 clock pulses later. If no display can be obtained on the logic analyzer, turn power on and off and verify program execution starting at the Local Initialize Subroutine. If an erroneous display is observed, use the logic analyzer and an oscilloscope to isolate the problem to the ROM containing the program, the Instruction Register, the A-D Control Register and Gates, the A-D Converter, or the Counters. (The TRIGGER OUTPUT of the logic analyzer can be used to sync the oscilloscope at any address.)

e. If the conversion described in step d is proper, check that an LCOR instruction is generated at address 072_8 and that an LTC instruction is generated to load the Display Register at address 177_8. If both of these instructions are generated properly, use standard signal tracing techniques to isolate the problem to the Under/Over-Range Decoder, the Main Counter, or the Display Assembly.

8-62. Example 2: Abnormal Indication is Observed for Step 8. This example was chosen because it illustrates Power Meter autoranging during a program cycle. When the RANGE HOLD switch is released for step 8, an LCRD instruction should be generated during the Under Range Subroutine to count the Range Counter down to range 4, then an LSOR instruction should be generated to blank the front-panel digital readout (refer to Service Sheet 3, Linear Under-Range Conversion). The range 4 output of the Range Counter, in turn, should cause the True-Range Decoder to change the digital readout decimal point position, and should also select higher gain operation of the Amplifier, Demodulator, and Filter circuit. Thus, the input voltage to the A-D Converter at DC test point A3TP4 should rise to 0.980 Vdc by the time that the subsequent Auto Zero Subroutine is completed. Program execution and circuit operation from this point on was verified in steps 1 through 7. The key step in isolating an abnormal indication then, is to check that the output of the Amplifier, Demodulator, and Filter circuit rises to the specified value by the end of the Auto Zero Subroutinte which follows the Under Range Subroutine. The main reason for making this check

TROUBLESHOOTING

Standard Instrument Checkout (cont'd)

first is that if the output of the Amplifier, Demodulator, and Filter circuit does not rise to an in-range level by the end of the Auto Zero Subroutine, a range 4 under-range conversion will be detected. A second Under Range Subroutine will then be executed to count the Range Counter down to range 3 and the range 3 output of the Range Counter will change the output of the True-Range Decoder and the gain of the Amplifier, Demodulator, and Filter circuit a second time. Depending on the type of failure present, either an under-range conversion or an over-range conversion could be detected for range 3. Thus, for this type of problem, neither the final range that the Power Meter will settle on nor the resultant front-panel indication can be predicted.

8-63. To isolate a step 8 abnormal indication proceed as follows:

a. Check the output of the Range Counter to determine what range the Power Meter settles on. If the Power Meter settles on range 4, sync the logic analyzer on address 052_8 as described in Example 1 to determine whether the operating program is cycling. If the program is not cycling, turn off power and reestablish the conditions of step 7. Then turn power back on, release the RANGE HOLD switch, and verify program execution starting at the Under Range Subroutine.

b. If the Power Meter has settled on range 4 and the operating program is cycling normally, refer to Service Sheets 2 and 3 and isolate the problem to the True-Range Decoder, the Amplifier, Demodulator, and Filter circuit, the Over/Under-Range Decoder, or the Display Assembly.

Table 8-2. Program Mnemonic Descriptions (1 of 5)

Mnemonic	Service Sheet	Subroutine	Description
PROGRAM QUALIFIER INPUTS			
NAUTO	3, 4, 6, 10, 11	Remote Initialize Under Range Over Range	When low, enables Power Meter to automatically select most accurate measurement range. When high, causes Power Meter to hold last range selected, either locally or remotely.
YH1 YH2 YH4 YH8	2, 3, 4, 6, 9, 10, 12	Linear, Positive — Conversion (YH1, YH2 only) Linear, Negative — Conversion (YH1, YH2 only) Log Conversion (all)	Main counter hundreds output (BCD).
YK1	2, 3, 4, 6, 9, 10, 12	Remote Initialize Measurement should be Linear, Positive-Conversion Linear, Negative-Conversion	Least significant digit of main counter thousands output (BCD).
YK8	3, 9 10	Power Up Auto Zero Delay	Most significant digit of main counter thousands output (BCD).

Table 8-2. Program Mnemonic Descriptions (2 of 5)

Mnemonic	Service Sheet	Subroutine	Description
YM1 YM2	3, 10	Remote Initialize Measurement Relative dB Over/Under Range Continue	Two-bit code which selects measurement mode as follows: YM2 YM1 Mode 1 1 dBm 0 1 dB Rel 1 0 Watts 0 0 dB Ref (dB [REF] switch pressed)
YPLS	2, 3, 8, 10	Measurement Linear, Positive-Conversion Linear, Negative-Conversion Log Conversion	A-D converter output. During measurement subroutine, indicates whether A-D input is above or below A-D threshold (YPLS high or low, respectively). During conversion subroutines, changes state when A-D converter discharges through threshold.
YR1 YR2 YR3	2, 3, 4 7, 10 12	Power Up Remote Initialize Local Initialize Under Range (YR2, YR3 only) Over Range	Three-bit code which selects measurement range as follows: YR3 YR2 YR1 Range 0 0 0 0 (Remote only) 0 0 1 1 0 1 0 2 0 1 1 3 1 0 0 4 1 0 1 5 1 1 0 6 (Invalid; Power Meter 1 1 1 7 automatically selects range 5 even if NAUTO high)
YRMT (DACQ)	3, 4, 10, 11	Display and Remote Talk	Remote input. When HP-IB option installed, serves as I/O transfer control signal (refer to description and timing diagram provided under Principles of Operation).
YRMT (FAST)	3, 4, 10, 11	Remote Initialize Delay	Remote input. When HP-IB option installed, functions in conjunction with YRMT (HOLD) to select measurement rate as indicated below. When BCD interface option installed, functions in conjunction with YRMT (DACQ) to select measurement rate as indicated below. FAST HOLD/DACQ Measurement Rate X low (level) Disabled (hold) high high (pulse) trigger (with settling time) low high (pulse) trigger (immediate) high high (level) free run (at maximum rate) low high (level) free run (with settling time)

Table 8-2. Program Mnemonic Descriptions (3 of 5)

Mnemonic	Service Sheet	Subroutine	Description
YRMT (HOLD)	3, 4 10, 11	Local/Remote Branch Display and Remote Talk	Remote input. When HP-IB option installed, functions in conjunction with YRMT (FAST) to select measurement rate as indicated above.
YRMT (MORE DATA)	3, 4 10, 11	Display and Remote Talk	Remote talk I/O transfer control signal associated with HP-IB option. Set low at start of talk cycle to indicate that last word of data message not sent to external controller; reset high at end of talk cycle.
YRMT (REMOTE)	3, 4 10, 11	Local/Remote Branch Delay Display and Remote Talk	Remote input. When low, selects local operation of Power Meter; when high, selects remote operation of Power Meter
YRMT (RFDQ)	3, 4, 10,11	Display and Remote Talk	Remote talk I/O transfer control signal associated with HP-IB option (refer to description and timing diagram provided under Principles of Operation).
YRMT (TALK)	3, 4, 10,11	Display and Remote Talk	Remote talk enable input associated with HP-IB option; set low by external controller to request output data from Power Meter.
NZRO	3,9,10	Relative dB	Relative counter status output. Goes low to indicate that contents of relative counter are equal to 0.
		INSTRUCTIONS	
LAZ	3, 10	Power Up Local/Remote Branch Remote Initialize Auto Zero Delay Display and Remote Talk	Sets A-D auto-zero register thereby enabling A-D converter auto-zero loop.
LCKM	3, 10	Power Up Remote Initialize Local Initialize	Loads mode select bits into mode register.

Table 8-2. Program Mnemonic Descriptions (4 of 5)

Mnemonic	Service Sheet	Subroutine	Description
LCLR	3, 9, 10	Power Up Remote Initialize Auto Zero Measurement Over/Under Range Continue Delay	Sets sign register (sign +) and clears main counter.
LCNT	3, 9, 10	Power Up Remote Initialize Auto Zero Measurement Linear, Positive-Conversion Linear, Negative-Conversion Log Conversion Relative dB Delay	Enables one up/down clock pulse to main counter.
LCOR	3, 9, 10	Linear, Positive-Conversion Linear, Negative-Conversion Log Conversion Relative dB	Clears over-range and under-range flip-flops and loads contents of reference register into relative counter.
LCRD	10	Power Up Remote Initialize Local Initialize Under Range	Counts range counter down one range.
LCRU	10	Power Up Over Range	Counts range counter up one range.
LINP	3, 10	Measurement	Sets 1/2 of A-D conversion control register, thereby enabling A-D converter to charge to input voltage level.
LLRA	3, 9, 10	Remote Initialize	Loads remote range select inputs into range register.
LLRE	3, 9, 10	Power Up Relative dB Over/Under Range Continue	Loads contents of main counter into reference register.
LPSC	3, 9, 10	Measurement	Loads true-range counter and sign preset inputs into main counter and sign register, respectively.

Table 8-2. Program Mnemonic Descriptions (5 of 5)

Mnemonic	Service Sheet	Subroutine	Description
LREL	3, 9, 10	Relative dB	Serves as down clock to relative counter, and as steering input to main counter up/down count control logic.
LRMP	3, 10	Measurement Linear, Positive-Conversion Linear, Negative-Conversion Log Conversion	Sets 1/2 of A-D conversion control register. Output of register is then gated with various status signals to enable A-D converter conversion ramp as follows: Linear Positive Conversion Ramp — enabled when Watts mode selected and A-D input voltage exceeds threshold. Linear Negative-Conversion Ramp — enabled when Watts mode selected and A-D input voltage is below threshold. Log Conversion Ramp and Log Reference — enabled when dBm, or dB Rel mode selected.
LSDAV	3, 10, 11 13	Display and Remote Talk	Remote talk I/O transfer control signal (refer to description and timing diagram provided under Principles of Operation.
LSOR	3, 10	Power Up Measurement Under Range Over Range	Sets overrange flip-flop to provide blanking output to display, and, if under range flip-flop is reset, to light OVER RANGE lamp.
LSUR	3, 10	Measurement Under Range	Sets underrange flip-flop to light UNDER RANGE lamp.
LTC	2, 3, 4, 6, 11, 13	Power Up Display and Remote Talk	Clocks display sign flip-flop and loads sign and contents of main counter into display registers.

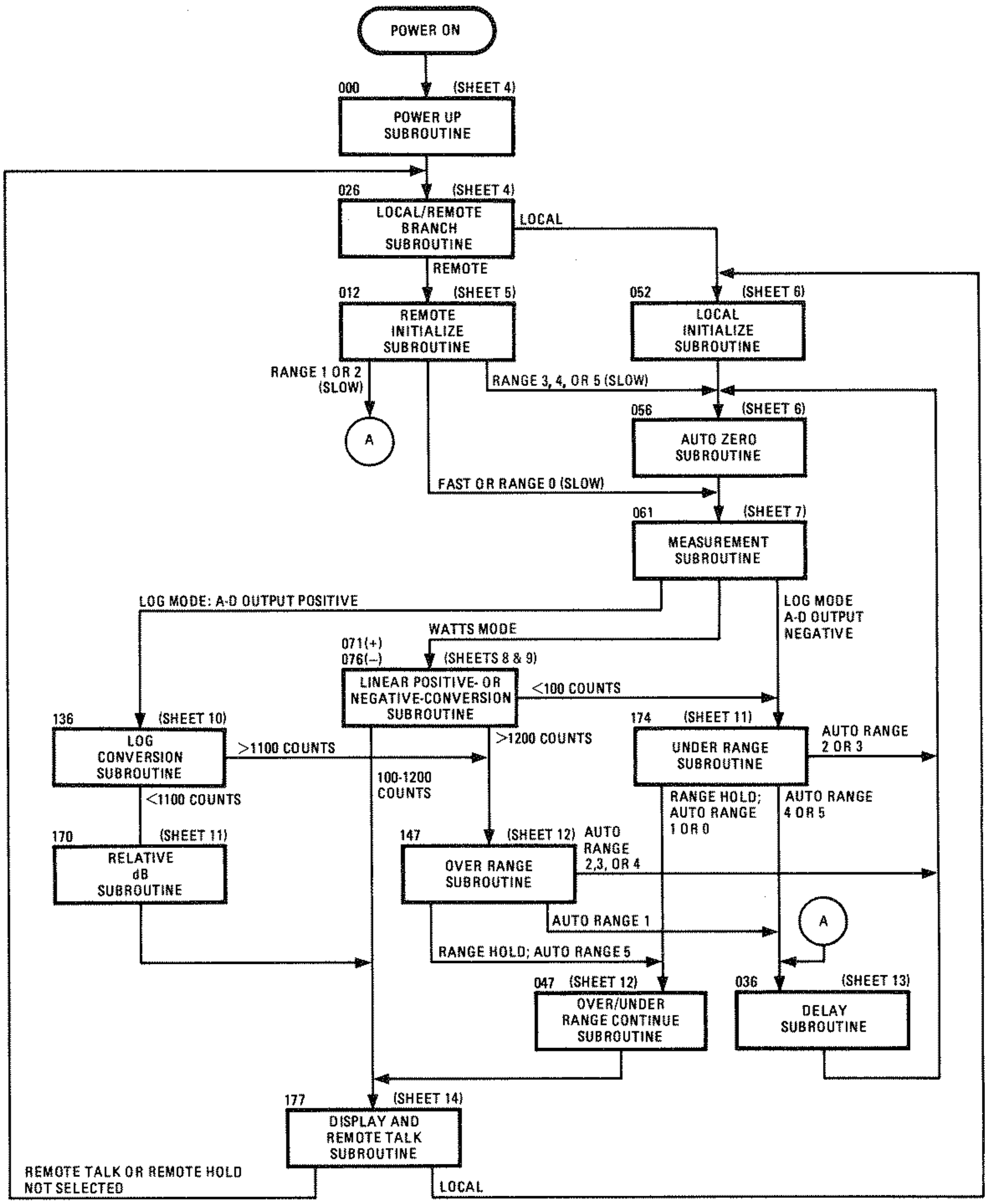
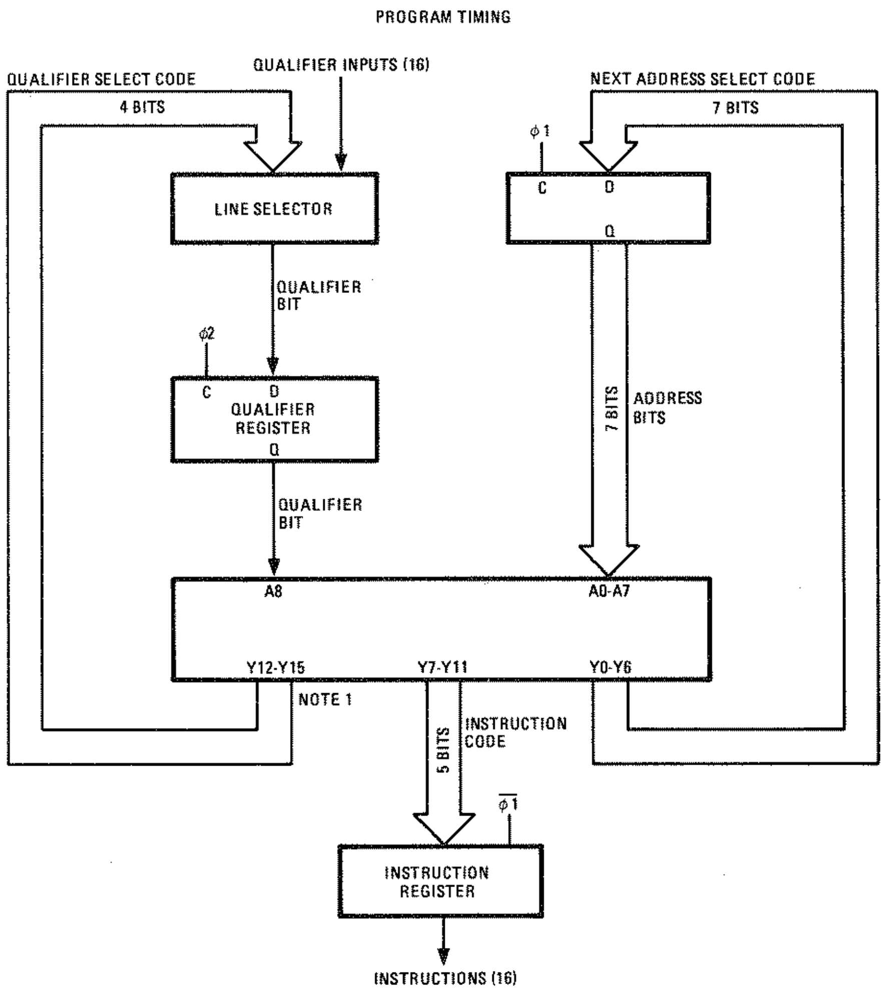
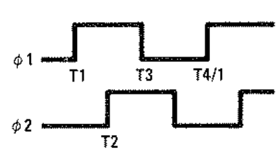


Figure 8-15. Operating Program Flow Chart (1 of 14)

2





NOTE
1. FOR ROM OUTPUTS, LOGICAL 1 = 0V

T1a. NEXT ADDRESS SELECT BITS CLOCKED INTO STATE REGISTER AND APPLIED TO ROM. ROM OUTPUTS ADDRESSED WORD'

b. QUALIFIER OUTPUT OF LINE SELECTOR DETERMINED BY QUALIFIER SELECT CODE.

T2. QUALIFIER CLOCKED INTO QUALIFIER REGISTER AND APPLIED TO ROM AS ADDRESS MODIFIER. ROM OUTPUTS ADDRESSED WORD.

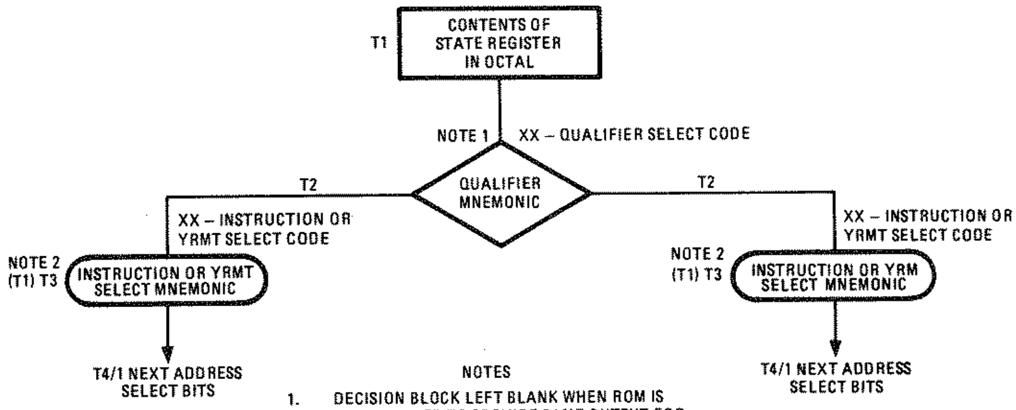
T3. INSTRUCTION REGISTER ENABLED; INSTRUCTION CODE SELECTS OUTPUT.

T4/1. INSTRUCTION REGISTER DISABLED; NEXT CYCLE INITIATED AS LISTED FOR 1a AND 1b.

Figure 8-15. Operating Program Flow Chart (2 of 14)

Service Model 436A

FLOW CHART ARRANGEMENT



NOTES

1. DECISION BLOCK LEFT BLANK WHEN ROM IS PROGRAMMED TO PROVIDE SAME OUTPUT FOR EITHER 1 OR 0 QUALIFIER STATE.
2. WHEN A YRMT SELECT CODE IS GENERATED AT T1, INSTRUCTION REGISTER IS DISABLED AND STATE OF YRMT LINE AT T2 DETERMINES NEXT ADDRESS AT T4/1.

QUALIFIER SELECT CODES

Y_{15}	Y_{14}	Y_{13}	Y_{12}		
0	0	0	0	+5V	(0_8)
0	0	0	1	YH1	(1_8)
0	0	1	0	YH2	(2_8)
0	0	1	1	YH4	(3_8)
0	1	0	0	YH8	(4_8)
0	1	0	1	YK1	(5_8)
0	1	1	0	YK8	(6_8)
0	1	1	1	YPLS	(7_8)
1	0	0	0	NRZO	(10_8)
1	0	0	1	YR1	(11_8)
1	0	1	0	YR2	(12_8)
1	0	1	1	YR3	(13_8)
1	1	0	0	NAUTO	(14_8)
1	1	0	1	YM1	(15_8)
1	1	1	0	YM2	(16_8)
1	1	1	1	YRMT	(17_8)*

*YRMT IS A MULTIPLEXED QUALIFIER LINE. INSTRUCTION CODE SELECTS OUTPUT OF MULTIPLEXER.

INSTRUCTION CODES

Y_{11}	Y_{10}	Y_9	Y_8	Y_7		
0	0	0	0	0	LSDAV	(0_8)
0	0	0	0	1	LAZ	(1_8)
0	0	0	1	0	LINP	(2_8)
0	0	0	1	1	LRMP	(3_8)
0	0	1	0	0	LREL	(4_8)
0	0	1	0	1	LSOR	(5_8)
0	0	1	1	0	LSUR	(6_8)
0	0	1	1	1	LCRU	(10_8)
0	1	0	0	0	LCOR	(7_8)
0	1	0	0	1	LCRD	(11_8)
0	1	0	1	0	LCRA	(12_8)
0	1	0	1	1	LCKM	(13_8)
0	1	1	0	0	LLRE	(14_8)
0	1	1	0	1	LCLR	(15_8)
0	1	1	1	0	LPSC	(16_8)
0	1	1	1	1	LTC	(17_8)
1	0	0	0	0	SAME AS ABOVE	
		THRU			EXCEPT LCNT ALSO	
1	0	1	1	1	GENERATED TO CLOCK MAIN COUNTER	
					*YRMT SELECT CODES	
1	1	0	0	0	DISABLE	
1	1	0	0	1	SELECT LDAV (31_8) AS YRMT QUALIFIER	
1	1	0	1	0	SELECT LTALK (32_8) " "	
1	1	0	1	1	SELECT HMDT (33_8) " "	
1	1	1	0	0	SELECT LRFDQ (34_8) " "	
1	1	1	0	1	SELECT LFAST (35_8) " "	
1	1	1	1	0	SELECT LHOLD (36_8) " "	
1	1	1	1	1	SELECT LREMOTE (37_8) " "	

Figure 8-15. Operating Program Flow Chart (3 of 14)

4a

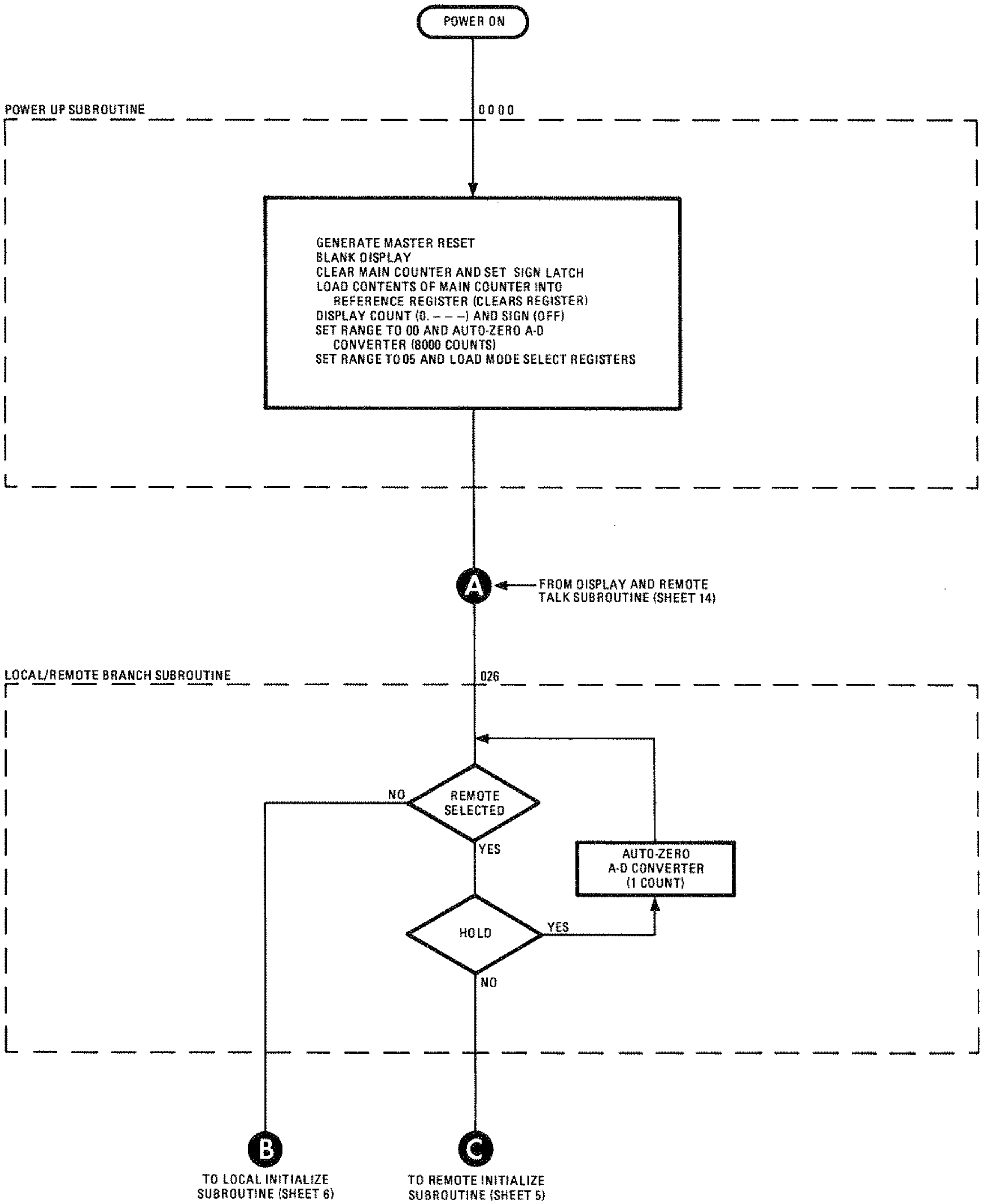
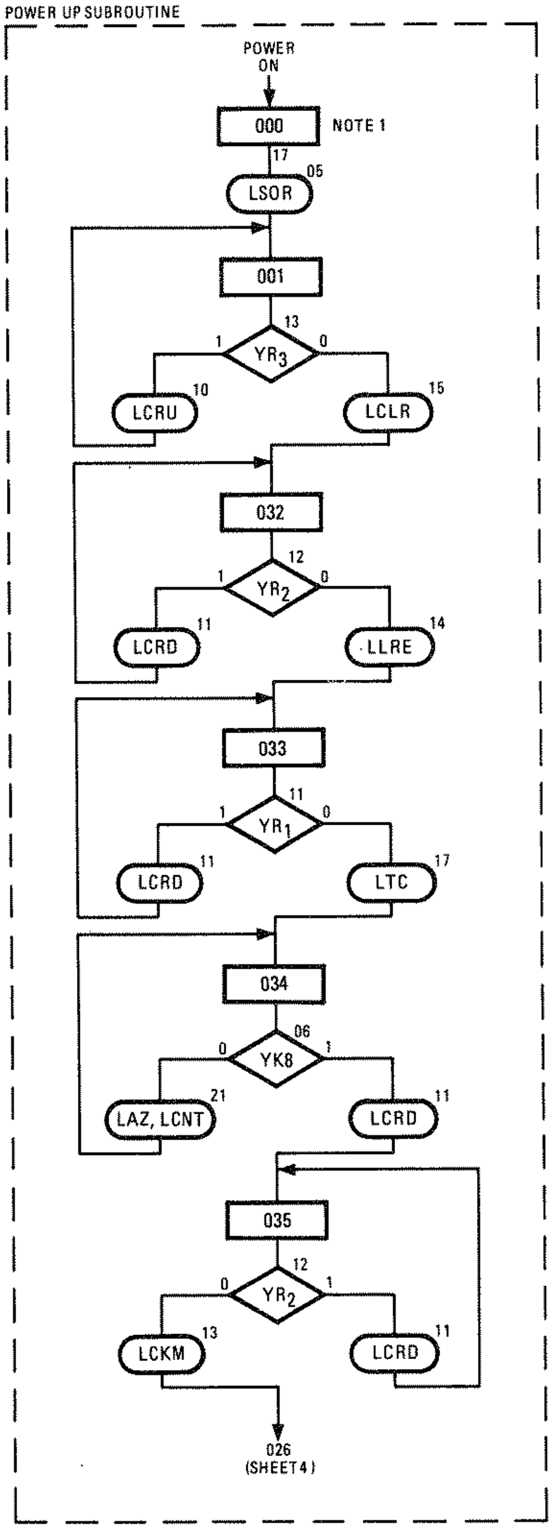
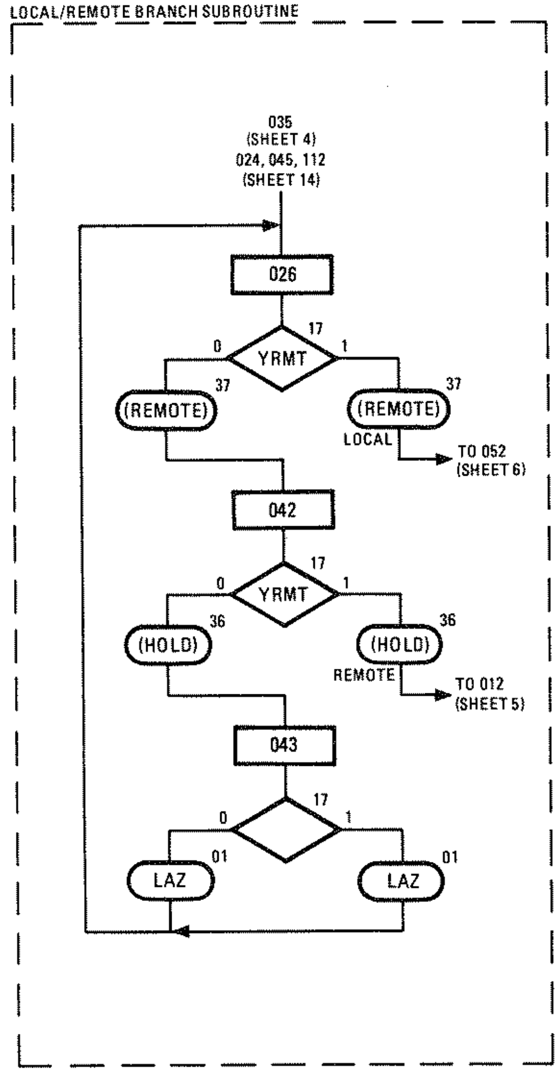


Figure 8-15. Operating Program Flow Chart (4A of 14)





NOTE

1. ADDRESS 0000 WILL BE HELD UNTIL END OF LPU PULSE (SEE SERVICE SHEET 10).

Figure 8-15. Operating Program Flow Chart (4B of 14)

5a

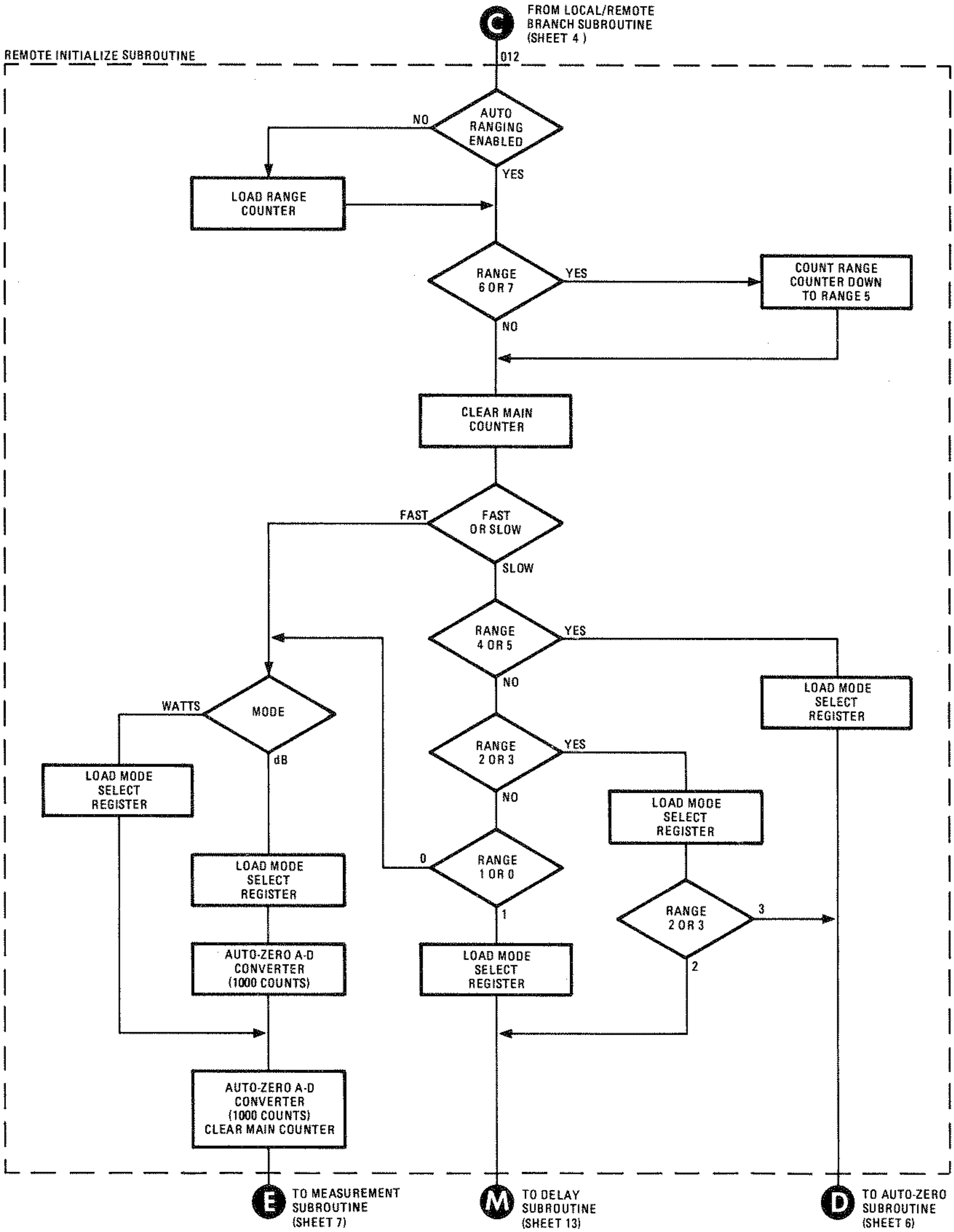


Figure 8-15. Operating Program Flow Chart (5A of 14)

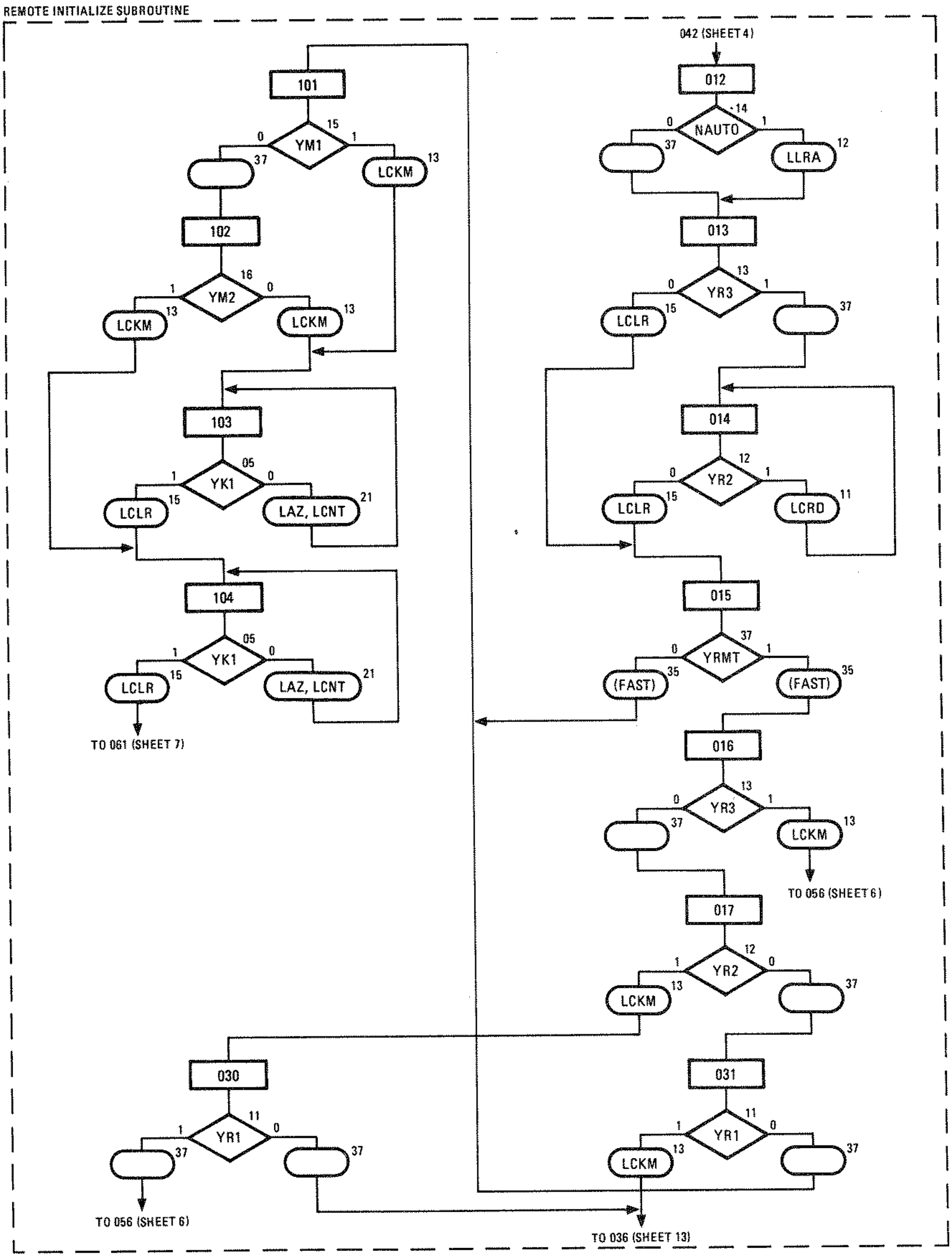


Figure 8-15. Operating Program Flow Chart (5B of 14)

6a

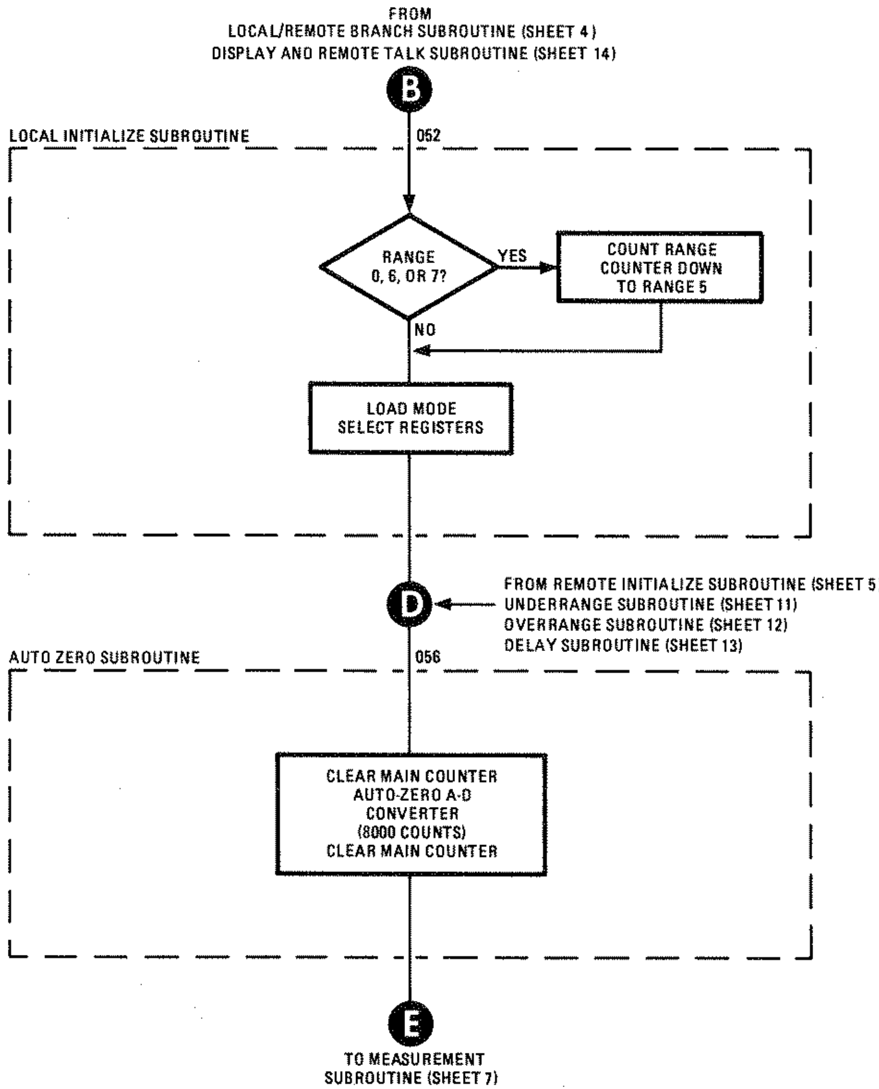


Figure 8-15. Operating Program Flow Chart (6A of 14)

6b

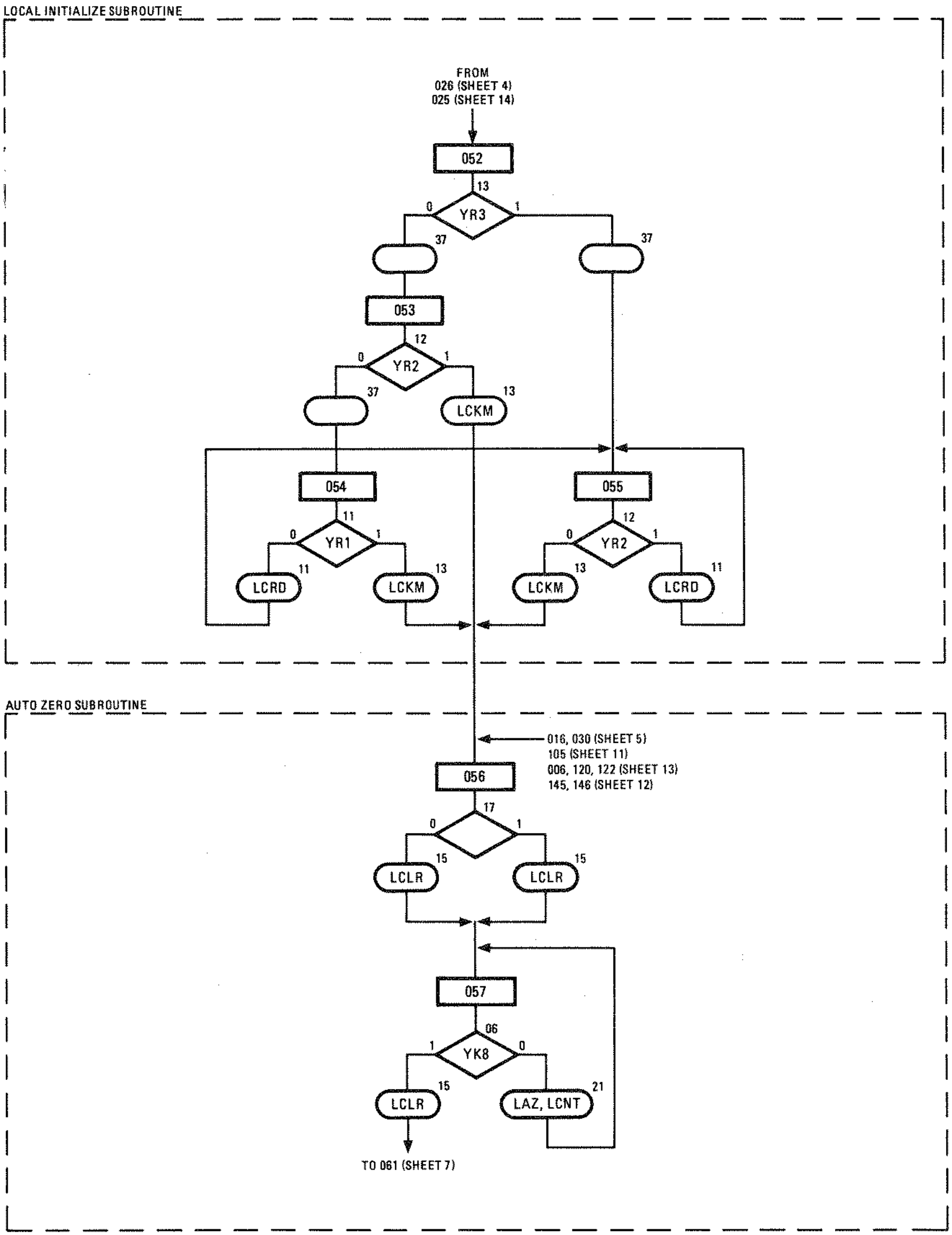


Figure 8-15. Operating Program Flow Chart (6B of 14)

7a

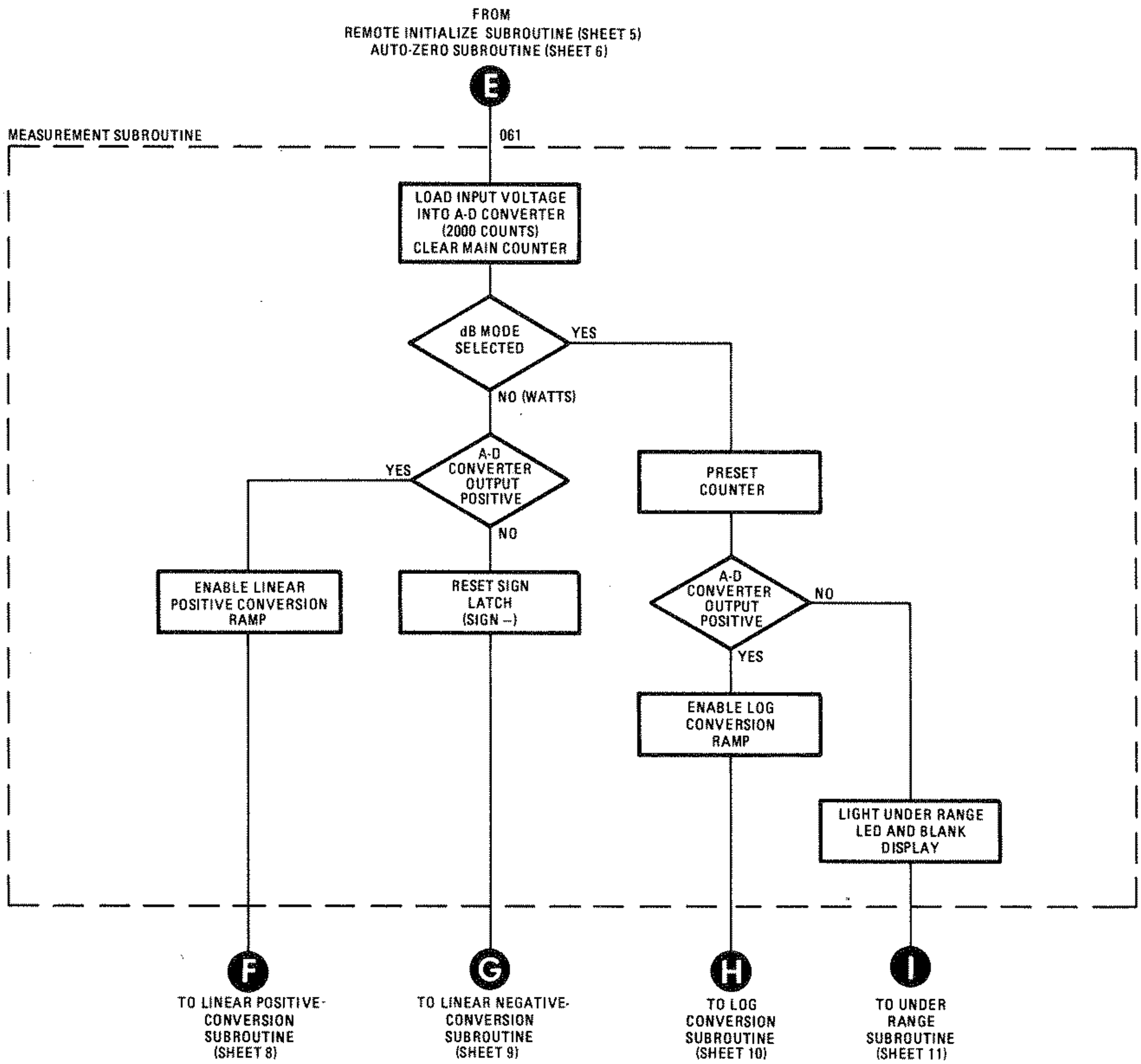


Figure 8-15. Operating Program Flow Chart (7A of 14)

7b

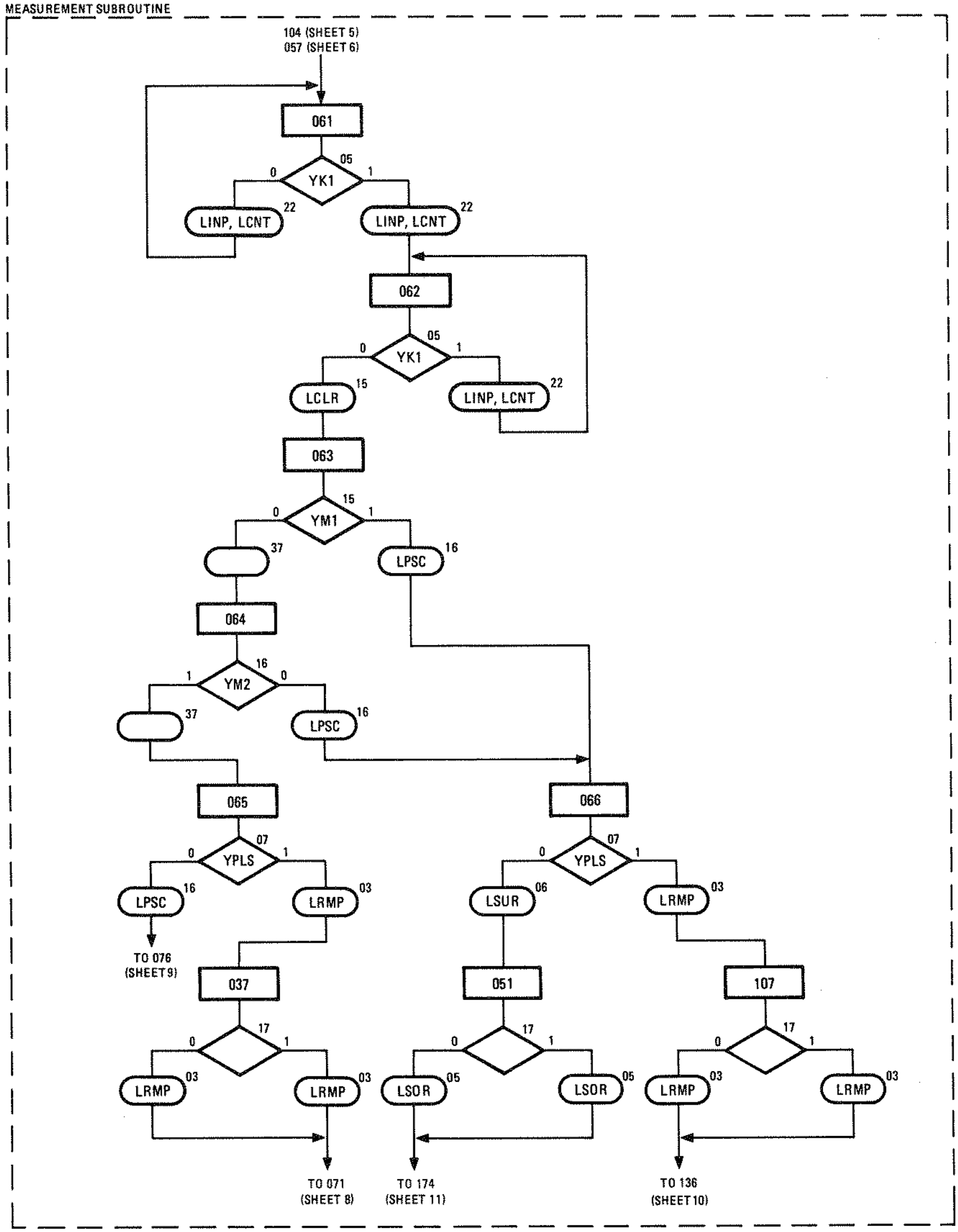


Figure 8-15. Operating Program Flow Chart (7B of 14)

8a

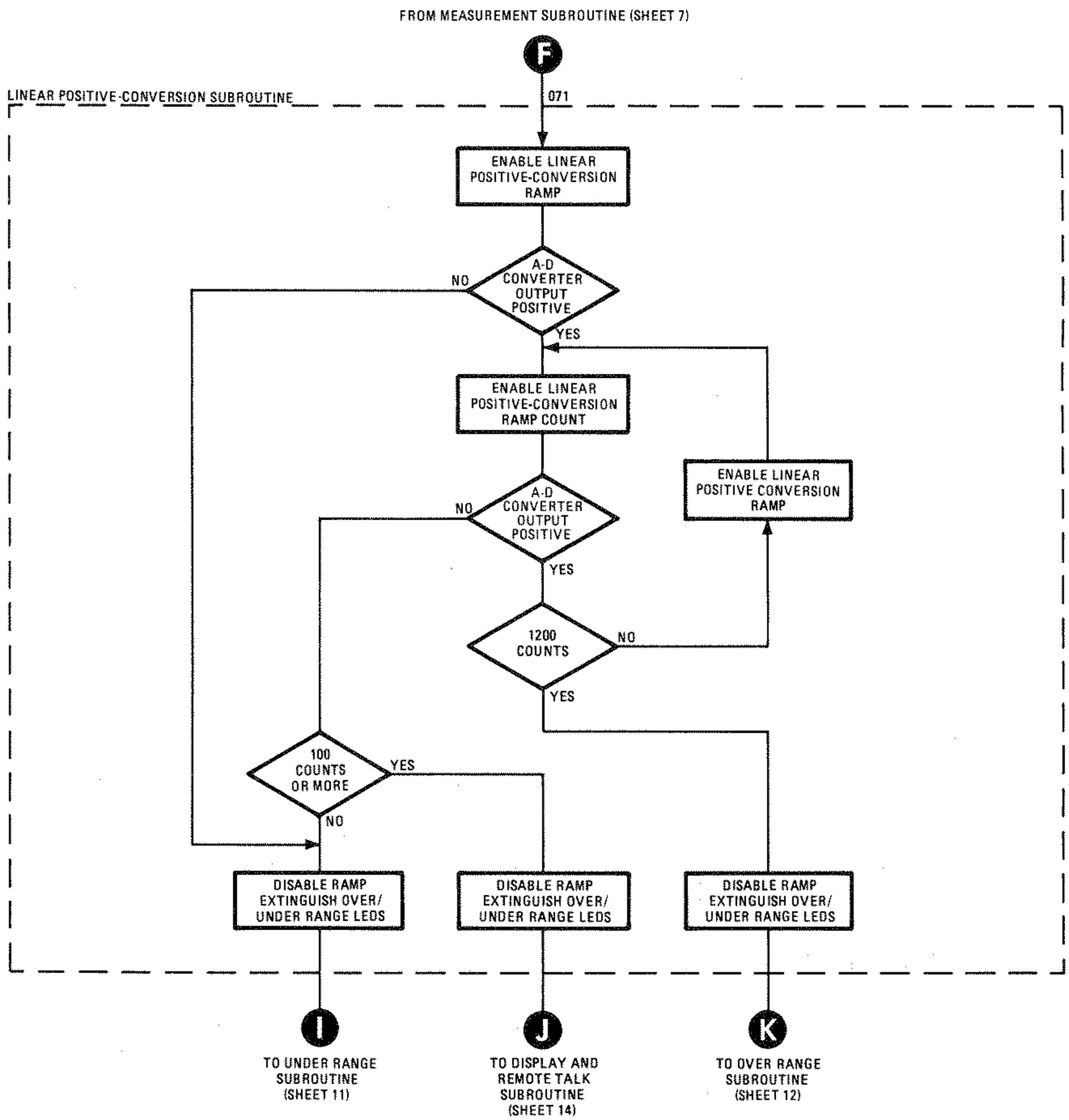


Figure 8-15. Operating Program Flow Chart (8A of 14)

8b

LINEAR POSITIVE CONVERSION SUBROUTINE

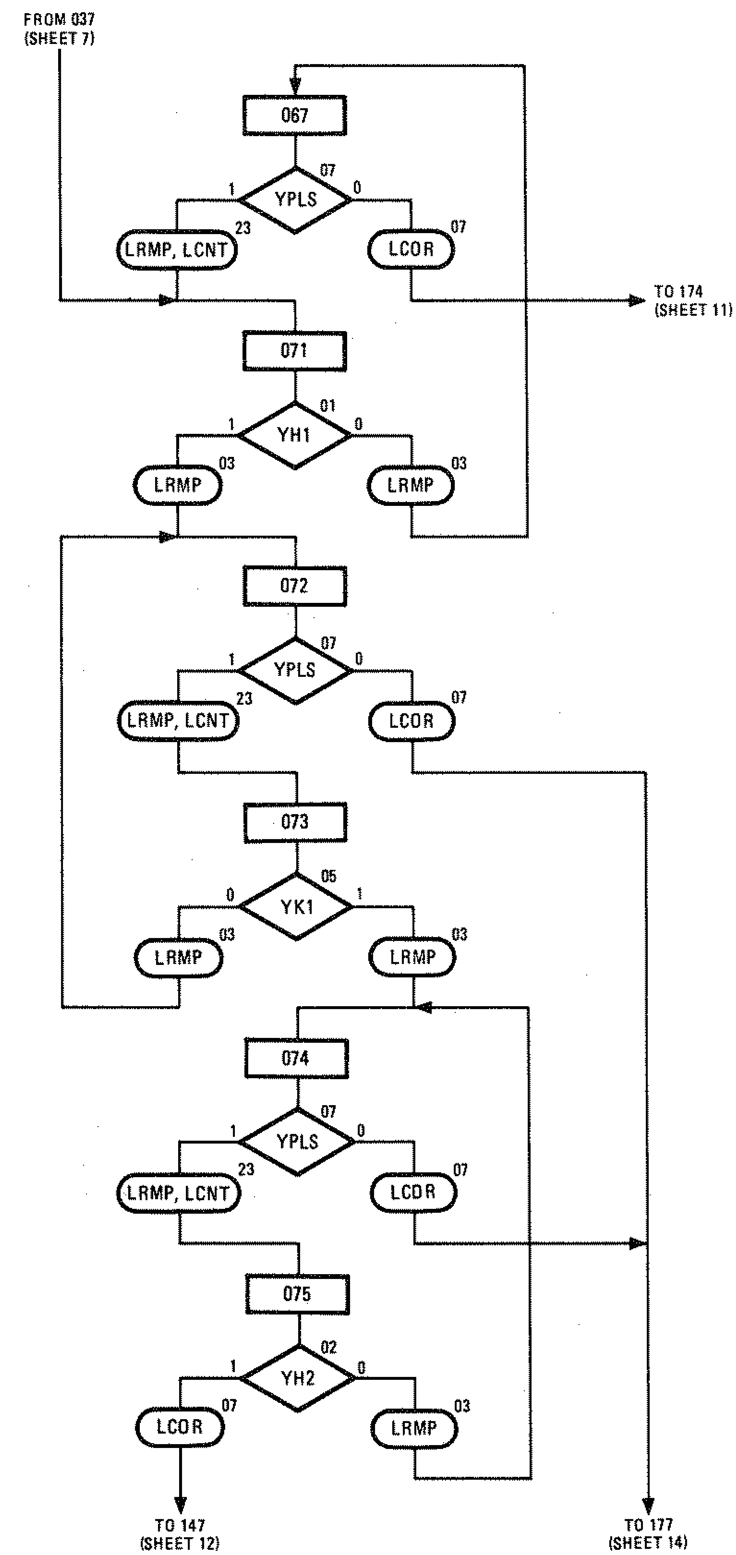


Figure 8-15. Operating Program Flow Chart (8B of 14)

9a

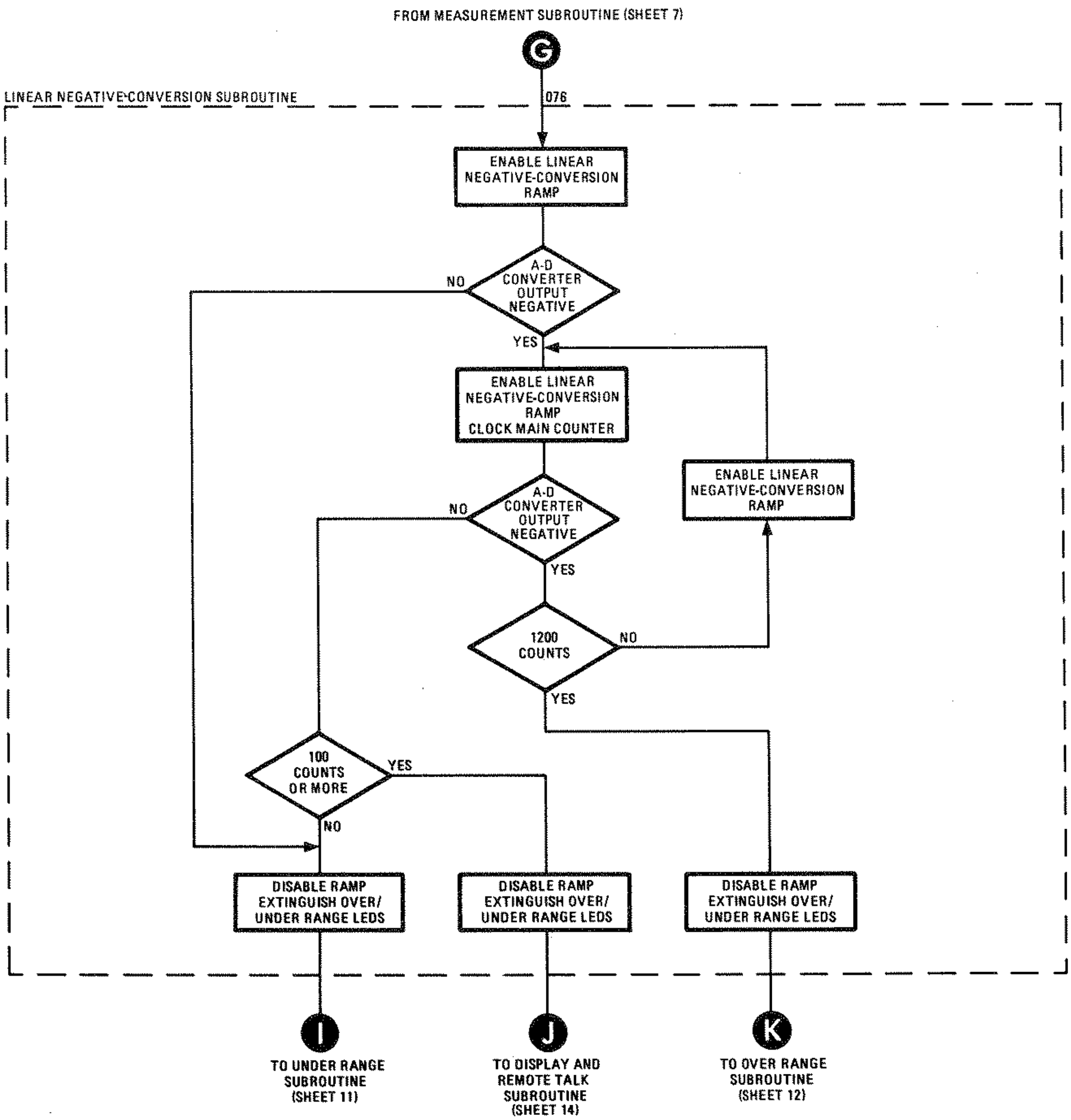


Figure 8-15. Operating Program Flow Chart (9A of 14)

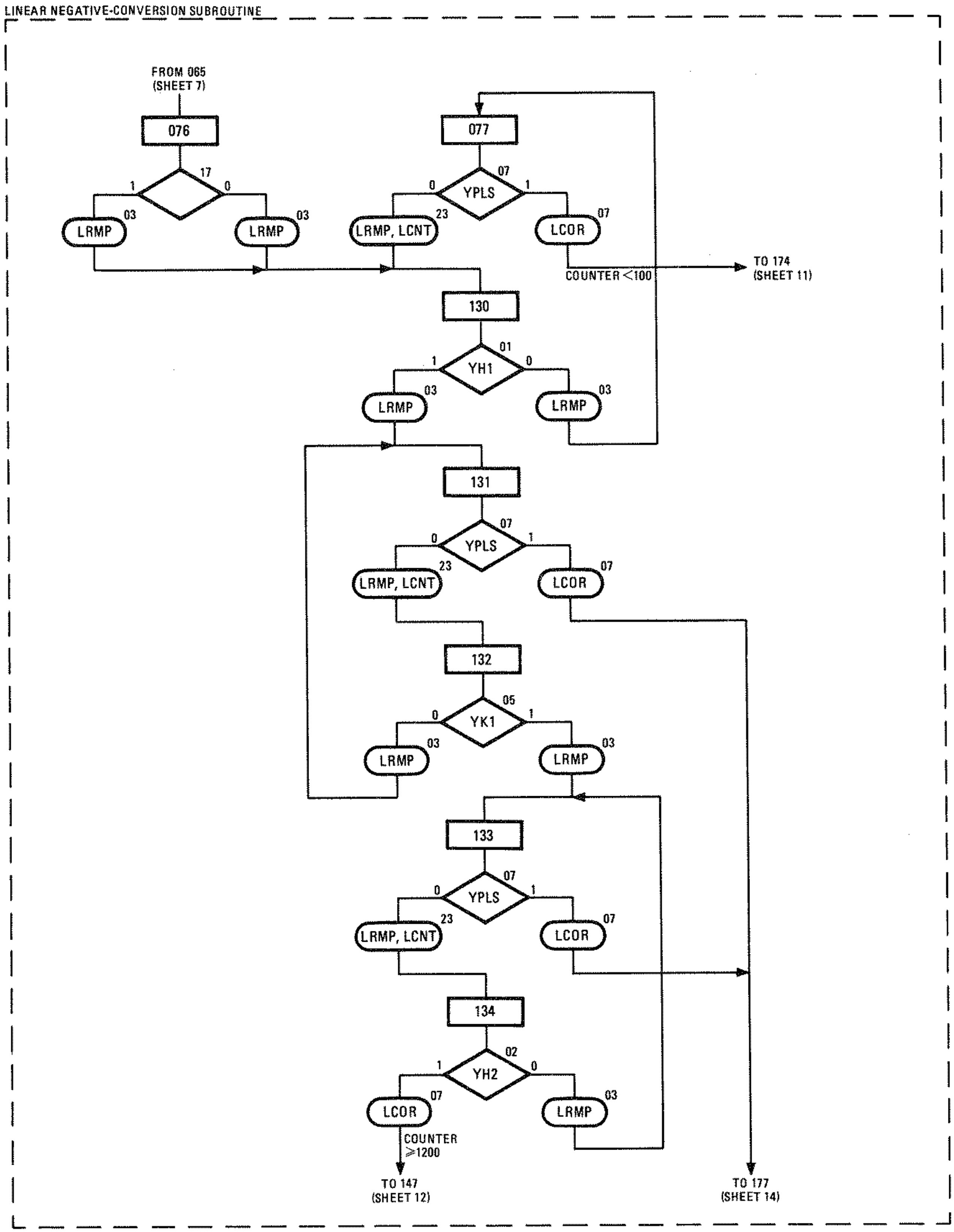


Figure 8-15. Operating Program Flow Chart (9B of 14)

10a

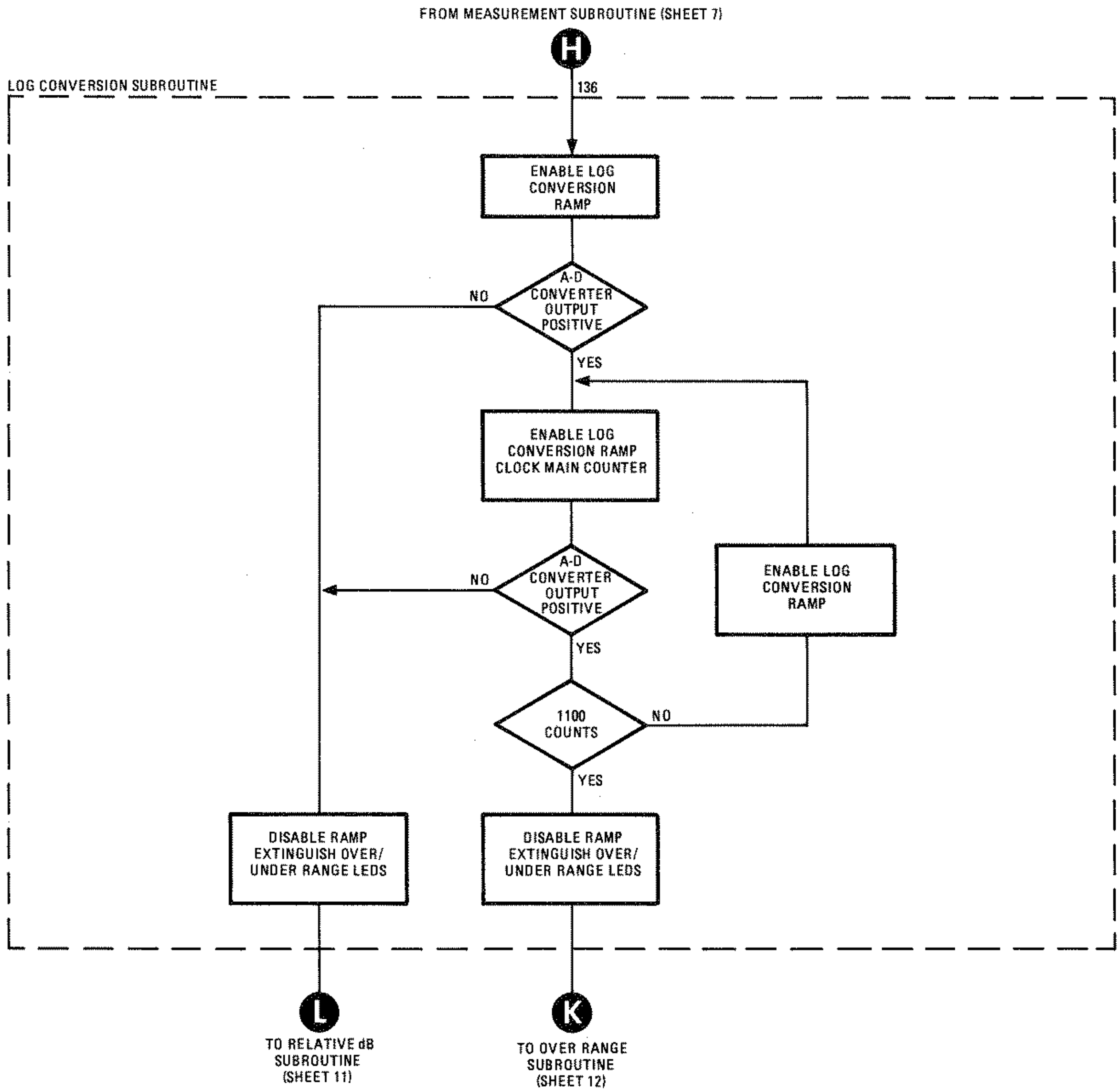


Figure 8-15. Operating Program Flow Chart (10A of 14)

10b

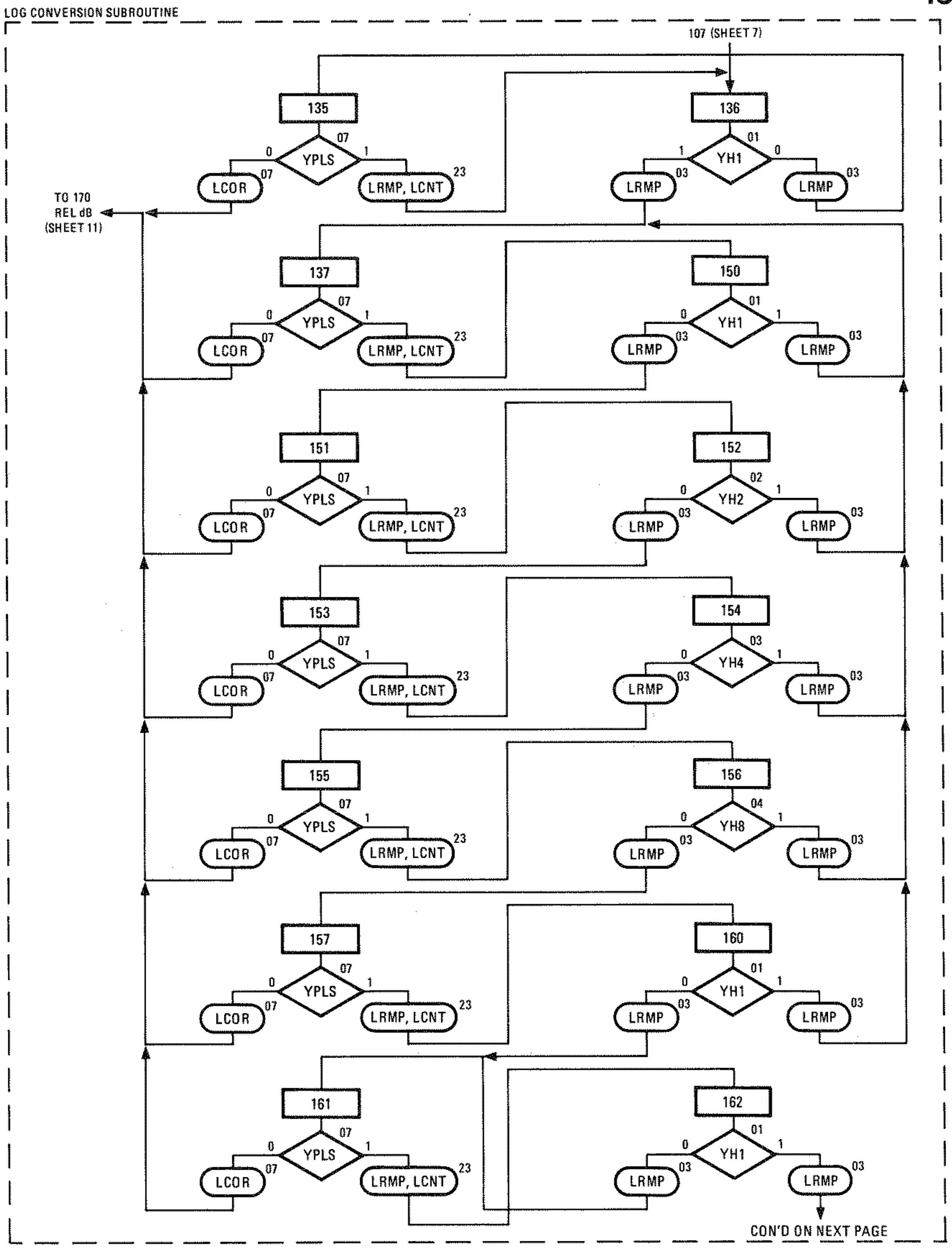


Figure 8-15. Operating Program Flow Chart (10B of 14)

10c

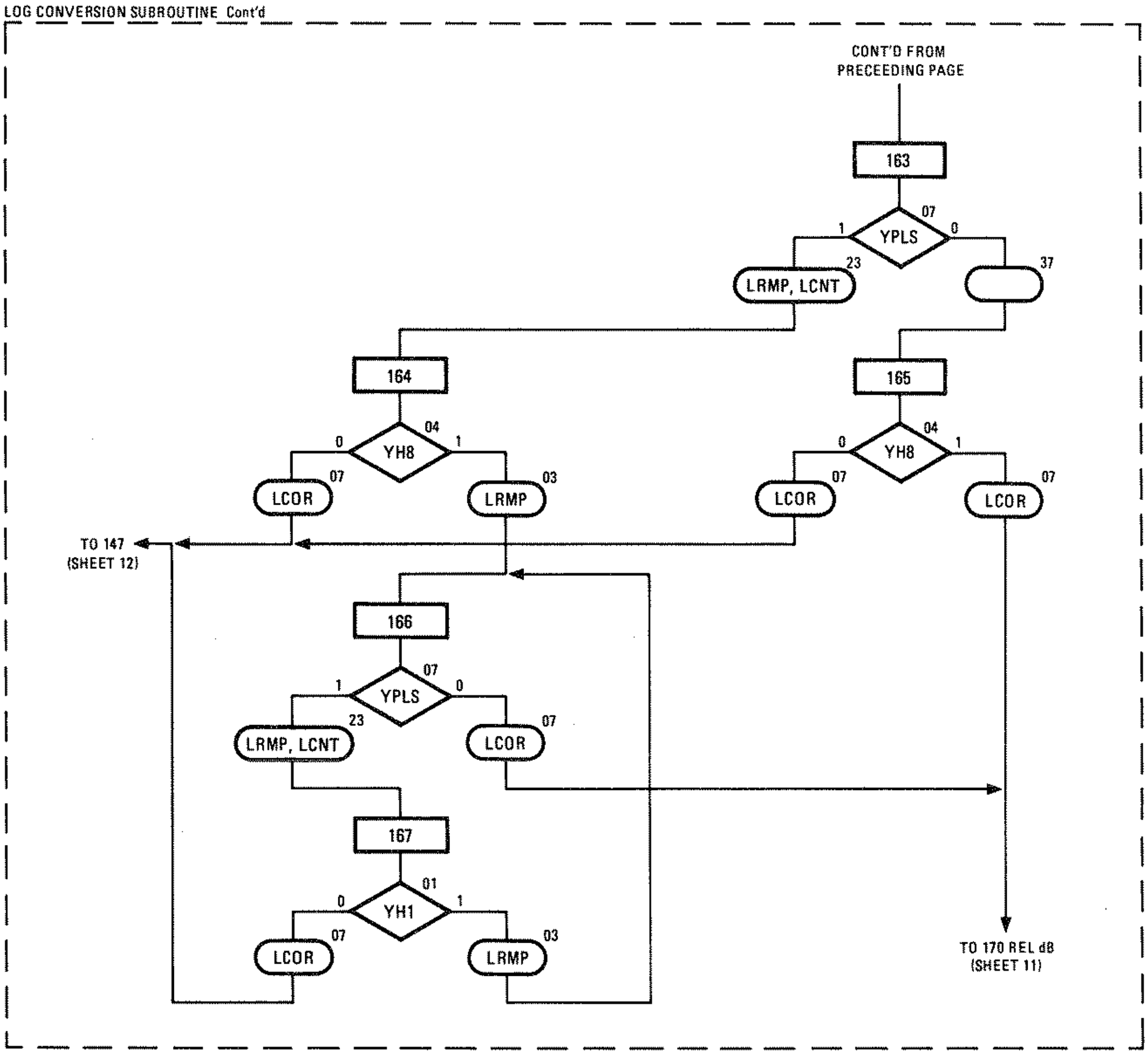


Figure 8-15. Operating Program Flow Chart (10C of 14)

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11a

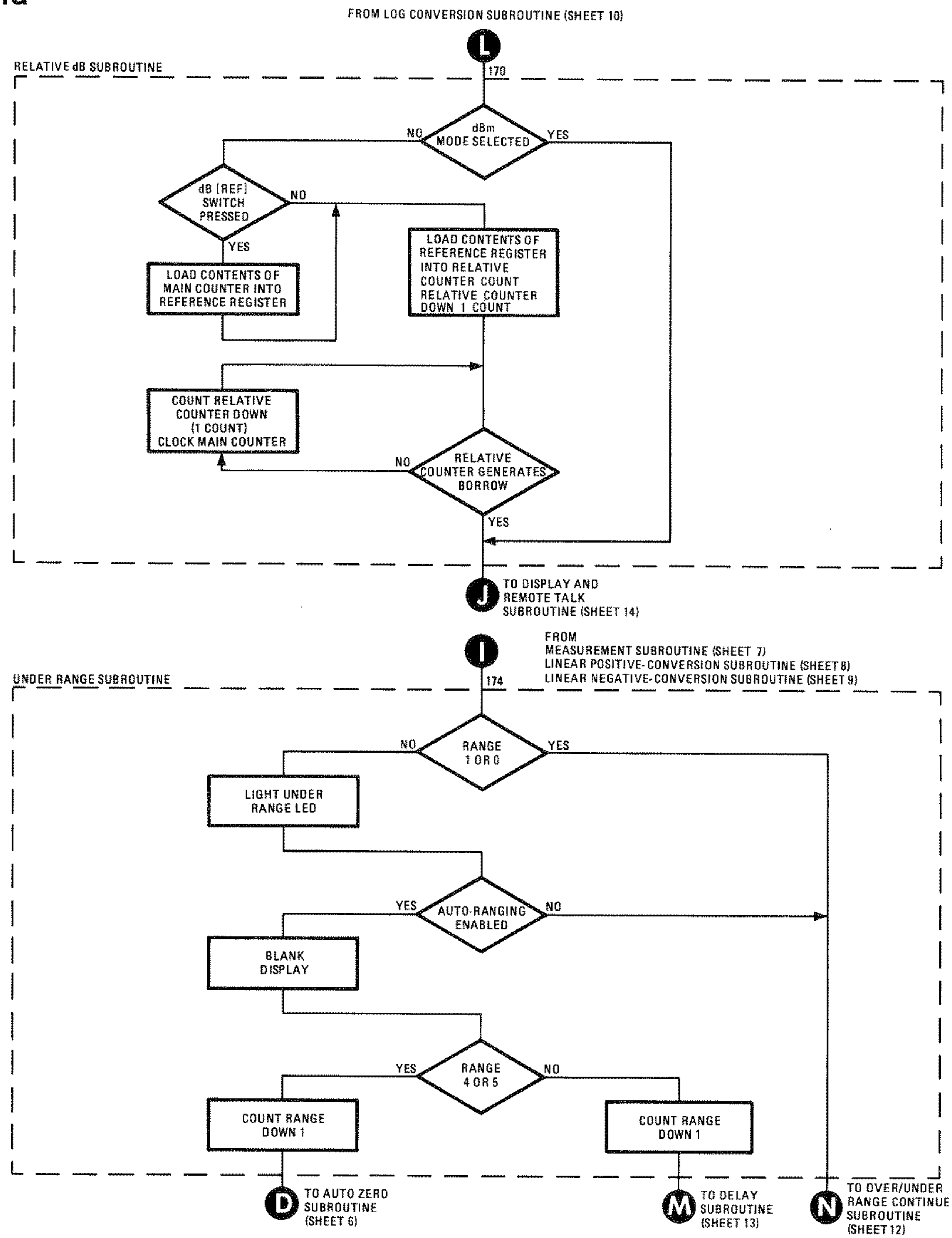

Figure 8-15. Operating Program Flow Chart (11A of 14)

11b

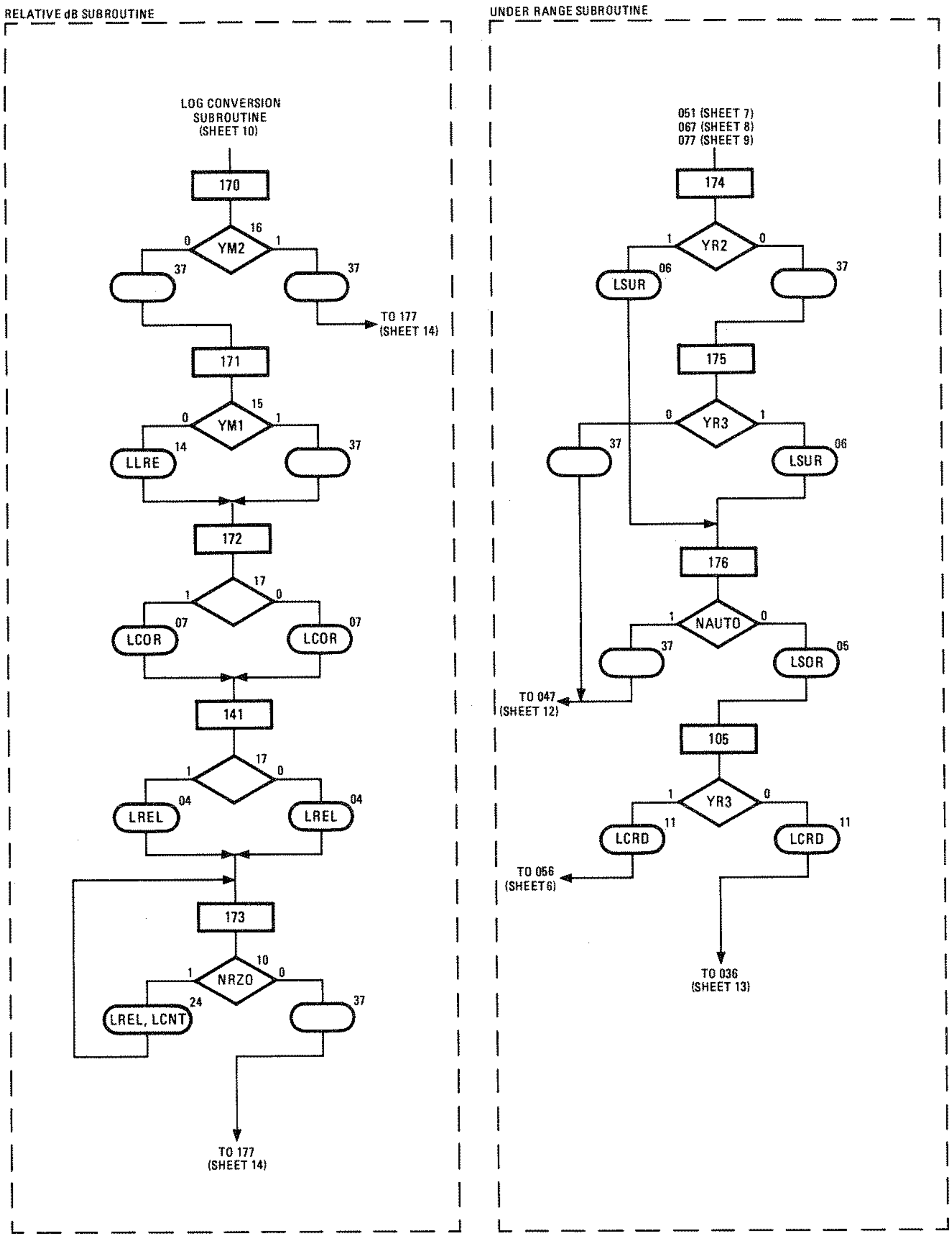

Figure 8-15. Operating Program Flow Chart (11B of 14)

12a

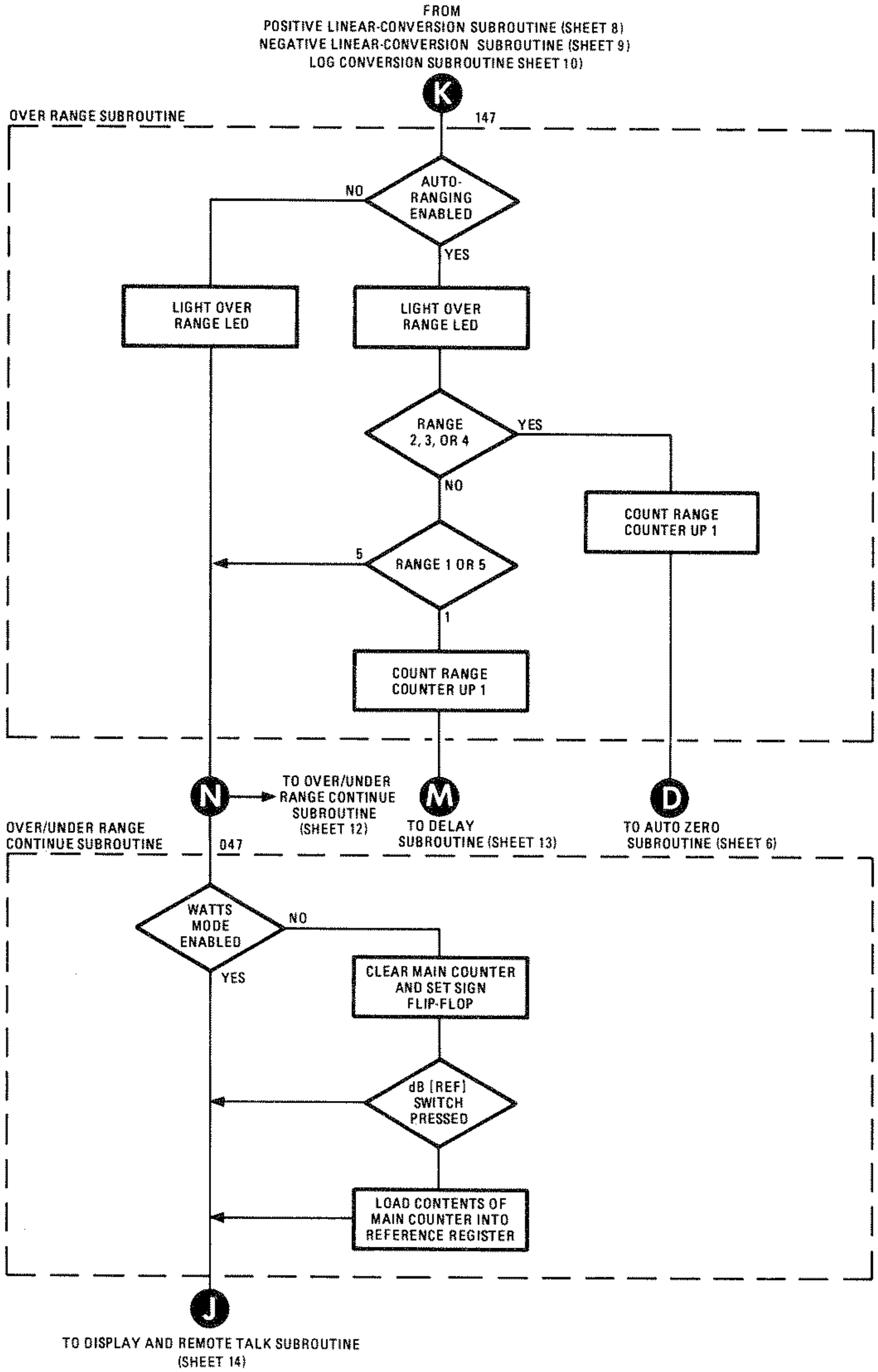

Figure 8-15. Operating Program Flow Chart (12A of 14)

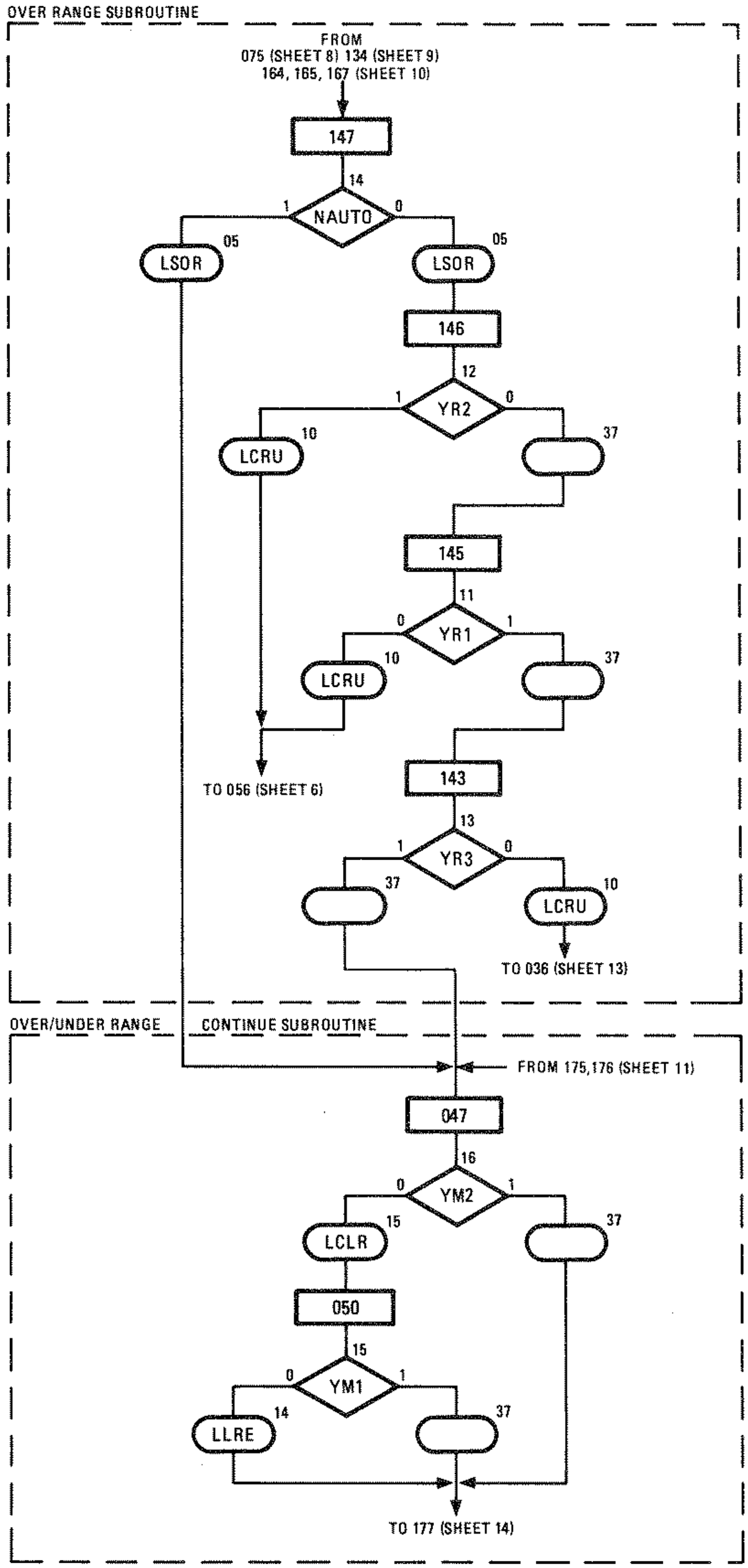

Figure 8-15. Operating Program Flow Chart (12B of 14)

13a

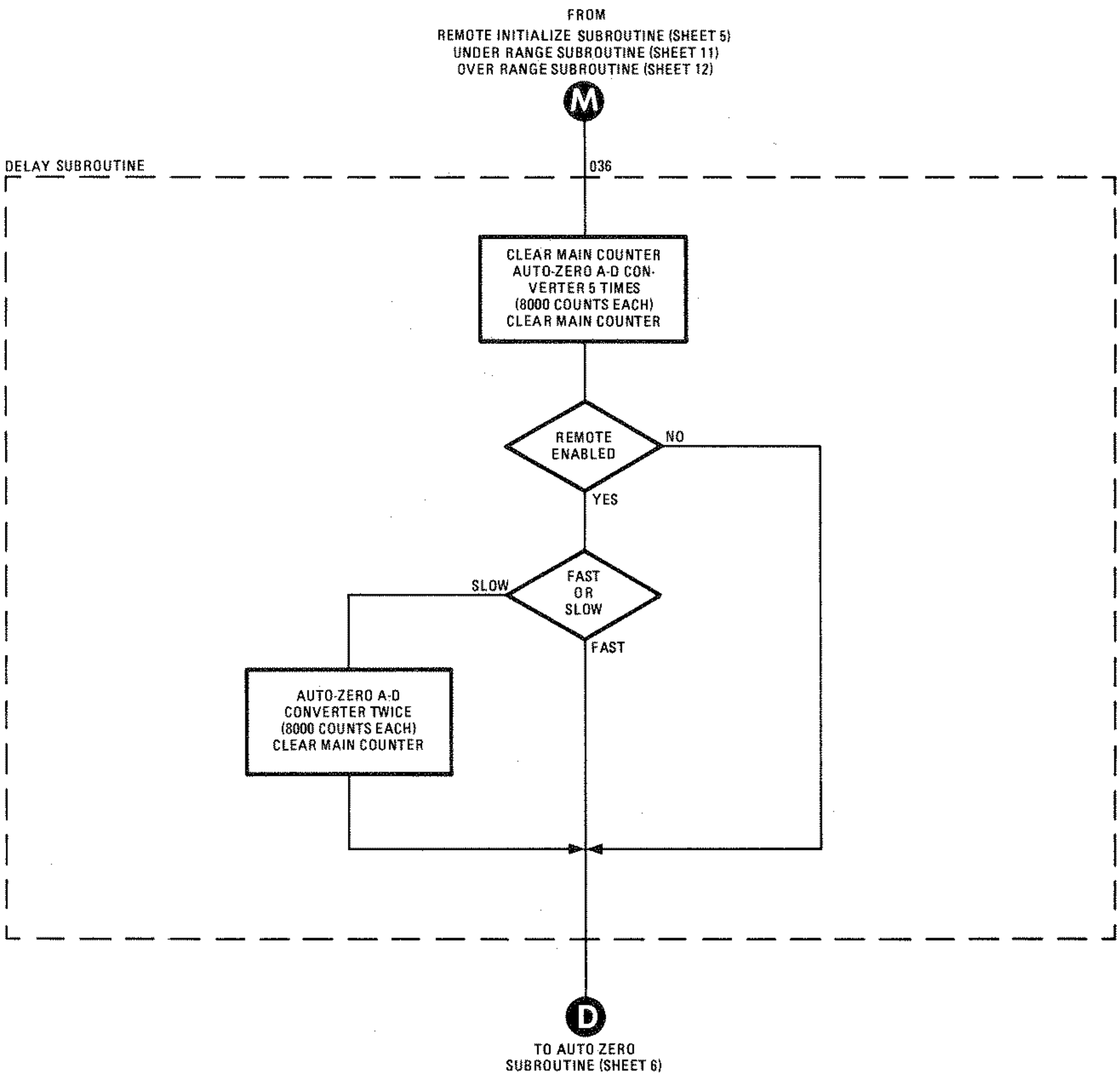

Figure 8-15. Operating Program Flow Chart (13A of 14)

13b

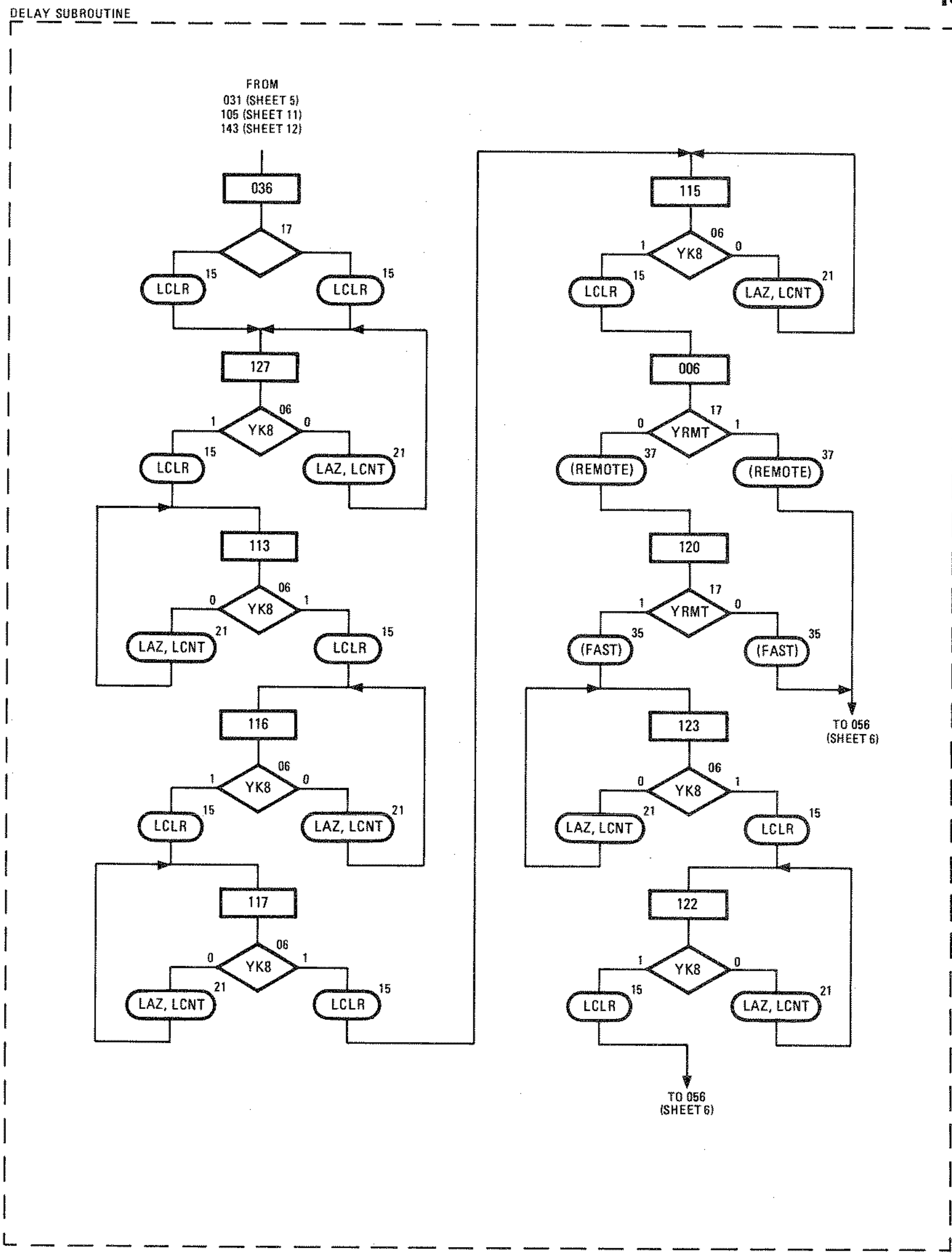

Figure 8-15. Operating Program Flow Chart (13B of 14)

14a

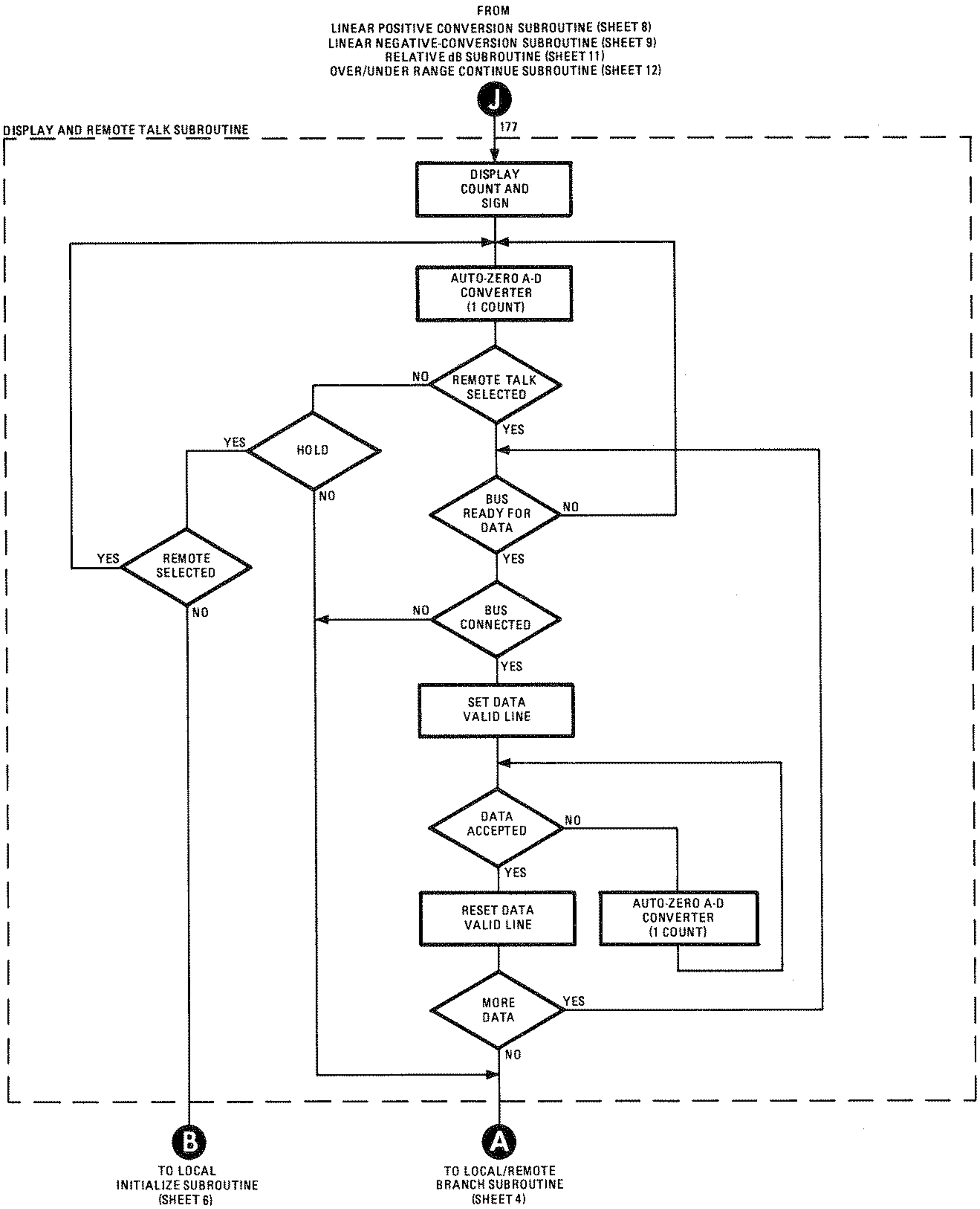

Figure 8-15. Operating Program Flow Chart (14A of 14)

14b

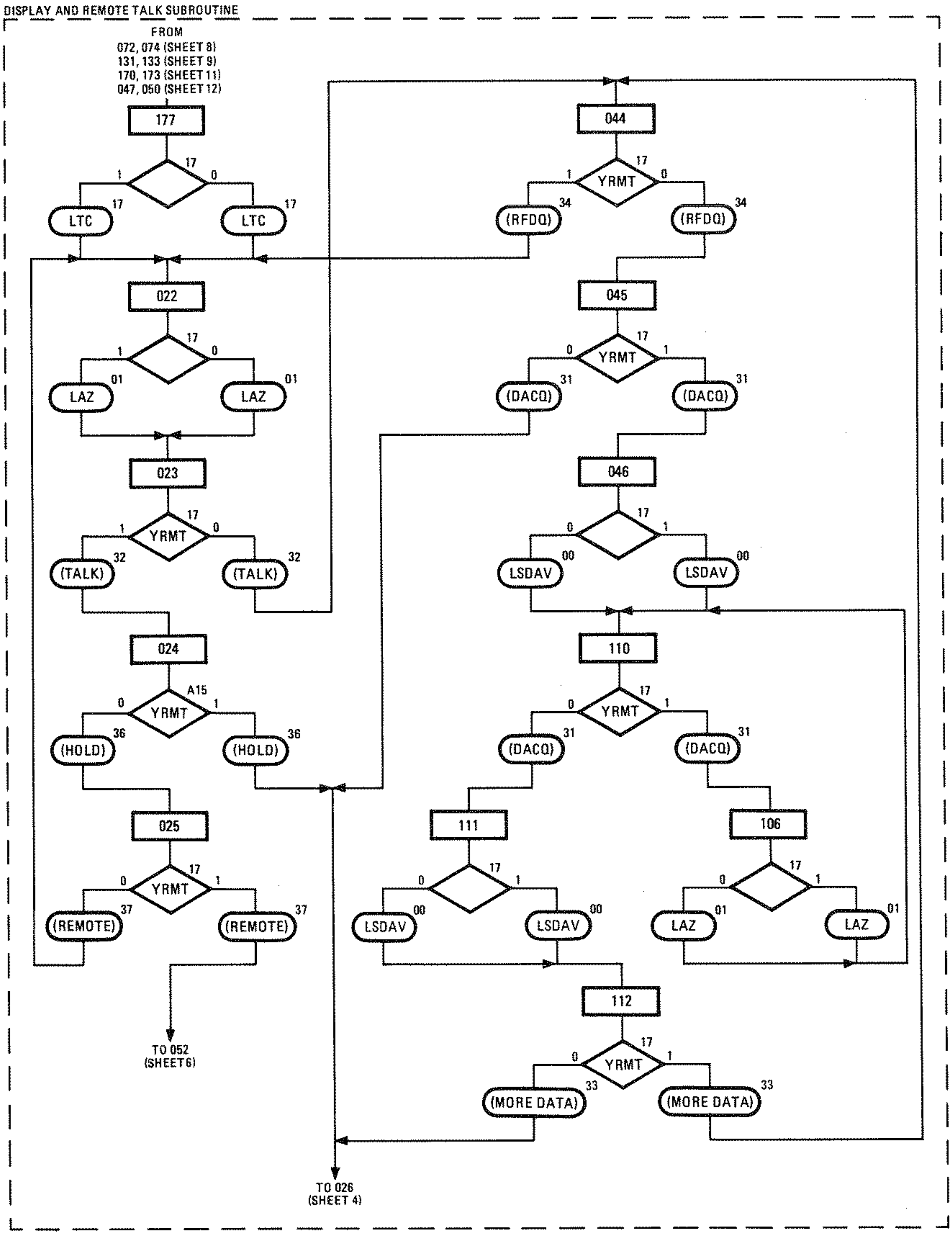

Figure 8-15. Operating Program Flow Chart (14B of 14)

Table 8-3. Standard Instrument Checkout (1 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
1	Connect Range Calibrator to Power Meter and set equipment controls as follows: **Range Calibrator** FUNCTION. . . . . CALIBRATE POLARITY . . . . NORMAL RANGE . . . . 30 mW LINE . . . . ON **Power Meter** CAL FACTOR % . . . 100 POWER REF . . . . Off (out) MODE . . . . WATT RANGE HOLD . . . ON (in) LINE . . . . ON When power is first applied verify that digital readout is blanked. Then wait two seconds for display to stabilize and verify that: a. Power Supply outputs are: +15.0 ± 0.5 Vdc; less than 0.01 Vac ripple and noise −15.0 ± 0.5 Vdc; less than 0.01 Vac ripple and noise +5.00 ±0.25 Vdc; less than 0.01 Vac ripple and noise. b. Digital Readout indicates 31.6 ±8.0 mW. c. mW lamp is lit and all other front-panel lamps are not lit.	**NOTE** *If the Power Meter is equipped with either remote interface option (002 or 024), remove both the A6 and A7 Assemblies before performing the standard checkout procedure.* DESCRIPTION — This step verifies that the power supplies are operating properly, that the Power Meter powers up normally, and that the Power Meter is capable of displaying a WATT MODE, range 5 30% input power level. **NOTE** *If Power Supply outputs are not within specifications, the ROMs used in the instrument may provide random outputs, thereby causing the Power Meter to operate erratically.* KEY OPERATING SEQUENCE **Power Up Subroutine** Refer to Table 8-6, Operating Program Descriptions **Local Initialize Subroutine** Branch to Auto Zero Subroutine **Auto Zero Subroutine** Refer to Table 8-6, Operating Program Descriptions **Measurement Subroutine** **NOTE** *A-D Converter input voltage at DC test point (A3TP4 should be stabilized at +0.316 ± 0.080 Vdc at address 061.* Load input voltage into A-D Converter (ramp amplitude at RMP test point A3TP2 is 2.24 ± 0.57 Vp-p). Initiate linear positive-conversion and branch to Linear Positive-Conversion Subroutine. **Linear Positive Conversion Subroutine** Detect YPLS = 0 at address 072 (633 ± 160 clock pulse, 10.5 ± 2.7 ms after address 071). Clear OVER and UNDER RANGE indications Branch to Display and Remote Talk Subroutine **Display and Remote Talk Subroutine** Display main counter output (316 ± 80) and positive sign (off)

Table 8-3. Standard Instrument Checkout (2 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
2	Turn Power Meter CAL ADJ control slightly clockwise and counterclockwise and verify that indication on Digital Readout increases and decreases.	DESCRIPTION — The previous step verified program execution up to the first address of the Display and Remote Talk Subroutine. This step verifies that the Power Meter CAL ADJ control is operational and that the program branches from the Display and Remote Talk Subroutine to the Local Initialize Subroutine, and then continues to cycle. KEY OPERATING SEQUENCE — Program execution and circuit operation verified in previous step except as indicated below. **Display and Remote Talk Subroutine** Branch to Local Initialize Subroutine . **Measurement Subroutine** **NOTE** *Voltage at DC test point A3TP4 should vary as CAL ADJ control is rotated.* Ramp amplitude at RMP test point A3TP2 changes in proportion to voltage change at DC test point A3TP4 (1 mV change at A3TP4 = 7.1 mV change in p-p ramp amplitude).
3	Set Range Calibrator RANGE switch to 100 mW and adjust CAL ADJ control to obtain 100.1 indication on Digital Readout.	DESCRIPTION — This step verifies that the Power Meter is capable of properly displaying a WATT MODE, Range 5 100% input power level. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: **Measurement Subroutine** Voltage at DC test point A3TP4 is adjustable to 1.001 ± 0.003V. Ramp amplitude at RMP test point A3TP2 is 7.1 Vp-p. **Linear Positive Conversion Subroutine** Detect YPLS = 0 at address 074 (2004 clock pulses, 33.4 ms, after address 071). Branch to Display and Remote Talk Subroutine.
4	Turn Power Meter CAL ADJ control to obtain 100.0 mW indication, then set CAL FACTOR % switch, in turn, to each position. Verify that the indications given on the following page are obtained.	DESCRIPTION — This step verifies that the CAL FACTOR % switch is operating properly and that the Power Meter is capable of properly displaying a WATT MODE, Range 5 117% input power level. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated on the following page.

Table 8-3. Standard Instrument Checkout (3 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
4 (cont)	Position / Indication 99 101.0 ±0.2 mW 98 102.0 ±0.2 mW 97 103.1 ±0.2 mW 96 104.2 ±0.2 mW 95 105.3 ±0.2 mW 94 106.4 ±0.2 mW 93 107.5 ±0.2 mW 92 108.7 ±0.2 mW 91 109.9 ±0.2 mW 90 111.1 ±0.2 mW 89 112.4 ±0.2 mW 88 113.6 ±0.2 mW 87 114.9 ±0.2 mW 86 116.3 ±0.2 mW 85 117.6 ±0.2 mW	CAL FACTOR % Switch Position / A-D Converter Input Voltage (DC test point A3TP4) / A-D Converter Ramp Amplitude (RMP test point A3TP2) 99 1.010 ±0.002 7.171 ±0.014 98 1.020 ±0.002 7.242 ±0.014 97 1.031 ±0.002 7.320 ±0.014 96 1.042 ±0.002 7.398 ±0.014 95 1.053 ±0.002 7.467 ±0.014 94 1.064 ±0.002 7.554 ±0.014 93 1.075 ±0.002 7.633 ±0.014 92 1.087 ±0.002 7.718 ±0.014 91 1.099 ±0.002 7.803 ±0.014 90 1.111 ±0.002 7.889 ±0.014 89 1.124 ±0.002 7.980 ±0.014 88 1.136 ±0.002 8.066 ±0.014 87 1.149 ±0.002 8.158 ±0.014 86 1.163 ±0.002 8.257 ±0.014 85 1.176 ±0.002 8.350 ±0.014
5	Turn Power Meter CAL ADJ control clockwise as required to obtain OVER RANGE indication; i.e., Digital Readout is blanked and OVER RANGE indicator is lit.	DESCRIPTION — This step verifies that the Power Meter is capable of detecting and indicating an OVER RANGE indication. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: **Measurement Subroutine** A-D Converter Input Voltage at DC test point A3TP4 is adjustable to greater than +1.200V. Ramp amplitude at RMP test point A3TP2 is greater than 8.4 Vp-p. **Linear Positive-Conversion Subroutine** Branch from address 075 to Over Range Subroutine (2403 clock pulses, 33.4 ms, after start address 071). **Over Range Subroutine** Light OVER RANGE indicator and blank Digital Readout (1_ . _). Branch to Over/Under Range Continue Subroutine. **Over/Under Range Continue Subroutine** Branch to Display and Remote Talk Subroutine.

Table 8-3. Standard Instrument Checkout (4 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
6	Turn Power Meter CAL ADJ control counterclockwise until OVER RANGE lamp goes out and indication appears on Digital Readout.	DESCRIPTION— This step verifies that the Power Meter is capable of detecting the end of an over range condition and resetting the front-panel display accordingly. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: **Over Range Subroutine** Branch to Over/Under Range Continue Subroutine when over range condition exists. **Over/Under Range Continue Subroutine** Branch to Display and Remote Talk Subroutine when over range condition exists. **Measurement Subroutine** A-D Converter input voltage at DC test point A3TP4 decreases to less than 1.200V. Ramp amplitude at RMP test point A3TP2 decreases to less than 8.5 Vp-p. **Linear Positive-Conversion Subroutine** Detect YPLS = 0 at address 074; reset OVER RANGE indication and clear blanked display.
7	Set CAL FACTOR % switch to 100 and turn Power Meter CAL ADJ control counterclockwise until Digital Readout indicates 99.0 mW. Then set Range Calibrator RANGE switch to 10 mW and verify that Digital Readout indicates 9.8 ± 0.2 mW and that UNDER RANGE indicator lights.	DESCRIPTION — This step verifies that the Power Meter is capable of detecting and indicating an under-range condition. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: **Measurement Subroutine** A-D Converter input voltage at DC test point A3TP4 is 0.098 ± 0.001V. Ramp amplitude at RMP test point A3TP2 is 0.696 ± 0.014 Vp-p. **Linear Positive Conversion Subroutine** YPLS = 0 detected at address 067 (delay = 198 ± 2 clock pulses, 3.3 ms, after start address 071). Branch to Under Range Subroutine. **Under Range Subroutine** Light UNDER RANGE indicator. Branch to Over/Under Range Continue Subroutine.

Table 8-3. Standard Instrument Checkout (7 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
14	Set Range Calibrator RANGE switch to 300 μW and verify that Power Meter auto-ranges to range 3 (refer to step 8) and that Digital Readout indicates .316 ± .01 mW.	DESCRIPTION — This step verifies that the Power Meter will auto-range from range 4 to range 3 when the input power level is changed from a range 4 30% level to a range 3 30% level. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except for range counter range 3 output and range 3 A-D Converter input voltage rise time at A3TP4. **Measurement Subroutine** (1st cycle after new input level) A-D Converter input voltage at DC test point A3TP4 decreases to less than 0.100V (range 4 selected). **Under Range Subroutine** Count range counter down one range to range 3. **Local Initialize Subroutine** Branch to Auto Zero Subroutine. **Auto Zero Subroutine** A-D Converter input voltage at DC test point A3TP4 stabilizes at 0.316 ± 0.002V by end of Auto Zero Subroutine (delay of 8000 clock pulses, 133 ms, after start address 056).
15	Set Range Calibrator RANGE switch to 30 μW and verify that Power Meter auto-ranges to range 2 according to the following sequence: a. Digital Readout blanks (0_ . _) momentarily and UNDER RANGE lamp lights momentarily. b. mW lamp goes out, μW lamp lights, and decimal point moves two places to right while Digital Readout is blanked. c. Digital Readout indication changes from blanked to 31.6 ± 1.0 mW.	DESCRIPTION — This step verifies that the Power Meter will auto-range from range 3 to range 2 when the input power level is changed from a range 3 30% level to a range 2 30% level. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: **Measurement Subroutine** (1st cycle after new input level) A-D Converter input voltage at DC test point A3TP4 decreases to less than 0.100V (range 3 selected). **Under Range Subroutine** Light UNDER RANGE indicator (address 174). Blank Digital Readout (reference; previously verified). Branch to Delay Subroutine. **Delay Subroutine** Auto Zero A-D Converter (40,000 clock pulses, 666 ms). Branch to Auto Zero Subroutine. **Auto Zero Subroutine** A-D Converter input voltage (A3TP4) stabilizes at 0.316 +0.10V by end of Auto Zero Subroutine (delay of 8000 counts, 133 ms, after start address 056). **NOTE** *As previously verified, UNDER RANGE indication is reset and Digital Readout is unblanked in first subsequent Linear Positive Conversion Subroutine.*

Table 8-3. Standard Instrument Checkout (8 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
16	Set Power Meter RANGE HOLD switch to on (in) and Range Calibrator FUNCTION switch to STANDBY. Press Power Meter SENSOR ZERO switch and verify that μW lamp remains lit and that ZERO lamp lights and remains lit for approximately four seconds. Adjust ZERO OFF potentiometer A3R47 as required to obtain 00.0 indication with blinking — sign when ZERO lamp is lit, and verify that indication remains at 00.0 ± 00.2 when ZERO lamp goes out.	DESCRIPTION — This step is a course adjustment of the ZERO OFF potentiometer; it provides a proper reference for the spike balance adjustment performed in the next step. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: a. Power Meter remains configured in WATT MODE (refer to Service Sheet 3, Mode Selection). b. Voltage at DC test point A3TP4 is adjustable to ±0.010V.
17	Set Range Calibrator FUNCTION switch to CALIBRATE and RANGE switch to 100 μW. Observe indication on Digital Readout and adjust Power Meter CAL ADJ control to obtain 100.0 μW indication. Then press and hold SENSOR ZERO switch and adjust BAL potentiometer A3R65 as required to obtain 60.0 ± 0.2 μW indication while ZERO lamp is lit.	DESCRIPTION — This step adjusts BAL potentiometer A3R65 to center the sensor zero circuit output voltage range (Service Sheet 8). KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: a. Voltage at DC test point A3TP4 is adjustable to 1.000 ±0.002V when SENSOR ZERO switch is not pressed. b. Voltage at DC test point A3TP4 is adjustable to 0.600 ± 0.002V with BAL potentiometer A3R65 when SENSOR ZERO switch is pressed.
18	Set Range Calibrator FUNCTION switch to STANDBY, then press and release Power Meter SENSOR ZERO switch. Verify that Digital Readout indication changes back to 00.0 with blinking — sign while ZERO lamp is lit and remains at 00.0 ± 00.2 when ZERO lamp goes out.	DESCRIPTION — This step rezeros the Power Sensor to establish the proper reference conditions for the next step.
19	Set Range Calibrator RANGE switch to 3 μW and FUNCTION switch to CALIBRATE. Verify that an UNDER RANGE indication is observed, then release Power Meter RANGE HOLD switch and verify that Power Meter auto-ranges to range 1 according to the following sequence: a. μW lamp remains lit. b. Digital Readout blanks momentarily and UNDER RANGE lamp lights momentarily; decimal point moves one position to left while Digital Readout is blanked. c. Digital Readout indication changes from blanked to 3.16 ± 1.0 mW.	DESCRIPTION — This step verifies the capability of the Power Meter to auto-range from range 2 to range 1 and to properly display a range 1 30% input power level. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: a. A-D Converter input voltage at DC test point A3TP4 is 0.032 ± 0.01V when RANGE HOLD switch is set to on (in). b. Range counter is counted down to range 1 during Under Range Subroutine when RANGE HOLD switch is set to off. c. Program branches from Local Initialize Subroutine (address 054) to Auto Zero Subroutine. d. A-D Converter input voltage at DC test point A3TP4 rises to 0.316 ± 0.01V within ten seconds after range counter is counted down to range 1.

Table 8-3. Standard Instrument Checkout (9 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
20	Set Range Calibrator FUNCTION switch to STANDBY, press Power Meter SENSOR ZERO switch, and adjust ZERO OFF potentiometer A3R47 as required to obtain 0.00 ± 0.02 indication with blinking – sign while ZERO lamp is lit. Verify that UNDER RANGE lamp does not light and that Digital Readout indication remains at 00.0 ± 0.02 when ZERO lamp goes out. **NOTE** *Power Meter is now calibrated for WATT MODE operation and zeroed on the most sensitive range.*	DESCRIPTION — This step provides fine adjustment of the ZERO OFF potentiometer. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: a. When A-D Converter input voltage at DC test point A3TP4 decreases to less than 0.100V after FUNCTION switch is set to STANDBY, operating program branches from Under Range Subroutine (address 175) to Over/Under Range Continue Subroutine. b. A-D Converter input voltage at DC test point A3TP4 is adjustable to ±0.002V.
21	Set Range Calibrator RANGE switch to 30 μW and FUNCTION switch to CALIBRATE. Verify that Power Meter auto-ranges to range 2 (μW lamp is lit and decimal point is positioned immediately to left of least significant digit) and Digital Readout indicates 31.6 ± 0.2 μW.	DESCRIPTION — This step verifies that the Power Meter will auto-range from range 1 to range 2 when a range 2 28% input power level is applied. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: a. A-D Converter input voltage at DC test point A3TP4 rises to greater than 1.200V in less than 10 seconds. b. Range counter is counted up to range 2 during Over Range Subroutine and program branches to Delay Subroutine (address 143). c. A-D Converter input voltage at DC test point A3TP4 is stabilized at 0.316V by end of first Auto Zero Subroutine following Over Range Subroutine.
22	Set Range Calibrator RANGE switch to 300 μW and verify that Power Meter auto-ranges to range 3 (μW lamp goes out and mW lamp lights; decimal point moves two positions to left) and that Digital Readout indicates 0.316 ± 0.002 mW.	DESCRIPTION — This step verifies that the Power Meter will auto-range from range 2 to range 3 when a range 3 28% input power level is applied. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: a. A-D Converter input voltage at DC test point A3TP4 rises to greater than 1.200V within one second after input level is changed. b. Range counter is counted up to range 3 during Over Range Subroutine and program branches to Auto Zero Subroutine (address 146). c. A-D Converter input voltage at DC test point A3TP4 is stabilized at 0.316V by end of Auto Zero Subroutine.

Table 8-3. Standard Instrument Checkout (10 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
23	Set Range Calibrator RANGE switch to 3 mW and verify that Power Meter autoranges to range 4 (decimal point moves one place to right, mW lamp remains lit).	DESCRIPTION — This step verifies that the Power Meter will autorange from range 3 to range 4 when a range 4 28% input signal level is applied. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: a. A-D Converter input voltage at DC test point A3TP4 rises to greater than 1.200V within 0.10 second after level is changed. b. Range counter is counted up to range 4 during Over Range Subroutine (program branching and instructions previously verified). c. A-D Converter input voltage at DC test point A3TP4 is stabilized at 0.316V by end of Auto Zero Subroutine.
24	Set Power Meter RANGE HOLD switch to on (in) and Range Calibrator FUNCTION switch to STANDBY. Then set dBm MODE switch to on (in) and verify that indication changes as follows: a. UNDER RANGE lamp remains lit. b. mW lamp goes out and dBm lamp lights. c. Digital Readout blanks (0_ . _).	DESCRIPTION — This step verifies that the Power Meter can be configured for dBm MODE measurements. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: **Local Initialize Subroutine** Mode Register loaded **Measurement Subroutine** A-D Converter input voltage at DC test point A3TP4 is 0.000 ± 0.002V. Main counter is preset to 0000. Sign is preset positive. UNDER RANGE indicator is lighted. Digital Readout is blanked. Branch to Under Range Subroutine.

Table 8-3. Standard Instrument Checkout (11 of 17)

<table>
<tr><th>Step</th><th>Instrument Setup and Test Procedure</th><th>Test Description and Key Operating Sequence</th></tr>
<tr><td>25</td><td>Set Range Calibrator RANGE switch to 0 dBm and FUNCTION switch to CALIBRATE. Adjust Power Meter LZR potentiometer (A3R59) as required to obtain 0.00 dBm indication on Digital Readout.

NOTE
This step sets the A-D Converter log threshold. When the specified indication is obtained, the Digital Readout should be just on the verge of blanking, i.e., the Digital Readout may randomly alternate between 0.00 dBm and UNDER RANGE blanked (0_ . _).</td><td>DESCRIPTION — This step sets the A-D Converter Log Conversion threshold.

KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below:

Measurement Subroutine
A-D Converter input voltage at DC test point A3TP4 is 0.100 ± 0.002 Vdc.
Ramp amplitude at RMP test point A3TP2 is 0.71 ± 0.144 Vp-p.
LZR potentiometer can be adjusted so that YPLS qualifier alternates between 0 and 1 at address 066.
When YPLS=0, branch to Under Range Subroutine (reference; previously verified).
When YPLS=1, branch to Log Conversion Subroutine.

Log Conversion Subroutine
Detect YPLS=0 at address 135.
Branch to Relative dB Subroutine.

Relative dB Subroutine
Branch to Display and Remote Talk Subroutine.</td></tr>
<tr><td>26</td><td>Set Power Meter CAL FACTOR % switch to 85 and verify that Digital Readout indicates 0.70 ± 0.02 dBm. Then adjust CAL ADJ control as required to obtain the following indications:

a. 1.01 dBm.
b. 2.02 dBm.

After verifying indications, set CAL FACTOR % switch to 100 and readjust CAL ADJ control to obtain 0.00 dBm indication.</td><td>DESCRIPTION — This step verifies the exponential slope of the log conversion ramp and the branching between various addresses in the Log Conversion Subroutine.

KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below:

<table>
<tr><th>A-D Converter Input Voltage (DC Test Point A3TP4)</th><th>Ramp Amplitude (RMP Test Point A3TP2)</th><th>Addresses Verified, Log Conversion Subroutine</th><th></th></tr>
<tr><td>0.117 ± 0.002
(0.70 ± 0.02 dBm)</td><td>0.831 ± 0.014</td><td>135,136</td><td rowspan="3">detect YPLS=0 and branch to dB Rel Subroutine</td></tr>
<tr><td>0.126 ± 0.002
(1.01 dBm)</td><td>0.895 ± 0.014</td><td>137, 150</td></tr>
<tr><td>0.159 ± 0.002
(2.02 dBm)</td><td>1.129 ± 0.014</td><td>151, 152</td></tr>
</table>

NOTE
If necessary, adjust LFS potentiometer A3R48 to obtain specified ramp amplitude.</td></tr>
</table>

Table 8-3. Standard Instrument Checkout (12 of 17)

<table>
<tr><th>Step</th><th>Instrument Setup and Test Procedure</th><th>Test Description and Key Operating Sequence</th></tr>
<tr><td>27</td><td>Set Power Meter CAL FACTOR % switch to 100 and Range Calibrator RANGE switch to 5 dBm. Adjust CAL ADJ control to obtain 5.06 dBm indication, then readjust CAL ADJ control to obtain 5.00 dBm indication.</td><td>DESCRIPTION — This step verifies the slope of the Log Conversion Ramp for a 46% input power level and the branching between various addresses in the Log Conversion Subroutine.

KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below:

A-D Converter Input Voltage (DC Test Point A3TP4) | Ramp Amplitude (RMP Test Point A3TP2) | Addresses Verified, Log Conversion Subroutine
0.320 ± 0.003 | 2.272 ± 0.014Vp-p | 153, 154, (detect YPLS = 0 and branch to dB Rel Subroutine)

NOTE
If necessary, adjust LFS potentiometer A3R48 to obtain specified ramp amplitude.</td></tr>
<tr><td>28</td><td>Set Range Calibrator RANGE switch to 10 dBm and adjust CAL ADJ control to obtain the following indications:
a. 10.02 dBm
b. 10.03 dBm
c. 10.05 dBm
d. OVER RANGE blanked Digital Readout (1_. _).</td><td>DESCRIPTION— This step verifies the slope of the Log Conversion Ramp for a 91% input power level and the branching between various addresses in the Log Conversion Subroutine.

KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below:

A-D Converter Input Voltage (DC Test Point A3TP4) | Ramp Amplitude (RMP Test Point A3TP2) | Addresses Verified, Log Conversion Subroutine
1.005 ± 0.002 (10.02 dBm) | 7.136 ± 0.014 Vp-p | 155,156 (detect YPLS=0 and branch to dB Rel Subroutine)
1.007 ± 0.002 (10.03 dBm) | 7.150 ± 0.014 Vp-p | 157, 160 (detect YPLS=0 and branch to dB Rel Subroutine)
1.012 ± 0.002 (10.05 dBm) | 7.185 ± 0.014 Vp-p | 161,162 (detect YPLS=0 and branch to dB Rel Subroutine)
>1.260V (OVER RANGE) | >8.946 Vp-p | 162, 163, 164, 165

NOTE
If necessary, adjust LFS potentiometer A3R48 to obtain specified ramp amplitude.</td></tr>
</table>

Table 8-3. Standard Instrument Checkout (13 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
29	Readjust CAL ADJ control to obtain 10.00 dBm indication on Digital Readout. Then set WATT MODE switch to on and adjust CAL ADJ control as required to obtain 10.00 mW indication. After obtaining this indication, set dBm MODE switch to on and adjust LFS potentiometer A3R48 to obtain 10.00 dBm indication. **NOTE** *Power Meter is now fully calibrated for both linear and log measurements.*	DESCRIPTION — This step adjusts the slope of the Log Conversion Ramp. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except for A-D Converter; refer to Service Sheet 8.
30	Set Range Calibrator RANGE switch to −15 dBm. Verify that UNDER RANGE indication is observed, set RANGE HOLD switch to off (out), and verify that Digital Readout indicates −15.00 ± 0.50 dBm. Then set Range Calibrator FUNCTION switch to STANDBY, press Power Meter SENSOR ZERO switch, return Range Calibrator FUNCTION switch to CALIBRATE when ZERO lamp goes out, and verify that Digital Readout indication is −15.00 ±0.02 dBm.	DESCRIPTION — This step verifies that the main counter is preset properly and that it can be counted down normally for the negative dBm ranges. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except for main counter preset and down counting; refer to Service Sheet 9.
31	Set Range Calibrator RANGE switch to −10.00 dBm and adjust Power Meter CAL ADJ control to obtain the following indications: a. 9.99 dBm b. 9.97 dBm c. OVER RANGE blanked (−0 _ . _) After verifying indications, readjust CAL ADJ control to obtain −10.00 dBm indication.	DESCRIPTION — This step verifies branching between various addresses in the Log Conversion Subroutine. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except for branching between Log Conversion Subroutine addresses listed below: a. 9.99 dBm indication verifies the following address branches: 163, 165, dB Rel Subroutine. b. 9.97 dBm indication verifies the following address branches: 164, 166, 167, branch to dB Rel Subroutine from address 166. c. OVER RANGE indication verifies the branch from address 167 to the Over Range subroutine.

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Table 8-3. Standard Instrument Checkout (14 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
32	Set Range Calibrator RANGE switch to −5 dBm, then press Power Meter dB [REF] MODE switch and hold for two seconds. Verify that dBm lamp goes out, dB (REL) lamp lights, and indication on Digital Readout changes to −0.00.	DESCRIPTION — This step verifies the capability of the Power Meter to store a dB reference level and to indicate input power levels with respect to the stored reference. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: a. Program execution and circuit operation when dB [REF] switch is pressed. **Local Initialize Subroutine** Mode select inputs loaded into mode register; output of mode register indicates Power Meter configured for dB [REF] MODE. **Measurement Subroutine** Branch to Log Conversion Subroutine. **Log Conversion Subroutine** Branch to dB Relative Subroutine (reference; previously verified. **dB Relative Subroutine** Load sign and contents of main counter into reference register. Load contents of reference register into relative register. Count main and relative counters down until contents of relative counter = 0. Branch to Display and Remote Talk Subroutine. **NOTE** *Program execution and circuit operation when dB [REF] switch released is same as above except contents of main counter are not loaded into reference register.*
33	Set Power Meter RANGE HOLD switch to off (out) and Range Calibrator RANGE switch, in turn, to −10 and +5 dBm. Verify that Digital Readout indication changes to −5.00 ± 0.02 and 10.00 ± 0.02 dBm, respectively. Then set Range Calibrator RANGE switch to −5 dBm and adjust CAL ADJ control as required to obtain 1.00 dBm indication on Digital Readout. After verifying 1.00 dBm indication, readjust CAL ADJ control for 0.00 indication.	DESCRIPTION — This step verifies the up/down counting of the main counter when a negative dB reference value is stored. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: **NOTE** *dB Relative Subroutine address 171 (YM1=1) not verified in previous step.* a. When RANGE switch is set to −10 dBm, main counter is counted down to obtain specified indication on Digital Readout. b. When RANGE switch is set to +5 dBm, main counter is counted up to obtain specified indication. c. When RANGE switch is set to −5 dBm and CAL ADJ control is adjusted for 1.00 dBm indication, main counter is first counted down to 0000 then up to 0100 to obtain indication (sign changes when main counter goes through 0).

Table 8-3. Standard Instrument Checkout (15 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
34	Set Range Calibrator RANGE switch to 5 dBm. Press dB [REF] MODE switch, and observe indication on Digital Readout change to 0.00 dBm. Then set Range Calibrator RANGE switch, in turn, to 10 and −5 dBm and verify that Digital Readout indication changes to +5.00 ± 0.02 and −10.00 ± 0.02 dBm, respectively.	DESCRIPTION — This step verifies the up/down counting of the main counter when a positive dBm reference value is stored. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: a. When RANGE switch is set to 10 dBm, main counter is counted down to obtain specified indication. b. When RANGE switch is set to −5 dBm, main counter is counted up to obtain specified indication.
35	Set Range Calibrator RANGE switch to 5 dBm and adjust CAL ADJ control to obtain −1.00 dBm indication on Digital Readout.	DESCRIPTION — This step verifies the down/up counting of the main counter when a positive dBm reference value is stored and a slightly less positive input power level is applied. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except for down/up counting of main counter (sign changes when main counter goes through 0 000); refer to Service Sheet 9.
36	Set Range Calibrator RANGE switch to 20 dBm, press dB [REF] switch and observe that Digital Readout indication changes 0.00. Then turn CAL ADJ control clockwise to obtain OVER RANGE blanked indication and counterclockwise to clear OVER RANGE indication. Verify that when OVER RANGE indication is cleared, new indication on Digital Readout is with respect to stored reference of 20.00 dBm.	DESCRIPTION — This step verifies that dB Relative Subroutine address branching is proper for a dB (REL) MODE OVER RANGE condition. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except for addresses 047 (YM2=0) and 050 (YM1=1) of Over/Under Range Continue Subroutine.
37	Repeat step 35 except press dB [REF] switch when OVER RANGE indication is present. Verify that when OVER RANGE indication is cleared, new indication is greater than 20.00 dBm.	DESCRIPTION — This step verifies that the reference register is cleared when the dB [REF] switch is pressed while an OVER RANGE condition exists. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except for address 050 (YM1=0) of Over/Under Range Continue Subroutine.

Table 8-3. Standard Instrument Checkout (16 of 17)

Step	Instrument Setup and Test Procedure	Test Description and Key Operating Sequence
38	Set Range Calibrator RANGE switch to 5 dBm and adjust Power Meter CAL ADJ control to obtain 5.00 indication on Digital Readout. Then set Power Meter MODE WATT switch to on and Range Calibrator POLARITY switch to REVERSE. Verify that Power Meter Digital Readout indicates −3.16 ± 6.3 mW.	DESCRIPTION — Negative Watt readout capability is provided to enable detection of high noise conditions. This step verifies that capability of the Power Meter to detect and indicate a 28% negative power level. (A negative WATT MODE measurement simulates a high noise condition at the input of the Power Sensor.) KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: **Measurement Subroutine** A-D Converter input voltage at DC test point A3TP4 = −0.316 ± 0.002V Preset counter and branch to Linear Negative-Conversion Subroutine (reference; previously verified). **Linear Negative-Conversion Subroutine** Initiate Linear Negative-Conversion Ramp and count main counter up. Detect YPLS=0 at address 131 (633 ± 126 clock pulses from address 077) and branch to Display and Remote Talk Subroutine.
39	Set Power Meter RANGE HOLD switch to on (in) and Range Calibrator RANGE switch to 10 mW. Verify that Digital Readout indicates 10 ± 2 mW, and record indication.	DESCRIPTION — This step verifies the capability of the Power Meter to indicate a 91% (of max) negative power level. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: **Measurement Subroutine** A-D Converter input voltage at DC test point A3TP4 = 1.000 ± 0.002V. **Linear Negative-Conversion Subroutine** Detect YPLS=0 and branch to Display and Remote Talk Subroutine at address: a. 131 for minimum specified level (reference; verified in previous step). b. 133 for 10.00 mW or greater indication (delay = 2201 ± 200 clock pulses from address 077).

Table 8-3. Standard Instrument Checkout (17 of 17)

Step	Instrument Setup and Test Porcedure	Test Description and Key Operating Sequence
40	Set Range Calibrator RANGE switch to 30 mW and verify that OVER RANGE indication is observed.	DESCRIPTION — This step verifies that the Power Meter will detect and display a negative power level OVER RANGE condition. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except as indicated below: a. A-D Converter input voltage at DC test point A3TP4 is greater than −1.200V. b. Program branches from address 134 of Linear Negative-Conversion Subroutine to Display and Remote Talk Subroutine.
41	Set Range Calibrator RANGE switch back to 10 mW and verify that Digital Readout indication returns to level observed in step 39.	DESCRIPTION — This step verifies the capability of the Power Meter to reset a negative power level OVER RANGE condition when an in-range negative power level is applied. KEY OPERATING SEQUENCE — Program execution and circuit operation previously verified except for LCOR instruction associated with address 131 or 133 (refer to step 39).
42	Rotate Power Meter CAL ADJ control as required to change Digital Readout indication from under 10.00 to over 10.00 or vice versa.	DESCRIPTION — This step verifies the last remaining address branch of the Linear-Negative Conversion Subroutine. KEY OPERATING SEQUENCE — Refer to step 39.
43	Set Range Calibrator POLARITY switch to NORMAL and readjust Power Meter CAL ADJ control to obtain 10.00 mW indication. Then verify Power Meter operation per Performance Tests of Section IV. If any indication is abnormal, adjust Power Meter as specified in Section V. If indication is still abnormal after performing adjustment procedure, refer to Table 8-6 for list of unverified instructions, and to analog circuit troubleshooting information provided on Service Sheets 7 and 8.	

8-64. HP-IB Instrument Checkout

8-65. Test programs for verifying the operation of an HP-IB equipped Power Meter are provided in Figures 8-16 and 8-17. The test program provided in Figure 8-16 is written for use on an HP 9830A Calculator, and the program in Figure 8-17 is written for use on an HP 9820A Calculator. The two programs are functionally identical; their only differences are in the specific programming statements required for each calculator.

The HP-IB Verification Program is also available on disk, for use with the HP 9836A, by ordering part number 00436-10047. A cassette is available for use with the HP 9825A, by ordering HP part number 00436-10007.

8-66. The test programs are designed to check out both the operation of the HP-IB circuitry, and that portion of the Power Meter operating program associated with remote operation. After the program is loaded into the calculator memory, it is executed by pressing the RUN and EXECUTE keys in sequence. If the Power Meter functions properly, the program will pause three times. Each pause will be indicated by a printout directing that the CAL ADJ control be adjusted to obtain a specific front-panel indication. (The first pause also directs that the Power Sensor be connected to the POWER REF OUTPUT.) When the proper indications are obtained for the first two pauses, the program will automatically continue. For the third pause, the operator must press the CONT and EXECUTE keys to restart the program after the CAL ADJ and CAL FACTOR % controls are adjusted to obtain the specified indication. The test program will then cycle to the end and print out TESTS COMPLETE to indicate that the Power Meter is functioning properly.

8-67. If the Power Meter does not function properly for any of the tests contained in the program, the program will halt and print out an error number. Table 8-4 describes the specific problem associated with each error number, the test background, and rationale for the error, and a logical procedure for isolating the error. (Specific programming statements and references contained in Table 8-4 are applicable to the HP 9830A Diagnostic Program only; if an HP 9820A Calculator is used for the checkout of the Power Meter, it will be necessary to convert the programming statements and references to the 9820A equivalents.) The fault isolation procedure, in turn, is written in general terms and assumes an understanding of HP-IB circuit operation and Power Meter operating program execution. For information covering the Power Meter operating program, refer to Figure 8-16, Table 8-3, and Table 8-4. For information covering HP-IB circuit operation, refer to Service Sheet 4.

NOTE

A read byte subroutine is provided at the end of the diagnostic program to facilitate fault isolation. When this subroutine is used, the calculator display is two words behind the HP-IB ROM output (see Service Sheet 4); i.e., when the ROM is outputting word 2, word 1 is in the calculator's I/O register and word 0 is displayed.

```
10 REM 4-01-75 436A HP-IB CHECKS COMBINED RRG
20 REM PROGRAM WILL RUN AFTER ERROR WITH CONT EXECUTE
30 REMOTE LOCAL CHECKS
40 T=E=Z=1
50 FORMAT 3B
60 FORMAT B
70 FORMAT 2B,"T"
80 FORMAT 3B,F9.0
90 GOSUB 2410
100 CMD "?U"
105 OUTPUT (13,60)1024
107 GOSUB 2340
110 CMD "?M5"
120 WAIT 5000
130 IF (STAT13#3) THEN 150
140 GOTO 160
150 GOSUB 2310
160 CMD "?U"
170 OUTPUT (13,60)768;
180 GOSUB 2340
190 CMD "?U-","RC"
200 CMD "?U"
210 OUTPUT (13,60)1024;
220 GOSUB 2340
230 T=T+1
240 E=2
250 GOSUB 2370
260 IF M=67 THEN 280
270 GOTO 290
280 GOSUB 2310
290 IF T=2 THEN 230
300 E=3
310 CMD "?U"
320 OUTPUT (13,60)768;
330 GOSUB 2340
340 CMD "?U-","T"
350 T=T+1
360 GOSUB 2370
370 IF T=4 THEN 340
380 IF M#67 THEN 400
390 GOTO 410
400 GOSUB 2310
410 E=T=4
415 REMOTE ZERO CHECKS
420 CMD "?U-","Z2T"
430 GOSUB 2370
440 IF S#85 THEN 460
450 GOTO 470
460 GOSUB 2310
470 IF E=4.5 THEN 510
480 E=4.5
490 GOTO 420
```

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (1 of 25)

```
510 CMD "?U-","Z1T"
520 T=T+1
530 E=5
540 GOSUB 2370
550 IF T=16 THEN 2310
560 IF ABS(D*10↑8)>1.5 THEN 510
570 CMD "?U-","AT"
580 GOSUB 2370
590 E=T=6
600 IF S#84 THEN 620
610 GOTO 630
620 GOSUB 2310
630 WAIT 10000
640 CMD "?U-","AT"
650 E=7
660 GOSUB 2370
680 IF S#80 THEN 2310
690 Z=Z+1
700 E=8
710 IF Z=5 THEN 730
720 GOTO 740
730 GOSUB 2310
740 CMD "?U-","T"
750 GOSUB 2370
760 IF ABSD<4*10↑(-8) THEN 780
770 GOTO 410
780 REM 436A MODE CHECKS
790 M=64
800 M=M+1
810 FOR I=1 TO 6
820 DATA 49,73,-30,50,74,-20,51,75,-10,52,76,0,53,77,10,57,73,-30
830 READ R,R1,D1
840 CMD "?U-"
850 OUTPUT (13,70)R,M
860 GOSUB 2340
870 E=E+1
880 CMD "?M5"
890 ENTER (13,80)S,R2,M1,D
900 IF R1#R2 THEN 980
910 IF M1#M THEN 980
920 IF M#68 THEN 940
930 IF D#D1 THEN 990
940 NEXT I
950 RESTORE
960 IF M=68 THEN 1040
970 GOTO 800
980 IF M#68 THEN 1000
990 PRINT "DATA IS";D"SHOULD BE";D1
1000 PRINT "MODE PRGM";M,"RECEIVED";M1"RANGE PRGM";R,
1005 PRINT "IS";R2"STATUS";S
1010 GOSUB 2310
1020 PRINT "****"
1030 GOTO 940
```

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (2 of 25)

```
1040 REM DEVICE CLEAR CHECKS
1050 CMD "?U-","5DR"
1060 GOSUB 2410
1070 CMD "?U-","T"
1080 GOSUB 2370
1090 E=33
1100 IF S#80 THEN 1140
1110 IF R#73 THEN 1140
1120 IF M#65 THEN 1140
1130 GOTO 1150
1140 GOSUB 2310
1150 E=34
1160 RESTORE 1190
1170 CMD "?U-","DI
1180 FOR I=1 TO 7
1190 DATA 4,16,21,22,29,52,84
1200 READ V
1210 OUTPUT (13,50)256,V,512;
1220 GOSUB 2340
1230 NEXT I
1240 CMD "?U-","I"
1250 CMD "?M5"
1260 ENTER (13,80)S,R,M,D
1270 IF M#68 THEN 1290
1280 GOTO 1300
1290 GOSUB 2310
1300 GOSUB 2410
1310 E=35
1320 WAIT 200
1330 CMD "?U-","D3I"
1340 GOSUB 2370
1350 IF S#82 THEN 1390
1360 IF R#75 THEN 1390
1370 IF M#68 THEN 1390
1380 GOTO 1400
1390 GOSUB 2310
1400 REM ADDRESS CHECKS
1410 E=36
1420 CMD "?U-","AI"
1430 GOSUB 2370
1440 CMD "?U% ),=<","DI"
1450 CMD "?U-","I"
1460 GOSUB 2370
1470 IF M#65 THEN 1490
1480 GOTO 1500
1490 GOSUB 2310
1500 REM CHECKS FAST/SLOW
1510 GOSUB 2410
1520 E=37
1530 CMD "?U-","A2I"
1540 GOSUB 2370
1550 CMD "?U-","T"
```

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (3 of 25)

```
1560 CMD "?M5"
1570 WAIT 200
1580 IF (STAT13#2) THEN 1600
1590 GOTO 1610
1600 GOSUB 2310
1610 ENTER (13,80)S,R,M,D
1620 E=38
1630 CMD "?U-","I"
1640 CMD "?M5"
1650 WAIT 200
1660 IF (STAT13#3) THEN 1680
1670 GOTO 1700
1680 GOSUB 2310
1700 REM 436A POWER ON CHECKS WITH 8481 MOUNT 2-10-75
1710 T=1
1720 CMD "?U-","3R+"
1730 PRINT "CONNECT MOUNT TO POWER REF, POWER REF ON"
1740 PRINT "SET CAL ADJ FOR .799MW"
1750 PRINT
1760 E=39
1770 T=T+1
1780 IF T=301 THEN 2310
1790 GOSUB 2370
1800 DISP "DATA=";D*10↑6
1810 IF D#0.000799 THEN 1770
1820 PRINT ".799 MW RECEIVED"
1830 PRINT "SET CAL ADJ FOR .866 MW"
1840 PRINT
1850 T=1
1860 E=40
1870 T=T+1
1880 IF T=301 THEN 2310
1890 GOSUB 2370
1900 DISP "DATA=";D*10↑6
1910 IF D#0.000866 THEN 1870
1920 PRINT ".866MW RECEIVED"
1930 PRINT
1940 CMD "?"
1950 PRINT "ADJ 436A DISPLAY FOR 1.000 MW +-.001"
1960 PRINT "THEN SET CAL FACTOR TO 85%"
1970 PRINT "CONT EXECUTE"
1980 PRINT
1990 STOP
2000 CMD "?U-","-"
2010 GOSUB 2410
2020 E=41
2030 CMD "?U-","T"
2040 GOSUB 2370
2050 IF 0.000997<D<0.001003 THEN 2070
2060 GOTO 2080
2070 GOSUB 2310
2080 RESTORE 2090
```

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (4 of 25)

```
2090 DATA 81,53,65,83,53,68,82,50,65
2100 READ S1,R,M
2110 E=E+1
2120 CMD "?U-"
2130 OUTPUT (13,70)R,M
2140 GOSUB 2340
2150 GOSUB 2370
2160 IF S#S1 THEN 2180
2170 GOTO 2190
2180 GOSUB 2310
2190 IF E#44 THEN 2100
2200 CMD "?U-","A3-T"
2210 E=45
2220 GOSUB 2370
2230 IF 0.001168<D<0.001184 THEN 2250
2240 GOTO 2260
2250 GOSUB 2310
2260 CMD "?U"
2270 OUTPUT (13,60)1024;
2280 OUTPUT (13,60)768;
2290 PRINT "TESTS COMPLETE"
2300 STOP
2310 PRINT "ERROR #";E
2320 STOP
2330 RETURN
2340 REM ADDS PRINT FOR TRACE
2350 DISP "RUNNING"
2360 RETURN
2370 REM ENTER DATA
2380 CMD "?M5"
2390 ENTER (13,80)S,R,M,D
2400 RETURN
2410 REM DEV CLR
2420 CMD "?U"
2430 OUTPUT (13,50)256,20,512;
2440 GOSUB 2340
2450 RETURN
2460 END
5000 CMD "?U-","R"
5010 CMD "?M5"
5020 A=RBYTE13
5030 PRINT A
5040 GOTO 5020
5050 END
```

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (5 of 25)

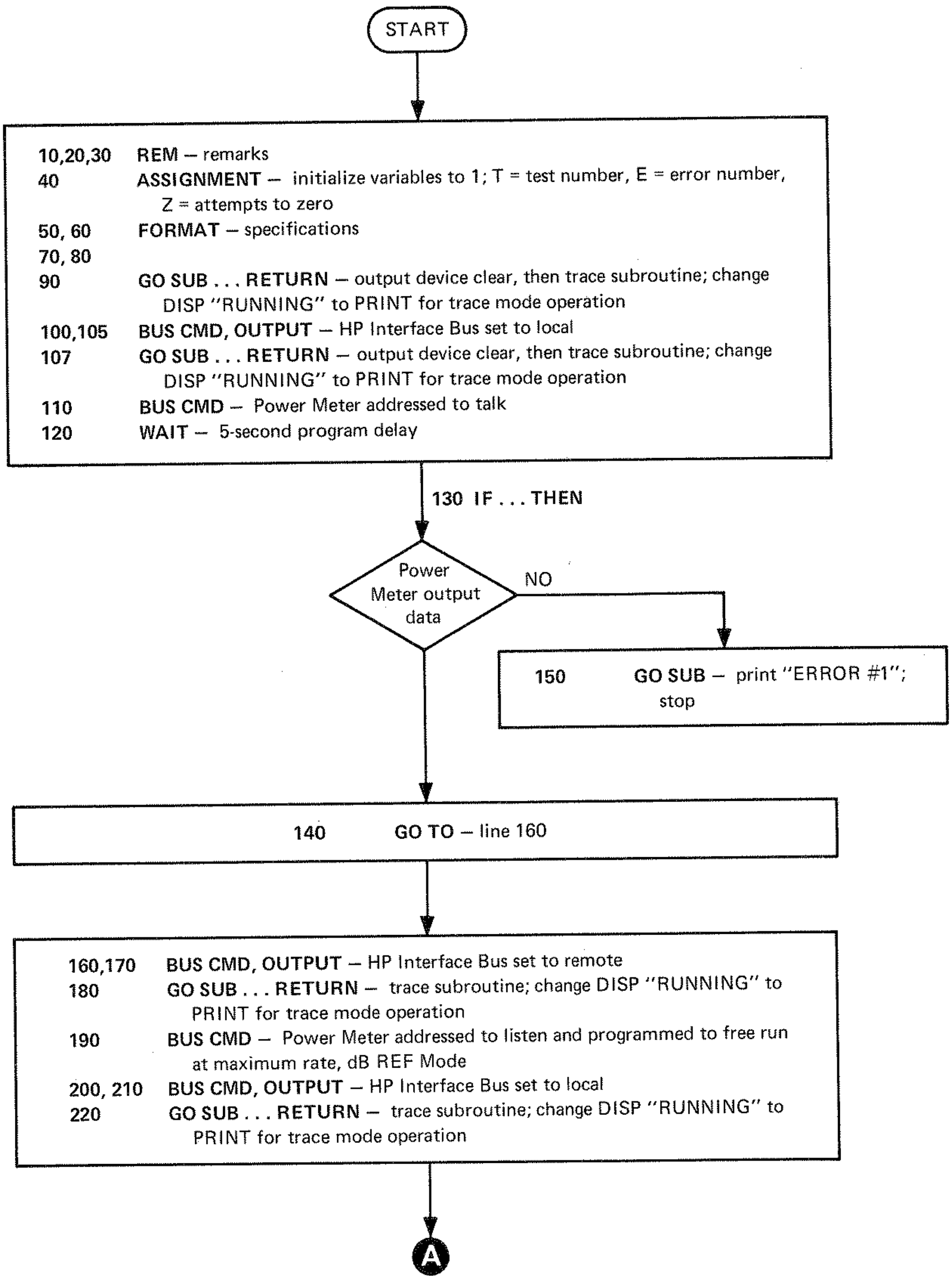

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (6 of 25)

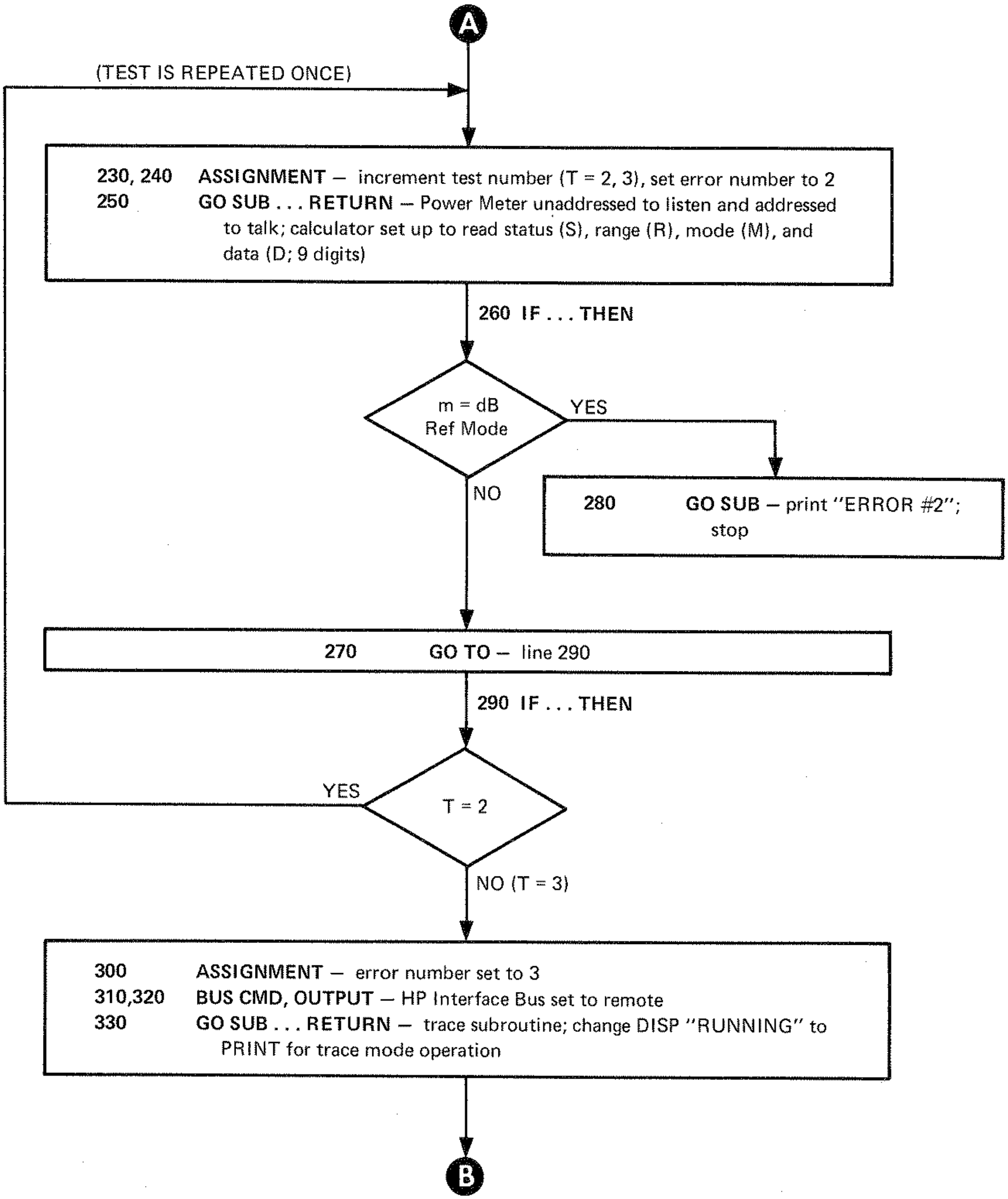

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (7 of 25)

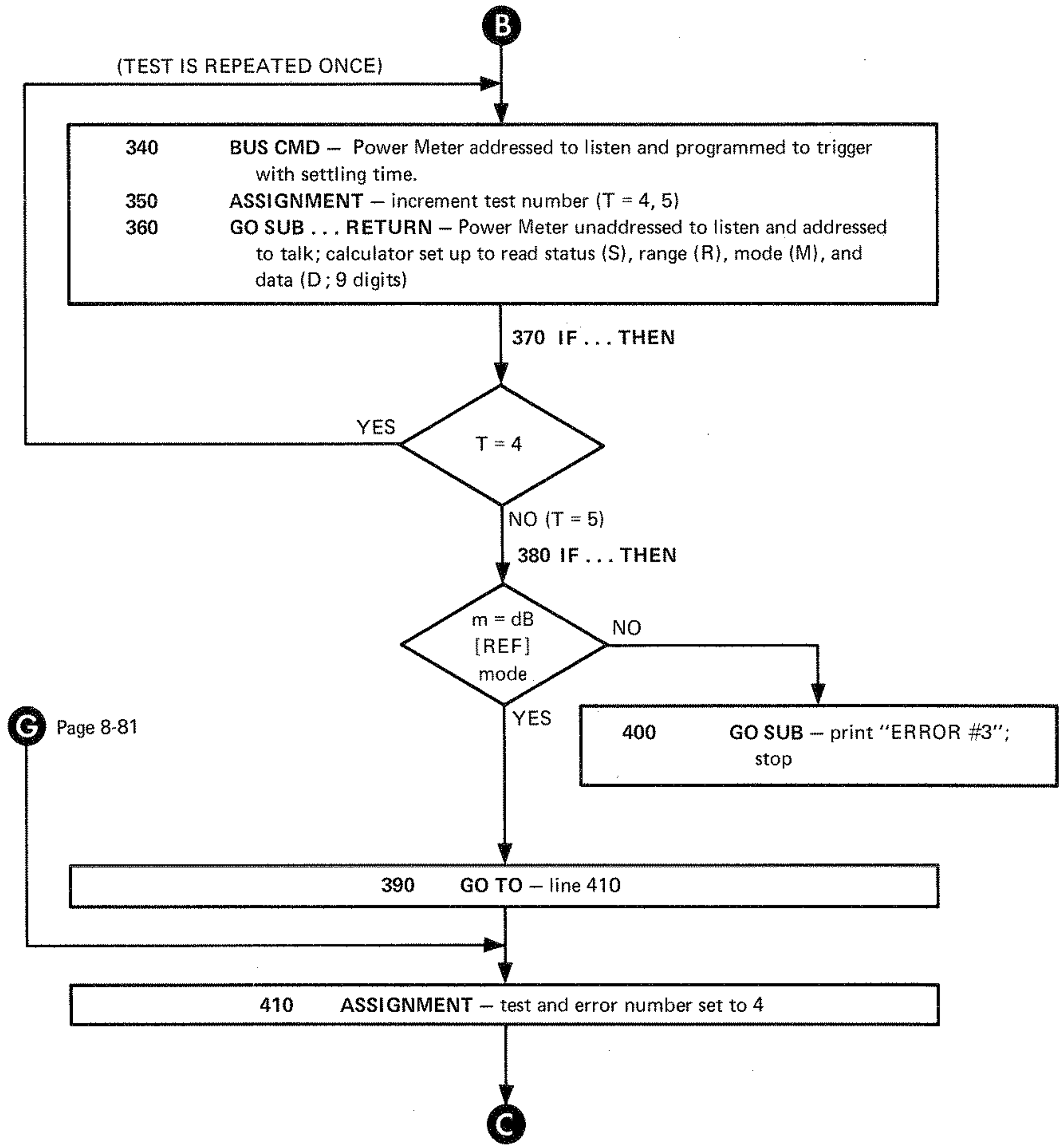

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (8 of 25)

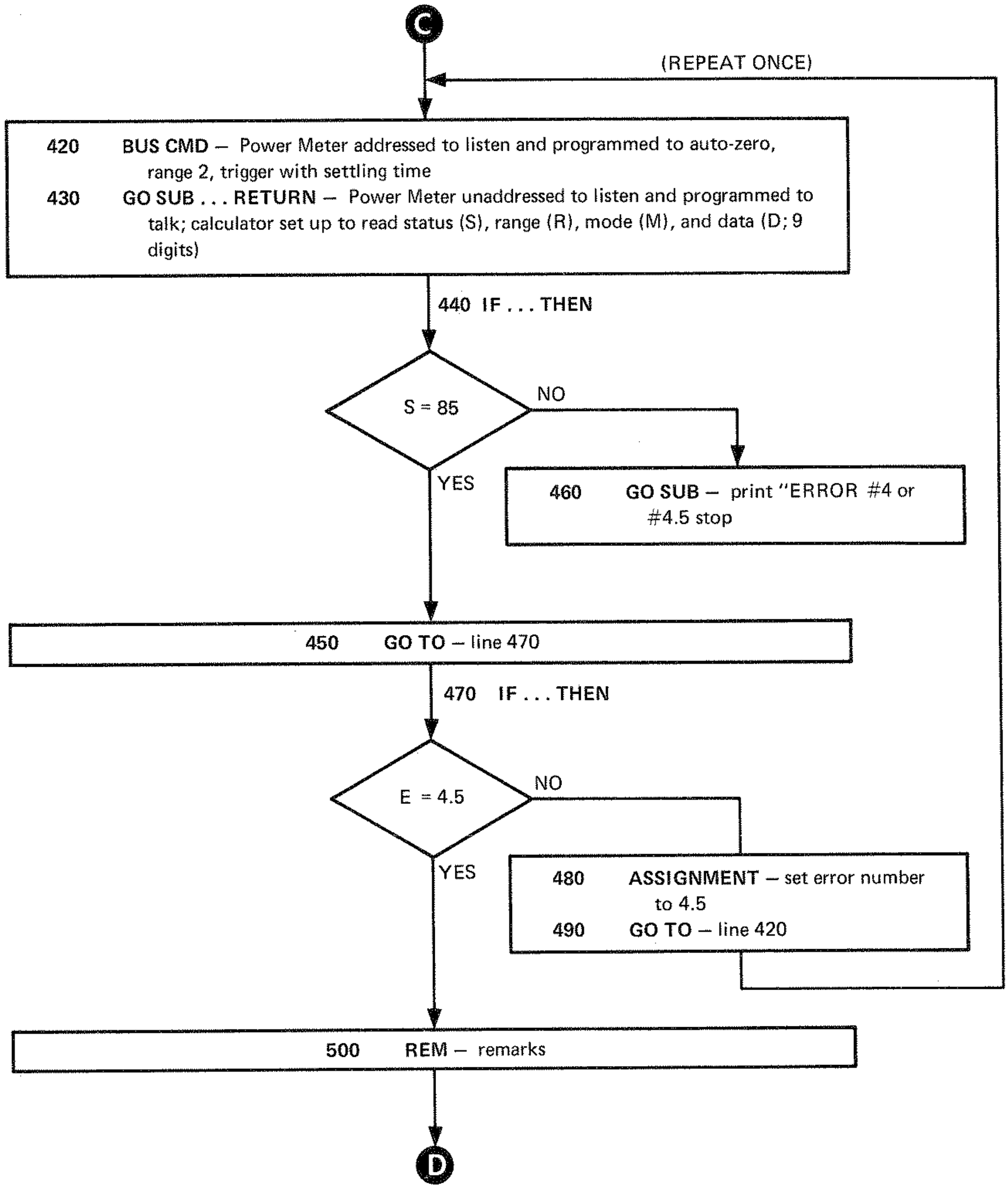

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator)(9 of 25)

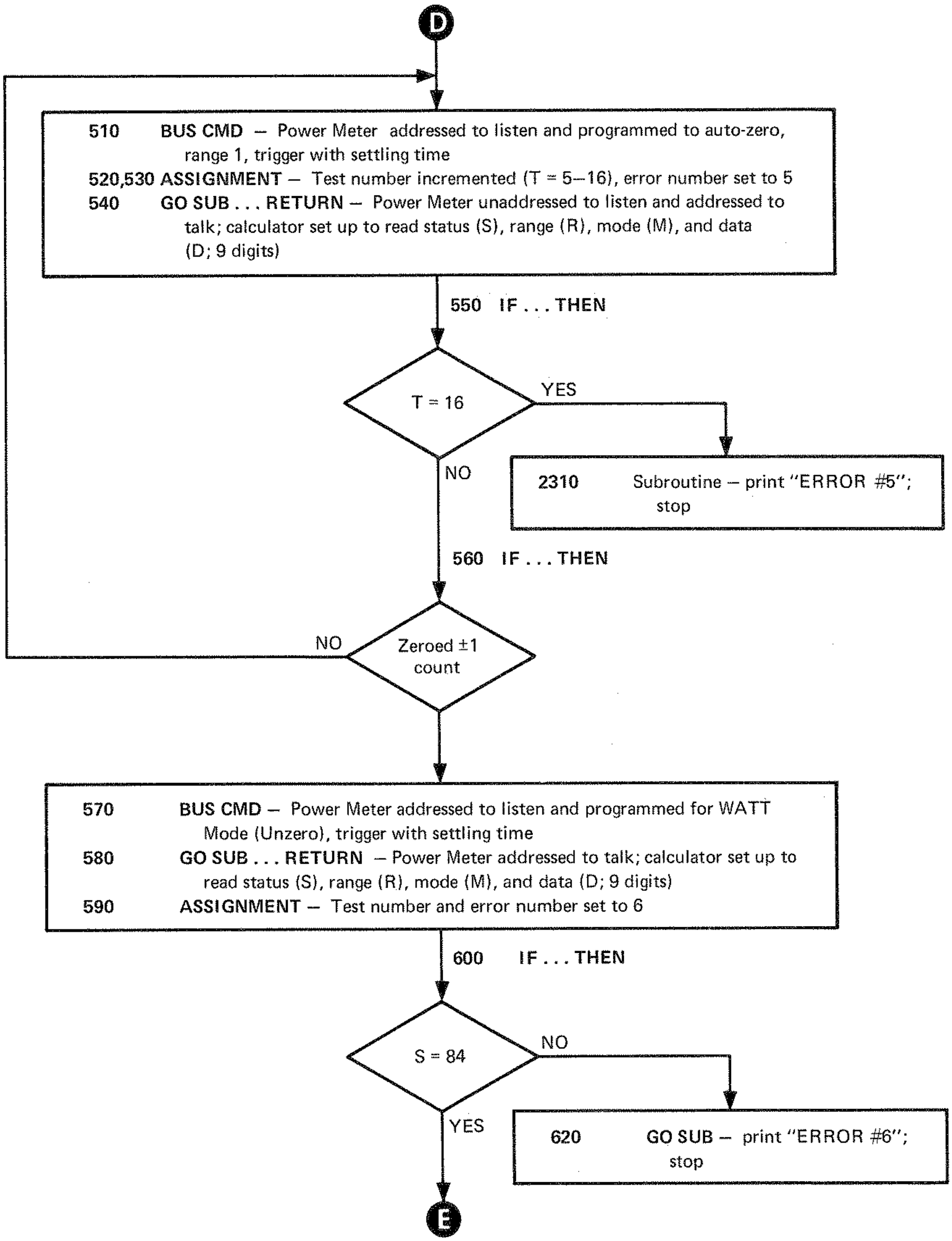

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (10 of 25)

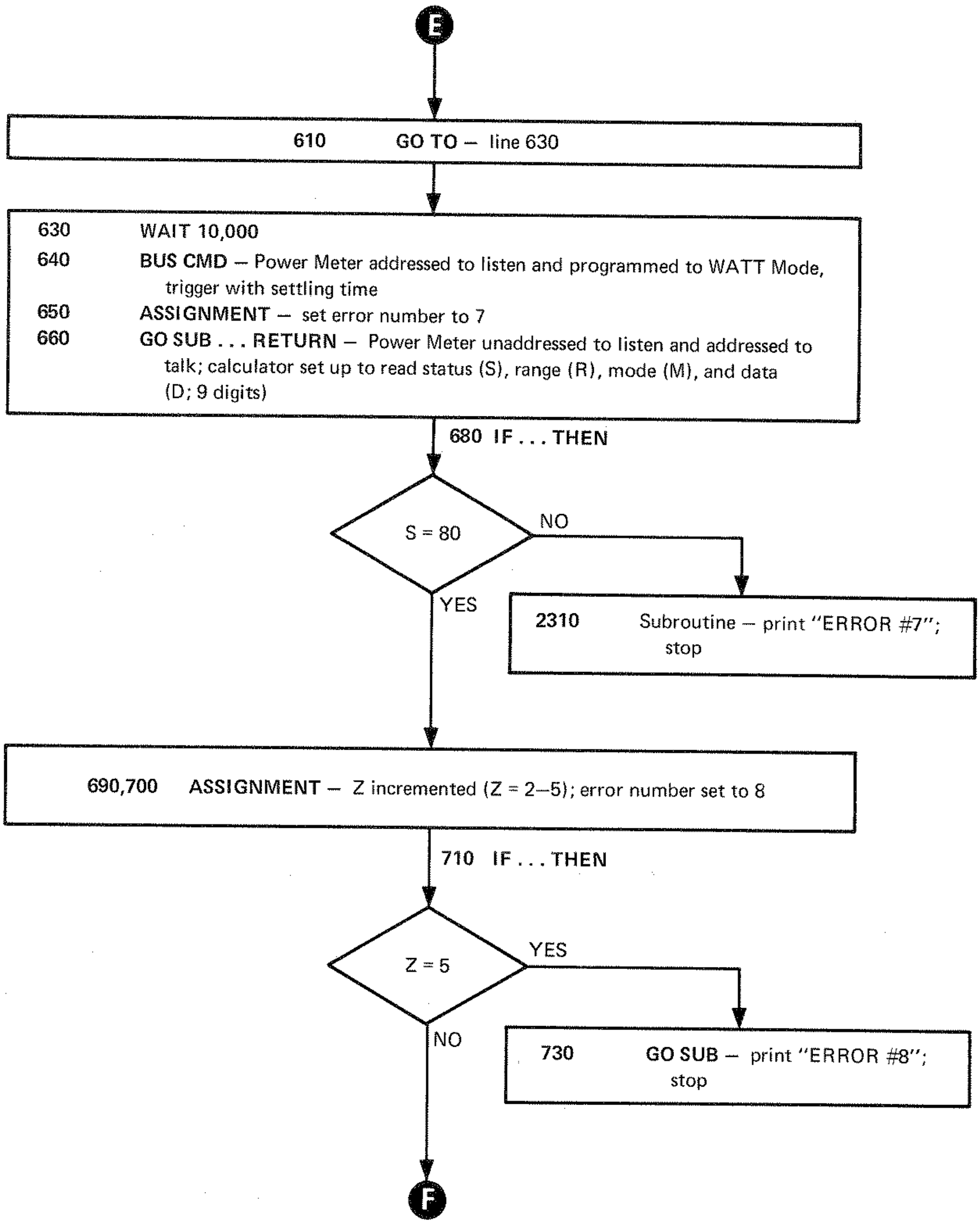

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator)(11 of 25)

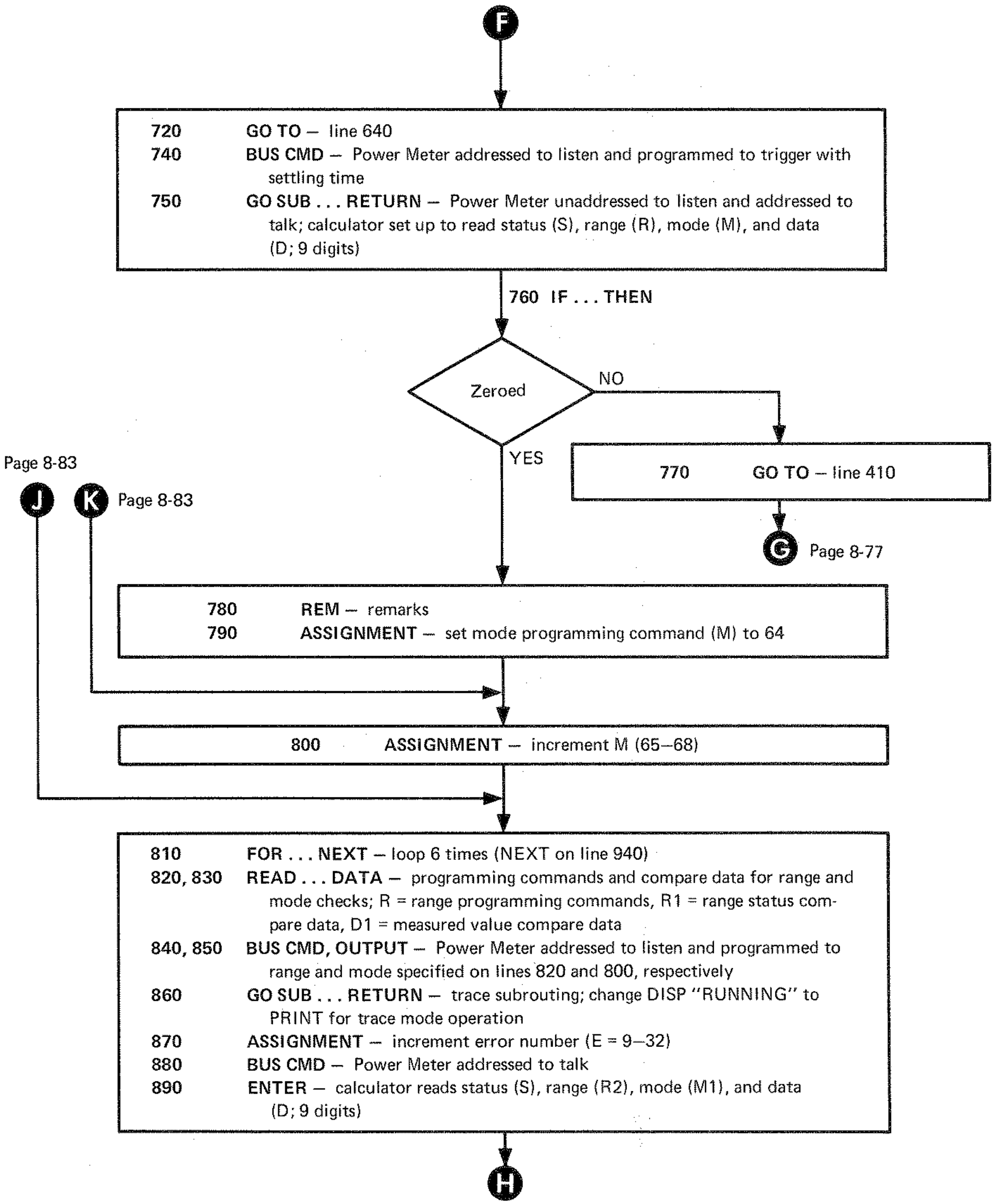

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (12 of 25)

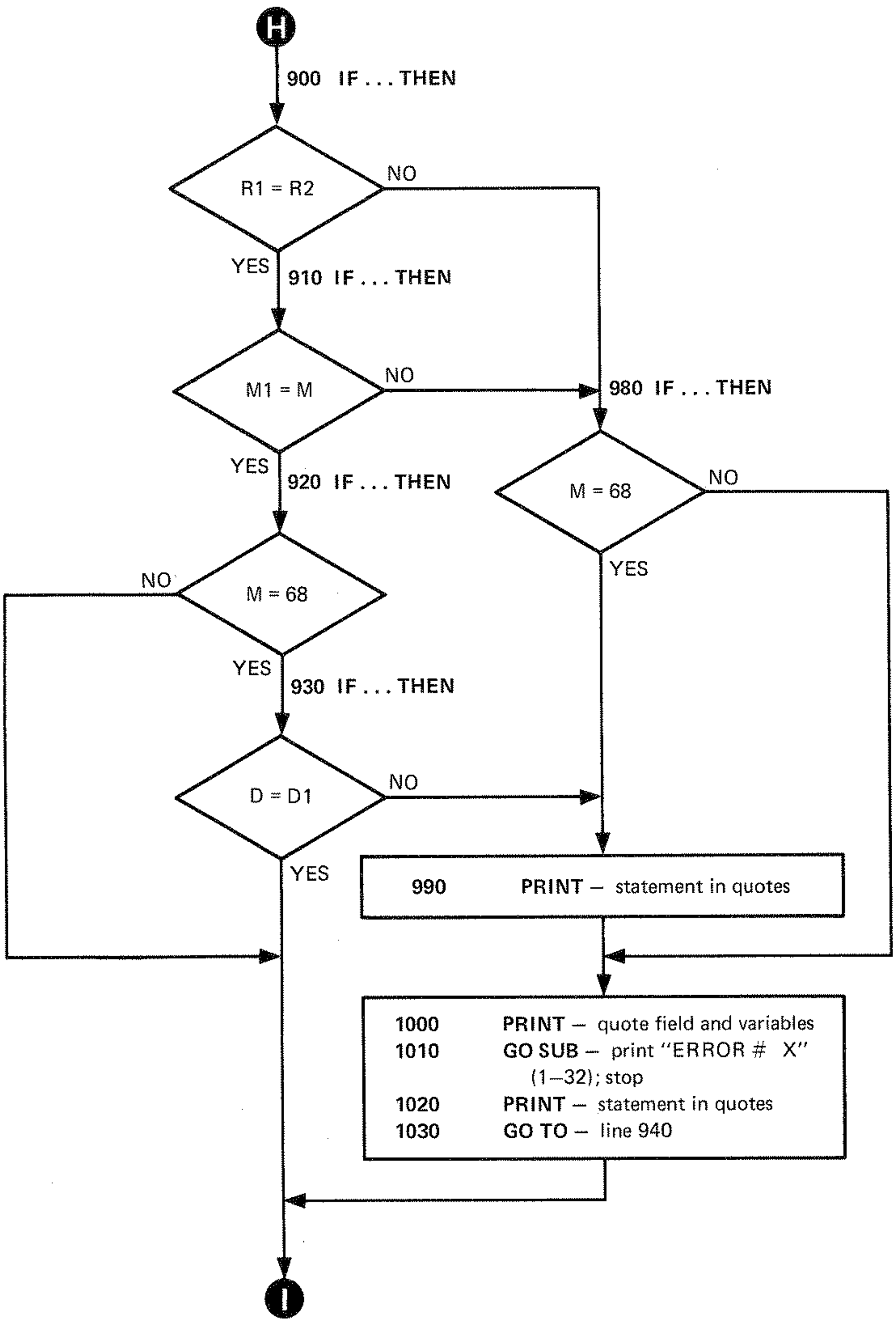

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (13 of 25)

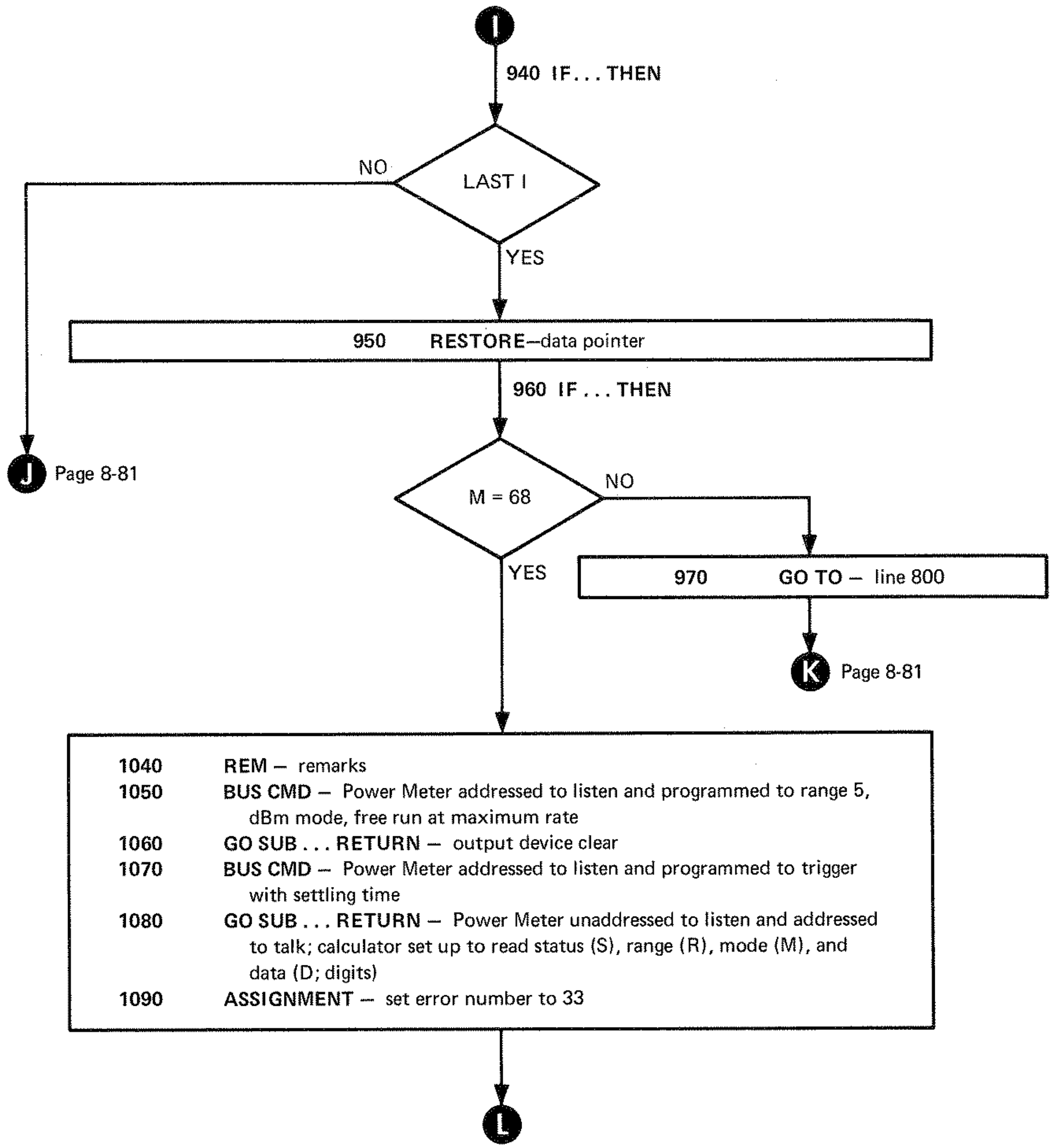

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (14 of 25)

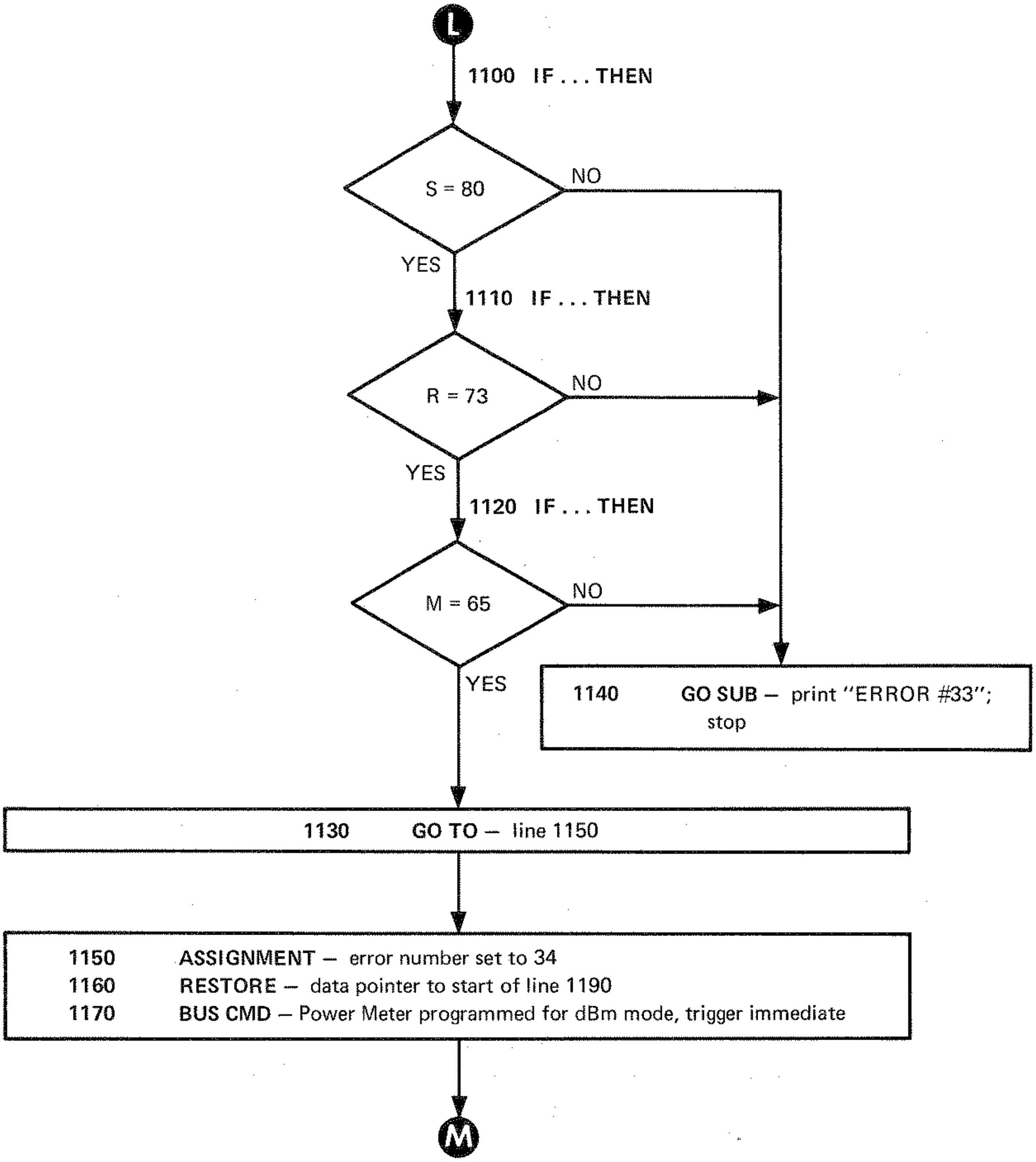

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (15 of 25)

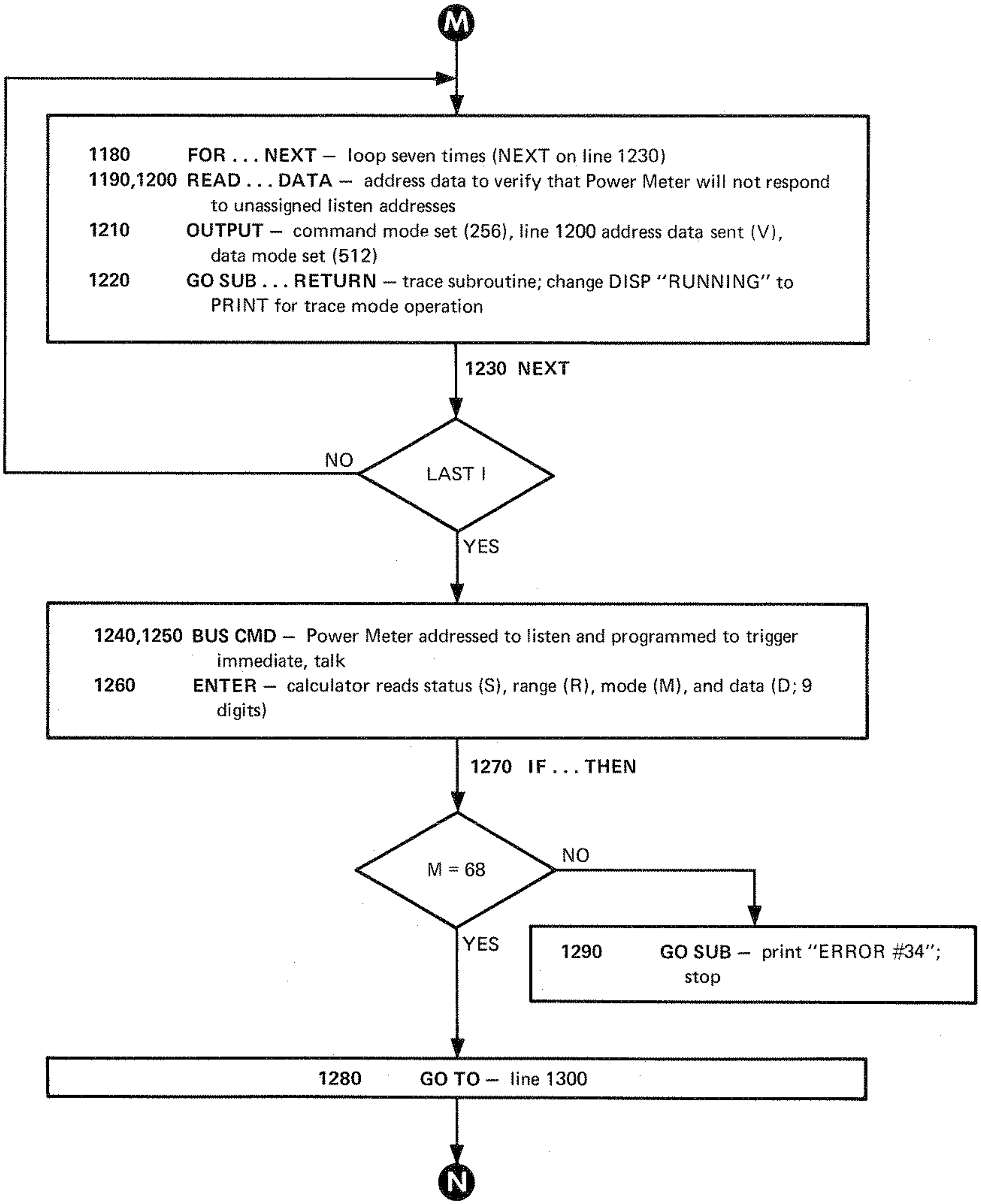

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (16 of 25)

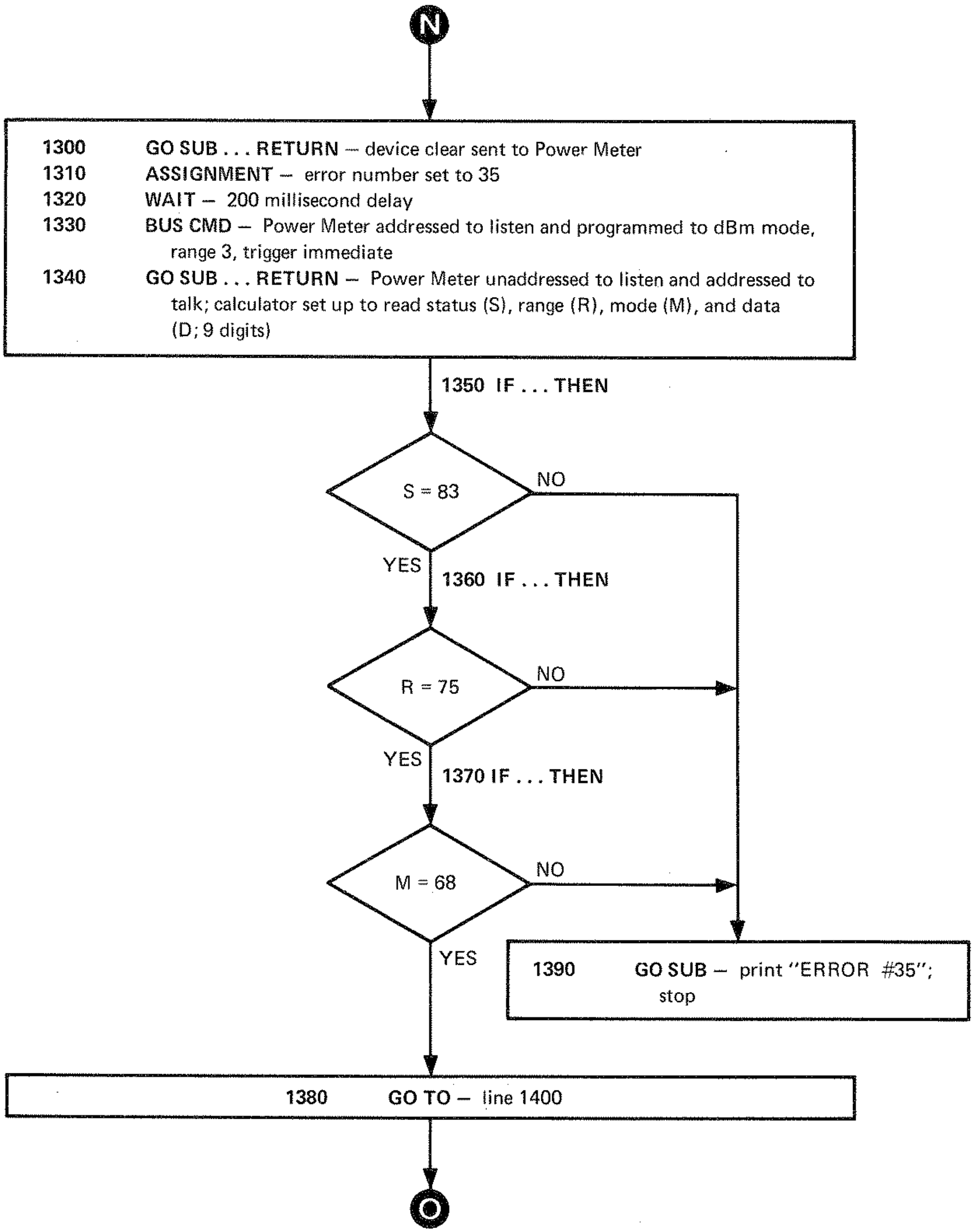

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (17 of 25)

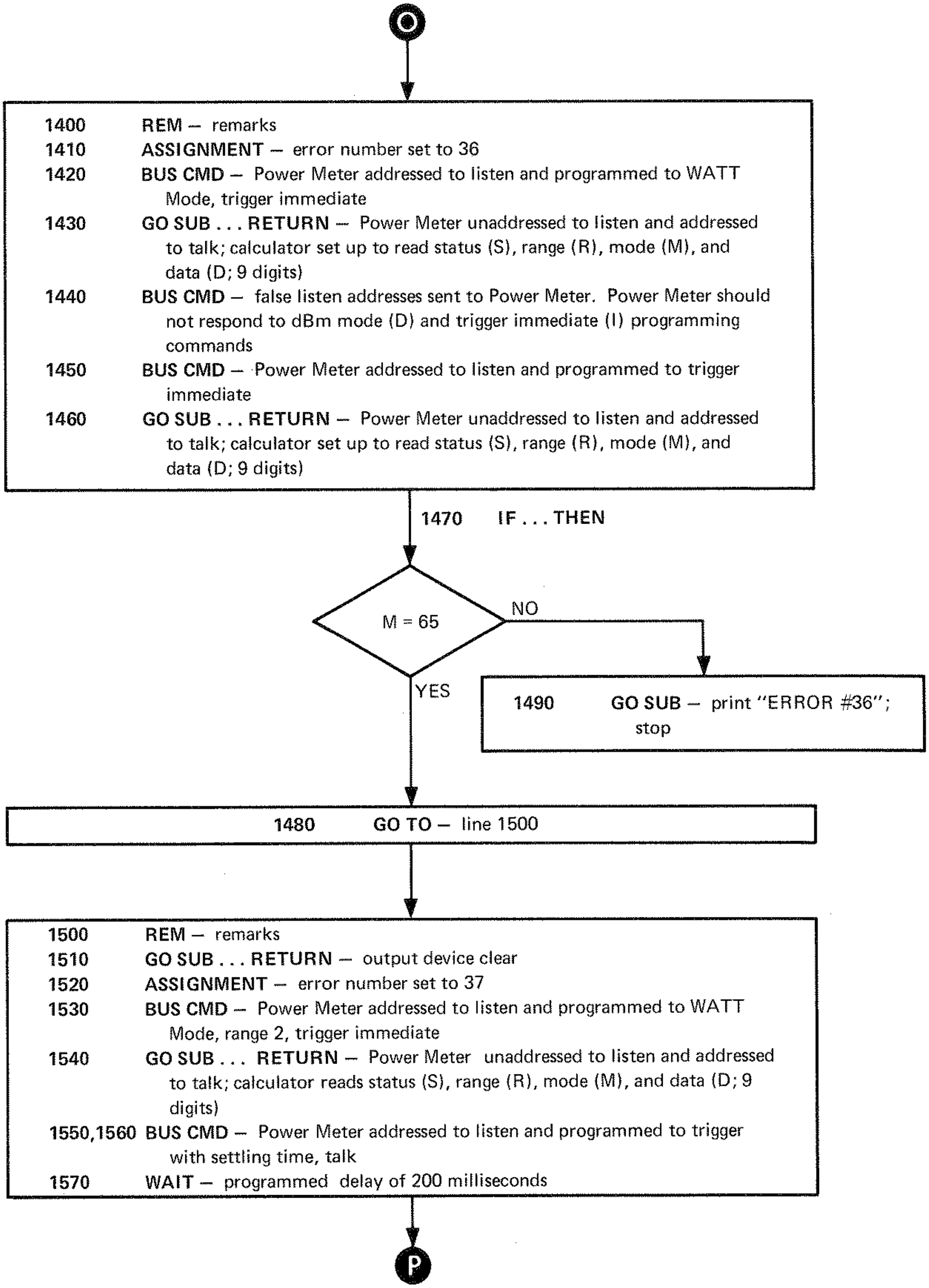

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (18 of 25)

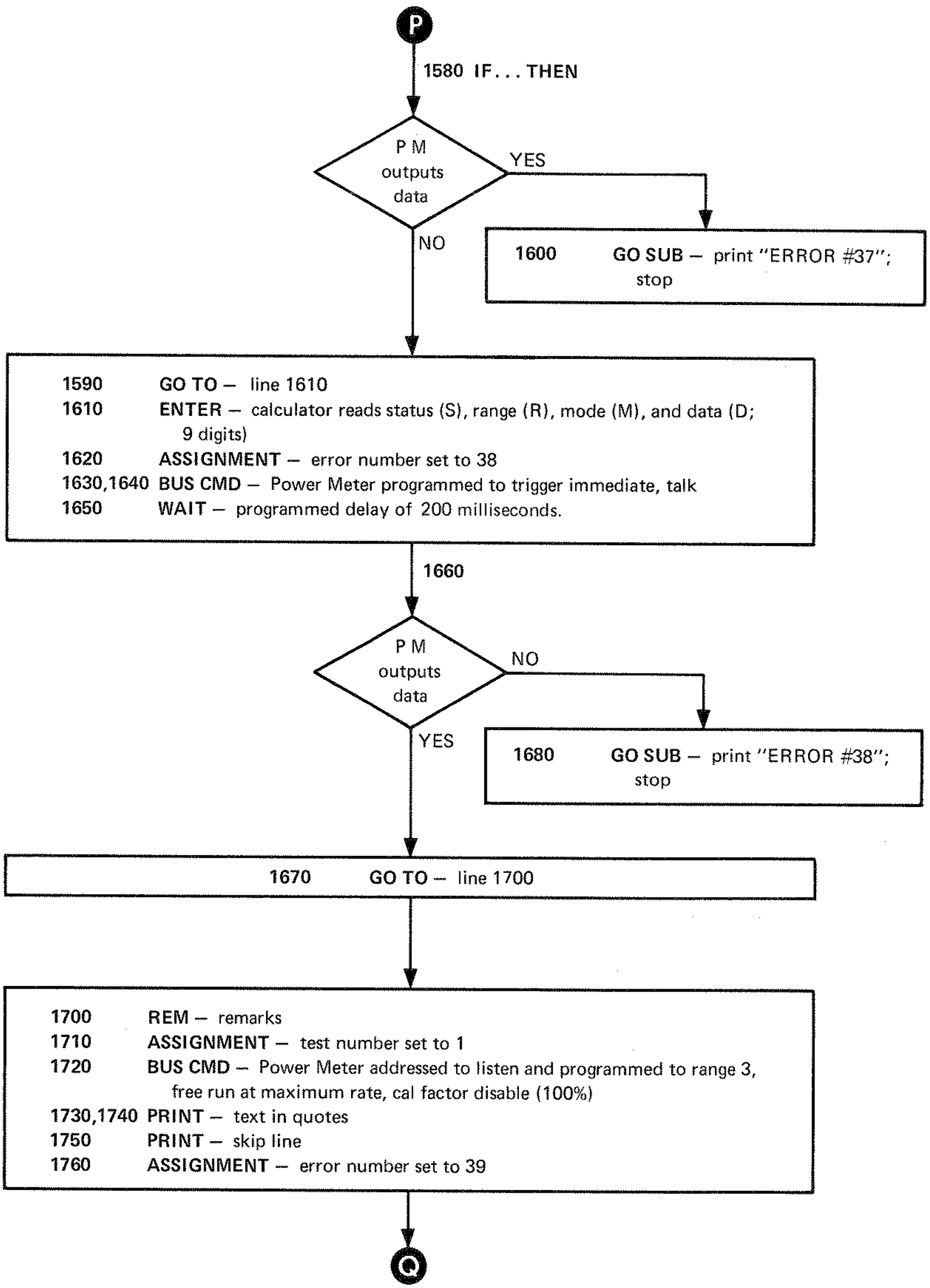

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (19 of 25)

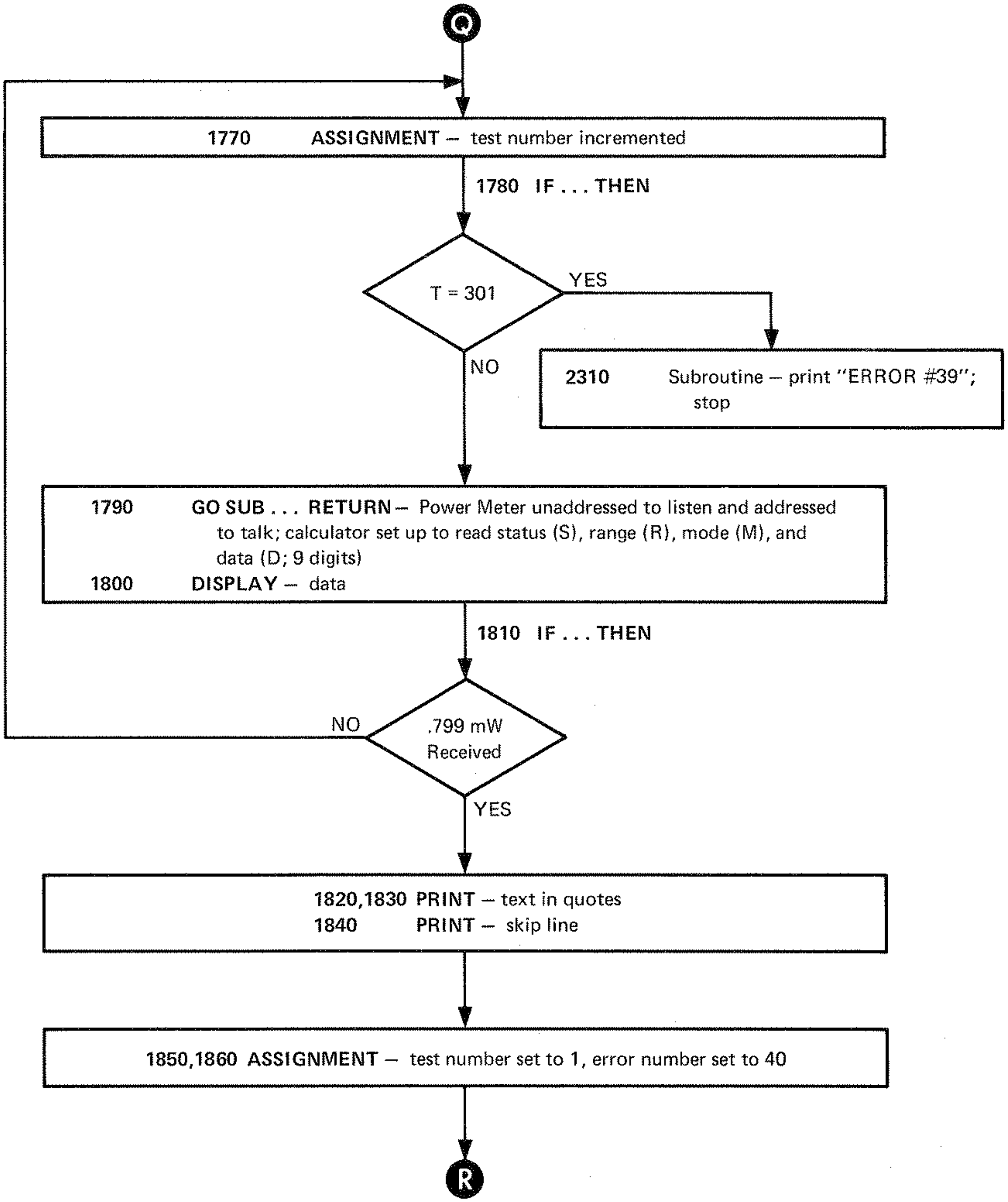

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (20 of 25)

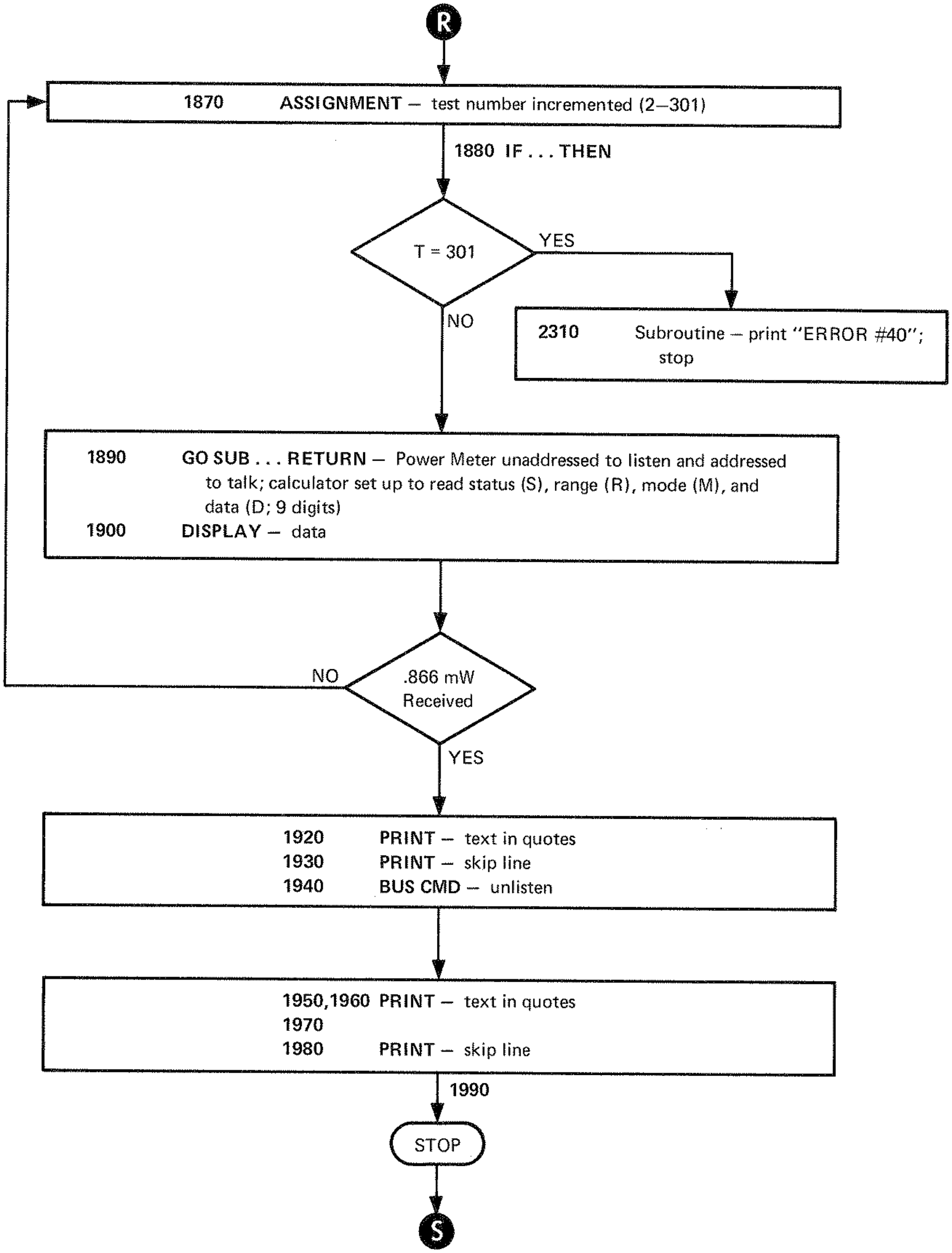

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (21 of 25)

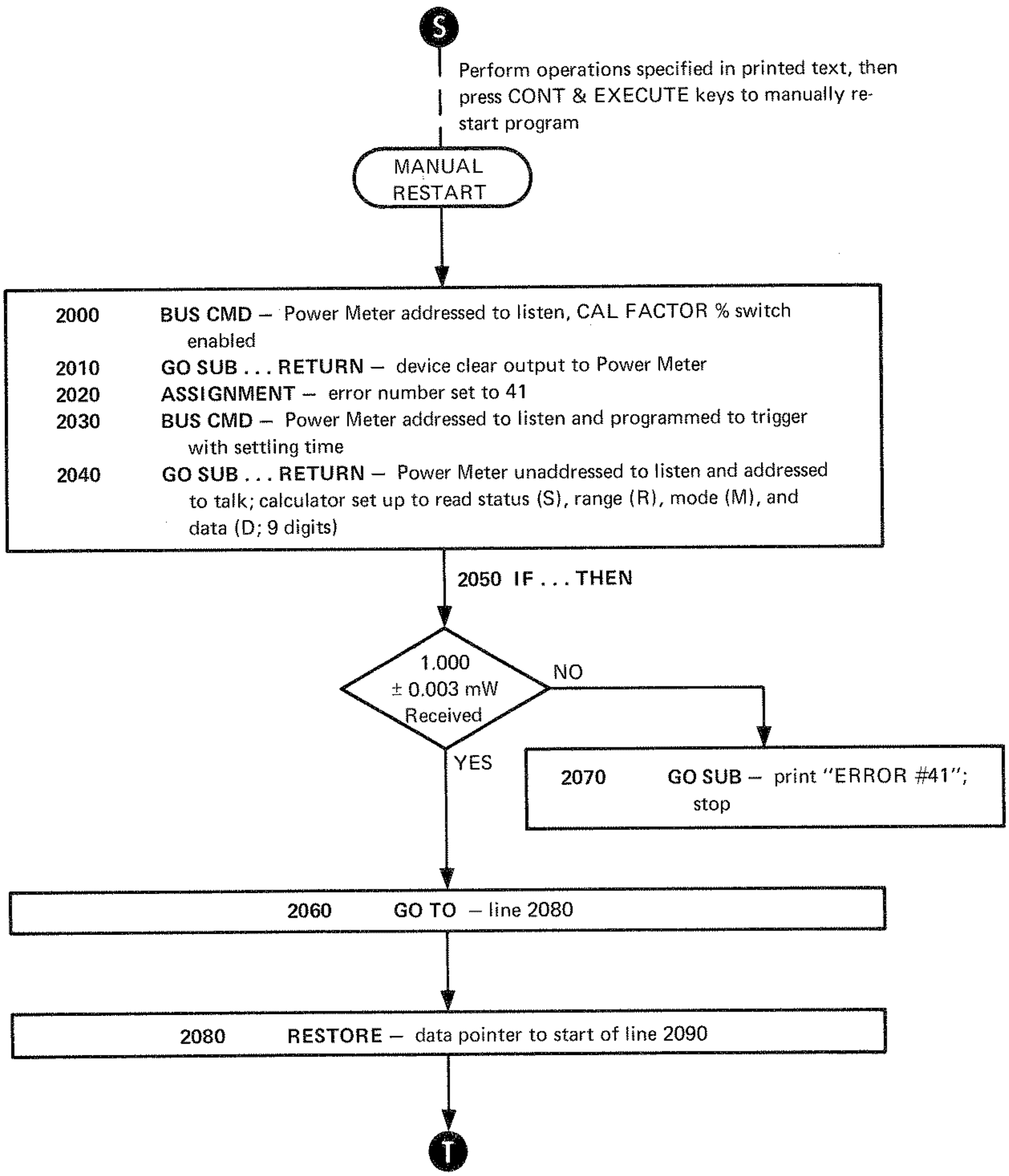

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (22 of 25)

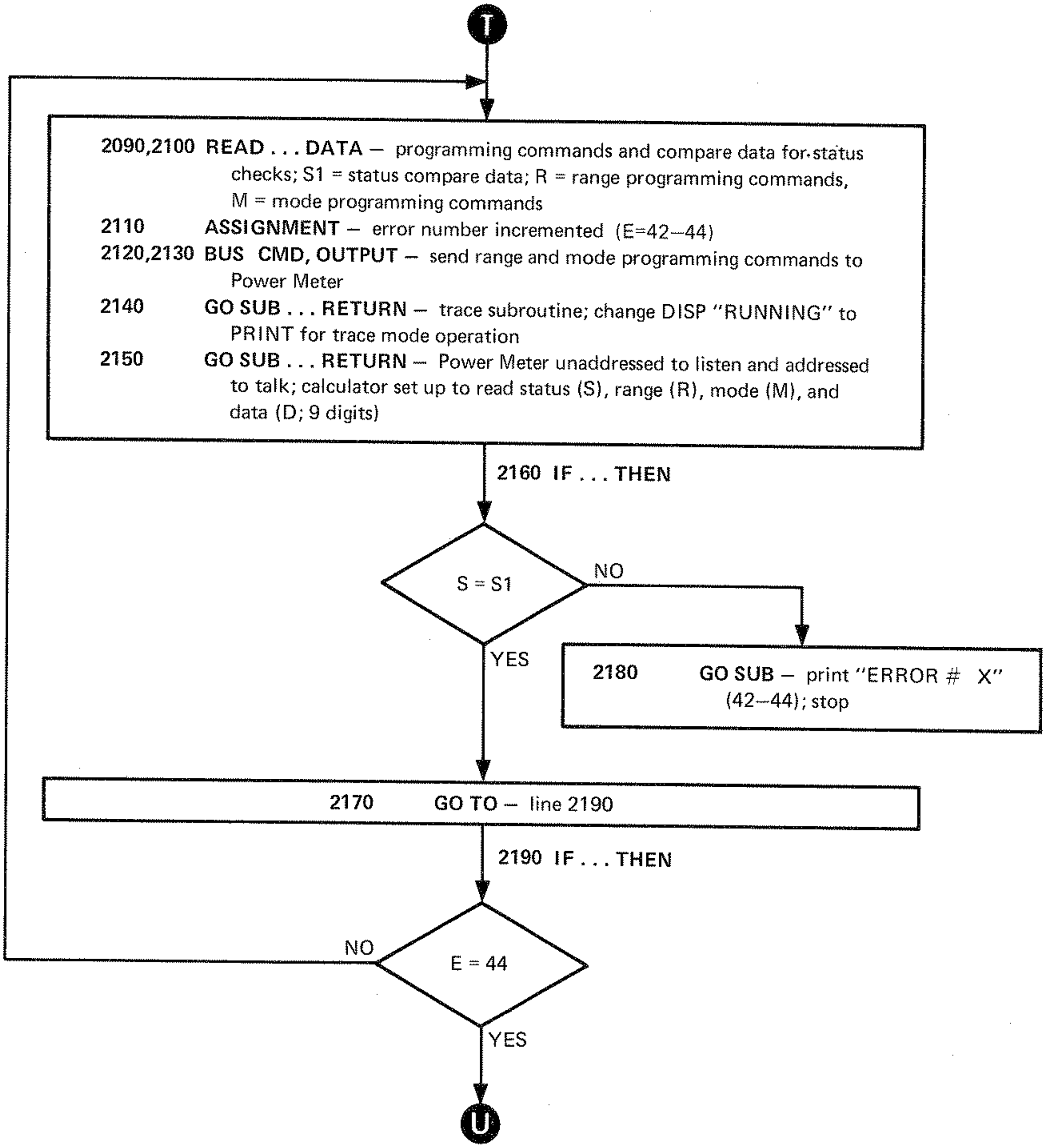

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (23 of 25)

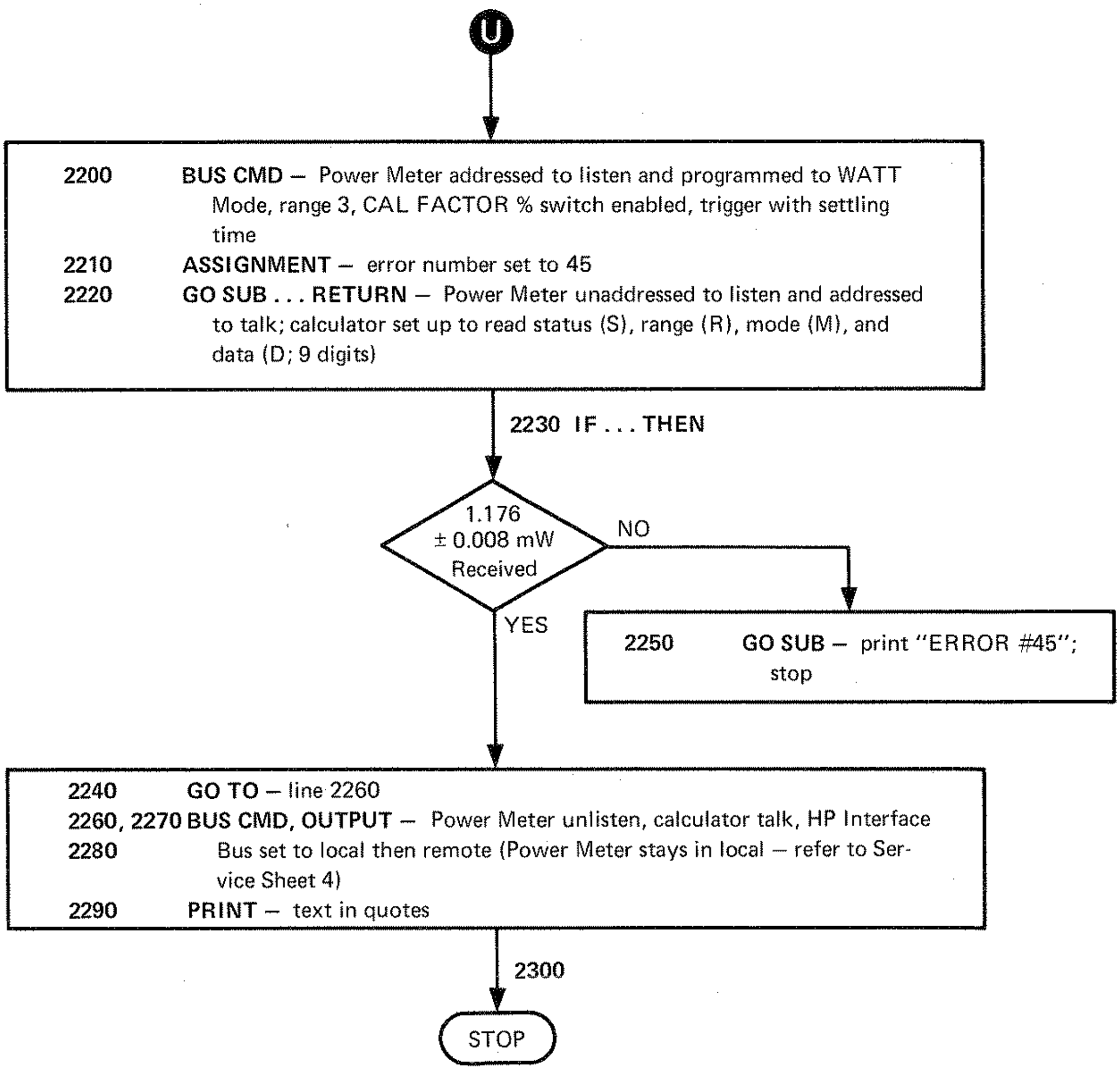

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (24 of 25)

Print Error Subroutine

2310	**PRINT** – error number	
2320	**STOP** – (press CONT EXECUTE to restart program at line 2330 or RUN EXECUTE to restart program at line 10). (Line 2320 may be eliminated to run listing all Errors).	
2330	**RETURN** – to line following GO SUB branch to subroutine	

Trace Subroutine

2340	**REM** – Adds PRINT for TRACE
2350	**DISPLAY** – "RUNNING"
2360	**RETURN** – to line following GO SUB branch to subroutine

Enter Data Subroutine

2370	**REM** – enter data
2380	**BUS CMD** – Power Meter programmed to talk, calculator to listen
2390	**ENTER** – calculator set up to read status (S), range (R), mode (M), and data (D; 9 digits)
2400	**RETURN** – to line following GO SUB branch to subroutine

Device Clear Subroutine

2410	**REM** – DEV CLR
2420	**BUS CMD** – Power Meter unlistening calculator talk
2430	**OUTPUT** – Set HP Interface Bus to command mode, output device clear, then set HP Interface Bus to data mode
2440	**GO SUB** – trace subroutine

2450	**RETURN**–to line following GO SUB reference to subroutine
2460	**END**

Figure 8-16. HP-IB Verification Program (HP 9830A Calculator) (25 of 25)

```
0:
CMD "[illegible]"⊢
1:
CMD "?U-","R";
CMD "?M5"⊢
2:
GSB "WAIT1"⊢
3:
1→R1→R2→R3⊢
4:
IF RDS 13≠3;GTO
"ERROR"⊢
5:
CMD "?U"⊢
6:
FMT Y3,Z;WRT 13⊢
7:
CMD "?U-","RC"⊢
8:
CMD "?U"⊢
9:
FMT Y4,Z;WRT 13⊢
10:
"TEST1";R1+1→R1;
2→R2⊢
11:
CMD "?M5"⊢
12:
GSB "RDB"⊢
13:
IF C=67;GTO "ERR
OR"⊢
14:
IF R1=2;GTO "TES
T1"⊢
15:
3→R2;CMD "?U-";
FMT Y3,Z;WRT 13⊢
16:
"TEST2";CMD "?U-
","T","?M5"⊢
17:
R1+1→R1⊢
18:
GSB "RDB"⊢
19:
IF R1=4;GTO "TES
T2"⊢
20:
IF C≠67;GTO "ERR
OR"⊢
21:
4→R1→R2⊢
22:
"TEST3";CMD "?U-
","Z2T","?M5"⊢
23:
GSB "RDB"⊢
24:
IF A≠85;GTO "ERR
OR"⊢
25:
"TEST4";CMD "?U-
","Z1T","?M5"⊢
26:
R1+1→R1;5→R2⊢
27:
GSB "RDB"⊢
28:
IF R1=16;GTO "ER
ROR"⊢
29:
IF AB(R7*1000000
00)>1.5;GTO "TES
T4"⊢
30:
"TEST5";CMD "?U-
","AT","?M5"⊢
31:
GSB "RDB"⊢
32:
6→R2→R1⊢
33:
IF A≠84;GTO "ERR
OR"⊢
34:
"TEST6";CMD "?U-
","AT"⊢
35:
R1+1→R1⊢
36:
CMD "?M5"⊢
37:
7→R2⊢
38:
GSB "RDB"⊢
39:
IF R1=17;GTO "ER
ROR"⊢
40:
IF A≠80;GTO "TES
T6"⊢
41:
"TEST7";R3+1→R3;
```

Figure 8-17. HP-IB Verification Program (HP 9820A Calculator) (1 of 4)

```
8→R2⊢
42:
IF R3≠5;GTO "ERR
OR"⊢
43:
"TEST8";CMD "?U-
","T","?M5"⊢
44:
GSB "RDB"⊢
45:
IF X≤4*0.0000000
1;GTO 47⊢
46:
GTO "TEST4"⊢
47:
PRT "MODE CHECKS
"⊢
48:
48→R5;2→R2⊢
49:
CMD "▓"⊢
50:
64→R6;0→R8;R5+1→
R5⊢
51:
CMD "?U-";FXD 0.
2;WTB 13,R5;FMT
"T";WRT 13⊢
52:
R6+1→R6;R8+1→R8⊢
53:
CMD "?U-";FMT
FXD 0.2;WTB 13,R
6;FMT "T";WRT 13
;FMT Y2,Z;WRT 13
⊢
54:
CMD "?M5"⊢
55:
GSB "RDB"⊢
56:
IF R6≠C;GTO "ERR
OR"⊢
57:
IF R8≠4;GTO 52⊢
58:
IF B≠77;GTO 49⊢
59:
PRT "DEVICE CLEA
R"⊢
60:
PRT "CHECKS"⊢
61:
CMD "?U-","5DR"⊢
62:
CMD "▓"⊢
63:
CMD "?U-","T","?
M5"⊢
64:
33→R2⊢
65:
GSB "RDB"⊢
66:
IF A≠80;GTO "ERR
OR"⊢
67:
IF B≠73;GTO "ERR
OR"⊢
68:
IF C≠65;GTO "ERR
OR"⊢
69:
34→R2⊢
70:
CMD "?U-","DI"⊢
71:
CMD "G"⊢
72:
CMD "?M5"⊢
73:
GSB "RDB"⊢
74:
IF C≠68;GTO "ERR
OR"⊢
75:
35→R2⊢
76:
CMD "▓"⊢
77:
CMD "?U-","D3I",
"?M5"⊢
78:
GSB "RDB"⊢
79:
IF A≠83;GTO "ERR
OR"⊢
80:
IF B≠75;GTO "ERR
OR"⊢
81:
```

Figure 8-17. HP-IB Verification Program (HP 9820A Calculator) (2 of 4)

```
IF C≠68;GTO "ERR
OR"├
82:
PRT "ADDRESS CHE
CKS"├
83:
36→R2├
84:
CMD "?U-","5AI",
"?M5"├
85:
GSB "RDB"├
86:
CMD "?U%)=/","DI
"├
87:
CMD "?U-","I","?
M5"├
88:
GSB "RDB"├
89:
IF C≠65;GTO "ERR
OR"├
90:
PRT "TRIGGER CHE
CKS"├
91:
PRT "FAST/SLOW"├
92:
CMD "[illegible]"├
93:
37→R2├
94:
CMD "?U-","A2I",
"?M5"├
95:
GSB "RDB"├
96:
CMD "?U-","T","?
M5"├
97:
GSB "WAIT2"├
98:
IF RDS 13≠2;GTO
"ERROR"├
99:
CMD "?M5"├
100:
GSB "RDB"├
101:
38→R2├
102:
CMD "?U-","I","?
M5"├
103:
GSB "WAIT2"├
104:
IF RDS 13≠3;GTO
"ERROR"├
105:
PRT "436 POWER "
├
106:
PRT "CONNECTED";
1→R8├
107:
CMD "?U-","3R+"├
108:
PRT "CONNECT SEN
SOR "├
109:
PRT "POWER REF O
N"├
110:
PRT "SET CAL ADJ
 FOR"├
111:
PRT ".799MW"├
112:
39→R2;R8+1→R8├
113:
IF R8=301;GTO "E
RROR"├
114:
CMD "?M5"├
115:
FMT *;RED 13,X├
116:
DSP "DATA=",X├
117:
IF X≠0.000799;
GTO 114├
118:
PRT ".799MW RECE
IVED"├
119:
PRT "SET CAL ADJ
 .866MW"├
120:
40→R2;1→R8├
121:
R8+1→R8├
122:
IF R8=301;GTO "E
```

Figure 8-17. HP-IB Verification Program (HP 9820A Calculator) (3 of 4)

```
RROR"⊦
123:
CMD "?M5"⊦
124:
FMT *;RED 13,X⊦
135:
DSP "DATA =",X⊦
126:
IF X≠0.000866;
GTO 123⊦
127:
PRT ".866 MW REC
EIVED"⊦
128:
CMD "?"⊦
129:
PRT "ADJ 436A FO
R"⊦
130:
PRT "1.000MW"⊦
131:
PRT "SET CAL FAC
TOR"⊦
132:
PRT "TO 85"⊦
133:
STP ⊦
134:
CMD "?U-","-T"⊦
135:
CMD "Z"⊦
136:
41→R2⊦
137:
CMD "?U-","T","?
M5"⊦
138:
GSB "RDB"⊦
139:
IF X>0.001003;
GTO "ERROR"⊦
140:
IF X≤0.000997;
GTO "ERROR"⊦
141:
CMD "I";FMT Y3,Z
;WRT 13⊦
142:
81→R4;53→R5;65→R
6;42→R2⊦
143:
CMD "?U-"⊦
144:
FMT FXD 0.2;WTB
13,R5;WTB 13,R6;
FMT "T";WRT 13⊦
145:
CMD "?M5"⊦
146:
GSB "RDB"⊦
147:
IF A≠R4;GTO "ERR
OR"⊦
148:
IF R2=42;GTO 151
⊦
149:
IF R2=43;GTO 152
⊦
150:
IF R2=44;GTO 153
⊦
151:
82→R4;50→R5;43→R
2;GTO 143⊦
152:
83→R4;53→R5;68→R
6;44→R2;GTO 143⊦
153:
CMD "?U-","A3-T"
,"?M5"⊦
154:
45→R2⊦
155:
GSB "RDB"⊦
156:
IF X>0.001184;
GTO "ERROR"⊦
157:
IF X≤0.001168;
GTO "ERROR"⊦
158:
CMD "?U-"⊦
159:
FMT 4,Z;WRT 13⊦
160:
FMT 3,Z;WRT 13⊦
161:
PRT "TEST COMPLE
TE"⊦
162:
END ⊦
163:
"RDB":RDB 13→A;
RDB 13→B;RDB 13→
C;FMT *;RED 13,X
⊦
164:
FXD 0.2;PRT A,B,
C;FXD 6.6;PRT X⊦
165:
RET ⊦
166:
"ERROR":FXD 0.2;
PRT "ERROR=",R2⊦
167:
"STOP"⊦
168:
"WAIT1":0→Y⊦
169:
Y+1→Y⊦
170:
IF Y≠278;GTO 169
⊦
171:
RET ⊦
172:
"WAIT2":0→Y⊦
173:
Y+1→Y⊦
174:
IF Y≠11;GTO 173⊦
175:
RET ⊦
176:
END ⊦
R67
```

Figure 8-17. HP-IB Verification Program (HP 9820A Calculator) (4 of 4)

Table 8-4. HP-IB Circuit Troubleshooting (1 of 18)

<table>
<tr><th>Error No.</th><th>Problem and Description</th><th>Corrective Action</th></tr>
<tr><td>None</td><td>Problem – Program hangs up without printing out error number. (RUNNING does not flash periodically on calculator display.)

Description – Signal output from Power Meter causes calculator to lock up.</td><td>A. Check that IFC input to Power Meter (Service Sheet 11) is not being held low by some circuit in Power Meter.
B. Check that Power Meter DAV output (Service Sheet 12) is not held low, indicating that Power Meter has data output for calculator.
C. Turn power on and off to Power Meter, restart program at line 10 (STEP PROGRAM) and verify handshake timing (refer to Service Sheet 4).</td></tr>
<tr><td>1</td><td>Problem – Power Meter does not output data after being addressed to talk.

Description – HP Interface Bus is set to local. (Remote Enable line false), and Power Meter is addressed to talk. Calculator I/O status is then checked to verify that Power Meter outputs data character during Display and Remote Talk Subroutine.</td><td>Turn power on and off to Power Meter. Then initialize test program (INIT key) and use STEP key to execute test program line-by-line. Check that the following indications are obtained for line 110:
A. Power Meter is addressed to talk.
B. The following display is obtained with logic analyzer connected normally (refer to troubleshooting example) and set up for single sweep, TRIGGER WORD 044_8 (Display and Remote Talk Subroutine Address).

00 010 011 15   00 010 010 7
00 100 100 16   00 010 011 8
10 100 101 1   10 100 100 9
00 100 110 2   00 010 010 10
01 001 000 3   00 010 011 11
01 001 001 4   10 100 100 12
11 001 010 5   00 010 010 13
10 100 100 6   00 010 011 14</td></tr>
<tr><td>2</td><td>Problem – Power Meter data output indicates dB [REF] mode selected.

Description –
1. HP Interface Bus is set to remote, then Power Meter is addressed to listen and programmed to free run at maximum rate, dB [REF] mode.
2. HP Interface Bus is set to local to disable remote operation of Power Meter.
3. Power Meter is addressed to talk and calculator enters data. Since local operation is enabled, the Power Meter mode output should indicate the mode selected by the front panel switches.</td><td>Turn power on and off to Power Meter. Go to line 110 and use STEP key to execute program line-by-line. Check that the following indications are obtained.
a. Line 160
1) Power Meter is unaddressed to talk.
2) Operating program branches from Display and Remote Talk Subroutine to Local/Remote Branch Subroutine. Program then continues to free run as previously verified for local operation.
b. Line 190
1) Power Meter is addressed to listen and configured for remote operation.
2) Measurement rate select logic stores programming command and provides low H HOLD and high H FAST outputs.
3) Mode Select logic stores programming command and provides dB [REF] mode output.</td></tr>
</table>

Table 8-4. HP-IB Circuit Troubleshooting (2 of 18)

Error No.	Problem and Description	Corrective Action
2 (cont)		4) Operating program branches from Local/Remote Branch Subroutine to Remote Initialize Subroutine. 5) The following display is observed with logic analyzer connected normally (refer to troubleshooting example) and set up for single sweep, TRIGGER WORD 012_8 (Remote Initialize Subroutine Address). 00 001 010 1 01 000 011 9 00 001 011 2 01 000 011 10 00 001 101 3 01 000 011 11 01 000 001 4 01 000 011 12 01 000 010 5 01 000 011 13 01 000 011 6 01 000 011 14 01 000 011 7 01 000 011 15 01 000 011 8 01 000 011 16 6) Operating program brances from Remote Initialize Subroutine to Measurement Subroutine, then continues to cycle normally as previously verified. **c. Line 210** – Power Meter configured for local operation. **d. Line 250/2380** – Power Meter is addressed to talk. **e. Line 250/2390** – Power Meter outputs complete data message. Verify data message per Read Byte Subroutine starting at line 5000.
3	**Problem** – Power Meter data output does not indicate dB[REF] mode selected. **Description** – The Power Meter was programmed to the dB [REF] mode in the previous test. Then the HP Interface Bus was set to local. For this test, the HP Interface Bus is set to remote and the Power Meter is programmed to take a triggered measurement with settling time. Thus, the dB [REF] output of the mode select logic should be loaded into the mode register during the operating program Remote Initialize Subroutine and the Power Meter should output MODE data character C during the Display and Remote Talk Subroutine.	Turn Power on and off to Power Meter. Then GO TO line 140, and use STEP key to execute program line-by-line. Check that the following indications are obtained: **a. Line 160** 1) Power Meter is unaddressed to talk. 2) Operating program branches from Display and Remote Talk Subroutine to Local Remote Branch Subroutine. Program then continues to free run as previously verified for local operation. **b. Line 190** 1) Power Meter is addressed to listen and configured for remote operation. 2) Measurement rate select logic stores programming command and provides low H HOLD and high H FAST outputs. 3) Mode select logic stores programming command and provides dB [REF] mode output. 4) Operating program branches from Local/Remote Branch Subroutine to Remote Initialize Subroutine.

Table 8-4. HP-IB Circuit Troubleshooting (3 of 18)

Error No.	Problem and Description	Corrective Action
3 (cont)		5) The following display is observed with logic analyzer connected normally (refer to troubleshooting example) and set up for single sweep, TRIGGER WORD 012_8 (Remote Initialize Subroutine Address). 00 001 010 1 01 000 011 9 00 001 011 2 01 000 011 10 00 001 101 3 01 000 011 11 01 000 001 4 01 000 011 12 01 000 010 5 01 000 011 13 01 000 011 6 01 000 011 14 01 000 011 7 01 000 011 15 01 000 011 8 01 000 011 16 6) The output of the mode select logic is loaded into the mode register (Service Sheet 3 during the Remote Initialize Subroutine). 7) Operating program branches from Remote Initialize Subroutine to Measurement Subroutine, then continues to cycle normally as previously verified. c. **Lines 210, 250, and 260** – previously verified. d. **Line 340** – (first pass) 1) Power Meter is addressed to listen and configured for remote operation. 2) H HOLD output of measurement rate select logic is set high by LTC instruction. 3) Operating program enters Display and Remote Talk Subroutine hold loop (addresses 022_8, 023_8, 024_8, 025_8). e. **Line 360/2390** – (first pass) 1) Power Meter outputs complete data message (ignore data) then branches to Local/Remote Branch Subroutine. 2) Power Meter enters Local/Remote Branch Subroutine hold loop. f. **Line 340** – (second pass) 1) Measurement rate select logic provides low H HOLD output to initiate program cycle. Program branches to Remote Initialize Subroutine. 2) The following display is observed with the logic analyzer connected normally (refer to troubleshooting example) and set up for single sweep, TRIGGER WORD 012_8 (Remote Initialize Subroutine address).

Table 8-4. HP-IB Circuit Troubleshooting (4 of 18)

Error No.	Problem and Description	Corrective Action
3 (cont)		00 001 010 1 01 010 111 9 00 001 011 2 01 010 111 10 10 001 101 3 01 010 111 11 00 001 110 4 01 010 111 12 00 001 111 5 01 010 111 13 10 011 001 6 01 010 111 14 10 011 110 7 01 010 111 15 01 010 111 8 01 010 111 16 3) Operating program branches from Delay Subroutine to Auto Zero Subroutine and cycles to Display and Remote Talk Subroutine. 4) Power Meter enters Display and Remote Talk Subroutine hold loop. **g. Line 360/2390** – (second pass) – Power Meter outputs complete data message. Verify data message per Read Byte Subroutine starting at line 5000.
4, 4.5	**Error** – If "ERROR #4" is printed, the Power Meter operating cycle is not synced to the trigger with settling time programming command. If "ERROR # 4" and "ERROR #4.5" are printed, the Power Meter did not respond properly to one or more of the programming commands. **Description** – 1. The error number is set to 4 and the Power Meter is programmed to auto zero, range 2, and trigger with settling time. Thus the Power Meter should output STATUS character U during the Display and Remote Talk Subroutine, thereby indicating that the auto zero loop is enabled, that it is operating on some range other than one, and that the input signal level is UNDER RANGE.	A. Turn power on and off to Power Meter, then manually send the following program command: CMD"?U–","T". Check that the programming command configures Power Meter for remote operation and causes operating program to enter Display and Remote Talk Subroutine hold loop (addresses 022_8, 023_8, 024_8, 025_8). **NOTE** *H HOLD output of measurement rate select logic is set low by programming command and reset high by LTC instruction generated at start of Display and Remote Talk Subroutine.* B. GO TO line 410 and use STEP key to execute program line-by-line. Check that the following indications are obtained. **a. Line 420–** 1) Auto zero enable logic stores auto zero programming command and provides auto zero enable output. 2) Range select logic stores range programming command and provides range 2 output. 3) H HOLD output of measurement rate select logic set low by trigger with settling time programming command. 4) Operating program branches from Display and Remote Talk Subroutine to Local/Remote Branch Subroutine. 5) Operating program branches to Remote Initialize Subroutine and the following display is observed with logic analyzer connected normally and set up for single

Table 8-4. HP-IB Circuit Troubleshooting (5 of 18)

Error No.	Problem and Description	Corrective Action
4, 4.5 (cont)	**Description (cont'd)** 2. The error number is set to 4.5 and the programming commands and status check are repeated. Thus, if error number 4 is detected and error number 4.5 is not detected, it indicates that the first Power Meter data output occurred before the remote programming commands were accessed by the operating program during the Remote Initialize Subroutine. (Power Meter free runs instead of entering hold loop until trigger input is received.) If both error numbers 4 and 4.5 are detected, it indicates that the Power Meter did not respond properly to the programming commands or that the Power Meter is improperly coding the STATUS output character.	B. **a. Line 420 (cont'd)** sweep, TRIGGER WORD 012_8 (Remote Initialize Subroutine address). 10 001 010 1 01 010 111 9 00 001 011 2 01 010 111 10 10 001 101 3 01 010 111 11 00 001 110 4 01 010 111 12 10 001 111 5 01 010 111 13 00 011 000 6 01 010 111 14 10 011 110 7 01 010 111 15 01 010 111 8 01 010 111 16 6) Range counter (Service Sheet 3) is preset to range 2 and output of mode select logic is loaded into mode register during Remote Initialize Subroutine time. 7) Operating program branches from Remote Initialize Subroutine and cycles to Display and Remote Talk Subroutine hold loop (address 022_8, 023_8, 024_8, 025_8. **b. Line 430/2390** – Power Meter outputs complete data message. Verify data message per Read Byte Subroutine starting at line 5000. **NOTE** *Status output is generated by buffering HOR and HUR outputs of over/under range decoder and YM3 output of mode select logic. For a description of circuit operation for this test, refer to Service Sheet 3, Mode Selection and Log Under-Range Registration.*
5	**Error** – Power Meter does not auto zero after ten tries. **Description** – The Power Meter is programmed to auto zero, range 1, trigger with settling time. Then the DATA output is checked to verify that it indicates 0.000 ± 0.001 μW. If the DATA output exceeds this value, the test number is incremented and the programming commands and DATA checks are repeated. If the DATA output still exceeds 0.000 ± 0.001 μW after ten tries (7=16), "ERROR # 5" is detected.	Change line 5000 to CMD "?U–", "ZIV". Then turn power on and off to Power Meter and check that RF power is not applied to Power Sensor. GO TO line 5000 and use STEP key to manually execute Read Byte Subroutine. Check that: **NOTE** *Program execution and circuit operation previously verified by local checkout procedure and preceding error checks except as specified below:* A. Range counter (Service Sheet 3) accepts range programming command and outputs range 1.

Table 8-4. HP-IB Circuit Troubleshooting (6 of 18)

Error No.	Problem and Description	Corrective Action
5 (cont)		B. Remote Initialize Subroutine address branching is as follows: 10 001 010 1 00 001 111 5 00 001 011 2 10 011 001 6 10 001 101 3 00 011 110 7 00 001 110 4 01 010 111 8 C. Range counter (Service Sheet 3) is preset to range 1 during Remote Initialize Subroutine. D. Operating program branches from Remote Initialize Subroutine to Delay Subroutine. E. Power Meter outputs correct data characters
6	**Error** – Power Meter status output does not indicate auto zeroing, range 1. **Description** – The Power Meter was programmed to auto zero on range 1 for the previous test. For this test, the Power Meter is programmed to the Watt Mode and a measurement is triggered. Then the Power Meter output status is checked to ensure that the auto-zero timer circuit (Service Sheet 10) holds the Power Meter in an auto zero loop for a period of approximately four seconds after the auto zero function is terminated.	Check Power Meter status output per Read Byte Subroutine starting at line 2500. **NOTE** *Status output is generated by buffering HOR and HUR outputs of over/under range decoder and YM3 output of mode select logic. For a description of circuit operation for this test, refer to Service Sheet 3, Mode Selection and Linear Under-Range Registration.*
7	**Error** – Power Meter status output does not indicate measured value valid. **Description** – For this test, the Power Meter was programmed to the Watt Mode, and a measurement was triggered. 10 seconds were allowed for the auto zero loop to clear, then the Power Meter was addressed to talk and the output status character was checked. Since range 1 was previously programmed, the Power Meter should output status character P, indicating that a valid measurement was taken. (For Watt Mode, range 1, an UNDER RANGE indication is not generated during the Under-Range Subroutine.)	GO TO line 640 and use STEP key to execute program line-by-line. Check that the following indications are obtained: **a. Line 640** 1) Auto zero enable logic is reset. 2) Mode enable logic outputs Watt mode. **b. Line 660** – Power Meter outputs correct status. Status output can be verified per Read Byte Subroutine starting at line 5000. **NOTE** *Status output is generated by buffering HOR and HUR outputs of over/under range decoder and YM3 output of mode select logic. For a description of circuit operation for this test, refer to Service Sheet 3, Mode Selection and Linear Under-Range Registration .*

Table 8-4. HP-IB Circuit Troubleshooting (7 of 18)

Error No.	Problem and Description	Corrective Action
8	**Error** — Power Meter does not hold 0 after being auto zeroed five consecutive times. **Description** — For the previous test, the Power Meter was programmed to the Watt Mode, thereby clearing the auto zero loop. For this test the Power Meter data output is checked to ensure that the Power Meter remains zeroed while configured for Watt Mode Operation.	Check Power Meter data output per Read Byte Subroutine starting at line 5000. (Data output should correspond to front-panel digital readout which was previously verified for local operation.)
9	**Error** — Power Meter range or mode output character wrong. **Description** — Power Meter programmed to Watt Mode, range 1, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Turn Power Meter on and off, then manually program Power Meter to Watt Mode, Range 1, trigger with settling time. (CMD "?U–","A1T"). B. Verify Power Meter Mode and Range character output per Read Byte Subroutine starting at line 5000. C. Check that 1) Mode select logic outputs Watt Mode. 2) Range Select Logic outputs range 1. 3) Range Counter is preset to range 1 during Remote Initialize Subroutine.
10	**Error** — Power Meter range or mode output character wrong. **Description** — Power Meter programmed to Watt Mode, range 2, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Turn Power Meter on and off, then manually program Power Meter to Watt Mode, range 2, trigger with settling time (CMD "?U–" "A2T"). B. Verify Power Meter mode and range character output per Read Byte Subroutines starting at line 5000. C. Check that: 1) Mode select logic outputs Watt Mode. 2) Range select logic outputs range 2. 3) Range counter is preset to range 2 during Remote Initialize Subroutine.
11	**Error** — Power Meter range or mode output character wrong. **Description** — Power Meter programmed to Watt Mode, range 3, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to Watt Mode, range 3, trigger with settling time (CMD "?U–","A3T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs Watt Mode. 2) Range select logic outputs range 3. 3) Range counter is preset to range 3 during Remote Initialize Subroutine. 4) Operating program branches from address 030_8 to address 056_8 (Remote Initialize Subroutine to Auto Zero Subroutine).

Table 8-4. HP-IB Circuit Troubleshooting (8 of 18)

Error No.	Problem and Description	Corrective Action
12	**Error** – Power Meter range or mode output character wrong. **Description** – Power Meter programmed to watt mode, range 4, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to Watt Mode, range 4, trigger with settling time (CMD "?U–" , "A4T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs Watt Mode. 2) Range select logic outputs range 4. 3) Range counter is preset to range 4 during Remote Initialize Subroutine. 4) The following display is obtained with the logic analyzer connected normally (refer to troubleshooting example) and set up for single sweep, TRIGGER WORD 012_8 (Remote Initialize Subroutine address). 10 001 010 1 10 001 110 5 10 001 011 2 00 101 110 6 00 001 100 3 00 101 111 7 10 001 101 4 00 101 111 8
13	**Error** – Power Meter range or mode output character wrong. **Description** – Power Meter programmed to Watt Mode, range 5, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Turn power on and off to Power Meter. Then manually program Power Meter to Watt Mode, range 5, trigger with settling time (CMD "?U–" , "A5T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs Watt Mode. 2) Range select logic outputs range 5. 3) Range counter is preset to range 5 during Remote Initialize Subroutine.
14	**Error** – Power Meter range or mode output character wrong. **Description** – Power Meter programmed to Watt Mode, auto range, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Turn power on and off to Power Meter. Then manually program Power Meter to Watt Mode, auto range, trigger with settling time (CMD "?U–" , "A9T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs Watt Mode. 2) Range select logic sets NAUTO output true. 3) Operating program branches from Remote Initialize Subroutine to Auto Zero Subroutine (Address 012_8 Q=1 not previously verified). 4) Range counter is counted down to range 1 during Power Meter operating program cycle.

Table 8-4. HP-IB Circuit Troubleshooting (9 of 18)

Error No.	Problem and Description	Corrective Action
15	**Error** – Power Meter range or mode output character wrong. **Description** – Power Meter programmed to dB (Rel) mode, range 1, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to dB (REL) mode, range 1, trigger with settling time (CMD "?U–" ,"B1T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 2500. C. Check that: 1) Mode select logic outputs dB [REF] mode and resets NAUTO output. 2) Range select logic outputs range 1. 3) Range counter is preset to range 1 and output of mode select logic is loaded into mode register during Remote Initialize Subroutine.
16	**Error** – Power Meter range or mode output character checked. **Description** – Power Meter programmed to dB (REL) mode, range 2, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to dB (REL) mode, range 2, trigger with settling time (CMD "?U–" , "B2T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs dB (REL) mode. 2) Range select logic outputs range 2. 3) Range counter is preset to range 2 during Remote Initialize Subroutine.
17	**Error** – Power Meter range or mode output character wrong. **Description** – Power Meter programmed to dB (REL) mode, range 3, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to dB (REL) mode, range 3, trigger with settling time (CMD "?U–" , "B3T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs dB (REL) mode. 2) Range select logic outputs range 3. 3) Range counter is preset to range 3 during Remote Initialize Subroutine.
18	**Error** – Power Meter range or mode output character wrong. **Description** – Power Meter programmed to dB (REL) mode, range 4, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to dB (REL) mode, range 4, trigger with settling time (CMD "?U–" , "B4T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic output dB (REL) mode. 2) Range select logic output range 4. 3) Range counter is preset to range 4 and output of mode select logic is loaded into mode register during Remote Initialize Subroutine.

Table 8-4. HP-IB Circuit Troubleshooting (10 of 18)

Error No.	Problem and Description	Corrective Action
19	**Error** — Power Meter range or mode output character wrong. **Description** — Power Meter programmed to dB (REL) mode, range 5, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to dB (REL) mode, range 5, trigger with settling time (CMD "?U–" , "B5T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic output dB (REL) mode. 2) Range select logic output range 5. 3) Range counter is preset to range 5 during Remote Initialize Subroutine.
20	**Error** — Power Meter range or mode output character wrong. **Description** — Power Meter programmed to dB (REL) mode, auto range, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to dB (REL) mode, auto range, trigger with settling time (CMD "?U–" , "B9T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs dB (REL) mode. 2) Range select logic sets NAUTO output true. 3) Range counter is counted down to range 1 during Power Meter operating program cycle.
21	**Error** — Power Meter range or mode output character wrong. **Description** — Power Meter programmed to dB [REF] mode, range 1, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to dB [REF] mode, range 1, trigger with settling time (CMD "?U–" , "C1T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs dB [REF] mode. 2) Range select logic outputs range 1 and resets NAUTO output. 3) Range counter is preset to range 1 and output of mode select logic is loaded into mode register during Remote Initialize Subroutine.
22	**Error** — Power Meter range or mode output character wrong. **Description** — Power Meter programmed to dB [REF] mode, range 2, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to dB [REF] mode, range 2, trigger with settling time (CMD "?U–" , "C2T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs dB [REF] mode. 2) Range select logic outputs range 2. 3) Range counter is preset to range 2 during Remote Initialize Subroutine.

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Table 8-4. HP-IB Circuit Troubleshooting (11 of 18)

Error No.	Problem and Description	Corrective Action
23	**Error** – Power Meter range or mode output character wrong. **Description** – Power Meter programmed to dB [REF] mode, range 3, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to dB [REF] mode, range 3, trigger with settling time (CMD "?U–" , "C3T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs dB [REF] mode. 2) Range select logic outputs range 3. 3) Range counter is preset to range 3 during Remote Initialize Subroutine.
24	**Error** – Power Meter range or mode output character wrong. **Description** – Power Meter programmed to dB [REF] mode, range 4, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power meter to dB [REF] mode, range 4, trigger with settling time (CMD "?U–" , "C4T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs dB [REF] mode. 2) Range select logic outputs range 4. 3) Range counter is preset to range 4 during Remote Initialize Subroutine.
25	**Error** – Power Meter range or mode output character wrong. **Description** – Power Meter programmed to dB [REF] mode, range 5, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to dB [REF] mode, range 5, trigger with settling time (CMD "?U–" , "C5T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs dB [REF] mode. 2) Range select logic outputs range 5. 3) Range counter is preset to range 5 during Remote Initialize Subroutine.
26	**Error** – Power Meter range or mode output characters wrong. **Description** – Power Meter programmed to dB [REF] mode, auto range, trigger with settling time. Then Power Meter addressed to talk and range and mode output characters checked.	A. Manually program Power Meter to dB [REF] mode, auto range, trigger with settling time (CMD "?U–" , "C9T"). B. Verify Power Meter mode and range character output per Read Byte Subroutine starting at line 5000. C. Check that: 1) Mode select logic outputs dB (REL) mode. 2) Range select logic sets NAUTO output true. 3) Range counter is counted down to range 1 during Power Meter operating program cycle.

Table 8-4. HP-IB Circuit Troubleshooting (12 of 18)

Error No.	Problem and Description	Corrective Action
27	**Error** — Power Meter range, mode, or data output wrong. **Description** — Power Meter programmed to dBm mode, range 1, trigger with settling time. Then Power Meter addressed to talk and range, mode, and data output checked. (Data output corresponds to minimum threshold of dBm range 1, —30 dBm).	A. Manaully program Power Meter to dBm mode, range 1, trigger with settling time (CMD "?U—" , "D1T"). B. Verify Power Meter mode, range and data character output per Read Byte Subroutine starting at line 5000. (Data output should correspond to indication on Digital Readout previously verified for local operation.) C. Check that: 1) Mode select logic outputs dBm mode. 2) Range select logic outputs range 1 and resets NAUTO output. 3) Range counter is preset to range 1 during Remote Initialize Subroutine.
28	**Error** — Power Meter range, mode, or data output wrong. **Description** — Power Meter programmed to dBm mode, range 2, trigger with settling time. Then Power Meter addressed to talk and range mode and data output checked. (Data output should correspond to minimum threshold of dBm range 2, —20 dBm.)	A. Manually program Power Meter to dBm mode, range 2, trigger with settling time (CMD "?U—" , "D2T"). B. Verify Power Meter mode data and range character output per Read Byte Subroutine starting at line 5000. (Data output should correspond to indication on Digital Readout previously verified for local operation.) C. Check that: 1) Mode select logic outputs dBm mode. 2) Range select logic outputs range 2. 3) Range counter is preset to range 2 during Remote Initialize Subroutine.
29	**Error** — Power Meter range, mode, or data output wrong. **Description** — Power Meter programmed to dBm mode, range 3, trigger with settling time. Then Power Meter addressed to talk and range mode and data output checked. (Data output should correspond to minimum threshold of dBm range 3, —10 dBm.)	A. Manually program Power Meter to dBm mode, range 3, trigger with settling time (CMD "?U—" , "D3T"). B. Verify Power Meter mode, data, and range character output per Read Byte Subroutine starting at line 5000. (Data output should correspond to indication on Digital Readout previously verified for local operation.) C. Check that: 1) Mode select logic outputs dBm mode. 2) Range select logic outputs range 3. 3) Range counter is preset to range 3 during Remote Initialize Subroutine.

Table 8-4. HP-IB Circuit Troubleshooting (13 of 18)

Error No.	Problem and Description	Corrective Action
30	**Error –** Power Meter range or mode output character wrong. **Description –** Power Meter programmed to dBm mode, range 4, trigger with settling time. Then Power Meter addressed to talk and range, mode, and data output checked. (Data output should correspond to minimum threshold of dBm range 4, 0 dBm.)	A. Manually program Power Meter to dBm mode, range 4, triggered with settling time (CMD "?U–" , "D4T"). B. Verify Power Meter mode data, and range character output per Read Byte Subroutine starting at line 5000. (Data output should correspond to indication on Digital Readout previously verified for local operation.) C. Check that: 1) Mode select logic outputs dBm mode. 2) Range select logic outputs range 4. 3) Range counter is preset to range 4 during Remote Initialize Subroutine.
31	**Error –** Power Meter range, mode, or data output wrong. **Description –** Power Meter programmed to dBm mode, range 5, trigger with settling time. Then Power Meter addressed to talk and range, mode, and data output checked. (Data output should correspond to minimum threshold of dBm range 5, 10 dBm.)	A. Manually program Power Meter to dBm mode, range 5, trigger with settling time (CMD "?U–" , "D5T"). B. Verify Power Meter mode, data, and range character output per Read Byte Subroutine starting at line 5000. (Data output should correspond to indication on Digital Readout previously verified for local operation.) C. Check that: 1) Mode select logic outputs dBm mode. 2) Range select logic outputs range 5. 3) Range counter is preset to range 5 during Remote Initialize Subroutine.
32	**Error –** Power Meter range, mode, or data output wrong. **Description –** Power Meter programmed to dBm mode, auto range, trigger with settling time. Then Power Meter addressed to talk and range, mode, and data output checked. (Data output should correspond to minimum threshold of dBm range 1, –30 dBm.)	A. Manually program Power Meter to dB [REF] mode, auto range, trigger with settling time (CMD "?U– ,"D9T"). B. Verify Power Meter mode, range, and data character output per Read Byte Subroutine starting at line 5000. (Data character output should correspond to indication on Digital Readout previously verified for local operation.) C. Check that: 1) Mode select logic outputs dBm mode. 2) Range select logic sets NAUTO output true. 3) Range counter is counted down to range 1 during Power Meter operating program cycle.

Table 8-4. HP-IB Circuit Troubleshooting (14 of 18)

Error No.	Problem and Description	Corrective Action
33	**Error** – Power Meter does not respond properly to device clear. **Description** – The Power Meter is first programmed to range 5, dBm mode, free run at maximum rate. Then a device clear is sent to the Power Meter to select Watt mode, auto range, hold operation. Following the device clear, a measurement is triggered, the Power Meter is addressed to talk, and the Power Meter status, range, and mode outputs are checked to verify proper response to the device clear.	Turn power on and off to Power Meter. Then GO TO line 1040 and use STEP key to manually execute program line-by-line. Check that the following indications are observed. **a. Line 1050** – 1) Power Meter configured for remote operation. 2) The following display is observed with logic analyzer connected normally (refer to troubleshooting example) and set up for single sweep, TRIGGER WORD 012_8. 10 001 010 1 11 000 001 5 10 001 011 2 01 000 011 6 00 001 100 3 01 000 011 7 00 001 101 4 01 000 011 8 3) dBm output of mode select logic is loaded into mode register. **b. Line 1060/2430** – 1) Device clear decoder (Service Sheet 11) generates LPU output in response to device clear command. 2) Mode select logic outputs Watt mode in response to LPU input. 3) Range select logic sets auto range qualifier true in response to LPU input. 4) Measurement rate select logic sets H HOLD output true in response to LPU input. 5) Operating program initialized to starting address 000_8 by LPU signal. Program then cycles to Local/Remote Branch Subroutine hold loop (026_8, 042_8, 043_8) when LPU signal is terminated. (During Power Up Subroutine, watt mode output of mode select logic is loaded into mode register.) **c. Line 1070** – Measurement triggered and operating program cycles to hold loop in Display and Remote Talk Subroutine. During program cycle, range counter is counted down to range 1. **d. Line 1080/2380** – Power Meter outputs correct status, mode, and range characters. Power Meter output can be verified per Read Byte Subroutine starting at line 5000.
34	**Error** – Power Meter incorrectly decodes address data as device clear. **Description** – The Power Meter is programmed to the dBm mode and a measurement is triggered to load the mode select registers. Then a number of ASCII characters are sent to the Power Meter to ensure that it will not erroneously decode these characters as a device clear command. After the last character is	GO TO line 1150 and use STEP key to manually execute test program line-by-line. Check LPU output of device clear decoder (Service Sheet 11) for each ASCII character sent.

Service Model 436A

Table 8-4. HP-IB Circuit Troubleshooting (15 of 18)

Error No.	Problem and Description	Corrective Action
34 (cont)	sent, the Power Meter is programmed to trigger immediate, talk and the mode output is checked to ensure that the Power Meter is still operating in the dBm mode.	
35	**Error** – Power Meter doesn't go into hold after receiving device clear. **Description** – A device clear is sent to the Power Meter to select watt mode, auto range operation. Then a 200 ms delay is provided after which the Power Meter is programmed to the dBm mode, range 3, trigger immediate. Following these programming commands, a talk cycle is enabled and the calculator checks Power Meter output status, range, and mode data. The purpose of this test is to verify that the device clear command causes the Power Meter to enter a hold condition while awaiting a trigger command. If the device clear doesn't cause the Power Meter to enter the hold loop, the talk cycle will be enabled before the programming commands are loaded into the mode register and range counter. Thus the Power Meter will output the mode, range, and status selected by the preceding device clear command.	Turn power on and off to Power Meter. Then send the following programming command to configure the Power Meter for remote operation CMD "?U–". After the Power Meter is configured for remote operation, GO TO line 1300 and use STEP key to manually execute program line-by-line. Check that the following indications are observed: a. **Line 1300/2430** – Operating program is initialized to starting address 000_8 by LPU output of device clear decoder. Operating program then cycles to Local/Remote Branch Subroutine hold loop when LPU signal is terminated. b. **Line 1330** – H HOLD output of measurement rate select logic is set false by trigger immediate programming command and operating program cycles to Display and Remote Talk Subroutine hold loop. c. **Line 1340/2380** – Power Meter outputs connect status, range and mode characters. Power Meter output can be verified per Read Byte Subroutine starting at line 5000.
36	**Error** – Power Meter responds to invalid listen address. **Description** – The Power Meter is programmed to the watt mode, and a measurement is triggered to load the mode select registers. Then a Power Meter talk cycle is enabled to unaddress the Power Meter to listen. After the talk cycle, false listen addresses are sent to the Power Meter followed by a dBm mode programming command. If the Power Meter is functioning properly it will not respond to the dBm mode programming command because it should not be addressed to listen. Thus, it should output mode character A, thereby indicating that it is operating in the watt mode.	GO TO line 1410 and use STEP key to manually execute program line-by-line. Check that Power Meter is unaddressed to listen in line 1430 and is not addressed to listen in line 1440 (H LSTN test point A11TP4 remains low). If Power Meter is addressed to listen in line 1440 use the following program to isolate the malfunction: CMD "? MS" – (H LSTN test point goes low) CMD "?U–" – (H LSTN test point goes high) CMD "?MS" – (H LSTN test point goes low) CMD "?U%" – (H LSTN test point remains low) CMD "?U)" – (H LSTN test point remains low) CMD "?U," – (H LSTN test point remains low) CMD "?U–=" – (H LSTN test point remains low) CMD "?U/" – (H LSTN test point remains low) **NOTE** *Address 102_8 Q = 0 of Remote Initialize Subroutine has not been previously verified. To verify this address, turn power on and off to Power Meter, set front-panel MODE switch to dBm, then manually program Power Meter to remote mode and then to watt mode, range 3, trigger immediate (CMD "?U–") (CMD "?U–", "A3I") and check that the following indications are obtained.*

Table 8-4. HP-IB Circuit Troubleshooting (16 of 18)

Error No.	Problem and Description	Corrective Action
36 (cont)		1) The following display is obtained with the logic analyzer connected normally (refer to troubleshooting example) and set up for single sweep, TRIGGER WORD 012_8 (Remote Initialize Subroutine address). 10 001 010 1 11 000 010 5 00 001 011 2 01 000 100 6 00 001 101 3 01 000 100 7 01 000 001 4 01 000 100 8 2) The watt mode output of the mode select logic is loaded into the mode register during the Remote Initialize Subroutine.
37	**Error** – Power Meter takes trigger immediate measurement when programmed to trigger with settling time. **Description** – The Power Meter is first programmed to watt mode, range 2, trigger immediate, then a talk cycle is enabled to cause the Power Meter to enter the Remote Initialize Subroutine hold loop. Following the talk cycle a trigger with settling time programming command is sent to the Power Meter and the calculator checks I/O status after a 200 ms delay. Since the Power Meter is programmed to range 2, access time to the first data character is approximately 1130 ms. Thus, the calculator should detect STAT 13 = 2.	GO TO line 1530 and use STEP key to manually execute program line-by-line. Check that the following indications are obtained: **a. Line 1530** – 1) L HOLD output of measurement rate select logic is set false by trigger immediate programming command. 2) Operating program branches from Local/Remote Branch Subroutine Hold Loop to Remote Initialize Subroutine. 3) The following display is observed with the logic analyzer connected normally (refer to troubleshooting example) and set up for single sweep, TRIGGER WORD 012_8 (Remote Initialize Subroutine Address). 10 001 010 1 11 000 010 5 00 001 011 2 01 000 100 6 00 001 101 3 01 000 100 7 01 000 001 4 01 000 100 8 **b. Line 1550** – The following display is observed with the logic analyzer connected normally (refer to troubleshooting example) and set up for single sweep, TRIGGER WORD 012_8 (Remote Initialize Subroutine Address). 10 001 010 1 10 001 111 5 00 001 011 2 00 011 000 6 10 001 101 3 10 011 110 7 00 001 110 4 01 010 111 8
38	**Error** – Power Meter takes trigger with settling time measurement when programmed to trigger immediate. **Description** – A talk cycle is first enabled to complete the output data transfer initiated for the previous test. Then a trigger immediate programming command is sent to the Power Meter to initiate the next talk cycle and the calculator checks I/O status after a 200 ms delay. Since the Power Meter is programmed to the Watt Mode, worst case access time to the first output data character is 70 ms. Thus, the calculator should detect STAT 13 = 3.	GO TO line 1610 and use STEP key to manually execute program line-by-line. Check that the following display is obtained with the logic analyzer connected normally and set up for single sweep, TRIGGER WORD 012_8 (Remote Initialize Subroutine Address). 10 001 010 1 11 000 010 5 00 001 011 2 01 000 100 6 00 001 101 3 01 000 100 7 01 000 001 4 01 000 100 8

Table 8-4. HP-IB Circuit Troubleshooting (17 of 18)

Error No.	Problem and Description	Corrective Action
39	**Error** – Power Meter data output wrong when CAL ADJ control is adjusted to obtain .799 mW indication on front-panel Digital Readout. **Description** – The test number is set to 1 and the Power Meter is programmed to range 3, free run at maximum rate. CAL FACTOR % switch disabled (100%). Then the Power Meter is addressed to talk and the output data is checked after each talk cycle. If the output data does not indicate .799 mW within 300 talk cycles, an error is detected.	**NOTE** *Operating program execution and circuit operation previously verified per local checkout procedure except as indicated below.* Check Power Meter data output per Read Byte Subroutine starting at line 5000.
40	**Error** – Power Meter data output wrong when CAL ADJ control is adjusted to obtain .866 mW indication on front-panel Digital Readout. **Description** – The test number is set to 1 and the Power Meter continues to free run at the maximum rate on watt mode range 3. Since the Power Meter is still addressed to talk, it outputs data during each talk cycle and the calculator checks to see if the data indicates .866 mW. If the output data does not indicate .866 mW within 300 talk cycles, an error is detected.	**NOTE** *Operating program execution and circuit operation previously verified per local checkout procedure except as indicated below.* Check Power Meter data output per Read Byte Subroutine starting at line 5000.
41	**Error** – Device clear command does not disable CAL FACTOR % switch. **Description** – The verification program halts and the CAL ADJ control is adjusted to obtain a 1.000 mW indication on the front panel digital readout (Power Meter is free running per previous programming commands.) Then the verification program is manually restarted and a cal factor enable programming command is sent to the Power Meter followed by a device clear command. After the programming commands are sent, a talk cycle is enabled and the calculator checks the data output to ensure that the device clear command disabled the CAL FACTOR % switch.	Program Power Meter to free run (CMD "?U–", "R"). Then GO TO line 2000 and use STEP key to manually exercise program line-by-line. Check that the following indications are obtained: a. **Line 2000** – Cal Factor Disable Logic sets Cal Factor Disable output false (front-panel digital readout indication changes from 1.00 mW to 1.17 ± 0.01 mW). b. **Line 2010/2430** – Cal Factor Disable Logic sets Cal Factor Disable output true in response to LPU output of device clear generator. (Device clear places operating program in hold loop; since measurement is not triggered, display does not change.) c. **Line 2030** – Measurement is triggered and front-panel digital readout indication changes to 1.00 mW). d. **2040/2390** – Power Meter outputs correct data characters. Power Meter data output can be verified per Read Byte Subroutine starting at line 5000.

Table 8-4. HP-IB Circuit Troubleshooting (18 of 18)

Error No.	Problem and Description	Corrective Action
42	**Error** – Power Meter does not provide under range, watt mode status output. **Description** – The Power Meter is programmed to range 5, watt mode, and a measurement is triggered. Then a talk cycle is enabled and the calculator checks the Power Meter status output. Since a 1 mW RF level is applied to the Power Sensor, the status output should indicate under range, watt mode.	Manually program Power Meter CMD "?U–" ,"A5R". Check Power Meter status output per Read Byte Subroutine starting at line 5000. **NOTE** *Power Meter status output is generated by buffering HOR and HUR outputs of over/under range decoder and YM3 output of mode select logic. For a description of circuit operation for this test, refer to Service Sheet 3, Block Diagram Description, Mode Selection and Linear Under Range Registration.*
43	**Error** – Power Meter does not provide under range log mode status output. **Description** – The Power Meter is programmed to range 5, dBm mode and a measurement is triggered. Then a talk cycle is enabled and the calculator checks the Power Meter output status. Since a 1 mW RF level is applied to the Power Sensor, the status output should indicate under range, log mode.	Manually program Power Meter CMD "?U–" , "D5R". Check Power Meter status output per Read Byte Subroutine starting at line 5000. **NOTE** *Power Meter status output is generated by buffering HOR and HUR outputs of over/under range decoder and YM3 output of mode select logic. For a description of circuit operation for this test, refer to Service Sheet 3, Block Diagram Description, Mode Selection and Log Under-Range Registration.*
44	**Error** – Power Meter does not provide over range status output. **Description** – The Power Meter is programmed to range 2, watt mode, and a measurement is triggered. Then a talk cycle is enabled and the calculator checks the Power Meter status output. Since a 1 mW RF level is applied to the Power Sensor, the status output should indicate an over range condition.	Manually program Power Meter CMD "?U–" , "A2R". Check Power Meter status output per Read Byte Subroutine starting at line 5000. **NOTE** *Power Meter status output is generated by buffering HOR and HUR outputs of over/under range decoder and YM3 output of mode select logic. For a description of circuit operation for this test, refer to Service Sheet 3, Block Diagram Description, Mode Selection and Linear Over-Range Registration.*
45	**Error** – Cal factor enable programming command does not enable CAL FACTOR % switch. **Description** – The Power Meter is programmed to watt mode, range 3, CAL FACTOR % switch enabled, trigger with settling time. Then a talk cycle is enabled and the calculator checks Power Meter data output. Since CAL FACTOR % switch is now enabled in the 85% position, the data output should be 1.176 ± 0.008 mW. (CAL ADJ control was previously adjusted to obtain a 1.000 mW indication with CAL FACTOR % switch disabled. Disabling the switch is the same as setting it to 100% when it is enabled.)	Manually program Power Meter CMD "?U–" , "+R". GO TO line 2200 and use STEP key to manually execute program line-by-line. Check that the following indications are obtained: **a. Line 2200** – Cal Factor Disable output of Cal Factor Disable logic is set false by programming command (front-panel Digital Readout indication changes from 1.000 mW to 1.176 mW). **b. Line 2220/2380** – Power Meter outputs correct data character. Power Meter data character output can be verified per Read Byte Subroutine starting at line 5000.

CIRCUIT DESCRIPTIONS

Paragraphs 8-68, 8-69 and Table 8-5 were deleted.

8-70. BLOCK DIAGRAM CIRCUIT DESCRIPTIONS

8-71. Service Sheet 1

8-72. The Model 436A is a digital readout Power Meter which can be operated locally via front-panel controls or remotely via the HP-IB Interface Bus (Option 022). The overall power range and frequency response of the Power Meter is determined by the Power Sensor to which it is connected.

8-73. When the Power Meter is operated locally, the Push-Button Switch Assembly enables selection of the measurement mode (dB, watts) and the auto-ranging circuits normally select the most sensitive range for measurement of input power. Should the operator desire to make all measurements on a specific range, however, a RANGE HOLD switch allows the Power Meter to be locked in any one of the five measurement ranges.

8-74. When the Power Meter is operated remotely, the front-panel controls are disabled, and measurement mode and range are selected by programming inputs from the remote interface. Remote operation can only be enabled via the remote interface; it cannot be enabled via the front panel.

8-75. As shown on Service Sheet 1, all of the Power Meter operating functions are enabled and/or sequenced by the outputs of the Controller. These outputs, in turn, are generated by processing the qualifier, mode, and range select inputs according to an operating program stored in a MOS memory chip. Thus, in order to understand the functions of the circuits shown on the block diagram, it is first necessary to consider their relationship to the operating program. An overall flow chart of the operating program is illustrated in Figure 8-15, Sheet 1. As shown in the figure, the operating program is divided into subroutines with each subroutine providing some dedicated function. When the Power Meter is first turned on, the operating program is preset to its power up address and the power up subroutine is executed to initialize the Power Meter circuits. After the power up subroutine is executed, the program cycles normally with one measurement being taken and the results displayed for each cycle. During each cycle, the circuits shown on the block diagram operate as described in the following paragraphs.

a. **Power Sensor, Amplifier, Demodulator, Filter, and True-Range Decoder.** The inputs to these circuits from the Controller are allowed to change only once during each program cycle. Thus, the circuits are, in effect, continuously enabled and provide constant outputs. The outputs of the Amplifier, Filter, and Demodulator Circuits are dc representations of the RF input power level applied to the Power Sensor. The outputs of the True-Range Decoder are reference values which account for the different sensitivities of the various types of Power Sensors that can be used with the Power Meter.

b. **Counters, Clock Generator, and Analog-to-Digital Converter.** The Clock Generator provides program clock outputs which enable sequencing of the operating program and counting of the Up/Down Counters. The Counters are enabled by the Controller to provide timing references for execution of the operating program and to function in conjunction with the Analog-to-Digital (A-D) Converter to convert the dc output of the Amplifer, Demodulator, and Filter Circuit to an equivalent BCD number.

c. **Display.** The Display is updated during each program cycle as required to indicate current range, mode, input power level, and/or over/under-range status. After each update the new indications are continuously maintained until the next update.

d. **Controller.** The Controller provides the necessary hardware/software interface between the operating program and the remainder of the Power Meter circuits.

e. **Pushbutton Switch Assembly.** The Pushbutton Switch Assembly is enabled when the Power Meter is configured for local operation and is disabled when the Power Meter is configured for remote operation. When enabled, the switches provide continuous mode select and auto-range qualifier outputs which are processed by the Controller once during each operating cycle to enable the desired Power Meter operation.

f. **Remote Interface Circuits.** The Remote Interface Circuits enable the Power Meter to be interfaced to a remote controller via an HP-IB or BCD format. Thus, when remote operation is enabled, these circuits essentially take over the

CIRCUIT DESCRIPTIONS

Service Sheet 1 (cont'd)
functions of the Pushbutton Switch Assembly and the Display in that they provide for remote control of Power Meter operation and remote display of the results. When remote operation is enabled, the Pushbutton Switch Assembly is disabled; the Display, however, remains enabled and provides a local display of the output data transmitted to the remote controller.

g. **Power Reference Oscillator.** The Power Reference Oscillator is enabled when the front-panel POWER REF ON switch is depressed and provides 1 mW at 50 MHz output for calibration purposes.

h. **Power Supply Assembly.** The Power Supply Assembly is enabled when the LINE ON-OFF switch is set to the ON position and provides +5, +15, and —15 Vdc outputs necessary for operation of the Power Meter circuits.

8-75. Service Sheet 2

8-76. Amplifier, Demodulator, and Filter Circuit. The Amplifier, Demodulator and Filter Circuits convert RF input power levels applied to the Power Sensor into proportional dc outputs. The basic operation of these circuits is described in the following paragraphs.

a. The Power Sensor dissipates RF input power into a 50-ohm termination and generates a dc voltage proportional to the RF input power level.

b. The 220 Hz Multivibrator provides the 220 Hz drive signals to the Power Sensor to switch the dc voltage and thereby generate a modulated 220 Hz signal which is proportional in amplitude to the RF input power level and in phase with the 220 Hz reference signal applied to the phase detector.

c. The Power Sensor's Input Amplifier and the Power Meter's First Amplifier function together to amplify the modulated 220 Hz signal by a factor of 600.

d. The overall gain factor of the Second and Third Amplifiers is determined by the RANGE SELECT input to the Range and Filter Control ROM and the setting of the front-panel CAL ADJ control. The CAL ADJ control is normally set as required to calibrate the Power Sensor and the Power Meter to a known standard. When the CAL ADJ control is set properly, the outputs of the ROM configure the Attenuators such that the minimum and maximum signal levels at A2TP3 (AC) are the same for each range. (For either Watts or dB measurements an in-range input power level corresponds to a 0.3 to 3.6 Vp-p signal level at A2TP3.)

e. The Phase Detector functions as a chopper-stablized amplifier to remove any noise riding on the modulated 220 Hz input. Thus, the output of the Phase Detector is an unfiltered dc signal which is proportional to the true amplitude of the modulated 220 Hz input signal.

f. The Meter Driver Amplifier buffers the ϕ DET output and applies it to the front-panel Meter (M1) via an RC filter and a diode limiter network. Since the response of the meter is not limited by the Variable Low-Pass Filter, the meter serves to provide relatively instantaneous indications of changes in input power level. Calibration of the meter to the front-panel Digital Readout is accomplished via the METER ADJ control.

g. The diode limiter clips over range outputs of the Phase Detector to reduce the time that it takes for the Variable Low-Pass Filter to respond to a full-scale change in input signal level. The response time of the Filter varies with the bandpass selected by the outputs of the ROM. For ranges 5, 4, and 3, the bandpass is 17 Hz. For ranges 2 and 1, the bandpass is reduced by factors of ten to 1.7 Hz and 0.17 Hz, respectively. These bandpass values represent the optimum tradeoff between filter response time and signal-to-noise ratio. On the higher ranges, the gain of the Power Meter is relatively low and the 17-Hz bandpass enables the Filter to respond to a full-scale change in input signal level in 0.1 second (see Figure 3-7). On the lower ranges, the gain of the Power Meter increases and a higher noise level is present at the output of the Phase Detector. Thus, a narrower bandpass is required to maintain the desired signal-to-noise ratio at the input of the A-D Converter. The time required for the Filter to respond to a full-scale change in input signal level is 1 second on range 2 and ten seconds on range 1.

CIRCUIT DESCRIPTIONS

Service Sheet 2 (cont'd)

h. The DC Amplifier buffers the output of the Filter and applies it to the A-D Converter for conversion to a BCD number. The gain of the DC Amplifier is 1 when the CAL FACTOR % switch is set to 100. The gain increases by approximately 1% for each lower-numbered position. The switch is normally set to the position specified on the Power Sensor's CAL FACTOR curve. When the switch is set properly, the output of the DC Amplifier in millivolts indicates the numeric value of the RF input power level. The decimal point and multiplier are provided by the True Range Decoder.

8-77. Auto-Zero Assembly. The Auto-Zero Assembly's function is to remove any dc offset voltage associated with the Power Sensor. When the front-panel SENSOR ZERO switch is pressed, the Controller activates the Sensor Auto-Zero Enable input for a period of approximately four seconds. While this input is active, a feedback loop is configured between the Auto-Zero Assembly and the Power Sensor to allow a capacitor in the Auto-Zero circuit to charge to a value that cancels the dc offset of the Power Sensor. Loop stability is achieved when the Mount Auto-Zero output of the Auto-Zero Assembly holds the dc level at A3TP4 (DC) at 0.000 ± 0.002V. After the Sensor Auto-Zero Enable input is terminated, the feedback loop is broken, and the capacitor is held at the charged value. Thus the Mount Auto-Zero output continues to cancel the dc offset of the Power Sensor, thereby allowing accurate measurement of RF input power levels.

8-78. Analog-to-Digital (A-D) Converter. The Analog-to-Digital Converter (Figure 8-18) operates together with the Counters (see Service Sheet 3) to convert the dc output of the Amplifier, Demodulator, and Filter Circuits to a four-digit BCD number which indicates the numeric value of the RF input power level applied to the Power Sensor. Operation of the A-D Converter can be divided into three basic functions, auto-zero function, measurement function, and conversion function. As shown in Figure 8-15, Sheet 1, a subroutine is dedicated to each of these functions and the functions are performed in sequence during every program cycle. (Additional auto-zero functions may be enabled at other times in the program cycle if various predetermined operating conditions are detected.) During the auto-zero subroutine, a feedback loop is closed to remove any dc offset voltage present at the reference (+) input of the Ramp Generator. During the measurement subroutine, the Ramp Generator is charged to −7 times the dc input value. During the conversion subroutine, the Ramp Generator is discharged at a linear or exponential rate and the Counters are clocked to measure the time that it takes for the Ramp Generator to discharge through threshold.

8-79. A-D Converter Auto-Zero Function. The auto-zero function is enabled when the Controller activates the AUTO-ZERO ENABLE input to the A-D Converter. During the Auto-Zero subroutine, this input is maintained for 133 ms (the Controller enables the main Counter when the input is activated, and terminates the input when the count reaches 8000). For auto-zero functions generated at other points in the program cyle, the auto-zero timing interval varies according to the instantaneous conditions detected. While the AUTO-ZERO ENABLE input is active, the Auto-Zero Switch is closed and a feedback loop is configured from the output of the Comparator to the positive input of the Ramp Generator. Loop stability is achieved when capacitor C1 charges such that the output of the Comparator is 2.00 Vdc. When the Auto-Zero Enable input is terminated, the Auto-Zero Switch is opened and the charge on C1 holds the output of the Comparator at 2.00 Vdc which is the appropriate mid-range value for initiating the measurement function.

8-80. A-D Converter Measurement Function. The measurement function is initiated when the Controller activates the Load DC INPUT. This input is then maintained active for approximately 33 ms. (The Controller enables the Main Counter when the input is activated and terminates the input when the output of the Main Counter reaches 2000.) While the input is active, the DC Input Switch is closed to allow C3 to charge to −7 times the DC Input level. When the input is terminated, the DC Input Switch is opened and the Controller enables a linear or log conversion to discharge C3.

8-81. A-D Converter Linear Conversion. A linear conversion function is selected to discharge C3 when the Power Meter is configured for WATT MODE operation. During the conversion, C3 is discharged at the rate of 3 mV per clock pulse, and the Main Counter is counted up from 0000 on

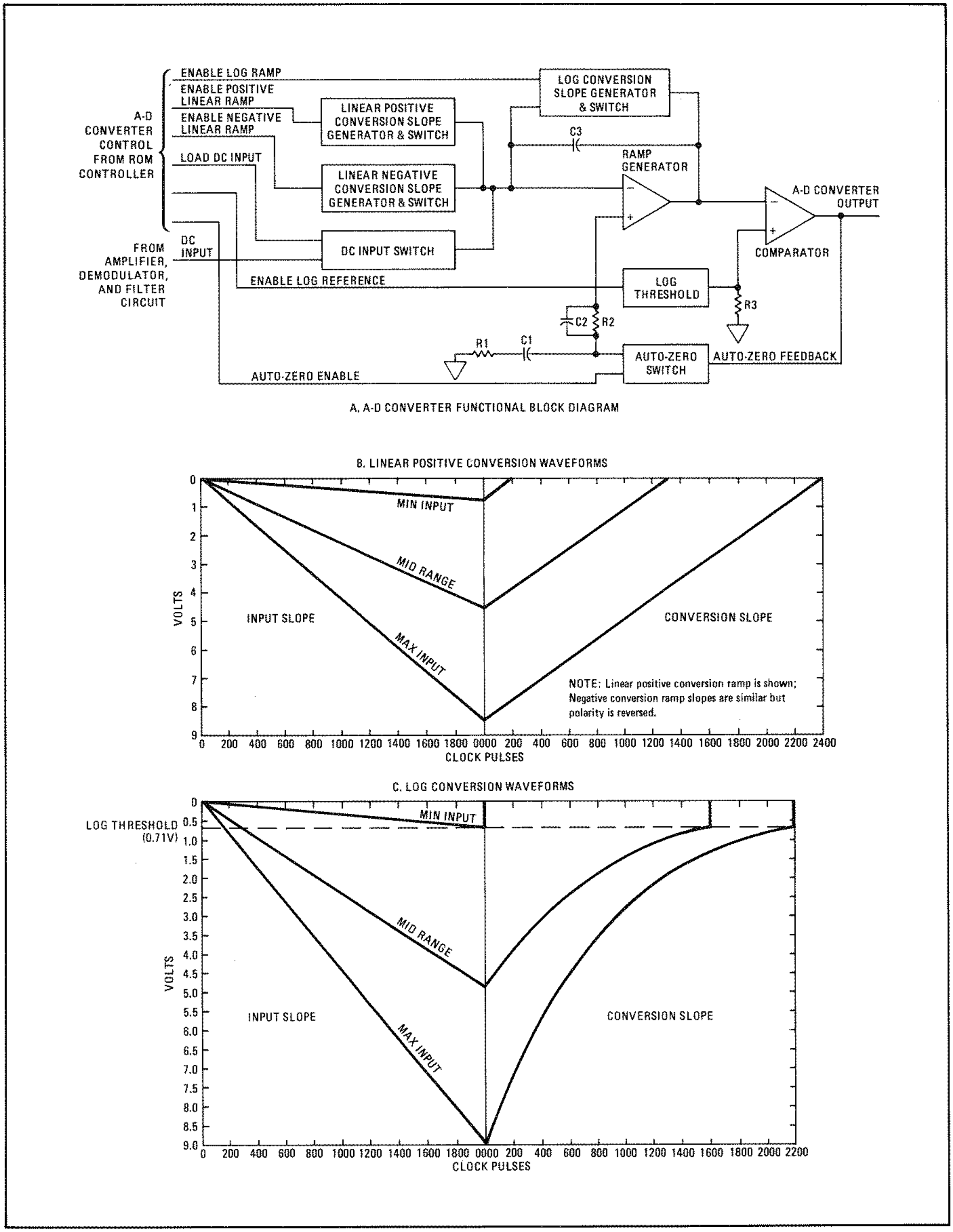

Figure 8-18. Analog-to-Digital Converter Simplified Diagram and Waveforms

CIRCUIT DESCRIPTIONS

Service Sheet 2 (cont'd)

every other clock pulse. Thus, the Main Counter is incremented each time that C3 is discharged by 7 mV. Since C3 was charged to −7 times the dc input level during the measurement function, each count represents a 1 mV dc input level. When C3 is fully discharged, then the output of the Main Counter is equal to the original dc input in millivolts. As stated previously, this number represents the RF input power level applied to the Power Sensor.

8-82. The operating sequence for the linear conversion function is described in the following paragraphs.

a. The Controller first checks the A-D qualifier output of the Comparator. If the qualifier is a logic one, the Controller activates the LRP input to enable a positive conversion. If the qualifier is a logic 0, the Controller activates the LRM input to enable a negative conversion. The LRP or LRM input is then held active for the duration of the conversion.

b. After the LRP or LRM input is activated, the Controller alternately monitors the qualifier outputs of the Comparator and the Main Counter to detect completion of the conversion when the Comparator qualifier changes state, or when the output of the Main Counter reaches 1200. If the Comparator's output changes state before the output of the Main Counter reaches 0100, an under-range conversion is detected. If the output of the Comparator does not change state by the time the output of the Main Counter reaches 1200, an over-range conversion is detected. If the output of the Comparator changes state anywhere between these two points in time, the Controller detects an in-range conversion.

c. When the Controller detects that the conversion is completed, it terminates the LRP or LRM input and updates the front-panel status and Digital Readout indications as described in Service Sheet 3.

8-83. A-D Converter Log Conversion. A log conversion function is selected to discharge C3 when the Power Meter is configured for dB operation. This function is similar to a linear conversion except as noted below.

a. The LRL input is activated to discharge C3 at an exponential rate so that the output of the counter indicates the RF input power level in dB.

b. The LLGR input is activated to change the Comparator's threshold input to −0.71V so that an under-range condition is detected if C3 charges to less than this value during the measurement function. (The negative linear conversion mentioned above serves to indicate high noise levels at the input to the Power Sensor. Any true input power level will cause a positive dc input to be applied to the A-D Converter.)

c. An over-range conversion is detected if the A-D qualifier does not change state before 1100 counts (> +1.26 Vdc input).

d. The Controller may cause the Instruction Decoder to execute a dB relative conversion before updating the front-panel Digital Readout indication. During the dB relative conversion, the output of the counter is changed to indicate the RF input power level with respect to a reference value stored previously (refer to Service Sheet 3).

8-84. True-Range Decoder. The function of the True-Range Decoder is to indicate the power level represented by the dc voltage at A3TP4 (DC) and, if the power level is to be displayed in dB, to preset the Main Counter to the minimum threshold of the range selected. The Power Meter has five measurement ranges. Each range covers a power of ten (1—12μW, 10—120 μW, 100 μW—1.2 mW, etc.) and slightly overlaps the previous range to prevent ambiguous measurements. The exponents assigned to the five ranges vary according to the sensitivity of the Power sensor in use. Thus, the indication displayed for any range is only relative until the sensitivity of the Power Sensor is factored in. The True-Range Decoder accomplishes this by determining the sensitivity of the Power Sensor from the Mount Resistor Input, then combining this information with the Range Select and Log Mode outputs of the Controller to address a ROM. The resulting outputs of the ROM are described in the following paragraphs.

a. True-Range Exponent: This output is provided for both linear and dB operation of the Power Meter and consists of a five-bit binary code which indicates the input power level as 10^{-X}

CIRCUIT DESCRIPTIONS

Service Sheet 2 (cont'd)

b. Watts Mode, True Range: This output is provided only for linear operation of the Power Meter (LOG Mode input inactive) and lights a front-panel lamp to indicate that the Digital Readout is in Watts (W), milliwatts (mW), microwatts (μW), or nanowatts (nW).

c. True-Range Counter and Sign Preset: This output is provided only for dB operation of the Power Meter (Log Mode input active) and presets the Main Counter to the predetermined value assigned as the starting point for the particular dB range selected. (For any A-D conversion, the Main Counter is always preset to the lowest value associated with a particular range and then counted in the direction of increasing power. When WATT Mode operation of the Power Meter is selected, the starting value for each range is ±0000. When dB mode operation of the Power Meter is selected, the starting point for each range depends on the sensitivity of the Power Sensor; e.g. for the —10 dB range the Main Counter is preset to 2000 and the sign is preset to —, for the 20 dB range, the Main Counter is preset to 1000 and the sign is preset to +).

d. Decimal Point Select: This output is provided for both linear and dB operation of the Power Meter and lights the appropriate decimal point on the Digital Readout to indicate the true sensitivity of the range selected (e.g., 1.000 mW, 10.00 mW, 20.00 dB, etc.).

8-85. Display Assembly. The Display Assembly indicates the Power Meter's operating mode and range status, and displays the sign and numeric value of the RF input power level applied to the Power Sensor. The status indications are provided via individual light emitting diode (LED) indicators that are turned on and off independently by the inputs from the Controller and the True-Range Decoder. The power level indications are displayed via numeric segment indicators (Digital Readout). The sign indiction is controlled directly by the output of the Controller. When the Display Sign — (minus) input is active, the center segment of the first indicator is lighted to display a minus (—) sign; when the input is not active, the segment is turned off to indicate a positive sign.

8-86. The numeric value indication is effected by clocking the BCD output of the Main Counter into the Display Drivers on the positive-going edge of the Display Count Strobe. The Display Drivers then convert the BCD input into a format that lights individual segments of the numeric indicators to form a decimal number. (Decimal point positioning is controlled by the Decimal Point Select output of the True-Range Decoder.) The LBLANK input to the Display Drivers is activated to blank all but the most significant digit for various under and over-range conditions. Similarly, the Display Drivers also employ a ripple blanking capability to turn off the most significant digit when it is a zero.

8-87. Service Sheet 3

8-88. General. In order to understand the operation of the circuits shown on the block diagram, it is necessary to consider Power Meter operation in terms of the operating program stored in the State Controller. As stated previously, the program is executed on a cyclic basis with one measurement taken and the results displayed per cycle. On Figure 8-15, Sheet 1, it is shown that each cycle starts when the program enters the Local/Remote Branch or Local Initialize Subroutines and ends when the program exits the Display and Remote Talk Subroutine. Between these two points in time a number of additional subroutines are executed to control circuit operation on a step-by-step basis. Each step is a two-way communication between the program and one or more circuits. The talk lines are the outputs of the Instruction Decoder, and the listen lines are the qualifier inputs to the Line Selector. To effect the communication, each step occupies two addresses to allow an either/or decision and to select the next step (refer to paragraph 8-94, Program Execution). Since the decisions are made in series, each subroutine can be viewed as a sequential logic circuit charged with the responsibility of controlling one or more operating functions.

8-89. For purposes of definition, the Power Meter operating functions can be divided into two classes, fixed and variable. Fixed functions are basic to each measurement and are performed during each cycle. Variable functions are associated with a particular mode, measurement status, etc. They are performed only when a predetermined condition is detected during execution of the program cycle. On Figure 8-15, Sheet 1, fixed functions are

CIRCUIT DESCRIPTIONS

Service Sheet 3 (cont'd)

indicated by a single-line exit from a subroutine; variable functions are indicated by multi-line exits.

8-90. For maintenance purposes, it is convenient to think of each operating function as a window that can be opened or closed at some point in the program cycle. In some cases the program opens the window for a fixed amount of time to enable the function, then closes the window to terminate that function. In other cases the program opens the window and latches a circuit to keep it open for the remainder of the cycle. This type of window is then checked at the start of each future program cycle. If the type of operation selected does not change, the circuit is relatched to keep the window open for another cycle. If the type of operation changes, the circuit is unlatched and a new circuit is latched to keep a different window open during the program cycle.

8-91. In order to understand Power Meter operation to the level required for troubleshooting, it is necessary to know exactly when, why, and how a window is opened or closed to enable or terminate an operating function. Table 8-6 is provided as an aid to this understanding. This table describes the function(s) of each address or group of addresses, and references a signal flow description which indicates how the hardware circuits operate to perform the function. To close the theory/troubleshooting loop, an additional reference is made to a checkout procedure which can be used to verfiy that the function was performed properly.

8-92. The best way to use the information in Table 8-6 is in small segments. Refer to Figure 8-15 and follow program execution starting at the Power Up Subroutine. If circuit operation is obvious, go on to the next subroutine. If it is not obvious, refer to Table 8-6 and proceed to the Block Diagram Description referenced. The Block Diagram Descriptions are written in terms of hardware operation. They summarize qualifier/instruction communication and concentrate on explaining how the instruction is processed to enable the function, and on how the qualifier is generated to indicate status. After a general understanding of hardware operation is gained, go back to Figure 8-15 and trace out the address branching required to effect the qualifier/instruction communications talked about in the Block Diagram Description. When a logic analyzer is available, each of these address branches serve as a valuable tool for troubleshooting. Overall circuit operation can be rapidly analyzed by looking at key addresses within the subroutines (refer to example provided under TROUBLESHOOTING, Table 8-3, Standard Instrument Checkout.) When the problem is isolated to a circuit, additional addresses can be selected as sync points for checking circuit operation on a step-by-step basis.

Table 8-6. Operating Program Descriptions (1 of 11)

Sub-Routine	Address	Function	Branch To	Troubleshooting Refer to	Block Diagram Description	
					Service Sheet	Title
Power Up	000	Blank Display (LSOR; UNDER RANGE or OVER RANGE indicator will light depending on whether under/over range decoder powers up in set or reset mode).	Address 001_8	Table 8-3, Step 1	2 3	Display Assembly Program and Remote Interface Circuit Initialization.
	001, 032, 033	a. Count to range counter down to range 0(LCRD)	Address 034_8	Table 8-3, Step 1	10	Range Counter
		b. Clear main counter and set sign positive (LCLR)		Table 8-3, Step 1	9	Main Counter
		c. Load contents of main counter (0000) into reference register to clear register (LLRE)		Table 8-3, Step 1	9	Reference Register
		d. Display blanked count and sign (0_ . _ _) (LTC) Note: — indicates blanked digit		Table 8-3, Step 1	6	Display Assembly
	034	a. Auto zero A-D converter for 8000 counts (LAZ, LCNT)	Address 035_8	Table 8-3, Step 1	2 3	A-D Converter, Auto-Zero Function A-D Converter Auto-Zeroing
		b. Count range counter down to range 7 (LCRD)	Address 035_8	Table 8-3, Step 1	10	N/A (Circuit Operation covered under Digital Integrated Circuits and Symbols)
	035	a. Count range counter down to range 5 (LCRD)	Local/Remote Branch Subroutine Address 026_8	Table 8-3, Step 1	10	
		b. Load mode select input into mode register (LCKM)	Local/Remote Branch Subroutine Address 026_8	Table 8-3, Step 1	3	Mode Selection
Local/ Remote Branch	026	Check whether local or remote operation is selected (Remote, 037_8)	a. Local initialize subroutine, address 052 for local operation. b. Address 042 for remote operation	Table 8-3, Step 1 Table 8-4, Error #3 (HP-IB Opt.)	3 4	Program Execution Remote Enable

Table 8-6. Operating Program Descriptions (2 of 11)

Sub-Routine	Address	Function	Branch To	Troubleshooting Refer To	Block Diagram Description	
					Service Sheet	Title
Local/ Remote Branch (cont'd)	042	Check whether free run or triggered operation is selected	a. Branch to Remote Initialize sub-routine, Address 012 for free run or if trigger is received to initiate program cycle b. 043 if trigger not received	Table 8-4, Error #3 (HP-IB Option)	3 4	Program Execution Measurement Rate Programming Command Processing
	043	Auto-zero A-D Converter one count (LAZ)	Address 026	Table 8-4, Error #3, (HP-IB Option)	2, 3	A-D Converter Auto-Zero Function
Remote Initialize	012	a. Hold range selected in previous program cycle if autoranging selected (Blank Instruction)	Address 013	Table 8-4, Error #3 (HP-IB Opt.)	3 4	Range Selection Range Programming Command Processing
		b. Load remote range select inputs into range counter if autoranging not selected (LLRA)	Address 013	Table 8-4, Error #4 and 4.5 (HP-IB Option)		
	013, 014	a. Count range counter down to range 5 if range 6 or 7 selected (LCRD)	Address 015	Not verified	3 4	Range Selection Range Programming Processing
		b. Clear main counter (LCLR)	Address 015	Table 8-4, Error #4, 4.5 & 12 (HP-IB Option)	9	N/A (Circuit Operation covered under Digital Integrated Circuits & Symbols)
	015	a. Check whether delayed or immediate measurement enabled (FAST, 035_8)	Address 016 for delayed measurement Address 101 for immediate measurement	Table 8-4, Error #3 (HP-IB Option) Table 8-4, Error #33 (HP-IB Option)	3 4	Program Execution Measurement Rate Programming Command Processing

Table 8-6. Operating Program Descriptions (3 of 11)

Sub-Routine	Address	Function	Branch To	Troubleshooting Refer To	Block Diagram Description	
					Service Sheet	Title
Remote Initialize (Cont'd)	016, 017, 030, 031	a. Determine Range (YR1, YR2, YR3)	Auto-Zero subroutine, Address 056, for range 3,4,or 5	Table 8-4, Error #11 and 12 (HP-IB Option)	3	Range Selection,
		b. Load mode select inputs into mode register	Delay subroutine, Address 036, for range 1 or 2	Table 8-4, Errors #4, 4.5 and 5 (HP-IB Option)		Mode Selection
	101, 102	a. Determine mode selected for previous program cycle	Address 104 if Watts mode was selected for previous program cycle	Table 8-4, Error #36 (HP-IB Option)	3	Mode Selection
		b. Load mode select inputs into mode register to select mode for current program cycle (LCKM)	Address 103 if Watts mode was not selected for previous program cycle	Table 8-4, Errors #3 and 33 (HP-IB Option)		
	103	a. Auto-zero A-D converter for 1000 counts (LAZ, LCNT) b. Clear main counter (LCLR)	Address 104	Table 8-4 Error #33 (HP-IB Option)	2, 3	A-D Converter Auto-Zero Function
	104	a. Auto-zero A-D converter for 1000 counts (LAZ, LCNT) b. Clear main counter (LCLR)	Measurement Subroutine Address 061	Table 8-4, Error #33 (HP-IB Option)	2, 3	A-D Converter Auto-Zero Function
Local Initialize	052, 053, 054, 055	a. Count range counter down to range 5 if range 0, 6, or 7 is selected (LCRD) b. Load mode select inputs into mode register	Auto-Zero Subroutine, Address 056	Table 8-3, Step 1 (range 5 branch) Step 14 (range 3 branch) Step 19 (range 1 branch) Step 24 (mode register loaded)	3	Range Selection, Mode Selection

Table 8-6. Operating Program Description (4 of 11)

Sub-Routine	Address	Function	Branch To	Troubleshooting Refer To	Block Diagram Description	
					Service Sheet	Title
Auto-Zero Subroutine	056	Clear main counter (LCLR)	Address 057	Table 8-3, Step 1	2, 3	A-D Converter Auto-Zero Function
	057	a. Auto-zero A-D converter for 8000 Counts (LAZ, LCNT) b. Clear main counter (LCLR)	Measurement Subroutine Address 061			
Measurement Subroutine	061, 062	a. Load dc input voltage into A-D converter for 2000 counts (LINP, LCNT) **NOTE** *Ramp charges to −7.09 times dc input.* b. Clear main counter (LCLR)	Address 063	Table 8-3, Step 1	2, 3	A-D Converter Measurement Function
	063, 064	a. Check mode selected b. Load outputs for true-range decoder into sign detector and main counter if dBm, dB [REF], or dB (REL) mode selected.	Address 065 for WATT mode Address 066 for dBm dB [REF] or dB (REL) mode	Table 8-3, Step 1 Table 8-3, Step 24 (dBm mode) Step 32 (dB [REF] mode)	3 3	Mode Selection A-D Converter Log Conversion
	065, 037	a. Check whether A-D ramp has changed to negative or positive dc input b. Load outputs of true-range decoder (−sign, 0000 count) into sign detector and main counter (LPSC) if dc input was negative, indicating negative power (noise) input c. Enable A D ramp positive-conversion slope (LRMP) is dc; input was positive	Linear Negative Conversion Subroutine, Address 076, for negative dc input Linear Positive Conversion Subroutine, Address 071, for positive dc input	Table 8-3, Step 10 Table 8-3, Step 1	2, 3	A-D Converter Linear Conversion
	066, 051, 107	a. Check whether dc input is under range (A-D ramp input slope does not exceed log threshold) b. Light UNDER RANGE lamp (LSUR) and blank display (LSOR) if dc input under range	Under Range Subroutine, Address 174 if dc input under range Log Conversion Subroutine, Address 136 if dc input not under range	Table 8-3, Step 24 Table 8-3, Step 25	2, 3	A-D Converter Log Conversion

Table 8-6. Operating Program Description (5 of 11)

Sub-Routine	Address	Function	Branch To	Troubleshooting Refer To	Block Diagram Description	
					Service Sheet	Title
Measurement Subroutine (cont'd)	066, 051, 107 (cont'd)	c. Enable A-D ramp log-conversion slope (LRMP) if dc input not under range.				
Linear Positive-Conversion Subroutine	067, 071, 072, 073, 074, 075	a. Enable linear positive-conversion ramp (LRMP) and count main counter up on every other clock pulse (LCNT) b. Check A-D converter output qualifier prior to each count to detect under-range, in-range or over-range condition c. Detect under-range (address 067) if A-D converter output qualifier changes state before main counter is counted up 100 counts d. Detect in-range condition (address 072 or 074) if A-D converter output qualifier changes state between 100 and 1199 counts e. Detect over-range condition (address 075) if A-D converter output qualifier does not change state before 1200 counts f. Clear over/under range decoder (LCOR)	Under-Range Subroutine Address 174 if <100 counts Display and Remote Talk Subroutine Address 177, if between 100 and 1199 counts Over Range Subroutine, Address 147, if 1200 counts	Table 8-3, Step 7 Table 8-3, Step 1 (addresses 071, 067, 072, 073) Step 3 (addresses 074, 075) Step 6 (address 074 LCOR instruction Table 8-3, Step 5	2, 3	A-D Converter Linear Conversion
Linear Negative-Conversion Subroutine	076 077, 130, 131, 132, 133	a. Enable linear negative conversion ramp (LRMP) and count main counter up on every other clock pulse (LCNT) b. Check A-D Converter output qualifier prior to each count to detect under-range, in-range or over-range condition c. Detect under range (address 077) if A-D converter output qualifier changes before main counter is counted up to 100 counts.	Under Range Subroutine Address 174 if < 100 counts Display and Remote Talk Subroutine, Address 177, if between 100 and 1199 counts	Table 8-3, Step 10 (addresses 076, 130, 077) Table 8-3, Step 38 (addresses 130, 131) Steps 39 and 42 (addresses 131, 132, 133) Step 41 (address 131, LCOR instruction	2, 3	A-D Converter Linear Conversion

Table 8-6. Operating Program Description (6 of 11)

Sub-Routine	Address	Function	Branch To	Troubleshooting Refer To	Block Diagram Description	
					Service Sheet	Title
Linear Negative-Conversion Sub-routine (cont'd)		d. Detect in range condition (address 131 or 133) if A-D converter output qualifier changes between 100 and 1199 counts. e. Detect over range condition (address 134) if A-D converter output qualifier does not change state before 1200 counts f. Clear over/under range decoder (LCOR)	Over Range Sub-routine, address 147 if 1200 counts	Table 8-3, Step 40		
Log Conversion	135, 136, 137, 150, 151, 152, 153, 154, 155, 156, 157, 160, 161, 162, 163, 164, 165, 166, 167	**NOTE** *For log (dB) conversion, the main counter can be preset to a negative number and counted down, or it can be preset to a positive number and counted up. In addition, if the output of the main counter reaches 0000 when it is being counted down, a borrow pulse is generated to change the direction of counting. The count decoding of this subroutine is such that an in-range measurement is detected whenever the A-D converter output qualifier changes state before 1100 clocks are applied to the main counter regardless of the direction of counting.*			2, 3	A-D Converter Log Conversion
		a. Enable log-conversion ramp (LRMP) and count main counter up or down on every other clock pulse (LCNT)		Table 8-3, Step 25 (address 135)		
		b. Check A-D converter output qualifier prior to each count to detect in-range or over-range condition	dB Relative Sub-routine, address 170, if <1100 counts	Table 8-3, Step 26 (address 135, 136 137, 150, 151, 152)		
		c. Detect in-range condition (address 135, 137, 151, 153, 155, 157, 161, 165), if A-D Converter output qualifier changes state before 1100 counts	Over range sub-routine, address 147, if >1100 counts	Step 27 (address 153, 154) Step 28 (address 155, 156, 157, 160, 161, 162, 163, 164, 165)		

Table 8-6. Operating Program Description (7 of 11)

Sub-Routine	Address	Function	Branch To	Troubleshooting Refer to	Block Diagram Description	
					Service Sheet	Title
Log Conversion (cont'd)		d. Detect over-range condition (address 164 or 167) if A-D converter output does not change state by 1100 counts e. Clear over/under-range decoder (LCOR		Step 31 (addresses 163, 164 165, 166, 167)		
Relative dB	170	Check whether dBm mode selected	Display and Remote Talk Subroutine, Address 177, if dBm mode selected	Table 8-3, Step 25	3	Mode Selection
			Address 171 if dBm mode not selected	Table 8-3, Step 32		
	171,172, 141, 173	a. Store contents of main counter in reference register (LLRE) if dB [REF] mode selected b. Load contents of reference register into relative counter (LCOR) and set NRZO qualifier logic 1 c. Count relative counter down (LREL) to 0000 (NRZO=0) and count main counter up or down (LCNT) as required to algebraically subtract reference from measured power level.	Display and Remote Talk Subroutine Address 177	Table 8-3, Step 32 (except address 171, YMI branch) Step 33 (address 171, YM1 branch)	3	dB Relative Conversion
Under-Range	174,175	Light UNDER RANGE lamp (LSUR) if measurement was taken on ranges 2 through 5	Address 176 if measurement was taken on ranges 2 through 5	Table 8-3, Step 7 (range 5) Step 15 (range 3)	2	Display Assembly
			Over/Under Range Continue Subroutine Address 047 if measment was taken on ranges 0 or 1	Table 8-3, Step 20	3	A-D Converter Linear Under-Range Conversion A-D Converter Log Under-Range Conversion Range Selection
	176	Blank display (LSOR) if auto-ranging enabled	Address 105 if auto ranging enabled	Table 8-3, Step 8		
			Over/Under Range Continue Subroutine Address 047 if auto-ranging not enabled	Table 8-3, Step 7		

Table 8-6. Operating Program Description (8 of 11)

Sub-Routine	Address	Function	Branch To	Troubleshooting Refer To	Block Diagram Description	
					Service Sheet	Title
Under-Range (cont'd)	105	Count range counter down one range (LCRD)	Auto Zero Subroutine Address 056 if measurement was taken on range 4 or 5	Table 8-3, Step 8		
			Delay Subroutine, Address 036, if measurement was taken on range 2 or 3	Table 8-3, Step 15		
Over-Range	147	Blank Display (LSOR)	Over/Under Range Continue Subroutine, Address 047, if auto-ranging is not enabled	Table 8-3, Step 5 (LSOR instruction) Step 6 (branch to address 047)	2 3	Display Assembly A-D Converter Linear Over-Range Conversion
			Address 146 if auto-ranging is enabled	Table 8-3, Step 9		
	145, 146	Count range counter up one range if measurement was taken on range 2, 3, or 4	Auto-Zero Subroutine, Address 056, if measurement was taken on range 0 2, 3, or 4	Table 8-3, Step 9 (range 4) Step 22 (range 2)		A-D Converter Log Over-Range Conversion
			Address 143 if measurement was taken on range 0, 1 or 5	Table 8-3, Step 21		Range Selection
	143	Count range counter up one range if measurement was taken on range 1	Delay Subroutine, Address 036, if measurement was taken on range 1.	Table 8-3, Step 21		
			Over/Under Range Continue Subroutine, Address 047, if measurement was taken on range 5	Table 8-3, Step 36		
Over/Under Range Continue	047	Clear main counter (LCLR) if dB [REF] or dB (REL) mode selected	Display and Remote Talk Subroutine Address 177, if Watt or dBm Mode Selected	Table 8-3, Step 6	3	dB Relative Conversion
			Address 040 if dB [REF] or dB (REL) mode selected	Table 8-3, Step 36		
	050	Load contents of main counter into reference register (LLRE) if dB [REF] mode selected	Display and Remote Talk Subroutine, Address 177	Table 8-3, Step 36 (dB (REL) mode) Step 37 (dB [REF mode)		

Table 8-6. Operating Program Description (9 of 11)

Sub-Routine	Address	Function	Branch To	Troubleshooting Refer To	Block Diagram Description	
					Service Sheet	Title
Delay	036, 127, 113, 116, 117, 115	Auto-Zero A-D Converter for 666 ms (main counter is cleared by LCLR instruction, auto-zeroing is enabled by LAZ and LCNT instructions. Auto zero period is 8000 counts for each address) **NOTE** *This subroutine is associated with range 1 and 2 measurements. It essentially serves as a program pause to allow the output of the variable low-pass filter to settle.*	Address 006	Table 8-3, Step 15	2 2, 3	Amplifier, Demodulator & Filter Circuits A-D Converter Auto-Zero Function
	006	Check whether local or remote operation is enabled (REMOTE 37_8)	Auto-Zero Subroutine, Address 056 for local operation Address 120 for remote operation	Table 8-3, Step 15	3 4 5	Program Execution Remote Enable General Description
	120	Check whether immediate or delayed measurement is enabled	Auto-zero subroutine, Address 056 for immediate measurement Address 123 for delayed measurement		3 4 5	Program Execution Measurement Rate Programming Command Processing Measurement Rate Programming, Remote Qualifier/ Program Interface and Talk Cycle
	123, 122	Auto-zero A-D Converter for 267 ms (main counter is cleared by LCLR instruction; auto-zeroing is enabled by LAZ and LCNT instructions. Auto-zero period is 8000 counts for each address)	Auto-Zero subroutine, address 056	Table 8-4, Errors # 4, and 4.5 (HP-IB Option) Table 8-5, Step 3 (BCD Option)	2, 3	A-D Converter Auto-Zero Function
Display and Remote Talk	177	Transfer count and sign to front panel display and inform remote interface circuits that measurement completed (LTC)	Address 022	Table 8-3 Step 1	2 2, 3	Display Assembly True-Range Decoder A-D Converter Linear Conversion A-D Converter Log Conversion

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Table 8-6. Operating Program Description (10 of 11)

Sub-Routine	Address	Function	Branch To	Troubleshooting Refer To	Block Diagram Description	
					Service Sheet	Title
Display and Remote Talk (cont'd)	022	Auto-zero A-D converter for one count (LAZ)	Address 023	Table 8-3, Step 2	2, 3	A-D Converter Auto-Zero Function
	023	Check whether remote talk selected (TALK 32_8)	Address 024 if remote talk not selected.	Table 8-3, Step 2	3 4	Program Execution Talk Cycle
			Address 044 if remote talk selected		5	Measurement Rate, Programming, Remote Qualifier/ Program Interface, and Talk Cycle
	024	Check whether free-run or triggered operation is selected (HOLD 036_8)	Local/Remote Branch Subroutine, Address 026, for free-run or if trigger is received to initiate new program cycle	Table 8-3, Step 2	3 4	Program Execution Measurement Rate Programming Command Processing
			Address 025 if trigger is not recieved	Table 8-4, Errors #4 and 4.5 (HP-IB Option); (N/A for BCD Option)	5	Measurement Rate Programming, Remote Qualifier/ Program Interface, and Talk Cycle
	025	Check whether local or remote operation is selected (REMOTE 037_8)	Local Initialize Subroutine, Address 052 for local opertion	Not Verified	3 4	Program Execution Remote Enable
			Address 022 for remote operation	Table 8-4, Error #3 (HP-IB Option) (N/A for BCD Option)	5	General Description
	044	Check whether remote listener ready for data (RFDQ, 34_8)	Address 022 if remote listener not ready for data	Table 8-4, Error #1 (HP-IB Option); (N/A for BCD Option)	3 4 5	Program Execution Talk Cycle Measurement Rate Programming, Remote Qualifier/ Program Interface and Talk Cycle
			Address 045 if remote listener ready for data			
	045	Check whether data accepted line set (DACQ, 31_8)	Local/Remote Branch Subroutine Address 045, if line set	Not Verified	3 4	Program Execution Talk Cycle
			Address 046 if line reset	Table 8-4, Error #1 (HP-IB Option) Table 8-5, Step 2 (BCD Option)	5	Measurement Rate Programming, Remote Qualifier/ Program Interface and Talk Cycle

Table 8-6. Operating Program Description (11 of 11)

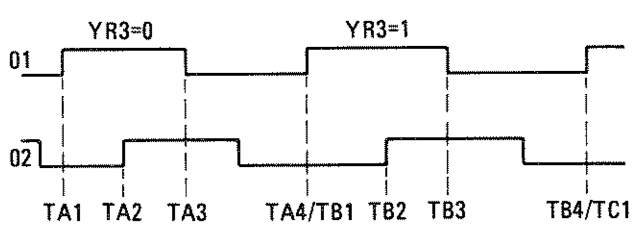
Sub-Routine	Address	Function	Branch To	Troubleshooting Refer to	Block Diagram Description	
					Service Sheet	Title
Display and Remote Talk (cont'd)	046	Set data valid line to enable output data transfer (LSDAV)	Address 110	Table 8-4, Error #1 (HP-IB Option) Table 8-5, Step 2 (BCD Option)	3 4 5	Program Execution Talk Cycle Measurement Rate Programming, Remote Qualifier/ Program Interface and Talk Cycle
	110	Check whether data accepted line set to indicate data received OK (DACQ, 31_8)	Address 111 if data accepted	Table 8-4, Error #1 (HP-IB Option) Table 8-5, Step 2 (BCD Option)	3 4 5	Program Execution Talk Cycle
			Address 106 if data not accepted	Table 8-5, Step 3 (BCD Option) (N/A for HP-IB Option)		
	106	Auto-zero A-D converter one count (LAZ)	Address 110	Table 8-5, Step 3 (BCD Option); (N/A for HP-IB Option)	2	Analog-to-Digital Converter Auto-Zero Function
	111	Reset data valid line to indicate data transferred (LSDAV)	Address 112	Table 8-4, Error #1 (HP-IB Option) Table 8-5, Step 3 (BCD Option)	3 4 5	Program Execution Talk Cycle Measurement Rate Programming, Remote Qualifier/ Program Interface, and Talk Cycle
	112	Check whether Power Meter has more data for remote listener (MORE DATA 33_8)	Address 110 if more data	Table 8-4, Error #1 (HP-IB Option) (N/A for BCD Option)	3 4 5	Program Execution Talk Cycle Measurement Rate Programming, Remote Qualifier/ Program Interface, and Talk Cycle
			Local/Remote Branch Subroutine Address 026 if no more data	Table 8-4, Error #2 (HP-IB Option) Table 8-5, Step 3 (BCD Option)		

CIRCUIT DESCRIPTIONS

8-93. Program and Remote Interface Circuit Initialization. When power is turned on, a Master Reset (LPU) is generated by the Power Up Detector to select local operation of the Power Meter (refer to Service Sheets 4 and 5) and to initialize the operating program to power up address 000_8. If the Power Meter is subsequently configured for remote operation and a device clear input is received, the remote interface circuits also generate a power up reset. The power up reset output of the Remote Interface Circuits reinitializes the operating program to power up address 000_8 but it does not terminate remote operation. Instead, it presets the Remote Interface Circuits to select the following operating conditions: WATT MODE, Range 6 (counted down to range 5 before measurement), Autoranging enabled, CAL FACTOR % switch disabled.

8-94. Program Execution. The operating program consists of a group of 16-bit data words stored in the State Controller. The words are designated by address with 000_8 being the lowest address and 377_8 being the highest address. As stated previously, a power up reset signal (LPU) is generated by the Controller when power is turned on to initialize the program to starting address 000_8. From then on the program is self-executing with branching between the words being controlled by the Power Meter operating conditions detected. Thus, the program is essentially a sequential logic circuit which interfaces with the Power Meter hardware circuits to control their operation. General processing of the operating program by the Controller is illustrated in Figure 8-15, Sheets 2 and 3. In the following examples, specific words are used to illustrate Controller circuit operation associated with local and remote qualifier selection.

A. Example 1. Local Qualifier Selection; Starting Address 000_8.



	Qualifier Select Code	Instruction Select Code	Next Address Select Code
BIT	15 14 13 12	11 10 9 8 7	6 5 4 3 2 1 0
Word 000_8	X X X X	1 0 1 0 1	0 0 0 0 0 0 1
	No qualifier associated with word 000_8	05_8 (LSOR)	001_8

1. TA1 — Leading edge of first 01 Clock following termination of Power Up Reset (LPU).

   a. Address 001_8 clocked into State Register and applied to State Controller.

   b. State Controller produces word 001_8:

	Qualifier Select Code	Instruction Select Code	Next Address Select Code
BIT	15 14 13 12	11 10 9 8 7	6 5 4 3 2 1 0
Word 001_8	1 0 1 1	0 1 1 0 1	0 0 1 1 0 1 0
	13_8(YR3)	15_8 (LCLR)	032_8

   c. Line Selector produces qualifier 13_8 (YR3).

2. TA2.

   a. YR3 qualifier (logic 1) clocked into Qualifier Register and applied to State Controller (State Controller address changed to 201_8). Qualifier Register not clocked again until TB2.

   b. State Controller produces word 201_8.

	Qualifier Select Code	Instruction Select Code	Next Address Select Code
BIT	15 14 13 12	11 10 9 8 7	6 5 4 3 2 1 0
Word 201_8	1 0 1 1	0 1 0 0 0	0 0 0 0 0 0 1
	13_8 (YR3)	10_8(LCRU)	$(001_8+Q=1) = 201_8$

3. TA3 — Instruction Decoder enabled; LCRU instruction generated to count down Range Counter.

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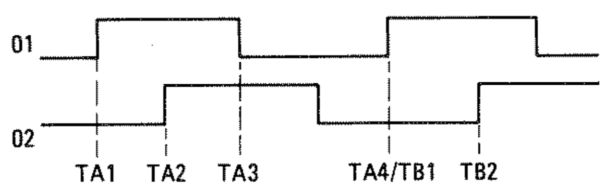
Service Sheet 3 (cont'd)

4. TA4/TB1
   a. Address 001 clocked into State Register and applied to State Controller.
   b. Qualifier Register output still high (logic 1) so State Controller produces word 201_8.
5. TB2
   a. YR3 qualifier (logic 0) clocked into Qualifier Register and applied to State Controller. Qualifier Register not clocked again until TC2.
   b. State Controller produces word 001_8.
6. TB3 — Instruction Decoder enabled; LCLR instruction generated to clear Main Counter.
7. TB4/TC1
   a. Address 032_8 clocked into State Register and applied to State Controller (A=logic 0).
   b. State Controller produces word 032_8.
8. TC2/TC3, etc. — Cycle continues as described in steps 1 through 7.

B. Example 2. Remote Qualifier Selection; Starting Address 035_8

	Qualifier Select Code				Instruction Select Code					Next Address Select Code						
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 035_8	1	0	1	0	0	1	0	1	1	0	0	1	0	1	1	0
	12_8 (YR2)				13_8 (LCKM)					$(026_8 + Q=0) = 026_8$						



1. TA1
   a. Address 026_8 clocked into State Register and applied to State Controller.
   b. Qualifier Register output is logic 0, so State Controller produces word 026_8.
   c. Remote Qualifier (YRMT) is input to Line Selector via Multiplexer in Remote Interface Circuits. When Instruction Code 30_8 through 37_8 and Qualifier Select Code is 17_8, Instruction Decoder is disabled and Remote Qualifier is applied to State Controller via Line Selector.
2. TA2
   a. Remote Qualifier clocked into Qualifier Register and applied to State Register.
   b. If qualifier is low (logic 0), State Controller continues to output word 026_8; if qualifier is high (logic 1), then word 226_8 is produced.

	Qualifier Select Code				Instruction Select Code					Next Address Select Code						
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 226_8	X	X	X	X	1	1	1	1	1	0	1	0	1	0	1	0
					37_8					$(052_8 + Q=1) = 252_8$						

3. TA3 — No operation, Instruction Decoder disabled by Instruction Select Code.
4. TA4/TB1
   a. Next Address Select Code locked into State Register.
   b. State Controller produces word 042_8 or 252_8.
5. TB2, etc. — Cycle repeated as described in steps 1 through 4.

8-95. As illustrated in the examples, the operating program is not addressed in numerical order. To simplify the understanding of how the program causes the circuits to operate, Figure 8-15 is arranged so that all of the words associated with a particular function are grouped together and designated a subroutine. After the power up subroutine is completed, a complete program cycle is executed for each measurement. The cycle is considered to start at the Local Initialize or Local/Remote Branch subroutine and to end at the Display and Remote Talk Subroutine. (When auto-ranging is enabled and an out-of-range measurement is obtained, a measurement sub-loop is enabled to prevent completion of the program

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Service Sheet 3 (cont'd)

cycle until an in-range measurement is obtained on any range, or an out-of-range measurement is obtained on the last range.) When local operation is selected, the program is allowed to free run and measurements are taken asynchronously to changes in the RF input power level. When remote operation is selected, an additional capability is provided to enable the start of each program cycle to be triggered by an external input. Thus, for remote operation, measurements can be taken synchronously or asynchronously to changes in the RF input power level.

8-96. Mode Selection. The Mode Select inputs are applied to the Controller in a "WIRED OR" configuration to enable either Local or Remote mode selection. When the Power Meter is configured for Local Operation, the Remote Enable input to the Pushbutton Switch Assembly is high and the Mode Select outputs of the Remote Interface Circuits are set to the logic 1 (+5V) state. Thus, the Pushbutton Switch Assembly is enabled to select the operating mode for the Power Meter. When the Power Meter is configured for remote operation, the Remote Enable input is low, the outputs of the Pushbutton Switch Assembly are held at logic 1, and the Mode Select outputs of the Remote Interface Circuits select the operating mode of the Power Meter.

8-97. The Mode Select inputs (IYM1 and IYM2) are coded as indicated below to select the operating mode of the Power Meter. These inputs are clocked into the Mode Register at the start of each program cycle by the LCKM output of the Instruction Decoder. The resultant outputs of the Mode Register are then gated together for the duration of the program cycle to provide the following signals as required to implement the operating mode selected.

Mode	IYM2	IYM1
WATT	1	0
dB (REL)	0	1
dB [REF]	0	0
dBm	1	1

a. Mode Qualifiers. These outputs are coded as listed above to indicate the operating mode selected. They are accessed at various points in the program cycle to control program branching and/or instruction generation.

b. dBm Mode Selected. When the dBm Mode is selected, this output is active and lights the front-panel dBm indicator.

c. Log Mode and YLog. These outputs are active when either the dBm, dB [REF], or dB (REL) Mode is selected. The Log Mode signal forms part of the address applied to the True-Range Decoder. The YLOG signal is gated with other inputs by the Up/Down Count Control Logic to control the direction in which the Main Counter counts when enabled by the Controller.

d. Mode Bits 1 and 2. Mode Bits 1 and 2 are coded as listed previously to indicate to the Remote Interface Circuits which operating mode is selected for the Power Meter. Additionally, the NM2 signal is also applied to the Display Assembly to light the dB (REL) indicator when the dB Relative Mode is selected.

8-98. When the front-panel SENSOR ZERO switch is pressed, the NZR input to the Auto-Zero Timer enables the Sensor Zero output to be activated for a period of approximatley four seconds. While this signal is active it overrides the Mode Select inputs to the Buffers and sets the IYM2 and the IYM1 outputs to 1 and 0, respectively. Thus if the Power Meter was not configured for Watts Mode operation when the SENSOR ZERO switch was pressed, Watts operation will be enabled at the start of the first program cycle after the Sensor Zero signal is activated. The Power Meter will then return to the operating mode selected by the Mode Select inputs at the start of the first program cycle following termination of the Sensor Zero signal. While the Sensor Zero signal is active, the remaining outputs of the Buffers are active and provide the following functions:

a. Sensor Auto-Zero Enable. This output is applied to the Auto-Zero circuits to close the feedback loop to the Power Sensor.

b. Sensor Auto-Zero Status. This output is applied to the Display Assembly to light the ZERO indicator.

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Service Sheet 3 (cont'd)

c. RF Blanking. This output is available at a rear panel connector for suppression of an external instrument's RF output.

8-99. Range Selection. The Auto-Range Qualifier input is applied to the Controller in a "WIRED OR" configuration to enable local or remote control of this function (Remote Enable line high or low, respectively). When this input is low, the operating program is enabled to count the Range Counter up (LCRU instruction) or down (LCRD instruction) as required to obtain an in-range measurement. When the input is high, the operating program is inhibited from changing the range upon detection of an under-range or an over-range condition. Thus, for local operation a high Auto-Range Qualifier input causes the Power Meter to hold the last range previously selected in the Power Up Subroutine or during execution of the operating program. For remote operation, a high Auto-Range Qualifier input causes the Remote Range Select inputs to be loaded into the Range Counter at the start of each program cycle to select a specific range for each measurement.

8-100. In addition to checking the Auto-Range Qualifier at various points in the program cycle, the operating program also checks for an invalid range selection at the start of each cycle. When remote operation is selected, ranges 6 and 7 are considered invalid; when local operation is selected, range 0 is also considered invalid. Upon detection of an invalid range, the operating program generates LCRD instructions as required to count the Range Counter down to range 5.

8-101. A-D Converter Auto-Zero Function. The Controller and Main Counter operating cycle associated with auto-zeroing the A-D Converter is described in the following paragraphs.

a. The Controller first generates an LCLR instruction to set the output of the Main Counter to 0000 and to store a positive sign in the Sign Latch (YSPL high, NSPL low).

b. The Controller then generates LAZ and LCNT instructions on the trailing edge of every 01 Clock Pulse while monitoring the Count Qualifier outputs of the Main Counter. The LCNT instructions are processed by the Up/Down Count Control Logic as indicated in Table 8-7 to provide Up Clock outputs to the Main Counter. The LAZ instructions are clocked into the A-D Control Register by the HPLS 2 clock, thereby maintaining a continuous LAZO output to the A-D Converter.

c. When the Count Qualifier outputs equal a predetermined value stored in the operating program, the Controller terminates the LAZ and LCNT instructions and generates an LCLR instruction. The LCLR instruction returns the output of the Main Counter to 0000 and stores a positive sign in the Sign Latch (YSPL high; NSPL low). The absence of the LAZ instruction causes the HPLS 2 clock pulse to reset the LAZO output of the A-D Control Register, thereby terminating the Auto-Zero function.

8-102. A-D Converter Measurement Function. The Controller and the Main Counter operating cycle associated with the measurement function is the same as described before for the Auto-Zero Function except that an LINP instruction is generated in lieu of an LAZ instruction. The LINP instruction enables the LRIN output of the A-D Control Register. This output is then maintained for 33.32 mS (Main Counter is counted up to 2000) to allow the A-D ramp to charge to −7 times the dc input volage.

8-103. A-D Converter Linear Conversion. An A-D converter linear conversion is enabled following the measurement function when the Power Meter is configured for WATT MODE operation. The Controller and Main Counter operating cycle associated with a linear conversion is described in the following paragraph.

a. The Controller checks the A-D Converter qualifier to ascertain whether it represents a positive or negative input power level. (A negative power level indicates a high noise condition at the input to the Power Sensor). If it represents a negative power level, an LPSC instruction is generated to load the True-Range Counter and Sign Preset inputs into the Main Counter and Sign Latch, respectively. For WATT MODE operation these inputs are such that the output of the Main Counter remains at 0000 and the output of the Sign Latch changes to indicate a negative sign.

Table 8-7. Up/Down Count Control Logic Steering

Function	Inputs to Up/Down Count Control Logic							Output	Notes
	LCNT	LREL	YLOG	YSPL	NSPL	YSPL-Ref	NSPL Ref		
A-D Converter Auto-Zeroing and DC Input Loading	Pulse	High	X	High	X	X	X	Up Clock	1
A-D Converter Linear Conversion	Pulse	X	Low	X	X	X	X	Up Clock	1
A-D Converter dB Conversion	Pulse	High	High	High	X	X	X	Up Clock	1, 2
	Pulse	High	High	Low	X	X	X	Down Clock	1,2
Counter dB Rel Conversion	Pulse	Pulse	High	High	Low	High	Low	Up Clock	3
	Pulse	Pulse	High	High	Low	Low	High	Down Clock	3
	Pulse	Pulse	High	Low	High	High	Low	Down Clock	3
	Pulse	Pulse	High	Low	High	Low	High	Up Clock	3

NOTES:

1. *X indicates don't care.*
2. *Main Counter is always preset to minimum threshold of range selected (−20.00 dBm, +10.00 dBm, etc.) and counted in direction of increasing power. Thus, if Sign Latch is preset positive, Main Counter is counted up; if Sign Latch is preset negative, Main Counter is counted down. If Main Counter is counted through 0000 Borrow output toggles Sign Latch thereby causing output and count direction to reverse.*
3. *The purpose of the dB Relative function is to indicate an input power level with respect to a reference value stored in the Reference Register. This function is effected as follows:*
   a. *First the dB value of the RF input power level is acquired via an A-D conversion.*
   b. *The reference number stored in the Reference Register is loaded into the Relative Counter.*
   c. *The Relative Counter is counted down to 0000.*
   d. *The sign of the stored reference is compared with the sign of the RF input power level. If the signs are the same the Main Counter is counted down to "subtract" the reference value from the measured value; if the signs are not the same, the Main Counter is counted up to "add" the reference value to the measured value.*
   e. *If the Main Counter is counted down through 0000, the Borrow output resets the Sign Latch and the count direction is reversed.*
   f. *When the Relative Counter output is 0000, the Main Counter output indicates the measured value with respect to the stored reference.*

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Service Sheet 3 (cont'd)

b. The Controller then monitors the count and A-D qualifier inputs while generating an LRMP instruction on the negative alternation of every 01 clock pulse and an LCNT instruction on the negative alternation of every other 01 clock pulse. The LCNT instructions are processed by the Up/Down Count Control Logic as indicated in Table 8-7 to provide up clock inputs to the Main Counter. The LRMP instructions are clocked into the A-D Control Register by the HPLS 2 clock, thereby providing a continuous Ramp Enable output to the A-D Control Gates. This signal is then gated with the outputs of the Sign Latch and the YLOG signal to provide a continuous LRP output when the sign of the input power level is positive, and a continuous LRM output when the sign of the input power level is negative.

c. The continuous LRP or LRM input causes the A-D ramp to be discharged at a constant rate. If the ramp discharges through threshold in less than 0100 counts, an under-range condition is detected. If the ramp does not reach threshold by 1200 counts, an over-range condition is detected. If the ramp reaches threshold between these two points in time, an in-range condition is detected.

8-104. A-D Converter Linear Under-Range Registration. Registration of a linear under-range conversion is described in the following paragraphs.

a. The LRMP instruction is disabled, causing the HPLS 2 clock to reset the LRP or LRM output of the A-D Control Register and gates. With this signal reset, the LRP or LRM output of the A-D Control Gates is disabled, thereby terminating the conversion.

b. The LCNT instruction is also terminated to "freeze" the number in the Main Counter.

c. An LCOR instruction is generated to reset the outputs of the Over/Under Range Decoder.

d. If the measurement was taken on range 1, and LTC instruction is generated to transfer the output of the Sign Latch to the Sign Display Indicator via the Display Sign Latch, to load the output of the Main Counter into the Display Registers, and to indicate to the Remote Interface Circuits that the measurement is completed.

e. If the measurement was taken on ranges 2 through 5 with Auto-Ranging disabled, an LSUR instruction is generated prior to the LTC instruction to enable the UR LED and HUR status outputs of the Over/Under Range Decoder. The UR LED output lights the front-panel UNDER RANGE indicator. The HUR output is gated with the HOR output by the Remote Interface Circuits to provide one of four possible status outputs to the Remote Interface Control Circuit.

f. If the measurement was taken on ranges two through five with Auto-Ranging enabled, an LTC instruction is not generated. Instead, an LSOR instruction is generated to enable the LBLANK output of the Over/Under Range Decoder and thus blank the front panel display. (An LCOR instruction resets all outputs of the Over/Under Range Decoder. An LSOR instruction enables the LBLANK, HOR, and OR LED outputs. An LSUR instruction enables the HUR and UR LED outputs and resets the OR LED output; it does not affect the LBLANK or HOR outputs. The Over/Under Range Decoder outputs are not processed by the Remote Interface Circuits until an LTC instruction is generated.) Following the LSOR instruction, and LCRD instruction is generated to count the Range Counter down one range, then another measurement is taken. This cycle is repeated until either an in range measurement is obtained, or the Range Counter is counted down to range 1. Registration of an in-range condition is accomplished the same as for a range 1 under-range condition.

8-105. A-D Converter Linear In-Range Registration. Registration of a linear in-range conversion is accomplished as previously described for an under-range, range 1 condition.

8-106. A-D Converter Linear Over-Range Registration. Registration of an over-range conversion is described in the following paragraphs.

a. The LRMP instruction is disabled, causing the HPLS 2 clock to reset the LRP or LRM output of the A-D Control Register and gates and thereby terminating the conversion.

b. The LCNT instruction is also terminated to "freeze" the number in the Main Counter.

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c. An LCOR instruction is generated to reset the outputs of the Over/Under Range Decoder.

d. If the measurement was taken on ranges 5 or on ranges one through four with Auto-Ranging disabled, an LSOR instruction is generated to enable the OR LED, HOR, and LBLANK outputs of the Over/Under Range Decoder. The OR LED output lights the front-panel OVER RANGE indicator, the LBLANK output blanks the front-panel numeric display, and the HOR output is gated with the HUR output by the Remote Interface Circuits to provide one of four status outputs to the Remote Interface Controller. After the LSOR instruction is generated, an LTC instruction is generated to transfer the output of the Sign Latch to the front-panel Sign Display Indicator via the Display Sign Latch, to load the output of the Main Counter into the Display Registers, and to indicate to the Remote Interface Circuits that the measurement is completed. Since the LBLANK output is active at this time, only the most significant digit of the Main Counter output is displayed on the front-panel.

e. If the measurement was taken on ranges one through four with Auto-Ranging enabled, an LTC instruction is not generated after the LSOR instruction. Instead, an LCRU instruction is generated to count the Range Counter up one range, then another measurement is taken. This cycle is repeated until either an in-range measurement is obtained, or the Range Counter is counted up to range five.

8-107. A-D Converter Log Conversion. A log conversion is enabled following the measurement function when the Power Meter is configured for dBm, dB [REF], or dB (REL) Mode operation. The Controller and Main Counter operating cycle associated with this conversion is described in the following paragraphs.

NOTE

An LCLR instruction is generated following the measurement function to set the output of the Main Counter to 0000, and to store a positive sign in the Sign Latch.

a. The Controller generates an LPSC instruction to load the True-Range Counter and Sign Preset outputs of the True-Range Decoder into the Main Counter and Sign Latch, respectively. As stated on Service Sheet 2, these inputs correspond to the minimum threshold of the range selected. The threshold can be either a positive or negative number (—1000, +2000, etc.) and, for any given range, it is determined by the overall sensitivity of the Power Sensor in use.

b. The Controller checks the state of the A-D qualifier input to determine whether the dc input has caused the A-D ramp to exceed the value of the log threshold. (When the YLOG input to the A-D Control Gates is active, the LLGR output is enabled to select the log threshold whenever the A-D Converter is not being auto-zeroed.) If the A-D qualifier input is 0V, indicating that the ramp has not charged through threshold, the Controller detects an under-range conversion. Registration of the under-range conversion is described below.

c. If the A-D qualifier is +5V, indicating that the ramp has charged through threshold, the Controller alternately monitors the count and A-D qualifier inputs while generating an LRMP instruction on the negative alternation of each 01 clock pulse and an LCNT instruction on the negative alternation of every other 01 clock pulse. The LCNT instructions are processed by the Up/Down Count Control Logic as indicated in Table 8-7 to provide up or down clock outputs to the Main Counter. The LRMP instructions are clocked into the A-D Control Register by the HPLS 2 clock, thereby providing a continuous ramp enable output to the A-D Control Gates. Since the YLOG input to the A-D Control Gates is also active, the gates provide a continuous LRL output along with the LLGR output to enable the log conversion slope of the A-D ramp.

d. The continuous LRL output causes the A-D ramp to be discharged at an exponential rate. If the ramp discharges through threshold in less than 1100 counts, an in-range conversion is detected. If the ramp does not reach threshold by 1100 counts, an over-range conversion is detected. Registration of in-range and over-range conditions is covered in the following paragraphs.

8-108. A-D Converter Log Under-Range Registration. Registration of a log under-range conversion is described in the following paragraphs.

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a. The Controller generates an LSUR instruction followed by an LSOR instruction to enable the UR LED, HUR, HOR, and LBLANK outputs of the Over/Under Range Decoder. The UR LED output lights the front-panel UNDER RANGE indicator and the LBLANK output blanks the front-panel display. The HUR and HOR outputs are gated together by the Remote Interface Circuits to provide one of four possible status outputs to the Remote Interface Controller.

b. If the measurement was taken on ranges 2 through 5 with Auto-Ranging enabled, and LCRD instruction is generated to count the Range Counter down one range, then another measurement is taken. This cycle is repeated until an in-range measurement is obtained or the Range Counter is counted down to range 1.

c. If the measurement was taken on range 1, or on ranges 1 through 5 with Auto-Ranging disabled, an LCRD instruction is not generated to count the Range Counter down. Instead, the Mode Qualifier Bits are checked to determine whether dBm, dB (REL), or dB [REF] operation is selected. If dBm operation is selected, an LTC instruction is generated to transfer the output of the Sign Latch to the front-panel Sign Indicator via the Display Sign Latch, to load the output of the Main Counter into the Display Registers, and to indicate to the Remote Interface Circuits that the measurement is completed. If dB (REL) operation is selected, an LCLR instruction is generated prior to the LTC instruction to set the output of the Main Counter to 0000. If dB [REF] operation is selected, an LLRE isntruction is generated after the LCLR instruction and before the LTC instruction to load the 0000 output of the Main Counter into the Reference Register, thereby clearing any reference value previously stored. (Refer to the paragraph dB (REL) Conversion.)

8-109. A-D Converter In-Range Registration. Registration of an in-range conversion is described in the following paragraphs.

a. The LRMP instruction is terminated, causing the HPLS 2 clock to reset the LRMP output of the A-D Control Register. With this signal reset, the LRL output of the A-D Control Gates is disabled, thereby terminating the conversion.

b. The LCNT instruction is also terminated to "freeze" the number in the Main Counter.

c. An LCOR instruction is generated to reset the outputs of the Under/Over Range Decoder.

d. The Mode Qualifier Bits are checked to determine whether dBm, dB (REL), or dB [REF] operation is selected. If dBm operation is selected, an LTC instruction is generated to transfer the output of the Sign Latch to the front-panel Sign Indicator via the Display Sign Latch, to load the output of the Main Counter into the Display Registers, and to indicate to the Remote Interface Circuits that the measurement is completed. If dB [REF] or dB (REL) operation is selected, a relative dB conversion is performed as described below before the LTC instruction is generated.

8-110. A-D Converter Log Over-Range Registration. Registration of an over-range conversion is described in the following paragraph.

a. The LRMP instruction is terminated, causing the HPLS 2 clock to reset the LRMP output of the A-D Control Register. With this signal reset, the LRL output of the A-D Control Gates is disabled, thereby terminating the conversion.

b. The LCNT instruction is also terminated to "freeze" the number in the Main Counter.

c. An LCOR instruction is generated to reset the outputs of the Over/Under Range Decoder.

d. If the measurement was taken on range 1 through 4 with Auto-Ranging enabled, an LCRU instruction is generated to count the Range Counter up one range, then another measurement is taken. This cycle is repeated until an in-range measurement is obtained or the Range Counter is counted up to range 5.

e. If the measurement was taken on range 5, or on ranges 1 through 4 with Auto-Ranging disabled, an LCRU instruction is not generated to count the Range Counter up. Instead, the Mode Qualifier Bits are checked to determine whether dBm, dB (REL) or dB [REF] operation is selected. If dBm operation is selected, an LTC instruction is generated to transfer the output of the Sign Latch

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to the front-panel Sign Indicator via the Display Sign Latch, to load the output of the Main Counter into the Display Register, and to indicate to the Remote Interface Circuits that the measurement is completed. If dB (REL) operation is selected, an LCLR instruction is generated prior to the LTC instruction to set the output of the Main Counter to 0000. If dB [REF] operation is selected, an LLRE instruction is generated after the LCLR instruction and before the LTC instruction to load the 0000 output of the Main Counter into the Reference Register, thereby clearing any reference value previously stored. (Refer to paragraph dB (REL) Conversion.)

8-111. **A-D Converter dB (REL) Conversion.** A dB (REL) conversion is performed after an in-range log conversion when the Power Meter is configured for dB [REF] or dB (REL) Mode operation. The purpose of this conversion is to indicate the RF input power level with respect to a stored reference. The reference is selected by pressing the dB [REF] switch when the desired level is applied to the Power Meter. While the dB [REF] switch is pressed, the reference is updated during each program cycle. When the dB [REF] switch is released, the reference is "frozen" and the Power Meter is automatically configured for dB (REL) operation on the next program cycle. The Power Meter will then remain configured for dB (REL) operation until WATT or dBm MODE operation is subsequently selected.

8-112. When the Mode Qualifier Bits indicate that the dB [REF] mode is selected, an LLRE instruction is generated after an in-range log conversion to load the outputs of the Main Counter and the Sign Latch into the Reference Register. (Power Meter accuracy specifications apply to in-range measurements. If the dB [REF] mode is selected and an out-of-range log conversion is detected, an LCLR instruction is generated prior to the LLRE instruction to set the output of the Main Counter to 0000 and to store a positive sign in the Sign Latch. Thus, the Reference Register is effectively cleared to prevent an inaccurate reference from being used as the basis of future dB (REL) indications.) After the measured value is stored in the Reference Register, a dB (REL) conversion is enabled to indicate the measured value with respect to the stored reference. At the end of this conversion the output of the Main Counter will be 0000 because the measured value and the reference value were equal at the start of the conversion. The Controller then continues to enable one log and one dB [REF]/dB(REL) conversion per program cycle until the dB [REF] switch is released and the Mode Qualifier Bits change to indicate that the dB (REL) Mode is enabled. Following each dB [REF]/dB(REL) conversion, the outputs of the Main Counter (0000) are loaded into the front-panel Display Register by the LTC instruction.

8-113. When the dB [REF] switch is released, the new Mode Select Code is loaded into the Mode Register at the start of the next program cycle to enable the dB (REL) mode. For this mode an LLRE instruction is not generated after an in-range log conversion. Thus, the reference stored during the last program cycle is used for each dB relative conversion. The Controller and Main Counter operating cycle associated with the dB relative conversion is described in the following paragraphs.

a. An LCOR instruction is generated to load the output of the Reference Register into the Relative Counter and to set the Relative Counter = 0 (NRZ0) qualifier to logic one. When this qualifier subsequently changes state, the Controller will detect that the conversion is completed.

b. The Controller generates an LREL instruction to count the Relative Counter down one count. This is necessary because the Relative Counter has to be clocked one count past 0000 to change the state of the Relative Counter = 0 (NRZ0) qualifier.

c. The Controller monitors the Relative Counter = 0 qualifier (set to logic 1 by LCOR instruction) while generating LREL and LCNT instructions on the trailing edge of every negative alternation of the 01 clock pulse. The LREL instructions serve as down clocks to the Relative Counter and are gated with the LCNT instruction by the Up/Down Count Control Logic to provide up or down clock outputs to the Main Counter as indicated in Table 8-7. Note that up clocks are provided when the signs of the input and reference power levels are different and down clocks are provided when the signs are same. Note also that if the Main Counter is counted down through 0000, the Borrow output of the Main Counter toggles the

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Sign Latch, causing the sign outputs and, thus, the direction of counting to change. As illustrated in the examples below, this counting technique comprises an algebraic subtraction with the input power level representing the minuend and the reference power level representing the subtrahend.

Input Power Level	+5.00 dB	+5.00 dB	+5.00 dB
	−	−	−
Reference Level	+3.00 dB	+7.00 dB	−5.00 dB
Result	+2.00 dB	−2.00 dB	+10,00 dB
Input Power Level	−5.00 dB	−5.00 dB	−5.00 dB
	−	−	−
Reference Level	−3.00 dB	−7.00 dB	+5.00 dB
Result	−2.00 dB	+2.00 dB	−10.00 dB

d. When the Relative Counter = 0 qualifier changes state, the Controller detects that the conversion is completed and terminates the LREL and LCNT instructions. At this point, the outputs of the Main Counter and the Sign Latch indicate the input power level with respect to the stored reference.

e. After terminating the LREL and LCNT instructions, the Controller generates an LTC instruction to transfer the output of the Sign Latch to the front-panel Sign Indicator via the Display Sign Latch, to load the output of the Main Counter into the Display Register, and to indicate to the Remote Interface Circuits that the measurement is completed.

8-114. Service Sheet 4

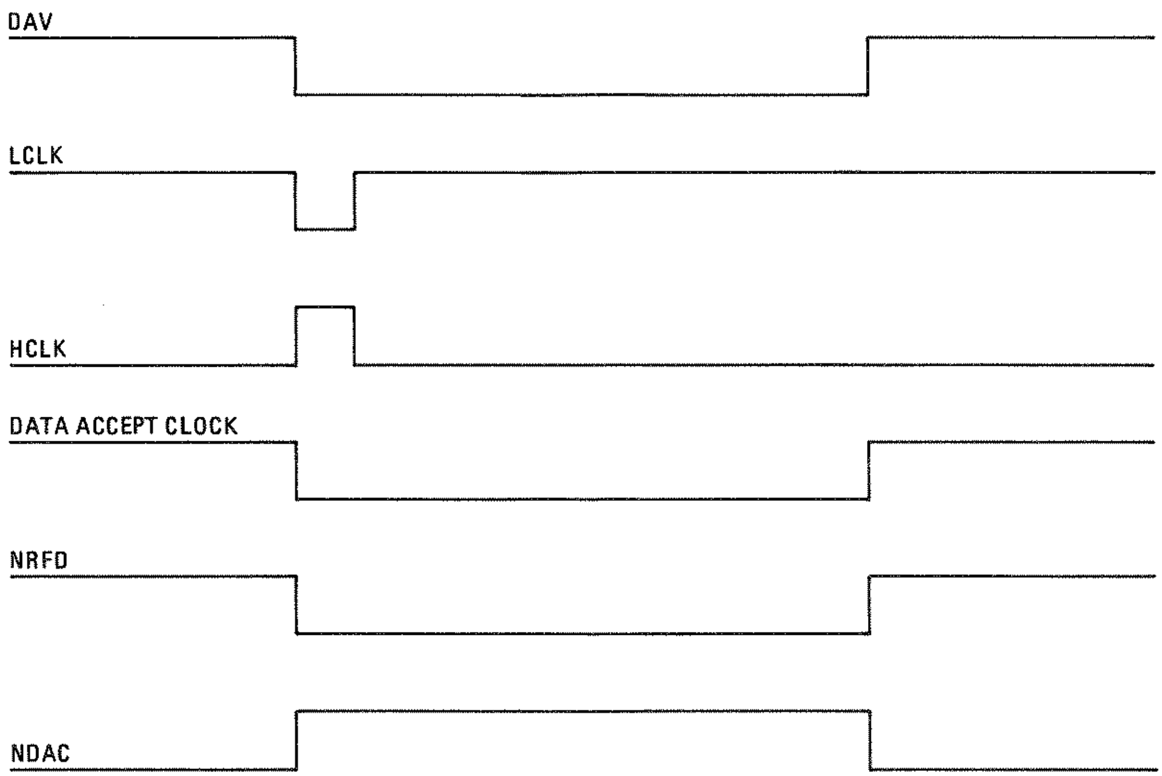
8-115. General. The Hewlett-Packard Interface Bus circuits (Option 022) add talker/listener capability to the Power Meter. When the listener function is selected, the Power Meter accepts programming inputs asynchronously to the operating program and stores the data so that it can be accessed during each program cycle. When the talker function is selected, the Power Meter outputs measurement and status data in a bit-parallel, word-serial format during the display and remote talk subroutine.

8-116. The descriptions which follow assume a basic understanding of Hewlett-Packard Interface Bus (HP-IB) operation. For additional information covering HP-IB operation, refer to "Hewlett-Packard Interface Bus Users Guide" (HP Part No. 59300-90001 for HP 9820, and 59300-90002 for HP 9830) and "Condensed Description of the Hewlett-Packard Interface Bus" (HP Part No. 59401-90030).

8-117. Command Mode Operation.

8-118. The HP-IB circuits are placed in the command mode when the Remote Interface Controller sets the comand mode enable (ATN) line low. In this mode the HP-IB circuits will respond to a listen address, a talk address, an unlisten command, a universal device clear command, an interface clear (IFC) input, and a remote enable (REN) input.

8-119. Handshake Timing. When the HP-IB circuits are in the command mode, the LATN output of the Clock Generator is held low to disable the Function Decoder and to enable the Listen Transfer Control Gates. (The LATN input to the Listen Transfer Control Gates is OR'ed with the L Listen input so that the gates are also enabled when the bus is in the data mode and the Power Meter is addressed to listen.) While the Listen Transfer Control Gates are enabled, they function in conjunction with the Clock Generator to generate the NRFD and NDAC outputs necessary to complete each Remote Interface Controller initiated data transfer cycle. (When the gates are disabled, the NRFD and NDAC outputs are set high so that they will not interface with HP Interface Bus operation.) When the Remote Interface Controller has data available, it sets the DAV line low, thereby enabling the Clock Generator to set the Data Accept Clock low a short time later as shown in Figure 8-19. The Listen Transfer Control Gates, in turn, process the low Data Accept Clock to set the NRFD line low (Not Ready For Data) and the NDAC line high (Data Accepted). These outputs are then maintained until all instruments on the HP Interface Bus indicate that they have accepted the data. When this occurs, the Remote Interface Controller sets the DAV line high, thereby terminating the Data Accept Clock a short time later. With the Data Accept Clock terminated, the NRFD output of the Listen Transfer Control Gates is set high (ready for data) and the Data Accept line is reset low to enable the next data transfer initiated by the Remote Interface Controller.



NOTES:

1. The HCLK output of the clock generator is enabled only during the command mode; the LCLK and data accept clocks are enabled in both the command and data modes.
2. The listen transfer control gates process the data accept clock to generate the NRFD and NDAC handshake signals in the command mode and, when the Power Meter is addressed to listen, in the data mode also. If the Power Meter is not addressed to Listen in the data mode, both signals are set high so that they do not affect HP-IB operation.

Figure 8-19. HP-IB Listen Handshake Timing

CIRCUIT DESCRIPTIONS

Service Sheet 4 (cont'd)

8-120. Talker and Listener Addressing. Factory installed jumpers select talk address "M" and listen address "—" for the Power Meter. (Instructions for reconnecting the jumpers to change the talk and listen addresses are provided in Section II, Installation.) In Table 2-2, it is shown that the binary code for both of these addresses is the same except for data bits 6 and 7. Thus, when either of these addresses is present on the data lines, the Address Decoder is enabled by data bits 1—5 and provides an Address Enabled output to the Listen and Talk Registers. Discrimination between the addresses is accomplished by the Talk Decoder and the Listen/Unlisten Decoder. For talk address "M", the Talk Decoder is enabled by data bits 6 and 7 and generates a Talk Clock output in response to the HCLK input. For listen address "—", the Listen/Unlisten Decoder is enabled by data bits 6 and 7 and generates a Listen Clock output in response to the HCLK input. (The data bits 1 through 5 inputs to the Listen/Unlisten Decoder enable it to produce an Unlisten output when the Remote Interface Controller generates a Universal Unlisten Command.)

8-121. Since the Talk or Listen Clock is generated while the Address enable signal is active, the associated register is clocked to the set state to enable the talk or listen function when the data bus is subsequently set to the data mode. Resetting of the register to terminate the function occurs when the Power Meter is unaddressed to talk or listen, or when the Remote Interface Controller activates the Interface Clear (IFC) line to clear the HP Interface Bus of all talkers and listeners.

8-122. The Power Meter can also be configured as a talker by setting the TALK ONLY/NORMAL switch to the TALK ONLY position. When the switch is in this position, the set input of the Talk Register is tied to ground to hold the register in the set state. Since there can only be one talker at a time on the HP Interface Bus, this function is normally selected only when there is no Remote Interface Controller connected to the system (e.g., when the Power Meter is interconnected with an HP 5150A Recorder) as the Power Meter has no provision for generating programming commands necessary to control the operation of other instruments on the HP Interface Bus.

8-123. Remote Enable. Remote operation of the Power Meter is enabled when the HREM and Remote Enable (LREM) outputs of the Remote Enable Logic are true (refer to Table 8-6 and to the Data Mode Programming paragraph). These outputs are provided by a gated flip-flop which is set only when the Listen Clock and Address Enable signals are active while the Remote Enable (REN) input is true (low). Thus, to select remote operation of the Power Meter, it is necessary to address the Power Meter to listen after the Remote Enable (REN) line is set true. The Remote Enable Logic will then remain set until the Remote Enable (REN) line is set false to terminate remote operation of all instruments on the HP Interface Bus.

NOTE

When the Power Meter is addressed to talk, it will output data after each measurement regardless of whether it is configured for local or remote operation. Refer to Figure 8-15, Sheet 14.

8-124. The remaining input to the Remote Enable Logic is the LPU signal generated by the Controller when the Power Meter is first turned on, and by the Device Clear Generator when a Device Clear Command is detected. This input is applied to the Remote Enable Logic in a "WIRED OR" configuration, and an RC network is used to discriminate between the signal sources. When the Power Meter is first turned on, the LPU output of the Controller is mainatined for approximately 500 ms, thereby allowing the RC network to discharge to 0V and reset the Remote Enable Logic. When a Device Clear Command is detected, the LPU output of the Device Clear Generator is equal in width to the HCLK input and does not discharge the RC network. Thus, when the Power Meter is first turned on, it is automatically configured for local operation. If remote operation is subsequently selected, the Power Meter will remain configured for remote operation until the Remote Enable (REN) input is set false to terminate remote operation of all instruments on the HP Interface Bus.

8-125. Device Clear. When a Device Clear Code is placed on the HP-IB data lines, the Device Clear Generator is enabled and provides an LPU otuput in response to the HCLK input. As shown on the block diagram, this output is tied to the LPU

CIRCUIT DESCRIPTIONS

Service Sheet 4 (cont'd)

output of the Controller in a "WIRED-OR" configuration. The pulse width of the Device Clear Decoder output, however, is much narrower than the Controller LPU output so it does not discharge the RC networks installed at the inputs to the Reset Generator and the Remote Enable Logic. Thus, the function of the Device Clear Decoder LPU output is limited to reinitializing the operating program to starting address 000_8 (refer to Table 8-6) and to selecting a predetermined operating mode and range for the Power Meter when remote operation is enabled (refer to the Data Mode Programming paragraph).

8-126. Interface Clear. When the Interface Clear (IFC) input is true (low) the Reset Generator is enabled and provides a Reset output to the Talk and Listen Registers. Thus if the Power Meter was addressed to talk or listen previously, the talk or listen function is cleared. Similarly, when power is first turned on to the Power Meter, the pulse width of the Controller LPU output is of sufficient duration to discharge the Reset Generator RC network and thereby cause a Reset output to be applied to the Talk and Listen Registers.

8-127. Talker Unaddressing. When the TALK ONLY/NORMAL switch is set to the NORMAL position, the Remote Interface Controller can unaddress the Power Meter to talk by setting the Interface Clear (IFC) line true (refer to previous description), by addressing some other instrument on the HP Interface Bus to talk, or by generating a Universal Untalk Command. In Table 2-2, it is shown that data bits 6 and 7 are coded the same for all valid HP-IB talk addresses and for the Universal Unlisten Command. When any of these codes are placed on the HP-IB data lines, the Talk Decoder is enabled and provides a Talk Clock output in response to the HCLK input. For any address but that selected by the factory installed jumpers, however, data bits 1 through 5 are coded such that the Address Decoder is disabled. Thus, the absence of the Address Enable signal causes the Talk Register to be clocked to the reset state by the Talk Clock.

8-128. Listener Unaddressing. The Remote Interface Controller can unaddress the Power Meter to listen by setting the Interface Clear (IFC) line true (refer to previous description), or by generating a Universal Unlisten Command. The Universal Unlisten Command is coded such that data bits 1 through 5 disable the Address Decoder and enable the Unlisten output of the Listen/Unlisten Decoder. Data bits 6 and 7 are coded the same as for any valid HP-IB listen address, so they enable the Listen/Unlisten Decoder to also provide a Listen Clock output in response to the HCLK input. With the Unlisten Signal Active and the Address Enable Signal Inactive, the Listen Register is clocked to the reset state by the Listen Clock.

8-129. The method of unaddressing the Power Meter to listen described previously prevents the Power Meter from being unaddressed to listen when other instruments on the HP-IB are designated as listeners. (There can only be one talker on the HP-IB at a time, but there can be up to five listeners.) If any other listen address than that assigned to the Power Meter is placed on the HP-IB, data bits 1 through 5 disable both the Address Decoder and the Unlisten output of the Listen/Unlisten Decoder. Thus, even though data bits 6 and 7 enable the Listen Clock output of the Listen/Unlisten decoder, the absence of the Address Enable and Unlisten inputs inhibits the Listen Register from changing state.

8-130. Data Mode Operation.

8-131. The HP-IB circuits are placed in the data mode when the Remote Interface Controller sets the Command Mode Enable (ATN) line to high. In this mode, the HP-IB circuits can function either as a talker or a listener. If remote operation of the Power Meter is enabled and the circuits were previously addressed to listen, they accept and decode programming inputs received over the HP-IB and store the data to control Power Meter operation. If remote operation of the Power Meter is enabled and the circuits were previously addressed to talk, they provide measurement and status outputs in a bit-parallel, word-serial format during the operating program Display and Remote Talk Subroutine.

8-132. Listen Handshake Timing. When the HP-IB is in the data mode and the HP-IB circuits are addressed to listen, the handshake timing outputs necessary to complete each Remote Interface Controller-initiated data transfer cycle are generated as described above for the command mode.

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Data Mode Operation (cont'd)

8-133. General Programming Command Decoding. When the HP-IB is in the data mode and the Power Meter is addressed to listen, the high LATN and H Listen signals enable the Function Decoder. The Function Decoder then processes the data bit 4 through 7 inputs each time that the LCLK is generated to indicate that valid data is present on the HP-IB. In Table 2-2 it is shown that either data bit 6 or 7 is true (0V) for each of the programming codes assigned to the Power Meter. With either of these data bit inputs low for the conditions described (LATN - high, LCLK - low, H Listen - high), the Function Decoder is gated on and decodes the HI04, HI05, and HI06 inputs to generate a Clock output which enables the appropriate logic circuit to respond to the programming command. The specific Clock output generated for each programming command is listed in Table 8-8, and the resulting logic circuit operation is summarized in Table 8-9.

8-134. When the HP-IB is not in the data mode, the Function Decoder is disabled by the low LATN input. Similarly, when the Power Meter is not addressed to listen, the low H Listen input disables the Function Decoder. While the Function Decoder is disabled, it does not respond to the data bit inputs and so no Clock outputs are provided to the Progamming Command Logic Circuits. Thus, the Programming Command Logic Circuits are inhibited from responding to any data inputs except programming commands specifically intended for the Power Meter.

8-135. Mode Programming Command Processing. The Mode Clock output of the Function Decoder resets the Auto Zero Enable Logic and clocks the LI01 and HI02 data bit inputs into the flip-flops in the Mode Select Logic. The outputs of the flip-flops are then gated with the HREM input to select the operating mode for the Power Meter when remote operation is enabled (HREM-high) and to allow front-panel "WIRED OR" selection of this function when local operation is enabled (refer to Service Sheet 3, Block Diagram Description, Mode Selection).

8-136. After a Mode Programming Command is loaded into the Mode Select Logic flip-flops, the flip-flops are inhibited from changing state until a new Mode Programmming Command or an LPU input is received. When a new Mode Programming Command is received, the outputs of the flip-flops change to reflect the new mode encoded in the command. When an LPU input is received, the flip-flops are reset to select WATT Mode operation of the Power Meter.

8-137. Range Programming Command Processing. The Range Clock output of the Function Decoder resets the Auto-Range Qualifier output of the Range Select Logic to disable Auto-Ranging, and also clocks the HI01, LI02, and LI03 data bit inputs into flip-flops in the Range Select Logic. The inverted outputs of the flip-flop are then continuously applied to the Controller as YRR1, YRR2, and YRR3 Range Select inputs. Since the Auto-Range Qualifier is reset, the Controller loads these inputs into the Range Counter at the start of each program cycle (when remote operation is enabled) to select the operating range for the Power Meter.

8-138. After a Range Select Command is loaded into the Range Select Logic flip-flops, the flip-flops are inhibited from changing state until a new Range Programming Command or an LPU input is received. When a new Range Programming Command is received, the outputs of the flip-flops change to reflect the new range encoded in the command. When an LPU input is received, the Range flip-flops are reset and the Auto-Range flip-flop is reset to select Auto-Ranging when remote operation of the Power Meter is enabled (refer to the paragraph on Auto-Range Programming Command Processing).

8-139. Auto-Range Programming Command Processing. The LPU input and the Auto-Range Enable output of the Function Decoder set a flip-flop in the Range Select Logic. The output of the flip-flop is then gated with the HREM input to select Auto-Ranging when remote operation is enabled (HREM-high) and to allow front-panel "WIRED OR" range control of this function when local operation is enabled. (When remote operation is enabled and the Auto-Range Qualifier is true, the Range Select outputs are not loaded into the Range Counter at the start of each program cycle. Instead, the Range Counter is counted up or down during each cycle as required to obtain an in-range measurement.) Resetting of the Auto-Range flip-flop occurs when the Function Decoder provides a Range Clock output (refer to previous description).

Table 8-8. Function Decoder Clock Selection

PROGRAMMING COMMAND	DATA BIT CODING			CLOCK SELECTED
	H104	H105	H106	
Range (1, 2, 3, 4, 5)	L	H	H	Range clock
Auto Range Select (9)	H	H	H	Auto Range Clock
Mode (A, B, C, D)	L	L	L	Mode Clock
Sensor Auto Zero Enable (Z)	H	H	C	Auto Zero Clock
Cal Factor Enable/Disable (+/-)	H	L	H	Cal Factor
Measurement Rate (H, I)	H	L	L	Rate Clock 1
Measurement Rate (R, T, V)	L	H	L	Rate Clock 2

Table 8-9. Programming Command Logic Operating Summary (1 of 2)

PROGRAMMING COMMAND	DATA BIT CODING						LOGIC CIRCUIT OUTPUT
	L101	H101	L102	H102	L103	H103	
Range 1	X	H	H	X	H	X	YRR1 - high; YRR2 and YRR3 - low
Range 2	X	L	L	X	H	X	YRR2 - high; YRR1 and YRR3 - low
Range 3	X	H	L	X	H	X	YRR1 and YRR2 - high; YRR3 - low
Range 4	X	L	H	X	L	X	YRR3 - high; YRR1 and YRR2 - low
Range 5	X	H	H	X	L	X	YRR1 and YRR3 - high; YRR2 - low
Auto-Range Select (9)	X	X	X	X	X	X	Auto-Range qualifier set true (low) by Auto-Range Clock output of Function Decoder
Watt Mode (A)	L	X	X	L	X	X	IYM1 - low; IYM2 - high
dB Rel Mode (B)	H	X	X	H	X	X	IYM1 - high; IYM2 - low
dB Ref Mode (C)	L	X	X	H	X	X	IYM1 - low; IYM2 - low
dBm Mode (D)	H	X	X	L	X	X	IYM1 - high; IYM2 - high
Sensor Auto Zero Enable (Z)	X	X	X	X	X	X	Auto-Zero Enable (NZR) output set true (low) by Auto-Zero Clock output of Function Decoder
Cal Factor Disable (+)	X	X	X	X	H	X	Cal Factor Disable - high
Cal Factor Enable (-)	X	X	X	X	L	X	Cal Factor Disable - open collector (≈ −15V)

NOTE: X Indicates Don't Care

Table 8-9. Programming Command Logic Operating Summary (2 of 2)

PROGRAMMING COMMAND	DATA BIT CODING						LOGIC CIRCUIT OUTPUT
	LI01	HI01	LI02	HI02	LI03	HI04	
Hold (H)	H	X	X	L	H	H	LRUN and LSLOW - high
Trigger with setting time (T)	H	X	X	L	L	L	LRUN - set low by programming command; reset by LTC instruction generated as start of display and remote talk subroutine LSLOW - low
Trigger immediate (I)	L	X	X	L	H	H	LRUN - set low by programming command; reset by LTC instruction generated at start of display and remote talk subroutine
Free run at maximum rate (R)	H	X	X	H	H	L	LRUN - low; LSLOW - high
Free run with settling time (V)	H	X	X	H	L	L	LRUN - low; LSLOW - low

NOTE: X Indicates Don't Care.

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Data Mode Operation (cont'd)

8-140. Sensor Auto-Zero Programming Command Processing. The Auto-Zero Clock output of the Function Decoder sets a flip-flop in the Auto Zero Enable Logic. The output of the flip-flop is then gated with the HREM input to select Sensor Auto-Zeroing when remote operation is enabled (refer to Service Sheet 3, Block Diagram Description, Mode Selection), and to allow front-panel "WIRED OR" control of this function when local operation is enabled. Resetting of the flip-flop occurs when the Function Decoder provides a Mode Clock output (refer to previous description) or when the Controller or the Device Clear Decoder generates an LPU output.

8-141. Cal Factor Programming Command Processing. The Auto-Zero Clock output of the Function Decoder clocks the LI03 data bit input into a flip-flop in the Cal Factor Disable Logic. The output of the flip-flop is then gated with the HREM input. When the HREM input is low, indicating that local operation is enabled, the Cal Factor Disable line is set false to enable the CAL FACTOR % switch (refer to Service Sheet 2). When the HREM input is high, indicating that remote operation is enabled, the state of the stored LI03 bit controls the Cal Factor Disable output. For a Cal Factor Enable (—) Programming Command, the stored bit is low and sets the Cal Factor Disable output false to enable the front-panel CAL FACTOR % switch. For a Cal Factor Disable (+) Programming Command, the stored bit is high and sets the Cal Factor Disable output true to disable the CAL FACTOR % switch. Disabling the switch is the same as setting it to the 100% position.

8-142. After a Cal Factor Programming Command is loaded into the Cal Factor Disable Logic flip-flop, the flip-flop is inhibited from changing state until a new Cal Factor Programming Command or an LPU input is received. When a new Cal Factor Programming Command is received, the flip-flop changes state to reflect the new state of the LI03 data bit. When an LPU input is received, the flip-flop is preset to set the Cal Factor Disable output true, disabling the front-panel switch.

8-143. Measurement Rate Programming Command Processing. The Rate Clock 1 and 2 outputs of the Function Decoder are ORed together so that either clock causes the Measurement Rate Select Logic to process the LI01, HI02, LI03, and HI04 data bit inputs. The LI03 bit selects the measurement rate

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Data Mode Operation (cont'd)

(delayed or immediate) and the remaining three bits select hold, triggered, or free-run operation of the Power Meter.

8-144. The LI03 bit is processed separately from the remaining data bit inputs to the Measurement Rate Select Logic. When the Function Generator provides a Rate Clock output, this bit is clocked into a flip-flop. If the LI03 bit is high, the flip-flop is clocked to the set state to select delayed measurements; if the LI03 bit is low, the flip-flop is clocked to the reset state to select immediate measurements. The output of the flip-flop is then continuously applied to the Remote Qualifier Multiplexer so that it can be accessed by the operating program. This output is then maintained until either a new Measurement Rate Programming Command or an LPU input is received. When a new Measurement Rate Programming Command is received, the output of the flip-flop changes to reflect the current state of the LI03 data bit. When an LPU input is received, the flip-flop is reset along with the Hold and Trigger flip-flops and the Power Meter is placed in a hold condition.

8-145. The LI02, HI02, and HI04 data bit inputs are processed together to select hold, free run, or triggered operation of the Power Meter. When the Function Decoder provides a Rate Clock output, the HI02 bit is clocked directly into a flip-flop and the LI01 and HI04 bits are NANDed together with the resultant output clocked into a second flip-flop. For purposes of definition, the flip-flop which accepts the HI02 bit is called the Hold Flip-Flop, and the flip-flop which accepts the gated input is called the Trigger Flip-Flop. When the HI02 bit is high, the Hold Flip-Flop is clocked to the set state to enable free run operation of the Power Meter. When the HI02 bit is low, the Hold Flip-Flop is clocked to the reset state to enable hold or triggered operation of the Power Meter. The way this is accomplished is by ORing the outputs of the Hold and Trigger Flip-Flops. When the Hold Flip-Flop is set, the OR gate is continuously enabled and provides a low H HOLD output to the Remote Multiplexer. When the Hold Flip-Flop is reset, the state of the Trigger Flip-Flop controls the H HOLD output of the OR gate. Operation of the Trigger Flip-Flop for a Hold or Triggered Measurement Programming Command is described in the following paragraphs.

a. When both the LI01 and HI04 data bits are high for a Hold Programming Command, the Trigger Flip-Flop is reset by the Rate Clock output of the Function Decoder. Since the Hold Flip-Flop is also reset, the OR gate is disabled and a high H HOLD output is provided to the Remote Multiplexer to inhibit the Power Meter from taking measurements (see Figure 8-15, Sheets 4 and 14).

b. When either the LI01 or HI04 data bit is low for a Triggered Measurement Programming Command, the Trigger Flip-Flop is set by the Rate Clock output of the Function Decoder, then reset by the LTC instruction generated at the start of the operating program Display and Remote Talk Subroutine. While the Flip-Flop is set, the OR gate is enabled and provides a low H HOLD output to the Remote Multiplexer to initiate a Power Meter measurement. After the measurement is completed and the flip-flop is reset, the OR gate is disabled by the low outputs of the Hold and Trigger Flip-Flops. Thus, the gate provides a high H HOLD output to inhibit further measurements until a Free Run or Triggered Measurement Programming Command is received.

8-146. The output of the Trigger Flip-Flop is also gated with the LTLK output of the Talk Register to provide a Talk Qualifier (HTLK; 032_8) input to the Remote Multiplexer. When the Power Meter is not addressed to Talk, the LTLK signal is high and a low HTLK input is applied to the Remote Multiplexer to inhibit the operating program from initiating an Output Data Transfer. When the Power Meter is addressed to Talk, the LTLK input is low and the HTLK output of the gate is controlled by the Trigger Flip-Flop as described in the following paragraphs.

a. When the Trigger Flip-Flop is reset by a Hold Programming Command, a continuously high HTLK qualifier is applied to the Remote Multiplexer to enable the operating program to initiate an Output Data Transfer after completing the measurement in progress (refer to Figure 8-15, Sheet 14). Following the Output Data Transfer, the operating program then detects the hold condition in the Local/Remote Branch Subroutine (H HOLD high) and enters an idle state while awaiting a Free-Run or Triggered Measurement Programming Command to initiate the next measurement.

b. When the Trigger Flip-Flop is set by a Free-Run or Triggered Measurement Programming

Data Mode Operation (cont'd)

Command, a low HTLK qualifier is applied to the Remote Multiplexer until the flip-flop is reset by the LTC instruction generated at the start of the Display and Remote Talk Subroutine. Since this instruction is generated before the operating program checks whether Remote Talk is enabled, the resulting HTLK qualifier enables the operating program to initiate an Output Data Transfer during the Display and Remote Talk Subroutine. If the Trigger Flip-Flop was set by a Free-Run Programming Command, the H HOLD qualifier will be low and the operating program will continue to take measurements and output data after each measurement until a new Measurement Rate Programming Command is received or the Power Meter is unaddressed to talk. If the Trigger Flip-Flop was set by a Triggered Measurement Programming Command, the H HOLD qualifier will be high after the LTC instruction and the operating program will enter an idle state during the Local/Remote Branch Subroutine while awaiting a Free-Run or Triggered Measurement Programming Command to initiate the next measurement. The reason that an Output Data Transfer is synced to the LTC instruction for a Triggered Measurement Programming Command is to ensure that valid measurement is taken before the Power Meter outputs data after being addressed to Talk.

8-147. The remaining input to the Hold and Trigger Flip-Flops is the LPU output of the Controller and the Device Clear Decoder. When this input is active, both registers are reset and a high H HOLD qualifier is applied to the Remote Multiplexer to place the Power Meter in a hold condition.

8-148. Remote Qualifier/Program Interface. When remote operation is enabled, each of the qualifier inputs to the Remote Qualifier Multiplexer is accessed at some point in the operating program cycle. The purpose and function of each qualifier is provided in Table 8-2, along with a listing of the subroutines in which the qualifier is accessed. The manner in which the qualifier is accessed by the operating program is covered on Service Sheet 3, Block Diagram Description.

NOTE

The Remote Qualifier Multiplexer inverts the qualifier inputs. Thus, a "true" qualifier input will be in the opposite state to that shown on the Operating Program Flow Chart.

8-149. Talk Cycle. During the Display and Remote Talk Subroutine of each program cycle, the operating program checks whether the Power Meter is addressed to Talk. If the Power Meter is addressed to Talk, the LTLK input to the Remote Qualifier Multiplexer will be low and an Output Data Transfer will be enabled as shown on Sheet 14 of Figure 8-15. Operation of the HP-IB circuits when the Power Meter is addressed to talk is described in the following paragraphs.

a. **Talk Transfer Control Gates.** The Talk Transfer Control Gates are enabled by the low LTLK and HATN inputs when the Power Meter is addressed to Talk and the HP-IB is in the data mode. While the gates are enabled, they provide high HOE 1 and high HOE 2 outputs to enable the Data Valid Status Generator and the Output Gates.

NOTE

As shown on Sheet 14 of Figure 8-15, the operating program will initiate an Output Data Transfer whenever the LTLK qualifier is low. If the HP-IB is not in the data mode, however, the Talk Transfer Control Gates will be disabled by the high HATN input and the resulting low HOE 2 output will set the HRFD qualifier output of the Data Valid Status Generator low. Similarly, if there is no listener on the HP-IB, the low NRFD input also sets the HRFD qualifier low. With this qualifier low, the operating program will enter a hold loop until the Power Meter is unaddressed to Talk.

b. **Data Valid Status Generator.** The Data Valid Status Generator functions in conjunction with the operating program to generate the timing signals necessary to complete a Power Meter initiated data transfer. A timing diagram of Data Valid Status Generator operation is provided in Figure 8-20. As shown in the figure, the JK flip-flop is initially reset by the LPU input and cannot change state until the Power Meter is addressed to Talk and all listeners on the HP-IB indicate that they are ready to accept data. When this occurs, both the

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HOE 2 and the NRFD inputs will be high and the Data Valid Status Generator will provide a high HRFDq qualifier input to the Remote Multiplexer. If the HP-IB is connected properly, the HDACq qualifier will be low at this time and the operating program will generate an LSDAV instruction to set the JK flip-flop.

NOTE

The HRFDq and the HDACq qualifier outputs of the Data Valid Status Generator are delayed slightly to allow settling time for the HP-IB listeners.

When the JK flip-flop is set, the combination of the high HIDAV and HOE 2 signals cause the output gates to set the DAV line low, thereby indicating that valid data is available on the HP-IB. (Word Counter, ROM, and Output Gate operation is described in the following paragraph.) After all of the listeners on the HP-IB accept the data, the DAC input to the Data Valid Status Generator goes high, causing the Status Generator to provide a high HDACq qualifier output to the Remote Qualifier Multiplexer. The operating program, in turn, detects the change in state of the HDACq qualifier and generates a second LSDAV instruction to reset the JK flip-flop. The low HIDAV output then disables the DAV output of the Output Gates and the negative-to-positive transition of the LIDAV signal clocks the Word Counter to the next ROM address. As shown on Sheet 14 of Figure 8-15 this cycle is then repeated until all 14 of the output data words are sent over the HP-IB. Note that the JK flip-flop is reset after each word is transferred. Thus, the JK flip-flop will be reset by the last LSDAV instruction of the Output Data Transfer and will remain reset until the operating program initiates the next Output Data Transfer.

8-150. **Word Counter, ROM, Line Selector, Multiplexer Gate, and Output Gate Operation.** All of these circuits function together to sequentially output data words 0 through 13 each time that the operating program enables an Output Data Transfer during the Display and Remote Talk Subroutine. Each word consists of seven data bits which are ASCII coded to select a status character as indicated in Table 8-10. Coding of data bits 7, 6, and 5 is accomplished by buffering the Y6, Y5, and Y4 outputs of the ROM. Coding of the remaining data bits is controlled by the Y7 output of the ROM. When this bit is low, the Line Selectors are enabled and they route the status inputs selected by the YO through Y3 outputs of the ROM to the Output Gates. When the Y7 bit is high, the Line Selectors are disabled and the YO through Y3 outputs of the ROM are buffered by the Multiplexer Gates to select the coding for data bits 1 through 4.

8-151. The output of the ROM, in turn, is selected by the address input from the Word Counter. This address is set to 0 at the start of each program cycle by the HLLD reset input to the Word Counter. While the ROM is at address 0, its output causes the Line Selectors to route the HOR, HUR, and YM3 status inputs to the Output Gates to form a Word 0 ASCII character as indicated in Table 8-10.

8-152. When the Power Meter is addressed to Talk, the Output Gates are enabled by the high HOE 1 and HOE 2 inputs and continually route data to the HP-IB. The HP-IB does not accept the data, however, until the Data Valid Status Generator provides a high HIDAV output to set the Data Valid (DAV) output true. When this occurs, each of the listeners accept the data and set the DAC line high to complete the data word transfer.

8-153. After all of the listeners have accepted the data, the Word Counter is clocked to the next address on the positive-going edge of the LIDAV output of the Data Valid Status Generator. For addresses 0 through 13 either the Y0 or the Y7 output of the ROM is high, so a low HMDT qualifier is applied to the Remote Multiplexer to enable each word to be sequentially transferred over the HP-IB. After word 13 is transferred, both the Y0 and Y7 outputs of the ROM go low and a high HMDT qualifier is applied to the Remote Multiplexer to terminate the data transfer cycle. The HMDT qualifier is then held high until the Word Counter is reset to 0 by the HHLD instruction generated at the start of the next program cycle.

8-154. The remaining address input to the ROM is the LQT signal. When this input is low, the outputs of the Word Counter select ROM addresses 00_8 through 15_8; when this input is high, the outputs of the Word Counter select ROM addresses 20_8

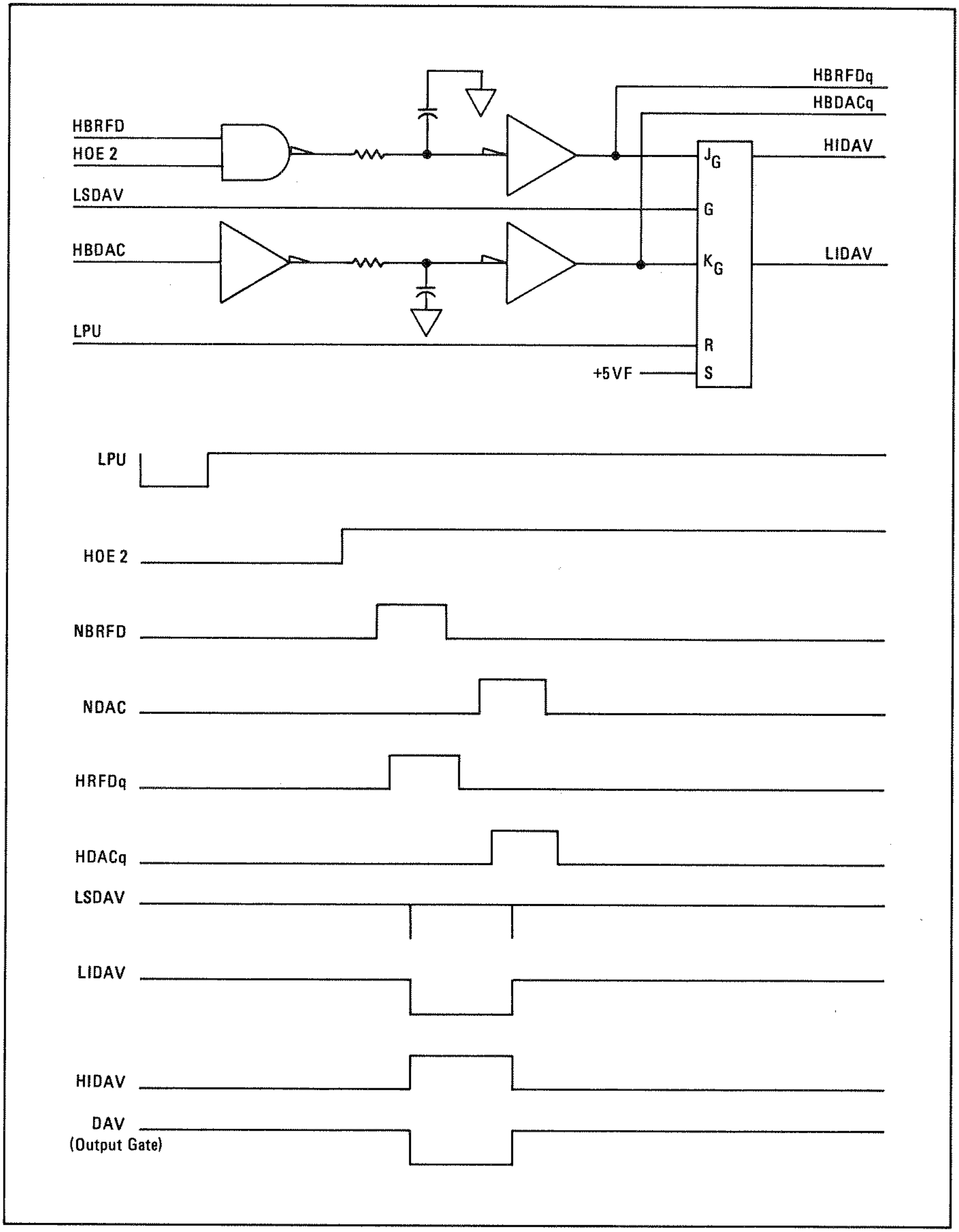


Figure 8-20. Data Valid Status Generator Timing

Table 8-10. Power Meter Talk HP-IB Output Data Format (1 of 3)

Word	Character	ROM Output – Y								Data Output – LDIO							Notes
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	
0 Status	P (In-Range)	L	H	L	H	L	L	L	H	L	H	L	H	H	H	H	1. ROM address 20_8. 2. Data output selected by HOR, HUR, & YM3 inputs to Line Selectors.
	Q (Under Range,Watts)									L	H	L	H	H	H	L	
	R (Over Range)									L	H	L	H	H	L	H	
	S (Under Range, Log)									L	H	L	H	H	L	L	
	T (Auto Zeroing, Range 1)									L	H	L	H	L	H	H	
	U (Auto Zeroing, Not Range 1)									L	H	L	H	L	H	L	
1 Range	I (Range 1)	L	H	L	L	L	L	H	H	L	H	H	L	H	H	L	1. ROM address 01_8 or 21_8. 2. Data output selected by YR1, YR2, & YR3 inputs to Line Selectors.
	J (Range 2)									L	H	H	L	H	L	H	
	K (Range 3)									L	H	H	L	H	L	L	
	L (Range 4)									L	H	H	L	L	H	H	
	M (Range 5)									L	H	H	L	L	H	L	
2 Mode	A (Watt)	L	H	L	L	L	H	L	H	L	H	H	H	H	H	L	1. ROM address 022_8. 2. Data output selected by NM1 and NM2 inputs to Line Selectors
	B (dB Rel)									L	H	H	H	H	L	H	
	C (dB Ref)									L	H	H	H	H	L	L	
	D (dBm)									L	H	H	H	L	H	H	
3 Sign	SP (plus)	H	L	H	L	H	H	H	H	H	L	H	L	H	L	L	1. ROM address 23_8. 2. Data output se- selected by ROM.
	– (minus)	H	L	H	L	L	L	H	L	H	L	H	L	L	H	L	1. ROM address 03_8. Data output se- lected by ROM.
4 YK Digit	0	L	L	H	H	L	H	H	H	H	L	L	H	H	H	H	1. ROM address 24_8. (cont'd)
	1									H	L	L	H	H	H	L	

Table 8-10. Power Meter Talk HP-IB Output Data Format (2 of 3)

Word	Character	ROM Output – Y								Data Output – LDIO							Notes
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	
4 YK Digit (cont'd)	2									H	L	L	H	H	L	H	2. Data output selected by YK1—YK4 inputs to Line Selectors.
	3									H	L	L	H	H	L	L	
	4									H	L	L	H	L	H	H	
	5									H	L	L	H	L	H	L	
	6									H	L	L	H	L	L	H	
	7									H	L	L	H	L	L	L	
	8									H	L	L	L	H	H	H	
	9									H	L	L	L	H	H	L	
5 YH Digit	0 – 9	L	L	H	H	H	L	L	H								1. ROM address 05_8 or 25_8. 2. Data output selected byYH1—YH4 inputs to Line Selectors.
6 YD Digit	0 – 9	L	L	H	H	H	L	H	H								1. ROM address 026_8. 2. Data output selected by YD1—YD4 inputs to Line Selectors.
7 YU Digit	0 – 9	L	L	H	H	H	H	L	H								1. ROM address 07_8 or 27_8. 2. Data output selected by YU1—YU4 inputs to Line Selectors
8 Exponent	E	H	H	L	L	H	L	H	L	L	H	H	H	L	H	L	1. ROM address 10_8 or 30_8. 2. Data output selected by ROM.
9	– (E "–")	H	L	H	L	L	L	H	L	H L	L H	H H	H H	H L	L H	H L	1. ROM address 11_8 or 31_8. 2. Data output selected by ROM.
10 HEX 4 Digit	E‾ "0" X	H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	1. ROM address 12_8. 2. Data output selected by ROM.
	E‾ "1" X	H	L	H	H	H	H	H	H	H	L	L	H	H	H	L	1. ROM address 32_8. 2. Data output selected by ROM.

Table 8-10. Power Meter Talk HP-IB Output Data Format (3 of 3)

Word	Character	ROM Output – Y								Data Output – LDIO							Notes
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	
11 HEX 1-3 Digit	0–9 (E^{-}X"X")	L	L	H	H	H	H	H	H								1. ROM address 13_8 or 33_8 2. Data output selected by HEX0-HEX3 inputs to Line Selectors
12	"CR" (Carriage Return)	H	L	L	L	L	L	H	L	H	H	H	L	L	H	L	1. ROM address 14_8 or 34_8. 2. Data output selected by ROM.
13	"LF" (Line Feed)	H	L	L	L	L	H	L	H	H	H	H	L	H	L	H	1. ROM address 15_8 or 35_8.

CIRCUIT DESCRIPTIONS

Data Mode Operation (cont'd)

through 35_8. For all words except 3 and 10, the ROM is programmed redundantly to provide the same outputs for either a OX or 2X address input (refer to Table 8-10). For Word 3, the ROM outputs an ASCII space code when the LQT input is set high by a low NSPL input (positive sign) and an ASCII minus sign code when the LQT input is set low by a high NSPL input (negative sign). For Word 10, the ROM provides an ASCII one code when the LQT input is set low by a high HEX 4 input and an ASCII zero code when the LQT input is set high by a low HEX 4 input.

Paragraphs 8-155 through 8-163 were deleted.

SERVICE SHEET 1

BLOCK DIAGRAM CIRCUIT DESCRIPTIONS

The Block Diagram Circuit Descriptions for Service Sheet 1 are covered in paragraphs 8-71 through 8-74, Troublshooting in paragraphs 8-55 through 8-62, and Standard Instrument Checkout in Table 8-3.

SERVICE SHEET 2

BLOCK DIAGRAM CIRCUIT DESCRIPTIONS

The Block Diagram Circuit Descriptions for Service Sheet 2 are covered in paragraphs 8-75 through 8-86, Troubleshooting in paragraphs 8-55 through 8-62, and Standard Instrument Checkout in Table 8-3.

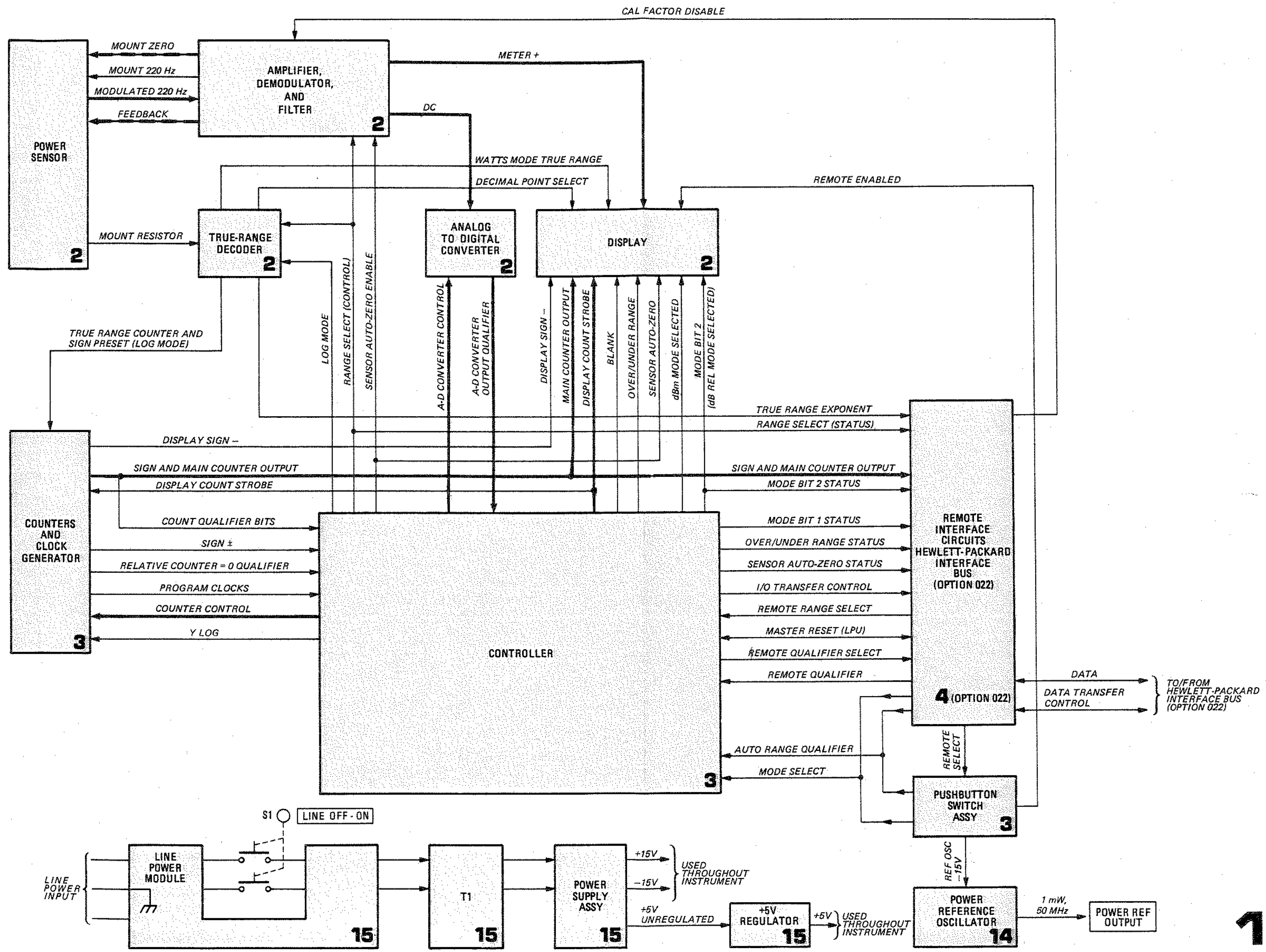
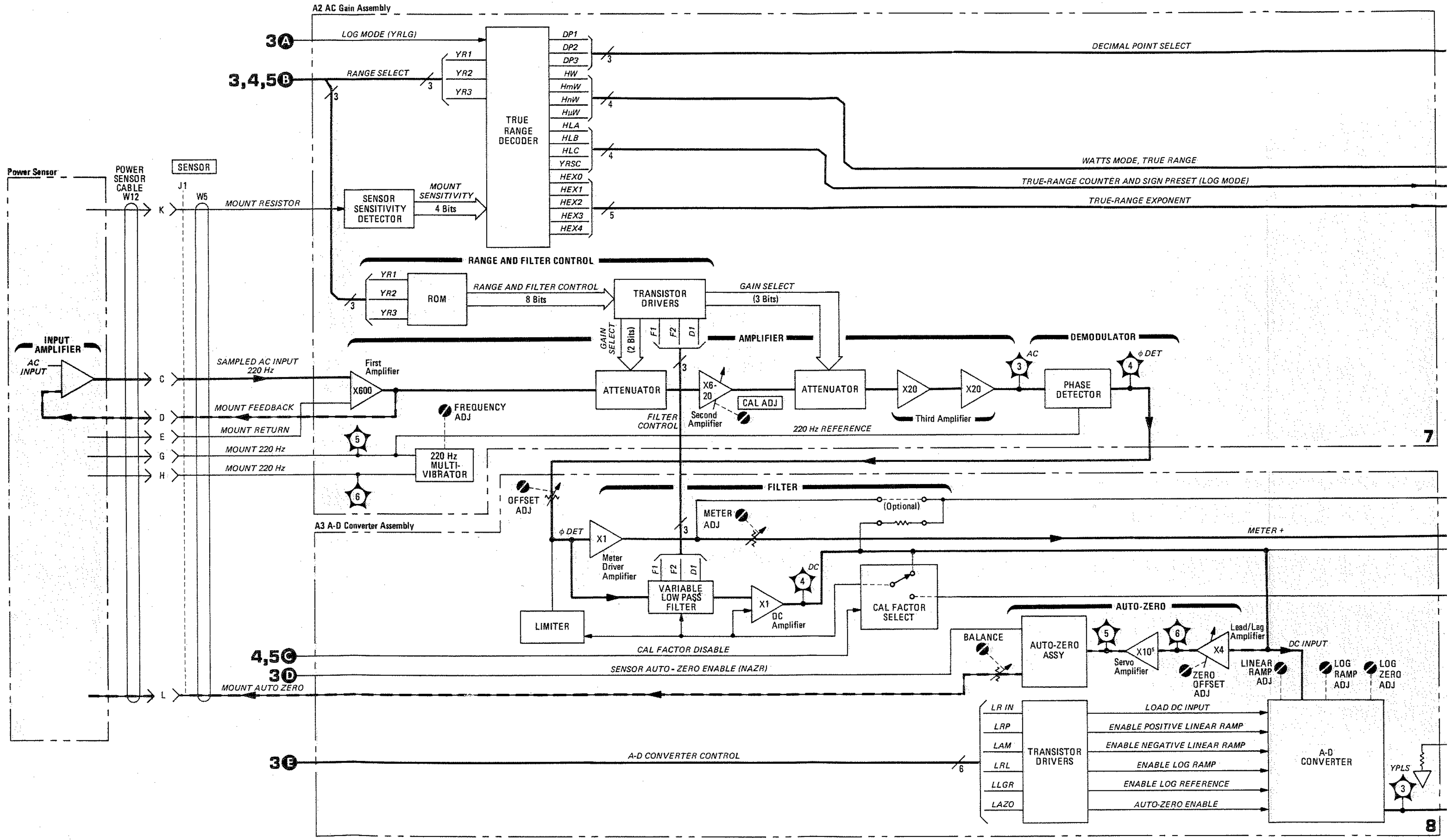


Figure 8-21. Overall Block Diagram

SERVICE SHEET 3

BLOCK DIAGRAM CIRCUIT DESCRIPTIONS

The Block Diagram Circuit Descriptions for Service Sheet 3 are covered in paragraphs 8-87 through 8-113, Troubleshooting in paragraphs 8-55 through 8-62, and Standard Instrument Checkout in Table 8-3.


A2 AC Gain Assembly
A3 A-D Converter Assembly
Power Sensor
INPUT AMPLIFIER
AC INPUT
POWER SENSOR CABLE W12
SENSOR
J1
W5
MOUNT RESISTOR
SAMPLED AC INPUT 220 Hz
MOUNT FEEDBACK
MOUNT RETURN
MOUNT 220 Hz
MOUNT 220 Hz
MOUNT AUTO ZERO
3A
3,4,5B
4,5C
3D
3E
LOG MODE (YRLG)
RANGE SELECT
TRUE RANGE DECODER
SENSOR SENSITIVITY DETECTOR
MOUNT SENSITIVITY
4 Bits
DECIMAL POINT SELECT
WATTS MODE, TRUE RANGE
TRUE-RANGE COUNTER AND SIGN PRESET (LOG MODE)
TRUE-RANGE EXPONENT
RANGE AND FILTER CONTROL
ROM
RANGE AND FILTER CONTROL
8 Bits
TRANSISTOR DRIVERS
GAIN SELECT
(3 Bits)
GAIN SELECT
(2 Bits)
AMPLIFIER
First Amplifier
X600
ATTENUATOR
X6-20
Second Amplifier
CAL ADJ
ATTENUATOR
X20
X20
Third Amplifier
FILTER CONTROL
220 Hz REFERENCE
DEMODULATOR
AC
PHASE DETECTOR
ϕ DET
FREQUENCY ADJ
220 Hz MULTI-VIBRATOR
FILTER
OFFSET ADJ
ϕ DET
X1
Meter Driver Amplifier
METER ADJ
(Optional)
METER +
VARIABLE LOW PASS FILTER
X1
DC Amplifier
DC
CAL FACTOR SELECT
LIMITER
CAL FACTOR DISABLE
SENSOR AUTO - ZERO ENABLE (NAZR)
AUTO-ZERO
BALANCE
AUTO-ZERO ASSY
Servo Amplifier
ZERO OFFSET ADJ
Lead/Lag Amplifier
DC INPUT
LINEAR RAMP ADJ
LOG RAMP ADJ
LOG ZERO ADJ
A-D CONVERTER CONTROL
TRANSISTOR DRIVERS
LOAD DC INPUT
ENABLE POSITIVE LINEAR RAMP
ENABLE NEGATIVE LINEAR RAMP
ENABLE LOG RAMP
ENABLE LOG REFERENCE
AUTO-ZERO ENABLE
A-D CONVERTER
YPLS
7
8

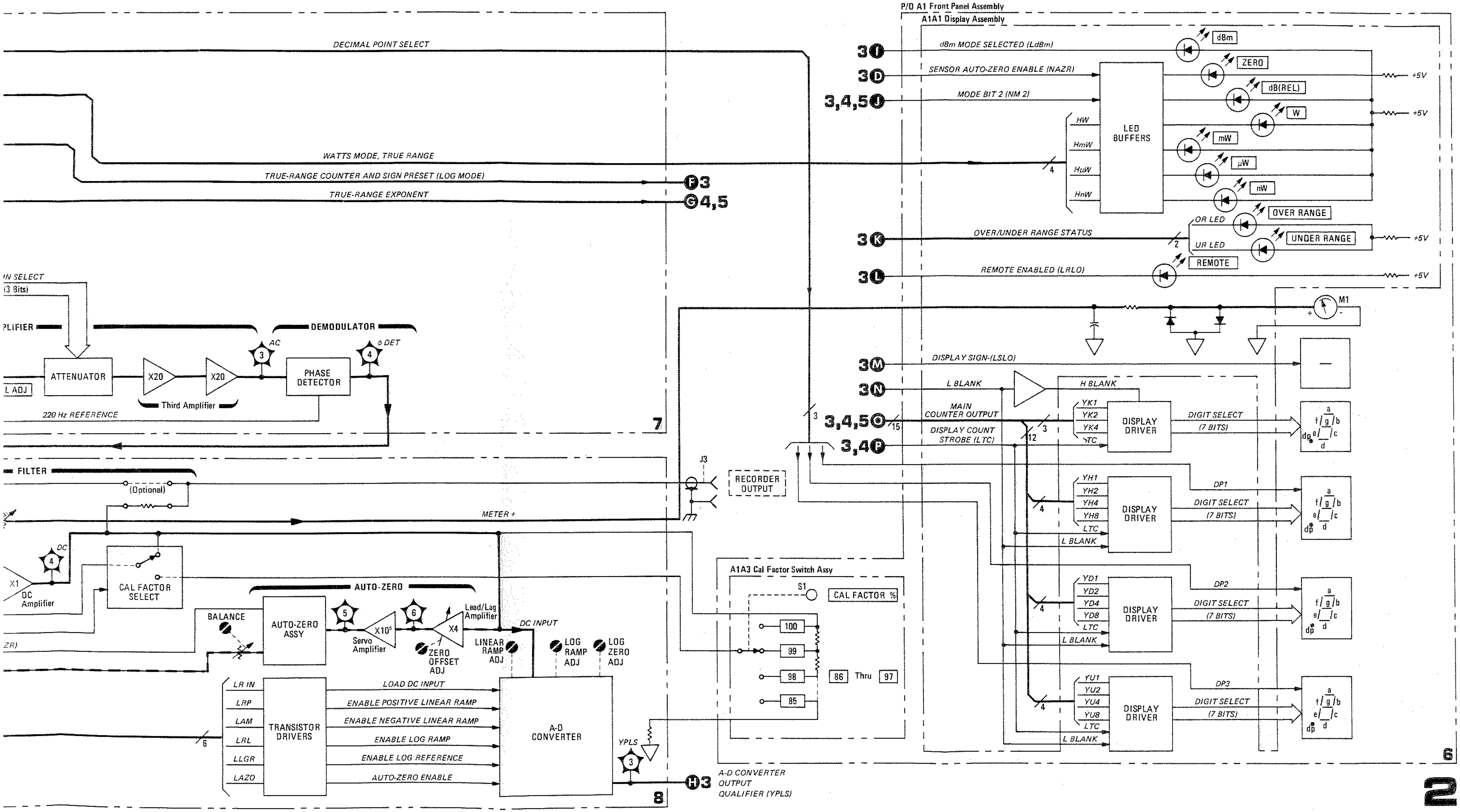
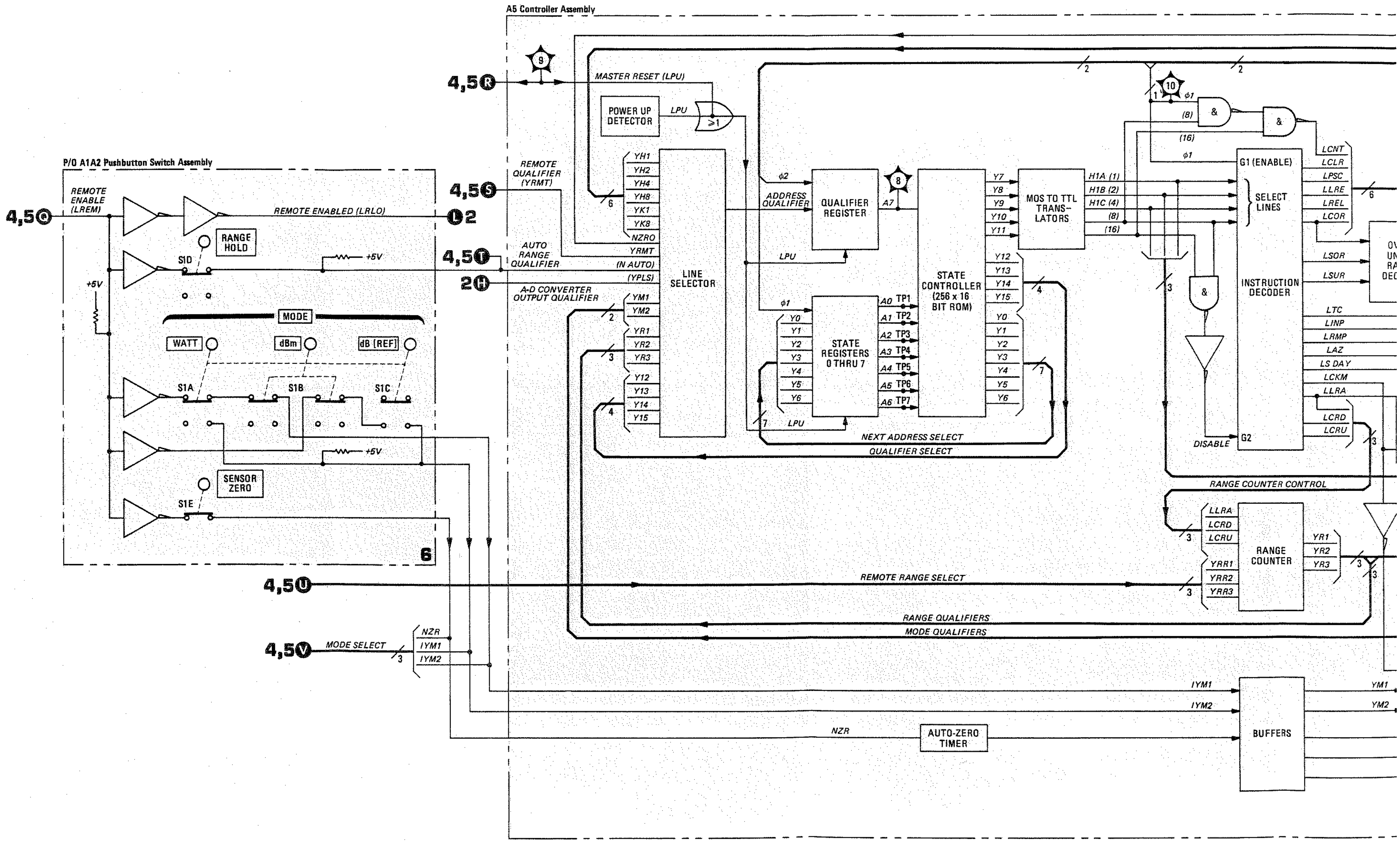


Figure 8-22. AC Gain, A-D Converter and Display Circuits Block Diagram

SERVICE SHEET 4

BLOCK DIAGRAM CIRCUIT DESCRIPTIONS

The Block Diagram Circuit Descriptions for Service Sheet 4 are covered in paragraphs 8-115 through 8-154, HP-IB Instrument Checkout in paragraphs 8-63 through 8-66, HP-IB Verification Programs in Figures 8-16 and 8-17, and Troubleshooting in Table 8-4.


A5 Controller Assembly
P/O A1A2 Pushbutton Switch Assembly
4,5Q
REMOTE ENABLE (LREM)
REMOTE ENABLED (LRLO)
L2
RANGE HOLD
S1D
+5V
MODE
WATT
dBm
dB (REF)
S1A
S1B
S1C
SENSOR ZERO
S1E
6
4,5R
MASTER RESET (LPU)
POWER UP DETECTOR
LPU
4,5S
REMOTE QUALIFIER (YRMT)
4,5T
AUTO RANGE QUALIFIER
2H
A-D CONVERTER OUTPUT QUALIFIER
YH1
YH2
YH4
YH8
YK1
YK8
NZRO
YRMT
(N AUTO)
(YPLS)
YM1
YM2
YR1
YR2
YR3
Y12
Y13
Y14
Y15
LINE SELECTOR
ADDRESS QUALIFIER
QUALIFIER REGISTER
A7
STATE REGISTERS 0 THRU 7
STATE CONTROLLER (256 x 16 BIT ROM)
TP1
TP2
TP3
TP4
TP5
TP6
TP7
NEXT ADDRESS SELECT
QUALIFIER SELECT
MOS TO TTL TRANS-LATORS
H1A (1)
H1B (2)
H1C (4)
(8)
(16)
G1 (ENABLE)
SELECT LINES
INSTRUCTION DECODER
G2
DISABLE
LCNT
LCLR
LPSC
LLRE
LREL
LCOR
LSOR
LSUR
LTC
LINP
LRMP
LAZ
LS DAY
LCKM
LLRA
LCRD
LCRU
RANGE COUNTER CONTROL
RANGE COUNTER
LLRA
LCRD
LCRU
YRR1
YRR2
YRR3
4,5U
REMOTE RANGE SELECT
RANGE QUALIFIERS
MODE QUALIFIERS
4,5V
MODE SELECT
NZR
IYM1
IYM2
AUTO-ZERO TIMER
BUFFERS

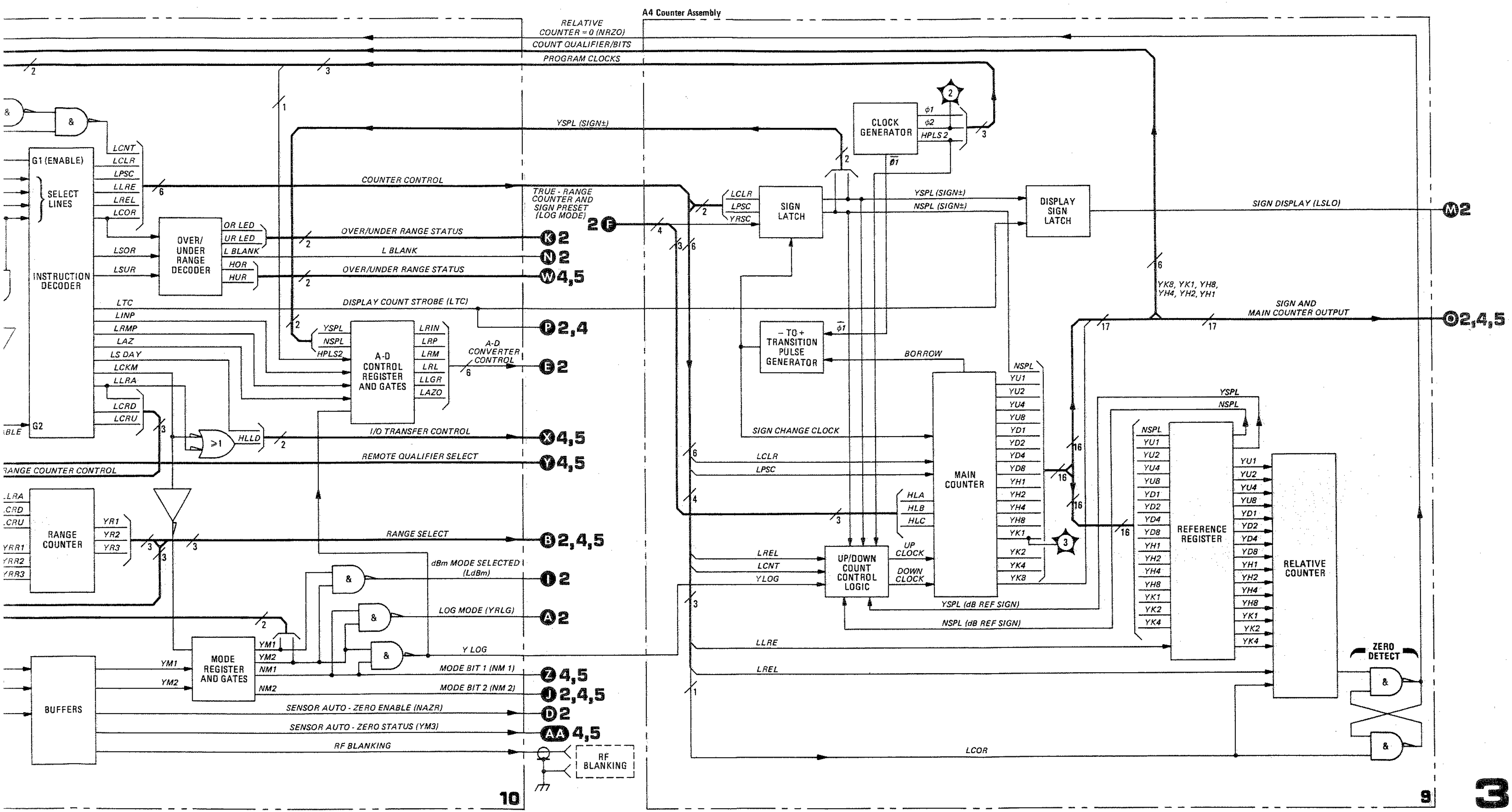
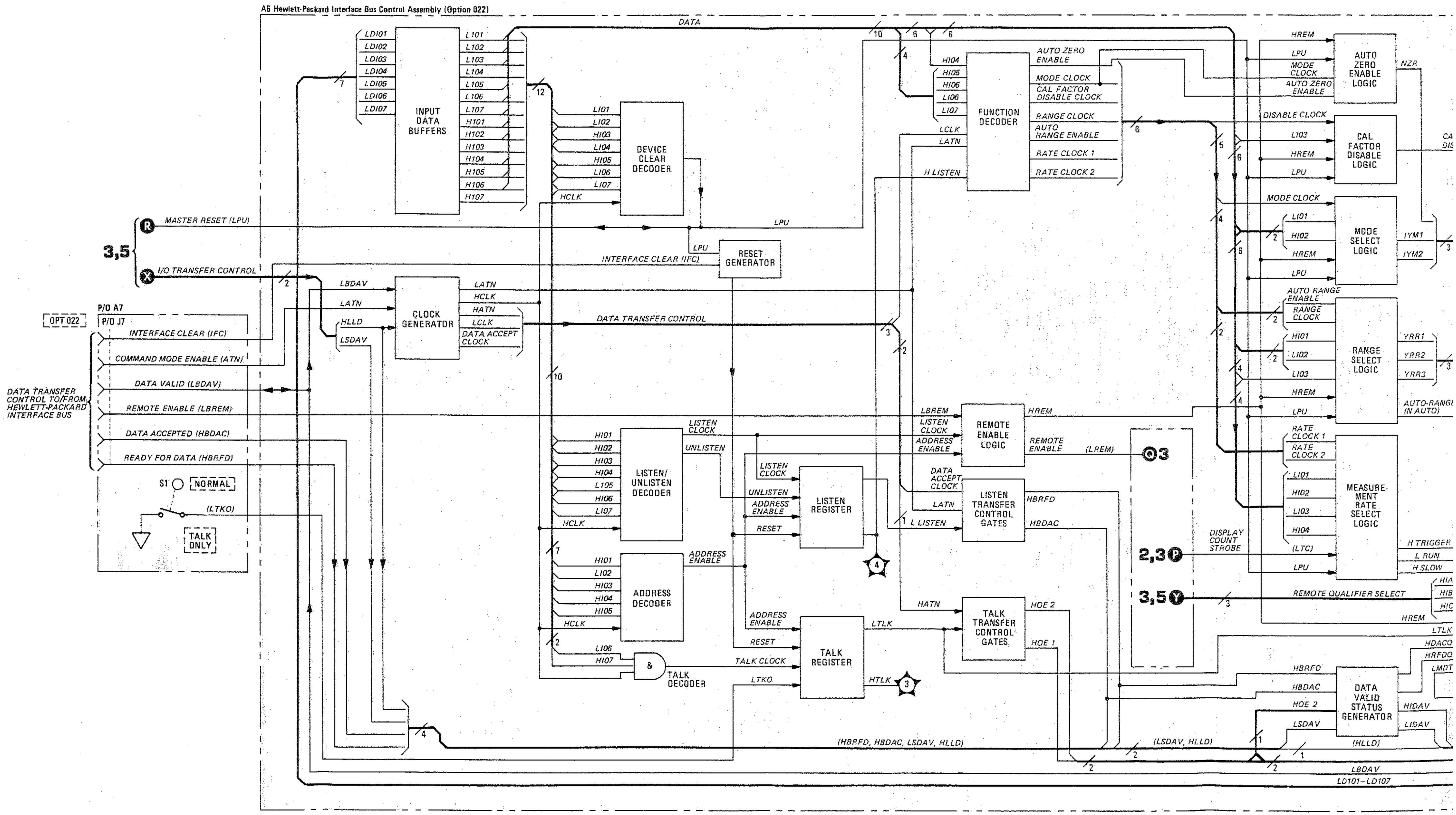


Figure 8-23. Controller and Counters Block Diagram


A6 Hewlett-Packard Interface Bus Control Assembly (Option 022)
INPUT DATA BUFFERS
DEVICE CLEAR DECODER
RESET GENERATOR
CLOCK GENERATOR
LISTEN/ UNLISTEN DECODER
ADDRESS DECODER
TALK DECODER
LISTEN REGISTER
TALK REGISTER
FUNCTION DECODER
REMOTE ENABLE LOGIC
LISTEN TRANSFER CONTROL GATES
TALK TRANSFER CONTROL GATES
AUTO ZERO ENABLE LOGIC
CAL FACTOR DISABLE LOGIC
MODE SELECT LOGIC
RANGE SELECT LOGIC
MEASURE-MENT RATE SELECT LOGIC
DATA VALID STATUS GENERATOR
MASTER RESET (LPU)
I/O TRANSFER CONTROL
3,5
OPT 022
P/O A7
P/O J7
INTERFACE CLEAR (IFC)
COMMAND MODE ENABLE (ATN)
DATA VALID (LBDAV)
REMOTE ENABLE (LBREM)
DATA ACCEPTED (HBDAC)
READY FOR DATA (HBRFD)
DATA TRANSFER CONTROL TO/FROM HEWLETT-PACKARD INTERFACE BUS
S1
NORMAL
TALK ONLY
(LTKO)
DATA
DATA TRANSFER CONTROL
INTERFACE CLEAR (IFC)
DISPLAY COUNT STROBE
REMOTE QUALIFIER SELECT
(HBRFD, HBDAC, LSDAV, HLLD)
(LSDAV, HLLD)
LBDAV
LD101–LD107
2,3
3,5
AUTO-RANGE (N AUTO)
H TRIGGER
L RUN
H SLOW

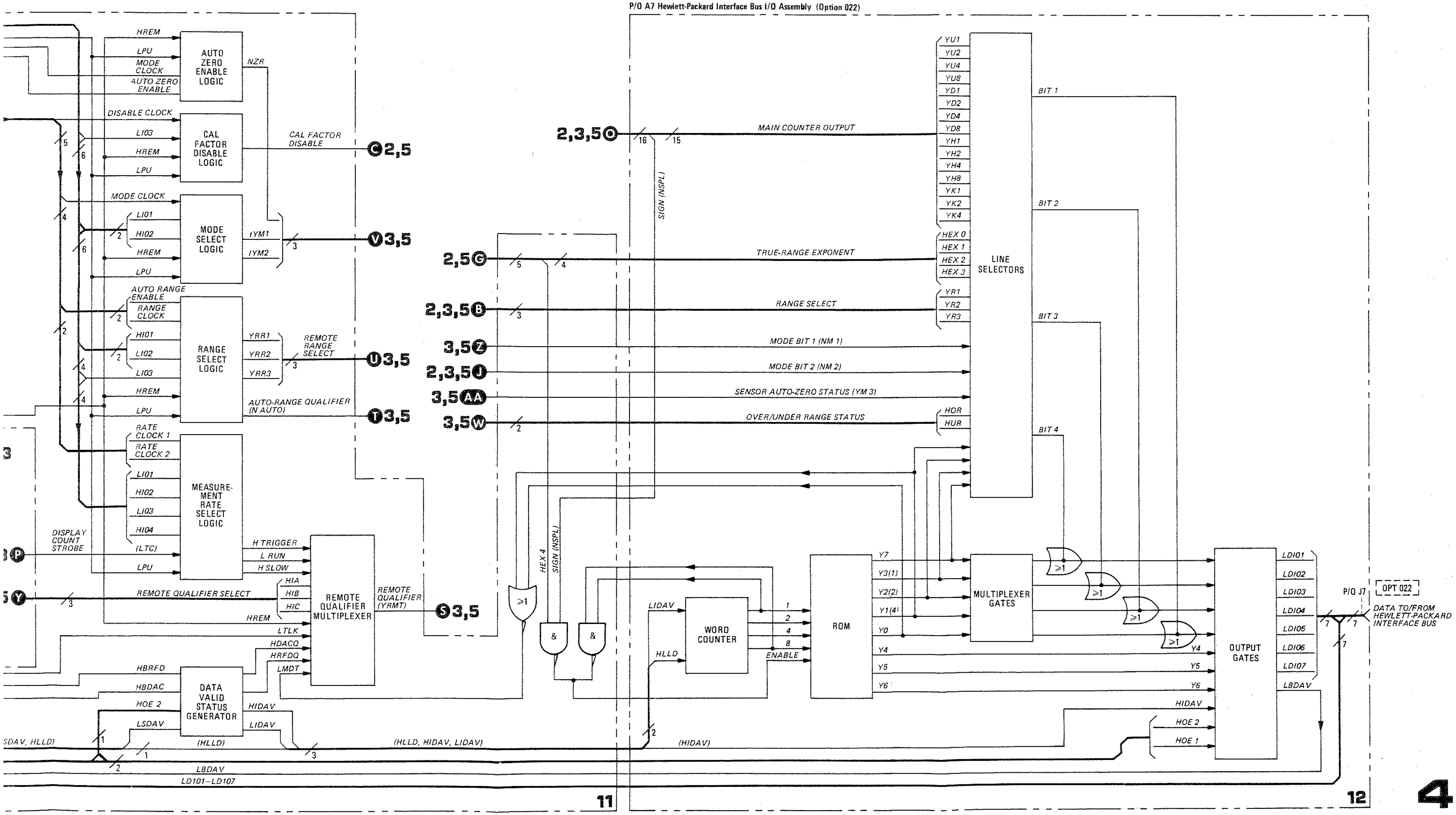


Figure 8-24. HP-IB (Option 022) Circuit Block Diagram

SERVICE SHEET 5 HAS BEEN DELETED

SERVICE SHEET 6

CIRCUIT DESCRIPTIONS

The circuits described in Service Sheet 6 are covered on Service Sheets 1 and 2 and Trouble-shooting in paragraphs 8-55 through 8-62.

Service Model 436A

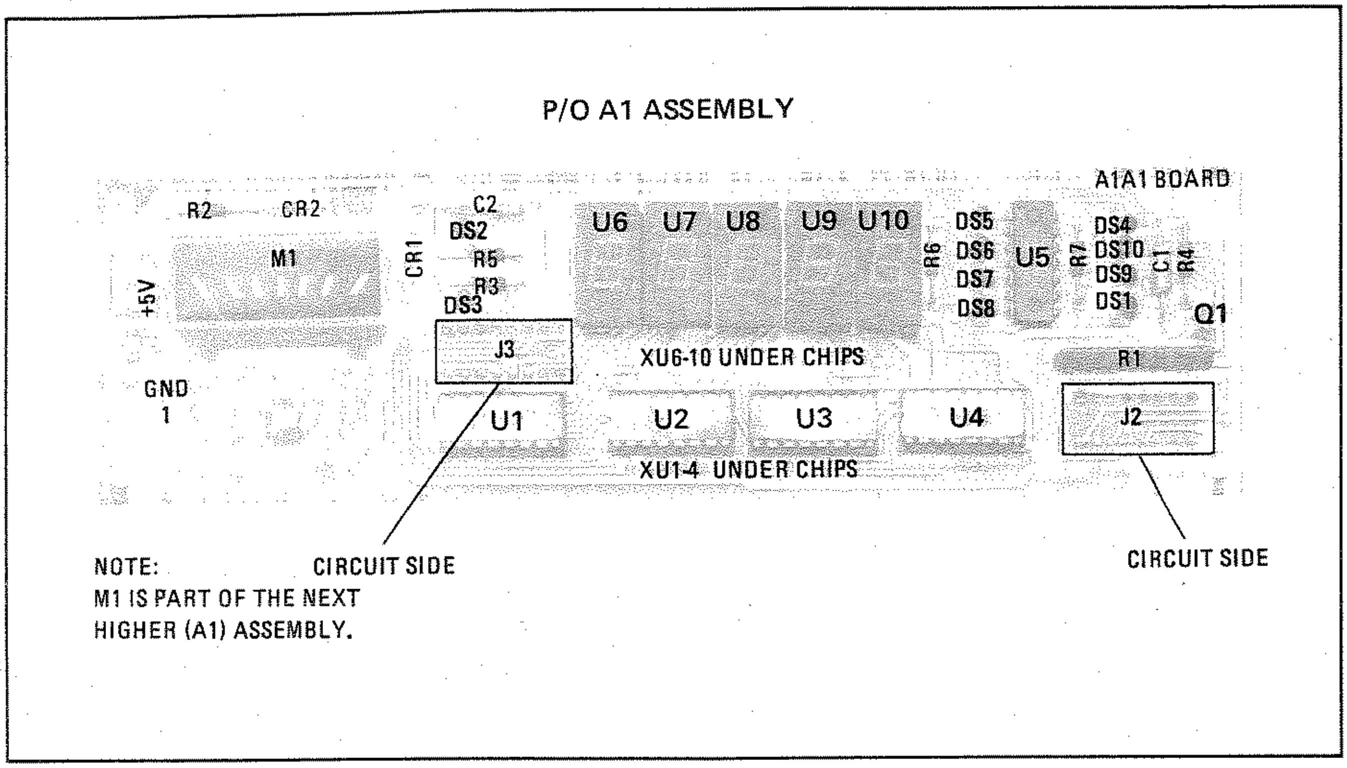


Figure 8-26. A1A1 Display Assembly Component Locations

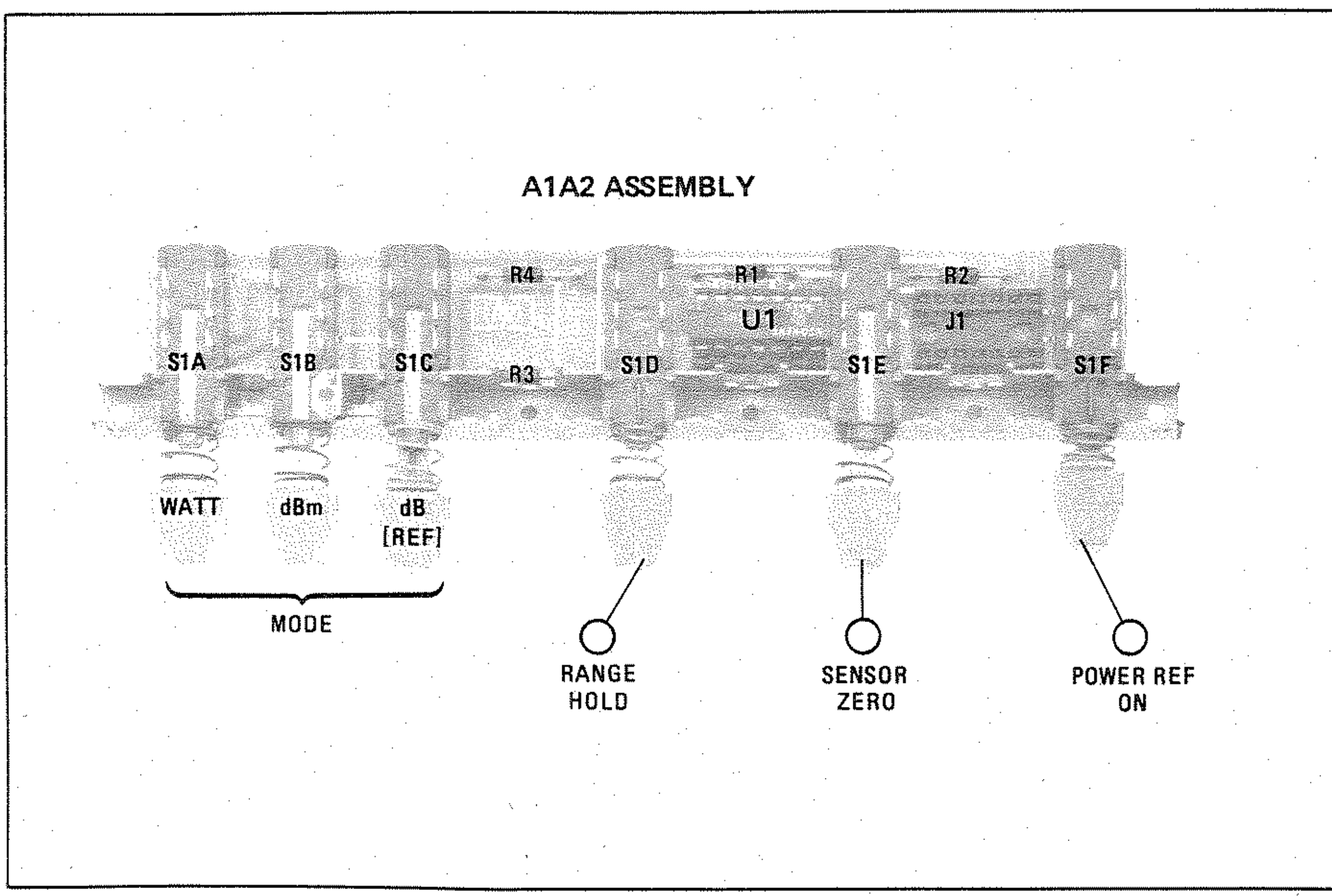


Figure 8-27. A1A2 Pushbutton Assembly Component Locations

Sensitivity Detector Logic

Maximum Range F.S.	U4B			U4A			U4C			U4D			U7			
	5	6	7	1	2	3	8	9	10	12	13	14	14	27	3	26
10 µW	6.1	11.9	0.0	13.7	5.4	6.1	0.7	8.5	6.1	6.1	7.1	0.0	0	1	0	0
100 µW	7.6	11.9	0.0	13.7	5.4	7.6	0.7	8.5	7.6	7.6	7.1	13.8	0	1	0	1
1 mW	9.0	11.8	0.0	13.7	5.4	9.0	13.8	8.5	9.0	9.0	10.1	0.0	0	1	1	0
10 mW	10.6	11.8	0.0	13.7	5.4	10.6	13.8	8.5	10.6	10.6	10.1	13.8	0	1	1	1
100 mW	0.0	11.8	0.0	.6	5.4	0.0	0.1	2.2	0.0	0.0	0.6	0.0	0	0	0	0
1W	1.5	11.8	0.0	.6	5.4	1.5	0.1	2.2	1.5	1.5	0.6	13.8	0	0	0	1
10W	2.9	11.8	0.0	.7	5.4	2.9	13.7	2.2	2.9	2.9	3.7	0.0	0	0	1	0
100W	4.5	11.8	0.0	.7	5.4	4.5	13.7	2.2	4.5	4.5	3.7	13.8	0	0	1	1
(Open) Error	15.1	11.8	13.8	13.7	5.4	15.1	13.8	8.5	15.1	15.1	10.1	13.8	1	1	1	1

All voltages shown are ± 0.1 Vdc.

Power Sensor Maximum and Minimum F. S. Ranges and Resistor Values

Power Sensor	Maximum Power Range F.S.	Minimum Power Range F.S.	Power Sensor Resistor Value
8484A	10 µW (–20 dBm)	1 nW (–60 dBm)	10.0kΩ
	100 µW (–10 dBm)	10 nW (–50 dBm)	14.7kΩ
	1 mW (0 dBm)	100 nW (–40 dBm)	21.5kΩ
	10 mW (+10 dBm)	1 µW (–30 dBm)	34.8kΩ
8481A/8482A/8483A	100 mW (+20 dBm)	10 µW (–20 dBm)	0Ω (Gnd)
	1 W (+30 dBm)	100 µW (–10 dBm)	1.62kΩ
8481H/8482H	10 W (+40 dBm)	1 mW (0 dBm)	3.46kΩ
8481B/ 8482B	100 W (+50 dBm)	10 mW (+10 dBm)	6.19kΩ

Input and Output Code for A2U6 ROM

Input & Pin No.	Range 1	2	3	4	5
YR1 10	1	0	1	0	1
YR2 11	0	1	1	0	0
YR3 12	0	0	0	1	1

1 = 5V; 0 ⩽ 0.3V

Range 1	2	3	4	5	Output Pin No.
0	0	0	1	1	9
1	1	1	0	0	7
0	1	1	1	1	6
1	0	1	0	1	5
1	1	0	1	0	4
0	1	1	1	1	3
1	0	0	0	0	2
1	0	1	1	1	1

1 = 0.6V; 0 = 0.1V

CIRCUIT DESCRIPTIONS

General

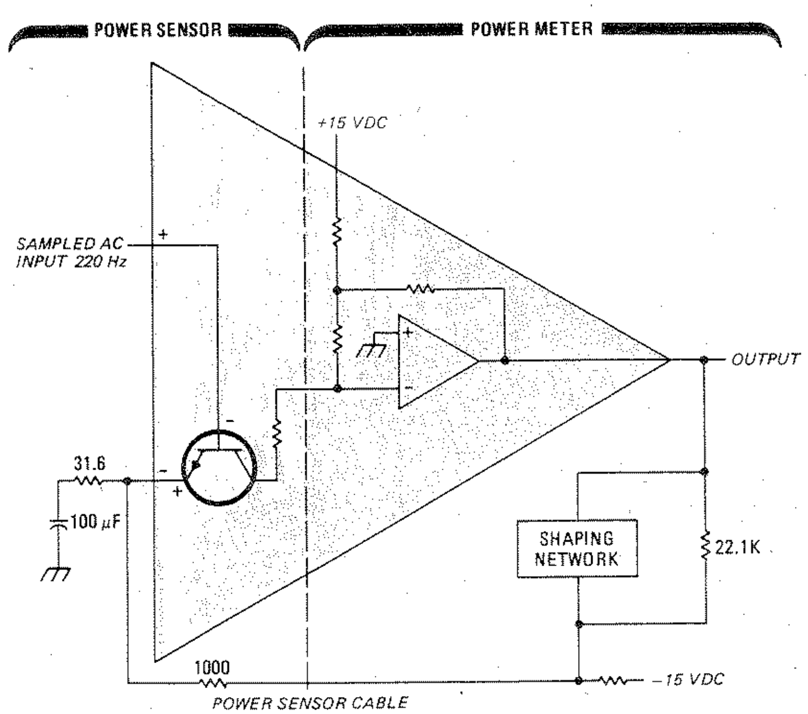
The RF input power applied to the Power Sensor is dissipated by the load impedance of the power sensing device. The dc output of the power sensing device is converted to a 220 Hz ac signal by a sampling gate (chopper) circuit. The ac signal, which is proportional to the RF input, is amplified by tuned ac amplifier stages in the Power Sensor and Power Meter. The Phase Detector converts the amplified 220 Hz ac signal back to a dc level which is proportional to the RF input power level.

The Attenuator reduces the ac signal for high power inputs. This allows equal measurement resolution for high and low power levels. The Phase Detector and a sampling gate circuit (in the Power Sensor) are driven in phase by the 220 Hz Multivibrator's outputs.

A2U5B is connected as a voltage follower between the Mount Return line and Analog Ground. This circuit ensures that a minimum voltage difference exists between the grounds thereby eliminating the possibility of unreliable readings. High current flow, through the ground return of cables which are greater than 1.52 meters (5 feet) long, causes the voltage difference.

First Amplifier

The First Amplifier of the Power Meter and the Power Sensor's output amplifier stage form a low-noise high-gain hybrid operational amplifier (refer to the figure below). The ac gain is approximately 600; dc bias is set by A2R1, R2, R5, R6, and R7.



Hybrid Operational Amplifier

Diodes A2CR1, CR2, VR1, and VR2 and their associated components are part of a shaping network which compensates for the non-linear output of the Power Sensor's sensing device. At RF inputs near the maximum power input (100 mW for Model 8481A) the power sensing device is slightly more efficient and the hybrid amplifier's gain is reduced slightly to provide a linear overall response.

The combination of A2C5, R10, and R11 is one of three RC networks in the ac amplifiers which determine the high frequency cutoff (240 Hz) of the 220 ± 20 Hz bandpass. A2C3, C4, and C6 are line noise filters.

Attenuator and Second Amplifier Assemblies

The Attenuator Networks and associated components on the A2 assembly form two separate attenuators and a variable low pass filter.

With high power RF inputs, relatively high voltages are coupled to the attenuator inputs. The higher the voltage the more it is attenuated, thus allowing for greater sensitivity needed for low power measurements while providing the needed resolution for each range. The various levels of attenuation permit five usable ranges whose values are determined by the Power Sensor being used. The following table shows the individual and combined effects of the attenuators on the ac signal. The attenuation resistors, therefore the value of attenuation, is selected by the outputs from the ROM A2U6 applied to the transistors A2Q21 through A2Q25.

RANGE	Attenuation		
	Network #1 (A2R24 & R25)	Network #2 (A2R37, R38, and R39)	Total
1	÷ 1	÷ 1	÷ 1
2	÷ 1	÷ 10	÷ 10
3	÷ 1	÷ 100	÷ 10^2
4	÷ 100	÷ 10	÷ 10^3
5	÷ 100	÷ 100	÷ 10^4

The bandpass of the ac amplifiers in the Power Meter is approximately 220 ± 20 Hz. The lower cutoff frequency (200 Hz) is fixed by the combination of A2C8 with A2R24 and R25; also A2C11 with A2R37, R38, and R39.

Second Amplifier

A2U1 and its associated components form an operational amplifier stage with variable voltage gain from 5 to 18. The front panel CAL ADJ gain control is set to compensate for differences in sensitivity of individual Power Sensors. The gain is determined by A2R28, R33, and the CAL ADJ control R16.

Third Amplifier

A2U2A and B and associated components are operational amplifiers with voltage gains of about 20 each. Gain for A2 U2A is determined by A2R52 and R53; for A2U2B by A2R48 and R49. Bias current is provided for A2U2A by A2R50.

The tuned amplifiers upper bandpass limit (240 Hz) is set by the parallel RC network of A2C12 and R48; A2C14 and R52; also in conjunction with a parallel RC network in the First Amplifier.

Phase Detector

The Phase Detector, like the sampling gate circuit in the Power Sensor, is driven by the 220 Hz Multivibrator drive signal. The 220 Hz switching signal (0 to −10 Vdc) is applied through the voltage divider A2R61 and R67 to the base of A2Q14 at a level of 0 to −0.6 Vdc. This signal turns Q14 on and off and causes the collector voltage to vary from 0 to −15 Vdc. The collector voltage from Q14 is applied to the base of A2Q13 through the voltage divider A2R60 and R62. This signal turns Q13 off and on causing the collector voltage to vary from 0 to −15 Vdc at a 220 Hz rate. The collector voltage from Q13 is applied to the gate of the n-channel FET Q12. This gate drive causes Q12 to turn on and off. When Q12 turns off, U8 operates as an amplifier with a gain of 1. When Q12 turns on, the non-inverting input to U8 is grounded, causing U8 to operate as an inverting amplifier with a gain of −1. Any phase difference between the 220 Hz input signal to U8 and the 220 Hz switching signal from Q12 will cause the output of U8 pin 6 to be offset from the zero dc baseline. The output of the Phase Detector is applied to the A3 A-D Converter Assembly.

Sensor Sensitivity Detector and True Range Decoder

The Sensor Sensitivity Detector circuit consists of U4A, B, C, D and associated components. The True Range Decoder consists of U7 and U3.

The Sensor Sensitivity Detector, U4A, B, C, and D, provides inputs to the True Range Decoder, U7 along with the Range Counter (YR1, YR2, and YR3) in Local Mode, the programmed range inputs (YRR1, YRR2, and YRR3) when in Remote Mode, and YRLR input to give the correct range indication and decimal point location for the RF input power level being measured by the Power Sensor.

The Sensor Sensitivity Detector provides one input code to the True Range Decoder determined by the Power Sensor being used. When the non-inverting inputs to U4A, B, C, and D are the less positive inputs, the outputs are at approximately 0 volts (ground). When the non-inverting inputs are the more positive inputs, the outputs are approximately +15 volts (see tables below). The level

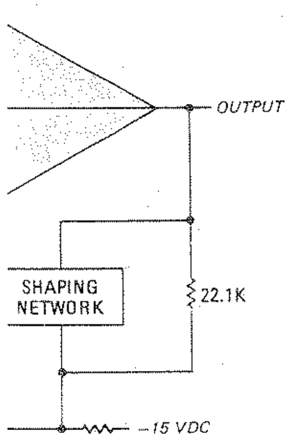
r Sensor is dissipated by
ɪevice. The dc output of
a 220 Hz ac signal by a
ac signal, which is
d by tuned ac amplifier
ter. The Phase Detector
ɪck to a dc level which is

high power inputs. This
or high and low power
ing gate circuit (in the
220 Hz Multivibrator's

ver between the Mount
circuit ensures that a
en the grounds thereby
readings. High current
s which are greater than
ge difference.

and the Power Sensor's
noise high-gain hybrid
below). The ac gain is
1, R2, R5, R6, and R7.

METER



lifier

Diodes A2CR1, CR2, VR1, and VR2 and their associated components are part of a shaping network which compensates for the non-linear output of the Power Sensor's sensing device. At RF inputs near the maximum power input (100 mW for Model 8481A) the power sensing device is slightly more efficient and the hybrid amplifier's gain is reduced slightly to provide a linear overall response.

The combination of A2C5, R10, and R11 is one of three RC networks in the ac amplifiers which determine the high frequency cutoff (240 Hz) of the 220 ± 20 Hz bandpass. A2C3, C4, and C6 are line noise filters.

Attenuator and Second Amplifier Assemblies

The Attenuator Networks and associated components on the A2 assembly form two separate attenuators and a variable low pass filter.

With high power RF inputs, relatively high voltages are coupled to the attenuator inputs. The higher the voltage the more it is attenuated, thus allowing for greater sensitivity needed for low power measurements while providing the needed resolution for each range. The various levels of attenuation permit five usable ranges whose values are determined by the Power Sensor being used. The following table shows the individual and combined effects of the attenuators on the ac signal. The attenuation resistors, therefore the value of attenuation, is selected by the outputs from the ROM A2U6 applied to the transistors A2Q21 through A2Q25.

RANGE	Attenuation		
	Network #1 (A2R24 & R25)	Network #2 (A2R37, R38, and R39)	Total
1	÷ 1	÷ 1	÷ 1
2	÷ 1	÷ 10	÷ 10
3	÷ 1	÷ 100	÷ 10^2
4	÷ 100	÷ 10	÷ 10^3
5	÷ 100	÷ 100	÷ 10^4

The bandpass of the ac amplifiers in the Power Meter is approximately 220 ± 20 Hz. The lower cutoff frequency (200 Hz) is fixed by the combination of A2C8 with A2R24 and R25; also A2C11 with A2R37, R38, and R39.

Second Amplifier

A2U1 and its associated components form an operational amplifier stage with variable voltage gain from 5 to 18. The front panel CAL ADJ gain control is set to compensate for differences in sensitivity of individual Power Sensors. The gain is

determined by A2R28, R33, and the CAL ADJ control R16.

Third Amplifier

A2U2A and B and associated components are operational amplifiers with voltage gains of about 20 each. Gain for A2 U2A is determined by A2R52 and R53; for A2U2B by A2R48 and R49. Bias current is provided for A2U2A by A2R50.

The tuned amplifiers upper bandpass limit (240 Hz) is set by the parallel RC network of A2C12 and R48; A2C14 and R52; also in conjunction with a parallel RC network in the First Amplifier.

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The Phase Detector, like the sampling gate circuit in the Power Sensor, is driven by the 220 Hz Multivibrator drive signal. The 220 Hz switching signal (0 to −10 Vdc) is applied through the voltage divider A2R61 and R67 to the base of A2Q14 at a level of 0 to −0.6 Vdc. This signal turns Q14 on and off and causes the collector voltage to vary from 0 to −15 Vdc. The collector voltage from Q14 is applied to the base of A2Q13 through the voltage divider A2R60 and R62. This signal turns Q13 off and on causing the collector voltage to vary from 0 to −15 Vdc at a 220 Hz rate. The collector voltage from Q13 is applied to the gate of the n-channel FET Q12. This gate drive causes Q12 to turn on and off. When Q12 turns off, U8 operates as an amplifier with a gain of 1. When Q12 turns on, the non-inverting input to U8 is grounded, causing U8 to operate as an inverting amplifier with a gain of −1. Any phase difference between the 220 Hz input signal to U8 and the 220 Hz switching signal from Q12 will cause the output of U8 pin 6 to be offset from the zero dc baseline. The output of the Phase Detector is applied to the A3 A-D Converter Assembly.

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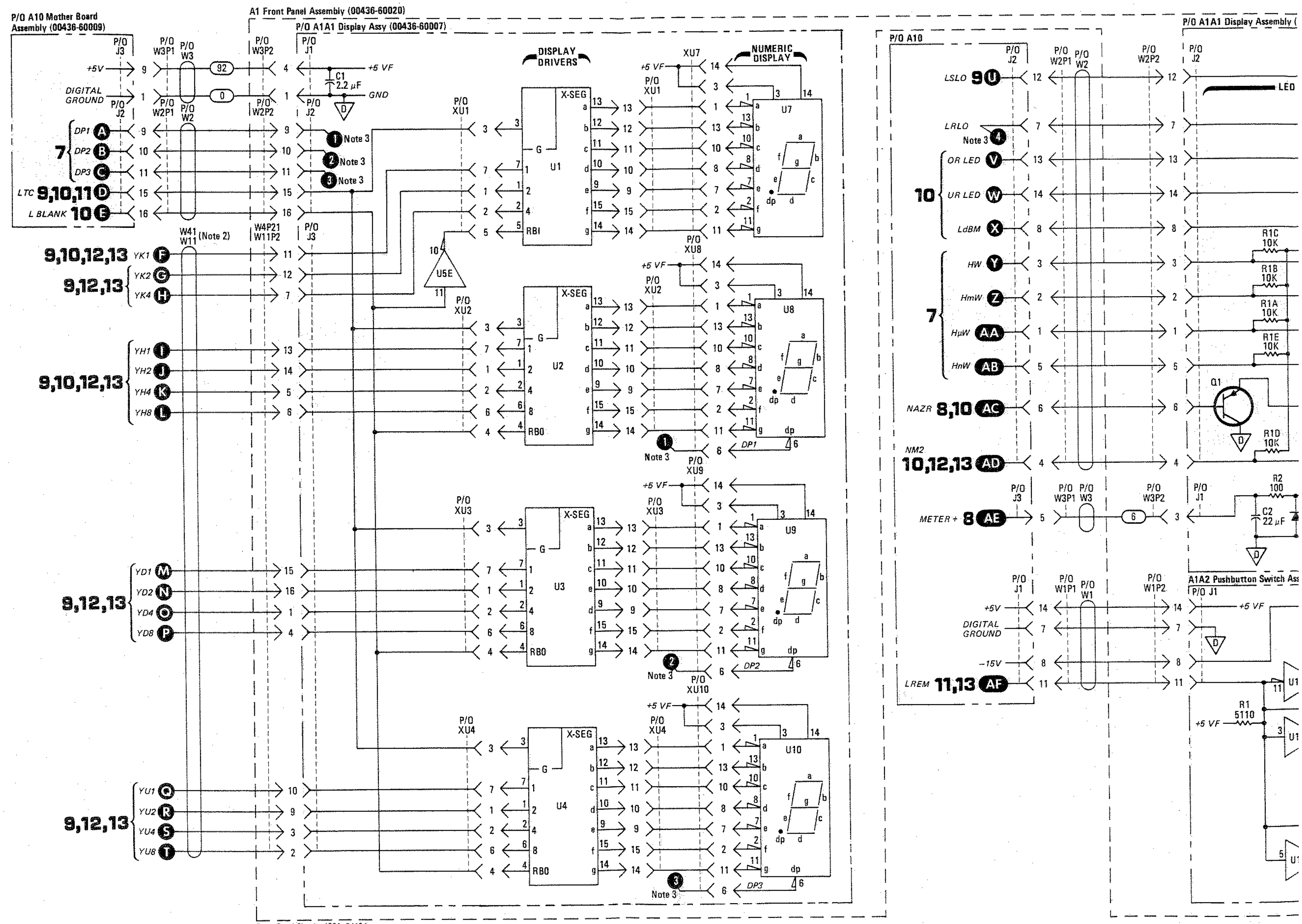
The Sensor Sensitivity Detector provides one input code to the True Range Decoder determined by the Power Sensor being used. When the non-inverting inputs to U4A, B, C, and D are the less positive inputs, the outputs are at approximately 0 volts (ground). When the non-inverting inputs are the more positive inputs, the outputs are approximately +15 volts (see tables below). The level

on non-inverting inputs to U4A, B, C, and D is determined by the voltage divider composed of A2R13 and the Sensor Resistor (see tables below). When the Sensor Resistor is 0 ohms (GND), the outputs of U4 are approximately 0 volts.

For a 10W maximum input to the Power Sensor, the Sensor Resistor is approximately 3.46k ohms and the voltage level at the non-inverting inputs of U4 is approximately +2.8 volts. The output of U4C changes to approximately +15 volts. This change was caused by the non-inverting input going more positive than the inverting input level which is approximately +2 volts. The inverting input level is determined by the voltage divider composed of A2R29, R30, and R31. A2R29 is in parallel with R31 to ground. When the output of U4C changes to +15 volts, the inverting input to U4D changes to approximately +4 volts because now R36 and R40 are in parallel with the +15 volts applied and R32 and R41 are in parallel to ground, thus forming a series parallel network between ground and +15 volts. The table below gives the complete list of U4 inputs and outputs for each Sensor Resistor and the logic input codes to U7.

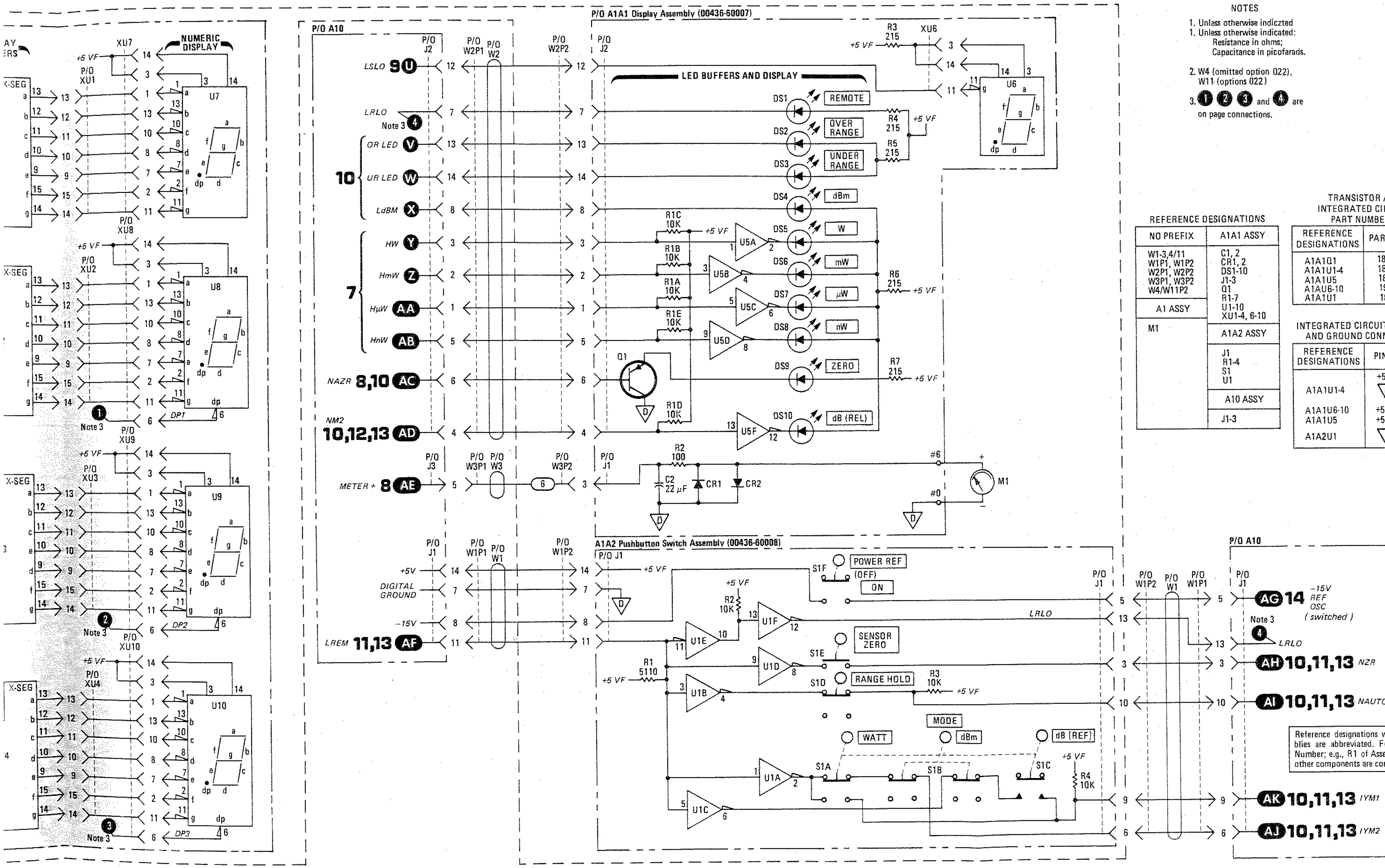
Front Panel Assembly
(A1A1, A1A2)
SERVICE SHEET 6



Front Panel Circuits 436A: 2410A

NOTES

1. Unless otherwise indiczted
1. Unless otherwise indicated:
Resistance in ohms;
Capacitance in picofarads.
2. W4 (omitted option 022).
W11 (options 022)
3. ❶ ❷ ❸ and ❹ are on page connections.



REFERENCE DESIGNATIONS

NO PREFIX	A1A1 ASSY
W1-3,4/11 W1P1, W1P2 W2P1, W2P2 W3P1, W3P2 W4/W11P2	C1, 2 CR1, 2 DS1-10 J1-3 Q1 R1-7 U1-10 XU1-4, 6-10
A1 ASSY	A1A2 ASSY
M1	J1 R1-4 S1 U1
	A10 ASSY
	J1-3

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBER
A1A1Q1	1853-0020
A1A1U1-4	1820-1361
A1A1U5	1820-0174
A1AU6-10	1990-0490
A1A1U1	1820-0175

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBER
A1A1U1-4	+5 VF – 16 D – 8
A1A1U6-10 A1A1U5	+5 VF – 3,14 +5 VF – 14
A1A2U1	D – 7

Reference designations within outline (— — —) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

6

A1,A1A1, A1A2,A10

Figure 8-28. Front Panel Assembly Schematic Diagram

SERVICE SHEET 8 (cont'd)

TROUBLESHOOTING

General

Before attempting to troubleshoot these circuits, verify that the power supply is operating properly. The voltages should be +5 Vdc, +15 Vdc, and −15 Vdc.

If the dc offset controls A3R2, A3R47, or A3R65 are incorrectly adjusted, the Auto-Zero circuits may not respond properly. Refer to the adjustment procedures in Section V.

Noise problems may be due to defective components in the Variable Low Pass Filter (especially in the two most sensitive ranges) or the Lead/Lag Amplifier which is an active low pass filter. A noise problem in the Lead/Lag Amplifier will be evident only during the zeroing sequence.

DC Amplifier, Lead/Lag Amplifier, and Servo Amplifier

Measure the dc input and output voltages. Verify that the amplifier outputs respond properly to the inputs. For troubleshooting operational amplifiers refer to Linear Integrated Circuits in Section VIII. A Servo Amplifier problem will be evident only during the Sensor-Zero sequence.

Auto Zero Assembly

The normal value range of the offset error voltage at A3A1, pin 5 is about −14 to +14 mVdc. The power sensing device normally exhibits a slight positive output due to ambient temperature, therefore the normal correction voltage is slightly negative, hence −4 mVdc.

The voltage measured at A3TP6 will provide an indication of how long the charge is retained on A3A1C_A. The voltage should remain virtually unchanged (±1 mVdc) for 24 hours.

If any component in the A3A1 assembly is found to be defective, the entire assembly must be replaced.

A-D Converter Circuit

Set Power Meter to Watt Mode and apply a 1.0 mW input signal to Power Sensor. Check that Power Meter is on range 3 and A3TP4 (DC) should be approximately +1.0 Vdc. Check A3TP2 (RMP) for a 0 to −7.0 volt ramp with a time of approximately 33.3 ms. If ramp does not reach −7.0 volts with 1.0 Vdc at A3TP4 (DC), check that LRIN instruction on XA3 pin 24 is pulsed low for 33.3 ms to turn transistors A3Q11 and A3Q12 off and FET A3Q13 on. Check that ramp at A3TP2 decreases from −7 volts to 0 volts at a linear rate. Check −VR at collector of A3Q17, approximately −6.2 Vdc and +VR at A3U5B pin 7, approximately +6.2 Vdc. The LRP instruction on XA3 pin 25 is pulsed low in the Watt Mode to turn transistors A3Q1 and A3Q6 off and FET A3Q16 on causing a positive linear ramp to be generated. The LRM instruction on XA3 pin 26 is pulsed low in the Watt Mode to turn transistors A3Q2 and A3Q7 off and FET A3Q15 on causing a negative linear ramp to be generated. LRM and LRP instructions remain high when dBm, dB [REF], or dB (REL) Modes are selected.

Set Power Meter to dBm Mode and apply a 1.0 mW input signal to Power Sensor. Check that ramp at A3TP3 decreases from −7.0 volts to threshold (reference) level at a log rate. Check that LLGR and LRL instructions on XA3 pins 3 and 4 respectively are pulsed low in dBm, dB [REF], and dB (REL) Modes. The LRL instruction turns transistors A3Q4 and A3Q9 off and FET A3Q19 on applying the LOG REF (Threshold) signal to A3U2 pin 3. The output of A3U1 pin 6 must discharge past this level before the voltage at A3TP3 (YPLS) can switch to 0 volts. LLGR and LRL instructions remain high in the Watt Mode.

Check that the LAZO instruction at XA3 pin 2 is pulsed low. This turns transistors A3Q5 and A3Q10 off and turns FETs A3Q14 and A3Q20 on causing A3TP3 (YPLS) to be +2.0 volts dc during the A-D Converter's Auto-Zero cycle.

A3TP3 (YPLS) is at +5 volts while the ramps are discharging, at 0 Vdc when the Comparator, A3U2, switches from high to low, and at +2 Vdc during the A-D Auto-Zero cycle.

The time that each instruction remains low is determined by the program.

VICE SHEET 8

CUIT DESCRIPTIONS

eral

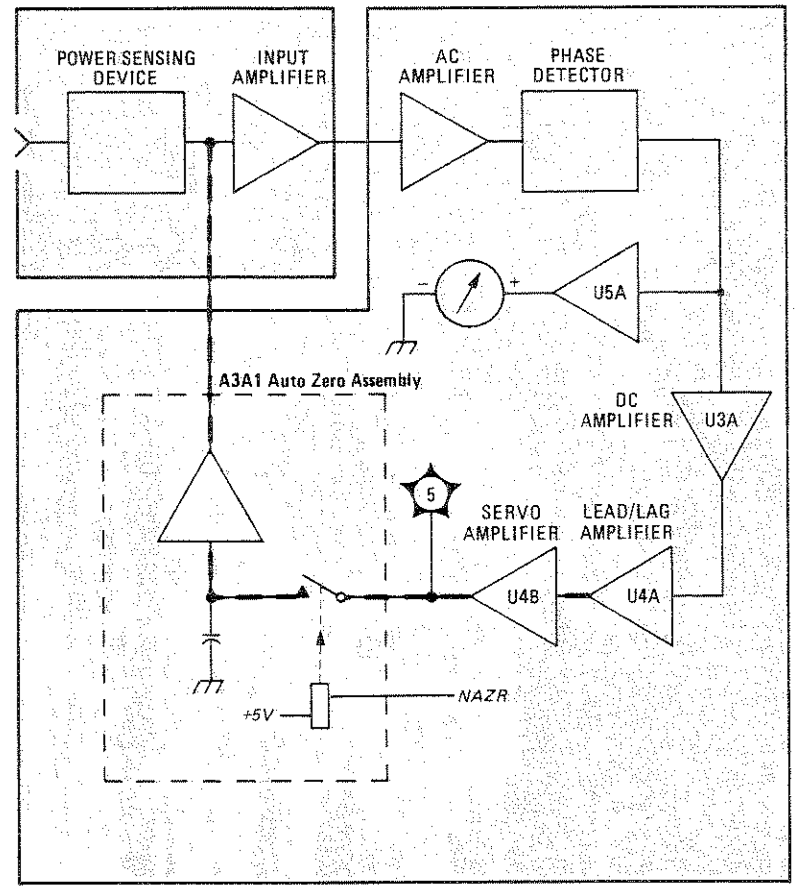
Phase Detector's output signal is applied to the Meter plifier and Limiter circuits. The input signal passes through the iter and Variable Low-Frequency Filter circuits before being lified by the DC Amplifier. The gain of the DC Amplifier is rolled by the setting of the CAL FACTOR % switch, A1S2. output of the DC Amplifier is applied to the Cal Factor Select iit, Lead/Lag Amplifier, RECORDER OUTPUT connector, the A-D Converter. The Meter Amplifier provides the ssary drive for the front panel meter (M1). It also provides an ltered signal for the rear panel RECORDER OUTPUT nector if the standard connection of A3R69 is not desired. The l/Lag Amplifier maintains the phase-gain response of the back loop in a stable mode. The Servo Amplifier has an grator in its feedback loop (C16 and R54) which also shapes overall phase-gain response of the Auto-Zero feedback path.

Servo Amplifier generates an error voltage if the DC plifier's output is not near zero volts. Without an RF input ied to the Power Sensor, the DC Amplifier's output is very e to 0 Vdc. When the SENSOR ZERO switch is depressed, or Sensor-Zero Remote command is enabled (NAZR), causing ZERO lamp to light, the relay in A3A1 to close its contacts, the Servo Amplifier's output to produce an error offset age. This error voltage is applied to the Auto-Zero Assembly A1) from where it is processed and summed with the output n the Power Sensor's sensing element. This composite voltage vides a correction signal of equal dc level but opposite polarity the output of the sensing element with no RF input signal lied. With the corrected input voltage, the DC Amplifier's put is exactly 0 Vdc. When the SENSOR ZERO switch is ased, or the NAZR signal is disabled, the Servo Amplifier's put voltage level is stored within the Auto-Zero Assembly and correction voltage remains coupled across the sensing element il another Auto-Zero correction is needed.

Transistor Drivers provide buffering and signal level version for the A-D Converter's control signals. The A-D nverter provides either a negative or positive linear or onential ramp to the Comparator. The Comparator's output 'LS) at A3TP3 is either high or low, if the A-D Converter's eshold is above or below the dc input signal level and is midway ween high and low during the A-D Converter's Auto-Zero le.

niter and Variable Low-Pass Filter Circuits

e Limiter circuit clips over-range outputs from the Phase tector to reduce the time for the Variable Low-Pass Filter to over from a greater than full-scale change in the input signal el. The response time of the Filter varies with the bandpass ected by the ROM's outputs (D1, F1, and F2). For ranges 5, 4, d 3, the bandpass is 17 Hz. For ranges 2 and 1, the bandpass is



Auto-Zero Feedback Path

reduced by factors of 10 to 1.7 and 0.17 Hz, respectively. The bandpass values represent the optimum tradeoff between filter response time and signal-to-noise ratio. On the higher ranges (3, 4, and 5), the gain of the Power Meter is relatively low and the 17 Hz bandpass enables the Filter to respond to a full-scale change in input level in 0.1 second (see Figure 3-7). On the lower ranges (1 and 2), the gain of the Power Meter increases and a higher noise level is present at the output of the Phase Detector. Thus, a narrower bandpass is required to maintain the desired signal-to-noise ratio at the input of the A-D Converter. The time required for the Filter to respond to a full-scale change in input level is one second on range 2 and ten seconds on range 1. Resistors A3R16, R22, R26, and R30 modify the Power Meter's Sensor-Zero feedback loop phase-gain response to maintain stability in the loop.

DC Amplifier

The output from the Variable Low-Pass Filter is applied to the input of the DC Amplifier. The DC OFF (DC Offset) control is adjusted to eliminate any dc offset voltage introduced by the DC Amplifier. The gain of the DC Amplifier is one when the CAL FACTOR % switch is set to the 100 position. The gain increases by approximately 1% for each lower-numbered switch

position. The output of the DC Amplifier is applied to the A-D Converter, the RECORDER OUTPUT connector, and the Lead/Lag Amplifier circuits.

Lead/Lag Amplifier and Servo Amplifiers

The output signal from the DC Amplifier is applied to the non-inverting input of U4A. The Lead/Lag Amplifier and Servo Amplifier are connected in series in the Sensor-Zero feedback loop and function only when the SENSOR ZERO switch is depressed or the Remote Interface produces a Sensor Zero command. R46 and C11 form a high frequency roll-off filter at the input to U4A. Capacitors C14 and C15 form a 0.5 μF non-polarized capacitor for the feedback across U4A. The combination of C13, C14, C15, R52, R53, and R55 reduce the high frequency response of U4A, while increasing the low frequency response of U4A. The output from U4A is applied to the non-inverting input of U4B, Servo Amplifier. VR4 and VR5 act to prevent the output of U4B from going more than ± 8.25V. The output from U4B is applied to the input of the Auto-Zero Assembly (A3A1). The source signal from the FET, A3A1 Q_A, is fed back to the inverting input of U4B through C16 and R54. The feedback path of U4B is an integrator that causes the high frequencies to be reduced. The output from the Auto-Zero Assembly is applied to the Power Sensor to develop a correction voltage that is input back to the DC Amplifier. This correction voltage is stored in capacitor A3A1C_A. When the SENSOR ZERO switch is released, this voltage holds the correction voltage constant at the Power Sensor. The special construction of the A3A1 assembly and the high gate impedance of A3A1Q_A reduces the leakage from A3A1C_A and therefore increases the storage time of the correction voltage. A3R65 BAL (Balance) control is provided to center the Auto-Zero circuit's output voltage range. (See Section V, Spike Balance Adjustment).

Transistor Drivers

The Transistor Driver circuits consist of transistors A3Q1 through A3Q12 and associated components. The Transistor Drivers provide buffering and signal level conversion for the control signals being applied to the A-D Converter from the Controller Assembly A5.

Transistors A3Q1 through A3Q12 are connected to provide a level transformation from TTL logic levels of 0 and +5 volts to 0 and −15 volts required to turn on and off the FET switches in the A-D Converter.

A-D (Analog-To-Digital) Converter

The A-D Converter Auto-Zero Enable (LAZO) signal causes FET's A3Q14 and A3Q20 to conduct. A3Q14's conduction holds the inverting input of A3U1 pin 2 low. A3Q20's conduction closes a feedback path from the output of the comparator (A3U2) through A3R66, A3R58, A3Q20, and A3R50 to the non-inverting input of A3U1 pin 3. This path allows A3C9 to charge up and hold the

YPLS (A3TP3) output of A3 value is valid for only Auto- signal opens the feedback pa A3U1.

The DC Input Enable (LRI applying the dc input volta inverting input of A3U1 pin A3VR2 produce a negative A3U5B, A3R40, and A3R43 gain of −1. Thus, producing at the output of A3U5B pin (LRP) causes FET A3Q16 negative input to A3U1 fr (Linearity) control is adjuste Section V, Adjustments). C approximately −7 times the Enable is terminated. A3C12 3.5 mV/clock pulse. The ou reduce to approximately 0 V the inverting input of A3U threshold was below the dc in input level.

The Enable Negative Ramp (to conduct, applying a posi source. The Enable Log F Reference (LLGR) cause FE A3Q19 completes a path to pin 3 of A3U2. This is the L of A3U1 discharges to the Comparator remains constan reaches the threshold level, tl to the opposite polarity.

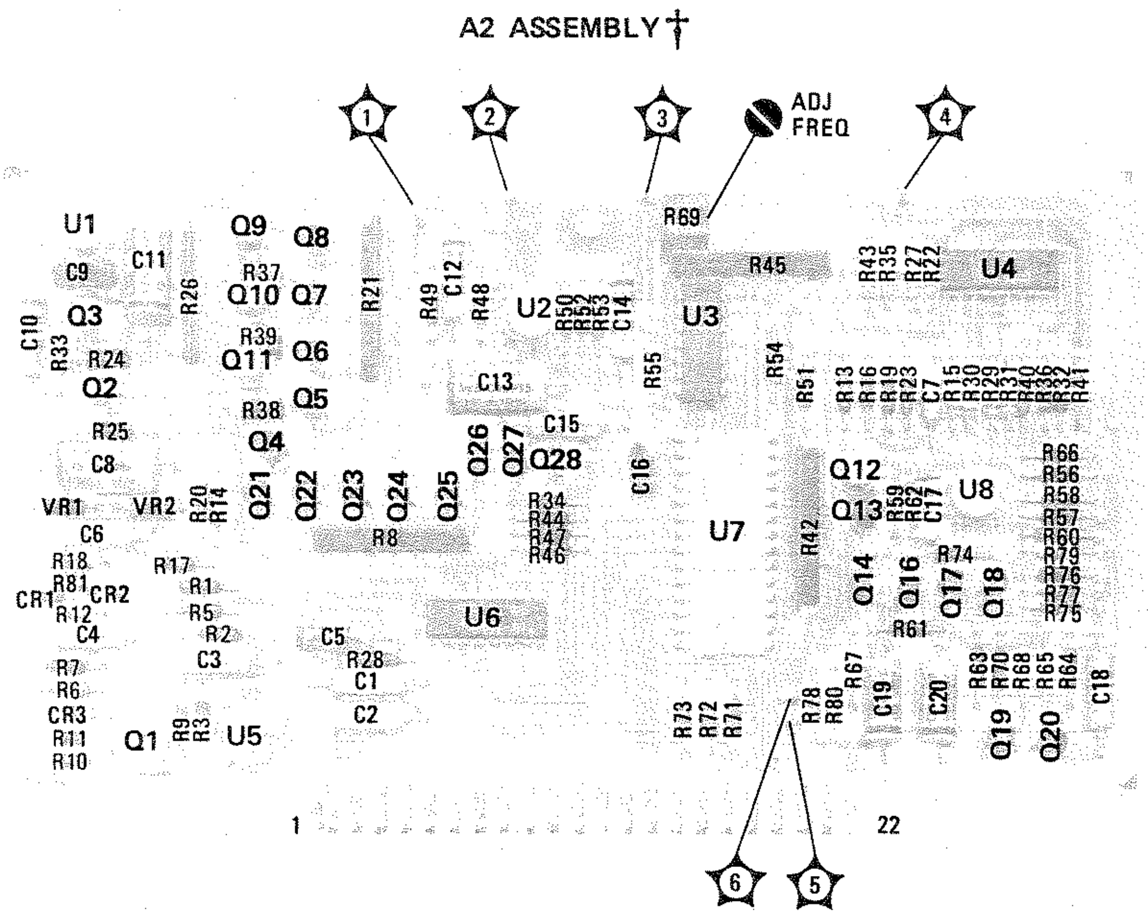
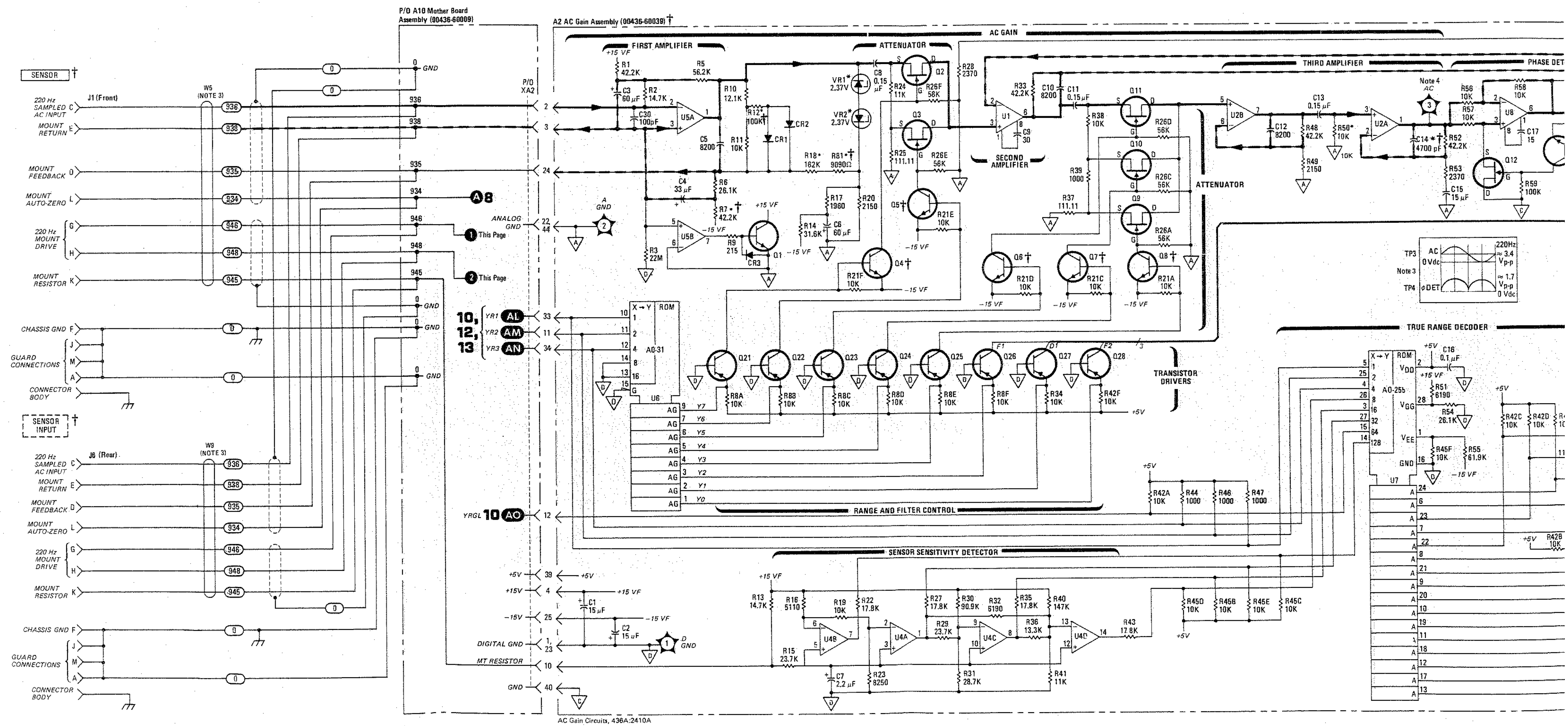
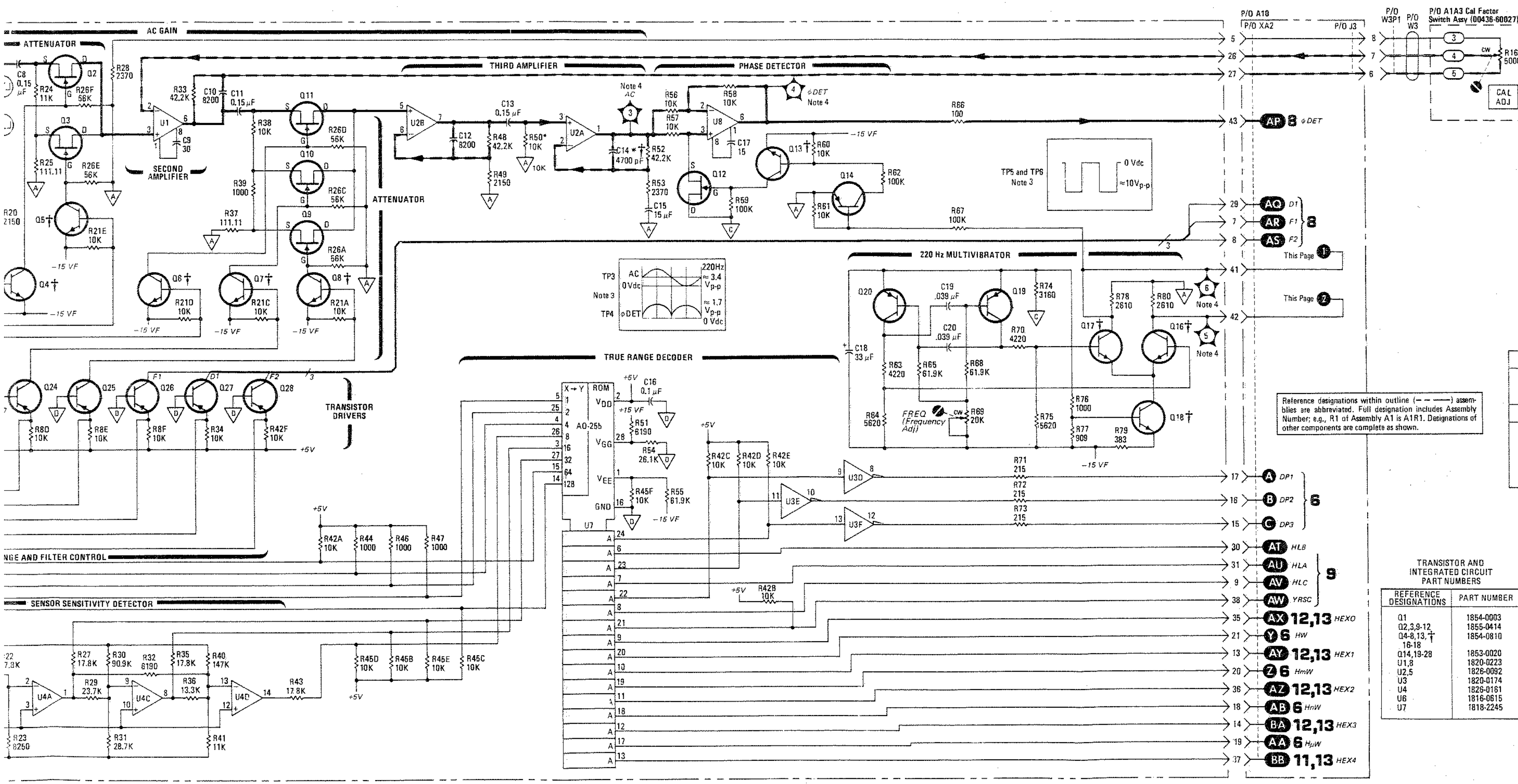


Figure 8-29. A2 AC Gain Assembly Component, Test Point, and Adjustment Locations



P/O A10 Mother Board Assembly (00436-60009)
A2 AC Gain Assembly (00436-60039) †
AC GAIN
FIRST AMPLIFIER
ATTENUATOR
SECOND AMPLIFIER
THIRD AMPLIFIER
PHASE DET
TRUE RANGE DECODER
TRANSISTOR DRIVERS
RANGE AND FILTER CONTROL
SENSOR SENSITIVITY DETECTOR
SENSOR †
220 Hz SAMPLED AC INPUT
MOUNT RETURN
MOUNT FEEDBACK
MOUNT AUTO-ZERO
220 Hz MOUNT DRIVE
MOUNT RESISTOR
CHASSIS GND
GUARD CONNECTIONS
CONNECTOR BODY
SENSOR INPUT †
J1 (Front)
J6 (Rear)
W5 (NOTE 3)
W9 (NOTE 3)
ANALOG GND
DIGITAL GND
MT RESISTOR
YRGL
This Page
TP3
TP4
Note 3
Note 4
220Hz
≈ 3.4 Vp-p
≈ 1.7 Vp-p
0 Vdc
AC Gain Circuits, 436A-2410A



NOTES

1. Unless otherwise indicated:
   Resistance in ohms;
   Capacitance in picofarads;
2. Asterisk (*) indicates selected component, average values shown.
3. For voltages and waveforms shown, controls are set as follows:
   RANGE 1mW
   CAL FACTOR % 100
   POWER REF . . . . ON

   Connect POWER SENSOR to POWER REF OUTPUT.

† Backdating information is found in Section VII.

REFERENCE DESIGNATIONS

NO PREFIX	A2 ASSY
J1,6 W3,5,9 W3P1	C1-20 CR1-3 Q1-14,16-28 R1-3,5-81 TP1-6 U1-8 VR1,2
A1A3 ASSY	A10 ASSY
R16	J3 XA2

† C21–35 Deleted

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBER
Q1	1854-0003
Q2,3,9-12	1855-0414
Q4-8,13,† 16-18	1854-0810
Q14,19-28	1853-0020
U1,8	1820-0223
U2,5	1826-0092
U3	1820-0174
U4	1826-0161
U6	1816-0615
U7	1818-2245

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBER
U1,8	+15 VF – 7 –15 VF – 4
U2,5	+15 VF – 8 –15 VF – 4
U3	+5V – 14 (D) – 7
U4	+15 VF – 4 (D) – 11
U6	+15 VF – 16 (D) – 8
U7	AS SHOWN

7
A1A3,A2,A10

Figure 8-30. AC Gain Assembly Schematic Diagram

SERVICE SHEET 9

CIRCUIT DESCRIPTIONS

The circuits described in Service Sheet 9 are covered on Service Sheets 1 and 3 and Troubleshooting in paragraphs 8-55 through 8-62.

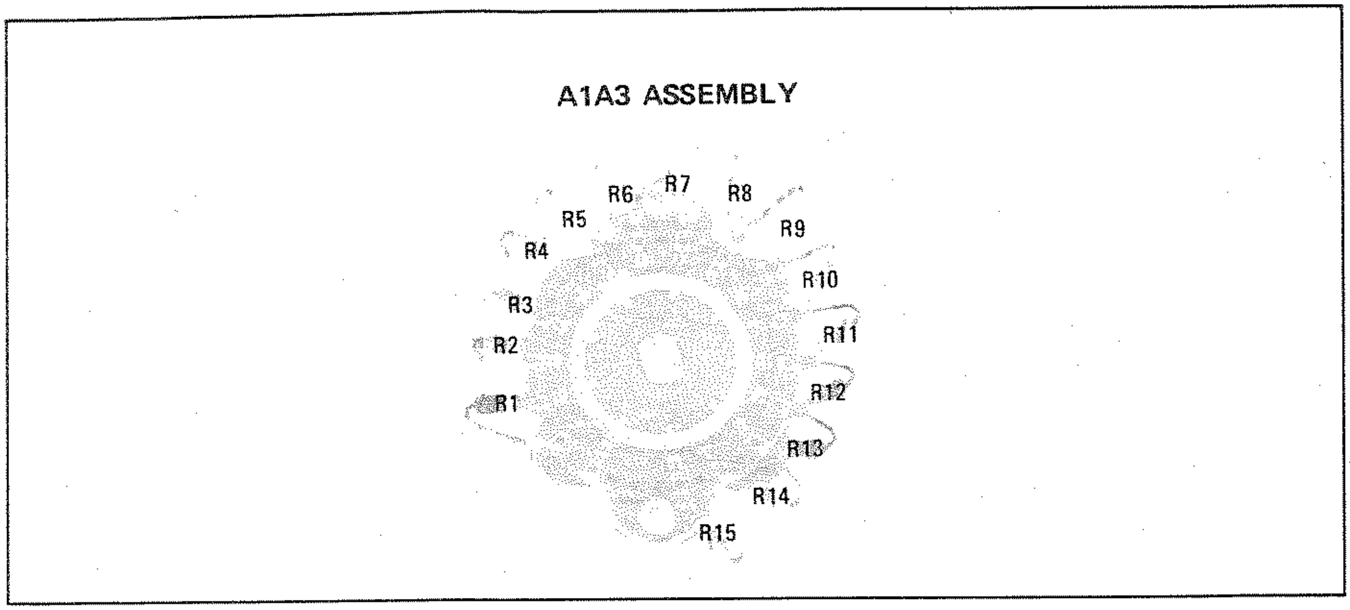


Figure 8-31. A1A3 CAL FACTOR % Switch Assembly Component Locations

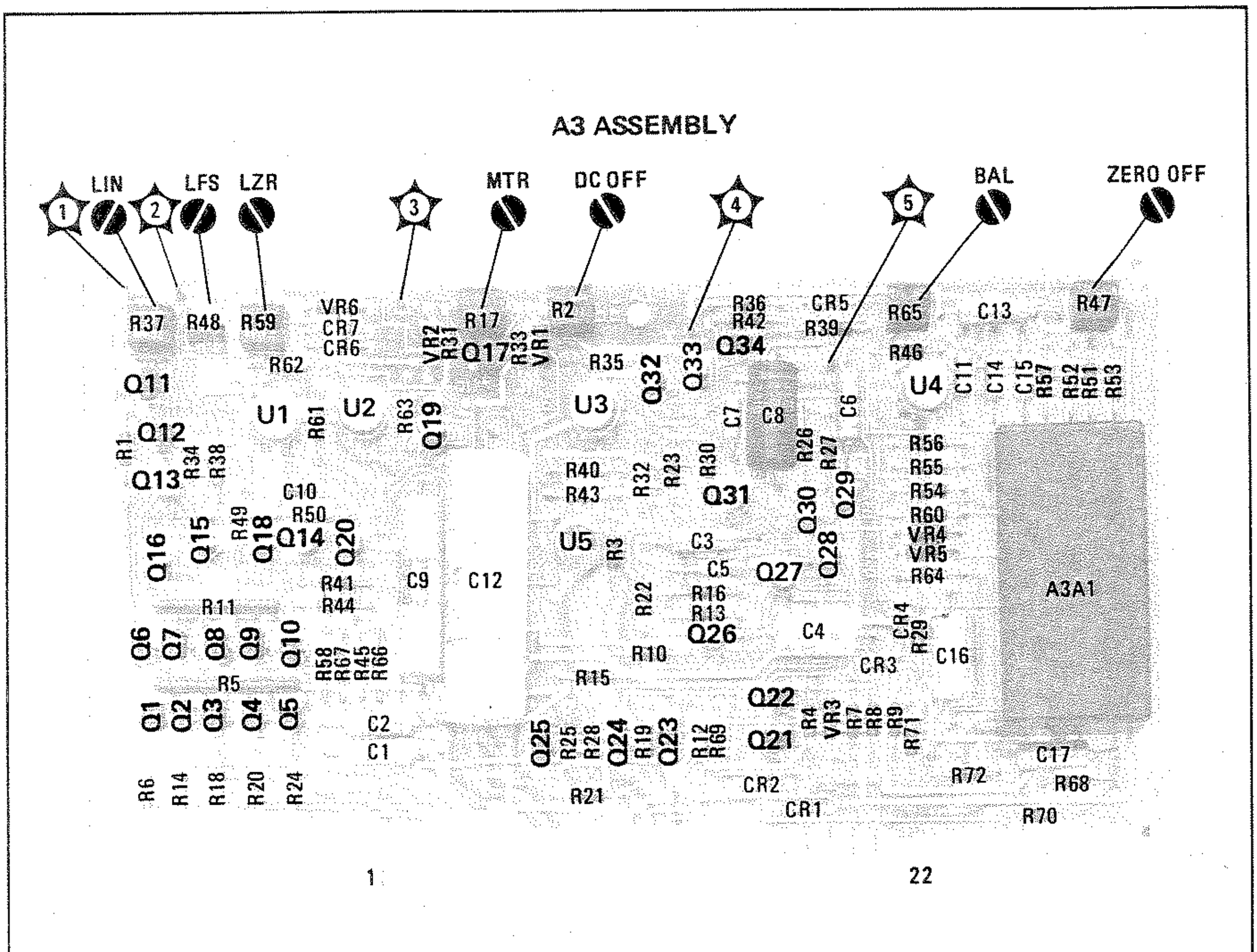
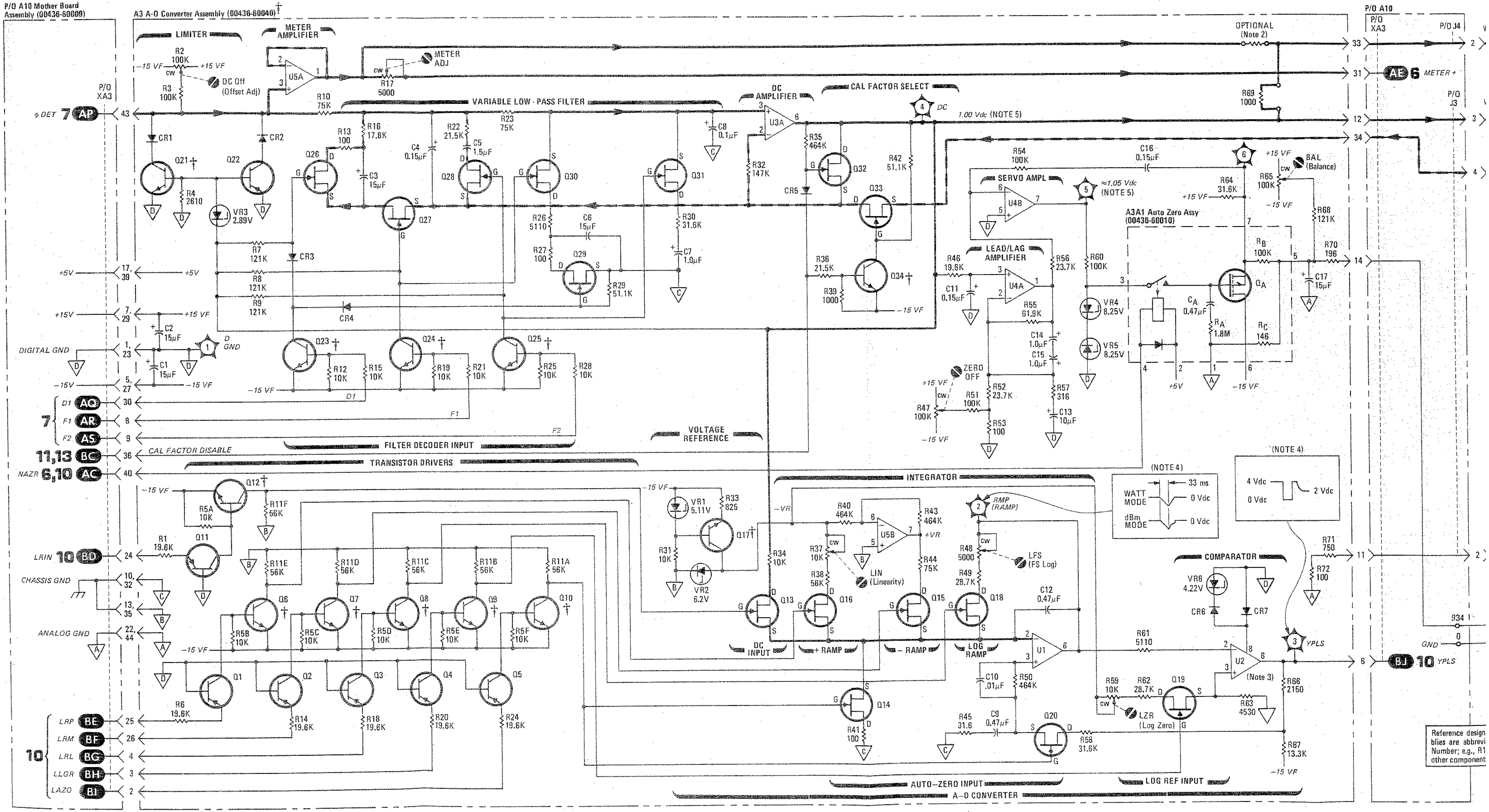
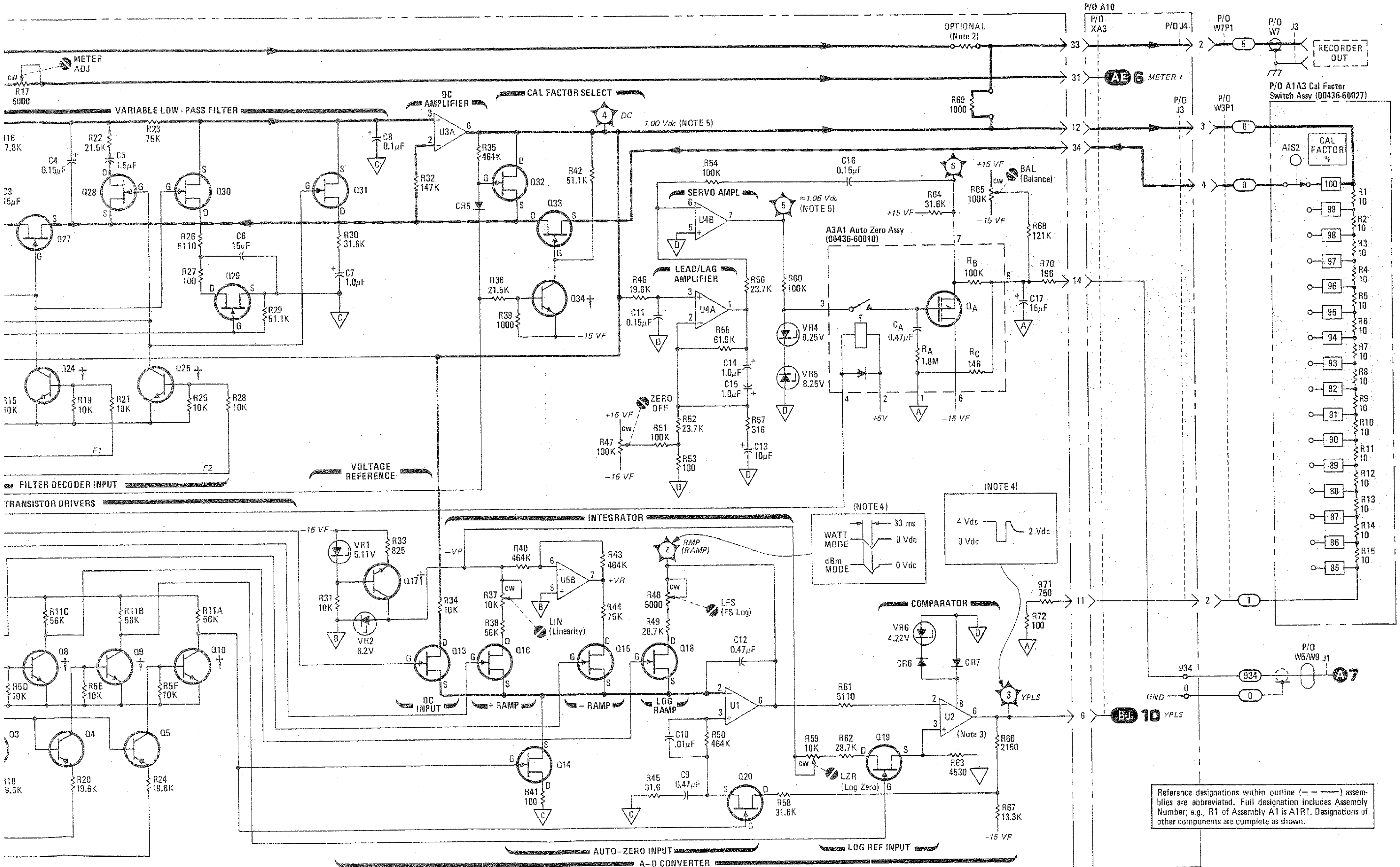


Figure 8-32. A3 A-D Converter Assembly Components, Test Point, and Adjustment Locations



A-D Converter Circuits 436A: 2410A



NOTES

1. Unless otherwise indicated: Resistance in ohms; Capacitance in picofarads.
2. Standard connection shown for R69, optional connection is between XA3-33 and A3U5A-1.
3. Pins 1 and 5 cut off.
4. For voltages and waveforms shown, controls are set as follows:
   - RANGE .... 1 mW
   - CAL FACTOR % ... 100
   - POWER REF ...... ON
   - Connect POWER SENSOR to POWER REF OUTPUT.

† Backdating information is found in Section VII.

REFERENCE DESIGNATIONS

NO PREFIX	A3 ASSY
J1,3 W5/W9,W7 W3P1 W7P1	C1-17 CR1-7 Q1-34 R1-72 TP1-6 U1-5 VR1-6
A1 ASSY	
S2	A10 ASSY
A1A3 ASSY	J3,4 XA3
R1-15	

† C18-22 Deleted

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBER
Q1-5,11,22	1853-0020
† Q6-10,12,17	1854-0810
21,23-25,34	
Q13-16,18,19, 20,26-33	1855-0414
U1,3	1826-0102
U2	1820-0223
U4,5	1826-0092

INTEGRATED CIRCUITS VOLTAGE CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBER
U1-3	−15 VF − 4 +15 VF − 7
U4,5	−15 VF − 4 +15 VF − 8

Reference designations within outline (— — ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

8

A1A3, A3, A10

Figure 8-33. A-D Converter Assembly Schematic Diagram

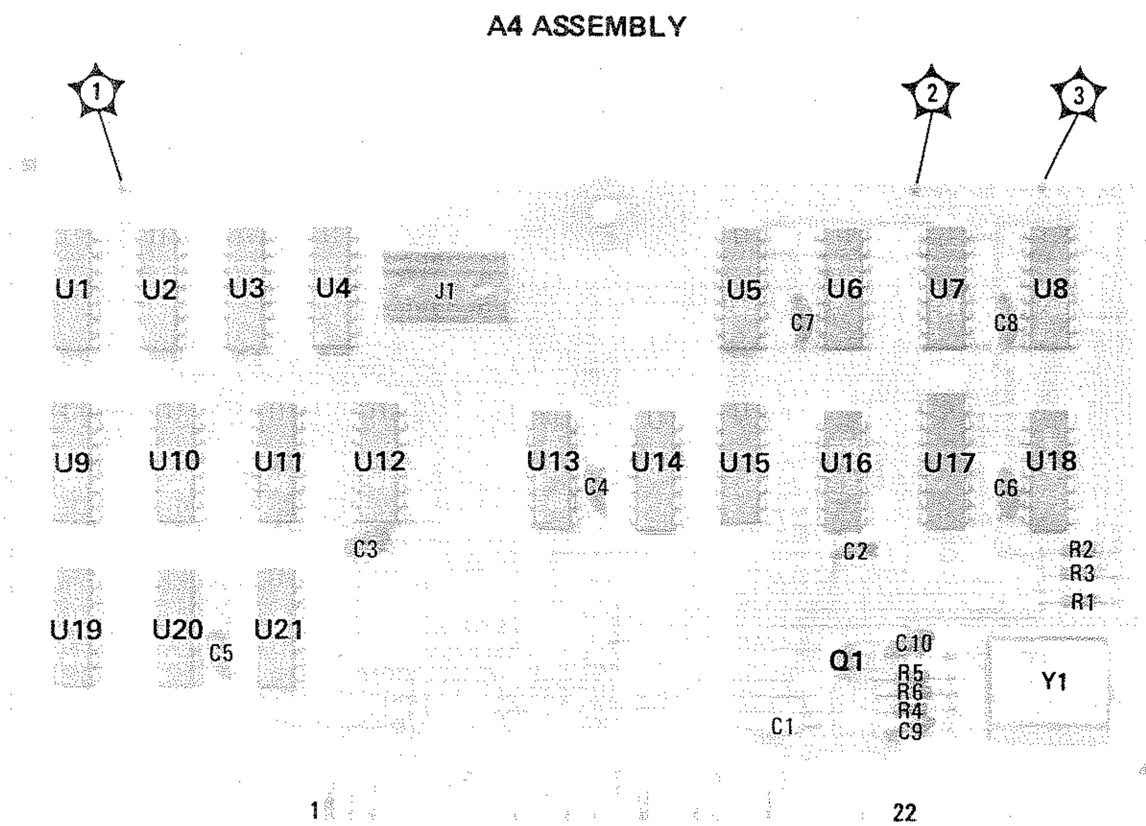
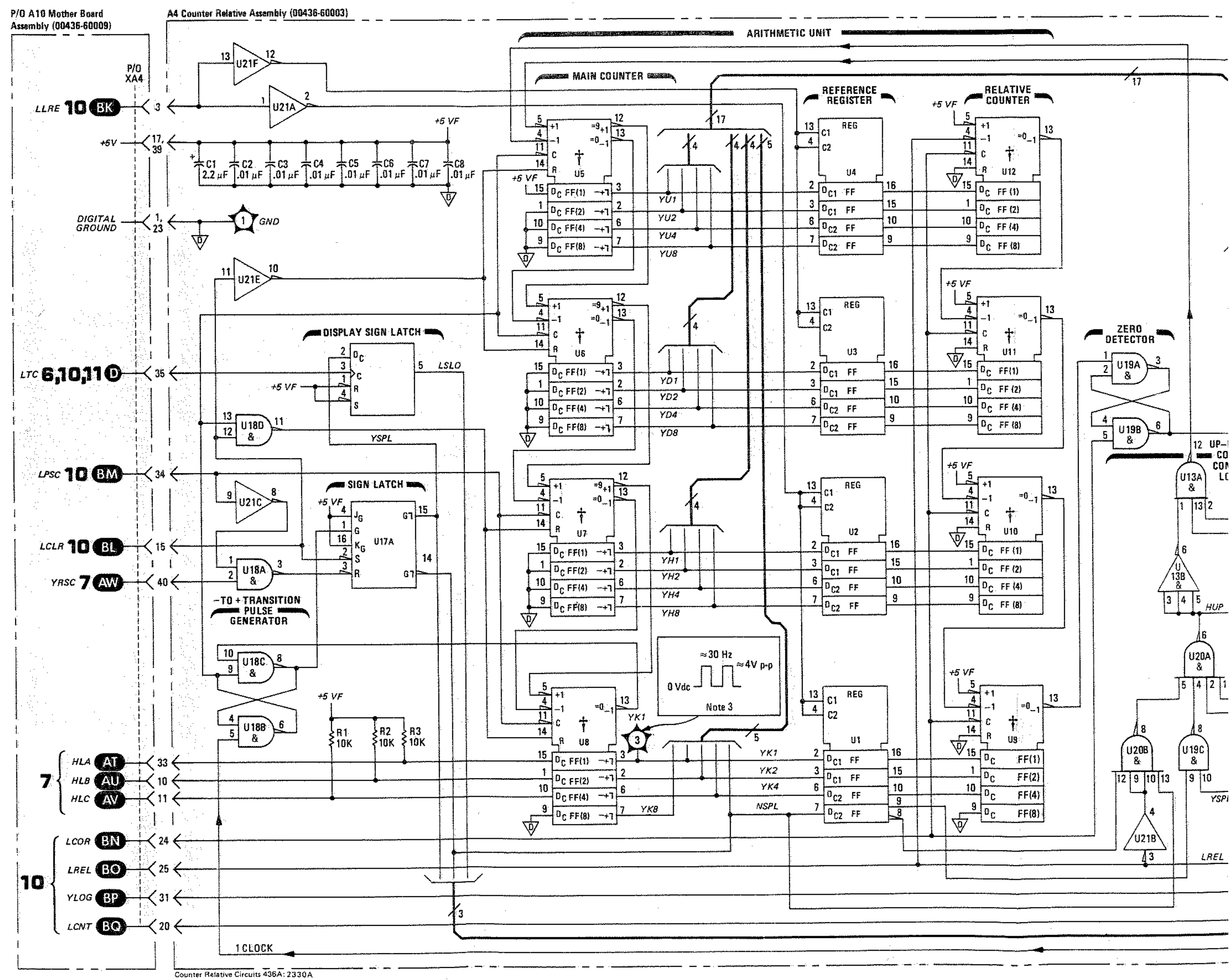
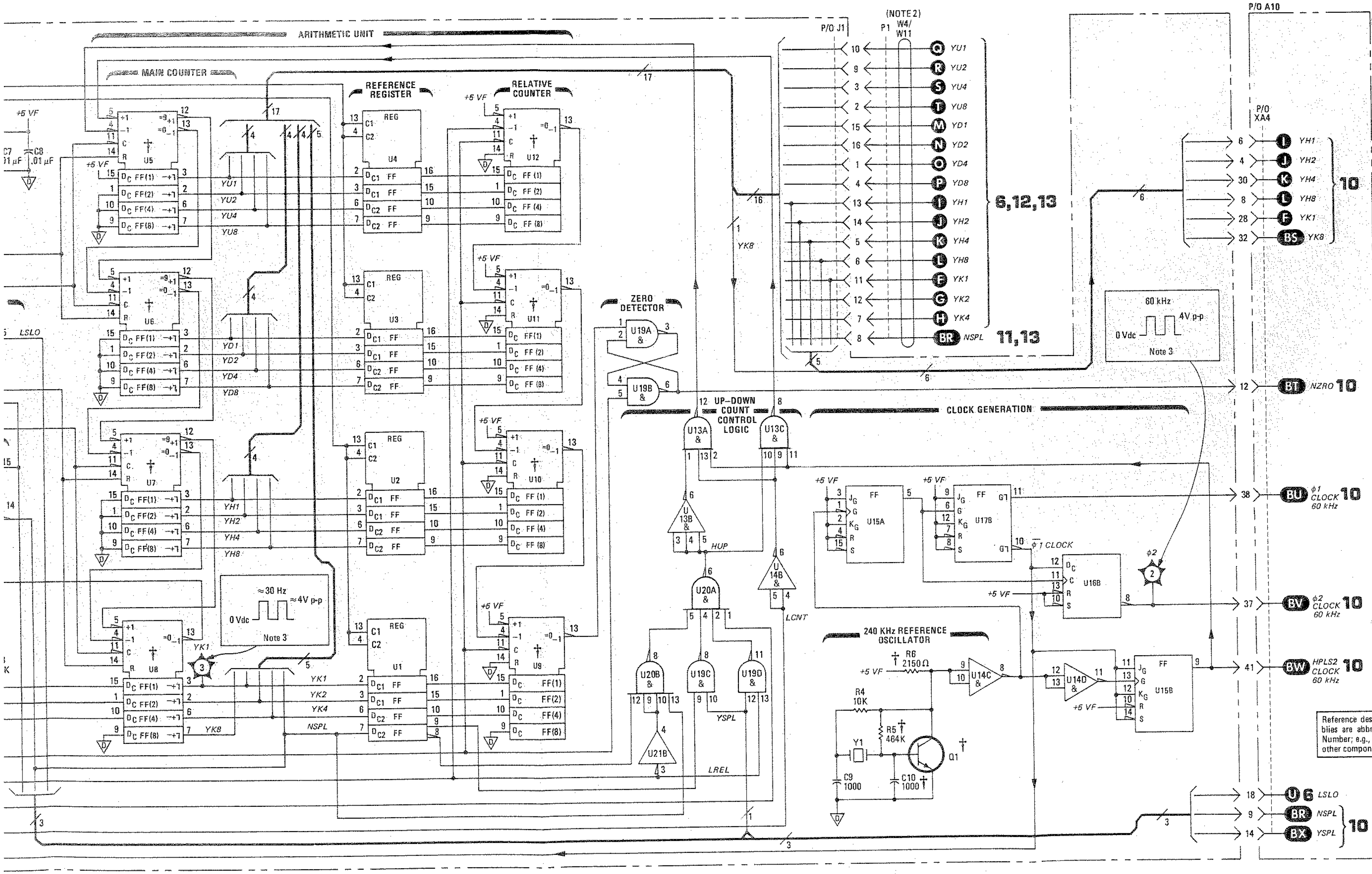


Figure 8-34. A4 Counter Relative Assembly Component and Test Point Locations


P/O A10 Mother Board Assembly (00436-60009)
A4 Counter Relative Assembly (00436-60003)
ARITHMETIC UNIT
MAIN COUNTER
REFERENCE REGISTER
RELATIVE COUNTER
ZERO DETECTOR
DISPLAY SIGN LATCH
SIGN LATCH
–TO + TRANSITION PULSE GENERATOR
P/O XA4
LLRE
+5V
DIGITAL GROUND
GND
LTC
LPSC
LCLR
YRSC
HLA
HLB
HLC
LCOR
LREL
YLOG
LCNT
1 CLOCK
LSLO
YSPL
HUP
NSPL
≈30 Hz
≈4V p-p
0 Vdc
Note 3
Counter Relative Circuits 436A: 2330A



Reference designations within outline (— — —) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. Unless otherwise indicated:
   Resistance in ohms;
   Capacitances in picofarads.
2. W4 (omitted on Options 22, 24)
   W11 (with Options 22, 24).
3. For voltages and waveforms shown, controls are set as follows:
   RANGE . . . . . . 1 mW
   CAL FACTOR % . . . 100%
   POWER REF . . . . ON

   Connect POWER SENSOR to POWER REF OUTPUT.

REFERENCE DESIGNATIONS

A4 ASSY	A10 ASSY
C1 – 10 J1 Q1 R1 – 6 TP1 – 3 U1 – 21 Y1	XA4
	NO PREFIX
	P1 W4/W11

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBER
† Q1	1854-0810
† U1–4	1820-1411
† U5–12	1820-1277
U13	1820-1202
U14, 18, 19	1820-1197
U15	1820-1212
U16	1820-0077
U17	1820-0076
U20	1820-1204
U21	1820-1199

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBER
U1–4	+5 VF –5 D –12
U5–12, 15	+5 VF –16 D –8
U13, 14, 16, 18–21	+5 VF –14 D –7
U17	+5 VF –5 D –13

† See backdating information in section VII.

9
A4, A10

Figure 8-35. Counter Relative Assembly Schematic Diagram

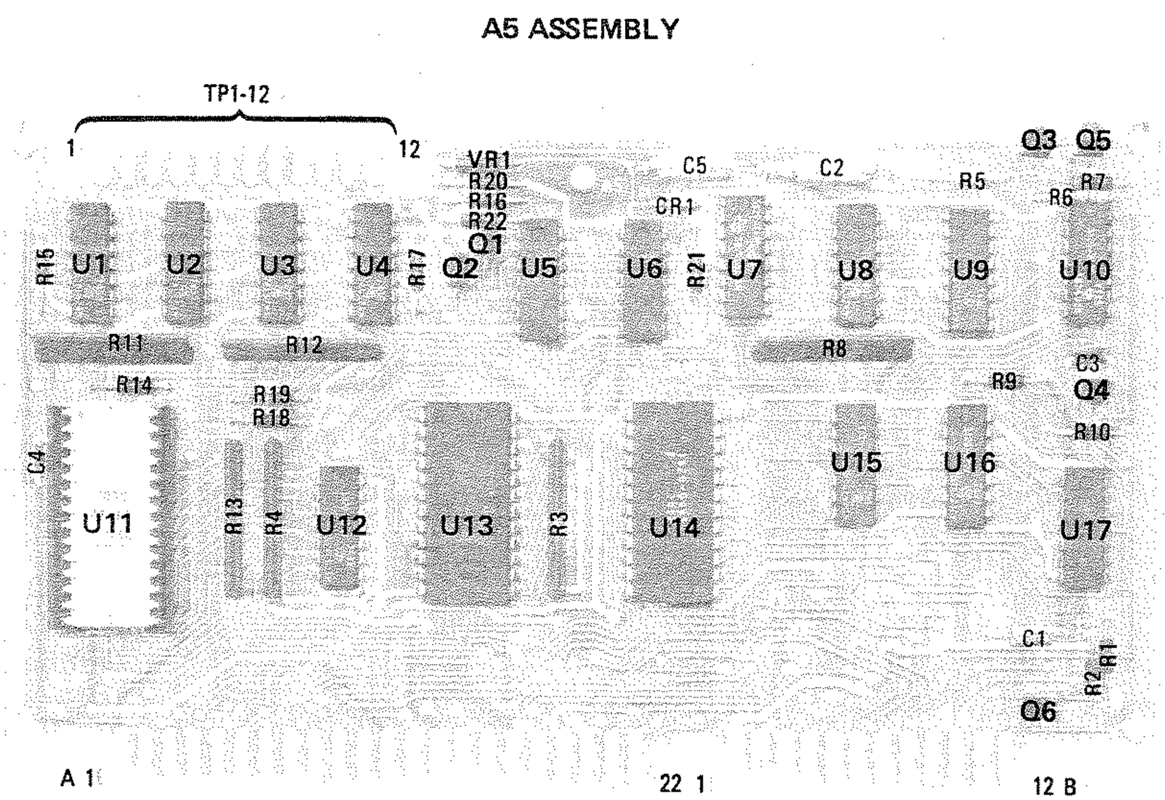


Figure 8-36. A5 Controller Assembly Component and Test Point Locations

SERVICE SHEET 11

CIRCUIT DESCRIPTIONS

The circuits described in Service Sheet 11 are covered in paragraphs 8-114 through 8-161, HP-IB Instrument Checkout in paragraphs 8-63 through 8-66, Troubleshooting in Table 8-4, and HP-IB Verification Programs in Figures 8-16 and 8-17.

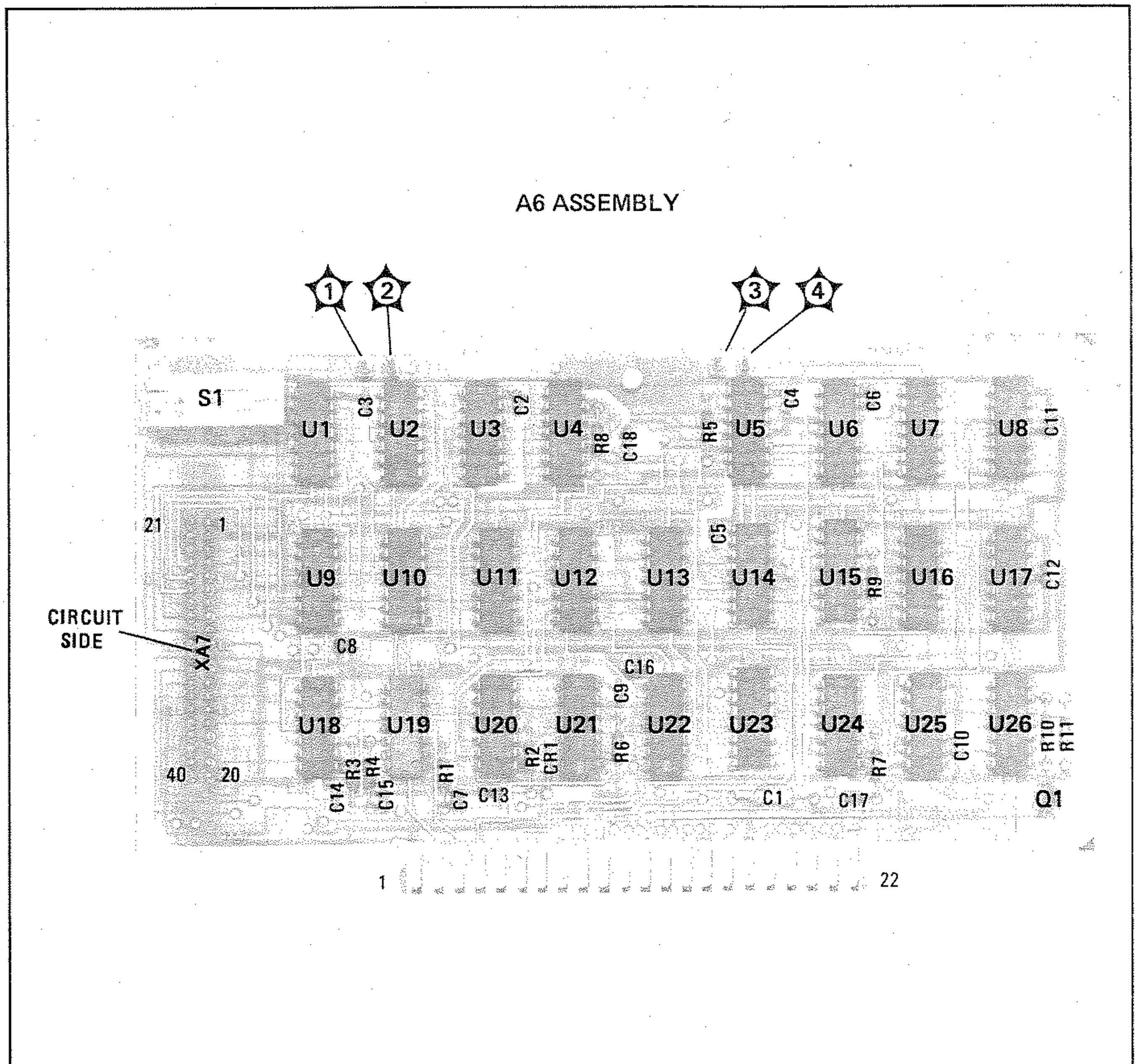
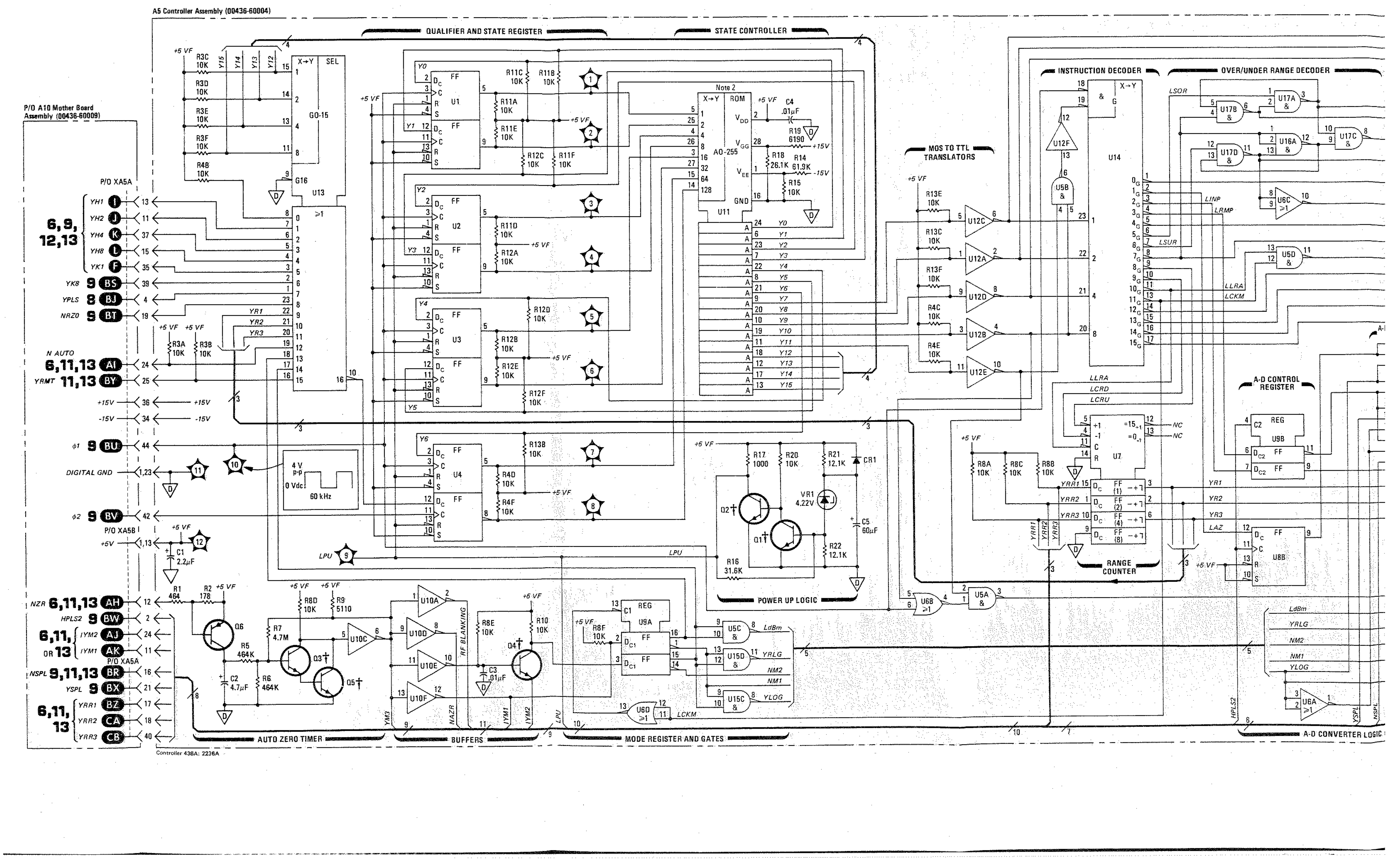
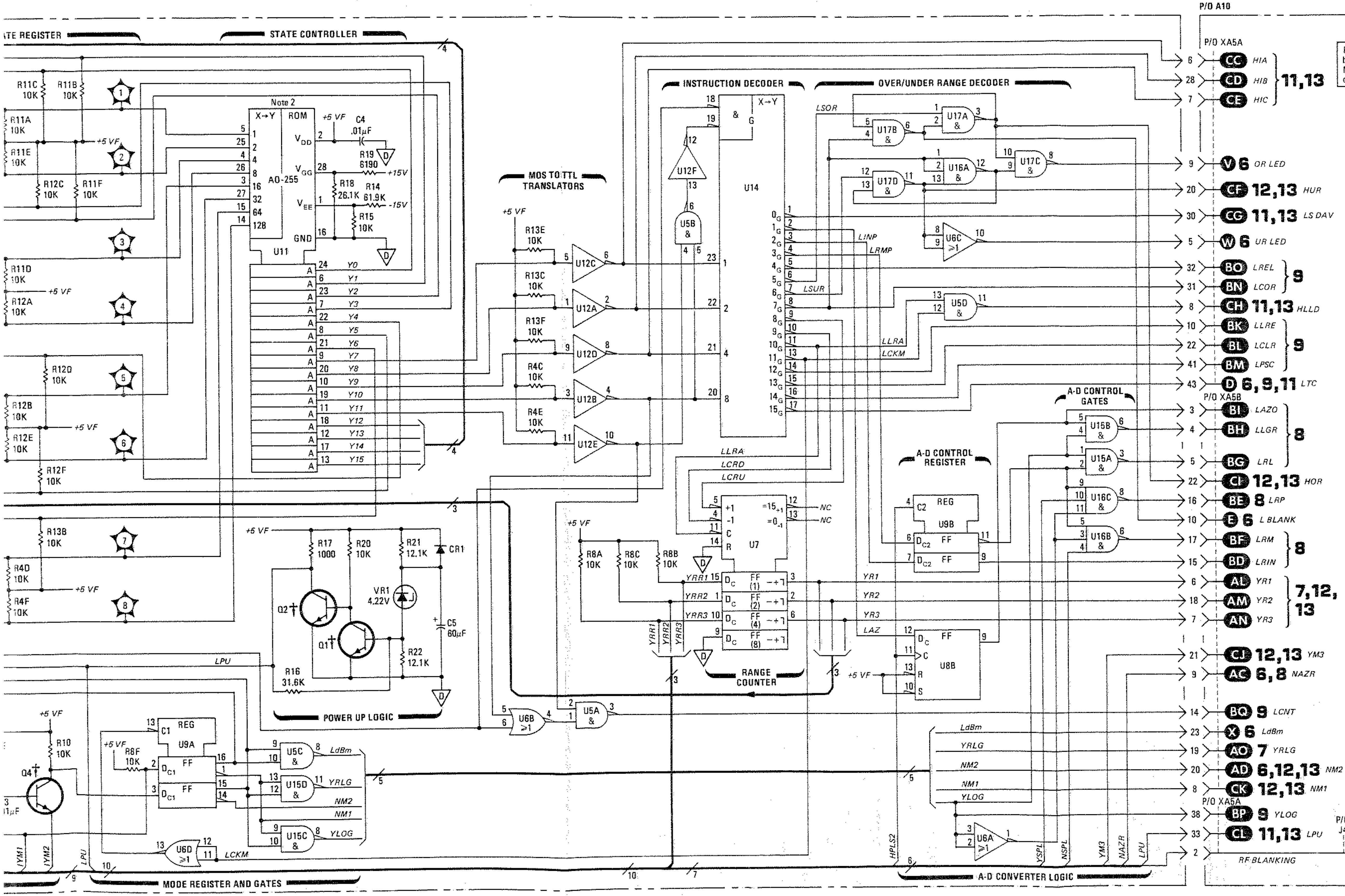


Figure 8-38. A6 HP-IB (Option 022) Control Assembly Component and Test Point Locations



A5 Controller Assembly (00436-60004)
P/O A10 Mother Board Assembly (00436-60009)
QUALIFIER AND STATE REGISTER
STATE CONTROLLER
INSTRUCTION DECODER
OVER/UNDER RANGE DECODER
MOS TO TTL TRANSLATORS
A-D CONTROL REGISTER
RANGE COUNTER
POWER UP LOGIC
AUTO ZERO TIMER
BUFFERS
MODE REGISTER AND GATES
A-D CONVERTER LOGIC
P/O XA5A
P/O XA5B
YH1, YH2, YH4, YH8, YK1 6,9,12,13
YK8 9 BS
YPLS 8 BJ
NRZ0 9 BT
N AUTO 6,11,13 AI
YRMT 11,13 BY
+15V
-15V
φ1 9 BU
DIGITAL GND
φ2 9 BV
+5V
NZR 6,11,13 AH
HPLS2 9 BW
IYM2 AJ
IYM1 AK
6,11, OR 13
NSPL 9,11,13 BR
YSPL 9 BX
YRR1 BZ
YRR2 CA
YRR3 CB
6,11,13
Note 2
AO-255
4 V P-P
0 Vdc
60 kHz
Controller 436A: 2236A



Reference designations within outline (— — —) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. Unless otherwise indicated:
   Resistance in ohms;
   Capacitance in picofarads.
2. Not supplied as part of A5 Assembly.

† Backdating information is found in Section VII.

REFERENCE DESIGNATIONS

NO PREFIX	A5 ASSY
J4 W7 W7P1	C1-5 CR1 Q1-6 R1-22 TP1-12 U1-17 VR1
A10 ASSY	
J4 XA5A,B	

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBER

REFERENCE DESIGNATIONS	PART NUMBER
† Q1-5	1854-0810
Q6	1853-0020
U1-4,8	1820-1112
U5, 17	1820-0054
U6	1820-0328
U7	1820-1194
U9	1820-1411
U10	1820-0175
U11	1818-2244
U12	1820-1199
U13	1820-0640
U14	1820-0495
U15	1820-1197
U16	1820-1202

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBER
U1-6,8,10, 12,15-17	+5 VF – 14 ⏚ – 7
U7	+5 VF – 16 ⏚ – 8
U9	+5 VF – 5 ⏚ – 12
U11 U13, 14	AS SHOWN + – 24 ⏚ – 12

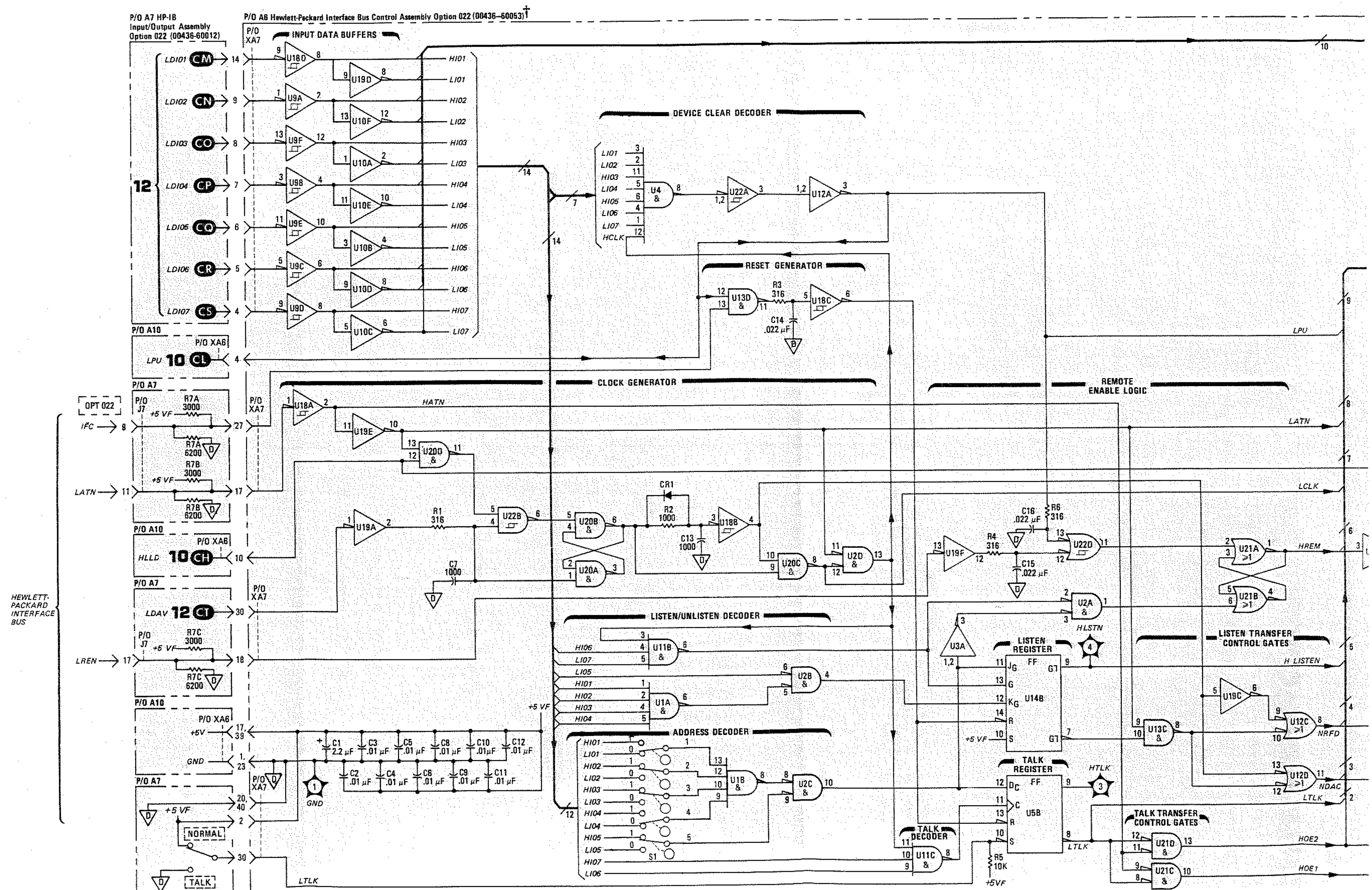
10
A5, A10

Figure 8-37. Controller Assembly Schematic Diagram

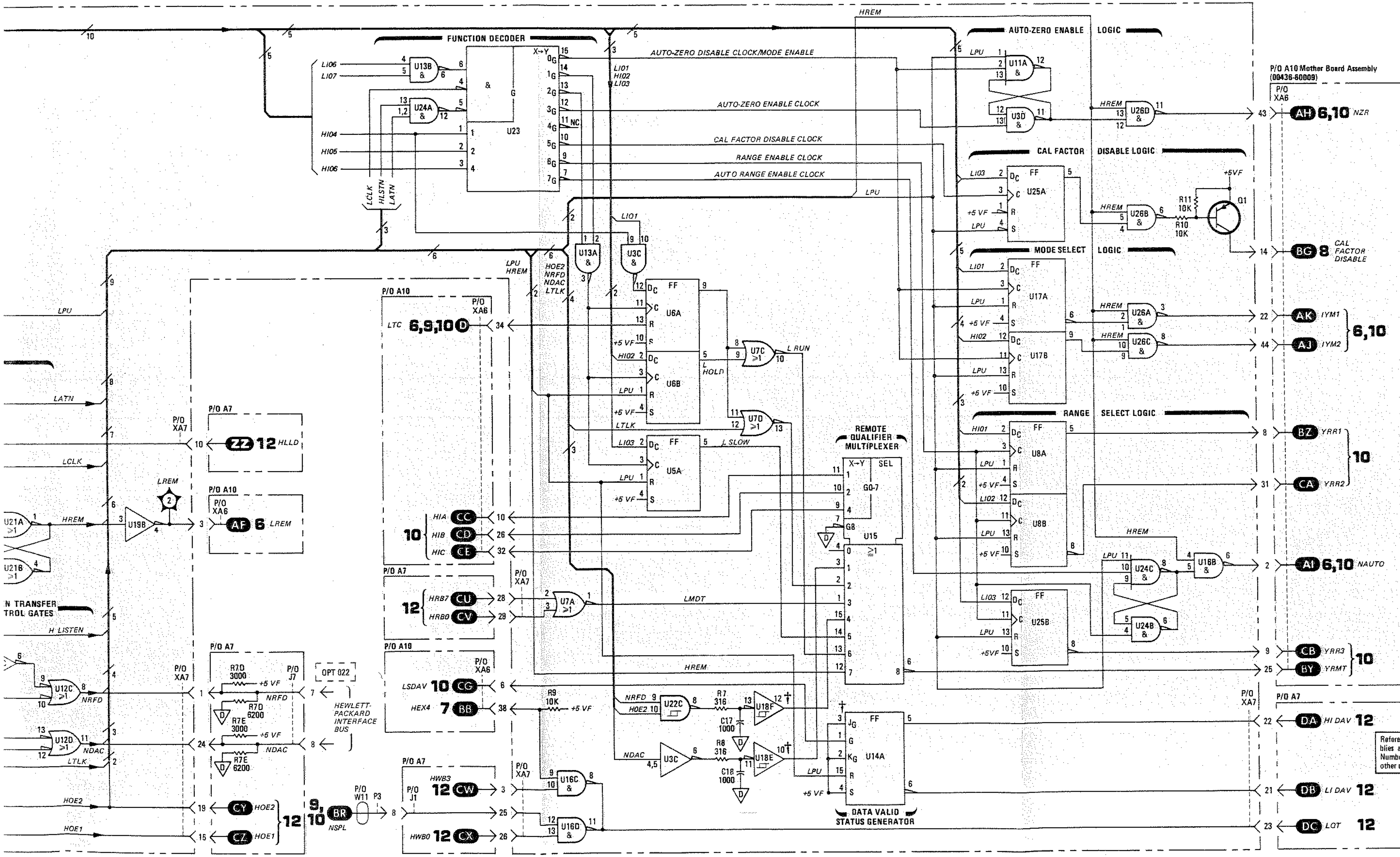
SERVICE SHEET 12

CIRCUIT DESCRIPTIONS

The circuits described in Service Sheet 12 are covered in paragraphs 8-111 through 8-154, HP-IB Instrument Checkout in paragraphs 8-63 through 8-66, Troubleshooting in Table 8-4, and HP-IB Verification Programs in Figures 8-16 and 8-17.



Hewlett-Packard Interface Bus Control Circuits Option 022, 436A:2330A



Reference designations within outline (— — —) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. Unless otherwise indicated:
   Resistance in ohms;
   Capacitance in picofarads;

† Backdating information is found in Section VII.

REFERENCE DESIGNATIONS

A6 ASSY	A7 ASSY
C1–18 CR1 Q1 R1–11 TP1–4 U1–26 XA7	J1, 7 R7 S1 XA6
	A10 ASSY
	XA6
	NO PREFIX
	P3 W11

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

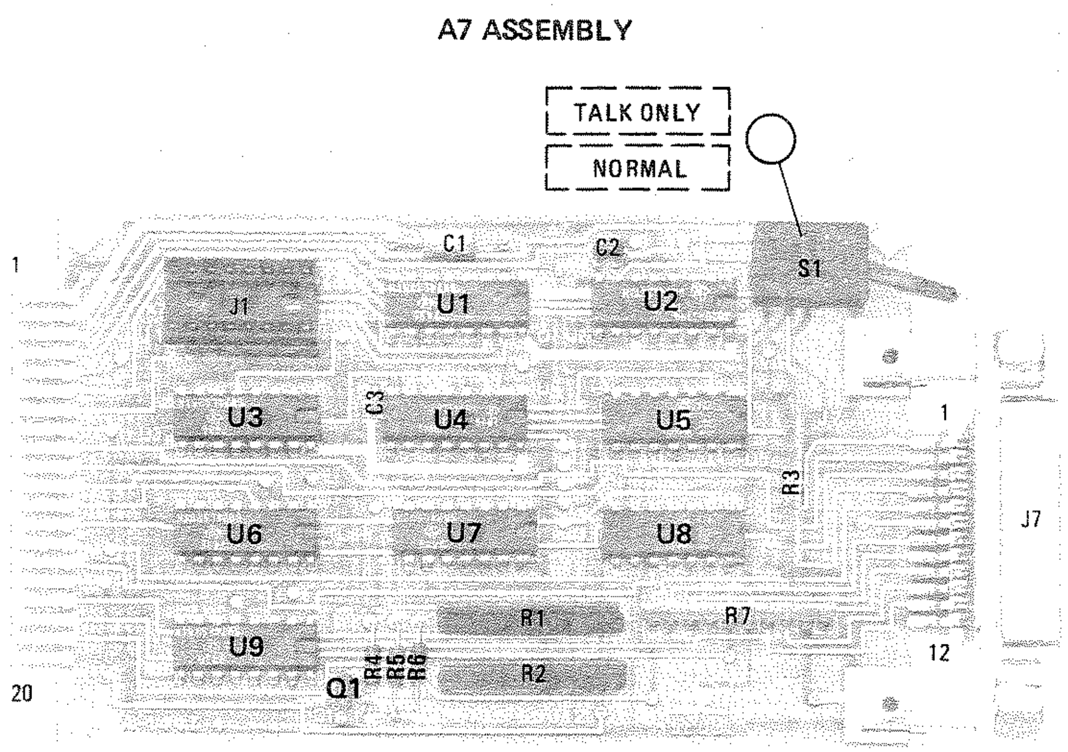
REFERENCE DESIGNATIONS	PART NUMBER
Q1	1853-0020
U1	1820-1204
U2, 7, 21	1820-1144
U3, 13, 20	1820-1197
U4	1820-1207
U5, 6, 8, 17, 25	1820-1112
U9, 18	1820-1053
U10, 19	1820-1199
U11, 24	1820-1202
U12	1820-0621
U14	1820-0629
U15	1820-1298
U16, 26	1820-1198
U22	1820-1056
U23	1820-1216

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBER
U1-13, 15-22, 24-26	+5 VF – 14 D – 7
U14, 23	+5 VF – 16 D – 8

11
A6,A7,A10

Figure 8-39. HP-IB (Option 022) Control Assembly Schematic Diagram



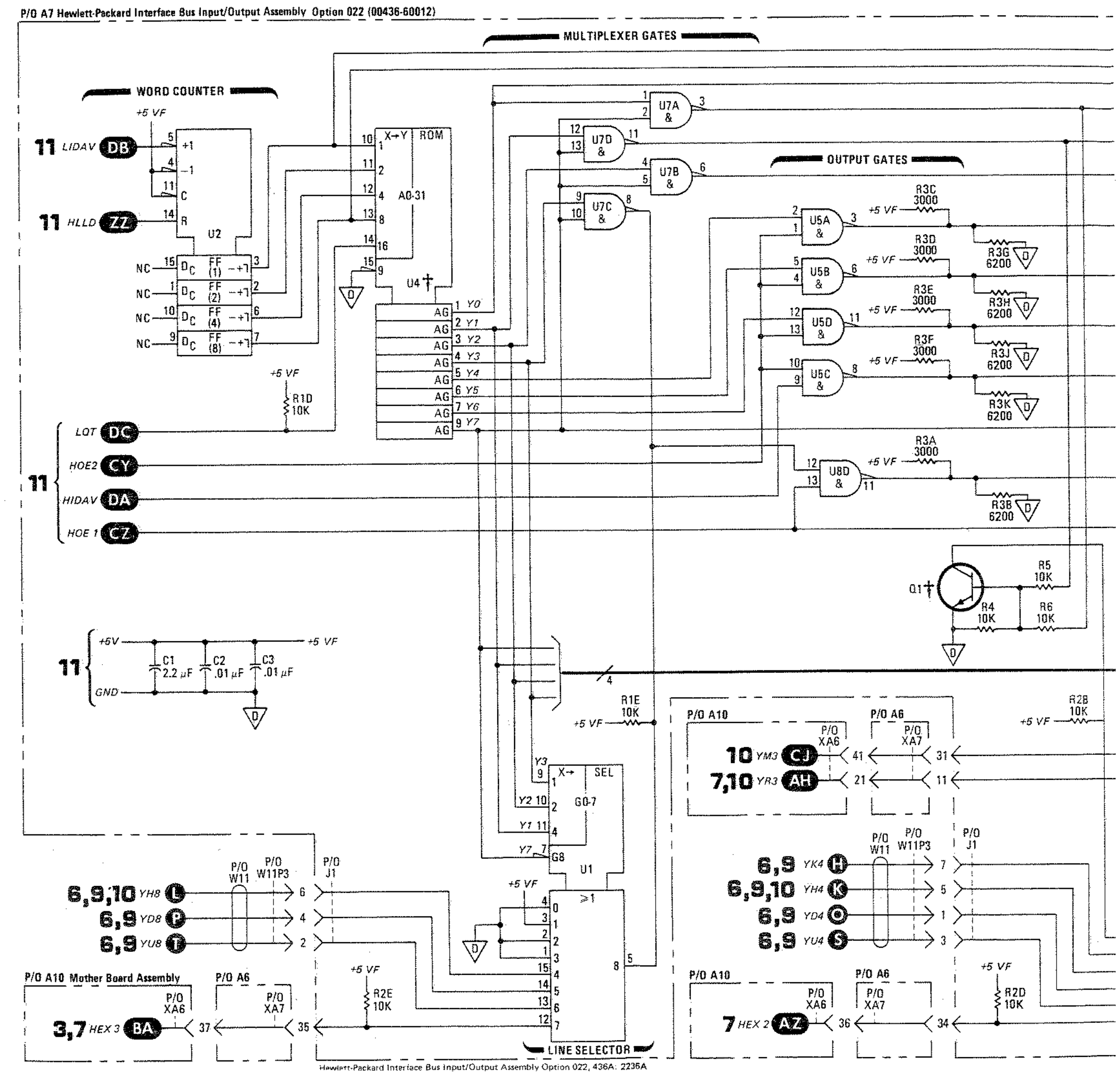
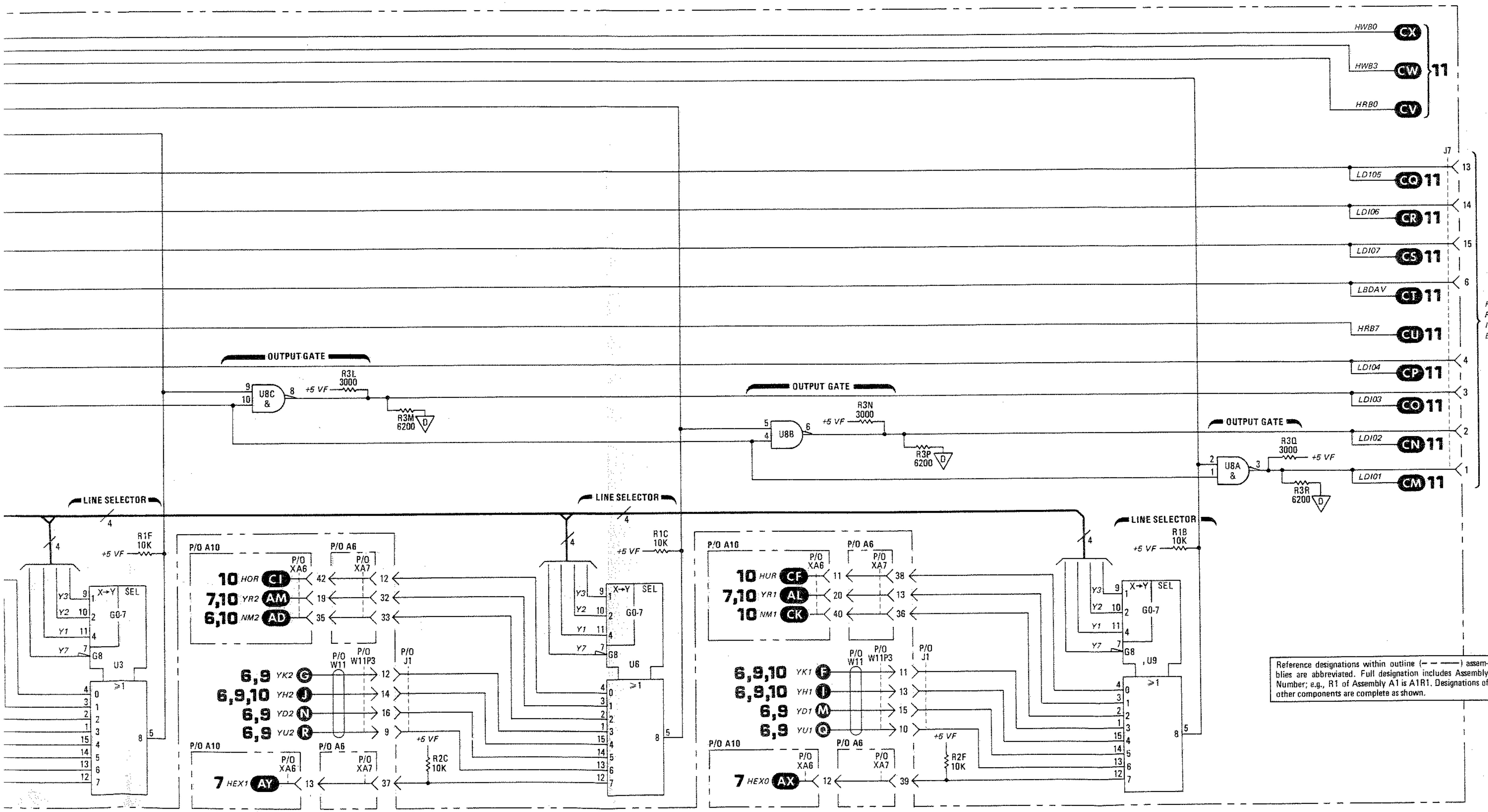


Figure 8-40. A7 HP-IB (Option 022) Input/Output Assembly Component and Test Point Locations



Reference designations within outline (— — —) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTE

1. Unless otherwise indicated:
   Resistance in ohms;
   Capacitance in picofarads.

† Backdating information found in Section VII.

REFERENCE DESIGNATIONS

NO PREFIX	A7 ASSY
W11 W11P3	C1–3 J1,7 Q1 R1–6 U1–9
A6 ASSY	A10 ASSY
XA7	XA6

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBE
†Q1	1854-0810
U1,3,6,9	1820-1298
U2	1820-1194
†U4	00436-8000
U5,8	1820-0621
U7	1820-1198

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBE
U1–3,4,5,6,9	+5 VF – 16 D – 8
U5,7,8	+5 VF – 14 D – 7

12

A6,A7,A1

Figure 8-41. HP-IB (Option 022) Input/Output Assembly Schematic Diagra

SERVICE SHEET 13 HAS BEEN DELETED

SERVICE SHEET 14

General

The A8A1 assembly provides a 50 ± 5 MHz output at 1 mW ± 0.7%. The oscillator's output is held constant by an ALC loop made up of a peak detector CR2 and comparator U2. The comparator reference input is from a very stable +5V power supply composed of U1, VR2 and their associated components. The LEVEL control R4 sets the comparator reference which controls the oscillator feedback level and thereby controls the A8A1 assembly POWER REF OUTPUT level. The oscillator's frequency is set by adjusting the FREQ ADJ control L1.

50 MHz Oscillator

The oscillator circuit is made up of common-emitter amplifier Q1 and its associated components. Resistors R12, R13, R14, and R15 bias Q1 for an emitter current of approximately 5 mA. The π-network tuned circuit, C11, C13, C14, and L1 determines the operating frequency. The amplifier gain is set by the operating circuit impedance across the tuned circuit and the emitter resistor R14 (which is ac coupled to ground by C12). The positive feedback required to sustain oscillation is satisfied in this circuit. Phase shift of 180° is a characteristic of both common-emitter amplifiers and π-network tuned circuits. This feedback is coupled through C9 and C10, back to the base of Q1. The FREQ ADJ control L1 sets the oscillator's frequency.

ALC Loop

At the positive peak of each cycle, current momentarily flows from the feedback loop through peak detector diode CR2 to C7. The resultant stored charge is coupled, as a dc input voltage, to pin 3 of U2. The peak detector's output is compared to the very stable reference input by comparator U2. Any difference between the comparator's input voltages produces an error voltage at the dc output. The comparator's output is coupled to a reactance voltage divider, capacitor C9 and varactor CR3. As the error output voltage goes more positive, the capacitive reactance of CR3 decreases, which reduces the oscillator feedback. Conversely, a more negative output voltage will increase the feedback. For example, if the oscillator output were to suddenly increase, the peak detector's output would become more positive. The comparator's output would become more positive, a lower CR3 reactance would decrease the feedback to Q1 which forces the oscillator's output level back to its original level. If the R4 LEVEL control were adjusted for a more positive reference voltage, the comparator's output would go more negative, the feedback would increase, allowing the oscillator's output to increase. Therefore, the peak detector's output would increase until it equals the comparator's reference level input, thus establishing a higher leveled-output signal from the oscillator.

SERVICE SHEET 14 (cont'd)

Frequency shaping components R9, R10, R11, and C8 determine the upper limit of frequency response of the ALC loop which prevents spurious oscillations.

+5V Power Supply

A8A1VR2 provides a reference voltage of −6.2 Vdc to the power supply reference amplifier A8U1. The gain of the reference amplifier is set by R3, R4, and R5 and is approximately −0.8 with R3 centered. The very stable output is coupled through CR1 as the reference voltage input to comparator U2. Diode CR1 provides temperature compensation for CR2.

TROUBLESHOOTING

General

Before trying to troubleshoot the A8A1 Assembly, verify the presence of +15 Vdc and −15 Vdc on the circuit board.

If a defect in the A8A1 Assembly is isolated and repaired, the correct output level (1 mW ± 0.7%) must be set by a very accurate power measurement system. Hewlett-Packard employs a special system, accurate to ±0.5% and traceable to the National Bureau of Standards. When setting the power level, a transfer error of ±0.2% is introducted making the total error ±0.7%. If a system this accurate is available it may be used to set the proper output level. Otherwise, Hewlett-Packard recommends returning the Power Meter so it can be reset at the factory. Contact your nearest Hewlett-Packard office for more information.

50 MHz Oscillator

Malfunctions of the oscillator circuit will occur as a wrong output frequency or as an abnormal output level. The voltage at TP2 will indicate if the ALC loop is trying to compensate for an incorrect output level.

Modulation of the 50 MHz signal or spurious signals, which are part of the output, may be caused by defects in R9, R10, R11, or C8 in the ALC loop.

ALC Loop and Power Supply

Isolating problems in the ALC Loop and Power Supply circuits may be quickly isolated by measuring dc voltages at the inputs and outputs of the integrated circuits.

SERVICE SHEET 15

CIRCUIT DESCRIPTIONS

General

The Power Line Module (A11), the Power Transformer (T1), the Power Supply Rectifier and Regulator Assembly (A9), and the +5V Regulator provide the +5 Vdc, +15 Vdc, and −15 Vdc voltages for the operation of the Power Meter.

Power Line Module and Transformer

The Power Meter requires a power source of 100, 120, 220, or 240 Vac, +5% −10%, 48 to 440 Hz, single phase. The Power Meter consumes about 20 watts of power. The line (mains) voltage selection is accomplished through the proper selection of A11TB1. (See paragraph on Line Voltage Selection in Section II of this manual.) The Power Transformer (T1) provides the proper voltages to the Power Supply Rectifier and Regulator Assembly (A9) and the +5V Regulator (U1) from the various line (mains) voltages.

Power Supply Rectifier and Regulator Assembly

Diodes A9CR3 through A9CR6 comprise a bridge rectifier circuit with capacitors A9C1 and C2 providing filtering for the rectified voltages. The filtered dc voltages are applied to the V_{in} inputs of A9U1 and A9U2 voltage regulators which provide regulated − and +15V.

Diodes A9CR1 and A9CR2 provide full-wave rectification of the 12 VAC secondary voltage.

+5V Regulator

The +5V Regulator (U1) is mounted on the rear panel for heat-sinking purposes. Capacitors C1 and C2 provide filtering for the input voltage to pin 1 of U1. The +5 Vdc output voltage of U1 is applied to a 6.2 volt zener diode (A10VR1) that provides over-voltage protection for the +5V supply. This protects the integrated circuits should the +5V supply go higher than 6.2 volts.

TROUBLESHOOTING

WARNINGS

If this instrument is to be energized via an auto-transformer for voltage reduction, make sure the common terminal is connected to the earthed pole of the power source. BEFORE SWITCHING ON THIS INSTRUMENT, the protective earth terminals of this instrument must be connected to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding).

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal is likely to make this instrument dangerous. Intentional interruption is prohibited.

Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuse holders must be avoided.

Whenever it is likely that the protection offered by fuses has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
Adjustments and service described herein are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

CAUTIONS

LINE VOLTAGE SELECTION

BEFORE SWITCHING ON THIS INSTRUMENT, make sure the instrument is set to the voltage of the power source.

BEFORE SWITCHING ON THIS INSTRUMENT, ensure that all devices connected to this instrument are connected to the protective (earth) ground.

BEFORE SWITCHING ON THIS INSTRUMENT, ensure that the line power (mains) plug is connected to a three-conductor line power outlet that has a protective (earth) ground. (Grounding one conductor of a two-conductor outlet is not sufficient.)

Set the LINE ON-OFF switch to OFF and remove the Line Power Cord (W8) from the Line Power Module (A11). Remove the red (2), violet (7), and white-red (92) wires from the feed-thru capacitors (C3, C4, and C5). Replace the Line Power Cord (W8) and set LINE ON-OFF to ON. If the supply voltages are now correct, the trouble is not in the Power Supply. If the +5V supply is still too low or too high, U1 or U2 is probably at fault. If either the +15V or −15V supplies are the source of trouble, the complete unit (U1 or U2) must be replaced. Any other problems can be solved with the aid of a VOM.

◀ Power Reference Oscillator Assembly (A8)
SERVICE SHEET 14

A8A1 ASSEMBLY

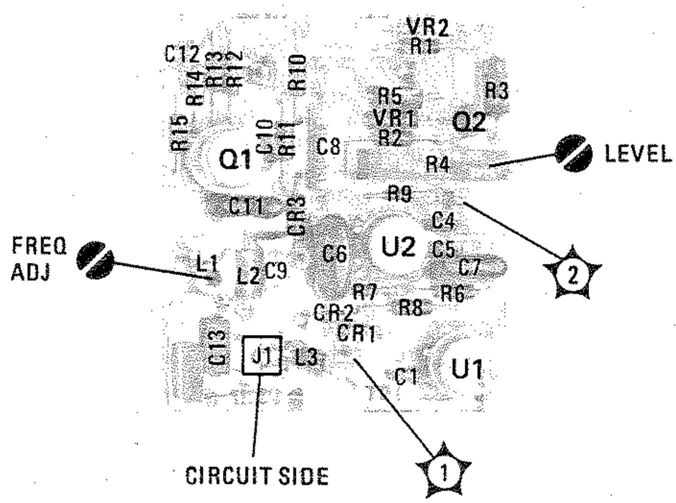
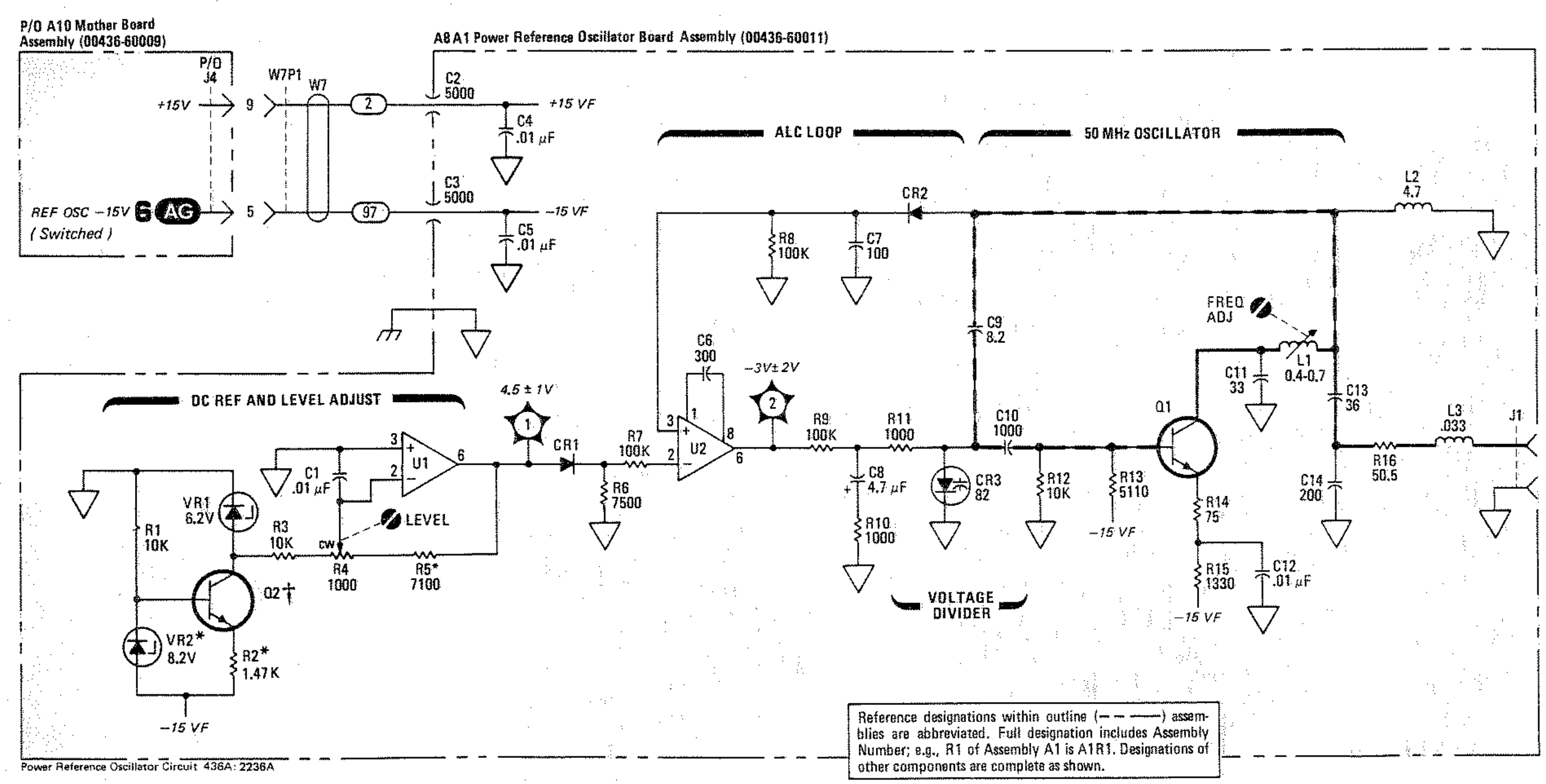


Figure 8-44. A8A1 Power Reference Oscillator Board Assembly Component, Test Point and Adjustment Locations



Reference designations within outline (— — ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. Unless otherwise indicated:
   Resistance in ohms;
   Capacitance in picofarads;
   Inductance in microhenries.
2. Asterisk (*) indicates selected component, average values shown.
3. W6 (omitted option 003)
   W10 (option 003).

† Backdating information is found in Section VII.

REFERENCE DESIGNATIONS

NO PREFIX	A8 A1 ASSY
J2 W6/W10 W7 W6P1/W10P1 W7P1	C1-14 CR1-3 J1 L1-3 Q1,2 R1-16 TP1,2 U1,2 VR1
A10 ASSY	
J4	

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBER
Q1	1854-0247
† Q2	1854-0810
U1	1826-0013
U2	1820-0223

INTEGRATED CIRCUIT VOLTAGE CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBER
U1,2	+15 VF − 7 −15 VF − 4

14
A8,A10

Figure 8-45. Power Reference Oscillator Assembly Schematic Diagram

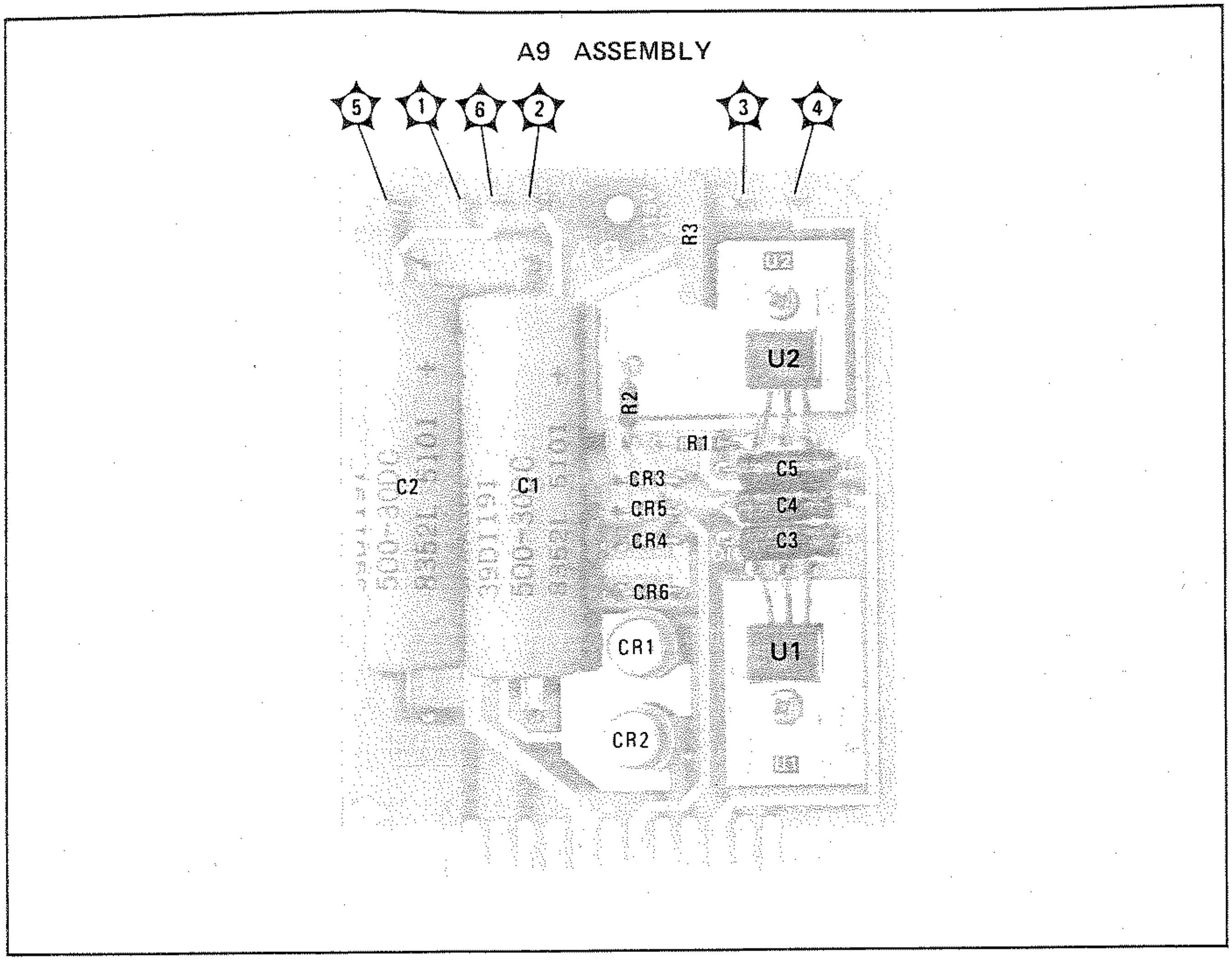


Figure 8-46. A9 Power Supply Rectifier and Regulator Assembly Component and Test Point Locations

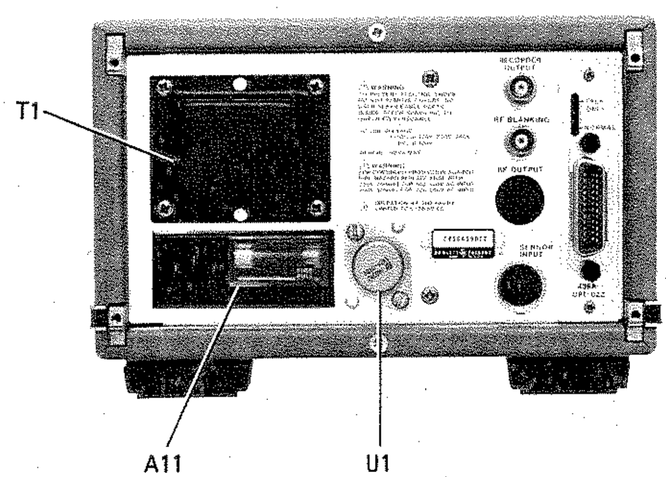
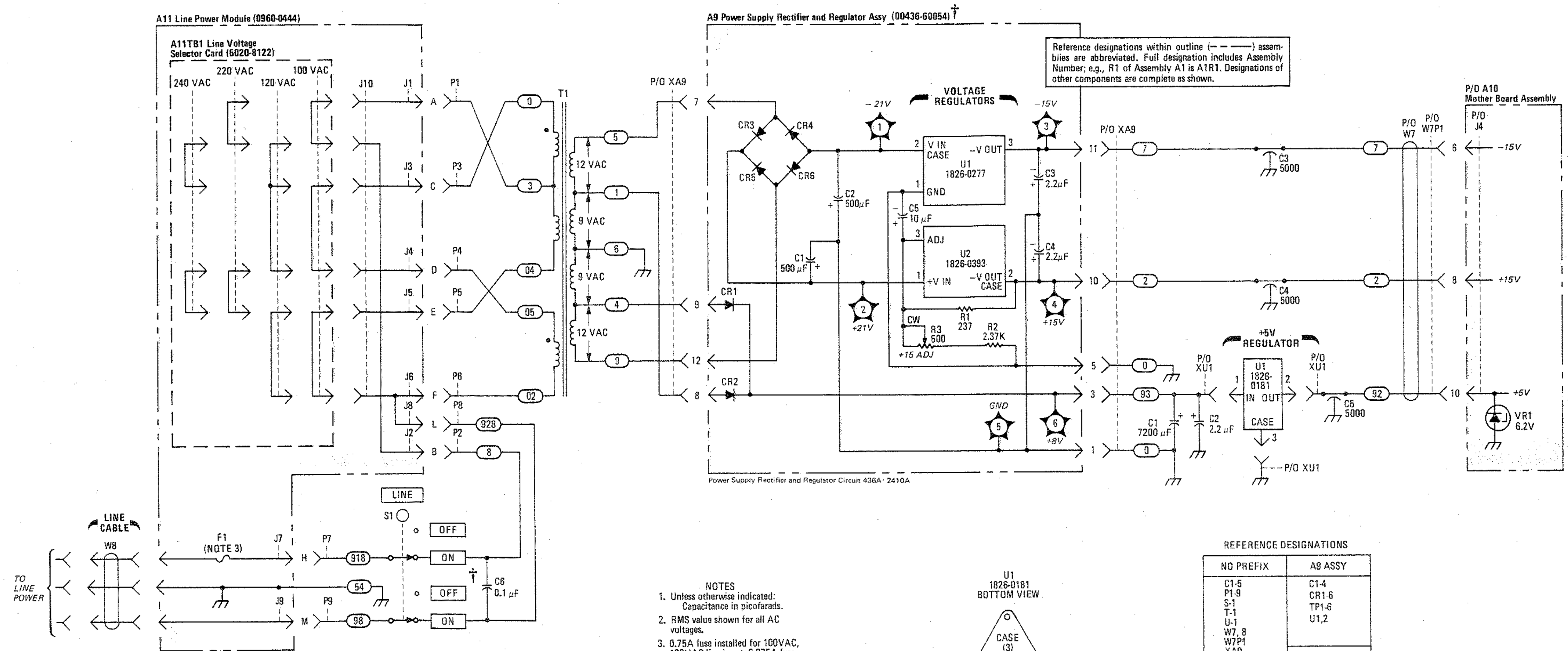
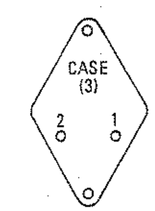


Figure 8-47. Rear Panel Mounted Power Supply Component Locations





WARNINGS

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal is likely to make this instrument dangerous. Intentional interruption is prohibited.

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

CAUTIONS

Before switching on this instrument, make sure the instrument is set to the voltage of the power source.

Before switching on this instrument, ensure that all devices connected to this instrument are connected to the protective (earth) ground.

Before switching on this instrument, ensure that the line power (mains) plug is connected to a three-conductor line power outlet that has a protective (earth) ground. (Grounding one conductor of a two-conductor outlet is not sufficient.)

NOTES

1. Unless otherwise indicated: Capacitance in picofarads.
2. RMS value shown for all AC voltages.
3. 0.75A fuse installed for 100VAC, 120VAC line input; 0.375A fuse installed for 220VAC, 240VAC line input.

† Backdating is found in Section VII

REFERENCE DESIGNATIONS

NO PREFIX	A9 ASSY
C1-5, P1-9, S-1, T-1, U-1, W7, 8, W7P1, XA9, XU1	C1-4, CR1-6, TP1-6, U1,2
	A11 ASSY
A10 ASSY	F1, J1-10
J4, VR1	

15

A9,A10,A11

Figure 8-48. Power Supply Rectifier and Regulator Assembly Schematic Diagram

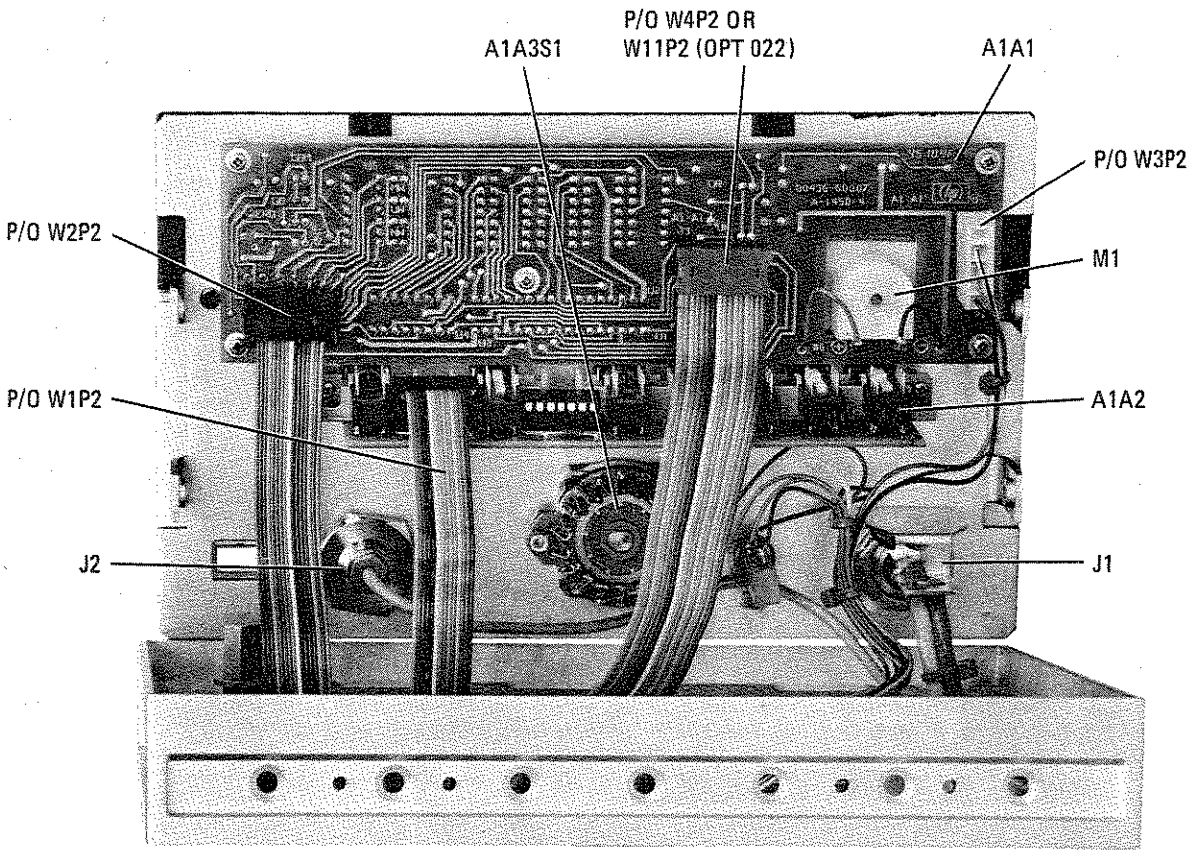


Figure 8-49 Rear View of Front Panel (Removed)

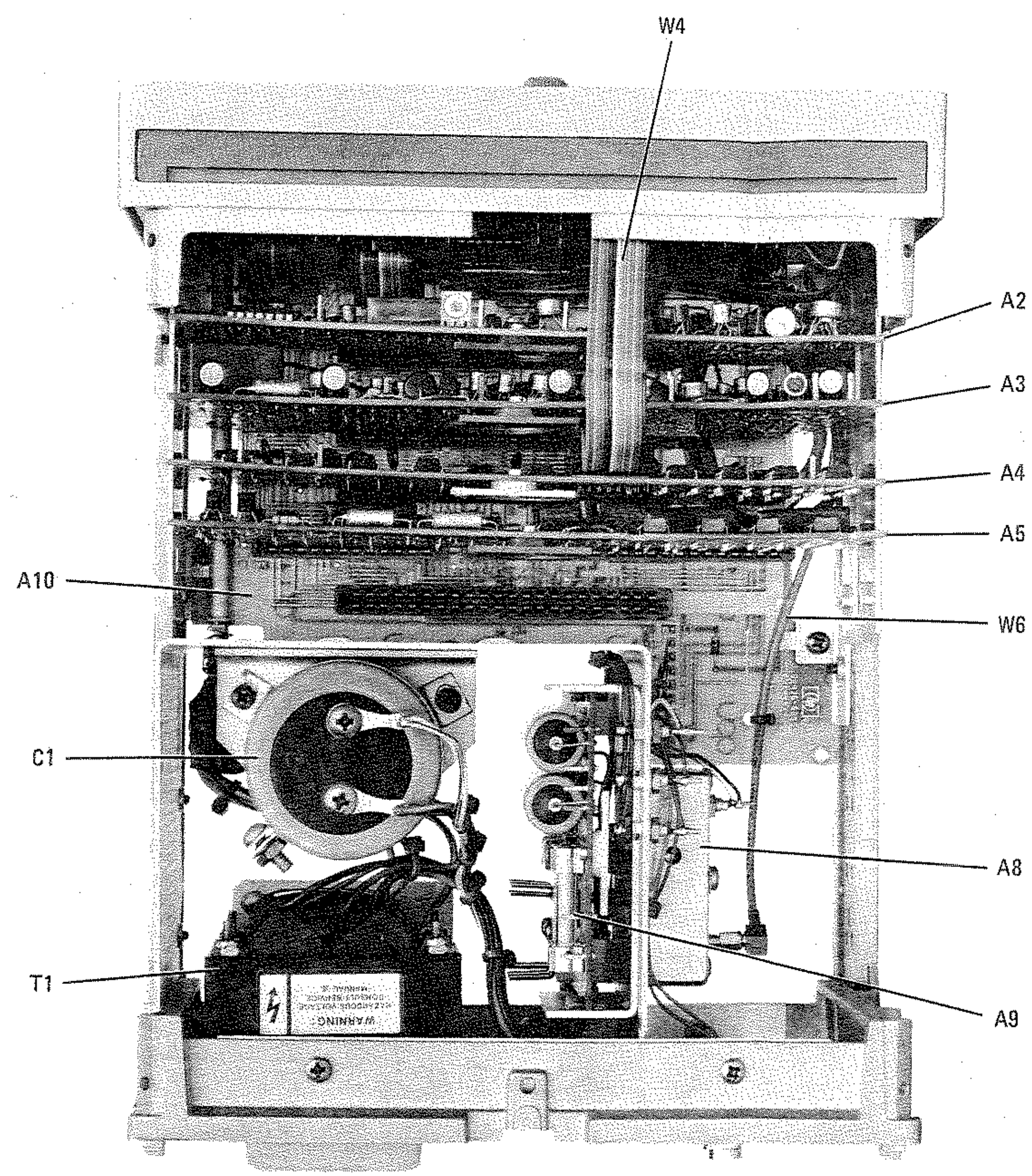


Figure 8-50 Top Internal View Standard Instrument

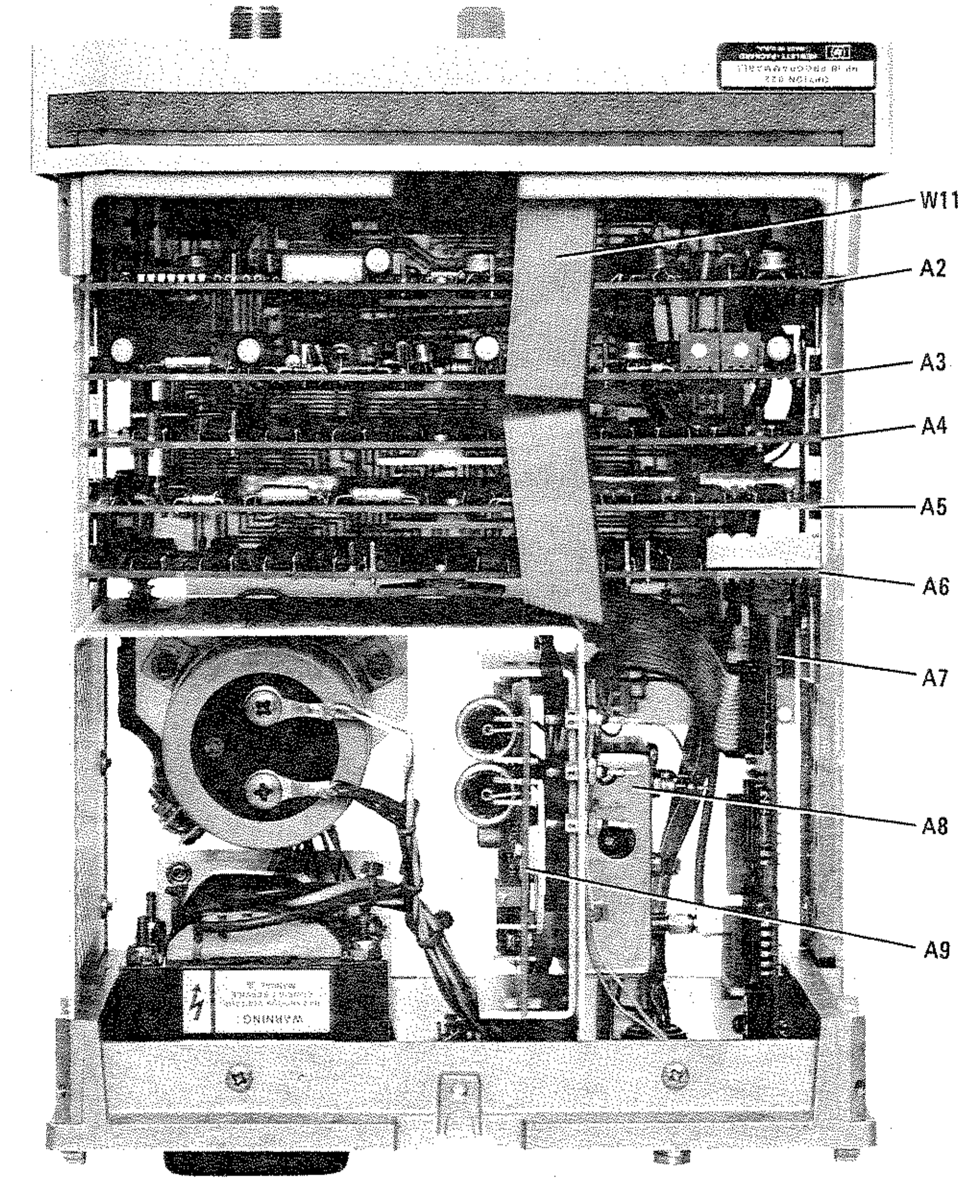


Figure 8-51 Top Internal View HP-IB