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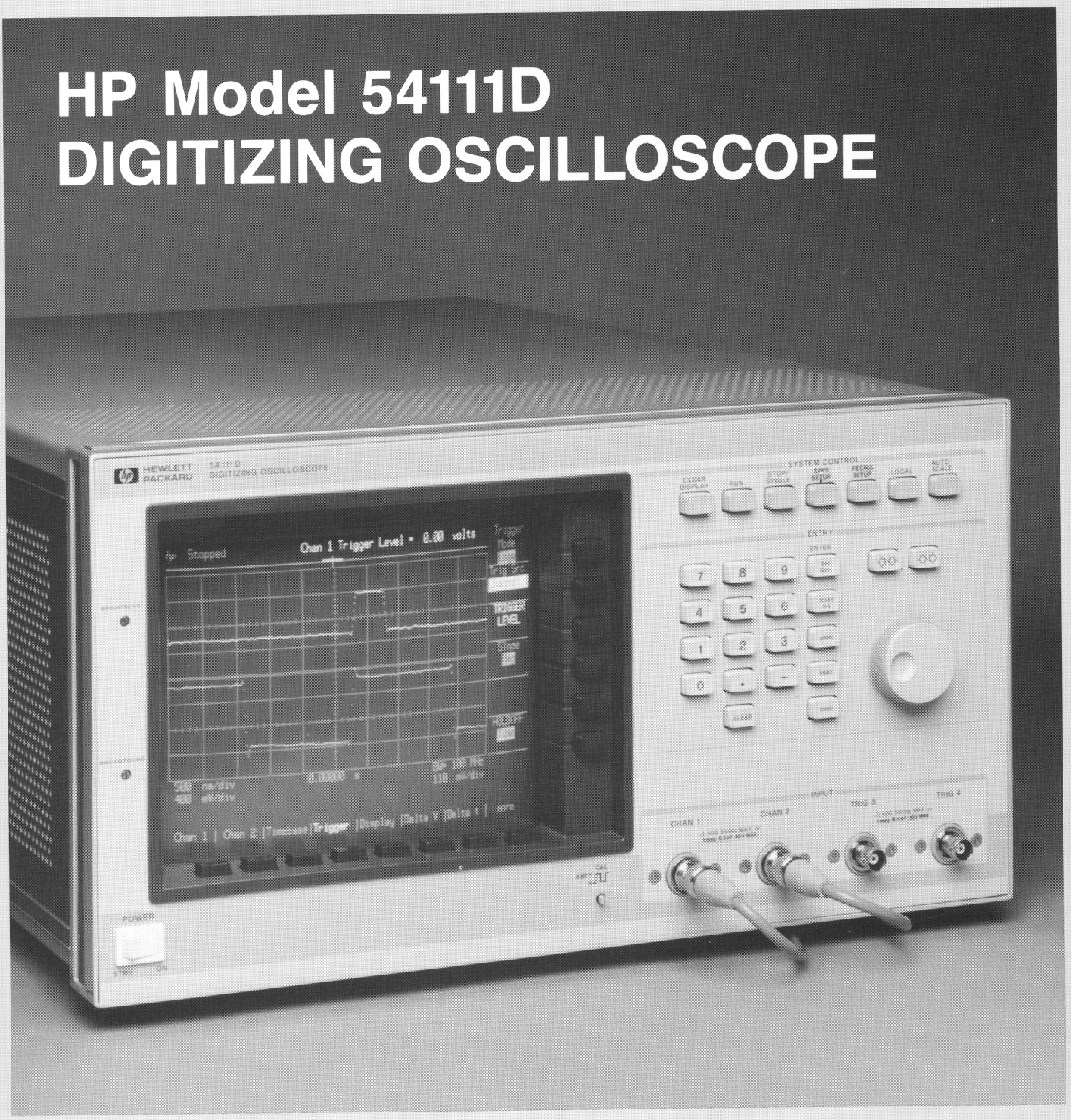
# SERVICE MANUAL

# HP Model 54111D
# DIGITIZING OSCILLOSCOPE




HEWLETT PACKARD

HEWLETT PACKARD

SERVICE MANUAL

# HP 54111D

# DIGITIZING OSCILLOSCOPE

**SERIAL NUMBERS**

This manual applies directly to instruments with serial numbers prefixed:

2808A

With changes described within, this manual also applies to instruments with serial prefixes:

2640A
2710A
2726A
2733A

For additional important information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section I.



Manual Part No. 54111-90912
Microfiche Part No. 54111-90812

**PRINTED: June 1988**

### CERTIFICATION

*Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.*

## WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument or software, or firmware will be uninterrupted or error free.

### LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

### EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

## ASSISTANCE

*Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.*

*For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.*

**CWA584**

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# SECTION 1
# GENERAL INFORMATION

## 1-1. INTRODUCTION

This Service Manual contains information necessary to test, adjust, and service the Hewlett-Packard 54111D Digitizing Oscilloscope. This manual is divided into nine sections as follows:

1 - General Information

2 - Installation

3 - Performance Tests

4 - Adjustments

5 - Replaceable Parts

6A - Instrument Disassembly

6B - Theory of Operation

6C - Service Menus/Keys

6D - Self-Tests/Troubleshooting

Information for operating, programming, and interfacing the HP 54111D is contained in the HP 54111D Operating and Programming Manual supplied with each instrument.

The General Information Section includes a description of the HP 54111D Digitizing Oscilloscope, its specifications, characteristics, options, and available accessories.

Listed on the title page of this manual is a Microfiche part number. This number can be used to order 4 X 6 inch microfilm transparencies of the manual. Each microfiche contains up to 96 photo-duplicates of the manual pages. The microfiche package also includes the latest Manual Changes supplement as well as pertinent Service Notes.

## 1-2. DESCRIPTION

The HP 54111D is a fully programmable, real-time digitizing oscilloscope. It uses a sample rate of 1 GS/second which gives a repetitive bandwidth of 500MHz and a real-time bandwidth of 250 MHz.

The inputs include two vertical signal channels and two trigger channels. The inputs can be set up for 50 Ohm impedance with dc coupling or 1 MOhm at 6.5 pf with ac or dc coupling. The signals from the vertical and trigger channels can be used to provide a qualified trigger for the instrument that can be a pattern of levels and/or edges (see table 1-2).

The color display of the HP 54111D provides 16 colors which are mapped to provide specific colors for specific functions. For example, channel 1 is displayed in yellow, channel 2 is displayed in green and error messages are displayed in red.

To ensure proper operation, extensive self-tests have been designed into the instrument. These self-tests are in addition to internal diagnostics which aid in efficient fault locating and repair should a failure occur.

## 1-3. SPECIFICATIONS

Instrument specifications are listed in table 1-1. These specifications are the performance standards against which the oscilloscope is tested.

## 1-4. OPERATING CHARACTERISTICS

Table 1-2 is a listing of the instruments operating characteristics. The operating characteristics are not specifications, but are typical operating characteristics included as additional information for the user.

## 1-5. GENERAL CHARACTERISTICS

Table 1-3 gives environmental limits, input power requirements, and mechanical dimensions.

## 1-6. SAFETY CONSIDERATIONS

This product is a Safety Class 1 instrument (provided with a protective earth terminal). Review the instrument and manual for safety markings and instructions before operating. A page, Safety Considerations, covering general safety concerns, is in the front of this manual. Specific warnings, cautions, and instructions are placed wherever applicable throughout the manual. These precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this instrument.
Hewlett-Packard assumes no liability for the customer's failure to comply with these requirements.

## 1-7. INSTRUMENTS COVERED BY MANUAL

The instrument serial number is located on the rear panel. Hewlett-Packard uses a two-part serial number consisting of a four-digit prefix and a five-digit suffix separated by a letter **(0000A00000).** The prefix is the same for all identical instruments and changes only when a modification is made that affects parts compatibility. The suffix is assigned and is different for each instrument. This manual applies directly to instruments with the serial prefixes shown on the title page.

An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

## 1-8. OPTIONS

In addition to power cord options, the following options are available for the HP 54111D:

- W30: Additional two years "return to HP"service support commencing at the end of the standard warranty.
- 090: Deletion of the two 10:1 divider probes.
- 908: Rack mounting kit.
- 910: Extra set of manuals consisting of Operating and Programming manuals and one Service manual.

## 1-9. ACCESSORIES SUPPLIED.

The following accessories are supplied with the HP 54111D:

- Two 10:1 divider probes, HP Model No. 10431A.
- One power cord.
- One set of operating and programming manuals.
- One service manual.

## 1-10. RECOMMENDED TEST EQUIPMENT

Equipment recommended to maintain the HP 54111D is listed in table 1-4. The function for which a piece of equipment is needed (Performance Tests, Adjustments, or Troubleshooting) is also given in the table.

*Table 1-1. Specifications*

## VERTICAL (VOLTAGE) [1]

| | | |
|---|---|---|
| **Channels** | 2 | |
| **Bandwidth (–3 dB)[2]** | **Real-time** | **Repetitive** |
| **dc-coupled** | dc to 250MHz | dc to 500 MHz[3] |
| **ac-coupled** | 10 Hz to 250 MHz | 10 Hz to 500 MHz[3] |
| **Transition Time (10% to 90%)** | See "Operating Characteristics" | 700 ps |
| **Deflection Factor (full-scale=8 div)** | 1 mV/div to 5 V/div continuous | |
| **Resolution (% of full scale)** | 8 bits to 25 MHz, (0.4%)<br>7 bits to 100 MHz, (0.8%)<br>6 bits to 250 MHz, (1.6%) | 6 bits, (1.6%)<br>8 bits with averaging<br>to 500 MHz, (0.4%) |
| **DC Gain Accuracy** | ±2% of full-scale [4] | |
| **DC Offset Accuracy** | ±1.5% of setting ±0.2 div [5] | |
| **DC Measurement Accuracy**<br>**single data point** | ±Gain Acc. ±Offset Acc. ±Resolution | |
| **between data points on same waveform** | ±Gain Acc. ±2 × Resolution | |
| **DC Offset Range** | ±200 mV (1 mV/div to 4 mV/div)<br>±1 V (5 mV/div to 49 mV/div)<br>±10 V (50 mV/div to 499 mV/div)<br>±40 V (500 mV/div to 5 V/div) | |
| **Input Coupling** | ac/dc/dc-50 Ω/gnd | |
| **Maximum Safe Input Voltage** | ±40 Volts @ 1 MΩ (dc + peak ac),<br>5 Vrms @ 50 Ω | |

**NOTE** *All voltages in table correspond to a 1:1 attenuation setting. If a 10:1 probe is attached, multiply all voltages by 10. The HP 10033A has a maximum voltage of ±200 V.*

1 Applies for temperature ranges ±5° C from point of last self-calibration.

2 Upper bandwidth limit for settings 1 mV/div to 4 mV/div is reduced to 150 MHz.

3 Repetitive bandwidth at sweep speeds 10 us/div and slower is not specified.

4 When calibrated to probe tip using the front panel calibration source. Applies to major ranges (5 mV/div, 10 mV/div, 20 mV/div, 50 mV/div, 100 mV/div, 200 mV/div, 500 mV/div, 1 V/div, 2 V/div). All settings other than these ranges are ±3% of full-scale. All settings from 1 mV/div to 4 mV/div are ±4% of full-scale.

5 Increases to ±.4 divisions at 5 mV/div to 9 mV/div, and ±1 division below 5 mV/div.

*Table 1-1. Specifications (cont.)*

| HORIZONTAL (TIME) [1] | Real-time | Repetitive |
|---|---|---|
| Digitizing Rate | 1 gigasample/s to 50 sample/s | |
| Deflection Factor | 500 ps/div to 1 s/div | |
| Memory Depth per Channel | 8K | 501 |
| Pre-trigger Delay Range | −8 μs at timebase settings 50 ns/div and faster, increasing to −160 s at 1 s/div. | |
| Post-trigger Delay Range | 160 ms at timebase settings 500 ns/div and faster, increasing to 10,000 s at 1 s/div. | |
| Time Interval Measurement Accuracy single channel | ±300 ps [2] ±0.03% of reading | ±100 ps [2] ±0.03% of reading |
| dual channel | ±600 ps [3] ±0.03% of reading | ±200 ps [3] ±0.03% of reading |

## TRIGGERING

| Sources | Internal Channels 1,2 | External Triggers 3,4 |
|---|---|---|
| Sensitivity | 0.1 of full-scale, dc to 200 MHz [4]<br>0.2 of full-scale, 200 MHz to 500 MHz [4] | 15 mV (high sensitivity) [5] dc to 200 MHz<br>45 mV (high sensitivity) [5] 200 MHz to 500 MHz |
| Trigger Level Range | ±3 x full-scale [6] | ±1 V (high sensitivity) [5] |
| Maximum Safe Voltage | NA | ±10 volts @ 1MΩ (dc + peak ac), 5 Vrms @ 50 Ω |
| Input Operating Range | NA | ±1 V (high sensitivity) [5] dc + peak ac |

1 Applies for temperature ranges ±5° C from point of last self-calibration.

2 Decreased to [±0.2% of time range(time/div x 10) ±0.03% of reading] for time ranges 200 ns and slower.

3 Decreased to [±0.4% of time range(time/div x 10) ±0.03% of reading] for time ranges 200 ns and slower.

4 Applies to settings 5 mV/div to 5 V/div only.

5 For low sensitivity, multiply voltage values by 10.

6 The trigger level range is centered on the offset level. Trigger level range is limited ot ±600 mV from 25 to 49 mV/div inclusive, ±6.0 V from 250 to 499 mV/div inclusive, and by the maximum safe input voltages at 2 V/div and above.

*Table 1-2. Operating Characteristics.*

## VERTICAL

***Real-time Mode Transition Time (10% to 90%):*** 1.4 ns.
Calculated by measuring a 1.4 ns risetime source. In the 6-bit filter mode, a 1.4 ns input risetime is measured as; 2.0 ns = $\sqrt{(1.4)^2 + (1.4)^2}$ .
***Input Impedance:*** 1 MΩ @ <6.5 pF or 50 Ω (dc)
***Input Protection:*** 50 ohm input resistance is protected where input rating is exceeded.
***Dynamic Performance (typical):***

| | Effective Bits of Resolution | | | | |
|---|---|---|---|---|---|
| **Input Frequency** | **1 MHz** | **20MHz** | **90MHz** | **250MHz** | **500MHz** |
| **6-bit Mode** | 5.5 | 5.5 | 5.2 | 5.0 * | N/A |
| **7-bit Mode** | 6.2 | 6.2 | 6.0 | N/A | N/A |
| **8-bit Mode** | 7.2 | 7.0 | N/A | N/A | N/A |

* Unfiltered data transfered over HP-IB.

***Channel-to-channel Isolaton:*** 60dB at 500MHz.

## HORIZONTAL

***Delay Between Channels:*** difference in delay between channels can be front panel calibrated to compensate for differences in input cables or probe length.
***Reference Location:*** the reference point can be located at the left edge, center, or right edge of the display. The reference point is the trigger plus the delay time.

## TRIGGER

**Holdoff**
***Holdoff-by-events:*** range of events counter is from 2 to 67 million events. Maximum counting rate is 80 MHz. An event is defined as anything that satisfies the triggering conditions selected.
***Holdoff-by-time:*** adjustable from 70 ns to 670 ms.

**Trigger Modes**
***Edge trigger:*** on any source.
***Pattern trigger:*** a pattern can be specified for all sources. Each source can be specified as high, low, or don't care. Trigger can occur on the last edge to enter the specified pattern or the first edge to exit the specified pattern.
***Time qualified pattern trigger:*** Trigger occurs on the first edge to exit the specified pattern, only if the pattern was present for less than [greater than] the specified time. Filter time is adjustable from 10 ns to 5 seconds. Recovery time is ≤ 8 ns. In the "Pattern present < [time]" mode, the pattern must be present ≥ 1 ns for the trigger to respond.
***State trigger:*** a pattern can be specified for any of the sources. Trigger can be set to occur on an edge of either polarity on the source specified as the clock (not one of the pattern sources) when the pattern is present or not present. Setup time for the pattern to be present prior to the clock edge is < 4 ns; hold time is zero. Maximum clock repetition rate is 80 MHz.

**Delayed Trigger**
***Events-delayed mode:*** the trigger can be armed by an edge on any source, then triggered by the nth edge on any other source. The number of events, n, can be set from 1 to $10^8$ - 1. Maximum event counting rate is 150 MHz.
***Time-delayed mode:*** the trigger can be armed by an edge on any source, then triggered by the first edge on any other source after a specified time has elapsed.

*Table 1-2. Operating Characteristics (cont.)*

## DISPLAY

***Data Display Resolution:*** 501 points horizontally by 256 points vertically.

**Data Display Formats**

***Split screen:*** channel displays are two or four divisions high, corresponding to quad or dual display mode.

***Full screen:*** channels are overlaid and are eight divisions high.

**Display Modes**

***Variable persistence:*** the time that each data point is retained on the display can be varied from 200 ms to 10 seconds, or it can be displayed in the infinite persistence mode.

***Averaging:*** the number of averages can be varied from 1 to 64. On each acquisition, 1/n times the new data is added to (n-1)/n of the previous value at each time coordinate. Averaging operates continously; the average does not converge to a final value after n acquisitions, except over HP-IB.

***Graticules:*** Full grid, axes with tic marks, frame with tic marks, or graticule off.

***Data Reconstruction:*** on sweep speeds when less than 500 points are acquired across the screen, a built-in digital filter will automatically reconstruct the data in the real-time acquisition modes (single-shot acquisition). The filter "off" position in the display mode will display raw data.

***Display Colors:*** A default color selection is set up. Different colors are used for display background, channels, functions, background text, highlighted text, advisories, markers, overlapping waveforms, and memories. If desired, colors may be changed either from the front panel or over HP-IB.

## HP-IB

***Data Transfer Rate:*** 80k bytes/s

## MEASUREMENT AIDS

***Markers:*** dual voltage markers and dual time markers are available. Voltage markers can be assigned to channels, memories, or functions.

***Automatic Edge Finders:*** the time markers can be assigned automatically to any displayed edge of either polarity on any channel. The voltage markers establish the threshold reference for the time markers in this mode.

***Automatic Pulse Parameter Measurements:*** the following pulse parameter measurements are performed automatically (as defined by IEEE standard 194-1977, "IEEE Standard Pulse Terms and Definitions").

| | |
|---|---|
| Frequency | Overshoot |
| Period | Peak-to-peak voltage |
| Duty Cycle | Average voltage |
| Pos Pulse Width | RMS voltage |
| Neg Pulse Width | Top voltage * |
| Rise time | Base voltage * |
| Fall time | Maximum voltage |
| Preshoot | Minimum voltage |

* only available over the HP-IB.

***Waveform Math:*** two independent functions are provided for waveform math. The operations provided are +, −, and invert. The vertical channels or any of the waveform memories can be used as operands for the waveform math.

## SETUP AIDS

***Presets:*** vertical deflection factor, offset, and trigger level can be preset independently on each channel for ECL and TTL levels.

***Auto-Scale:*** pressing the Auto-Scale button causes the vertical and horizontal deflection factors and the trigger source to be set for a display appropriate to the signals applied to the inputs. Requires a duty cyle greater than 0.1% and frequency greater than 50 Hz. Operative only for relatively stable input signals.

***Save/Recall:*** ten front panel setups may be saved in non-volatile memory. If Auto-Scale is inadvertently pressed, pressing Recall followed by Auto-Scale, restores the instrument to the state prior to the first Auto-Scale.

*Table 1-3. General Characteristics*

## ENVIRONMENTAL CONDITIONS

**Temperature**
**Operating:** 0°C to +55°C (+32°F to +131°F)
***Non-operating:*** −40°C to +75°C (−40°F to +167°F)

**Humidity**
***Operating:*** up to 95% relative humidity (non-condensing) at +40°C (+104°F)
***Non-operating:*** up to 90% relative humidity at +65°C (+149°F).

**Altitude**
***Operating:*** up to 4600 meters (15,000 ft)
***Non-operating:*** up to 15,300 meters (50,000 ft).
***Vibration:*** vibrated in three orthogonal axes for 15 minutes each axis; 0.38 mm (0.015 in) peak-to-peak excursion; 5 to 55 Hz; 1 minute/octave sweep.

## POWER REQUIREMENTS

***Voltage:*** 115/230 V ac, −25% to + 15%, 48-66 Hz.
***Power:*** 350 watts maximum, 700 VA maximum.

## WEIGHT

***Net:*** approximately 27 kg (59 lb).
***Shipping:*** approximately 32 kg (70 lb).

## DIMENSIONS

Refer to the outline drawings.

**NOTES:**

1. *Dimensions are for general information only. If dimensions are required for building special enclosures, contact your HP field engineer.*
2. *Dimensions are in millimetres and (inches).*

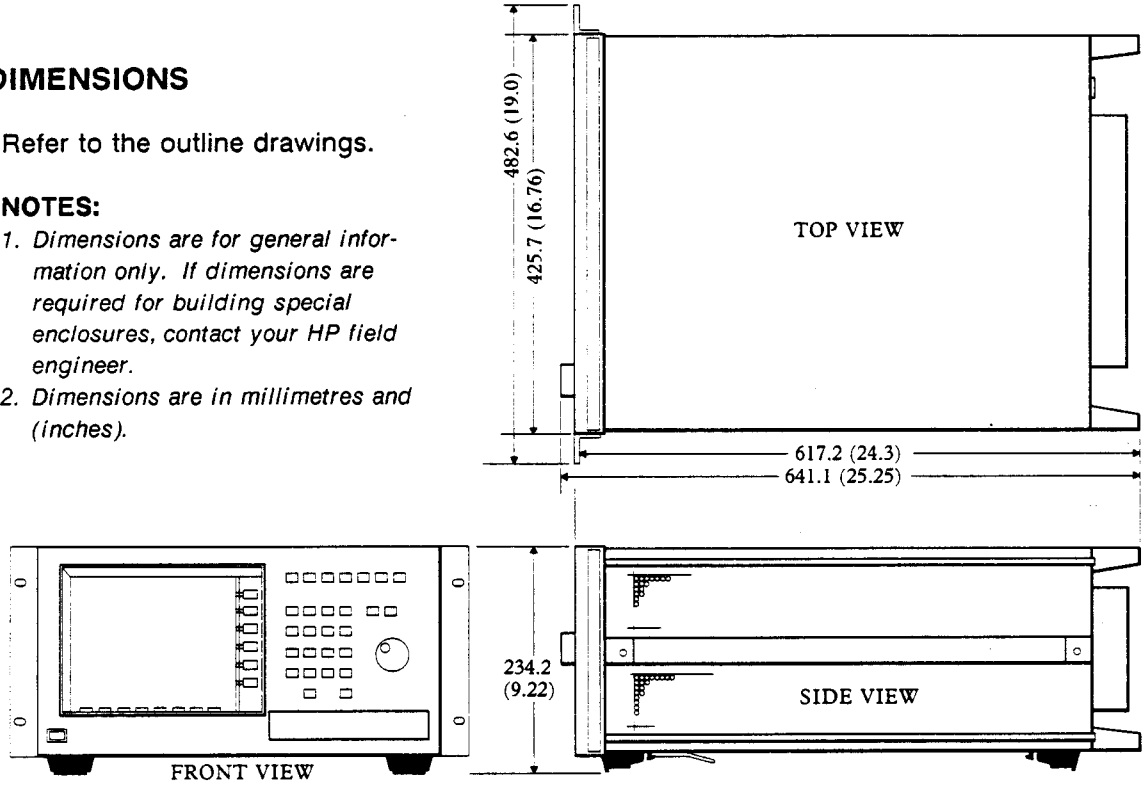


*Table 1-4. Recommended Test Equipment.*

| Equipment Required | Critical Specifications | Recommended Model | Use* |
|---|---|---|---|
| Signal Generator | 100 KHz to 500 MHz, <-34 dBm to >+12 dBm, timebase within ±0.003% | HP 8656B, check time-base to ±0.003% | P |
| Power Meter/Sensor | 100 KHz to 1 GHz, <-22 dBm to >+8 dBm | HP 436A/8482A | P,A |
| Pulse Generator | ≈70 ps transition time | TEK Type 284 | P |
| Digital Multimeter | Better than ±0.05% accuracy | HP 3468A | P,A,T |
| DC Supply | ±30 mV to ±70 V, 0.1 mV resolution | HP 6115A | P,A |
| Pulse Generator | ≤1% perturbation after 10 ns, 0 to -300 mV output pulse | Tektronix PG 506 | A |
| Pulse Generator | 20 ns pulse width at 300 ns period, square wave at >2 μs period, ≤2 ns risetime and falltime | HP 8082A | A |
| Frequency Counter | 51 MHz with 50 mV sensitivity and 6 digit resolution | HP 5384A | A |
| Oscilloscope | General purpose 300 MHz BW | HP 54201A | T |
| Divider Probe | 10:1, 1 MΩ | HP 10431A/033A/017A | P,A,T |
| Power Splitter | Outputs within 0.15 dB to 500 MHz | HP 11667B | P |
| Attenuator | 10 ±0.6 dB from 200-500 MHz | HP 8491B | P |
| Low-pass Filter | >35 dB attenuation at 2 GHz, -3 dB point above 1.250 GHz | RLC F30-1500-N | A |
| Adjustment tool | Non-metallic (for display) | HP 8710-1355 | A |
| Adjustment tool | (for attenuator adjustment) | HP 8710-1515 | A |
| Product Support Kit | No substitute | HP 54100-69006 | T |

* P = Performance Tests, A = Adjustment Procedures, T = Troubleshooting

# SECTION 2
# INSTALLATION

## 2-1. INTRODUCTION

This section contains the initial operation information for the HP 54111D digitizing oscilloscope. Included are power and grounding requirements, operating environment requirements, cleaning methods and storage and shipment requirements.

## 2-2. PREPARATION FOR USE

**POWER REQUIREMENTS.** The instrument requires a power source of either 115 or 230 VAC, -25% to +15%; single phase, 48 to 66 Hz; 350 watts, 700 VA maximum.

CAUTION

*The instrument may be damaged if the Line Voltage Select Switch is not properly set to match the input line voltage.*

**LINE VOLTAGE SELECTION.** Before turning ON the instrument verify that the Line Voltage Select Switch on the rear panel matches the input line voltage.

**POWER CABLE.** This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. See table 2-1 for option numbers of power cables and plug configurations available. Part numbers for each cable option are also listed in the parts list in Section VI.

## 2-3. OPERATING ENVIRONMENT

The operating environment is noted in table 1-3. Note should be made of the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Protection should be provided against internal condensation.

## 2-4. CLEANING REQUIREMENTS

When cleaning the instrument, CAUTION must be exercised on which cleaning agents are used. USE MILD SOAP AND WATER. If a harsh soap or solvent is used, the water-base paint finish WILL BE damaged.

CAUTION

*BE CAREFUL when cleaning the keyboard. Water can damage the keyboard circuitry if it seeps under the keys.*

## 2-5. STORAGE AND SHIPMENT

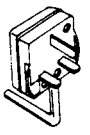
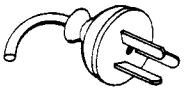
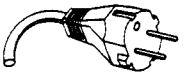
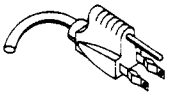
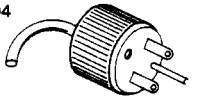
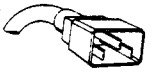
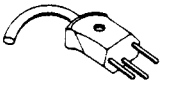
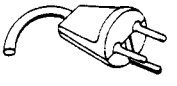
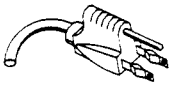
## 2-6. Environment

The instrument may be stored or shipped in environments within the following limits:

**Temperature:** -40 to +75° C (-40 to +167° F)
**Humidity:** Up to 90% at 65° C (+149° F)
**Altitude:** Up to 15 300 metres (50 000 feet)

The instrument should also be protected from temperature extremes which cause condensation within the instrument. Condensation within the instrument may cause malfunction if the instrument is operated under these conditions.

*Table 2-1. Power Cord Configurations*

| PLUG TYPE | CABLE PART NO. | PLUG DESCRIPTION | LENGTH IN/CM | COLOR | COUNTRY |
|---|---|---|---|---|---|
| OPT 900 250V  | 8120-1351<br>8120-1703 | Straight *BS1363A<br>90° | 90/228<br>90/228 | Gray<br>Mint Gray | United Kingdom,<br>Cyprus,<br>Nigeria,<br>Zimbabwe,<br>Singapore |
| OPT 901 250V  | 8120-1369<br>8120-0696 | Straight *NZSS198/ASC<br>90° | 79/200<br>87/221 | Gray<br>Mint Gray | Australia,<br>New Zealand |
| OPT 902 250V  | 8120-1689<br>8120-1692<br>8120-2857 | Straight *CEE7-Y11<br>90°<br>Straight (Shielded) | 79/200<br>79/200<br>79/200 | Mint Gray<br>Mint Gray<br>Coco Brown | East and West Europe,<br>Saudi Arabia,<br>So. Africa,<br>India (Unpolarized<br>in many nations) |
| OPT** 903 125V  | 8120-1378<br>8120-1521<br>8120-1992 | Straight *NEMA5-15P<br>90°<br>Straight (Medical)<br>UL544 | 90/228<br>90/228<br>96/244 | Jade Gray<br>Jade Gray<br>Black | United States,<br>Canada,<br>Mexico,<br>Philippines,<br>Taiwan, |
| OPT** 904 250V  | 8120-0698 | Straight *NEMA6-15P | 90/228 | Black | United States,<br>Canada |
| OPT 905 250V  | 8120-1396<br>8120-1625 | CEE22-V1<br>(System Cabinet Use)<br>250V | 30/76<br>96/244 | Jade Gray | For interconnecting<br>system components and<br>peripherals.<br>United States and<br>Canada only |
| OPT 906 250V  | 8120-2104<br>8120-2296 | Straight *SEV1011<br>1959-24507<br>Type 12<br>90° | 79/200<br>79/200 | Mint Gray<br>Mint Gray | Switzerland |
| OPT 912 220V  | 8120-2956<br>8120-2957 | Straight *DHCK107<br>90° | 79/200<br>79/200 | Mint Gray<br>Mint Gray | Denmark |
| OPT 917 250V  | 8120-4211<br>8120-4600 | Straight SABS164<br>90° | 79/200<br>79/200 | Jade Gray | Republic of South Africa<br>India |
| OPT 918 100V  | 8120-4753<br>8120-4754 | Straight Miti<br>90° | 90/230<br>90/230 | Dark Gray | Japan |

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP Part Number for complete cable including plug.
**These cords are included in the CSA certification approval of the equipment.
E = Earth Ground
L = Line
N = Neutral

AC.CABLES3

## 2-7. Packaging

**TAGGING FOR SERVICE.** If the instrument is to be shipped to a Hewlett-Packard office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

**ORIGINAL PACKAGING.** If the original packing material is not available or is unserviceable, material identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is to be shipped to a Hewlett-Packard office for servicing, attach a tag showing owner (with address), model number, complete instrument serial number, and a description of the service required. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

**OTHER PACKAGING.** The following general instructions should be used for repacking with commercially available materials.

a. Wrap instrument in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350 lb. test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

# SECTION 3
# PERFORMANCE TESTS

## 3-1. INTRODUCTION

The procedures in this section test the instrument's electrical performance using specifications in Section I as performance standards. The specification is also listed at the test for reference.

## 3-2. CALIBRATION CYCLE

This instrument requires periodic verification of performance. The instrument should be checked using the following performance tests yearly or every 2000 hours of operation. Amount of use, environmental conditions, and the users experience concerning need for calibration will contribute to performance verification requirements.

## 3-3. CALIBRATION REQUIREMENTS

To perform calibration of the HP 54111D, follow these steps:

1. Perform CLOCK and GAP adjustments in section 4.

2. Set up and look at the flatness using the GAIN and FLAT Adjustments procedure in section 4. Do not adjust unless necessary. If necessary, follow the procedure to adjust.

3. Ensure that the front panel CAL signal is 800 ±2 mV. Follow the Calibrator Amplitude Adjustment procedure in section 4 but do not adjust unless it is outside the above tolerance.

4. Perform the vertical self-calibration, ADC Reference Cal, Vertical Cal, and Probe Tip Cal per section 4.

5. Check the DC Gain Adjustment as in section 4. Do not adjust unless needed.

6. Perform Trigger Cal per section 4.

7. Perform Channel Skew per section 4.

8. Perform the Trigger Qualifier Adjustment procedures, checking first and adjusting only if necessary.

9. Perform all Performance Test procedures and record the results.

Use the following table to take the appropriate action in the event of a failed specification.

| FAILED PERF. TEST | ADJUSTMENT(S) OR ACTION |
|---|---|
| Measurement Accuracy | -Vertical self-cals<br>DC GAIN |
| Time Interval Accuracy | -Timebase Frequency Cal |
| Bandwidth | -Call HP Cust. Service |
| Transition Time | -Call HP Cust. Service |
| Trigger Sensitivity | -Call HP Cust. Service |

To perform a MIL STD calibration, do all Performance Tests first and record results in the performance record. Then perform the calibration as above.

## 3-4. TEST EQUIPMENT REQUIRED

Equipment recommended for performance tests is listed in table 1-4. Individual tests list the equipment necessary for that test. Any equipment that satisfies critical specifications given in the tables may be substituted.

## 3-5. TEST RECORD

Results of performance tests may be entered in the Performance Test Record (table 3-2) at the end of the procedures. The Test Record lists the tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison in periodic maintenance and troubleshooting and when testing after repairs or adjustments.

## 3-6. ABBREVIATED TEST PROCEDURES

To save time and the need for some test equipment, some tests can be dropped from the complete procedure. Following are two tests which may be dropped and reasons why.

TRANSITION TIME. Transition time has a close relationship with bandwidth. If bandwidth passes, the Transition Time test is not likely to fail. Dropping this test saves time and avoids the need for the fast transition pulse generator that is only used for this test (see Recommended Test Equipment table).

TIME INTERVAL ACCURACY. This test can be dropped if the Channel Skew and Timebase Frequency Cal are accurate. If such is the case, the Time Interval Accuracy test is not likely to fail. Dropping this test saves time.

## 3-7. TESTS AFTER REPLACEMENTS

Some performance tests may be necessary after replacement of an assembly, though it may not be necessary to test the entire instrument. Table 3-A (below) gives the minimum performance testing required after replacement of major assemblies.

*Table 3-1. Performance Tests Required After Assembly Replacement.*

| PERF. TEST / ASSEMBLY | Calibrator Amplitude | Measurement Accuracy | Offset Accuracy | Band-width | Rise-time | Time Interval Accuracy | Trigger Sens. |
|---|---|---|---|---|---|---|---|
| **Timebase** | # | X | | | | X | |
| **ADC Control** | | RCO | RCO | | | | RCO |
| **ADC** | | RCO | RCO | RCO | RCO | | |
| **Trigger** | | | | | | | Trig 3,4 |
| **Channel Atten.** | | RCO | RCO | RCO | RCO | | RCO |
| **Trigger Atten.** | | | | | | | RCO |

**NOTE:** No performance tests are required after replacing either the **Microprocessor, Input/output, Trigger Qualifier** or **Color Display** assemblies, the **Color CRT Module**, or the **Power Supplies**.

**KEY:**

- # Timebase assembly replacement requires Calibrator Amplitude adjustment. Adjustment sets calibrator amplitude with greater accuracy than the performance test requires so the performance test is unnecessary.
- X This test must be performed.
- RCO Replaced Channel Only. Perform the test only on the channel in which the assembly was replaced.

## 3-8. PROBES USED DURING TESTS

The HP 54111D uses a ring around the input BNC to sense a grounded contact pin on certain 10:1 probes, such as the HP 10431A, or 10033A. The HP 54111D scales the input properly when those 10:1 probes are being used.

Some parameters of the HP 54111D are specified with the instrument calibrated through a probe to the front panel CAL signal or a 10 V supply. Therefore, some of the performance tests require the use of a 10:1 divider probe and using the Probe Tip Cal to calibrate the instrument with that probe.

In the event that the probes shipped with the HP 54111D are not available for performance tests, any probe with comparable specifications, it must be a 1 MΩ probe designed for 1 MΩ inputs, may be used whether it has the grounded contact pin or not. Probe Tip Cal assumes that a 10:1 probe is being used so the calibration is properly done. The performance test procedures are written to allow use of unsensed probes, such as the HP 10017A.

Calibration with the probe is a user function. The HP 54111D can be calibrated to other probes once it is returned to the user.

## 3-9. PERFORMANCE TEST PROCEDURES

Performance test procedures start with the next paragraph. Any one, or all procedures may be done in any order.

**NOTE**

*Allow instrument to warm up for at least 30 minutes prior to beginning performance tests.*

## 3-10. ONE-KEY POWER UP

A one-key power up is a procedure where any one key is held depressed when the power is turned on. The key is held depressed until the power up cycle completes; "Powerup Self Test Passed!" (or Failed) is displayed. This is done to preset or reset the instrument to default conditions and prevent previous setups from interfering with the next test. It also simplifies the instrument setup procedure.

The one-key powerup is a part of many procedures and should be performed like any other procedural step.

## 3-11. CALIBRATOR AMPLITUDE

**Description:**

This procedure checks the amplitude of the front panel calibrator. This signal is used to run calibration routines in the instrument.

When being adjusted, this signal has a tighter specification than that required for passing this test. This is done to maintain the performance specification to the end of the calibration cycle (see Calibration Requirements).

**Specification:**

+0.8 ±0.008 Vdc

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| DC Voltmeter | Better than 0.25% accuracy | HP 3468A |

**Procedure A:**

1. Connect the voltmeter input to the front panel calibrator signal. Connect the voltmeter ground to the CHAN 1 input BNC ground.

2. With the softkeys, press ***more, Utility, Cal Menu, Timebase Cal***, and ***Timebase Freq Cal***.

3. If the voltmeter reads about +0.8 Vdc continue to step 4. If the measurement is about +0.4 Vdc, this instrument's hardware requires manual intervention to perform this test. Press ***Exit*** and continue with Procedure B on the next page.

4. The CAL signal should be +0.8 ±0.008 Vdc. Record the value and press ***Exit***.

**Procedure B:**

The calibrator output must be forced high manually.

1. Remove the top rear feet and the top cover.

2. Connect the voltmeter to the front panel CAL signal.

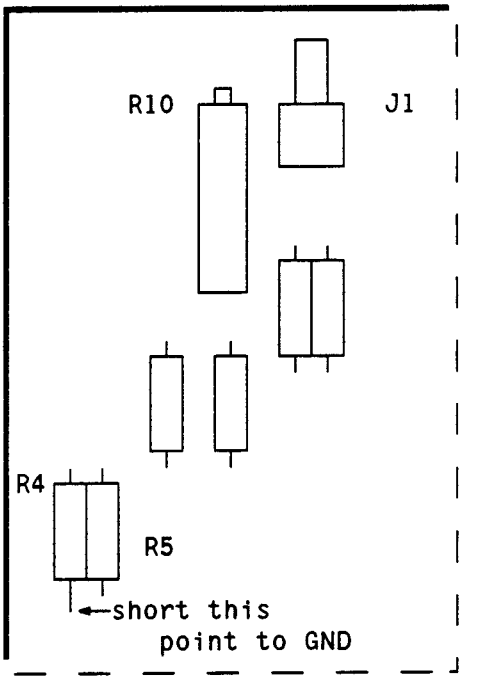
3. The drawing shows the top front corner of the Timebase assembly A1. The Timebase assembly is the left-most assembly in the card cage. Note the position of R4, specifically the bottom end of this resistor.

4. Connect one end of a jumper wire to the body of J1 on the Timebase. Connect a long grabber to the other end of the jumper.

5. Connect the grabber to the bottom end of R4.

6. The CAL signal should be +0.8 ±0.008 V. Record the value.

*Top-front corner of Timebase assy. (A1)*



## 3-12. MEASUREMENT ACCURACY

**Description:**

This test verifies the measurement accuracy of the instrument with a 10:1 probe at the input. Measurement accuracy consists of gain accuracy and resolution. The test uses positive and negative DC levels so that any OFFSET errors are nulled.

**Specification:**

Repetitive 6-bit with averaging and with a 10:1 probe at the input.

10 mV to 40 mV/div = ±4.8% of full scale * [4% gain +2 x resolution(0.4%)]
50 mV/div and above ** = ±2.8% of full scale * [2% gain +2 x resolution(0.4%)]

* Full scale = 8 div X V/div ** Major ranges only

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| DC Supply | ±30 mv to ±100 Vdc<br>0.1 mV resolution | HP 6115A |
| DC Voltmeter | Better than 0.1% accuracy | HP 3468A |
| Oscilloscope Probe | 10:1 1 MΩ | HP 10431A/033A/017A |

**Procedure:**

In this procedure, a positive then negative voltage is applied at each V/div range. Each voltage is measured and the difference is used to check gain on that range. With a supply like the HP 6115A, polarity is changed by floating the supply and reversing the connection of the probe to get the negative value. If you are using a supply with a polarity switch (or a voltage standard with negative voltage capability), reversing the probe connection is not necessary.

1. Perform a one-key powerup* to set instrument to default conditions, then set the following additional parameters.

   *Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Chan 1,2 | Display<br>VOLTS/DIV | Chan 1 ON/Chan 2 OFF<br>as required |
| Timebase | TIME/DIV | 2 us/div |
| Display | NUMBER OF AVERAGES<br>Screen | 64<br>Single |
| Delta V | V Markers | ON |

2. Connect the 10:1 divider probe to the CHAN 1 input of the HP 54111D and the front panel CAL signal and press ***more***.

3. If you are using an HP 10431A or 10033A probe, skip this step. Press ***Utility, Probe Menu,*** and ***CHAN 1 PROBE ATTN***, then in the ENTRY keys, 10 and ENTER.

4. Calibrate the HP 54111D to the 10:1 probe being used for the test. Press ***Utility, Cal Menu, Probe Tip Cal, Calibrate Probe Tip CHAN 1***, and ***Continue***. When calibration is done press ***Exit, more, Chan 1***, and ***VOLTS/DIV***.

5. Set the power supply to 0.0 V and remove any connection between the output and ground.

6. Use the following table for steps 7 through 17. For the first three V/div settings it is necessary to set the supply within ±0.1 mV with the voltmeter.

**WARNING**

*This test uses voltages of ±70 Vdc. Excercise caution to avoid shock hazard.*

| SCOPE V/div | INPUT VOLTAGE SETTINGS# | Δ | MEASURED Δ VOLTAGE LIMITS TOLERANCE | MIN | | MAX |
|---|---|---|---|---|---|---|
| 10 mv | ±35 mV* | 70 mV | ±4 mV | 66.0 mV | _____ | 74.0 mV |
| 20 mv | ±70 mV* | 140 mV | ±8 mV | 132 mV | _____ | 148 mV |
| 50 mV | ±175 mV* | 350 mV | ±12 mV | 338 mV | _____ | 362 mV |
| 100 mv | ±350 mV | 700 mV | ±24 mV | 676 mV | _____ | 724 mV |
| 200 mv | ±700 mV | 1.40 V | ±50 mV | 1.35 V | _____ | 1.45 V |
| 500 mV | ±1.75 V | 3.50 V | ±120 mV | 3.38 V | _____ | 3.62 V |
| 1 V | ±3.5 V | 7.00 V | ±240 mV | 6.76 V | _____ | 7.24 V |
| 2 V | ±7.0 V | 14.0 V | ±500 mV | 13.5 V | _____ | 14.5 V |
| 5 V | ±17.5 V | 35.0 V | ±1.2 V | 33.8 V | _____ | 36.2 V |
| 10 V | ±35.0 V | 70.0 V | ±2.4 V | 67.6 V | _____ | 72.4 V |
| 20 V | ±70.0 V | 140 V | ±5 V | 135 V | _____ | 145 V |

# For a supply without a polarity switch (like the HP 6115A) polarity is changed by switching the probe tip and ground of the 10:1 probe.

*Confirm these settings with the Voltmeter.

7. Connect the probe to the output of the supply (probe tip to +, ground clip to –).

8. Press ***Chan 1*** and ENTER the SCOPE V/div range with the ENTRY keypad.

9. Set the supply to the positive value of the voltage in the INPUT VOLTAGE - SETTINGS column of the table and press CLEAR DISPLAY to restart averaging.

10. Press ***Delta V*** and ***MARKER 2 POSITION***. When ***#Avgs = 64***, use the knob and cursors to set the marker over the trace. With the marker at best overlap the most overlap color will show.

11. Set the supply to the negative value of the voltage in the INPUT VOLTAGE - SETTINGS column of the table (or reverse the probe connections, probe tip to – and ground clip to +) and press CLEAR DISPLAY.

12. Press ***MARKER 1 POSITION*** and when ***#Avgs = 64***, overlap the trace with the marker.

13. Read and record the ΔV= in the lower right corner of the screen. It should fall within the specified limits in the table above.

14. If you are using a supply with no polarity switch reverse the probe connection (probe tip to +, ground to −).

15. Repeat steps 7 through 14 with the rest of the V/div ranges in the table.

16. Press ***Chan 1, Display (OFF), Chan 2***, and ***Display (ON).***

17. Repeat steps 2 through 15 substituting ***Chan 2*** for ***Chan 1.***

18. Set the dc power supply to 0.0V.

19. If you are doing the Offset Accuracy tests next, skip this step. If probe attenuation factors (step 3) were entered, set them back to 1.000 to avoid improper results in further tests. Press ***more, Utility, Probe Menu***; then, for both channels, ***CHAN X PROBE ATTN*** and in the ENTRY keys, 1 and ENTER.

---

## 3-13. OFFSET ACCURACY

**Description:**

This test verifies Offset accuracy. Resolution is a part of the specification for this test.

**Specification:**

Repetitive 6-bit with averaging and with a 10:1 probe at the input.

±1.5% of setting ± 0.2 div* ±Resolution[0.4% of full scale (8 div.)]

* ±0.4 div from 50-90 mV/div and ±1 div below 50 mV/div

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| DC Supply * | ±300 mV and ±9.5 V<br>1.0 mV resolution | HP 6115A |
| DC Voltmeter | Better than ±0.1% accuracy | HP 3468A |
| Oscilloscope Probe | 10:1 1MΩ | HP 10431A/033A/017A |

* The voltage source used for these tests could be any stable supply with the parameters shown above. You may use the offset of a signal generator or a dc calibration standard that meets the specifications. The HP 6115A is recommended because it is used in another test.

**Procedure:**

1. Perform a one-key powerup* to set instrument to default conditions, then set the following additional parameters.

*Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Chan 1,2 | Display | Chan 1 ON/Chan 2 OFF |
| Timebase | TIME/DIV | 2 us/div |
| Display | NUMBER OF AVERAGES<br>Screen<br>Graticule | 64<br>Single<br>Grid |

2. Connect the 10:1 probe to CHAN 1 of the HP 54111D.

3. If you are using an HP 10431A or 10033A probe skip this step. Press ***more, Utility, Probe Menu***, and ***CHAN 1 PROBE ATTN***, then ENTER 10.

4. If you just did the Vertical Accuracy tests skip this step. Calibrate the HP 54111D to the 10:1 probe being used for the test. Press ***Utility, Cal Menu, Probe Tip Cal, Calibrate Probe Tip CHAN 1***, and ***Continue***. When calibration is done, press ***Exit, more, Chan 1***, and ***VOLTS/DIV***.

5. Use the following table for steps 6 through 13.

| SUPPLY VOLTAGE | TOLERANCE | MEASUREMENT LIMITS MAX | | MIN |
|---|---|---|---|---|
| 0.00 V | ±24 mV | -24 mV | _____ | 24 mV |
| 300 mV | ±28 mV | 272 mV | _____ | 328 mV |
| -300 mV | ±28 mV | -272 mV | _____ | -328 mV |
| -9.50 V | ±170 mV | -9.33 V | _____ | -9.67 V |
| 9.50 V | ±170 mV | 9.33 V | _____ | 9.67 V |

6. Connect the probe ground clip to the probe tip.

7. Press ***VOLTS/DIV*** and ENTER 100 mV.

8. Press ***OFFSET*** and use the arrow keys to set the trace exactly to center screen when ***#Avgs = 64***. The ***Offset*** reading should be within the specification for 0.00 V in the table. Record the reading.

9. Set the supply to 0.00 V then connect the voltmeter and probe to the output of the supply (probe tip to + and ground clip to –).

10. Set the supply voltage and scope offset to the next value in the table. It is easiest to enter the offset value directly, using the key pad.

11. Adjust the offset using the knob and arrow keys until the trace is at center screen when ***#Avgs = 64***.

12. The ***Offset*** = value should be within the limits given in the table. Record the reading.

13. Repeat steps 10 through 12 with the other values in the above table. If using a supply with no polarity switch, for negative voltages reverse the probe tip and ground at the supply.

14. Remove the probe from the power supply and connect the probe ground to the probe tip.

15. Use the following table for steps 16 through 23. Follow steps 17 through 21 for a pass/fail test, or steps 17a through 20a for a precise test. The pass/fail test is faster. If a range is close to the specification for a pass/fail test, make a precise test of that range.

| V/div | PASS/FAIL LIMITS(div) | PRECISE LIMITS | | |
|---|---|---|---|---|
| 10 mV | ±1.0 | -10.4 mV | _____ | +10.4 mV |
| 20 mV | ±1.0 | -20.6 mV | _____ | +20.6 mV |
| 50 mV | ±0.4 | -22 mV | _____ | +22 mV |
| 100 mV | tested in step 4 | | | |
| 200 mV | ±0.2 | -46 mV | _____ | +46 mV |
| 500 mV | ±0.2 | -120 mV | _____ | +120 mV |
| 1 V | ±0.2 | -230 mV | _____ | +230 mV |
| 2 V | ±0.2 | -460 mV | _____ | +460 mV |
| 5 V | ±0.2 | -1.2 V | _____ | +1.2 V |
| 10 V | ±0.2 | -2.3 V | _____ | +2.3 V |
| 20 V | ±0.2 | -4.6 V | _____ | +4.6 V |

**NOTE**

Note that the minor division marks on the display are at 0.25 division increments and the specifications in the PASS/FAIL column of the table are 1.0, 0.4, and 0.2 divisions.

16. Press ***VOLTS/DIV*** and ENTER 10 mV.

PASS/FAIL TEST

17. Press ***OFFSET*** and ENTER 0 V.

18. Check the distance of the trace from the center horizontal axis. It should be within the DIVISIONS limits shown in the table above when ***#Avgs = 64***.

19. If trace is within limits in step 18, record the range as passing. If it appears to be outside the limits, make a precise test of this range (steps 17a and 18a at right), then continue with step 20.

20. Repeat steps 18 and 19 for each V/div range in the table.

21. After checking all ranges go to step 22.

PRECISE TEST

17a. Press ***OFFSET*** and use the cursor keys to set the trace to exactly center screen when ***#Avgs = 64***.

18a. Check that the Offset reading is within the specification in the LIMITS - VOLTAGE column. Record the reading and set offset to 0.0 V.

19a. Repeat steps 17a and 18a for each V/div range in the table. If if your doing a precise test of all ranges it is not necessary to set the offset to 0.00 V (step 18a) after each range check.

20a. After checking all ranges go to step 22.

22. Press ***Chan 1***, ***Display (Off)***, ***Chan 2***, and ***Display (On)***.

23. Repeat steps 2 through 21 (or 20a) for channel 2, substituting Chan 2 for Chan 1.

24. If probe attenuation factors (step 3) were entered, set them back to 1.000 to avoid improper results in further tests. Press ***more***, ***Utility***, ***Probe Menu***; then for both channels ***CHAN X PROBE ATTN*** and in the ENTRY keys, 1 and ENTER.

## 3-14. BANDWIDTH

**Description:**

This test checks the repetitive and real-time bandwidths of the HP 54111D.

**Specification:***

| | Real-time | Repetitive* |
|---|---|---|
| DC Coupled | 0 to 250 MHz | 0 to 500 MHz |
| AC Coupled *** | 10 Hz to 250 MHz | 10 Hz to 500 MHz |

* Upper bandwidth limit at input sensitivities below 5 mV/div is 150 MHz.

** Repetitive bandwidth at sweep speeds 10 us/div and slower not specified.

*** Not tested.

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Signal Generator | 100 KHz to 500 MHz<br>-22 to +12 dBm | HP 8656B |
| Power Meter/Sensor | 100 KHz to 500 MHz<br>-28 dBm to +8 dBm | HP 436A/8482A |
| Power splitter<br>Attenuator Type (N) | Outputs differ by <0.15dB<br>10 dB 100 kHz to 150 MHz | HP 11667A<br>HP 8491B |
| Cable<br>Adapter | Type N(m) 24 inch<br>N(m) to BNC(m) | HP 11500B<br>HP 1250-0082 |

**Procedure:**

1. Zero and calibrate the power meter using the Power Reference on the meter and the REF Cal Factor on the power sensor.

2. Connect the equipment as shown in the following diagram.

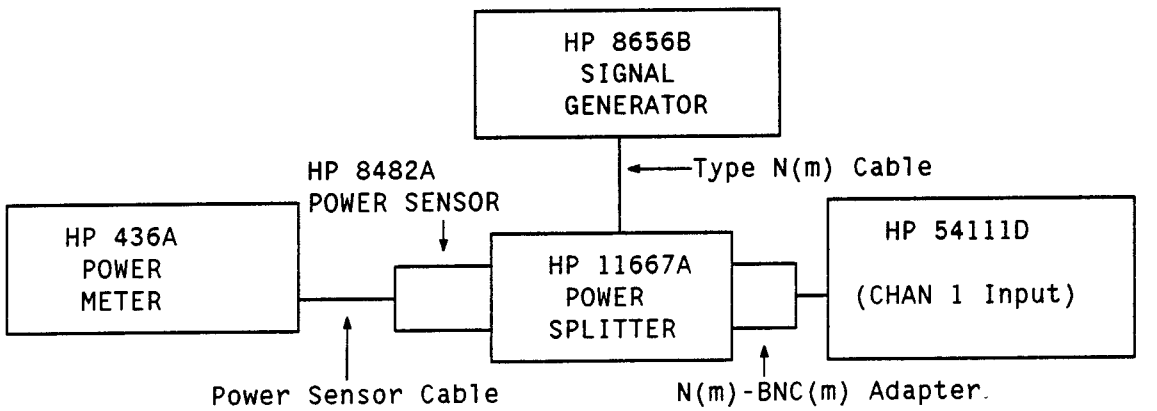



*Figure 3-1. Bandwidth Test Connections.*

3. Perform a one-key powerup* to set instrument to default conditions, then set the following additional parameters in the order given.
   *Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Display | Disp Mode<br>Resol'n<br>Screen | Real Time<br>6 bits<br>Single |
| Chan 1,2 | Display<br>VOLTS/DIV<br>Input Impedance | Chan 1 ON/Chan 2 OFF<br>200 mvolts/div<br>50Ω |
| Timebase | TIME/DIV<br>Auto/Trgd Sweep | 2 us/div<br>Trgd |
| Delta V | V Markers<br>Preset Levels | ON<br>0-100% |

REAL-TIME BANDWIDTH

4. Set up the 8656B signal generator with a 100 kHz signal at +12 dBm. The HP 54111D should display two cycles of a sinewave signal.

5. Set power meter Cal Factor % to 100 kHz value from the cal chart on the probe, press dB[REF] to set a 0 dB reference.

6. Press ***Delta V*** and ***Auto Level Set***. The V Markers will mark the top and bottom of the signal. Note the ΔV= value at the bottom of the screen.

7. Change the frequency of the signal generator to 250 MHz.

8. Change the power meter Cal Factor to the 250 MHz % value from cal chart.

9. Press ***Timebase*** and ***TIME/DIV*** and ENTER 2 ns.

10. Press ***Delta V***. Increment the signal generator output amplitude while occasionally pressing ***Auto Level Set*** on the HP 54111D.

11. When the ΔV= value (bottom of screen) is the same as noted in step 6, read and record the level on the power meter. It should be less than ±2.85 dB from the zero reference.

REPETITIVE BANDWIDTH

12. Set signal generator frequency to 100 kHz and amplitude to +12 dBm.

13. Set power meter Cal Factor % to 100 kHz value from the cal chart on the probe, press dB[REF] to set a 0 dB reference.

14. Press ***Timebase*** and ***TIME/DIV*** and ENTER 2 μsec.

15. Press ***Display*** then ***Disp Mode*** to obtain Repetitive mode. Confirm ***Averaging On*** and press ***Number of Averages***, and ENTER 8.

16. Press ***Delta V*** and ***Auto Level Set***. The V Markers will mark the top and bottom of the signal. Note the ΔV= value shown at the bottom-right of the display.

17. Press ***Timebase*** and ***TIME/DIV*** and ENTER 1 nsec.

18. Change the signal generator frequency to 500 MHz and set the power meter Cal Factor % to the 500 MHz value on the probe cal chart.

19. Press ***Delta V***. Do not press ***Auto Level Set*** yet.

20. Slowly adjust the signal generator output amplitude while occasionally pressing CLEAR DISPLAY. When the signal seems to be averaging so the peaks are near the markers, press CLEAR DISPLAY, allow ***#Avgs*** = to reach 8, then press ***Auto Level Set***.

21. When you can press CLEAR DISPLAY, wait for ***Avgs=8***, then press ***Auto Level Set***, and get the same ΔV= value as noted in step 16, read and record the level on the power meter. It should be less than ±2.85 dB from the zero reference.

22. Connect the signal to the CHAN 2 input and change the following menus on the HP 54111D.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Chan 1 | Display | OFF |
| Chan 2 | Display | ON |
| Timebase | TIME/DIV | 2.00 us/div |
| Trigger | Trig Src | Chan 2 |
| Display | Disp Mode | Real Time |

23. Repeat steps 4 through 21 for channel 2.

BANDWIDTH BELOW 5 MV/DIV (repetitive)

24. Insert the 10 dB attenuator between the power splitter and the channel input of the instrument being tested.

25. Set signal generator frequency to 100 kHz at -12 dBm.

26. Set power meter Cal Factor % to 100 kHz value from the cal chart on the probe, press dB[REF] to set a 0 dB reference.

27. Press ***Timebase*** and ***TIME/DIV*** and ENTER 2 μsec.

28. On the HP 54111D, press ***Chan 2*** and ***VOLTS/DIV*** and ENTER 4 mV. The display should show two cycles of signal.

29. Press ***Delta V*** and ***Auto Level Set***. The V Markers will mark the top and bottom of the signal. Note the ΔV= value shown at the bottom-right of the display.

30. Press ***Timebase*** and ***TIME/DIV*** and ENTER 5 ns.

31. Change the signal generator frequency to 150 MHz and set the power meter Cal Factor % to the 150 MHz value on the probe cal chart.

32. Press ***Delta V***. Do not press ***Auto Level Set*** yet.

33. Slowly adjust the signal generator output amplitude while occasionally pressing CLEAR DISPLAY. When the signal seems to be averaging so the peaks are near the markers, press CLEAR DISPLAY, allow ***#Avgs*** = to reach 8, then press ***Auto Level Set***.

34. When you can press CLEAR DISPLAY, wait for ***Avgs=8***, then press ***Auto Level Set***, and get the same ΔV= value as noted in step 28, read and record the level on the power meter. It should be less than ±2.85 dB from the zero reference. Record the reading.

35. Press ***Chan 2, Display (Off)***, then ***Chan 1, Display (On)***.

36. Connect the signal to the CHAN 1 input and repeat steps 25 to 34 for channel 1, substituting Chan 1 for Chan 2.

## 3-15. TRANSITION TIME

**Description:**

Transition Time (Risetime) is tested by applying a fast risetime pulse to the HP 54111D and making an automatic risetime measurement.

This test could be dropped for an abbreviated performance test (see paragraph 3-5).

**Specification:**

The repetitive transition time is ≤700 ps.

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Pulse Generator | ≈70 ps risetime | Tektronix TYPE 284 |
| Cable | BNC(m) | HP 10503A |
| Adapter | GR-to-BNC(f) | HP 1250-0850 |

**Procedure:**

1. Connect the pulse generator PULSE OUTPUT to the CHAN 1 input.
2. Press ***Chan 1*** and confirm or set ***Input Impedance*** to 50Ω. Press AUTOSCALE to establish the display, then continue setup of the 54111D as follows:

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Timebase | TIME/DIV | 500 ps/div |
| Display | Disp Mode<br>Averaging<br>NUMBER OF AVERAGES | Repetitive<br>ON<br>8 |

3. Set the ***V/div*** and ***OFFSET*** to provide the maximum waveform without clipping the signal. You can set ***VOLTS/DIV*** and ***OFFSET*** with the ENTRY keys with 1 mV resolution.
4. Press ***more*** in the menu keys, then ***Measure*** and ***more*** in the function keys.
5. When ***#Avgs*** = is greater than 1, press ***Rise Time***. If you need a more accurate measurement wait for the number of averages to reach 8 then press ***Rise Time*** again.
6. Risetime should read ≤700 ps. Record the reading.
7. Repeat steps 1 through 6 for channel 2, substituting Chan 2 for Chan 1.

## 3-16. TIME INTERVAL ACCURACY

**Description:**

Time interval accuracy is checked by correlating delay settings with a frequency-stable signal.

Usually performance tests are done before any adjustments. The HP 54111D however has self-calibration that may have been done by the user. Two of these self-cals, Timebase Cal and Channel Skew, will affect the time interval accuracy of the instrument.

- Though Timebase Cal is not usually a user calibration, particularly when traceability is being maintained, it can be easily done by the user. If the user has done Timebase Cal, the time interval measurement traceability is affected and the instrument may fail the Time Interval Accuracy tests.

- The Channel Skew self-cal is a user calibration. The user calibrates the time reference between channels to suit his measurements. If the Channel-to-Channel Accuracy part of the Time Interval Accuracy tests is done without adjusting Channel Skew, the test will be done with the users calibration and the instrument may fail.

If it is necessary to return the instrument to traceable calibration by doing Timebase Cal and Channel Skew before the Time Interval Accuracy tests, see the appropriate sections in the adjustment procedures, section 4 of this service manual. Timebase Cal and Channel Skew can be done without affecting any other performance tests or adjustments.

**Specification:**

Accuracy of the time interval measurements is to be within the following limits:

| | Repetitive | Real-time |
|---|---|---|
| Single Channel | ±100 ps ±0.03% of reading | ±300 ps ±0.03% of reading |
| Dual Channel | ±200 ps ±0.03% of reading | ±600 ps ±0.03% of reading |

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Signal Generator | 1.0 MHz and 500 MHz time base ±0.003% | HP 8656B-check time base to be within ±0.003% |
| Power splitter | 1.0 to 500 MHz frequency range | HP 11667A |
| Cable | Type N(m) 24 inch | HP 11500B |
| Adapter (2) | N(m) to BNC(f) | HP 1250-0780 |
| Cables (2) | BNC(m) 9 inch(equal length) | HP 10502A |

**Procedure:**

1. Read and record the Timebase Freq Cal figure. Press ***more, Utility, Cal Menu, Timebase Cal***, and ***Timebase Freq Cal***.

2. Record the ***Current value*** in the Performance Test Record; on the first page where it can be easily found, and at the Time Interval Accuracy section where the results of these tests are recorded. Continue with the rest of the tests.

3. Set the signal generator frequency to 500 MHz and amplitude to 120 mV.

4. Connect the signal generator to the input of the power splitter with the type N cable. With the N-to-BNC adapters and the BNC-to-BNC cables, connect the outputs of the power splitter to the channel inputs.

5. Perform a one-key powerup* to set instrument to default conditions.
   *Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

6. Press ***Chan 1*** and ***Chan 2*** menu keys in turn and set the ***Input Impedance*** on both to 50Ω.

7. Press AUTOSCALE to establish the display, then set or confirm the following parameters in the order given.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Display | NUMBER OF AVERAGES<br>Screen | 4<br>Single |
| Chan 1,2 | Display<br>VOLTS/DIV<br>OFFSET | Chan 1 ON/Chan 2 OFF<br>20 mvolts/div<br>0.00 V |
| Timebase | TIME/DIV | 500 ps/div |
| Trigger<br>Chan 1,2 | Trig Src<br>TRIGGER LEVEL<br>Slope | Chan 1<br>0.00 V (both channels)<br>Pos (both channels) |

SHORT DELAY - TIMEBASE ACCURACY

8. Press ***Timebase*** and ***DELAY***. Adjust the delay so the positive edge of the signal crosses the horizontal graticule exactly at center screen. Note the Delay reading on the display.

9. Add the delay reading from step 8 to each of the Set Delay values in the following table and use the entry keys to ENTER each sum as a Delay value. For each entry, check that the positive edge of the signal crosses the horizontal graticule within the "Divisions" specification from center screen. Record a pass or fail for each delay setting.

If you want to measure the error, for each Set Delay value ENTER the delay sum as above, then use the cursors or knob to make the positive edge cross the horizontal graticule exactly at center screen. Record the difference between the instrument reading and the delay sum. Each should be within the "Time" specification.

| Set Delay | Specification Divisions | Time | Record |
|---|---|---|---|
| 2 ns | ±0.2 | ±102 ps | _____ |
| 4 ns | ±0.2 | ±102 ps | _____ |
| 6 ns | ±0.2 | ±102 ps | _____ |
| 8 ns | ±0.2 | ±104 ps | _____ |
| 10 ns | ±0.2 | ±104 ps | _____ |
| 100 ns | ±0.26 | ±130 ps | _____ |
| 334 ns | ±0.4 | ±200 ps | _____ |

**NOTE.** 0.2 div = one minor graticule division

CHANNEL TO CHANNEL ACCURACY

10. Further set up the HP 54111D with the following parameters.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Chan 2 | Display | ON |
| Timebase | Delay | 0.00 s |
| Delta V | V Markers | ON |
| | MARKER 1 POSITION | Chan 1 0.00 V |
| | MARKER 2 POSITION | Chan 2 0.00 V |
| | Preset Levels | 50-50% |
| Delta t | T Markers | ON |
| | START ON XXX | POS |
| | EDGE X | 1 |
| | STOP ON XXX | POS |
| | EDGE X | 1 |

11. At ***Delta t*** press ***Edge Find***. The $\Delta t$= reading, in the lower-right corner of the display, should be 0.00 ±200 ps. Record the reading.

LONG DELAY - TIMEBASE ACCURACY

12. Change the frequency of the signal generator to 1 MHz.

13. Press AUTOSCALE to establish the signal.

14. Change the HP 54111D with the following parameters.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Chan 2 | Display | OFF |
| Timebase | TIME/DIV | 200 ns/div |
| Display | Screen | Single |
| Delta V | V Markers | OFF |
| Delta t | T Markers | OFF |

15. Press ***Trigger*** and ***Trigger Level***. Adjust the trigger so that the positive edge of the signal crosses exactly at center screen.

16. Press ***Timebase*** and ***Delay***. Enter 1 ms. The positive edge of the signal should cross within 1.5 divisions of center screen. Use the knob or cursors to set the positive slope at center screen. The delay should read 1.0 ms ±300 ns. Record the reading.

## 3-17. TRIGGER SENSITIVITY

**Description:**

Channel and external trigger paths are checked for sensitivity vs. frequency. The displayed signal must remain triggered for various frequency and input amplitude combinations.

**Specification:**

| | Channels 1 and 2 | Triggers 3 and 4 |
|---|---|---|
| dc to 200 MHz | 0.1 of full scale * | 15 mV p-p |
| 200MHz to 500 MHz | 0.2 of full scale * | 45 mV p-p |

* 5 mV/div to 5 V/div

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Signal Generator | 200 MHZ and 500 MHz<br><-33 dBm to >-13 dBm | HP 8656B |
| Power Meter/Sensor | 200 - 500 MHz<br>measure approximately -22 dBm | HP 436A/8482A |
| Power splitter | 200 to 500 Mhz frequency range | HP 11667A |
| Attenuator | 10 ±0.6 dB 200-500 MHz | HP 8491B |
| Cable | Type N(m) 24 inch | HP 11500B |
| Adapter | N(f) to BNC(m) | HP 1250-0077 |
| Adapters (2) | N(m) to BNC(f) | HP 1250-0780 |
| Cables (2) | BNC(m) 9 inch | HP 10502A |

**Procedure:**

CHAN 1, 2 TRIGGER TEST

1. With the Type N cable and N(f)-to-BNC(m) adapter, connect the signal generator to the CHAN 1 input.

2. Perform a one-key powerup* to set instrument to default conditions.
   *Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

3. Set the signal generator frequency for 200 MHz and amplitude to 9 mV rms.

4. Press ***Chan 1*** then ***Input Impedance*** to set 50Ω. Press AUTOSCALE to establish the display, then set or confirm the following parameters on the 54111D.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Chan 1 | VOLTS/DIV | 20 mvolts/div |
| Display | NUMBER OF AVERAGES | 8 |
| Delta V | V Markers<br>Preset Levels | ON<br>0-100% |

5. Press ***Trigger*** and ***Trigger Level***.

6. Reduce the output of the signal generator until ***Auto Triggering*** appears (top of display). Adjust ***Trigger Level*** as necessary to maintain triggering as long as possible. Increase output until stable triggering returns, indicated by no occurences of ***Auto Triggering*** in the display.

7. Press CLEAR DISPLAY. When ***#Avgs*** = becomes greater than 1, press ***Delta V*** and ***Auto Level Set***. Read and record ***ΔV***=. It should be less than 16 mV (0.1 of full scale or 0.8 div.). Waiting for the number of averages to become 8 will give a more accurate reading but 1 average will usually give an indication the test has passed.

8. Change the frequency of the signal generator to 500 MHz.

9. Press ***Trigger*** and ***Trigger Level***.

10. While optimizing triggering with the Trigger Level, increase the output of the signal generator until stable triggering returns, indicated by no occurences of ***Auto Triggering*** in the display.

11. Press CLEAR DISPLAY. When ***#Avgs*** = becomes greater than 1, press ***Delta V*** and ***Auto Level Set***. Read and record ***ΔV***=. It should be less than 32 mV (0.2 of full scale or 1.6 div.).

12. Connect the signal generator to the CHAN 2 input.

13. Repeat steps 3 through 11 for channel 2, substituting Chan 2 for Chan 1.

TRIG 3, 4 TRIGGER TEST

14. Connect the equipment as shown in the following diagram.

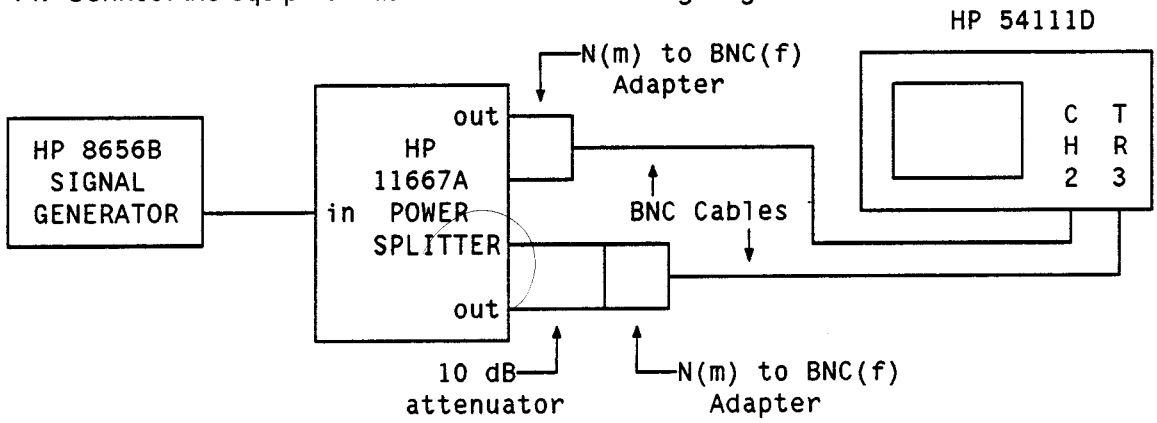



*Figure 3-2. Trigger Sensitivity Test Connections.*

15. Press ***Delta V*** and ***V Markers*** to shut them off and press ***Chan 2*** and ***VOLTS/DIV*** and ENTER 10 mV.

16. Zero and calibrate the power meter using the Power Reference on the meter and the REF Cal Factor on the power sensor.

17. Set the signal generator frequency to 200 MHz and output level to 50 mV rms.

18. Set the power meter Cal Factor % to the 200 MHz value from the chart on the probe.

19. Press ***Trigger*** and ***Trigger Src*** to select TRIG 3 and press the left arrow key to select ***HI SENS***.

20. Press ***INPUT Coupling*** and the left arrow key to select 50Ω.

21. Reduce the output of the signal generator until ***Auto Triggering*** appears in the display. Adjust ***Trigger Level*** as necessary to maintain triggering as long as possible. Increase output until stable triggering returns, indicated by no occurences of ***Auto Triggering*** in the display.

22. Disconnect the 10 dB attenuator at the power splitter and connect the power meter to this port of the splitter.

23. Read and record the power reading. It should be less than 5.62μW (15 mV p-p + 10 dB).

24. Set the signal generator to 500 MHz and set the power meter Cal Factor % to the 500 MHz value from the chart on the probe.

25. Disconnect the power meter and connect the TRIG 3 input to this port of the splitter with just the N to BNC adapter and BNC cable (no 10 dB attenuator).

26. Adjust ***Trigger Level*** to obtain ***Running*** in the display.

27. Reduce the output of the signal generator until ***Auto Triggering*** appears in the display. Adjust ***Trigger Level*** to maintain triggering as long as possible. Increase the output of the signal generator until stable triggering returns, indicated by no occurences of ***Auto Triggering*** in the display.

28. Disconnect the TRIG 3 input at the power splitter and connect the power meter.

29. Read and record the power reading. It should be less than 5.06 μW (45 mV p-p).

30. Disconnect the power meter and connect this splitter port through the 10 dB attenuator, N to BNC adapter, and BNC cable to the TRIG 4 input.

31. Repeat steps 17 through 29, substituting Trig 4 for Trig 3.

**NOTES**

*Table 3-2. Performance Test Record*

HEWLETT PACKARD

**HP 54111D**
**DIGITIZING OSCILLOSCOPE**

Tested by _____

Serial No. _____ Work Order No. _____

Recommended Calibration Interval - 1 Year/2000 hours Date _____

Recommended Next Calibration _____ Temperature _____

Timebase Freq. Cal - current value _____ Humidity _____

| TEST | LIMITS | | RESULTS | |
|---|---|---|---|---|
| 3-11 Calibrator Amplitude | | 0.792 to 0.808 V | _____ | |
| | RANGE | | CHAN 1 | CHAN 2 |
| 3-12 Measurement Accuracy | 10 mV | 66.0 mV to 74.0 mV | _____ | _____ |
| | 20 mV | 135 mV to 145 mV | _____ | _____ |
| | 50 mV | 338 mV to 362 mV | _____ | _____ |
| | 100 mV | 676 mV to 724 mV | _____ | _____ |
| | 200 mV | 1.35 V to 1.45 V | _____ | _____ |
| | 500 mV | 3.38 V to 3.62 V | _____ | _____ |
| | 1 V | 6.76 V to 7.24 V | _____ | _____ |
| | 2 V | 13.5 V to 14.5 V | _____ | _____ |
| | 5 V | 33.8 V to 36.2 V | _____ | _____ |
| | 10 V | 67.6 V to 72.4 V | _____ | _____ |
| | 20 V | 135 V to 145 V | _____ | _____ |
| | RANGE | | CHAN 1 | CHAN 2 |
| 3-13 Offset Accuracy | 100 mV | -24 mV to 24 mV | _____ | _____ |
| | | 272 mV to 328 mV | _____ | _____ |
| | | -272 mV to -328 mV | _____ | _____ |
| | | -9.33 V to -9.67 V | _____ | _____ |
| | | 9.33 V to 9.67 V | _____ | _____ |
| | 10 mV | ±1 div or ±10.4 mV | _____ | _____ |
| | 20 mV | ±1 div or ±20.6 mV | _____ | _____ |
| | 50 mV | ±0.4 div or ±22 mV | _____ | _____ |

*Table 3-2. Performance Test Record (con't.)*

| TEST | LIMITS | | | RESULTS | |
|---|---|---|---|---|---|
| 3-13 Vertical Offset Accuracy (con't.) | RANGE | | | CHAN 1 | CHAN 2 |
| | 200 mV | ±0.2 div or | ±46 mV | _____ | _____ |
| | 500 mV | ±0.2 div or | ±120 mV | _____ | _____ |
| | 1 V | ±0.2 div or | ±230 mV | _____ | _____ |
| | 2 V | ±0.2 div or | ±460 mV | _____ | _____ |
| | 5 V | ±0.2 div or | ±1.2 V | _____ | _____ |
| | 10 V | ±0.2 div or | ±2.3 V | _____ | _____ |
| | 20 V | ±0.2 div or | ±4.6 V | _____ | _____ |
| 3-14 Bandwidth | | | Down from reference | CHAN 1 | CHAN 2 |
| | Real Time | 250 MHz | <3 dB | _____ | _____ |
| | Repetitive | 500 MHz | <3 dB | _____ | _____ |
| | @ 4 mV/div | 150 MHz | <3 dB | _____ | _____ |
| 3-15 Transition Time | | | ≤700 ps | CHAN 1 _____ | CHAN 2 _____ |
| 3-16 Time Interval Accuracy | Timebase Freq Cal current value | | | _____ | |
| | Short Delay - Timebase Acc. | | | | |
| | 2 ns | ±0.2 div or | ±102 ps | _____ | |
| | 4 ns | ±0.2 div or | ±102 ps | _____ | |
| | 6 ns | ±0.2 div or | ±102 ps | _____ | |
| | 8 ns | ±0.2 div or | ±104 ps | _____ | |
| | 10 ns | ±0.2 div or | ±104 ps | _____ | |
| | 100 ns | ±0.26 div or | ±130 ps | _____ | |
| | 334 ns | ±0.4 div or | ±200 ps | _____ | |
| | Channel-to-Channel Accuracy | | | | |
| | | Δt = 0.00 | ±200 ps | _____ | |
| | Long Delay - Timebase Acc. | | | | |
| | | 1.0 ms | ±300 ns | _____ | |
| 3-17 Trigger Sensitivity | | Better than: | | CHAN 1 | CHAN 2 |
| | | full scale | or mV | | |
| | dc to 200 MHz | 0.1 div | 16 | _____ | _____ |
| | 200 to 500 MHz | 0.2 div | 32 | _____ | _____ |
| | | Better than: | | TRIG 3 | TRIG 4 |
| | | mV p-p | or μW | | |
| | dc to 200 MHz | 15 | 5.62 | _____ | _____ |
| | 200 to 500 MHz | 45 | 5.06 | _____ | _____ |

# SECTION 4
# ADJUSTMENTS

## 4-1. INTRODUCTION

This section describes the adjustments required to make the instrument meet published specifications. Included are adjustments to the power supplies, acquisition system and color display.

## 4-2. ADJUSTMENT REQUIREMENTS

Adjustments should be performed as warranted by the Calibration Procedure (see section 3), by requirements after repair, or requirements due to failure of a performance test (see section 3). Adjustments should not be performed only on the basis of an elapsed period of time.

**WARNING**

*Read the Safety Summary at the front of this manual before performing adjustment procedures. The apparatus should be disconnected from all voltage sources before it is opened for any adjustment, replacement, maintenance, or repair.*

## 4-3. TEST EQUIPMENT REQUIRED

Required test equipment is listed in Table 4-1 Recommended Test Equipment.

## 4-4. ACCESS TO ADJUSTMENTS

Most adjustments can be accessed by removing the instrument top cover. Remove the top-rear feet and then the top cover.

Power supply adjustments (not done during routine calibration) require the additional removal of the power supply cover (under the top cover).

Adjustment of the attenuators requires partial removal of the front panel and attenuators. For this reason, and because misadjustment is unlikely, attenuator adjustment is not recommended during routine calibration.

One adjustment in the Trigger Qualifier Adjustment section is near the center of the assembly and is hard to reach from the top. It may be necessary to remove the handle, bottom-right rear foot, and right side cover in addition to the top cover.

Most adjustments of the Color CRT Module are under the clear plastic covers and are accessable from the sides or bottom of the instrument. However, several are at the rear of the module and require removal of the module from the instrument and operation of the module while outside the instrument. They also require a special tool as noted in the procedure.

## 4-5. ONE-KEY POWER UP

A one-key power up is a procedure where any one key is held depressed when the power is turned on. The key is held depressed until the power up cycle completes; "Powerup Self Test Passed!" (or Failed) is displayed. This is done to preset or reset the instrument to default conditions and prevent previous setups from interfering with the next test. It also simplifies the instrument setup procedure.

The one-key powerup is a part of many procedures and should be performed like any other procedural step.

## 4-6. ADJUSTMENTS REQUIRED AFTER REPLACEMENTS

Some adjustments may be necessary after replacement of an assembly, though it may not be necessary to make all adjustments. The table below gives the adjustments necessary after replacement of a major assembly.

*Table 4-1. Adjustments Required After Assembly Replacement.*

| ADJUSTMENT / ASSEMBLY | Power Supplies | Clk & Gap | Gain & Flat | Calibrator Amplitude | Atten-uator | Complete* Self-Cal | DC Gain | Trigger Qualifier |
|---|---|---|---|---|---|---|---|---|
| **Timebase** | | X | | X | | X | | |
| **Microprocessor** | | | | | | X | | |
| **Input/Output** | | | | | | X | | |
| **ADC Control** | | | | | | X | RCO | |
| **ADC** | | RCO | RCO | | | Skip Probe Tip and Trigger cals | | |
| **Trigger** | | | | | | Skew only | | |
| **Trigger Qual.** | | | | | | Skew only | | X |
| **Channel Atten.** | | | | | Adj. at factory | X | RCO | |
| **Trigger Atten.** | | | | | | X | | |
| **Power Supplies** | Adjust supply replaced | | | | | | | |

**NOTE:** No adjustments are required after replacing the **Color Display** assembly and **Color CRT Module**.

**KEY:** RCO Replaced Channel Only. Perform this adjustment only on the channel in which the assembly was replaced.

X This adjustment must be performed.

* Self-calibration includes: ADC Reference Cal, Vertical Cal, Probe Tip Cal, Trigger Cal, and Timebase Cal (Timebase Frequency Cal and Channel Skew). See the appropriate procedures in this section.

## 4-7. POWER SUPPLY ADJUSTMENTS

**Description:**

This procedure is provided to adjust the power supply voltages in cases where either of the power supplies has been inadvertently mis-adjusted or repairs have been made.

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| DC Voltmeter | Better than 0.3% accuracy | HP 3468A |

**Analog Power Supply Procedure:**

**NOTE**

*First, check for the presence of A12R61. It is located at the top front corner of the Analog Supply assembly. If there is no potentiometer there, the instrument is a later version and no adjustment is required; continue with the Digital Supply procedure.*

This procedure adjusts the supply voltage to the fans.

The locations of the test points are marked on the power supply cover as well as the PC board. A12R61 is the only adjustment on the analog power supply.

**NOTE**

*The instrument **MUST** be stabilized at ambient temperature with power off (front panel power switch to STBY) before this adjustment is made. This voltage will rise as internal temperature increases.*

1. Connect positive voltmeter lead to the FAN test point.
2. Connect negative voltmeter lead to the -18 V test point.
3. Turn on instrument power (from STBY to ON).
4. Before instrument warms up, adjust A12R61 (the only pot on the board) for a voltmeter reading of 9.5 Vdc ±0.1 V.

**Digital Power Supply Procedure:**

The locations of test points are marked on the power supply cover as well as the assemblies. A13R56 is the only adjustment on the digital power supply. First, the voltage is measured to be sure that it requires adjustment.

1. Allow the instrument to stabilize (power on) for one to two minutes.
2. Connect positive voltmeter lead to the +5 V test point (actual voltage = +5.1 V).
3. Connect negative voltmeter lead to the −5 V test point (actual voltage = −5.3 V).
4. The voltmeter should read 10.4 Vdc ±0.01 V. If the measurement is within specifications stop here, if not then continue.
5. Disconnect power cord and remove voltmeter leads.

**WARNING**

*Hazardous voltages capable of causing injury or death are present on the Primary Power Supply board (A11) when power is applied and for a period of time after power is removed from the instrument. To avoid this hazard, DO NOT remove the top power supply shield until the LED on the Primary Power Supply board (A11) is extinguished. This LED is visible through an inspection hole in the cover labeled "+300 V WHEN LAMP IS ON".*

6. When the +300 V LED is extinguished, remove the top power supply cover.
7. Reconnect voltmeter leads per steps 2 and 3 above.
8. Reconnect power cord and allow instrument to stabilize for 1 to 2 minutes.
9. Adjust A13R56 for a voltmeter reading of 10.4 Vdc ± 0.01 V.
10. Disconnect power cord and wait for the +300 V LED to extinguish before re-installing power supply shield.

## 4-8. CLOCK AND GAP ADJUSTMENTS

**Description:**

These adjustments provide a clean clock to the sampling circuitry. There are two procedures: adjustment and testing. Testing is only necessary in certain cases per the adjustment procedure.

If this adjustment is a result of an assembly replacement (table 4-A), after doing all required adjustments, refer to table 3-A for required performance tests. Otherwise, perform Measurement Accuracy, Offset Accuracy, Bandwidth, and Risetime tests (section 3) on channel adjusted.

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Power Meter/Sensor | 1 GHz bandwidth | HP 436A with 8482A |
| Lowpass Filter | >35 dB attenuation at 2 GHz<br>-3 dB point above 1.25 GHz | RLC F30-1500-N |
| Digital Voltmeter | ±0.5% | HP 3468A |
| Adapter *<br>Adapter *<br>Cable * | BNC (f) to N (f)<br>SMB (f) to BNC (f)<br>BNC (m) | HP 1250-1474<br>HP 1250-1236<br>HP 10503A |

* It is necessary to adapt the SMB (m) connector at J6 to the filter and power meter. Use whatever you have that can properly handle the 1 GHz signal. You can use cables and adapters that are part of the HP 54100 Family Support Kit.

**Adjustment Procedure:**

1. Zero the power meter. It isn't necessary to calibrate it since all measurements are relative.

**NOTE**

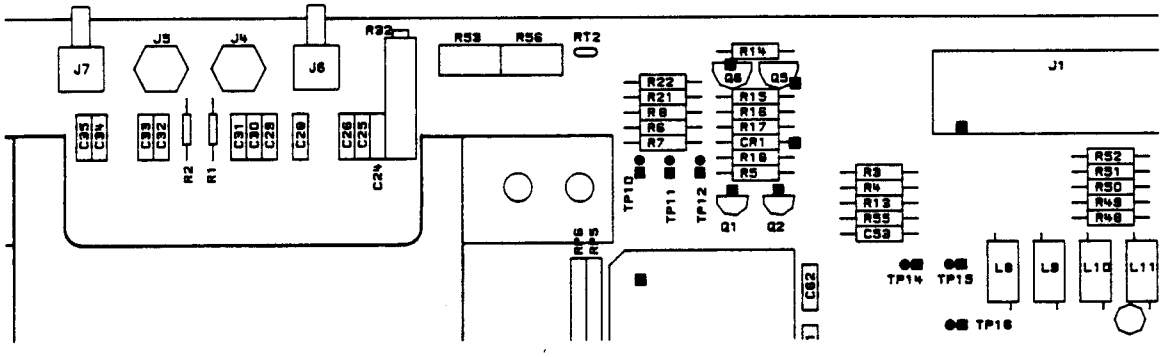
*The instrument must be warm during the following adjustments. Be sure that it is turned off only for short periods when installing or removing jumpers.*

**CAUTION**

*The instrument power must not be on while installing or removing jumpers. Improper shorting can cause hardware failure resulting in expensive repair.*

2. With POWER at STBY, use a jumper wire to short across R22 on the channel 1 ADC assembly (A5). See drawing below. If you have two jumpers, save time and short the resistor on channel 2 ADC (A7) also. Set POWER to ON.

   *View of center section of ADC assembly (A5, A7).*




3. Press ***more, Utility, Cal Menu, Timebase Cal***, and ***Timebase Frequency Cal***.

4. Locate the two FFCLK cables connecting J4 and J5 of the channel 1 ADC assembly (A5) and the Timebase assembly (A1). Disconnect them at the Timebase assembly.

5. Set the GAP (R56) adjustment on the channel 1 ADC assembly (A5) to mechanical center.

6. Connect the DVM to the J6 (T1) SMB connector on the channel 1 ADC assembly (A5).

7. Turn the CLK (R53) adjustment on the channel 1 ADC (A5) fully **counter-clockwise** and note the reading on the DVM (typically between −70 mV and −120 mV).

8. Turn the CLK adjustment fully **clockwise** and note the reading (near ground, 0 V).

9. Reconnect the FFCLK cables.

10. Set the CLK adjustment so the DVM reading is half way between the readings in steps 7 and 8. Set the voltage within 1.5 mV. If R53 reaches its limit before the voltage is reached, leave it at that point and be sure to do the Testing Procedure below after all adjustments are complete.

11. Disconnect the DVM from J6 and using the cable and adapters, connect the power meter with sensor, through the filter, to J6.

12. Set meter to dB[REF]

13. Adjust GAP (R56) for a maximum power reading. To maintain power meter resolution, it may be necessary to occasionally press dB[REF] on the meter.

    If there is more than one power peak set R56 to the highest.

    If R56 reaches its limit while the power reading is still increasing, set it at the limit and be sure to do the Testing Procedure below when all adjustments are complete.

14. If adjusting both channels, repeat steps 2 through 13 for channel 2 (A7), then go on to step 15. If channel 2 has R22 already shorted go back to step 4. If adjusting one channel, proceed directly to step 15.

CAUTION

*The instrument power must not be on while installing or removing jumpers. Improper shorting can cause hardware failure resulting in expensive repair.*

15. Set POWER to STBY and remove shorting clips. Set POWER to ON.

16. Press ***more, Utility, Cal Menu***, and ***ADC Reference Cal***.

17. If any adjustment is at its limit, continue with the testing procedure; if not, the adjustment procedure is complete.

**Testing Procedure:**

If either potentiometer for a channel was at its limit, it is necessary to check the results of the adjustment procedure on that channel. This is done by running some of the self test loops. For channel 1 (A5) run loops 27-31 and for channel 2 (A7) run loops 36-40. Use the following procedure to run the tests.

1. Press ***Exit Cal Menu*** then ***Test Menu***.

2. Press top function key (right edge of display) to select ***RUN FROM LOOP*** and ENTER test #.

3. Press ***RUN FROM LOOP*** to select ***REPEAT LOOP*** and ENTER 1000.

4. Press ***Start Test***.

5. When test has finished press ***Display Errors***. ***Failures*** = should be 0.

6. Press ***Exit Display*** and ***REPEAT LOOP*** to select ***RUN FROM LOOP*** and ENTER the next test number.

7. Press ***RUN FROM LOOP*** to select ***REPEAT LOOP*** then press ***Start Test***.

8. Repeat steps 5 through 7 until all necessary loops have been run.

9. After the necessary test loops have been run, press ***Exit Test Menu***. If any test loop fails, even once out of the 1000 repetitions, repeat the Clock and Gap adjustments for that channel and run the test loops again.

## 4-9. GAIN AND FLAT ADJUSTMENTS

**Description:**

There are two low frequency adjustments, GAIN and FLAT. These adjustments compensate for variations is the GaAs sampling circuitry and adjust the low frequency pulse response.

If this adjustment is a result of an assembly replacement (table 4-A), do all other required adjustments then refer to table 3-A for required performance tests. Otherwise, perform the Measurement Accuracy and Offset Accuracy tests (section 3) on channel adjusted.

**NOTE**

*Clock and Gap adjustments may influence the Gain and Flat adjustments. Be sure Clock and Gap adjustments are correct before starting this procedure.*

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Pulse Generator | ≤1% perturbation | Tektronix PG 506 |
| Cable | BNC (m) | HP 10503A |

**Procedure:**

1. Set up the pulse generator with the following parameters.

   ```
   Output select    - Fast rise
   Period           - 0.1 ms
     Var            - CCW
   Pulse Amplitude  - 0.2 V
   ```

2. Connect the positive FAST RISE OUTPUT (center BNC) of the pulse generator to the CHAN 1 input of the HP 54111D.

3. Press ***Chan 1*** and set or verify that the ***Input Impedance*** is 50Ω. Press AUTOSCALE to establish the signal. Set up the HP 54111D by setting or verifying the following parameters.

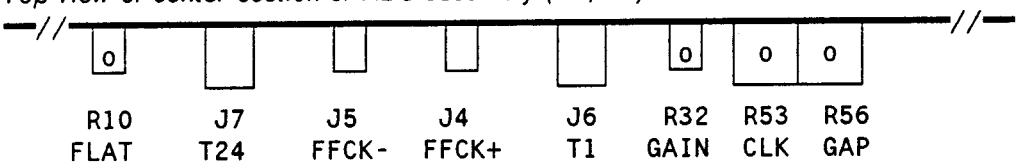
| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Chan 1,2 | VOLTS/DIV<br>OFFSET | 20 mvolts/div<br>as required |
| Timebase | TIME/DIV<br>DELAY<br>Delay Ref at<br>Auto/Trgd Sweep | 500 ns/div<br>2.2 us<br>Center<br>Trgd |
| Display | Disp Mode<br>Averaging<br>NUMBER OF AVERAGES<br>Screen<br>Graticule | Repetitive<br>ON<br>8<br>Single<br>Grid |

**NOTE**

*The signal will overdrive the input and the bottom will be clipped by the display. This will have no detrimental effect during these adjustments.*

4. Press ***Chan 1*** and ***OFFSET***. Adjust the ***OFFSET*** to put the top of the pulse 3 divisions above center screen. If it is slightly above or below a grid line, flatness deviations will be more readily apparent.

*Top view of center section of ADC assembly (A5, A7).*




5. On channel 1 ADC assembly (A5), adjust GAIN (R32) for start and end points of the pulse at the same level. To help visualize changes, use ***OFFSET*** to keep waveform close to the grid line.

6. Adjust FLAT (R10) for flattest pulse response.

7. Press ***more, Utility, Cal Menu, ADC Reference Cal,*** and ***more***.

8. Repeat the procedure, starting at step 5, until best flatness is achieved.

9. Repeat steps 2 through 8 for channel 2 (A7).

## 4-10. CALIBRATOR AMPLITUDE ADJUSTMENT

**Description:**

This procedure adjusts the amplitude of the front panel CAL signal. This signal is used to run calibration routines in the instrument.

The adjustment is done by forcing this signal high and adjusting it while measuring it with an accurate voltmeter. Forcing the signal high is done through a front panel setup. On earlier versions it is necessary to force the output high by using a shorting wire.

The performance test is not necessary after adjustment because the adjustment tolerance is tighter than the performance test tolerance.

If calibrator amplitude is adjusted as a result of replacement of an assembly (table 4-A), see table 3-A for appropriate performance tests. Otherwise, perform the Measurement Accuracy test in section 3 for both channels and the Probe Tip Calibration for TRIG 3 and TRIG 4 in this section.

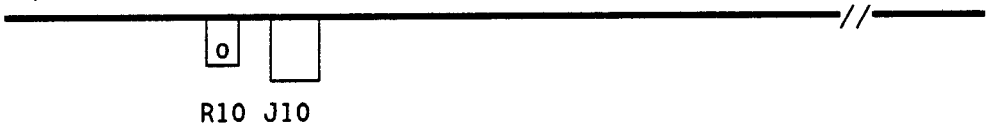
**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| DC Voltmeter | Better than 0.05% accuracy | HP 3468A |

**Procedure A:**

1. Connect the DC voltmeter + input to the front panel calibrator signal and – input to ground at the CHAN 1 input BNC.
2. In order, press ***more, Utility, Cal Menu, Timebase Cal*** and ***Timebase Freq Cal*** softkeys.
3. Read the voltmeter. If the measurement is about +0.8 Vdc the instrument is a later version and firmware controlled. Proceed to step 4. If the measurement is about +0.4 Vdc press ***Exit*** and continue with Procedure B on the next page.

*Top view of front of Timebase assembly (A1).*



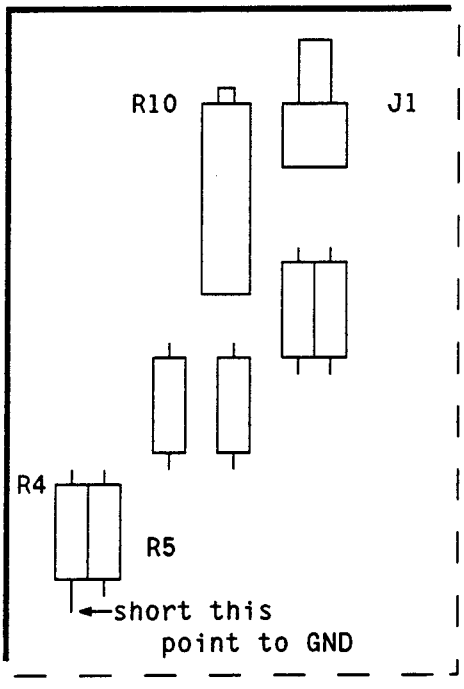

4. Adjust R10 as close as possible to +0.8000 V. It must be within ±0.002 Vdc. The adjustment is complete.
5. Press ***Exit***.

**Procedure B:**

The calibrator output must be forced high with a shorting wire so that it can be measured by a voltmeter.

1. Connect the DC voltmeter + input to the front panel calibrator signal and – input to ground at the CHAN 1 input BNC.
2. The drawing below shows the top front corner of the Timebase assembly A1. The Timebase assembly is the left-most assembly in the card cage. Note the position of R4, specifically the bottom end of this resistor.
3. Connect one end of a jumper wire to the body of J1 (see picture) on the Timebase. Connect a long grabber to the other end of the jumper.
4. Connect the grabber to the bottom end of R4.
5. Read the measurement on the voltmeter. Adjust R10 as close as possible to +0.8000 V. It must be within ±0.002 Vdc.
6. Disconnect the jumper and DVM.

*Top-front corner of Timebase assy. (A1)*



## 4-11. ATTENUATOR ADJUSTMENT

**Description:**

Channel 1 and channel 2 attenuator assemblies have two compensation adjustments, X10 and X100. These are set at the factory and normally do not require further adjustment.

Since replacement attenuators are adjusted at the factory no further adjustment should be necessary. For other adjustments necessary after attenuator replacement see table 4-A. For performance tests necessary after attenuator replacement see table 3-A. No performance tests are required after only adjusting an attenuator.

**NOTE**

***DO NOT PERFORM THESE ADJUSTMENTS DURING ROUTINE CALIBRATIONS.*** *It is necessary to partially disassemble the instrument for these adjustments.* ***DO NOT*** *perform these adjustments unless the Low Frequency Input Adjustments have been made and it is desirable to optimize flatness from 50 mV/div to 5 V/div.*

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Pulse Generator | ≤1% perturbation | Tektronix PG 506 |
| Cable | BNC (m) | HP 10503A |
| Adjustment tool | - - - - - - - - - - | HP 8710-1515 |

**Procedure:**

1. Without disconnecting any cabling, perform the Front Panel Removal procedure in Section 6A of this service manual. Set the front panel about 10 cm in front of its normal position.

2. With instrument in its normal operating position, remove the screw that fastens the rear of the attenuator to be adjusted. It can be reached from the top. *This screw is not captive.* ***DO NOT*** *allow it to fall into the instrument as it will be difficult to remove.*

3. Set the instrument on its left side and without disconnecting any cabling, slide the attenuator foreward, exposing its bottom. The adjustments are about 1 cm from the front edge. The X100 adjustment is in front and the X10 directly behind.

4. Set up the pulse generator with the following parameters.

```
Output select    - Fast rise
Period           - 0.1 ms
Pulse Amplitude - 500 mV
```

5. Connect the positive-going FAST RISE OUTPUT of the pulse generator to the input of the attenuator to be adjusted.

6. Press ***Chan X*** (whichever is appropriate) and ensure the ***Input Impedance*** is **50Ω**. Press AUTOSCALE to establish the signal. Continue setup of the HP 54111D by setting or verifying the following parameters.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Chan 1 or 2 | VOLTS/DIV | 50 mvolts/div |
| | OFFSET | 100 mV |
| Timebase | TIME/DIV | 5 us/div |
| | DELAY | 20 us |
| | Delay Ref at | Center |
| Display | Disp Mode | Repetitive |
| | Averaging | ON |
| | NUMBER OF AVERAGES | 8 |
| | Screen | Single |
| | Graticule | Grid |

7. Press ***Chan X*** (whichever is appropriate) and ***OFFSET*** and set the the offset to put the top of the pulse 3 divisions above center screen. If it is slightly above or below a grid line, flatness deviations will be more readily apparent.

8. Adjust X10 adjustment (rear capacitor) for best flatness.

9. Set VOLTS/DIV to 500 mV/div.

10. Set pulse generator amplitude to MAX or 5 V, whichever occurs first.

    **NOTE:** *If you are using a PG 506 the maximum output is about 1 V, so the pulse amplitude will be about 2 divisions. Do not set the HP 54111D for a lower range since 500 mV/div is the lowest that this adjustment covers.*

11. Press ***Chan X*** (whichever is appropriate) and ***OFFSET*** and set the the offset to put the top of the pulse 3 divisions above center screen. If it is slightly above or below a grid line, flatness deviations will be more readily apparent.

12. Adjust X100 adjustment (front capacitor) for best flatness.

13. If the other channel is being adjusted, repeat steps 2 through 12 for it.

14. After adjustments are complete reassemble instrument, reversing the disassembly procedure.

**CAUTION**

*Before installing front panel, be sure three-wire cables at front of attenuators do not become pinched and ensure that all probe sense rings around the input BNCs are inserted into their recesses properly.*

## 4-12. VERTICAL SELF-CALIBRATION

The self-calibration procedures calibrate circuitry with internal routines and adjustments. The following procedures are tailored to the Adjustments section and are therefore abbreviated.

If you are doing a complete adjustment procedure, follow the self-calibration completely and in the order given.

## 4-13. ADC Reference Calibration

Calibrates the ADC references.

**Procedure:**

1. Press ***more, Utility, Cal Menu***, and ***ADC Reference Cal***.
2. Continue with the next procedure, Vertical Calibration.

## 4-14. Vertical Calibration

Vertical calibration calibrates vertical sensitivity and offset.

**Procedure:**

1. Disconnect all inputs to CHAN 1 and CHAN 2.
2. Press the ***Vertical Cal*** and ***Continue***. When calibration is complete the instrument will return to the Cal Menu.
3. Continue with the next procedure, Probe Tip Cal.

## 4-15. Probe Tip Calibration

The Probe Tip Cal calibrates from the probe tip through the A/D converters.

**NOTE**

*This procedure is usually done for any channel or trigger that has had the probe changed. The vertical specifications for a channel or trigger are only met with the probe it was calibrated with.*

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Divider Probe | 10:1 1 MΩ | HP 10431A/033A/017A |

**Procedure:**

**NOTE**

*You may use the same probe for both channels and both triggers unless you need to calibrate each input to a specific probe (see note on previous page).*

1. Press ***Probe Tip Cal*** and ***Calibrate Probe Tip CHAN 1***. Follow the instructions on the display.
2. When the calibration for CHAN 1 is done calibrate CHAN 2, TRIG 3, and TRIG 4.
3. Press ***Exit*** then continue with the next procedure, DC Gain Adjustment.

---

## 4-16. DC GAIN ADJUSTMENT

This adjusts the DC gain to match the high frequency gain.

If DC Gain adjustment is a result of an assembly replacement (table 4-A), see table 3-A for necessary performance tests. Otherwise, perform the Measurement Accuracy and Offset Accuracy tests on the channel adjusted.

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| DC Supply | +780 to +820 mV<br>.1 mV resolution | HP 6115A |
| DC Voltmeter | Better than 0.1% accuracy | HP 3468A |
| Oscilloscope Probe | 10:1 | HP 10033A or 10017A |

**Procedure:**

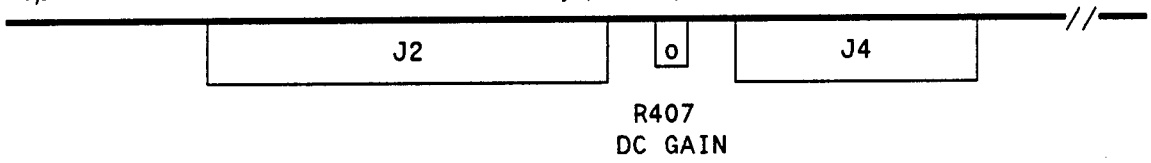
1. Perform a one-key powerup* to set the instrument to default conditions.
   *Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.
2. Connect the 10:1 probe to the CHAN 1 input. If you are using an HP 10033A probe, skip the next step.
3. Enter probe attenuation factors. Press ***more, Utility, Probe Menu***, then for both channels; ***CHAN X PROBE ATTN*** and in the ENTRY keys, 10 and ENTER.

4. Set the following additional parameters in the order given.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Display | NUMBER OF AVERAGES<br>Screen | 16<br>Single |
| Chan 1,2 | Display<br>VOLTS/DIV | Chan 1 ON, Chan 2 OFF<br>10 mvolts/div |
| Timebase | TIME/DIV | 5 us/div |
| Delta V | V Markers<br>Preset Levels | ON<br>50-50% |

5. Short probe tip to probe ground clip.
6. Press ***Auto Level Set*** and record the ***V(1)***= reading in the lower left corner of the display.
7. Add +800 mV to the reading in step 6.
8. Press ***Chan 1*** and ***OFFSET*** and set offset to the result from step 7.
9. Use the voltmeter to set the power supply to +800 mV ±1 mV.
10. Connect the probe to the output of the supply (probe tip to + and ground to –).

*Top view of front end of ADC Control assembly (A4, A6).*




11. On Chan 1 ADC Control assembly (A4), adjust DC GAIN (R407) to set the trace at center screen.
12. Disconnect the probe from the power supply and CHAN 1 input and connect it to the CHAN 2 input.
13. Press ***Chan 1***, ***Display (Off)***, ***Chan 2***, ***Display (On)***, and ***VOLTS/DIV***; then in the ENTRY keys, 10 and mV.
14. Press ***Delta V*** and repeat steps 5 to 11, substituting Chan 2 for Chan 1.
15. Perform a one-key powerup to return the instrument to default conditions.
    *Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

## 4-17. TRIGGER CALIBRATION

Trigger Cal calibrates trigger levels and trigger sensitivity (hysteresis).

**Procedure:**

1. Press ***Trigger Cal*** and follow the instructions on the display. It could take several minutes for the CHAN 1 and CHAN 2 trigger to calibrate. The arrow will move across the display, showing that the calibration is proceeding.

2. When CHAN 1 and CHAN 2 have calibrated the display will give further instructions. Follow the instructions to calibrate TRIG 3 and TRIG 4.

3. When calibration of the triggers is complete, the instrument will return to the Cal Menu.

## 4-18. TIMEBASE CALIBRATION

Timebase Calibration consists of Timebase Frequency Calibration and Channel Skew Alignment.

## 4-19. Timebase Frequency Calibration

The Timebase Frequency Calibration provides an error correction to compensate for a timebase frequency that is different from nominal. It improves the accuracy of time-interval measurements.

If the timebase frequency resulting from this procedure is recorded in the permanent file for this instrument it can be re-entered if the cal factors are inadvertently lost. Nominal is 50.05 MHz

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Frequency Counter * | 51 MHz and 50 mV sensitivity<br>5 digit resolution | HP 5384A |
| Cable | BNC (m) | HP 10503A |

* To maintain a traceable calibration (e.g., U.S. National Bureau of Standards), you must use a traceable frequency counter.

**Procedure:**

1. Press ***Timebase Cal*** and ***Timebase Freq Cal***.

2. **CAUTION!!** This adjustment affects timebase traceability. Press ***Exit*** to preserve present calibration.

3. Follow the instructions on the display.

4. Record the calibration factor in the Performance Test Record or other permanent record for this instrument.

5. Press ***Continue*** to enter the new frequency.

## 4-20. Channel Skew Alignment

Channel Skew time-aligns the signal that is input to CHAN 1, CHAN 2, TRIG 3, and TRIG 4.

Alignment occurs at the intersection of the input signal's rising edge and the HP 54111D's center horizontal graticule. For each input, this point becomes time-aligned with the zero-delay point.

Alignment includes time delays both internal and external to the HP 54111D, including probe or BNC cable length.

The primary importance in doing the Channel Skew procedure at this time is to set up the instrument for the Trigger Qualifier Adjustments. The setup is designed with that in mind.

For instruments with a serial prefix 2808A and later, the rear panel TIMEBASE CAL output can be used to do skew alignment. Use it instead of the pulse generator

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Pulse generator * | ≤500 kHz square wave<br>≤5 ns risetime | HP 8082A |
| Cable | BNC (m) (≈3 feet) | HP 10503A |
| Cables (2) | BNC (m) (9 inch, equal length) | HP 10502A |
| Adapter | BNC Tee (m)(f)(f) | 1250-0781 |
| Adapter (BNC Barrel) | BNC(f) to BNC(f) | 1250-0080 |

* The rear panel TIMEBASE CAL output can be used on instruments with a serial prefix of 2808A or later.

**Procedure:**

If the instrument to be calibrated has a serial prefix of 2808A or later, it is not necessary to set up the pulse generator when doing only the skew alignment. You can use the TIMEBASE CAL output as a signal, in the same manner as the pulse generator is used. The pulse generator will be used later however, when Trigger Qualifier adjustments are also done.

1. Skip this step if using the rear panel TIMEBASE CAL output. Set up the pulse generator with the following parameters. This setup is not necessary to do just channel skew. The same setup will be used in the Trigger Qualifier adjustments later.

   Input Mode - Norm
   Pulse - Normal
   Period - ≥2 us
   Width - Square Wave
   Leading edge - 1 ns
   Trailing edge - 1 ns
   Amplitude - +1.2 V
   Offset - -0.6 V

2. Connect the long BNC cable to the left pulse generator output (or HP 54111D TIMEBASE CAL output on prefix 2808A and later) and using the BNC barrel, connect the other end to the center of the BNC Tee.

3. Connect the two 9-inch BNC cables from the BNC Tee to the CHAN 1 and CHAN 2 inputs of the HP 54111D.

4. Press ***Chan 1*** and ***Chan 2*** in turn and set the input impedance on both channels to 50Ω.

5. Press AUTOSCALE to establish the display.

6. Change to or confirm the following on the HP 54111D.

| **MENU SELECT** | **FUNCTION SELECT** | **SETTING** when using: Pulse generator | Timebase Cal |
|---|---|---|---|
| Chan 1,2 | VOLTS/DIV | 200 mvolts/div | 30 mvolts/div |
| | OFFSET | 0.00V | -220 mV |
| Timebase | TIME/DIV | 500 ps | 500 ps |
| Trigger | Trigger Mode | Edge | Edge |
| Chan 1,2 | Trig Src | Chan 1 | Chan 1 |
| | TRIGGER LEVEL | 0.00 V | -220 mV |
| | Slope | Pos | Pos |
| Trig 3,4 | TRIGGER LEVEL | 0.00 V | -220 mV |
| | Slope | Pos | Pos |
| | INPUT | 50Ω | 50Ω |

7. Press ***more, Utility, Cal Menu, Timebase Cal***, and ***Channel Skew***.

8. Whichever signal source is being used, the requirements should be met. Press ***Continue*** to start the calibration.

9. Follow any prompts on the display during the procedure.

10. The instrument will align channel 1 and channel 2, then prompt you to move the CHAN 2 signal to TRIG 3 and press ***Continue***.

11. After aligning trigger 3 the display will prompt you to move the TRIG 3 signal to TRIG 4 and press ***Continue***.

12. When alignment is completed the instrument will return to the Cal Menu.

## 4-21. TRIGGER QUALIFIER ADJUSTMENTS

The Trigger Qualifier adjustments calibrate the time measurement functions of the HP 54111D. There are four adjustments. Some of them can be done individually, but some need to be preceeded by other adjustments. The figure below shows the proper sequence for each adjustment.

No performance tests are required after trigger qualifier adjustment.

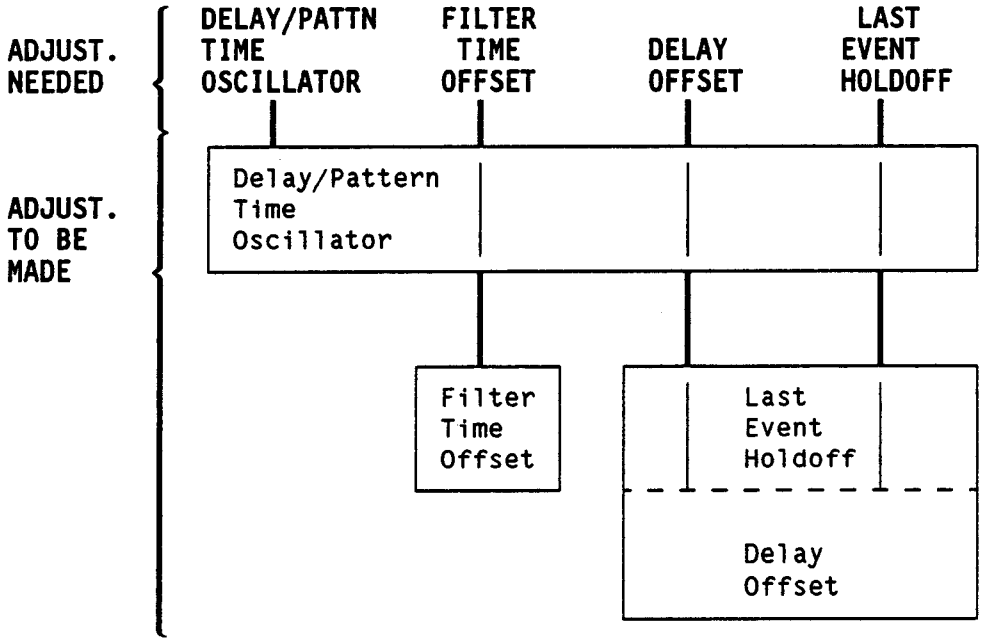



*Figure 4-1. Trigger Qualifier Adjustment Sequence.*

## 4-22. Delay/Pattern Time Oscillator Adjustment

**Description:**

This adjustment controls the frequency of the clock used to measure Trigger Qualifier time delays. It is not connected with the main timebase of the oscilloscope. The 100 MHz oscillator is adjusted for 50 MHz at J14.

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Frequency Counter | 50 MHz and 50 mV sensitivity<br>5 digit resolution | HP 5384A |
| Divider Probe | 10:1 1 MΩ | HP 10431A/033A/017A |

**Procedure:**

1. Set the following parameters on the HP 54111D. No other parameters are important.

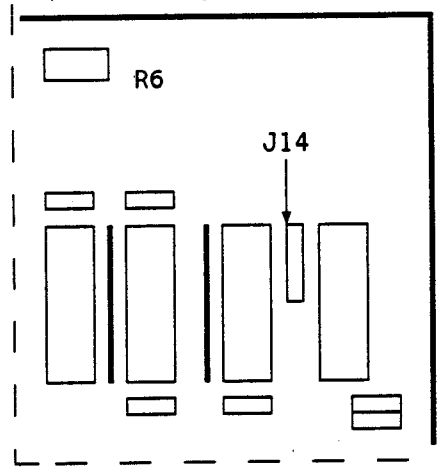
| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Timebase | Auto/Trgd Sweep | Trgd |
| Trigger | Trigger Mode<br>Trigger on Pattern<br>When<br>TIME | Pattern<br>X X X X<br>Present ><br>30.00 ns |

2. With the miniature divider probe, connect the frequency counter to J14 on the trigger qualifier assembly (A9). J14 is located at the rear of the board, about 4 cm down from the top edge (see views at right and below. It may be necessary to remove the side cover in order to see where to attach the probe and make the adjustment.

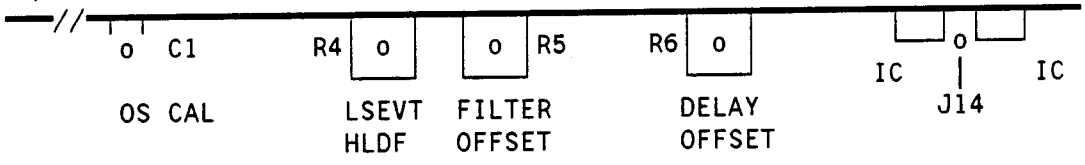
3. Adjust C1 (OS CAL) for a frequency of 50 MHz ±0.02 MHz. C1, the only adjustable capacitor, is near the center of the board, vertically and horizontally.

4. Disconnect the probe from J14.

*Top-rear of Trig Qual Assy*




*Top view of rear end of Trigger Qualifier Assembly (A9)*



## 4-23. Filter Time Offset Adjustment

**Description:**

Filter Offset is adjusted until oscilloscope will just trigger when a 20 ns pulse is applied.

**NOTE**

*Delay/Pattern Time Oscillator Adjustment must be performed before adjusting the Filter Time Offset.*

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Pulse generator | 300 ns period<br>20 ns adjustable pulse width<br>1 - 3 ns risetime and falltime | HP 8082A |
| BNC-to-BNC cable | | HP 10503A |

**Procedure:**

During this and the following procedures, the HP 54111D will use trigger levels and marker levels while making time interval measurements. The procedures are set up to use 0.0 V for both, so the signal generator is set up to swing the signal through 0 V.

If you are using a substitute pulse generator that cannot swing the 1.2 V p-p signal around 0 Volts, be sure to set the correct trigger level and V Markers in the HP 54111D setup (see footnote at bottom of table in step 2).

1. Set up the pulse generator with the following parameters.

```
Input Mode          - Norm
Pulse               - Normal
Period              - 300 ns
Delay               - 0 ns
Width               - 20.0 ns
Leading edge        - 1 ns
Trailing edge       - 1 ns
Amplitude           - +1.2 V
Offset              - -0.6 V
```

2. Perform a one-key powerup* to set instrument to default conditions, then set the following parameters in the order given. If you are doing the entire Trigger Qualifier adjustment procedure, store this setup by pressing SAVE SETUP and a numeric key. Use this SETUP as a starting point for the other procedures, or to recall the setup if the instrument power needs to be turned off.

*Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Display | Disp Mode | Repetitive |
| | NUMBER OF AVERAGES | 4 |
| | Screen | Single |
| Chan 1 | Display | ON |
| | VOLTS/DIV | 200 mvolts/div |
| | Input Impedance | 50Ω |
| Chan 2 | Display | OFF |
| | VOLTS/DIV | 100 mvolts/div |
| | OFFSET | -380 mvolts |
| | Input Impedance | 50Ω |
| Timebase | TIME/DIV | 5.00 ns/div |
| | Auto/Trgd Sweep | Trgd |
| Trigger | Trigger Mode | Edge |
| | Trig Src | Chan 1 |
| | TRIGGER LEVEL | 0.00 volts * (Chan 1,2) |
| | Slope | Neg (Chan 1,2) |
| Delta V | V Markers | ON |
| | MARKER 1 POSITION | Chan 1 0.00 volts * |
| | MARKER 2 POSITION | Chan 1 0.00 volts * |
| Delta t | T Markers | ON |
| | START ON POS EDGE | 1 |
| | STOP ON NEG EDGE | 1 |

* The Trigger Level and the V Marker references must be the same. If the pulse generator you are using cannot swing a signal around 0 Volts, set the trigger levels and V Markers to the same voltage, at the vertical center of the 1.2 V peak-to-peak signal.

3. Connect the pulse generator output to channel 1. The display should be pulse whose width is ≈20 ns with an amplitude of 6 divisions peak-to-peak. The trailing edge is at time zero (center screen).

4. Press ***Delta t*** and ***Edge Find*** to measure the width of the pulse. Adjust the pulse generator width to obtain a 20 ns ±100 ps pulsewidth measurement (Δt= 19.9 to 20.1 ns) each time ***Edge Find*** is pressed.

**NOTES**

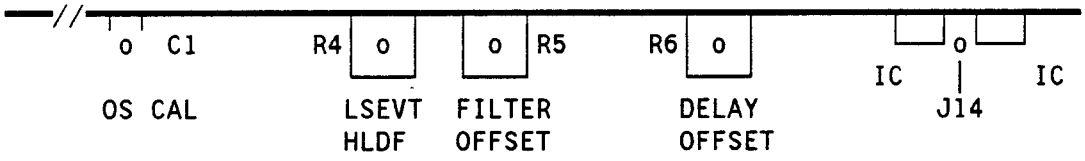
*Edge Find uses the V Markers as a reference to measure the pulse. The Measure functions use other parameters which may not be compatible with the adjustment being made.*

*If the increments of the pulse generator width control are too coarse, use the amplitude control as a fine adjustment of width. Increase amplitude to increase width and vice versa.*

5. Change the trigger parameters on the HP 54111D.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Trigger | Trigger Mode<br>Trig On Pattern<br>When<br>Time | Pattern<br>H X X X (default)<br>Present ><br>20.00 ns |

*Top view of rear end of Trigger Qualifier Assembly (A9)*




6. Adjust FILTER OFFSET (A9R5) until oscilloscope just triggers. Ideally, adjustment should be right on the threshold where the scope is intermittently triggering. This is indicated by slowed acquisition (the dots in the display are not replaced as quickly. Also the advisory "***Awaiting Trigger***" may occasionally appear.

7. If you are doing a complete adjustment procedure go directly to step 6 of the Last Event Holdoff Adjustment, the next procedure.

## 4-24. Last Event Holdoff and Delay Offset Adjustments

**Description:**

Last Event Holdoff is adjusted for a 4 ns delay after the second to the last event before main trigger is enabled. Delay Offset is adjusted so trigger will enable on a negative pulse edge which occurs 30 ns after a positive pulse edge.

**NOTE**

*The Last Event Holdoff and Delay Offset adjustments must be preceded by the Delay/Pattern Time Oscillator adjustment.*

**Equipment Required:**

| EQUIPMENT REQUIRED | CRITICAL SPECIFICATIONS | RECOMMENDED MODEL |
|---|---|---|
| Pulse generator | 20 ns adjustable pulse width<br>300 ns period<br>≤2 ns risetime and falltime | HP 8082A |
| Adapter | SMB (f) to BNC (f) | HP 1250-1236 |
| Cable | BNC (m) | HP 10503A |

* It is necessary to connect the SMB connector at J13 to the Channel 2 input BNC. Some cables and adapters are part of the HP 54110 Family Support Kit. Use whatever you have that can properly handle the 1 ns risetime pulse from J13.

**Procedure:**

LAST EVENT HOLDOFF ADJUSTMENT

1. Set up the pulse generator with the following parameters. If you are using a substitute pulse generator that cannot swing the 1.2 V p-p signal around a 0 Volt baseline, be sure to set the appropriate trigger level and V Markers in the HP 54111D set up.

```
Input Mode          - Normal
Pulse               - Normal
Period              - 300 ns
Delay               - 0 ns
Width               - 20.0 ns
Leading edge        - 1 ns
Trailing edge       - 1 ns
Amplitude           - +1.2 V
Offset              - -0.6 V
```

2. Perform a one-key powerup* to set instrument to default conditions, then set the following parameters in the order given. If you saved the setup from the Filter Time Offset, recall it.
*Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Display | Disp Mode | Repetitive |
| | NUMBER OF AVERAGES | 4 |
| | Screen | Single |
| Chan 1 | Display | ON |
| | VOLTS/DIV | 200 mvolts/div |
| | Input Impedance | 50Ω |
| Chan 2 | Display | OFF |
| | VOLTS/DIV | 100 mvolts/div |
| | OFFSET | -380 mvolts |
| | Input Impedance | 50Ω |
| Timebase | TIME/DIV | 5.00 ns/div |
| | Auto/Trgd Sweep | Trgd |
| Trigger | Trigger Mode | Edge |
| | Trig Src | Chan 1 |
| | TRIGGER LEVEL | 0.00 volts * (Chan 1,2) |
| | Slope | Neg (Chan 1,2) |
| Delta V | V Markers | ON |
| | MARKER 1 POSITION | Chan 1 0.00 volts * |
| | MARKER 2 POSITION | Chan 1 0.00 volts * |
| Delta t | T Markers | ON |
| | START ON POS EDGE | 1 |
| | STOP ON NEG EDGE | 1 |

* The Trigger Level and the V Marker references must be the same. If the pulse generator you are using cannot swing a signal around 0 Volts, set the trigger levels and V Markers to the same voltage, at the vertical center of the 1.2 V peak-to-peak signal.

3. Connect pulse generator output to channel 1. The display should be a ≈20 ns pulse with an amplitude of 6 divisions peak-to-peak. The trailing edge is at time zero (center screen).

4. Change the trigger parameters on the HP 54111D.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Trigger | Trigger Mode | Pattern |
| | Trig On Pattern | H X X X (default) |
| | When | Present > |
| | Time | 20.00 ns |

5. Adjust pulse generator pulse width using Width and Amplitude (fine adjust) until the oscilloscope is just on the threshold of triggering.

6. Set channel 1 to OFF, and channel 2 to ON.

7. Remove the short coaxial cable from J13 (DOUT, rear-most coax) on Trigger Qualifier assembly (A9). Connect the SMB-to-BNC cable between J13 and the input BNC of Chan 2. A pulse should be displayed.

8. Press ***Timebase***, and ***TIME/DIV*** and enter ***2.00 ns/div***. Press ***DELAY*** and use the knob to bring leading edge of the positive pulse on channel 2 to precisely center screen.

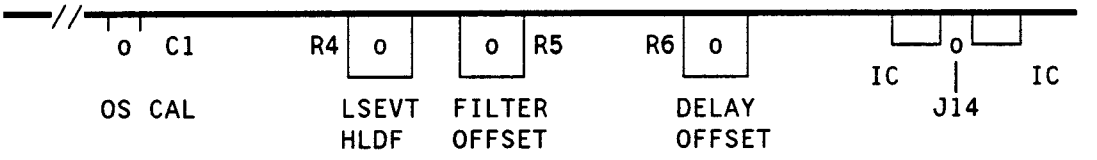
**NOTE**

*Do not change DELAY setting for the following steps.*

9. Change HP 54111D trigger to:

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Trigger | Trigger Mode<br>After XXX Edge<br>On<br>TRIGGER ON X EVENTS<br>Of XXX Edge<br>On | Events<br>Pos<br>Chan 1<br>2<br>Neg<br>Chan 1 |

*Top view of rear end of Trigger Qualifier Assembly (A9)*




10. Observe positive transition on channel 2 to the right of center screen and adjust LSEVT HLDF (A9R4) to position edge as close as possible to 2 divisions (4 ns) to the right of center screen. Edge must be between 1.5 and 4 divisions to the right of center screen.

11. Disconnect the SMB-to-BNC cable from J13 and reconnect the short SMB-to-SMB cable.

DELAY OFFSET ADJUSTMENT

**NOTE**

*Do not start this adjustment from this point. Delay/Pattern Time Oscillator Adjustment and Last Event Holdoff Adjustments must be performed before adjusting the Delay Offset (see figure 4-1).*

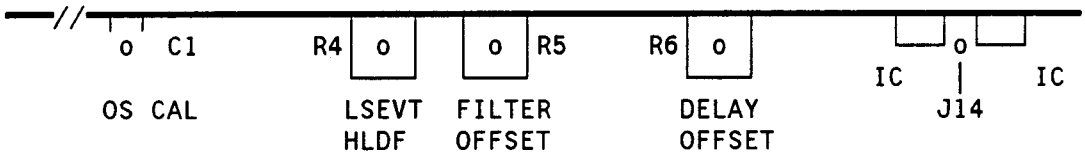
12. Change the following parameters on the pulse generator.

| | |
|---|---|
| Pulse | - Double |
| Delay | - 50.0 ns |
| Width | - 30.0 ns |

13. Change the following parameters on the HP 54111D.

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Chan 2 | Display | OFF |
| Timebase | TIME/DIV | 20 ns/div |
| Trigger | Trigger Mode | Edge |

*Top view of rear end of Trigger Qualifier Assembly (A9)*




14. Preset DELAY OFFSET (A9R6) fully clockwise.

15. The display should be two pulses approximately 30 ns wide, with an amplitude of 6 divisions peak-to-peak. The trailing edge of the first pulse is at time zero (center screen).

16. Press ***Delta t*** and ***Edge Find*** to measure the width of the first pulse. Adjust the pulse generator width to obtain a 30 ns ±100 ps pulsewidth measurement (Δt= 30.00 ns) every time ***Edge Find*** is pressed.

**NOTES**

*Edge Find uses the V Markers as a reference to measure the pulse. The Measure functions use other parameters which may not be compatible with the adjustment being made.*

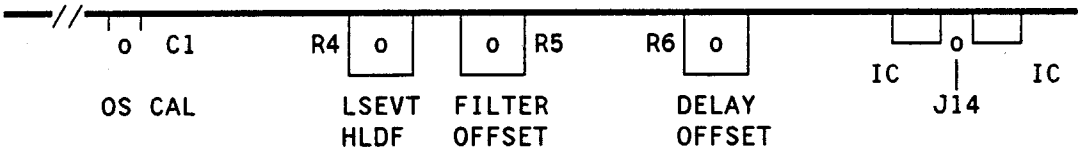
*If the increments of the pulse generator width control are too coarse, use the amplitude control as a fine adjustment of width. Increase amplitude to increase width and vice versa.*

17. Change HP 54111D trigger to:

| MENU SELECT | FUNCTION SELECT | SETTING |
|---|---|---|
| Trigger | Trigger Mode<br>After XXX Edge<br>On<br>DELAY XX.XX THEN<br>Trig On XXX Edge<br>On | Time<br>Pos<br>Chan 1<br>30 ns<br>Neg<br>Chan 1 |

18. The 54111D should be triggered on the negative edge of the second pulse.

*Top view of rear end of Trigger Qualifier Assembly (A9)*




19. Adjust DELAY OFFSET (A9R6) to the point where the scope switches from triggering on the second pulse to triggering on the first pulse. Ideally this would be the point where the scope is equally triggered on both negative edges as indicated by two pulses intermittently displayed either side of a stable pulse.

## 4-25. COLOR CRT MODULE ADJUSTMENTS

**NOTE**

***DO NOT PERFORM THESE ADJUSTMENTS DURING ROUTINE CALIBRATIONS.*** *The following procedures are provided only for the few extreme cases where either the earth's magnetic field or the user's environment cause an unusable display due to mis-convergence that cannot be corrected by degaussing the entire CRT screen.*

*It is recommended that these adjustments be performed only by qualified personnel who are familiar with color CRT convergence procedures.*

*Before starting adjustments, mark the position where potentiometers are set. This helps in returning adjustments to their original positions if it becomes necessary to restart the procedure.*

**Description:**

The Color CRT Module is adjusted to compensate for magnetic influences causing mis-convergence.

**NOTE**

***DO NOT*** *continue this procedure before first degaussing the CRT screen using the rear panel degaussing switch. In extreme cases of magnetism, it may be necessary to degauss the CRT using a conventional external television-type degaussing coil.* ***During any of the following adjustments, the CRT module must face west.***

**Equipment Required:**

Non-metallic Adjustment Tool ..... Sony Part Number 4-367-065-01
HP Part Number 8710-1355

**Procedure:**

**NOTE**

*The following adjustments are broken down in adjustment groups. The adjustment group sequence must be followed in order due to interaction and dependency. The adjustment group sequence is shown in the adjustment flow diagram on the next page. There will be cases where not all the adjustments groups will be used. For example, if the Geometry Adjustment Group corrects the problem, this will be the only group used.*

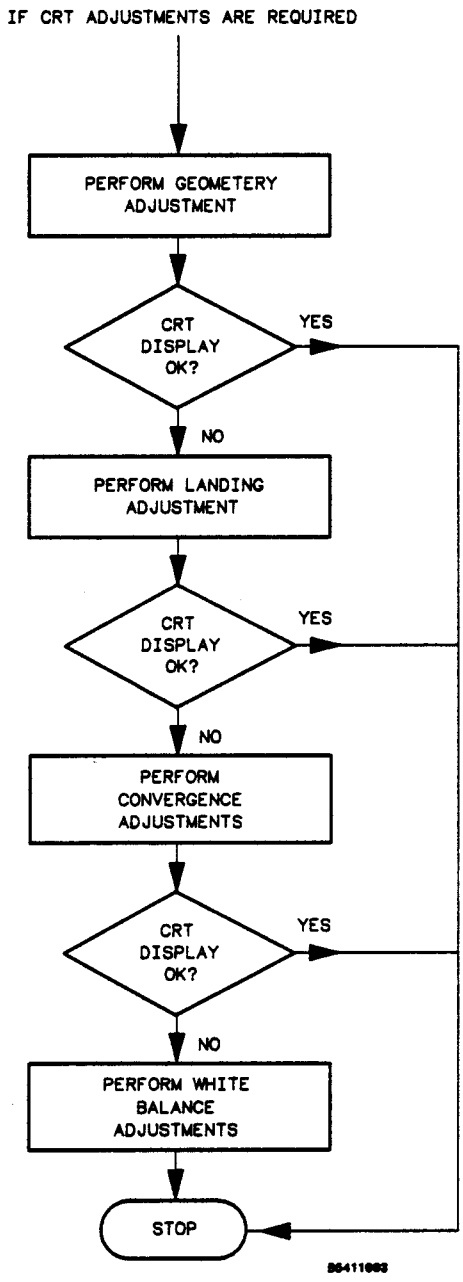



*Figure 4-2. CRT Module Adjustment Flow Diagram.*

**Geometry Adjustments**

1. Press ***Utility***, ***CRT Setup Menu***, then ***Pattern*** key as required until the white cross-hatch is displayed on CRT.

2. Preset front panel BACKGROUND control to mechanical center.

3. Preset front panel BRIGHTNESS control maximum clockwise.

4. Preset H.SUB SHIFT (RV006) and V.SUB SHIFT (RV008) located on the bottom PC board to mechanical center.

5. Using a flexible ruler, adjust H.SIZE (RV504) AND V.HEIGHT (RV502) located on the left hand side PC board so that the border of the cross-hatch pattern displayed on the CRT is 120.5 mm (4.74 in.) vertically and 161 mm (6.34 in.) horizontally.

6. Adjust V.CENT (RV510) AND H.CENT (RV503) located on the left hand side PC board to center pattern.

7. Adjust PIN AMP (RV506) located on the left hand side PC board to eliminate pincushion distortion in the vertical lines of the cross-hatch pattern as shown in the next figure.

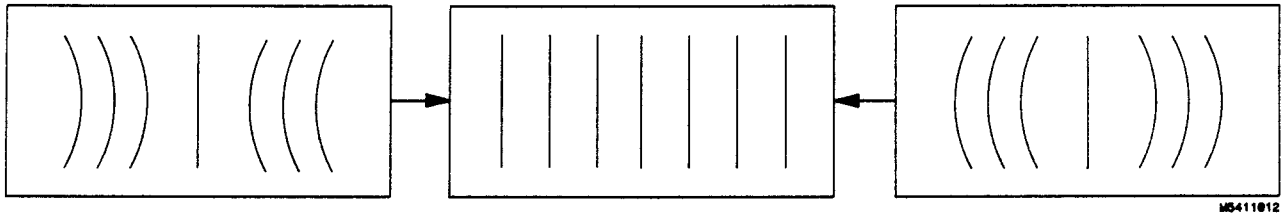



*Figure 4-3. PIN AMP Adjustment.*

8. Adjust PIN PHASE (RV505) located on the left side PC board to eliminate pin phase distortion in the vertical lines of the cross-hatch pattern as shown in the next figure.

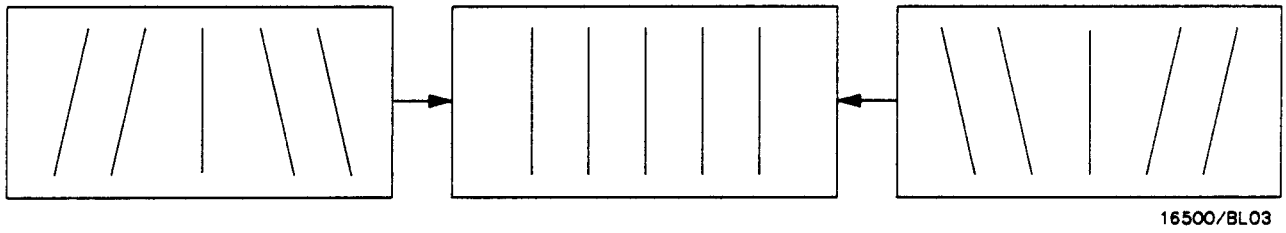



*Figure 4-4. PIN PHASE Adjustment.*

9. Adjust TOP PIN (RV511) located on the left hand side PC board so that top horizontal line is parallel with the center horizontal line.

10. Adjust BOTTOM PIN (RV512) located on the left hand side PC board so that bottom horizontal line is parallel with the center horizontal line.

**Focus, Landing, and Convergence Adjustment Preparation Procedures**

**NOTE**

*Note the original routing of all cabling for proper routing when module is re-installed in instrument. Then, re-route the cables from inside the module to the outside (left side) of module for reconnection to the power supply for adjustments.*

1. Remove Color CRT Module from the instrument (see section 6A of this service manual).
2. Reconnect instrument front panel and re-install front panel and CRT bezel (use two screws to temporarily hold front panel in place).
3. Loosen deflection yoke clamp screw.
4. With Color CRT Module placed to the left of mainframe, reconnect module.
5. Remove deflection yoke spacers by moving deflection yoke rearward and removing spacers.

**NOTE**

*The deflection yoke spacers are tapered rubber blocks located between front of yoke and rear of CRT funnel.*

6. Apply power and allow the instrument to thermally re-stabilize for 20 minutes.

**Focus Adjustment**

**NOTE**

*Geometry adjustments must be performed before making focus adjustment.*

1. In ***Utility*** menu, press ***CRT Setup Menu***, then press ***Pattern*** key as required until the white cross-hatch is displayed on CRT.
2. Adjust FOCUS (RV701) located on the rear PC board for best overall focus.

**Landing Adjustment**

1. In ***Utility*** menu, press ***CRT Setup Menu***, then press ***Color Purity*** key (fourth key from top) as required until a white raster is displayed on CRT.

2. Turn front panel BRIGHTNESS control fully clockwise.

3. Degauss entire CRT screen by pressing momentary DEGAUSSING switch located on the instrument rear panel.

**NOTE**

*In cases where the user's environment or shipping environment has caused high levels of magnetization to take place, it may be necessary to externally degauss the CRT using a conventional television type degaussing coil to completely degauss the CRT.*

4. Set purity magnet tabs to mechanical center (see next figure).

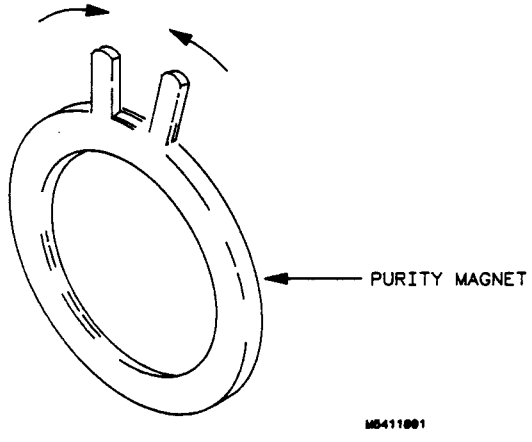



*Figure 4-5. Purity Magnet Centering.*

5. Press ***Color Purity*** key as required until a green raster is displayed on CRT.

6. Move deflection yoke rearward until left edge of raster turns red and right side of raster turns blue (see figure below).

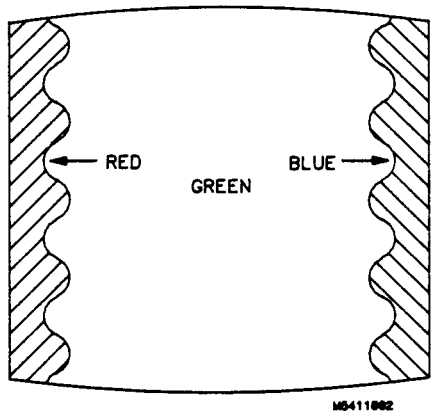



*Figure 4-6. Purity Magnet Adjustment Raster.*

7. Adjust purity magnets until green is in center of raster with red and blue bands evenly distributed on the sides (see above figure).

8. Move deflection yoke forward until entire raster is green.

**NOTE**

*Landing adjustment is easier if yoke is moved all the way forward and then moved back until raster is completely green.*

9. Using ***Color Purity*** key, replace green raster with red and then blue raster each time checking for proper landing adjustment (color purity of each).

10. If landing is not correct in step 9, repeat steps 6 through 9 for best compromise (see next figure).

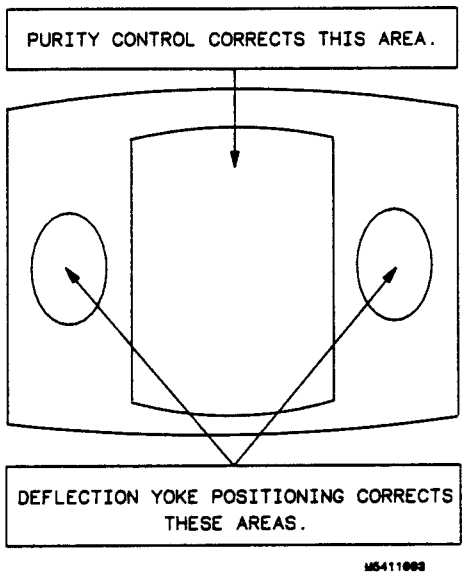



*Figure 4-7. Landing and Purity Adjustment Guide.*

11. If landing is not correct in step 10, readjust purity magnets for best landing of each color.

12. When landing adjustment is complete, tighten deflection yoke clamp screw just enough to keep yoke from moving. **DO NOT over tighten.**

**NOTE**

*While moving deflection yoke forward and rearward, rotate yoke as necessary to make vertical edges of raster parallel to the sides of the instrument frame.*

**Static Convergence**

1. Preset front panel BACKGROUND control to mechanical center.

2. Preset front panel BRIGHTNESS control maximum clockwise.

3. Temporarily disconnect power from instrument and remove PC board shield cover from rear of Color CRT Module by prying evenly on all four sides.

4. Re-apply power. Press ***more***, ***Utility***, and ***CRT Setup Menu*** keys. Press ***Pattern*** key as necessary to obtain the white cross-hatch pattern.

5. Check the four dots which are located around the center intersection of the cross-hatch pattern for coincidence of the blue, red and green dots. If the dots are not coincident, adjust H.STAT (RV703) located on the rear PC board to obtain horizontal coincidence and V.STAT (RV803) located on the bottom PC board to obtain vertical coincidence (see figure below).

**NOTE**

*Due to interaction, BEAM LANDING will need to be re-adjusted if either H.STAT or V.STAT adjustments are made. Once BEAM LANDING is re-adjusted, repeat step 5 above if necessary to obtain center screen coincidence of the dots.*

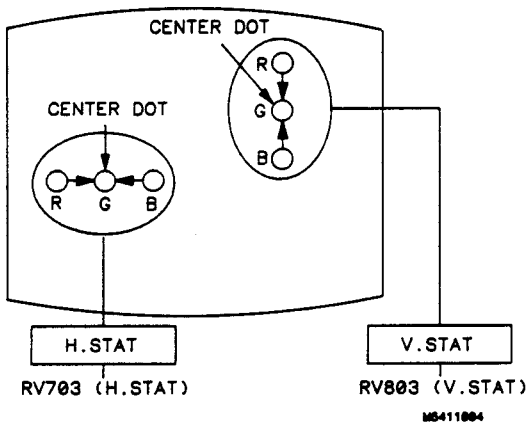



*Figure 4-8. Static Convergence.*

**Dynamic Convergence**

1. In ***Utility***, press ***CRT Setup Menu***, then press ***Pattern*** key (second key from top) as necessary to obtain the white cross-hatch pattern.

2. Adjust Y BOW (RV805) located on the bottom PC board to eliminate red, green and blue bowing at the top and bottom of the center vertical line (see next figure).

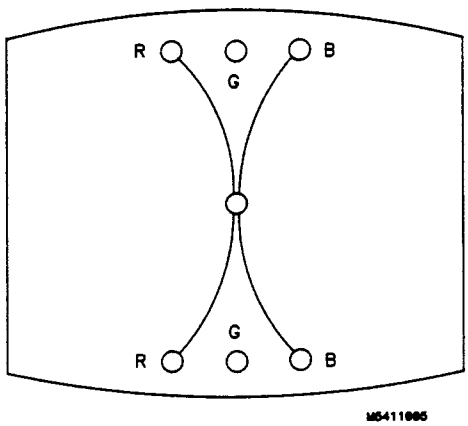



*Figure 4-9. Y BOW Adjustment.*

3. Adjust Y BOW CROSS (RV804) located on the bottom PC board to eliminate red green and blue orthogonal mis-alignment at the top and bottom of the center vertical line (see next figure).

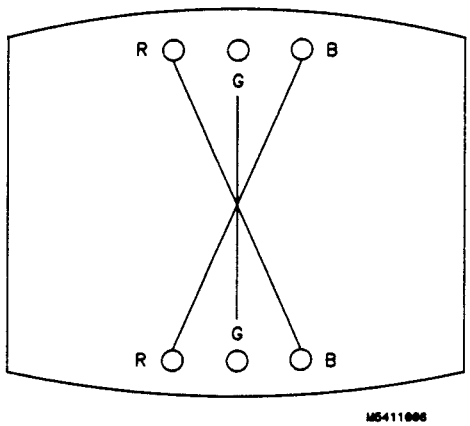



*Figure 4-10. Y BOW CROSS Adjustment.*

4. Adjust V.STAT TOP (RV801) and V.STAT BOTTOM (RV802) located on the bottom PC board to obtain coincidence of the red, blue and green at the intersection of the top and bottom horizontal lines with the center vertical line (see next two figures).

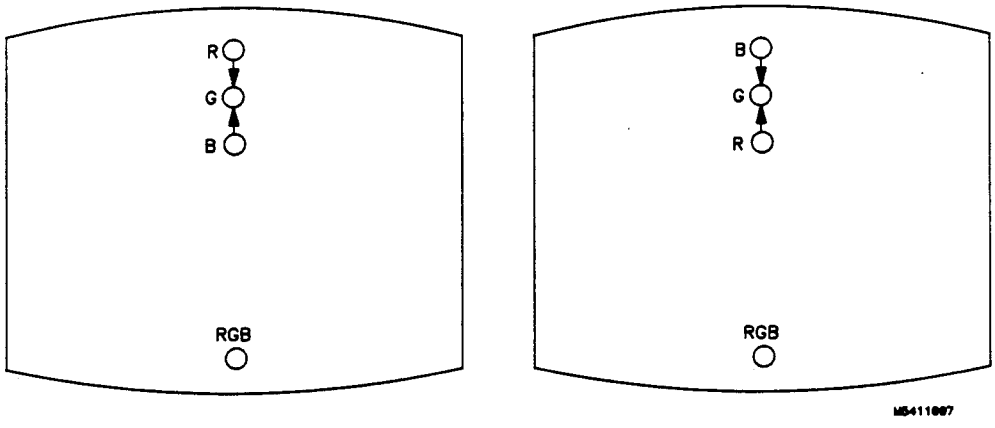



*Figure 4-11. V.STAT TOP Adjustment.*

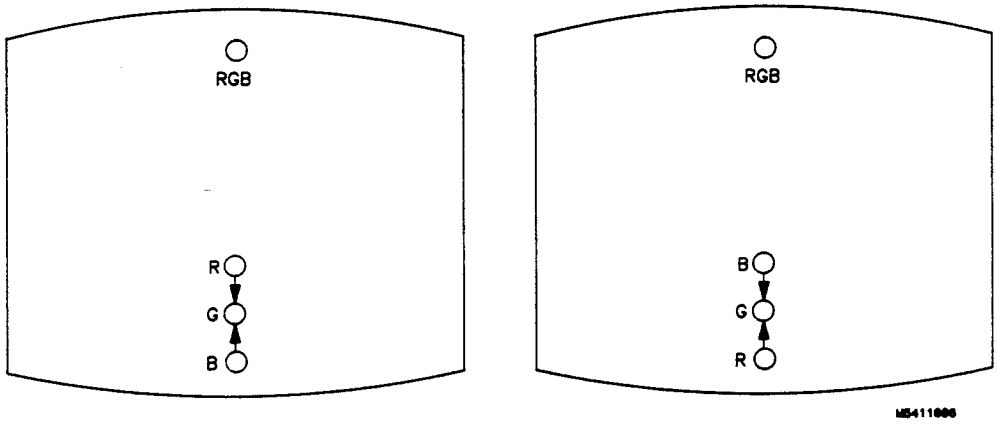



*Figure 4-12. V.STAT BOTTOM Adjustment.*

5. *Adjust H.AMP (RV807) located on the bottom PC board for equal amounts of mis-convergence at right and left sides of screen (see next figure).*

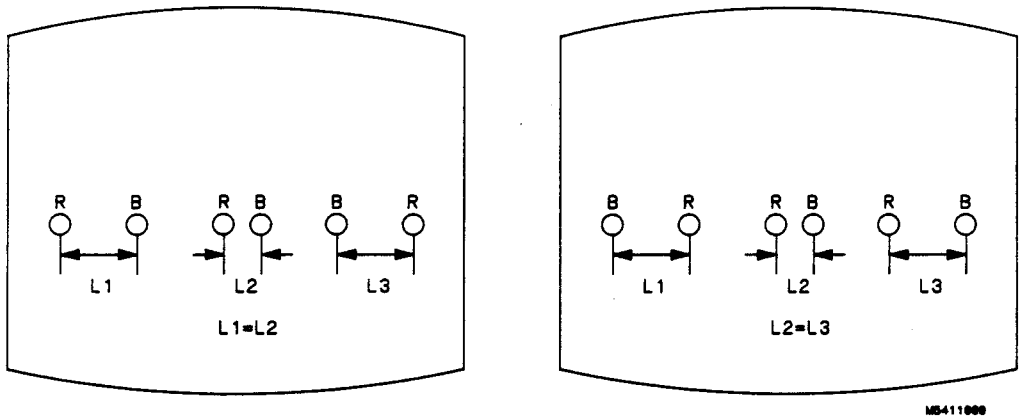



*Figure 4-13. H.AMP Adjustment.*

6. Adjust H.TILT (RV806) located on the bottom PC board for coincidence of red, green and blue at right and left sides of screen (see next figure).

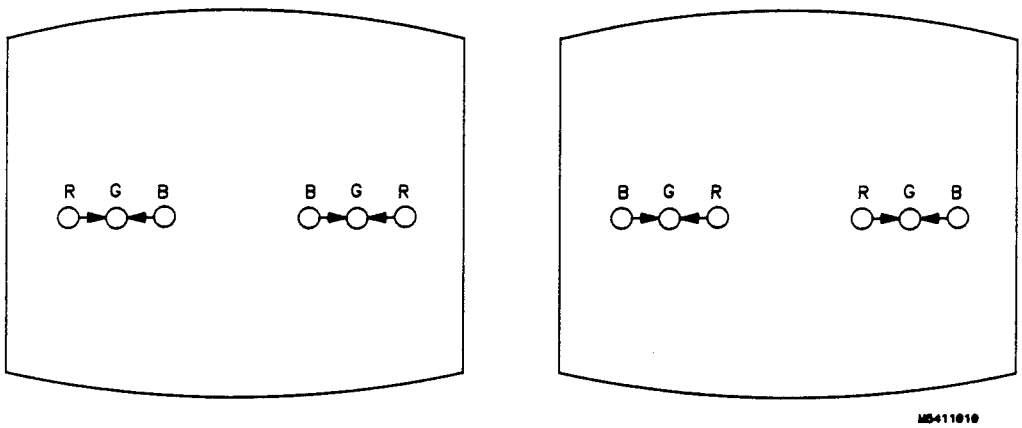



*Figure 4-14. H.TILT Adjustment.*

**White Balance**

1. In ***Utility***, press ***CRT Setup Menu***, then press ***Light Output*** key (third key from top) as necessary to obtain a blanked raster.

**NOTE**

*The completely blanked raster will contain the text for the function keys on the right side of the display, however, this will not affect the adjustment.*

2. Set front panel BACKGROUND and SUB BRT (RV901) located on the bottom PC board to mechanical center.

3. Set front panel BRIGHTNESS and SUB CONT (RV902) located on the bottom PC board to mechanical center.

4. Set G. DRIVE (RV921), B. DRIVE (RV931) and R. DRIVE (RV911) located on the bottom PC board to mechanical center.

5. Set G. BKG (RV721), B. BKG (RV731) and R. BKG (RV711) located on the rear PC board fully counterclockwise (CCW).

6. Adjust the SCREEN (RV702) located on the rear PC board until either red, green or blue raster just starts to become visible. Note which color becomes visible first and do not adjust the background control (BKG) for that color in the next step.

7. Adjust the other two background controls for best white balance.

8. Press ***Color Purity*** key as necessary to obtain the white raster.

9. Set front panel BRIGHTNESS control at maximum.

10. Observe the screen and adjust the DRIVE controls (RV921, RV931 and RV911) located on the bottom PC board for best white balance.

**NOTE**

*White balance is checked in two ways. First, using an average piece of white photocopy paper, compare the white on the CRT to the paper. Second, in the CONFIDENCE TEST function, the gray scale blocks are checked to make sure the block at the far left of the CRT is visible.*

11. Repeat steps 1-3 and 6-10 until satisfied with white balance.

# SECTION 5
# REPLACEABLE PARTS

## 5-1. INTRODUCTION

This section contains information for ordering parts. Table 5-1 lists the abbreviations used in the parts list and throughout this manual. Figure 5- 1, which covers several pages, shows the locations of mainframe parts. Table 5-2 is the list of replaceable mainframe parts. Replaceable parts lists for individual assemblies are included in the HP 54111D Service Data Supplement.

Additional information (about parts or different instrument versions) that may be a consideration when ordering, is given in a history section following the parts list. An asterisk keys affected parts in the parts list.

## 5-2. ABBREVIATIONS

Table 5-1 lists abbreviations used in the parts list, the schematics, and elsewhere in this manual. In some cases two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms may be used with both lowercase and uppercase letters.

## 5-3. PARTS LIST

Table 5-2, the list of replaceable mainframe parts, is organized as follows:

a. Exchange assemblies. These assemblies can be ordered at reduced cost when the inoperative assembly is returned to Hewlett-Packard.

b. External parts. These parts are associated with the outside of the instrument and might be replaced during routine maintenance due to loss or damage.

c. Internal parts. These parts are encountered when the instrument is disassembled for repair. It includes assemblies, cables, mechanical parts, hardware, and so fourth.

The following information is given for each part.

a. Hewlett-Packard part number and the check digit (for HP internal use).

b. Total quantity (Qty) in the instrument, given only once, at the first appearance of the part number in the list.

c. Description of the part.

d. A typical manufacturer of a given part in a five digit code. All mainframe parts for this instrument are made by Hewlett-Packard or ordered by description.

e. The manufacturers' number for the part.

An asterisk in the parts list is a prompt to look in the history section following table 5-2 for additional information concerning that part.

## 5-4. EXCHANGE ASSEMBLIES

Some of the parts used in this instrument have been set up on the Blue-stripe exchange program. This allows the customer to exchange his faulty assembly with one that has been repaired, calibrated, and performance-verified by the factory. The cost is significantly less than that of a new part.

Exchangeable parts are listed in a separate section in the replaceable parts table. They have a part number in the form XXXXX-695XX (where the new part would be XXXXX-665XX).

Before ordering a Blue-stripe assembly, check with you're local parts or repair organization for the procedures associated with the Blue-stripe program.

## 5-5. ORDERING INFORMATION

To order a part listed in the replaceable parts list, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service Office.

To order a part that is not listed in the replaceable parts table, include the instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

## 5-6. DIRECT MAIL ORDER SYSTEM

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are as follows:

a. Direct ordering and shipment from the HP Parts Center.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

Mail-order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this manual.

*Table 5-1. Reference Designators and Abbreviations.*

**REFERENCE DESIGNATORS**

| | |
|---|---|
| **A** | =assembly |
| **B** | =fan;motor |
| **BT** | =battery |
| **C** | =capacitor |
| **CR** | =diode;diode thyristor; varactor |
| **DL** | =delay line |
| **DS** | =annunciator;lamp;LED |
| **E** | =misc. electrical part |
| **F** | =fuse |
| **FL** | =filter |
| **H** | =hardware |
| **J** | =electrical connector (stationary portion);jack |
| **L** | =coil;inductor |
| **MP** | =misc. mechanical part |
| **P** | =electrical connector (moveable portion);plug |
| **Q** | =transistor;SCR; triode thyristor |
| **R** | =resistor |
| **RT** | =thermistor |
| **S** | =switch;jumper |
| **T** | =transformer |
| **TB** | =terminal board |
| **TP** | =test point |
| **U** | =integrated circuit; microcircuit |
| **V** | =electron tube; glow lamp |
| **VR** | =voltage regulator; breakdown diode |
| **W** | =cable |
| **X** | =socket |
| **Y** | =crystal unit(piezo-electric or quartz) |

**ABBREVIATIONS**

| | |
|---|---|
| **A** | =amperes |
| **A/D** | =analog-to-digital |
| **AC** | =alternating current |
| **ADJ** | =adjust(ment) |
| **AL** | =aluminum |
| **AMPL** | =amplifier |
| **ANLG** | =analog |
| **ANSI** | =American National Standards Institute |
| **ASSY** | =assembly |
| **ASTIG** | =astigmatism |
| **ASYNCHRO** | =asynchronous |
| **ATTEN** | =attenuator |
| **AWG** | =American wire gauge |
| **BAL** | =balance |
| **BCD** | =binary-code decimal |
| **BD** | =board |
| **BFR** | =buffer |
| **BIN** | =binary |
| **BRDG** | =bridge |
| **BSHG** | =bushing |
| **BW** | =bandwidth |
| **C** | =ceramic;cermet (resistor) |
| **CAL** | =calibrate;calibration |
| **CC** | =carbon composition |
| **CCW** | =counterclockwise |
| **CER** | =ceramic |
| **CFM** | =cubic feet/minute |
| **CH** | =choke |
| **CHAM** | =chamfered |
| **CHAN** | =channel |
| **CHAR** | =character |
| **CM** | =centimeter |
| **CMOS** | =complementary metal-oxide-semiconductor |
| **CMR** | =common mode rejection |
| **CNDCT** | =conductor |
| **CNTR** | =counter |
| **CON** | =connector |
| **CONT** | =contact |
| **CRT** | =cathode-ray tube |
| **CW** | =clockwise |
| **D** | =diameter |
| **D/A** | =digital-to-analog |
| **DAC** | =digital-to-analog converter |
| **DARL** | =darlington |
| **DAT** | =data |
| **DBL** | =double |
| **DBM** | =decibel referenced to 1mW |
| **DC** | =direct current |
| **DCDR** | =decoder |
| **DEG** | =degree |
| **DEMUX** | =demultiplexer |
| **DET** | =detector |
| **DIA** | =diameter |
| **DIP** | =dual in-line package |
| **DIV** | =division |
| **DMA** | =direct memory access |
| **DPDT** | =double-pole, double-throw |
| **DRC** | =DAC refresh controller |
| **DRVR** | =driver |
| **DWL** | =dowel |
| **ECL** | =emitter coupled logic |
| **ELAS** | =elastomeric |
| **EXT** | =external |
| **F** | =farads;metal film (resistor) |
| **FC** | =carbon film/ composition |
| **FD** | =feed |
| **FEM** | =female |
| **FF** | =flip-flop |
| **FL** | =flat |
| **FM** | =foam;from |
| **FR** | =front |
| **FT** | =gain bandwidth product |
| **FW** | =full wave |
| **FXD** | =fixed |
| **GEN** | =generator |
| **GND** | =ground(ed) |
| **GP** | =general purpose |
| **GRAT** | =graticule |
| **GRV** | =groove |
| **H** | =henries;high |
| **HD** | =hardware |
| **HDND** | =hardened |
| **HG** | =mercury |
| **HGT** | =height |
| **HLCL** | =helical |
| **HORIZ** | =horizontal |
| **HP** | =Hewlett-Packard |
| **HP-IB** | =Hewlett-Packard Interface Bus |
| **HR** | =hour(s) |
| **HV** | =high voltage |
| **HZ** | =Hertz |
| **I/O** | =input/output |
| **IC** | =integrated circuit |
| **ID** | =inside diameter |
| **IN** | =inch |
| **INCL** | =include(s) |
| **INCAND** | =incandescent |
| **INP** | =input |
| **INTEN** | =intensity |
| **INTL** | =internal |
| **INV** | =inverter |
| **JFET** | =junction field-effect transistor |
| **JKT** | =jacket |
| **K** | =kilo($10^3$) |
| **L** | =low |
| **LB** | =pound |
| **LCH** | =latch |
| **LCL** | =local |
| **LED** | =light-emitting diode |
| **LG** | =long |
| **LI** | =lithium |
| **LK** | =lock |
| **LKWR** | =lockwasher |
| **LS** | =low power Schottky |
| **LV** | =low voltage |
| **M** | =mega($10^6$);megohms; meter(distance) |
| **MACH** | =machine |
| **MAX** | =maximum |
| **MFR** | =manufacturer |
| **MICPROC** | =microprocessor |
| **MINTR** | =miniature |
| **MISC** | =miscellaneous |
| **MLD** | =molded |
| **MM** | =millimeter |
| **MO** | =metal oxide |
| **MTG** | =mounting |
| **MTLC** | =metallic |
| **MUX** | =multiplexer |
| **MW** | =milliwatt |
| **N** | =nano($10^{-9}$) |
| **NC** | =no connection |
| **NMOS** | =n-channel metal-oxide-semiconductor |
| **NPN** | =negative-positive-negative |
| **NPRN** | =neoprene |
| **NRFR** | =not recommended for field replacement |
| **NSR** | =not separately replaceable |
| **NUM** | =numeric |
| **OBD** | =order by description |
| **OCTL** | =octal |
| **OD** | =outside diameter |
| **OP AMP** | =operational amplifier |
| **OSC** | =oscillator |
| **P** | =plastic |
| **P/O** | =part of |
| **PC** | =printed circuit |
| **PCB** | =printed circuit board |
| **PD** | =power dissipation |
| **PF** | =picofards |
| **PI** | =plug in |
| **PL** | =plate(d) |
| **PLA** | =programmable logic array |
| **PLST** | =plastic |
| **PNP** | =positive-negative-positive |
| **POLYE** | =polyester |
| **POS** | =positive;position |
| **POT** | =potentiometer |
| **POZI** | =pozidrive |
| **PP** | =peak-to-peak |
| **PPM** | =parts per million |
| **PRCN** | =precision |
| **PREAMP** | =preamplifier |
| **PRGMBL** | =programmable |
| **PRL** | =parallel |
| **PROG** | =programmable |
| **PSTN** | =position |
| **PT** | =point |
| **PW** | =potted wirewound |
| **PWR** | =power |
| **R-S** | =reset-set |
| **RAM** | =random-access memory |
| **RECT** | =rectifier |
| **RET** | =retainer |
| **RF** | =radio frequency |
| **RGLTR** | =regulator |
| **RGTR** | =register |
| **RK** | =rack |
| **RMS** | =root-mean-square |
| **RND** | =round |
| **ROM** | =read-only memory |
| **RPG** | =rotary pulse generator |
| **RX** | =receiver |
| **S** | =Schottky-clamped; seconds(time) |
| **SCR** | =screw;silicon controlled rectifier |
| **SEC** | =second(time);secondary |
| **SEG** | =segment |
| **SEL** | =selector |
| **SGL** | =single |
| **SHF** | =shift |
| **SI** | =silicon |
| **SIP** | =single in-line package |
| **SKT** | =skirt |
| **SL** | =slide |
| **SLDR** | =solder |
| **SLT** | =slot(ted) |
| **SOLD** | =solenoid |
| **SPCL** | =special |
| **SQ** | =square |
| **SREG** | =shift register |
| **SRQ** | =service request |
| **STAT** | =static |
| **STD** | =standard |
| **SYNCHRO** | =synchronous |
| **TA** | =tantalum |
| **TBAX** | =tubeaxial |
| **TC** | =temperature coefficient |
| **TD** | =time delay |
| **THD** | =thread(ed) |
| **THK** | =thick |
| **THRU** | =through |
| **TP** | =test point |
| **TPG** | =tapping |
| **TPL** | =triple |
| **TRANS** | =transformer |
| **TRIG** | =trigger(ed) |
| **TRMR** | =trimmmer |
| **TRN** | =turn(s) |
| **TTL** | =transistor-transistor |
| **TX** | =transmitter |
| **U** | =micro($10^{-6}$) |
| **UL** | =Underwriters Laboratory |
| **UNREG** | =unregulated |
| **VA** | =voltampere |
| **VAC** | =volt,ac |
| **VAR** | =variable |
| **VCO** | =voltage-controlled oscillator |
| **VDC** | =volt,dc |
| **VERT** | =vertical |
| **VF** | =voltage,filtered |
| **VS** | =versus |
| **W** | =watts |
| **W/** | =with |
| **W/O** | =without |
| **WW** | =wirewound |
| **XSTR** | =transistor |
| **ZNR** | =zener |
| **°C** | =degree Celsius (Centigrade) |
| **°F** | =degree Fahrenheit |
| **°K** | =degree Kelvin |

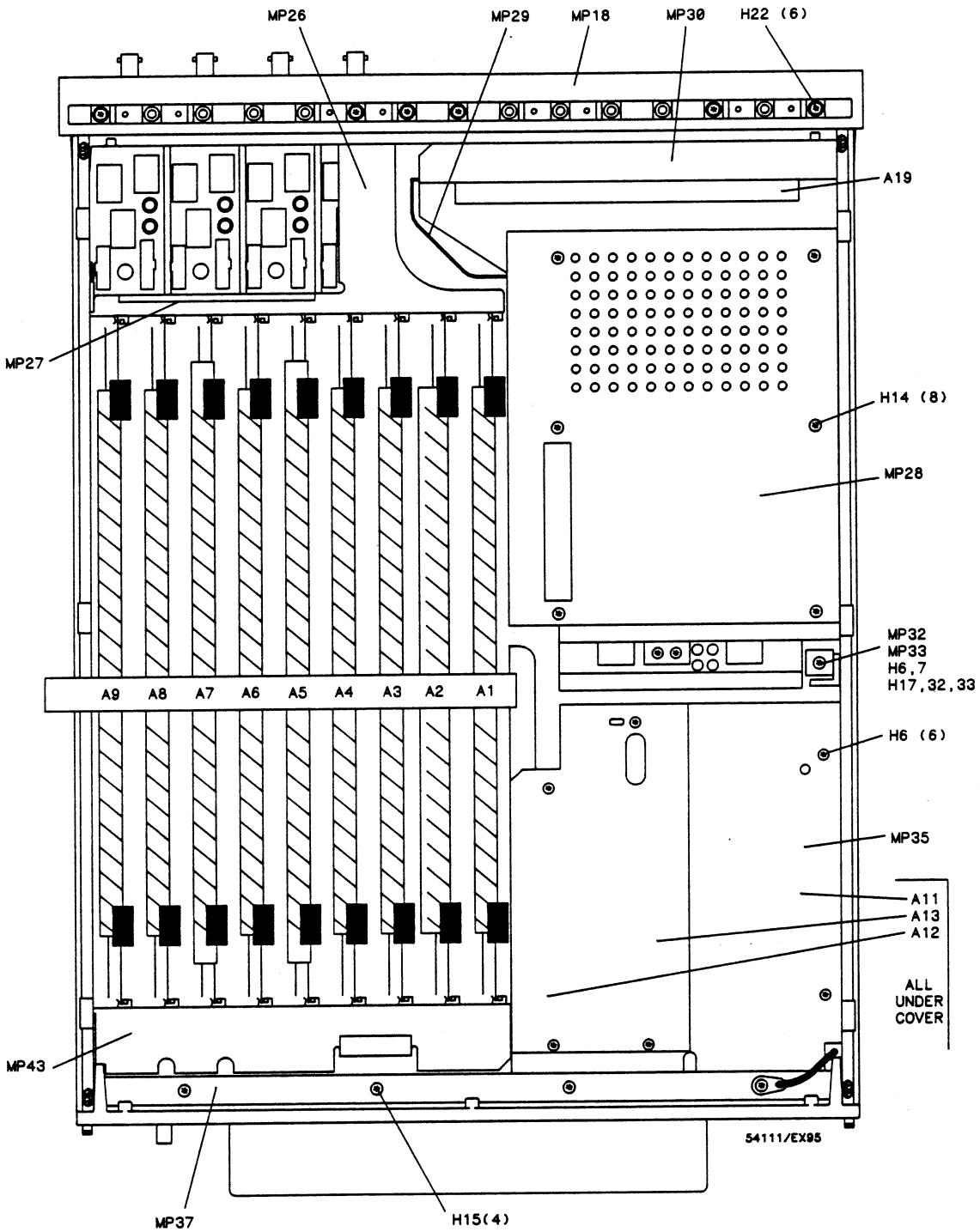



*Figure 5-1. Mainframe Parts Locations (sheet 1 of 5)*

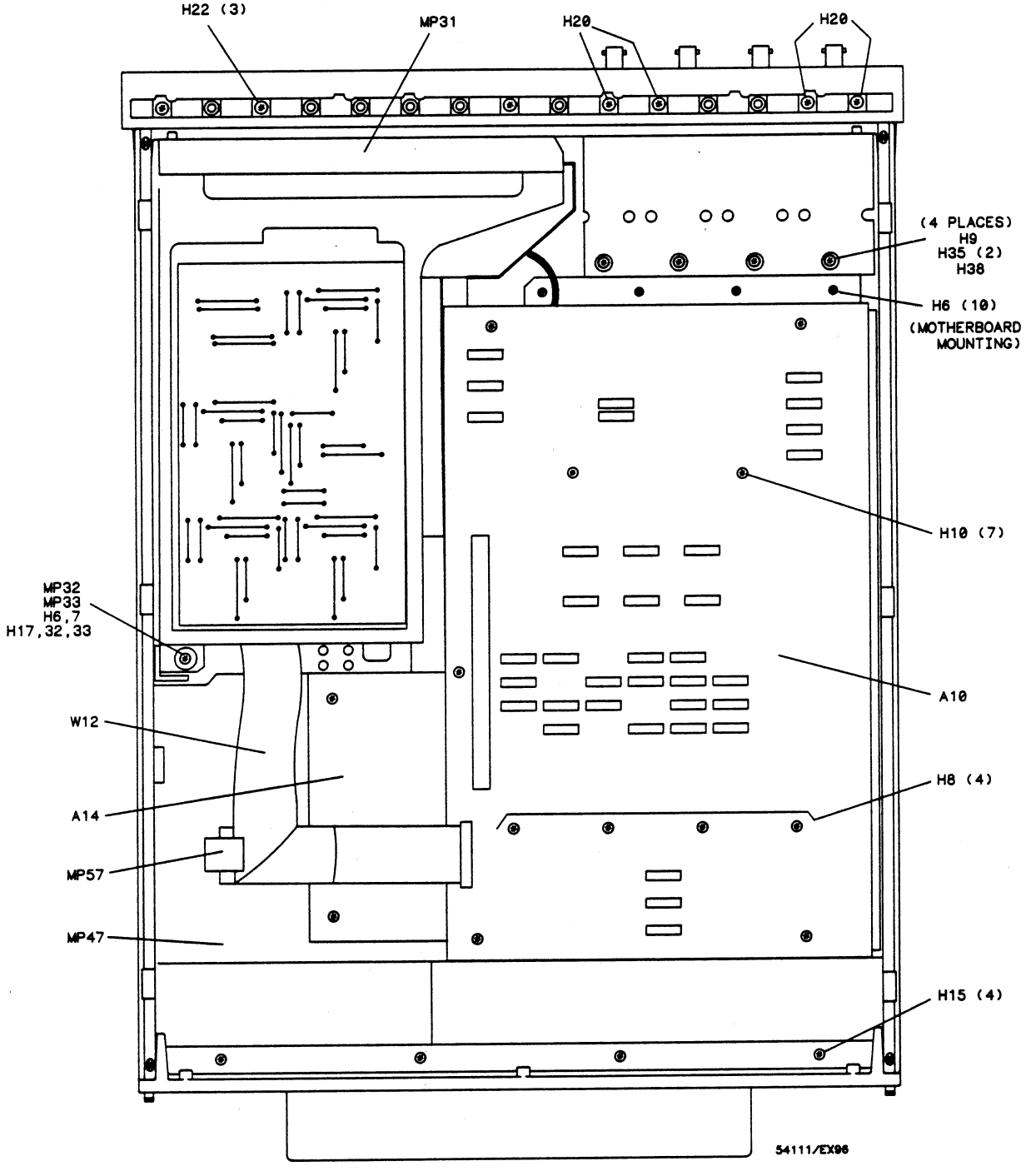



*Figure 5-1. Mainframe Parts Locations (sheet 2 of 5)*

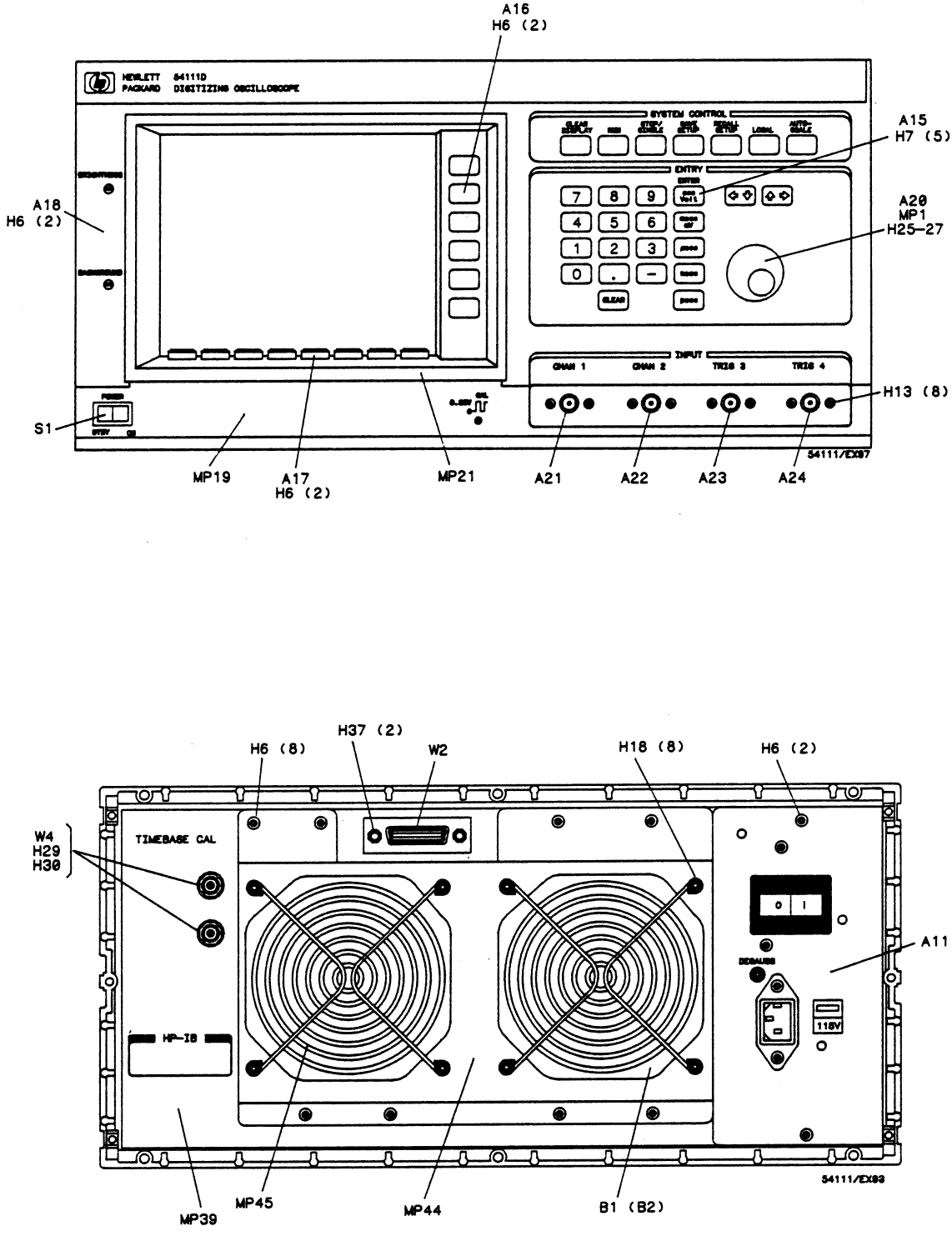
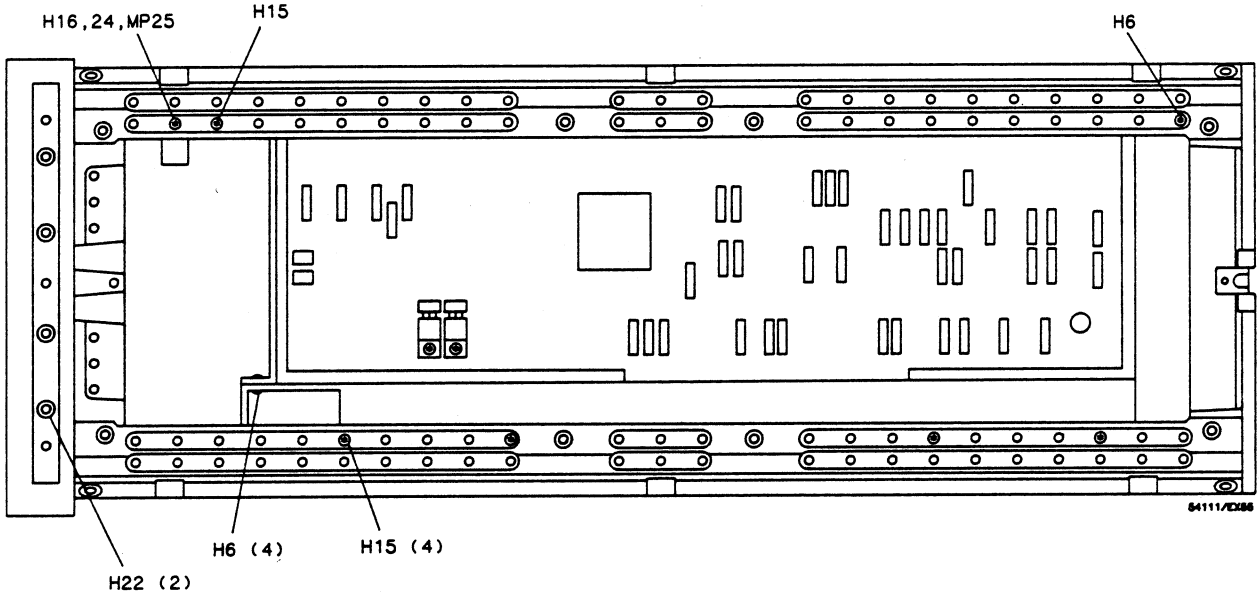



*Figure 5-1. Mainframe Parts Locations (sheet 3 of 5)*



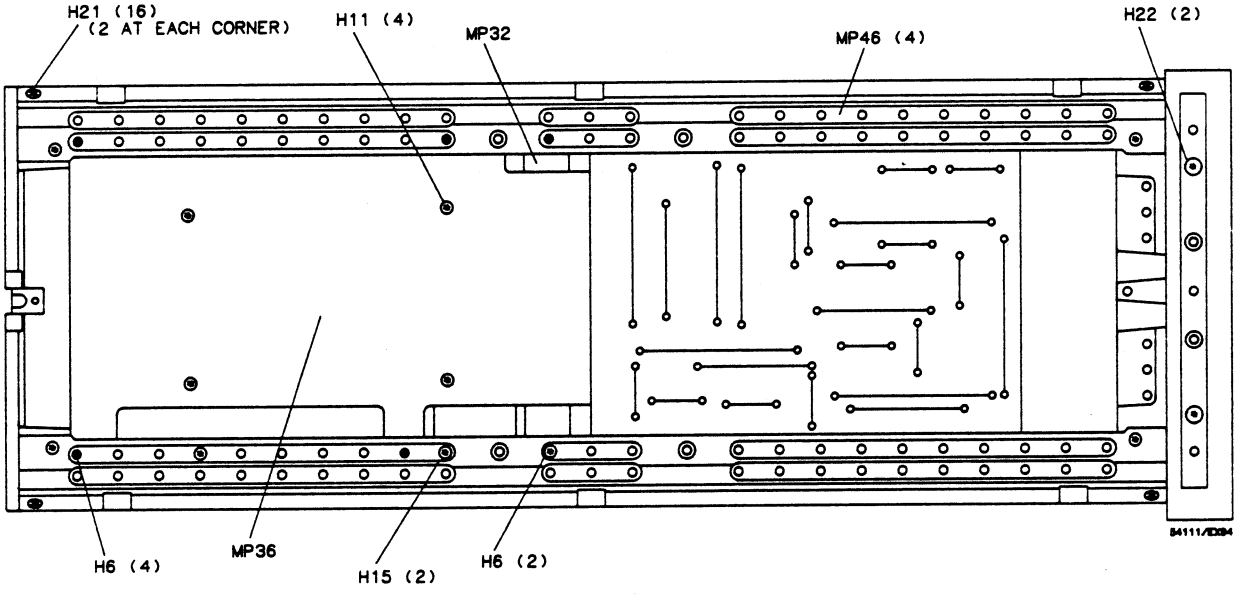




*Figure 5-1. Mainframe Parts Locations (sheet 4 of 5)*

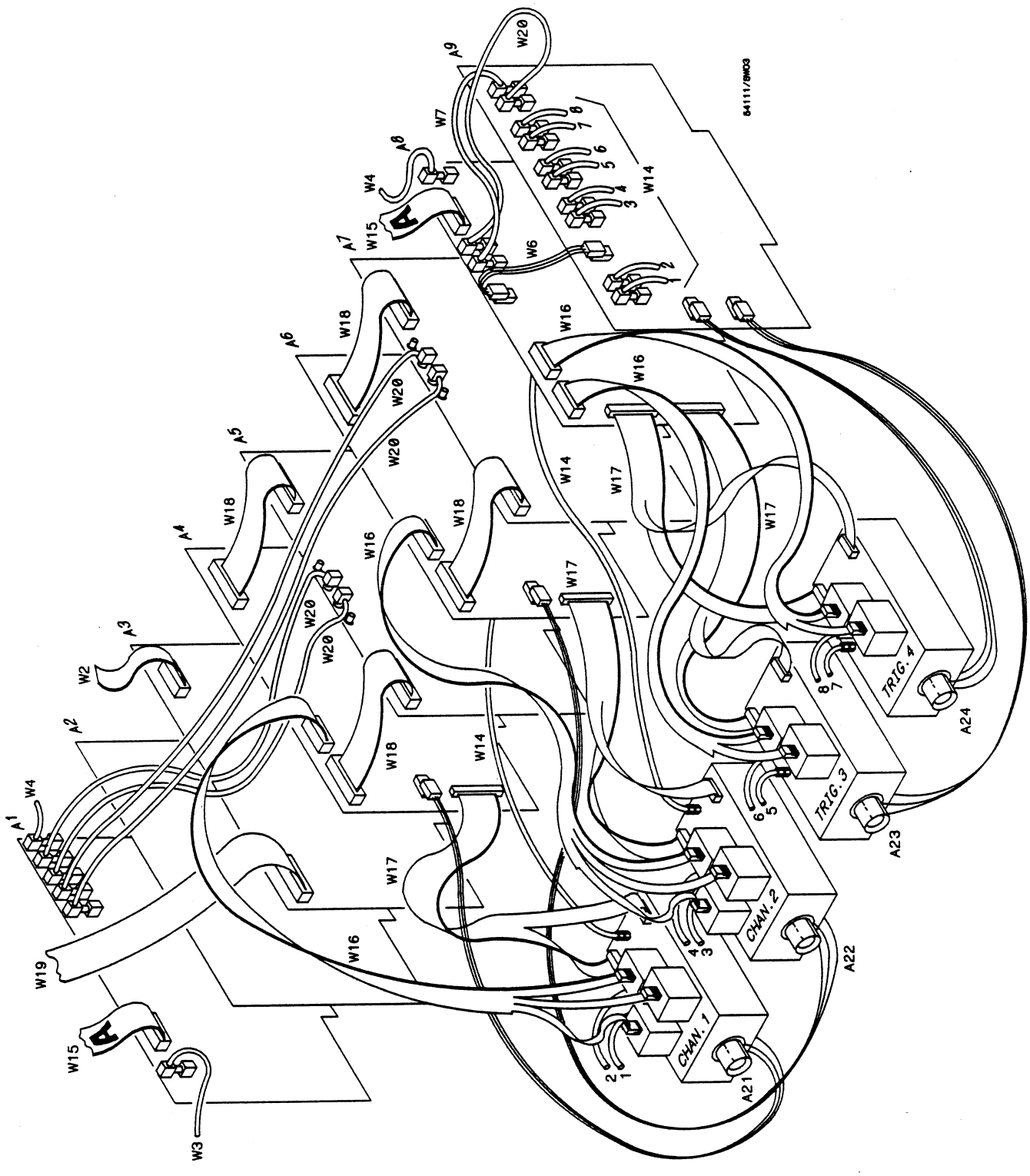



*Figure 5-1. Mainframe Parts Locations (sheet 5 of 5)*

*Table 5-2. Replaceable Parts*

| Reference Designator | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|---|
| | | | | MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES | | |
| | | | | 2640A, 2710A, 2726A, AND 2733A | | |
| | | | | ARE THE SAME AS THE CURRENT LIST | | |
| *A1, A2 | | | | See Parts History | | |
| | | | | **CURRENT PARTS LIST FOR HP 54111D** | | |
| | | | | MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIX 2808A | | |
| EXCHANGE ASSEMBLIES | | | | (See paragraph 5-4 for exchange assembly ordering information) | | |
| *A1 | 54111-69513 | 7 | 1 | TIMEBASE ASSEMBLY | 28480 | 54111-69513 |
| *A2 | 54111-69517 | 1 | 1 | MICROPROCESSOR ASSEMBLY | 28480 | 54111-69517 |
| A3 | 54111-69506 | 8 | 1 | INPUT/OUTPUT ASSEMBLY | 28480 | 54111-69506 |
| A4 | 54111-69518 | 9 | 2 | ADC CONTROL ASSEMBLY | 28480 | 54111-69518 |
| A5 | 54111-69501 | 3 | 2 | ANALOG-TO-DIGITAL CONVERTOR ASSEMBLY | 28480 | 54111-69501 |
| A6 | 54111-69518 | 9 | | ADC CONTROL ASSEMBLY | 28480 | 54111-69518 |
| A7 | 54111-69501 | 3 | | ANALOG-TO-DIGITAL CONVERTOR ASSEMBLY | 28480 | 54111-69501 |
| A8 | 54111-69504 | 6 | 1 | TRIGGER ASSEMBLY | 28480 | 54111-69504 |
| A9 | 54111-69505 | 7 | 1 | TRIGGER QUALIFIER ASSEMBLY | 28480 | 54111-69505 |
| A10 | 54110-69512 | 5 | 1 | BD ASSY COLOR DISPLAY | 28480 | 54110-69512 |
| A11 | 54110-69513 | 6 | 1 | BD ASSY PRIMARY POWER SUPPLY | 28480 | 54110-69513 |
| A12 | 54110-69510 | 3 | 1 | BD ASSY ANALOG POWER SUPPLY | 28480 | 54110-69510 |
| A13 | 54110-69506 | 1 | 1 | BD ASSY DIGITAL POWER SUPPLY | 28480 | 54110-69506 |
| EXTERNAL PARTS | | | | | | |
| E1 | 8160-0577 | 4 | 8ft | GROUND STRIP - RFI | 28480 | 8160-0577 |
| H1 | 0515-1384 | 8 | 2 | SCREW-MACH M5 10MM-LG FLAT-HEAD T25 | 00000 | ORDER BY DESCRIPTION |
| H2 | 0515-1444 | 1 | 4 | SCREW-MACH M3.5 25.4MM-LG PAN-HD TXX | 00000 | ORDER BY DESCRIPTION |
| H3 | 0515-1245 | 0 | 3 | SCREW-MACH M3.5 12MM-LG COVER MOUNTING | 28480 | 0515-1245 |
| H4 | 0510-1253 | 0 | 3 | RETAINING RING FOR COVER MOUNTING SCREW | 28480 | 0510-1253 |
| H5 | | | | NOT ASSIGNED | | |
| MP1 | 01650-47401 | 7 | 1 | KNOB - RPG | 28480 | 01650-47401 |
| MP2 | 5061-9448 | 3 | 1 | COVER - BOTTOM | 28480 | 5061-9448 |
| MP3 | 5040-7201 | 8 | 2 | FOOT - BOTTOM - FRONT | 28480 | 5040-7201 |
| MP4 | 5040-7222 | 3 | 2 | FOOT - BOTTOM REAR - NON SKID | 28480 | 5040-7222 |
| MP5 | 1460-1345 | 5 | 2 | TILT STAND SST | 28480 | 1460-1345 |
| MP6 | 8160-0590 | 1 | 2 | RFI STRIP-FINGERS | 28480 | 8160-0590 |
| MP7 | 54110-04103 | 4 | 1 | CVR - TOP | 28480 | 54110-04103 |
| MP8 | 54111-94301 | 4 | 1 | CABLE ROUTING DIAGRAM | 28480 | 54111-94301 |
| MP9 | 5001-0441 | 2 | 2 | TRIM STRIP - SIDE | 28480 | 5001-0441 |
| MP10 | 5040-7202 | 9 | 1 | TRIM STRIP - TOP | 28480 | 5040-7202 |
| MP11 | 54110-40502 | 3 | 4 | FOOT - REAR PANEL | 28480 | 54110-40502 |
| MP12 | 5060-9948 | 6 | 1 | CVR - PERF LF SIDE | 28480 | 5060-9948 |
| MP13 | 5061-9523 | 5 | 1 | CVR - PERF RT SIDE | 28480 | 5061-9523 |
| MP14 | 5060-9805 | 4 | 1 | STRAP - HANDLE | 28480 | 5060-9805 |
| MP15 | 5041-6819 | 4 | 1 | CAP - STRAP HANDLE (FRONT) | 28480 | 5041-6819 |
| MP16 | 5041-6820 | 7 | 1 | CAP - STRAP HANDLE (REAR) | *28480* | *5041-6820* |
| W1 | 8120-1521 | 6 | 1 | POWER CORD 125V USA/CANADA | 28480 | 8120-1521 |
| | 8120-1703 | 6 | | POWER CORD OPTION 900 UNITED KINGDOM | 28480 | 8120-1703 |
| | 8120-0696 | 4 | | POWER CORD OPTION 901 AUST/NEW ZEALAND | 28480 | 8120-0696 |
| | 8120-1692 | 2 | | POWER CORD OPTION 902 EUROPEAN CONTINENT | 28480 | 8120-1692 |
| | 8120-0698 | 6 | | POWER CORD OPTION 904 250V USA/CANADA | 28480 | 8120-0698 |
| | 8120-2296 | 4 | | POWER CORD OPTION 906 SWITZERLAND | 28480 | 8120-2296 |
| | 8120-2957 | 4 | | POWER CORD OPTION 912 DENMARK | 28480 | 8120-2957 |
| | 8120-4600 | 8 | | POWER CORD OPTION 917 SOUTH AFRICA | 28480 | 8120-4600 |
| | 8120-4754 | 3 | | POWER CORD OPTION 918 JAPAN | 28480 | 8120-4754 |

*Table 5-2. Replaceable Parts (Cont'd)*

| Reference Designator | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|---|
| PROBES | 10431A | 0 | 2 | DIVIDER PROBE - 10:1 | 28480 | 10431A |
| RACK MOUNT KIT | 5061-9679 | 2 | | RACK MOUNT KIT - OPTION 908 | 28480 | 5061-9679 |
| INTERNAL PARTS | | | | | | |
| *A1 | 54111-66513 | 1 | 1 | TIMEBASE ASSEMBLY | 28480 | 54111-66513 |
| *A2 | 54111-66517 | 5 | 1 | MICROPROCESSOR ASSEMBLY | 28480 | 54111-66517 |
| A3 | 54111-66506 | 2 | 1 | INPUT/OUTPUT ASSEMBLY | 28480 | 54111-66506 |
| A4 | 54111-66518 | 6 | 2 | ADC CONTROL ASSEMBLY CH1 | 28480 | 54111-66518 |
| A5 | 54111-66501 | 7 | 2 | ADC ASSEMBLY CH1 | 28480 | 54111-66501 |
| A6 | 54111-66518 | 6 | | ADC CONTROL ASSEMBLY CH2 | 28480 | 54111-66518 |
| A7 | 54111-66501 | 7 | | ADC ASSEMBLY CH2 | 28480 | 54111-66501 |
| A8 | 54111-66504 | 0 | 1 | TRIGGER ASSEMBLY | 28480 | 54111-66504 |
| A9 | 54111-66505 | 1 | 1 | TRIGGER QUALIFIER ASSEMBLY | 28480 | 54111-66505 |
| A10 | 54110-66512 | 9 | 1 | COLOR DISPLAY ASSEMBLY | 28480 | 54110-66512 |
| A11 | 54110-66513 | 0 | 1 | BD ASSY PRIMARY POWER SUPPLY | 28480 | 54110-66513 |
| A12 | 54110-66510 | 7 | 1 | BD ASSY ANALOG POWER SUPPLY | 28480 | 54110-66510 |
| A13 | 54110-66506 | 1 | 1 | BD ASSY DIGITAL POWER SUPPLY | 28480 | 54110-66506 |
| A14 | 54110-66511 | 8 | 1 | BD ASSY MOTHER | 28480 | 54110-66511 |
| A15 | 54100-66505 | 8 | 1 | BD ASSY CONTROL KEYBOARD | 28480 | 54100-66505 |
| A16 | 54110-66502 | 7 | 1 | BD ASSY FUNCTION KEYBOARD | 28480 | 54110-66502 |
| A17 | 54100-66520 | 7 | 1 | BD ASSY MENU KEYBOARD | 28480 | 54100-66520 |
| A18 | 54110-66509 | 4 | 1 | BD ASSY DISPLAY CONTROL | 28480 | 54110-66509 |
| A19 | 2090-0092 | 3 | 1 | MODULE - COLOR CRT | 28480 | 2090-0092 |
| A20 | 01980-61062 | 5 | 1 | ASSY - RPG | 28480 | 01980-61062 |
| A21 | 1NC1-0001 | 7 | 2 | ATTENUATOR ASSEMBLY CHANNEL 1 | 28480 | 1NC1-0001 |
| A22 | 1NC1-0001 | 7 | | ATTENUATOR ASSEMBLY CHANNEL 2 | 28480 | 1NC1-0001 |
| A23 | 1NC1-0002 | 8 | 2 | ATTENUATOR ASSEMBLY TRIGGER 3 | 28480 | 1NC1-0002 |
| A24 | 1NC1-0002 | 8 | | ATTENUATOR ASSEMBLY TRIGGER 4 | 28480 | 1NC1-0002 |
| B1 | 3160-0521 | 3 | 2 | FAN - TUBEAXIAL | 28480 | 3160-0521 |
| B2 | 3160-0521 | 3 | | FAN - TUBEAXIAL | 28480 | 3160-0521 |
| H6 | 0515-0372 | 2 | 39 | SCREW-MACH M3 8MM-LG PAN-HD T10 | 00000 | ORDER BY DESCRIPTION |
| H7 | 0515-0664 | 5 | 7 | SCREW-MACH M3 12MM-LG PAN-HD T10 | 00000 | ORDER BY DESCRIPTION |
| H8 | 0515-0430 | 3 | 4 | SCREW-MACH M3 6MM-LG PAN-HD T10 | 00000 | ORDER BY DESCRIPTION |
| H9 | 0515-0665 | 6 | 8 | SCREW-MACH M3 14MM-LG PAN-HD T10 | 00000 | ORDER BY DESCRIPTION |
| H10 | 0515-1410 | 1 | 7 | SCREW-MACH M3 20MM-LG PAN-HD T10 | 00000 | ORDER BY DESCRIPTION |
| H11 | 0515-1025 | 6 | 4 | SCREW-MACH M3 26MM-LG PAN-HD T10 | 00000 | ORDER BY DESCRIPTION |
| H12 | | | | NOT ASSIGNED | | |
| H13 | 0515-1035 | 4 | 8 | SCREW-MACH M3 8MM-LG FLAT-HEAD T10 | 00000 | ORDER BY DESCRIPTION |
| H14 | 0515-1271 | 2 | 8 | SCREW-MACH M3 6MM-LG THREAD ROLLING | 00000 | ORDER BY DESCRIPTION |
| H15 | 0515-0433 | 6 | 16 | SCREW-MACH M4 8MM-LG PAN-HD T15 | 00000 | ORDER BY DESCRIPTION |
| H16 | 0515-0383 | 5 | 1 | SCREW-MACH M4 16MM-LG PAN-HD T15 | 00000 | ORDER BY DESCRIPTION |
| H17 | 0515-0641 | 8 | 2 | SCREW-MACH M4 10MM-LG PAN-HD T15 | 00000 | ORDER BY DESCRIPTION |
| H18 | 0515-0435 | 8 | 8 | SCREW-MACH M4 14MM-LG PAN-HD T15 | 00000 | ORDER BY DESCRIPTION |
| H18 | 0361-1272 | 6 | 8 | FASTENER PUSH-PIN (newer instruments) H31 not used on these instruments | 28480 | 0361-1272 |
| H19 | | | | NOT ASSIGNED | | |
| H20 | 0515-1228 | 9 | 4 | SCREW-MACH M4 6MM-LG FLAT-HEAD T15 | 00000 | ORDER BY DESCRIPTION |
| H21 | 0515-1403 | 2 | 16 | SCREW-MACH M4 6MM-LG FLAT-HEAD T15 | 00000 | ORDER BY DESCRIPTION |
| H22 | 0515-1269 | 9 | 17 | SCREW-MACH M4 10MM-LG FLAT-HEAD T15 | 00000 | ORDER BY DESCRIPTION |
| H23 | 0535-0031 | 2 | 8 | NUT-HEX M3 W/LOCK WASHER | 00000 | ORDER BY DESCRIPTION |
| H24 | 0535-0043 | 6 | 1 | NUT-HEX M4 W/LOCK WASHER | 00000 | ORDER BY DESCRIPTION |
| H25 | 2950-0043 | 6 | 1 | NUT-HEX 3/8-32 | 00000 | ORDER BY DESCRIPTION |
| H26 | 3050-1176 | 3 | 1 | WASHER-FLAT NYLON 3/8 | 28480 | 3050-1176 |
| H27 | 2190-0016 | 3 | 1 | WASHER-INTERNAL LOCK 3/8 | 00000 | ORDER BY DESCRIPTION |
| H28 | | | | NOT ASSIGNED | | |
| H29 | 2950-0035 | 4 | 2 | NUT-HEX 15/32-32 | 00000 | ORDER BY DESCRIPTION |
| H30 | 2190-0068 | 5 | 2 | WASHER-INTERNAL LOCK 1/2 | 00000 | ORDER BY DESCRIPTION |
| H31 | 5061-6138 | 2 | 8 | NUT-INSERT M4 (inst with screw mtd fans) | 28480 | 5061-6138 |
| H32 | 2190-0763 | 1 | 2 | WASHER-FLAT METAL 0.14ID 0.50D | 28480 | 2190-0763 |
| H33 | 3050-1238 | 8 | 2 | WASHER-FLAT NEOPRENE 0.149ID 0.478OD | 28480 | 3050-1238 |
| H34 | | | | NOT ASSIGNED | | |
| H35 | 3050-0005 | 5 | 8 | WASHER-SHOULDER 0.14ID 0.375OD | 28480 | 3050-0005 |

See introduction to this section for ordering information

*Table 5-2. Replaceable Parts (Cont'd)*

| Reference Designator | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|---|
| H36 | 0380-1902 | 9 | 4 | STANDOFF-HEX M3 | 28480 | 0380-1902 |
| H37 | 0380-1686 | 6 | 2 | STANDOFF-HEX HP-IB | 28480 | 0380-1686 |
| H38 | 0360-0053 | 7 | 1 | TERMINAL-SOLDER LUG | 28480 | 0360-0053 |
| MP17 | | | | NOT ASSIGNED | | |
| MP18 | 5021-5807 | 6 | 1 | FRAME - FRONT | 28480 | 5021-5807 |
| MP19 | 54111-00204 | 9 | 1 | PANEL - FRONT | 28480 | 54111-00204 |
| MP20 | 54111-00203 | 8 | 1 | PANEL - SUB FRT | 28480 | 54111-00203 |
| MP21 | 54110-40501 | 2 | 1 | BEZEL - CRT | 28480 | 54110-40501 |
| MP22 | | | | NOT ASSIGNED | | |
| MP23 | 0403-0092 | 6 | 1 | RUBBER BUMPER (MENU KEYBOARD SUPPORT) | 28480 | 0403-0092 |
| MP24 | 1400-1362 | 0 | 2 | CLAMP - CABLE - TWIST TYPE | 28480 | 1400-1362 |
| MP25 | 1400-0025 | 0 | 1 | CLAMP - CABLE - TRIG CABLE SUPPORT | 28480 | 1400-0025 |
| MP26 | 54111-01203 | 0 | 1 | BKT - CARD CAGE FRT | 28480 | 54111-01203 |
| MP27 | 0400-0018 | 0 | .4ft | CHANNEL GROMMET - NYLON | 28480 | 0400-0018 |
| MP28 | 54111-00607 | 6 | 1 | SHIELD - COLOR CRT MODULE | 28480 | 54111-00607 |
| MP29 | 4320-0242 | 6 | .3ft | GROMMET - CHANNEL (earlier instruments) | 28480 | 4320-0242 |
| MP29 | 0400-0010 | 2 | 1 | GROMMET - ROUND (later instruments) | 28480 | 0400-0010 |
| MP30 | 54110-01201 | 7 | 1 | BRACKET - COLOR CRT MOD FRONT-TOP | 28480 | 54110-01201 |
| MP31 | 54110-01202 | 8 | 1 | BRACKET - COLOR CRT MOD FRONT-BOTTOM | 28480 | 54110-01202 |
| MP32 | *54110-01210* | 8 | 1 | *BRACKET - COLOR CRT MOD REAR-ON FRAME* | *28480* | *54110-01210* |
| MP33 | 54110-04702 | 9 | 1 | BRACKET - COLOR CRT MOD REAR-ON MODULE | 28480 | 54100-04702 |
| MP34 | | | | NOT ASSIGNED | | |
| MP35 | 54111-04104 | 6 | 1 | COVER - POWER SUPPLY (TOP) | 28480 | 54111-04104 |
| MP36 | 54110-04106 | 7 | 1 | COVER - POWER SUPPLY (SIDE) | 28480 | 54110-04106 |
| MP37 | 5021-5808 | 7 | 1 | FRAME - REAR | 28480 | 5021-5808 |
| MP38 | 54110-94302 | 4 | 1 | LABEL - GROUND CONNECTION WARNING | 28480 | 54110-94302 |
| MP39 | 54111-00202 | 7 | 1 | PANEL - REAR | 28480 | 54111-00202 |
| MP40 | 5958-5582 | 9 | 1 | LABLE - X-RAY | 28480 | 5958-5582 |
| MP41 | 7120-4835 | 0 | 1 | LABEL - CSA CERTIFICATION | 28480 | 7120-4835 |
| MP42 | | | | NOT ASSIGNED | | |
| MP43 | 54111-05201 | 6 | 1 | DEFL ASSY - AIR | 28480 | 54111-05201 |
| MP44 | 54110-04108 | 9 | 1 | HOUSING - FAN | 28480 | 54110-04108 |
| MP45 | 3160-0092 | 3 | 2 | FINGER GUARD | 28480 | 3160-0092 |
| MP46 | 5021-5838 | 3 | 4 | STRUT - SIDE | 28480 | 5021-5838 |
| MP47 | 54111-00101 | 5 | 1 | DECK - MAIN | 28480 | 54111-00101 |
| MP48 | | | | NOT ASSIGNED | | |
| MP49 | 5041-1480 | 5 | 2 | WIRE MARKER - BROWN | 28480 | 5041-1480 |
| MP50 | 5041-1481 | 6 | 2 | WIRE MARKER - WHITE | 28480 | 5041-1481 |
| MP51 | 5041-1482 | 7 | 2 | WIRE MARKER - VIOLET | 28480 | 5041-1482 |
| MP52 | 5041-1483 | 8 | 2 | WIRE MARKER - BLUE | 28480 | 5041-1483 |
| MP53 | 5041-1484 | 9 | 2 | WIRE MARKER - GREEN | 28480 | 5041-1484 |
| MP54 | 5041-1485 | 0 | 2 | WIRE MARKER - YELLOW | 28480 | 5041-1485 |
| MP55 | 5041-1486 | 1 | 2 | WIRE MARKER - ORANGE | 28480 | 5041-1486 |
| MP56 | 5041-1487 | 2 | 2 | WIRE MARKER - RED | 28480 | 5041-1487 |
| MP57 | 1400-0611 | 0 | 1 | CLAMP - CABLE - DISPLAY RIBBON CABLE | 28480 | 1400-0611 |
| MP58 | 1400-0679 | 0 | 2 | CLAMP - CABLE - MOTHER BD CABLE HOLDER | 28480 | 1400-0679 |
| S1 | 3101-2911 | 5 | 1 | SWITCH - ROCKER (Standby) | 28480 | 3101-2911 |
| W2 | 54111-61612 | 1 | 1 | CABLE - HPIB | 28480 | 54111-61612 |
| W3 | 54111-61601 | 8 | 1 | CABLE - COAX - FRONT PANEL CAL SIGNAL | 28480 | 54111-61601 |
| W4 | 54100-61610 | 6 | 2 | CABLE - COAX - LTRIG - TIMEBASE CAL | 28480 | 54100-61610 |
| W5 | 54100-61612 | 8 | 2 | CABLE - 3-WIRE - 300VDC PRIMARY POWER | 28480 | 54100-61612 |
| W6 | 54100-61613 | 9 | 1 | CABLE - 3-WIRE - HOLDOFF/GATE | 28480 | 54100-61613 |
| W7 | 54100-61614 | 0 | 1 | CABLE - COAX - 4 INCH - QUALTRIG(D) | 28480 | 54100-61614 |
| W8 | 54110-61601 | 5 | 1 | CABLE - 3-WIRE - COLOR CRT MOD POWER | 28480 | 54110-61601 |
| W9 | 54111-61611 | 0 | 1 | CABLE-SHIELDED-FRONT PANEL STBY SWITCH | 28480 | 54110-61611 |
| W10 | 54111-61610 | 1 | 1 | CABLE-SHIELDED-REAR CABLE STBY SWITCH | 28480 | 54111-61610 |
| W11 | 54110-61611 | 9 | 1 | CABLE - DISPLAY CONTROL | 28480 | 54110-61611 |
| W12 | 54110-61607 | 3 | 1 | CABLE - RIBBON - DISP ASSY TO COLOR MOD | 28480 | 54110-61607 |
| W13 | | | | NOT ASSIGNED | | |
| W14 | 54111-61602 | 9 | 10 | CABLE - COAX - VIN - TCLOCK/LTCLOCK | 28480 | 54111-61602 |
| W15 | 54111-61603 | 0 | 1 | CABLE - RIBBON - ATRIG | 28480 | 54111-61603 |
| W16 | 54111-61604 | 1 | 4 | CABLE - CHANNEL/TRIGGER SOLENOID CABLE | 28480 | 54111-61604 |
| W17 | 54111-61605 | 2 | 4 | CABLE - ATTENUATOR/TRIGGER POWER | 28480 | 54111-61605 |
| W18 | 54111-61606 | 3 | 4 | CABLE - RIBBON - CONTROL 1/2 | 28480 | 54111-61606 |
| W19 | 54100-61601 | 3 | 1 | CABLE - RIBBON - I/O TO FRONT PANEL | 28480 | 54100-61601 |
| W20 | 54111-61609 | 6 | 5 | CABLE - COAX - 12 INCH - TCLK | 28480 | 54111-61609 |

See introduction to this section for ordering information

## 5-7. INSTRUMENT AND PART HISTORY

The following provides a brief history of changes in the HP 54111D. Information can be used when ordering parts which may have changed during the manufacturing life of the instrument. It covers such issues as part compatability or part preferences. One key to this section is an asterisk by the reference designator or part number in the parts list.

A new assembly often obsoletes the older one. Because of the Blue- stripe exchange program, there is more chance that an instrument may contain a later version of a part. This also means instrument serial prefix is not a sure indication of the part complement in an instrument.

Even though a part may not have the same part number as the one in your instrument, use the part number in the parts list, along with any following history information, to be sure you are ordering the correct parts to repair your instrument.

### 1. Serial Prefixes 2640A, 2710A, 2726A, and 2733A

Differences connected with these serial prefixes are virtually transparent to the user and service person. Several assemblies were changed to accomodate manufacturing issues, but all later versions obsolete the earlier ones.

### 2. Serial Prefix 2808A

This serial prefix change updated the firmware (Microprocessor, A2) and changed the Timebase assembly (A1). The Microprocessor changed from 54111-66507 to -66517. The Timebase changed from 54111-66516 to -66513. The previous assemblies are obsolete.

The new Microprocessor (firmware dated March 10, 1988) directly replaces the old one. However, a Service Note, 54111D-6, describes a difference in the firmware that can affect bus controlled instruments and mentions added features of the new firmware. Check with your HP Customer Service representative.

The new Timebase assembly is not compatable with the old firmware. If the instrument has firmware dated April 22, 1987 (check through the Display Configuration menu), the firmware must be updated to ensure correct operation with the replacement Timebase. Service Note 54111D-4 covers this instance. Check with your HP Customer Service representative.

# SECTION 6A
# MAINFRAME DISASSEMBLY

## 6A-1. INTRODUCTION

This section contains removal and replacement procedures for mainframe assemblies. It includes a diagram showing assembly locations and a diagram showing how the instrument is cabled.

## 6A-2. SAFETY CONSIDERATIONS

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

**WARNING**

*This instrument is equipped with a standby switch on the front panel that DOES NOT de-energize the power supply. To avoid shock hazards capable of causing injury or death, the main power switch on the rear panel must be used to de-energize the instrument or the power cable must be disconnected when the instrument must be de-energized.*

**WARNING**

*These procedures are used while repairing an instrument that has protective covers removed and may have had power applied. Maintenance should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock). Read the Safety Summary in the front of this manual.*

**CAUTION**

*Do not remove or replace any of the circuit board assemblies in the instrument unless instrument power is removed. The boards contain components which may be damaged if the board is removed or replaced when instrument power is applied.*

**CAUTION**

*The HP 54111D is highly sensitive to Electrostatic Discharge (ESD). Proper ESD precautions should be taken whenever the covers of the instrument are removed and particularly when assemblies are being removed and replaced. Disconnecting and connecting cables can cause ESD into sensitive circuitry.*

*Use of an anti-static mat and a wrist strap that grounds the service person to the instrument or the mat is recommended. Keep all assemblies in anti-static bags when not installed in an instrument.*

## 6A-3. TOOLS REQUIRED

The hardware requires TORX® type tools for removal and replacement. Sizes required for the procedures in this section are #10 and #15.

If the display must be replaced, an 8 mm wrench or driver is also required.

If an attenuator must be replaced, a 6 mm open end wrench is needed. This wrench is provided in the HP 54100 Family Support Kit.

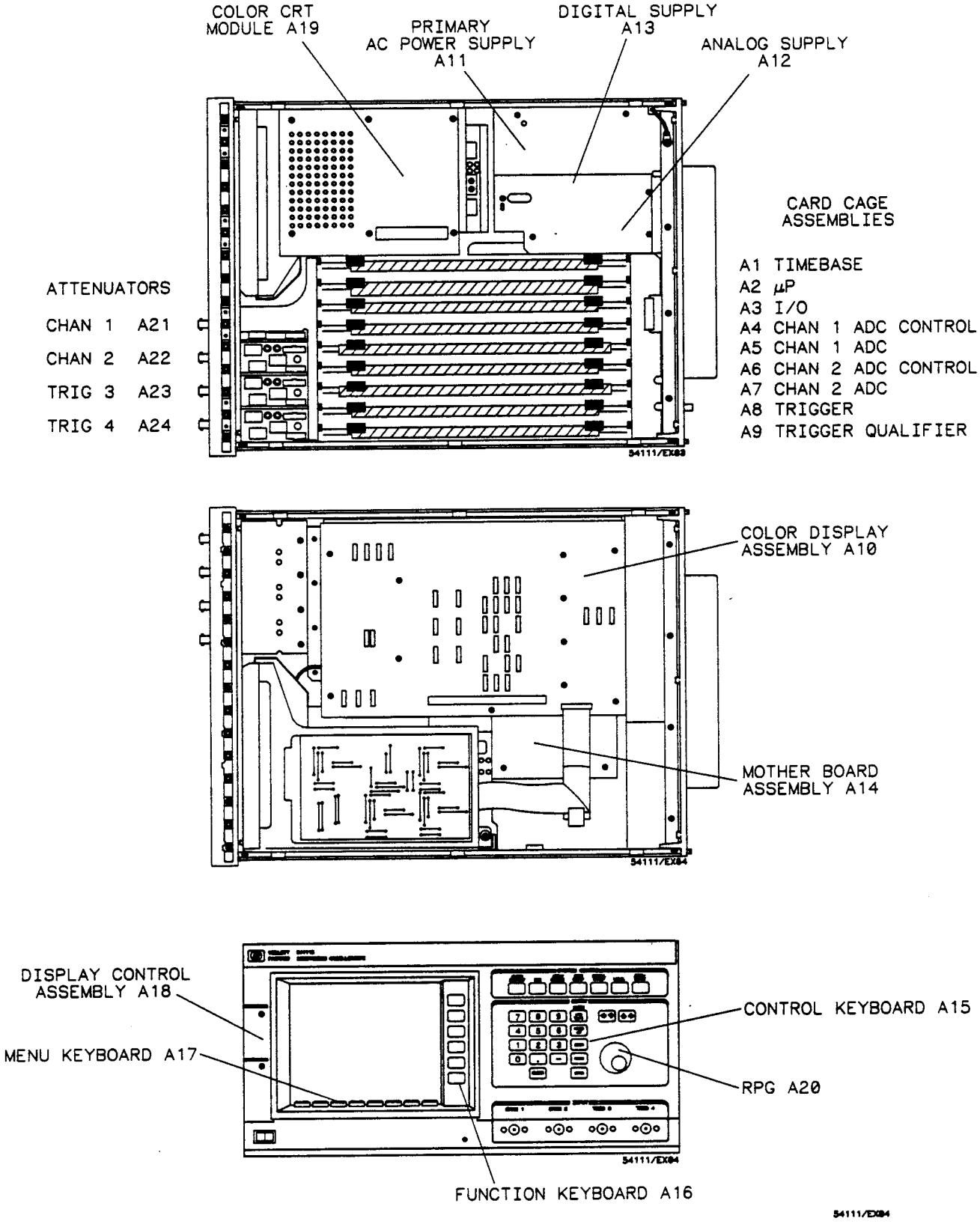



*Figure 6A-1. Major Assembly Locations.*

## 6A-4. MAJOR ASSEMBLY REMOVAL PROCEDURES

The following procedures should be followed when disassembling the instrument. Particular care should be taken with the cabling connecting card cage assemblies and attenuators.

## 6A-5. Card Cage PC Assemblies

**REMOVAL**

1. Disconnect power cable.
2. Remove the top rear feet, then the top cover.
3. Disconnect any cables from assembly to be removed. Some assemblies have cables along the front edge. These must be removed before the assembly is pulled up.
4. Refer to the illustration on top the power supply. Release PC assembly by pulling the flexible plastic extractors away from the assembly shield, then up.
5. Remove the assembly from the connector by pulling up on the extractors. As the assembly is removed from the instrument, check for cables connected to the center of the assembly and remove them.

**REPLACEMENT**

1. Insert PC assembly shield edges in proper guides.
2. Keep the extractors up while sliding the assembly in.
3. If the assembly has cabling to its center area, it must be connected as the board is being inserted.
4. If the assembly has cabling to its front edge, it will be easier to connect the cables as soon as the connector is below the top edge of the card cage frame. Refer to the cabling diagram on the instrument top cover or the diagram at the end of this section.
5. While keeping assembly properly aligned in guides, push it in. As the top edge of the assembly becomes level with the top of the card cage the connector will start to engage. Keep assembly level and apply even pressure until connector is seated.

**CAUTION**

***Do not use the extractors to lever the assembly into the connector.*** *Using the extractors makes it too easy to apply excessive force that might bend misaligned connector pins. If the connector will not seat, remove the assembly and check for bent pins.*

*Avoid pinching cabling between the assembly and the mainframe. The coaxial cables that connect to the center of the ADC assemblies are particularly vulnerable to pinching between the assembly and the main deck.*

6. Reconnect all remaining cabling. Refer to the diagram on the instrument cover or the diagram at the end of this section.

## 6A-6. Primary Power Supply

### REMOVAL

1. Disconnect power cable.
2. Remove the rear feet from the top right corner and left side.
3. Remove the top and left side covers.

**WARNING**

*Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.*

4. Through the hole in the top power supply shield, observe the red LED located on the Primary Power Supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding.
5. Remove top power supply shield (six screws).
6. Remove the screw that attaches the ground wire (green/yellow) to top corner of rear frame.
7. Remove the three cables at the top front of the Primary Power Supply PC board.
8. Remove four screws from power supply side cover (figure 6A-2).
9. Remove two screws which attach power supply assembly to rear panel (figure 6A-2).
10. Turn instrument onto its left side. Pull the power supply assembly rearward until the STBY switch cable at the rear of power supply board can be disconnected. Disconnect the cable.
11. Pull supply rearward until it clears the instrument.

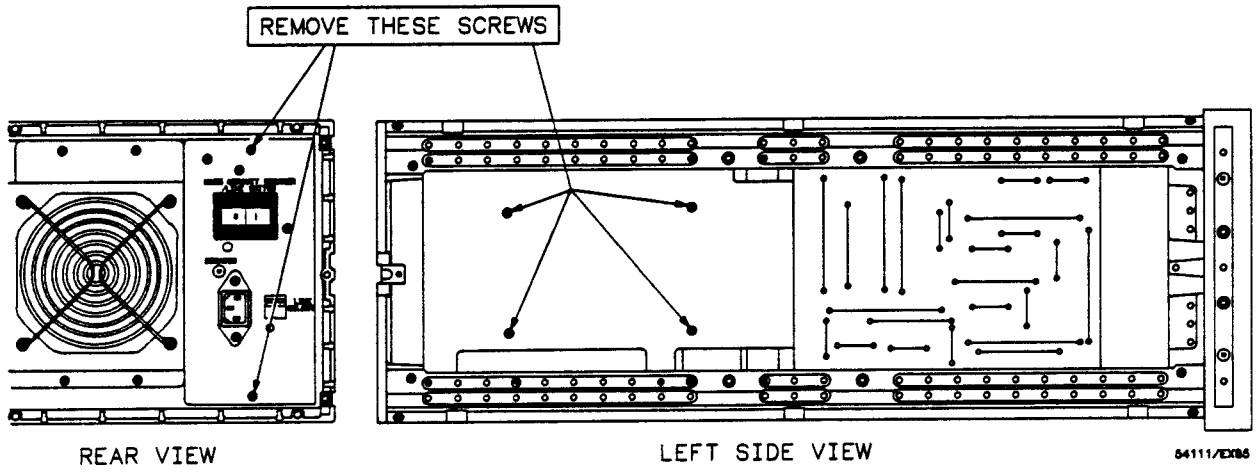



*Figure 6A-2. Primary Power Supply Mounting Screws.*

### PRIMARY POWER SUPPLY REPLACEMENT

Reverse removal procedure to install supply.

**WARNING**

*Power supply safety grounding will be defeated if ground wire removed in step 6 above is not reconnected. To avoid a defeated ground, make sure this green/yellow wire is re-attached to top rear corner of the rear frame.*

## 6A-7. Analog Power Supply

### REMOVAL

1. Disconnect power cable.
2. Remove the top rear feet and top cover.

**WARNING**

*Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.*

3. Through the hole in the top power supply shield, observe the red LED located on the Primary Power Supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding.
4. With the instrument on its left side, remove four screws along the bottom of the fan housing.
5. Set instrument back on its feet and remove the four screws along the top of the fan housing. Lay the fan housing flat, along the back of the instrument. It is not necessary to disconnect the fan power cable.
6. Remove top power supply shield (six screws).
7. Disconnect the Analog Power Supply input cable from the top front corner of the Primary Power Supply.
8. Use a flat-blade screwdriver to loosen the captive screw at the bottom front of the supply.
9. Release power supply board connector by pulling board straight up and off the guide posts.
10. Slide the Analog Power Supply back through the opening in the rear panel.

### REPLACEMENT

Reverse the removal procedure to install assembly.

## 6A-8. Digital Power Supply

### REMOVAL

1. Disconnect power cable.
2. Remove top rear feet and top cover.

**WARNING**

*Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.*

3. Through the hole in the top power supply shield, observe the red LED located on the Primary Power Supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding.
4. Remove top power supply shield (six screws).
5. Set the instrument on its left side. Loosen, approximately four turns, the bottom four fan housing mounting screws. Set the instrument on its feet and remove the top four fan housing mounting screws. This allows the fan housing to tilt back at the top, providing the necessary clearance for removing the Digital Power Supply.
6. Disconnect the Digital Power Supply input cable from the top front corner of the Primary Power Supply.
7. Use a flat-blade screwdriver to loosen the captive screw at the front bottom of the supply.
8. Release power supply board connector by pulling board straight up and off guide posts.
9. Remove the supply from the instrument by lifting front edge of board first then rotating board up and out.

### REPLACEMENT

Reverse removal procedure to install board.

## 6A-9. CRT Bezel, Function and Menu Keyboards

The keyboards at the side and bottom of the CRT can be removed by first removing the CRT Bezel.

### REMOVAL

1. While pushing down on top edge of bezel (see figure 6A-3), pull top edge away from front panel until holding tabs are clear of the front panel.
2. Lift bezel slightly and pull bottom of bezel away from front panel.
3. Pull bezel away from front panel just far enough to gain access to the ribbon cable connectors on Control Keyboard. They are located just to the right of the bezel opening in the front panel.
4. Disconnect the two ribbon cable connectors from the Control Keybard.

### REPLACEMENT

Reverse the removal procedure to install bezel.

**NOTE**

*The ribbon cables must be reconnected as follows: Function Keyboard cable (right side of bezel) to top connector on Control Keyboard and Menu Keyboard cable (bottom of bezel) to bottom connector on Control Keyboard.*

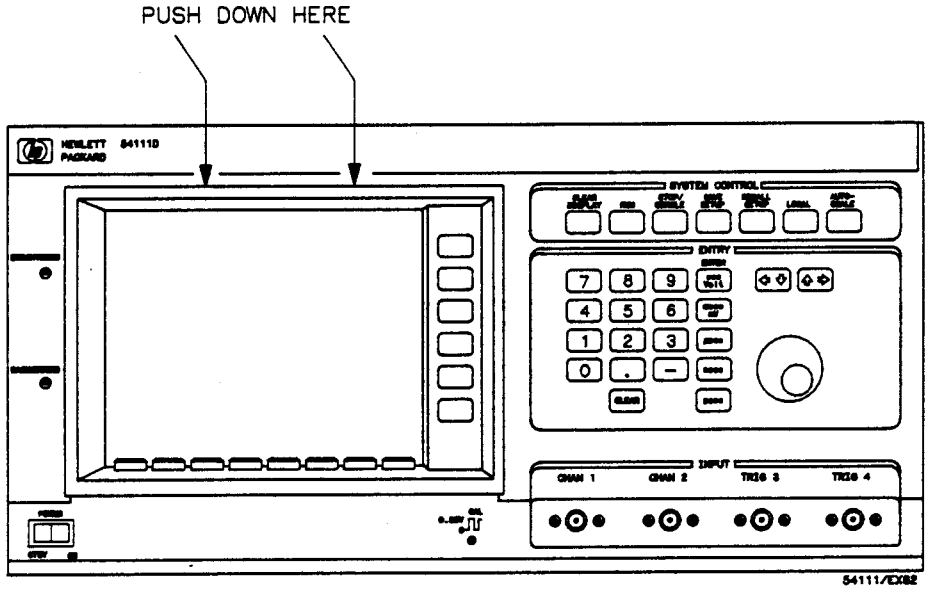



*Figure 6A-3. CRT Bezel Removal Pressure Locations.*

## 6A-10. Front Panel, Control Keyboard, and Display Control

Use steps 1 through 11 to remove Front Panel, steps 1 through 12 to remove Display Control, or steps 1 through 11 and steps 13 and 14 to remove Control Keyboard.

**NOTE**

*It is not necessary to remove the front panel to remove the keyboards around the CRT bezel. See the previous removal procedure.*

### FRONT PANEL REMOVAL

1. Disconnect power cable.
2. Remove the rear feet and the top, bottom, and side covers.
3. Remove top, and side trim strips from the front frame by carefully prying up at the ends of the strips with a flat blade screwdriver.
4. Remove the two front panel screws that were under each side trim strip.
5. Remove the two screws on either side of each of the input BNC connectors.
6. Remove six front panel screws as shown in the following figure.

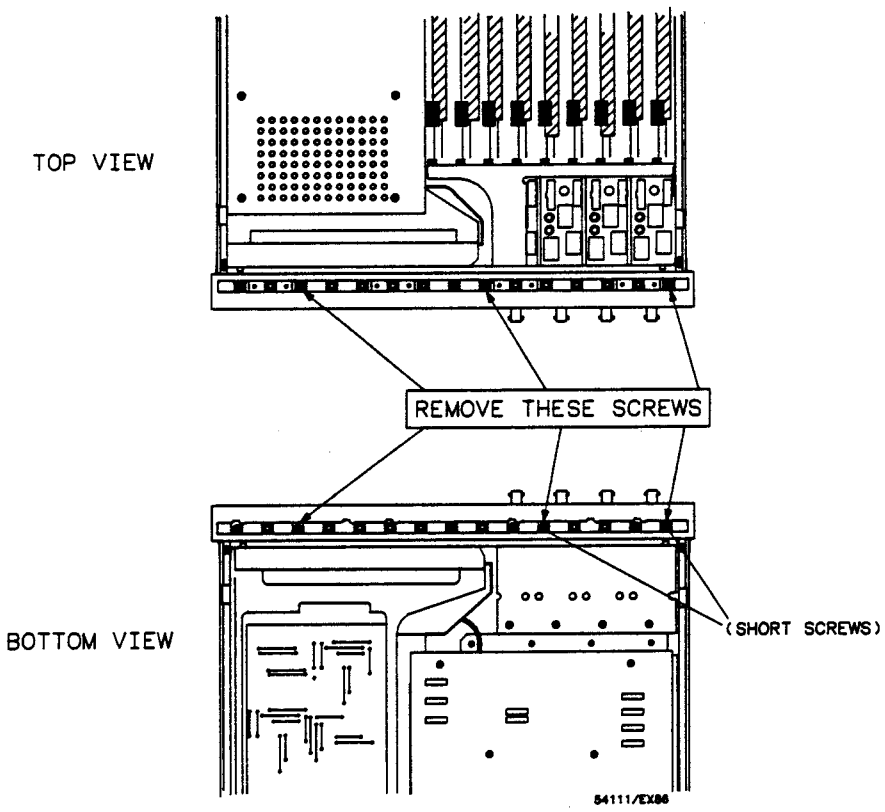



*Figure 6A-4. Top and Bottom Front Panel Mounting Screws.*

7. Set instrument in its normal operating position.

8. Note the routing of the calibrator signal coax at the front connector on the Timebase assembly (next to the Color CRT Module). Disconnect it at the Timebase and slide it out through the slot in the card cage bulkhead.

9. Disconnect the STBY switch by separating the two-wire interconnect just to the right of the CRT.

10. Pull front panel just far enough to gain access to the cable connector on the CRT Control board (left side of front panel) and disconnect the cable.

11. Open the two cable ties: top left, inside front panel and top right of CRT, and remove the cables.

12. Disconnect the large ribbon cable from the Control Keyboard and remove the front panel from the instrument.

**NOTE**

*At the front of the attenuators is a plastic bushing containing the Probe ID sensing ring. Note the orientation of this bushing and ring. The tabs of the bushing should be horizontal and fit into the recess on the front of the attenuator. Be sure the bushings for all attenuators are properly aligned before replacing the front panel.*

**DISPLAY CONTROL REMOVAL**

13. Remove two screws attaching the Display Control assembly.

**CONTROL KEYBOARD REMOVAL**

14. Disconnect the RPG cable at the Control Keyboard and the two cables from the CRT bezel keyboards.

    The Menu Keyboard (right side of bezel) cable goes to the top connector and the Function Keyboard (bottom of bezel) cable goes to the bottom connector on the Control Keyboard.

15. Remove five screws and remove board.

    Pass RPG cable through hole in Control Keyboard.

**ASSEMBLY REPLACEMENT**

Reverse the procedure to replace any of these assemblies.

## 6A-11. Attenuators

### REMOVAL

1. Remove Front Panel (refer to previous paragraph). Set instrument in its normal operating position.
2. Remove the screw at the rear of the attenuator to be removed. This screw is not captive. Don't let it fall into the interior of the instrument because it will be hard to retrieve.
3. Remove the connector for the three-wire cable that connects to the front of the attenuator. The connection is made at the front edge of one of the card cage boards.
3. Remove the connectors from the attenuator solenoids. Channel attenuators have three connectors on the end of each cable and trigger attenuators have two.
4. Remove the cable connectors at the back of the attenuators. Note the orientation of these connectors.
5. Remove the coaxial cables. It is necessary to remove the rear cable first. The HP 54100 Family Support Kit provides a 6 mm open-end wrench for removing these cables. The attenuator should now be free of the instrument.

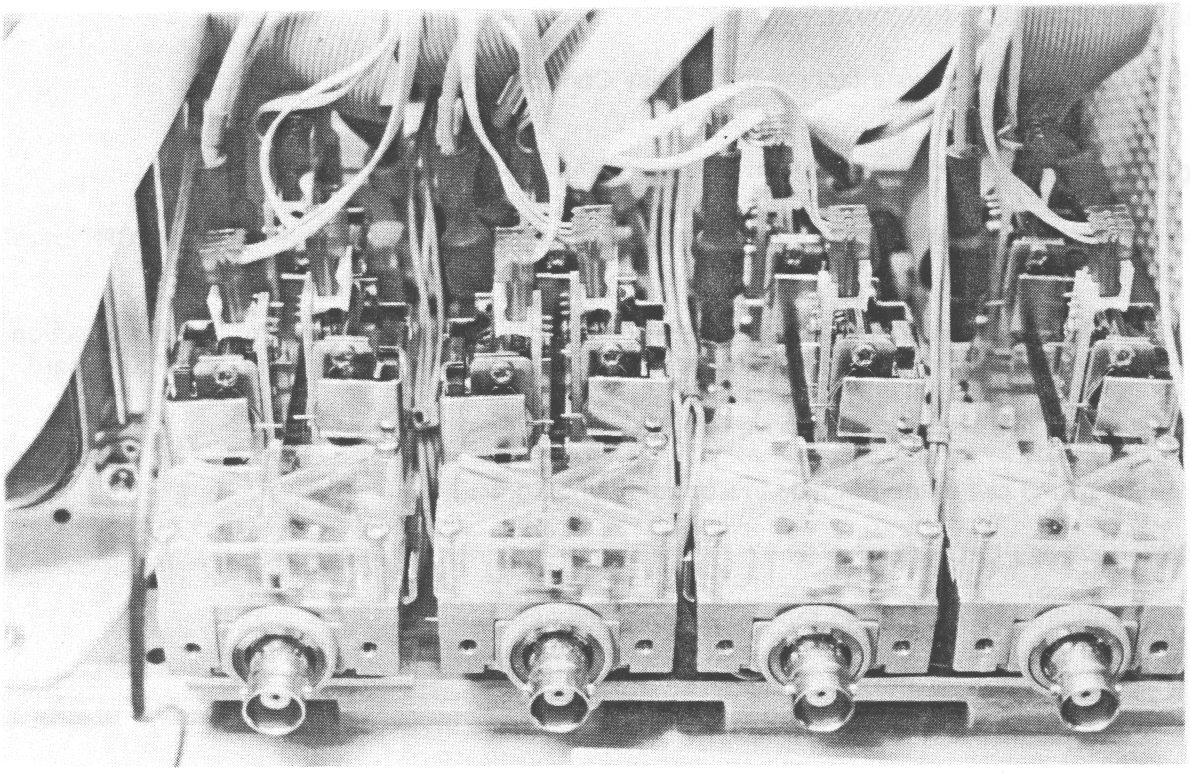


*Figure 6A-5. Channel and Trigger Attenuators.*

## REPLACEMENT

The replacement procedure is essentially the reverse of removal.

1. Connect the coaxial cables to the attenuator.

**NOTE**

*The two cables on the side are the trigger connections. The cable at the rear is the vertical signal connection. Only the Channel attenuators have this signal connector. The trigger cables have a colored marker at each end. Connect the cables to the attenuator using the following chart.*

| ATTENUATOR | FRONT CONNECTOR | REAR CONNECTOR |
|---|---|---|
| CHAN 1 | Brown | Red |
| CHAN 2 | Orange | Yellow |
| TRIG 3 | Green | Blue |
| TRIG 4 | Violet | White |

*In the event that the cables were inadvertently removed at the Trigger Qualifier, they should be re-installed in order of color, front to back, following the standard color code. You can also use the diagram on the cover of the instrument or at the back of this section.*

2. Connect the rear ribbon cables to the attenuator. The connectors are keyed.

3. Carefully connect the cables to the solenoids. The connectors are keyed but the keying can be defeated by excessive force. Use the cabling diagram on the inside of the instrument top cover or the figure at the end of this section.

4. Connect the three-wire cable to the front of the appropriate card cage assembly. Use the cabling diagram for reference. Route the cable along the right side of the attenuator.

5. Insert the rear mounting screw into the hole at the rear of the attenuator. Slide the attenuator into place and rest the mounting screw on the standoff. Hold the attenuator in line with the others while inserting the screw.

   **NOTE** *Leave the rear screw slightly loose so the attenuator will align with the front panel when front screws are tightened. Rear screw is tightened last.*

6. Recheck the routing of all cables, especially the three-wire cable. It can become pinched when the front panel is installed.

7. Check the alignment of the BNC sensing ring on all attenuators. It should fit into the recess in the front of the attenuator.

8. Install the front panel and reassemble the rest of the instrument. Use the appropriate procedures in this section.

## 6A-12. Color CRT Module

The Color CRT Module is replaceable only as a complete unit.

### COLOR CRT MODULE REMOVAL

1. Remove Front Panel (refer to the appropriate paragraph in this section).
2. Disconnect the flat wide ribbon cable from the Color Display Assembly and remove cable from clip.
3. Remove four screws that attach the Color Display Module to the front frame (see figure below).
4. Remove two screws attaching side of module to left side corner struts (see figure below).
5. Slowly pull module forward until the power cable (small three-wire) can be disconnected at the Primary Power Supply board.
6. Continue pulling module forward until it clears the instrument.

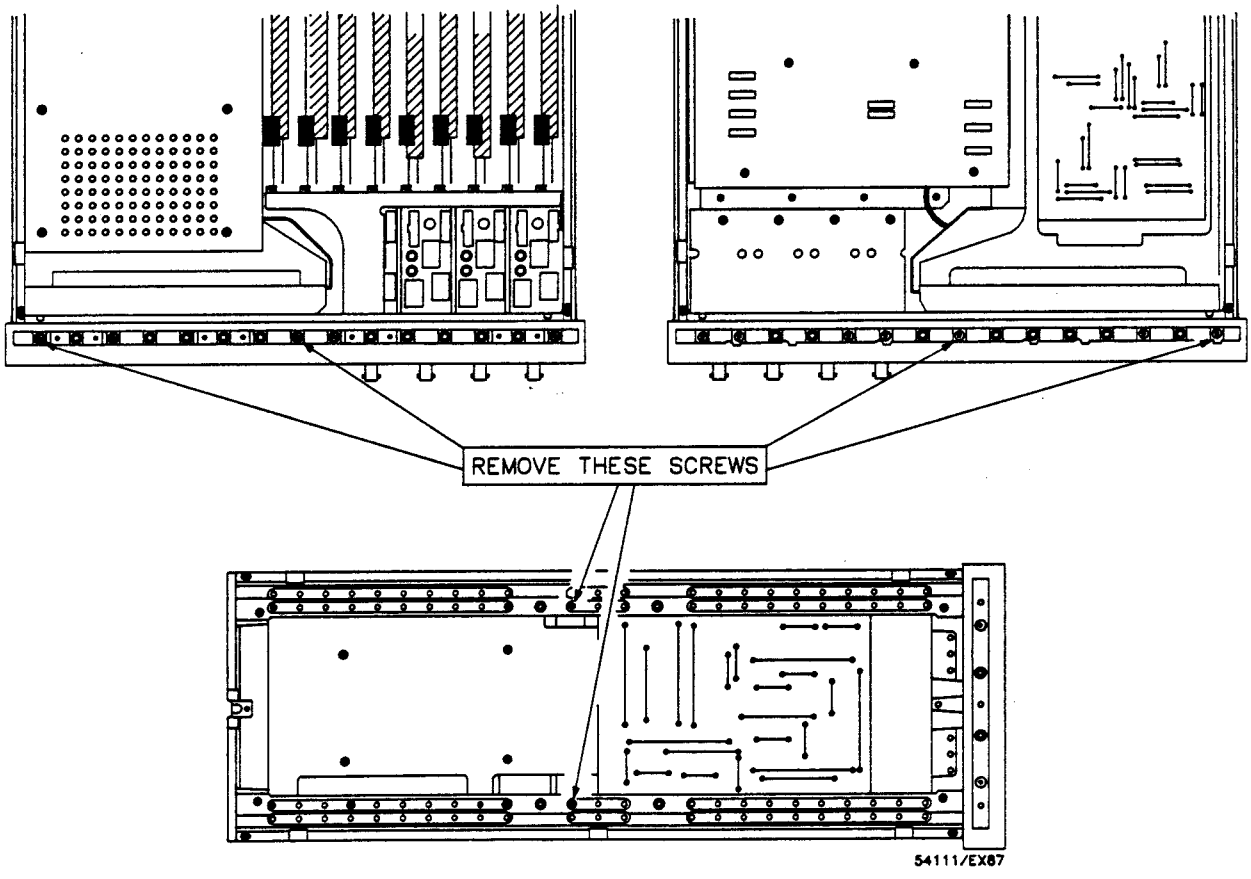



*Figure 6A-6. Color CRT Module Mounting Screws.*

## REPLACEMENT

It is necessary to remove several items from the inoperative Color CRT Module and install them on the new one. Use the following procedure to do that and install the new module.

TRANSFER PARTS TO NEW MODULE

1. Remove the eight small screws that hold the shield to the top and side of the inoperative module.

   THESE SCREWS ARE SPECIAL self-tapping screws, different from the screws in the rest of the instrument. They must be used for mounting the shield on the new module. Do not use them for any other purpose.

2. Use an 8 mm wrench to remove the four nuts on the front of the inoperative module and remove the shield.

3. Remove the front mounting brackets and put the 8 mm nuts back on the module.

4. Remove the 8 mm nuts from the new module, do not remove any other hardware, and install the front mounting brackets.

5. Install the shield on the new module. Place it over the two front mounting screws and front mounting brackets.

6. Install the four 8 mm nuts but leave them loose so the shield can move.

7. Use the special self-tapping screws (step 1) to fasten the top and side of the shield. They will be hard to start while they are tapping the holes. Be careful that excessive tightening does not strip the self- tapped holes.

8. Tighten the 8 mm nuts at the front of the module.

9. The rear bracket is two brackets connected together by shock mounting hardware. Remove the two screws that hold the bracket assembly to the rear of the inoperative module.

   THESE SCREWS ARE SPECIAL self-tapping screws that must be used for mounting the bracket assembly on the new display. Do not use them for any other purpose.

10. Mount the rear bracket assembly on the new module. The screws will be hard to start because they must self-tap the mounting holes. Be careful that excessive tightening does not strip the self-tapped holes.

11. Note the routing of the power cable and CRT Control cable and <u>one at a time</u>, remove them and install them on the new module.

12. Remove the wide flat ribbon cable from the old module and install it on the new one.

INSTALL NEW MODULE

13. Install the new module most of the way into the instrument. Avoid pinching cables as module is being installed.

14. Connect the power cable to the appropriate connector at the top front corner of the Primary Power Supply and slide module the rest of the way in.

15. Install, but do not tighten, the two rear and four front mounting screws (see figure 6A-6).

16. Install the front panel. Use the steps given in the front panel procedure except for steps 3, 2, and 1.

17. Push the module foreward, closing as much as possible the gap between the CRT and the bezel. Tighten the two rear and four front mounting screws.

18. Complete the rest of the instrument assembly by doing steps 3, 2, and 1 of the front panel procedure.

## 6A-13. Fans

### REMOVAL

1. Disconnect power cable.

2. Remove bottom rear feet and bottom cover.

3. Disconnect fan power cable from rear corner of Mother board.

4. Remove fan housing mounting screws as shown in the figure.

5. While noting fan cable routing, carefully remove fan housing from instrument.

6. Disconnect power cable connector from defective fan and remove fan from housing.

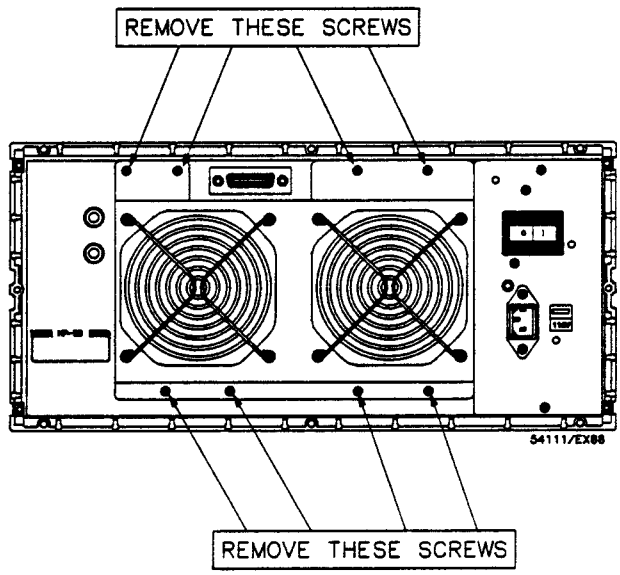



*Figure 6A-7. Fan Housing Mounting Screws.*

### REPLACEMENT

Reverse removal procedure to install fan. Be sure fan power cable does not get pinched between fan and rear panel.

## 6A-14. Color Display Assembly

### REMOVAL

1. Disconnect power cable.
2. Remove bottom rear feet and bottom cover.
3. Disconnect wide ribbon cable from Color Display assembly.
4. Remove assembly mounting screws as shown in the figure below.
5. Carefully lift board straight up to disengage Mother board connector.

**NOTE**

*The Display assembly to Mother Board connector will exhibit some removal resistance while the board is being removed. It is recommended the major lifting force be exerted on the edge of the Color Display Assembly at the connector.*

### REPLACEMENT

Reverse removal procedure to install assembly. Use additional care when inserting the connector pins into connector on Mother board.

**NOTE**

*Power for the Color Display Assembly is obtained from the Mother board via the four short mounting screws. Their positions are marked +5 and GD on the board. These mounting screws must be installed and tightened before proper operation of the instrument can be expected.*

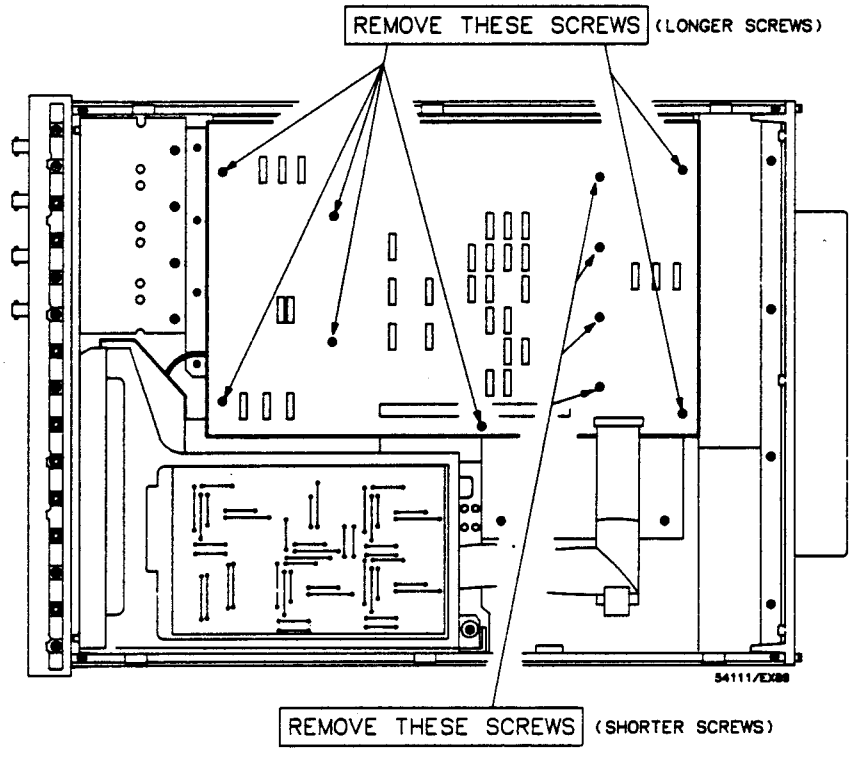



*Figure 6A-8. Color Display Assembly Mounting Screws.*

## 6A-15. Mother Board

### REMOVAL

1. Disconnect power cable.
2. Remove rear feet and all covers.
3. Remove all card cage PC boards (refer to earlier paragraph).
4. Remove Analog Power Supply and Digital Power Supply (refer to earlier paragraphs).
5. Remove Color Display Assembly (refer to earlier paragraph).
6. Disconnect fan power cable connector from corner of Mother board.
7. Loosen the STBY switch cable by removing the two nylon cable clamps from bottom of Mother board. Squeeze the clamps and pull them from the holes in the board.
8. Remove the remaining mounting screws and remove board (see figure below).

### REPLACEMENT

Reverse removal procedure to install board.

**NOTE**

*The Mother board and Display board share some of the same mounting screws. Therefore, when installing the Mother board install only the screws removed in step 8 above (shown in figure below).*

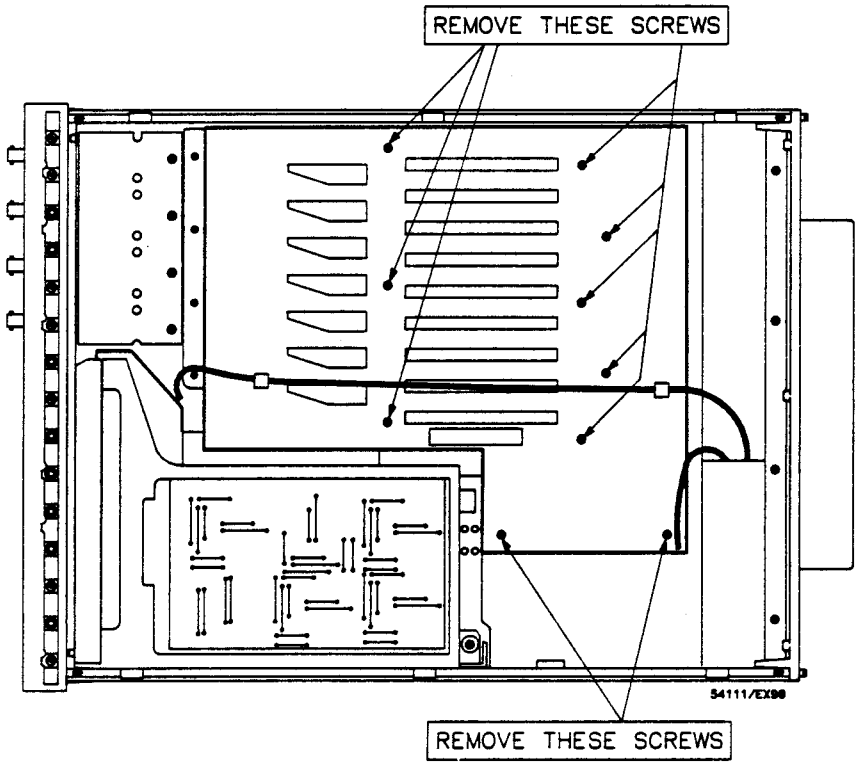



*Figure 6A-9. Mother Board Mounting Screws.*

## 6A-16. CABLING DIAGRAM

The following cabling diagram should be used when removing and replacing boards and assemblies.

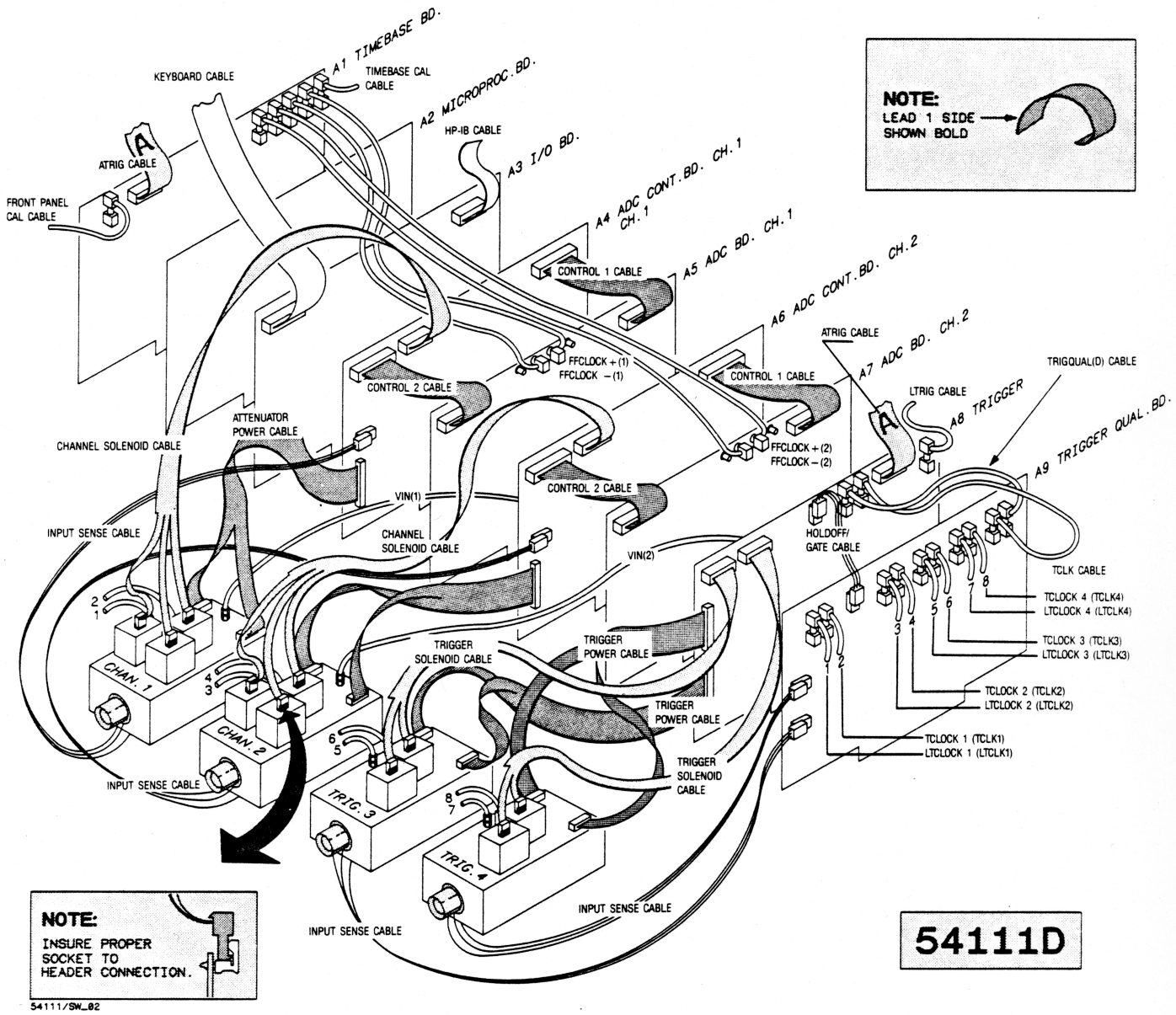



*Figure 6A-10. HP 54111D Cabling Diagram.*

# SECTION 6B
# THEORY OF OPERATION

## 6B-1. INSTRUMENT LEVEL THEORY

The HP 54111D is a digitizing oscilloscope with up to 1 GS/s sampling rate and 500 MHz repetitive bandwidth. It has two input channels, which are digitized and provide internal trigger. There are two additional external trigger channels.

The mainframe consists of power supplies, color monitor assembly, and display assembly. The card cage holds the acquisition system (except attenuators) as well as the Microprocessor assembly and Input/Output assembly.

The acquisition system consists of four attenuator assemblies (including two trigger attenuators), two Analog to Digital Converter (ADC) assemblies, two ADC Control assemblies, and the Trigger, Timebase, and Trigger Qualifier assemblies. The attenuators are located between the card cage and the front panel.

Refer to the Instrument Level Block Diagrams for the following discussion.

## 6B-2. TYPICAL DATA ACQUISITION CYCLE

The acquisition cycle begins on the Timebase assembly. Before the acquisition cycle begins, the RUN/HALT flip-flop is set to HALT. This forces the LRUN/HALT line high. The pre- and post-trigger delay times are then loaded into the timebase IC.

To begin the cycle, LRUN/HALT is brought low, and the timebase IC then asserts ARUN (Asynchrounous RUN). Data taking begins.

After two cycles of the pre-trigger delay clock, generated by the timebase IC, the pre-trigger delay counter begins counting down from its preloaded value. When it reaches zero, TRIG ARM is asserted by the Timebase.

The Timebase then waits for ATRIG to be asserted by the Trigger assembly, indicating that a trigger event has occurred. After ATRIG, the fine interpolator is started. The fine interpolator in the timebase IC counts until the fine interpolator gate ceases being asserted. This time interval is proportional to the amount of time between the trigger event and the next subsequent sample clock. The dual slope interpolator circuit has acted as a time-interval stretcher.

Two post-trigger delay clock counts after the fine interpolator control has been de-asserted by the timebase IC, the post-trigger delay counter begins counting down to zero. When it gets to zero data taking stops.

When the fine interpolator gate ceases being asserted by the dual slope interpolator, the processor reads the coarse and fine interpolation counters. Then it reads the contents of the interleaved A/D memory by rapidly advancing the memory to the beginning of the data, then single-stepping through it.

Acquired data is read sequentially from the four A/D memories (FISO) in a "round-robin" fashion, into RAM on the I/O assembly. After the FISOs are read, the Timebase IC asserts LIRQ1 and the microprocessor resets the Timebase IC by setting the LRUN/HALT flip-flop to HALT.

The cycle then repeats.

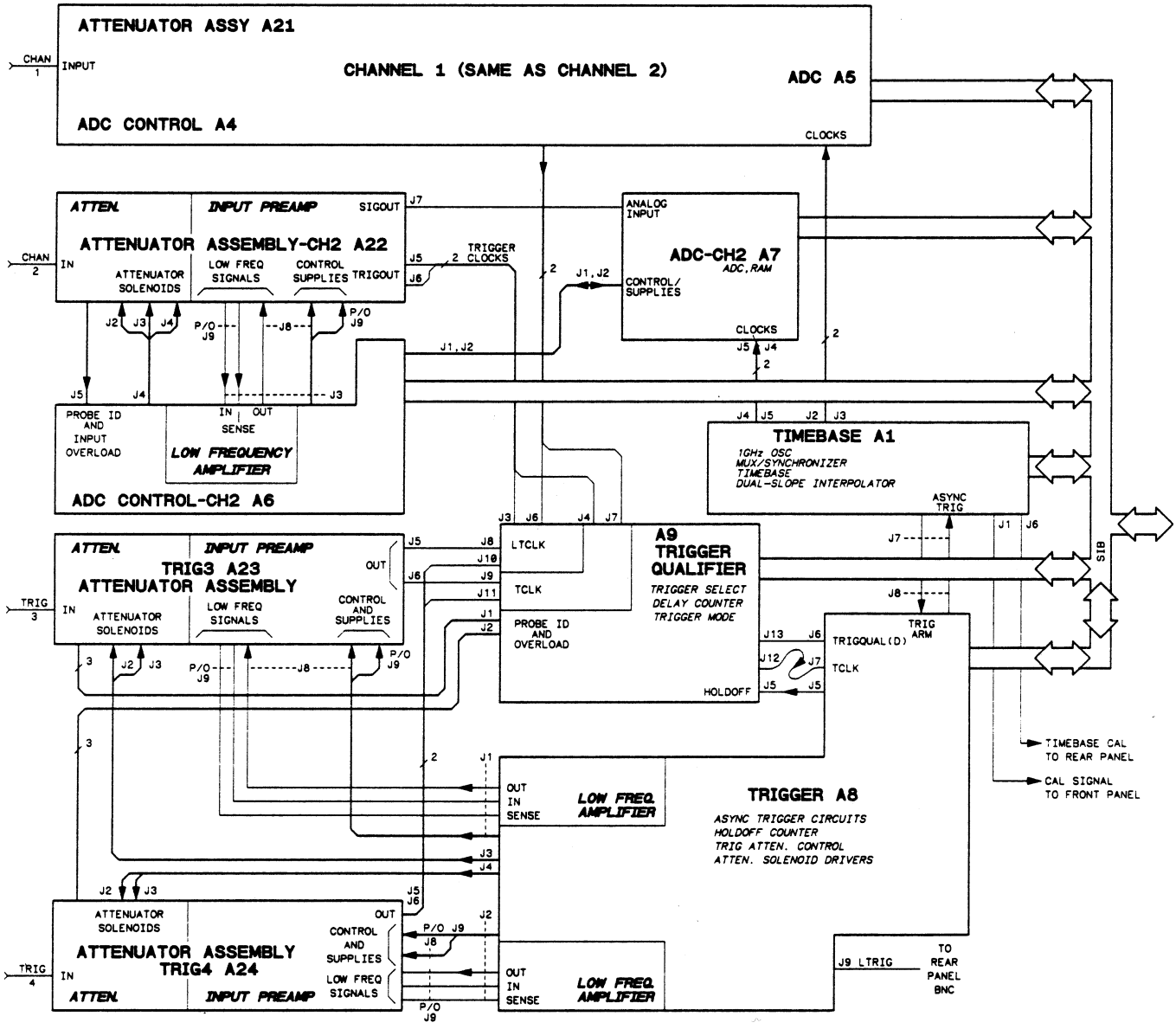



*Figure 6B-1. Instrument Block Diagram, Acquisition System*

## 6B-3. Acquisition

Channel 1 acquisition is identical to channel 2 acquisition. Use the Instrument Block Diagram, Acquisition System, for reference.

**CHANNEL ATTENUATOR.** The channel attenuator provides signal conditioning between the front panel channel input and the analog-to- digital converter. The outputs are a ±0.64 V single-ended signal, representative of the input signal, and two complementary trigger signals whose edges represent the desired trigger point for the channel. The ADC Control provides power supplies, control signals, and the low frequency amplifier, and it receives the probe ID and input overload signals.

**ANALOG-TO-DIGITAL CONVERTER.** The Analog-to-Digital Converter (ADC) digitizes and stores the channel input signals. It gets control and supplies from the ADC Control and sample clocks from the Timebase. The ADC flash converter outputs into FISO (fast in/slow out) sequential memory and the output from memory goes to the system interface bus (SIB).

**ADC CONTROL.** The ADC Control provides control for the attenuator and ADC assemblies. Interface to the SIB provides the control. Supply voltages are developed for the attenuator and ADC assemblies. The ADC Control carries the low frequency amplifier for the attenuator assembly.

## 6B-4. Triggering and Sample Clocking

**TRIGGER ATTENUATORS.** The trigger attenuator assemblies provide nearly the same functions as the channel attenuator assemblies. Part of the attenuator section is not used and the signal output is not used. The complementary trigger signals, probe ID, and overload are sent to the Trigger Qualifier. The Trigger provides the low frequency amplifier, control signals, and power supplies.

**TRIGGER QUALIFIER.** The Trigger Qualifier uses the trigger signals from the channel and trigger attenuator assemblies to provide edge and pattern recognition. Trigger delay circuitry is also a part of the Trigger Qualifier. HOLDOFF is an input from the Trigger. The Trigger Qualifier develops TCLK (trigger clock) and TRIGQUAL (D) (trigger qualifier) for the Trigger circuits. Probe ID and overload signals are inputs from the attenuator assemblies to the Trigger Qualifier.

**TRIGGER.** The Trigger provides the asynchronous trigger to the Timebase. Asynchronous trigger provides a time reference for, or terminates (after a time delay), the data acquisition.

TCLK clocks TRIGQUAL(D) (trigger qualifier) through the trigger circuitry. If holdoff is being used, as soon as a trigger occurs the holdoff counter (by events or time) disables the trigger circuitry until the counter times out.

The Trigger assembly includes the control circuitry and supplies for the trigger attenuators and low frequency amplifiers.

**TIMEBASE.** The Timebase generates the sample clocks for the ADC assembly. A 1 GHz oscillator provides the base sample rate. Frequency dividers provide sample rates down to 50 Hz. The trigger interpolator measures the time from the trigger to each sample when repetitive sampling is used.

After the pre-trigger delay, TRIGARM (trigger arm) enables the ATRIG signal to reach the timebase.

The Timebase provides a vertical calibration signal to a connector on the front panel. It provides either of two signals to a rear panel BNC. When the instrument is running in the acquisition modes, the signal is 500 KHz referenced to the system clock. In Timebase Cal mode it is 50 MHz referenced to the acquisition clock. In a small group of early instruments the rear panel signal is always referenced to the acquisition clock and varies with the sample rate.

## 6B-5. Instrument Control

Use the Instrument Block Diagram, Mainframe, for reference.

**MICROPROCESSOR.** The Microprocessor uses a 68000 16-bit processor to handle all processing on the system interface bus (SIB). The assembly includes 512K bytes of ROM and 32K bytes of non-volitile CMOS RAM. Bus buffers, interrupt logic, a time-out counter, and a bus arbitration circuit are part of the Microprocessor assembly. Because of the single controller in the HP 54111D, the bus arbitration circuitry is not used.

**INPUT/OUTPUT.** The Input/Output (I/O) assembly combines several functions on one PC board. The dynamic RAM on this assembly is used for basic operation of the instrument and to store waveforms. The keyboard control provides scanning and reading of the three keyboards and RPG (rotary pulse generator). The HP-IB interface couples the system interface bus (SIB) to the HP-IB port on the rear panel. An oscillator and divider circuit provides 16, 8, 4, and 2 MHz clocks for the system. The battery back-up provides battery power to the non-volitile RAM on the microprocessor assembly. The Power Test circuitry monitors the supplies on the SIB. The output of the circuit is a status bit that the microprocessor reads. If all supplies are greater than 50% it registers as passing. The Power-On Reset provides a glitch-free reset pulse to the SIB for use by any circuitry on the bus.

**FRONT PANEL ASSEMBLIES.** Front panel assemblies include three keyboards, an RPG (rotary pulse generator), and the Display Control. The Control Keyboard allows direct entry of values into the field selected on the CRT. The Function and Menu keyboards, to the right of and below the CRT respectively, give control of functions noted on the display. The RPG provides the digital equivalent of a potentiometer as well as sequential stepping through incremental functions. The Display Control provides analog brightness and background control of the display.

**COLOR DISPLAY ASSEMBLY.** The Color Display Assembly provides interface between the SIB and the Color CRT Module. It includes graphics RAM, character generation, and RGB generation. Horizontal sync, vertical sync, and blanking also drive the Color CRT Module.

**COLOR CRT MODULE.** The Color CRT Module includes the color CRT and its associated driving circuitry. It uses H and V sync, blanking, and red, green, and blue video from the Color Display assembly. The Color CRT Module is considered one replaceable part.

## 6B-6. Power Supplies

**PRIMARY SUPPLY.** The Primary supply provides an unregulated 300Vdc primary voltage to the switching supplies. It can be set for 115 or 230 V line input (-25%, +15%). A circuit breaker provides rear panel switching of the line input. The STBY (standby) switch on the front panel controls a 120 Vdc switching regulator which supplies the Color CRT Module as well as an on/off control voltage to the Analog and Digital supplies.

**DIGITAL SUPPLY.** The Digital Supply switching regulator provides +5 V and -5.2 V to most of the digital circuitry. It uses the 300 Vdc primary from the Primary Supply and is controlled (on/off) by an output from the 120 V Supply. These supplies are designated +5 and -5 on the SIB and are referenced to DGND of the SIB.

**ANALOG SUPPLY.** The Analog Supply switching regulator provides ±8.5 Vdc and ±18.5 Vdc to much of the analog circuitry. It uses the 300 Vdc primary from the Primary Supply and is controlled (on/off) by an output from the 120 V Supply. Many of the assemblies in the instrument use local regulation of these supplies to provide decoupling from system noise. These supplies are designated ±8 and ±18 on the SIB and are referenced to AGND of the SIB.

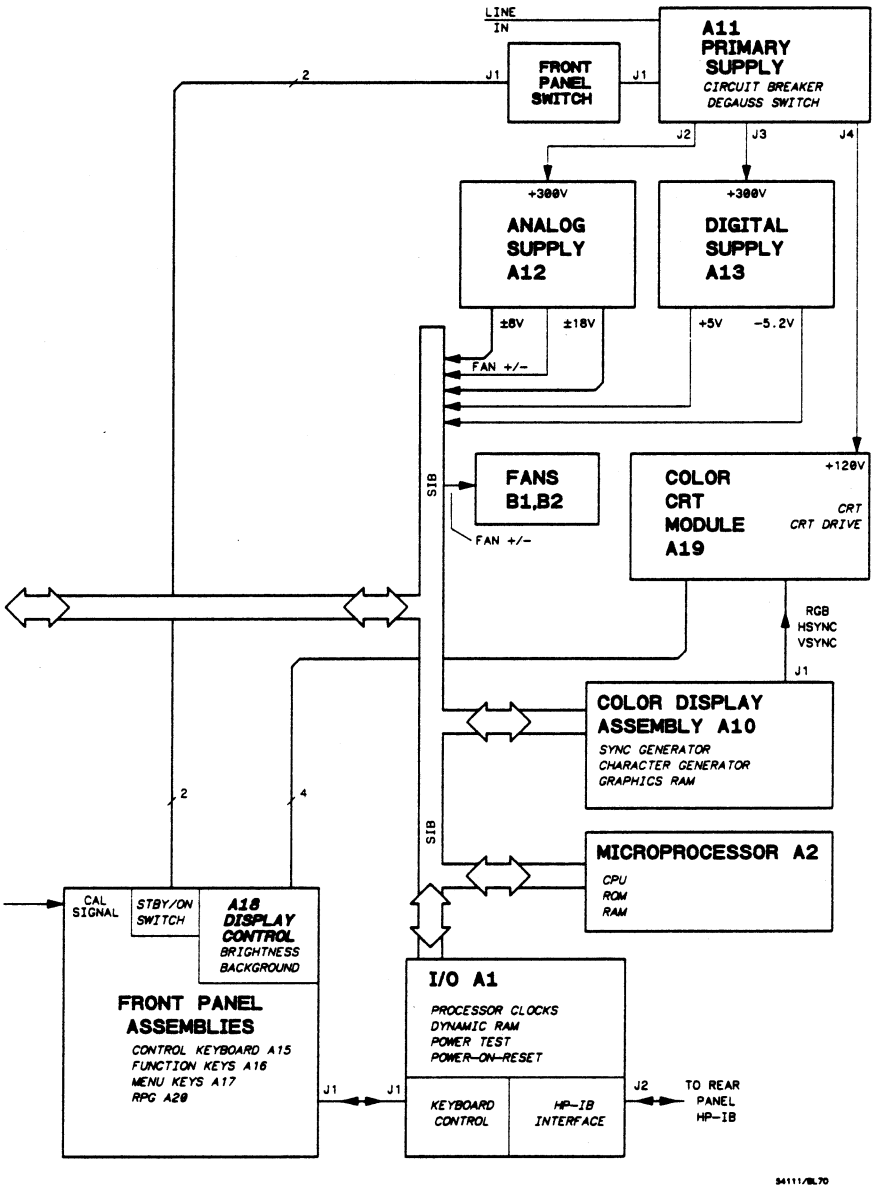



*Figure 6B-2. Instrument Block Diagram, Mainframe*

## 6B-7. ATTENUATOR ASSEMBLY THEORY

## 6B-8. Channel Attenuators

The Channel Attenuator assemblies consist of two main sections, the attenuator and the preamplifier. The Channel Attenuator assemblies get power and control from the ADC Control assembly for their respective channel. Refer to the Attenuator Assembly Block Diagram for the following discussion.

**INPUT ATTENUATOR.** The input attenuator section provides 50Ω or 1MΩ impedance switching and two ÷10 sections which can be cascaded for ÷100. Magnetically latching solenoids control the switching. A ring on the input BNC connector provides means for identifying high impedance 10:1 voltage divider probes. A sample of the input signal from a tap on the 50Ω input termination is used to control an overload protection circuit. The microprocessor removes the 50Ω termination if the input is overloaded.

**PREAMPLIFIER.** The preamplifier hybrid consists of several sections, a high-pass filter and FET and associated circuitry, the main preamplifier with trigger circuitry, the driver amplifier, and a differential-to-single converter.

At the input to the preamp, the low frequency component of the input signal is sent to the low frequency amplifier on the ADC Control assembly. AC/DC coupling and DC offset are incorporated in the low frequency amplifier.

Upon return to the attenuator assembly, the low frequency and high frequency signals are recombined and fed to the input FET of the preamplifier. The preamplifier incorporates most of the gain changing and the trigger conditioning. Three incremental gain ranges, ÷1, ÷2, and ÷4 affect the signal before trigger pick-off. Vernier gain affects the signal after trigger pick-off. Other signals control trigger functions.

The output of the preamplifier chip is fed to the driver chip. The gain of the driver can be increased by a factor of five for increased sensitivity.

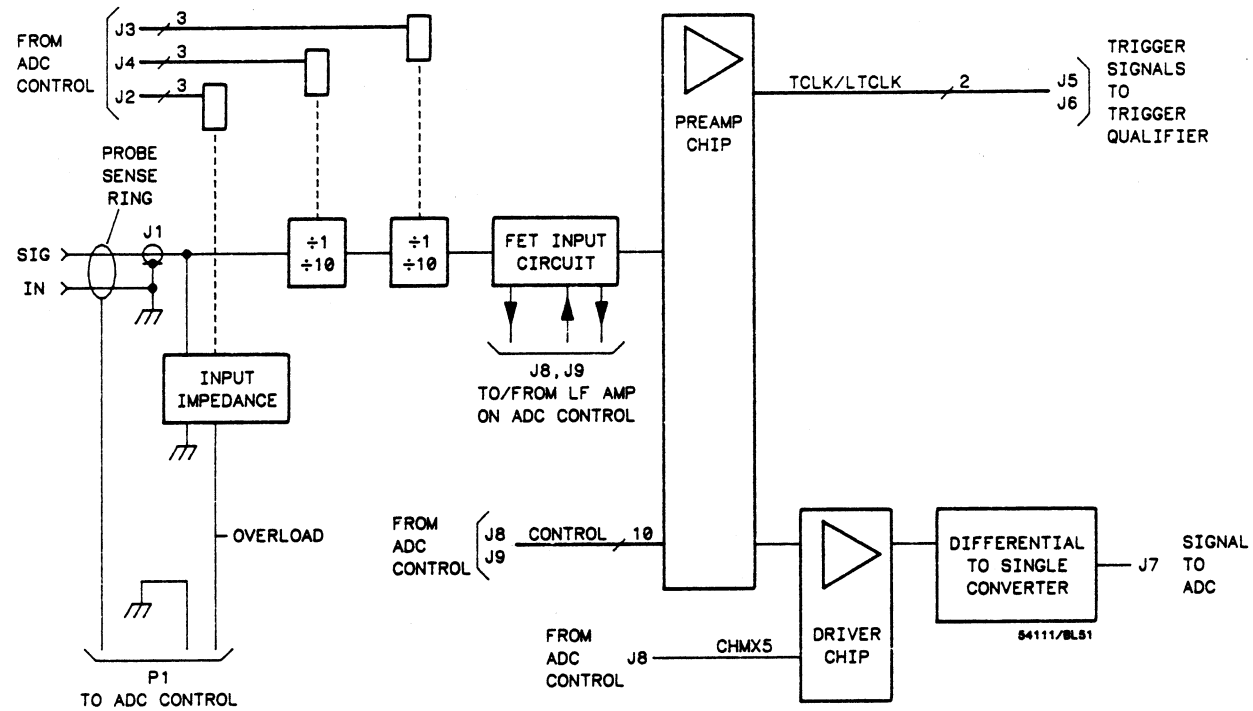
The output of the driver feeds the differential-to-single converter. The output of the converter is a coaxial connector which is connected by cable to the ADC assembly and analog-to-digital converter hybrid.

The trigger signals are two complementary signals whose edges represent the selected trigger point of the input signal. They are conducted via two coaxial cables to the Trigger Qualifier assembly.

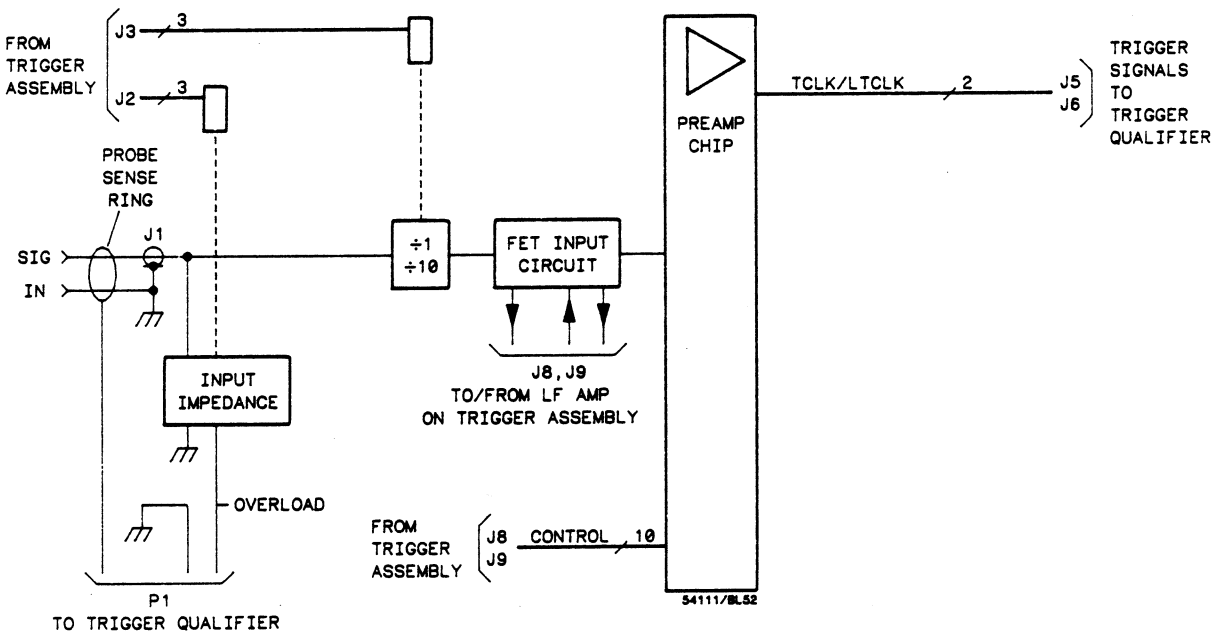
## 6B-9. Trigger Attenuators

The Trigger Attenuator assemblies are nearly the same as the Channel Attenuator assemblies. There are two major differences. First, there is a single divide-by-ten function at the attenuator input. Second, there is no main signal output. Only the two trigger signals are used. Also, the preamplifier is kept in the ÷4 gain mode.

Both Trigger Attenuator assemblies get power and control from the Trigger assembly. The low frequency amplifiers are also on the Trigger assembly. The trigger signals, probe ID, and input overload signals are sent to the Trigger Qualifier assembly.




CHANNEL ATTENUATOR ASSEMBLY BLOCK DIAGRAM




TRIGGER ATTENUATOR ASSEMBLY BLOCK DIAGRAM

*Figure 6B-3. Attenuator Assembly Block Diagrams*

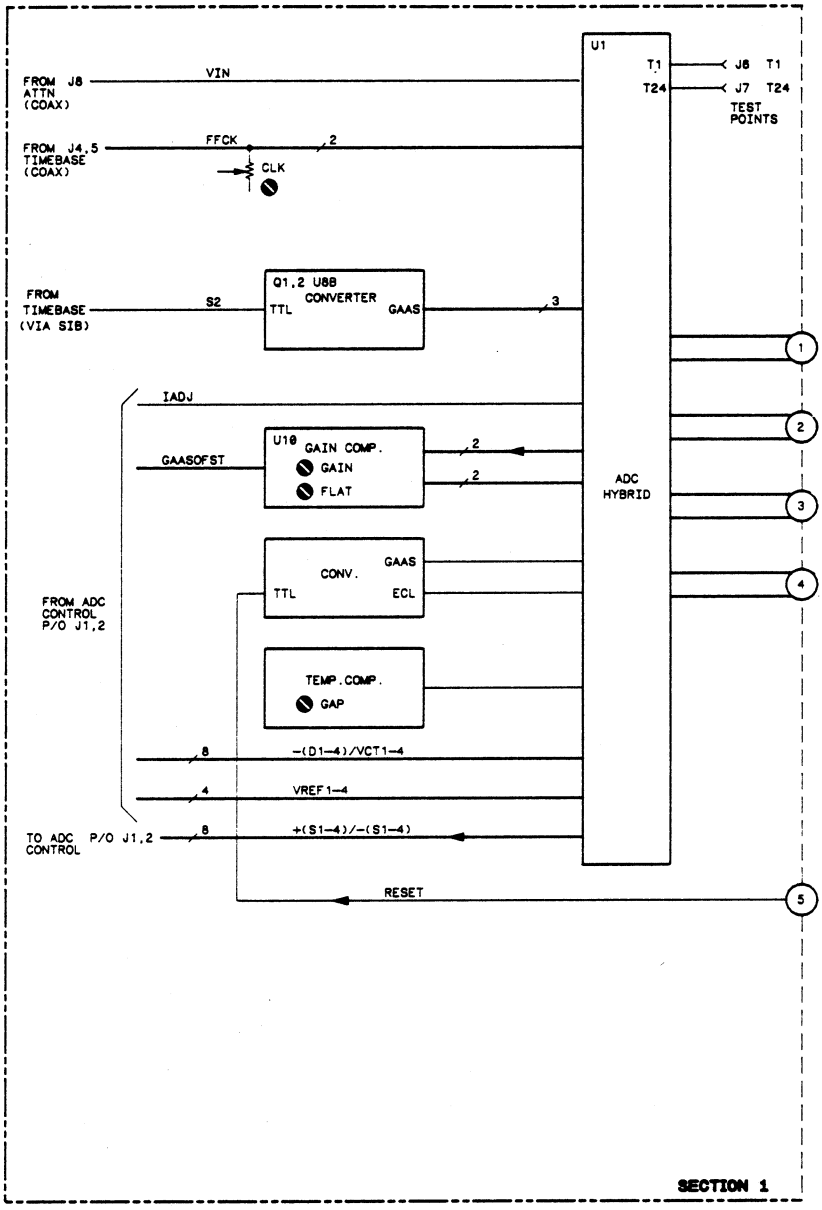



*Figure 6B-4. ADC Assembly Block Diagram (part 1)*

## 6B-10. ADC ASSEMBLY THEORY

The Analog-to-Digital Converter (ADC) assembly samples one channel input signal and stores it in memory.

Use the Analog-to-Digital Converter Assembly Block Diagram for the following discussion. The block diagram is laid out in two sections, corresponding to the two schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

### Section 1

The ADC hybrid is a multi function part. The input signal to each channel is sampled using a GaAs diode sampling bridge. The output of this sampler is distributed to four second-rank samplers, each of which drives a six bit flash ADC. These six bit converters run in four phaases at rates of up to 250 MSa/s, one fourth the sample rate. Each converter outputs gray-code data to one memory IC.

Each flash converter consists of an array of comparators, of which one input of each is connected to the input signal, and the other input is connected to a tap on an accurate voltage divider stick. A reference voltage is applied to the divider stick. At the time of the sample, the outputs of the comparators are latched. The amplitude of the signal determines which comparator outputs were high or low and logic circuitry then converts the comparator outputs to a 6-bit binary gray code.

VIN, the analog signal input, comes through a coaxial cable from the attenuator assembly. FFCK+/-, the complementary sample clocks, come from the Timebase assembly through coaxial cables. The CLK adjustment sets the differential offset. S2 is a control signal, also supplied by the Timebase. It is converted from TTL to GaAs levels by Q1, Q2, and part of U8. The RESET signal comes from the Timebase via the SIB and Section 2 of the block diagram.

The rest of the ADC support circuitry controls dc levels in the hybrid. The source for external input is the ADC control assembly. There is temperature compensation and four adjustments. For control of the voltage divider sticks there are 12 inputs from and eight outputs to the ADC control assembly.

The output of the ADC hybrid is four sets of 6-bit data, each set with its own clock. Each data bit and clock is a complementary signal pair, so there are 14 lines for each data set.

## Section 2

The FISO (fast in, slow out) memory is 2K bytes (16K bits). It is written and read serially. Each memory IC stores data from one of the four flash converters in the ADC hybrid. Seven pairs of complementary signals, six data bits and a clock, write data into one memory IC at one fourth the sample rate. The memory is eight bits wide. The remaining two data bits are used for a dither function.

Data is read from memory using the same clock signals, but at a rate compatible with the microprocessor. The outputs of the memories are paralleled and are run through a gray-to-binary code converter. The output of the converter is buffered onto the lower byte of the SIB data bus. The Timebase assembly puts "0"s on the upper byte of the data bus.

The Control Data Latch latches FISO control signals from the upper byte of the SIB. ADCR/LW, ADCRST, and LADCMEMRD control read/write and reset of the memory. ADCRST is also used to reset the ADC hybrid and FISO memory.

The circulating clock, FISOPHA-D, synchronizes reading data out of the memory. The microprocessor can read them to determine which FISO is being read.

## DITHERING

As the information is read from the four ADCs, a digital bias is applied at the input of the FISO memory. That is, the data from each converter is augmented from six to eight bits, these least significant bits being either 00, 01, 10, or 11 (in straight code). The resulting eight bit words are then passed through a six, seven, or eight-bit filter, resulting in a certain amount of bandwidth and S/N ratio for each filter. This process is called dithering.

If the signal is significantly oversampled, eight effective bits of resolution can be achieved at bandwidths of up to 25 MHz single-shot with 1 GSa/s sampling.

Without going into the mathematical detail of how dithering works, it effectively moves the thresholds of each A/D converter, making each converter's thresholds 1/4 LSB different from the the one before it. This small noise signal is then filtered out by the chosen interpolation filter. The result is better resolution out of the same number of hardware bits.

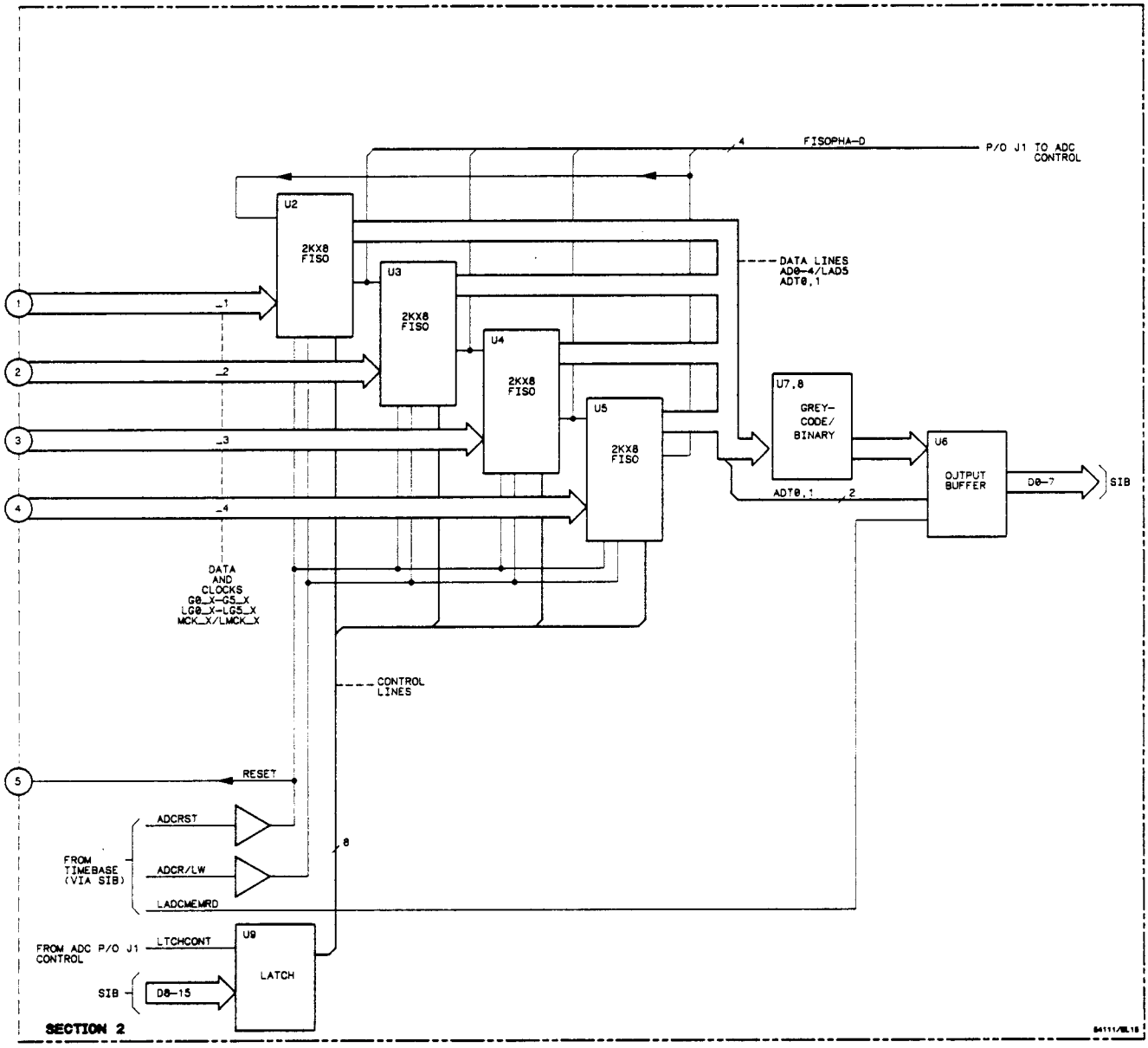



*Figure 6B-5. ADC Assembly Block Diagram (part 2)*

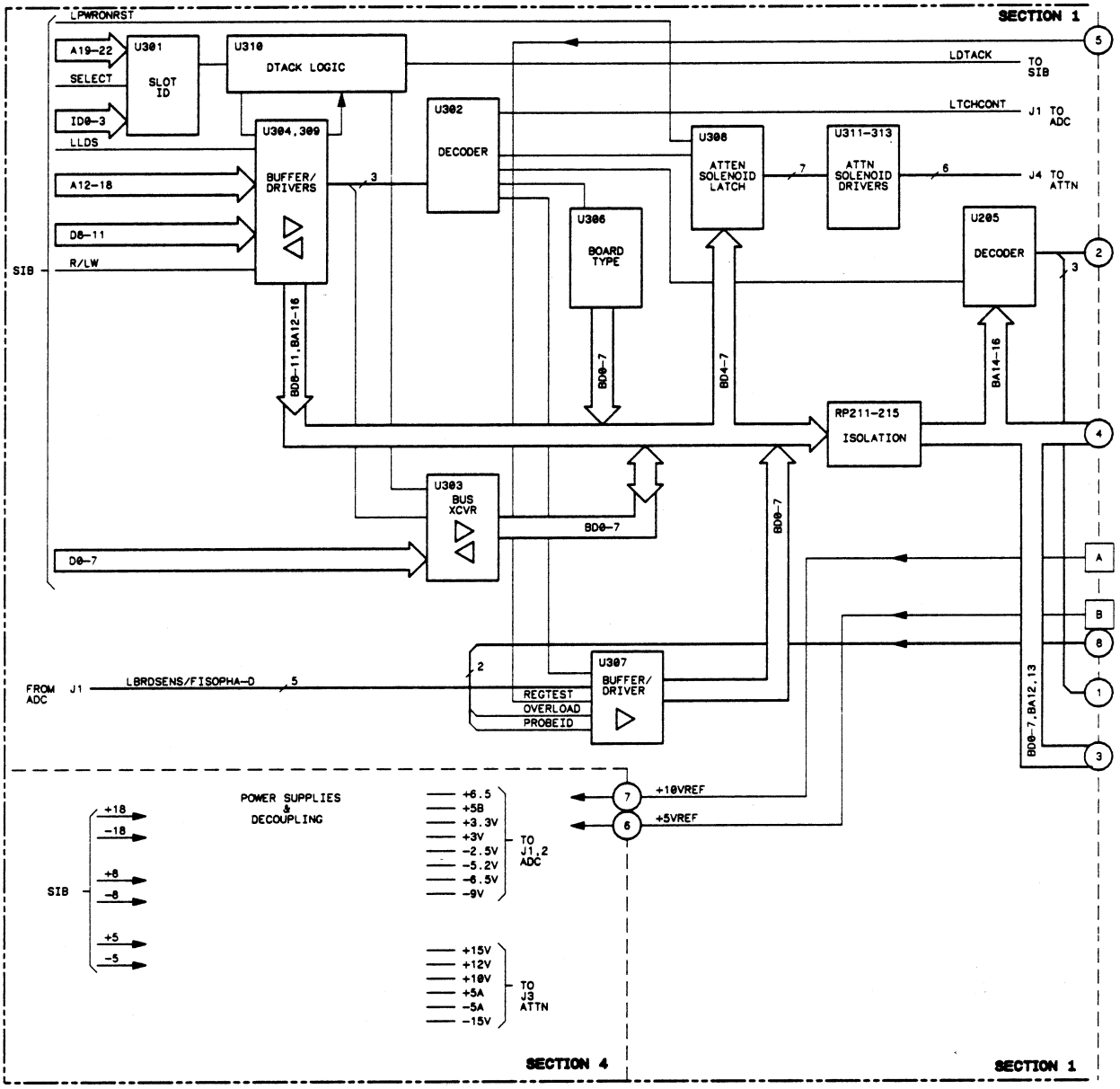



*Figure 6B-6. ADC Control Assembly Block Diagram (part 1)*

## 6B-11. ADC CONTROL ASSEMBLY THEORY

The ADC Control assembly provides supplies and most of the control for the Analog-to-Digital Converter (ADC) assembly.

Use the ADC Control Assembly Block Diagram for the following discussion. The block diagram is laid out in four sections, corresponding to the four schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

### Section 1

**SLOT ID.** U301 is a 4 bit comparator which compares address lines A19-22 with slot ID codes ID0-3. Slots are made unique by grounding appropriate pins at the mother board connector. Slots are numbered 0000 to 1001 from left to right. When the slot this assembly is in is addressed, the two codes are equal and U301 output goes high, enabling other circuitry.

**DTACK LOGIC.** Data transfer acknowledge circuitry buffers the output of the slot ID and develops the LDTACK signal.

**BUFFER/DRIVERS.** U304 and U309 improve the fan-in of several signals to prevent loading of the SIB.

**DECODER U302.** With address lines A17 and A18 and the R/LW line, U302 decodes read and write functions of this assembly.

**BOARD TYPE.** When board type is requested by the microprocessor, this assembly responds with a code over the data bus. The input pins of buffer U305 are encoded with the board type. Enabling U305 reads the code.

**ATTENUATOR SOLENOID LATCH.** U308 latches the channel attenuator setup data. This sets the attenuator input impedance and division ratio. A low on the LPWRONRST line keeps the driver circuitry from changing the attenuators during power-up.

**ATTENUATOR SOLENOID DRIVERS.** The solenoid drivers provide drive signals to input impedance and division ratio solenoids on the channel attenuators. The solenoids are magnetically latched, so only a short duration signal is needed to change settings.

**DECODER U205.** This decoder provides control signals for DACs and latches in the analog control circuitry.

**ISOLATION.** Resistors in the address and data lines isolate the analog circuitry from the digital circuitry.

**BUS TRANSCEIVER.** U303 buffers read/write data from/to the data bus of the SIB.

**BUFFER/DRIVER U307.** U307 buffers several signals from this assembly and the ADC assembly, onto the lower byte of the data bus.

### Section 4

Several power supply voltages are generated on this assembly. They use the supplies from the SIB and isolate circuitry on this assembly from the rest of the system. They also supply all the voltages for the ADC assembly and the channel attenuator.

## Section 2

Circuitry in this section controls the channel attenuator preamplifiers and part of the ADC. The low frequency amplifier for the attenuator preamp is also included here.

**LATCHES U203/U204.** U204 latches data from the data bus for control of the channel attenuator preamp. The output of U203 are also ANDed in U206 for test purposes. U203 latches data for control of circuitry in this section.

**REGISTER TEST.** Outputs from U203 and U204 are ANDed in U206 for internal testing purposes.

**TRIGGER LEVEL DAC.** This DAC provides a trigger level signal to the attenuator preamp. The bilateral switch in its output changes the trigger level range.

**CAL/OFFSET DAC.** This DAC provides the channel offset signal during acquisition and a calibration voltage during calibration procedures initiated by firmware. The reference output is also used for other purposes on this assembly and the attenuator preamp.

**QUAD DAC.** The quad DAC provides four analog signals. Two signals are for the ADC hybrid on the ADC assembly, one controls the attenuator vernier and the other controls the trigger sensitivity.

**LOW FREQUENCY AMP.** The low frequency amplifier is part of the input signal path. The low frequency component of the signal is picked off, amplified, and reinserted between the ÷10 attenuators and the preamp hybrid of the attenuator assembly. The ac/dc coupling and offset functions are accomplished in the low frequency amplifier.

**PROBE ID/INPUT OVERLOAD.** A sense ring at the input BNC identifies when a standard 10:1 probe is being used. The instrument automatically adjusts the vertical scaling to suit. A line from the channel attenuator monitors the signal on the 50Ω input termination resistor. The overload circuit provides an interrupt to the microprocessor over the IRQ2 line and a flag onto the data bus. Once the overload is cleared, the microprocessor sends a reset signal through U205 (section 1) which resets the sense circuit.

## Section 3

This section controls the divider sticks of the flash converter ADCs (see ADC assembly theory). There are four sets of control circuitry, one for each divider stick. Two quad DACs and a latch, controlled by calibration routines, set up the levels on the sticks.

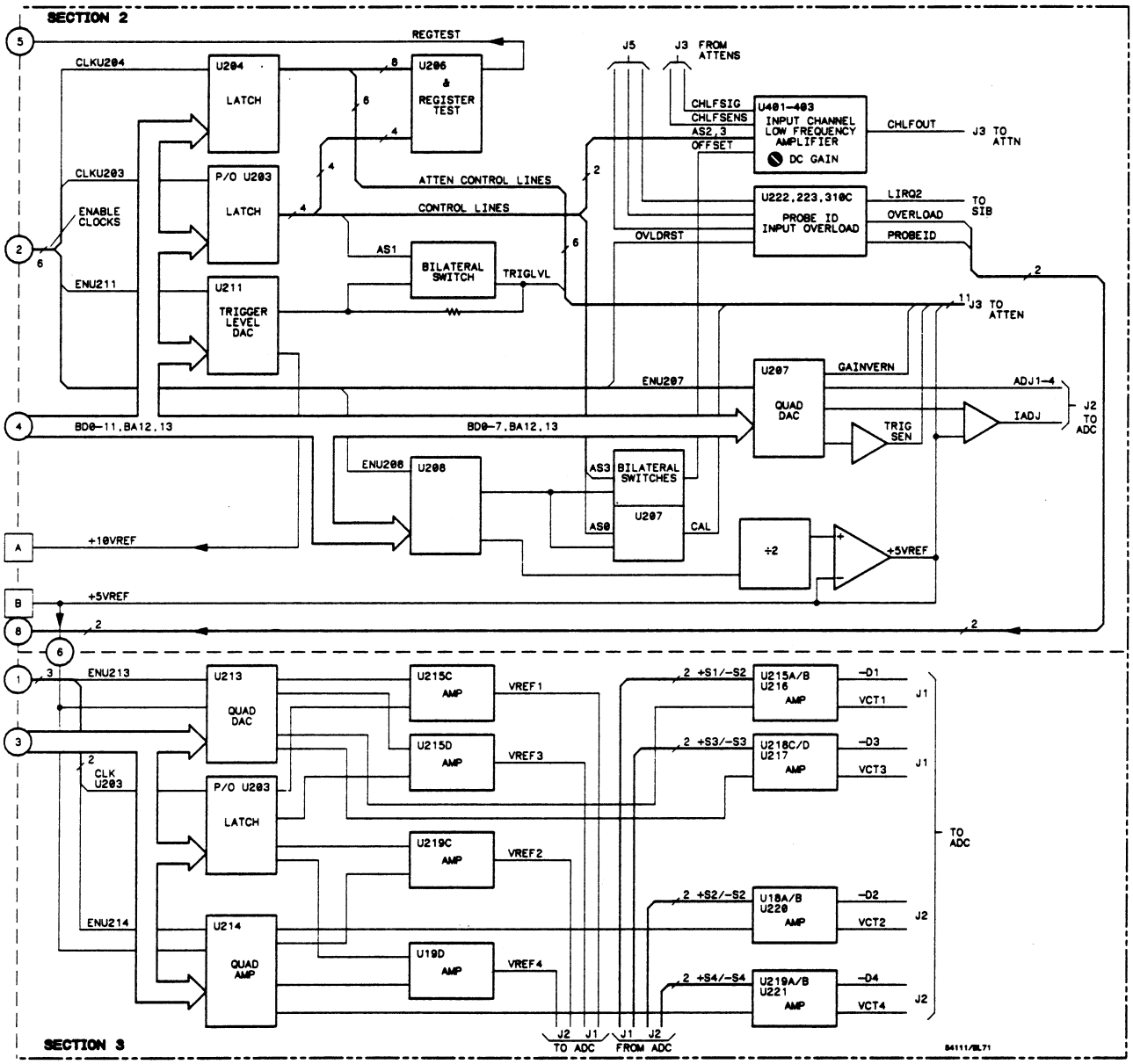



*Figure 6B-7. ADC Control Assembly Block Diagram (part 2)*

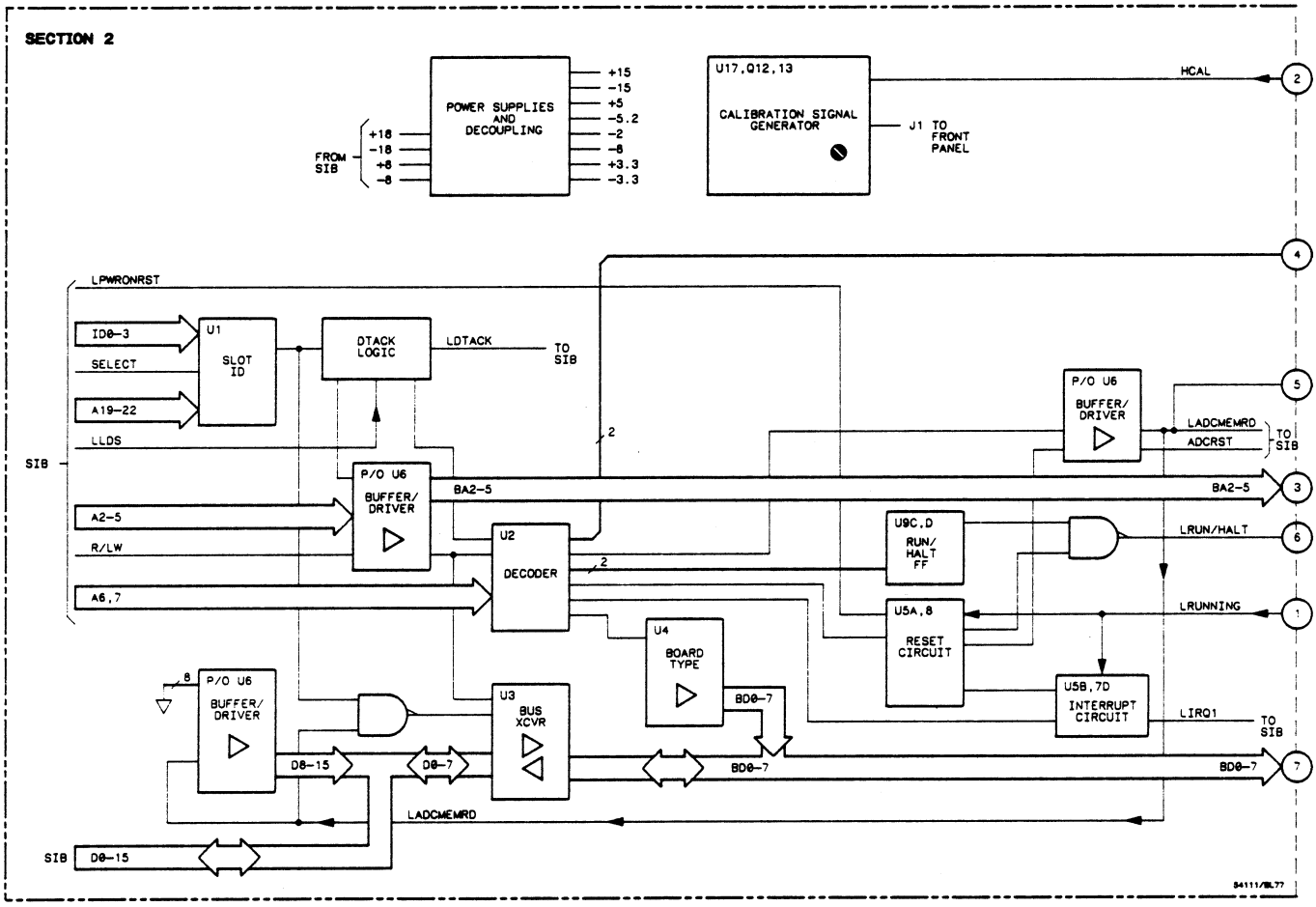



*Figure 6B-8. Timebase Assembly Block Diagram (part 1)*

## 6B-12. TIMEBASE ASSEMBLY THEORY

The Timebase assembly provides the acquisition sample clock. It provides several control signals to the Trigger and ADC assemblies as well as several other outputs.

Use the Timebase Assembly Block Diagram for the following discussion. The block diagram is laid out in two sections, corresponding to the two schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

### Section 2

Circuitry in section two provides control for the timebase and part of the ADC.

**SLOT ID.** U1 is a 4 bit comparator which compares address lines A19-22 with slot ID codes ID0-3. Slots are made unique by grounding appropriate pins at the mother board connector. Slots are numbered 0000 to 1001 from left to right. When the slot this assembly is in is addressed, the two codes are equal and U1 output goes high, enabling other circuitry.

**DTACK LOGIC.** Data Transfer Acknowledge circuitry buffers the output of the slot ID and develops the LDTACK signal.

**BUFFER/DRIVER U6.** U6 improves the fan-in of several signals to prevent loading of the SIB. It also buffers the memory read and ADCRST signals.

**DECODER.** With address lines A6 and A7 and the R/LW line, U2 decodes read and write functions of this assembly.

**BUFFER/DRIVER U10.** When the acquisition data is being read from the FISO memory onto the lower byte of the SIB data bus, U10 puts all zeros on the upper byte of the bus.

**BUS TRANSCEIVER.** U303 buffers read/write data from/to the data bus of the SIB.

**BOARD TYPE.** When board type is requested by the microprocessor, this assembly responds with a code over the data bus. The input pins of buffer U4 are encoded with the board type. Enabling U4 reads the code.

**RUN/HALT F-F.** The run/halt flip-flop uses two lines of decoder U2 to enable or disable the LRUN/HALT signal.

**RESET CIRCUIT.** The reset circuit provides a timed reset sequence for the acquisition system.

**INTERRUPT CIRCUIT.** The interrupt circuit drives the LIRQ2 line on the SIB.

**POWER SUPPLIES.** Several power supplies use the SIB power buses to derive specialized operating voltages for the circuitry in section 1. They also isolate this circuitry from the rest of the instrument environment.

**CALIBRATION SIGNAL GENERATOR.** This 2 KHz oscillator provides a square-wave signal to the front panel. When the instrument is in the Timebase Cal mode the output is forced high and the amplitude can be measured or adjusted to 0.8000 Vdc.

On some earlier instruments the signal is forced high by another method.

## Section 1

Circuitry in section one develops the acquisition sample clock. It also does the trigger interpolation.

During sampling, acquired data must be correlated to the trigger point. Each acquisition cycle has a different relationship to the trigger. Correlation is done by the trigger interpolator. It makes a high precision time interval measurement which is used to position the acquired data.

**1 GHZ OSCILLATOR.** The 1 GHZ oscillator uses a SAWR (surface acoustic wave resonator) to generate the basic acquisition sample clock.

**MUX/SYNCHRO.** The multiplexer/synchronizer IC provides the high frequency division ratios for the acquisition sample clock. Sample rates developed here are 1 GHz, 500 MHz, and 250 MHz. A 100 MHz output goes to the timebase IC for further division.

**TIMEBASE IC.** The timebase IC is a multifunction IC. It provides the majority of the sample clock rates, from 100 MHz down to 50 Hz. It divides the 100 MHz output of the multiplexer/synchronizer IC in a 1, 2, 4, 10 sequence. It feeds the divided rate back into the mux/synchro for output to the ADC assembly. It also provides counters and gating for coarse and fine interpolators and the pre- and post-trigger delay counters.

**FINE INTERPOLATOR.** The trigger interpolator consists of coarse and fine interpolators. The coarse interpolator is part of the timebase IC. The fine interpolator uses a dual slope technique to increase the accuracy of the time interval measurement. It is gated by the timebase IC and its output controls a counter in the timebase IC.

**TEST SIGNAL LOGIC.** This circuitry is a multiplexer and divider combination that selects one of two signals and outputs them to the rear panel. HCAL from the timebase IC selects the signal. When the instrument is in an acquisition mode, the rear panel output is the 2 MHz system clock from the SIB divided by four. When the instrument is in the Timebase CAL mode, the output is the 100 MHz output of the timebase IC divided by two.

HCAL from the timebase IC also controls the Calibration Signal Generator. When the instrument is in the Timebase Cal mode, HCAL forces the front panel CAL signal to 0.8 Vdc so that it can be measured or adjusted during performance tests or adjustment procedures respectively.

On a few earlier instruments the above circuitry is different. The rear panel signal is only a signal that is a divide-by-two function of the sample rate and the front panel CAL signal is forced high by another method.

**LOGIC U14.** Several signals are combined to develop S2, a signal that controls the high/low frequency modes of the ADC hybrid.

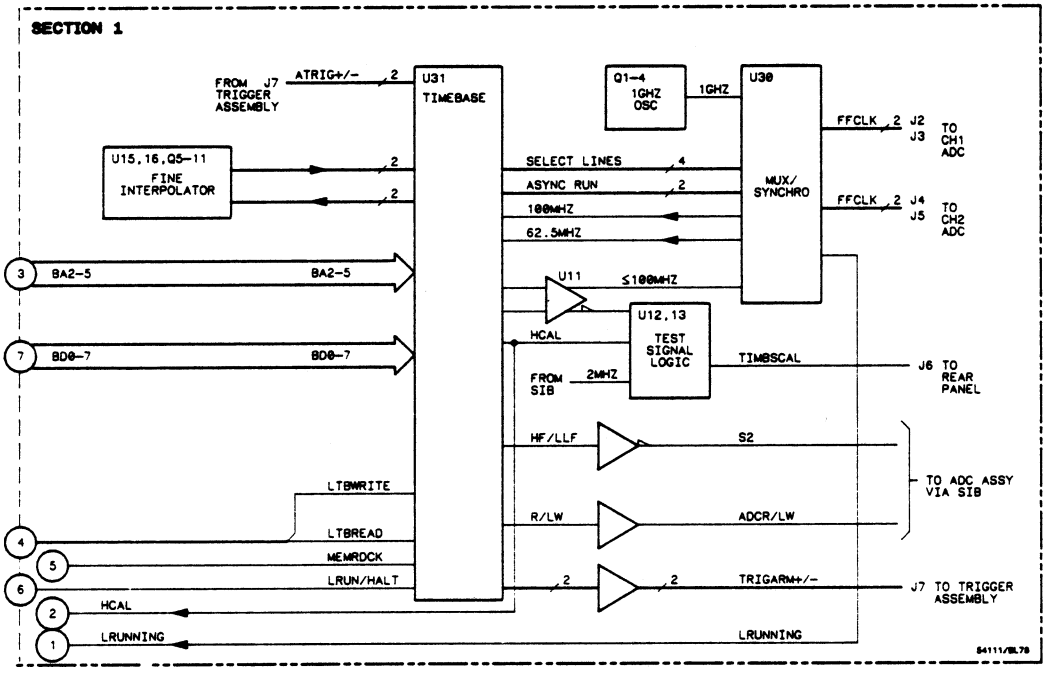



*Figure 6B-9. Timebase Assembly Block Diagram (part 2)*

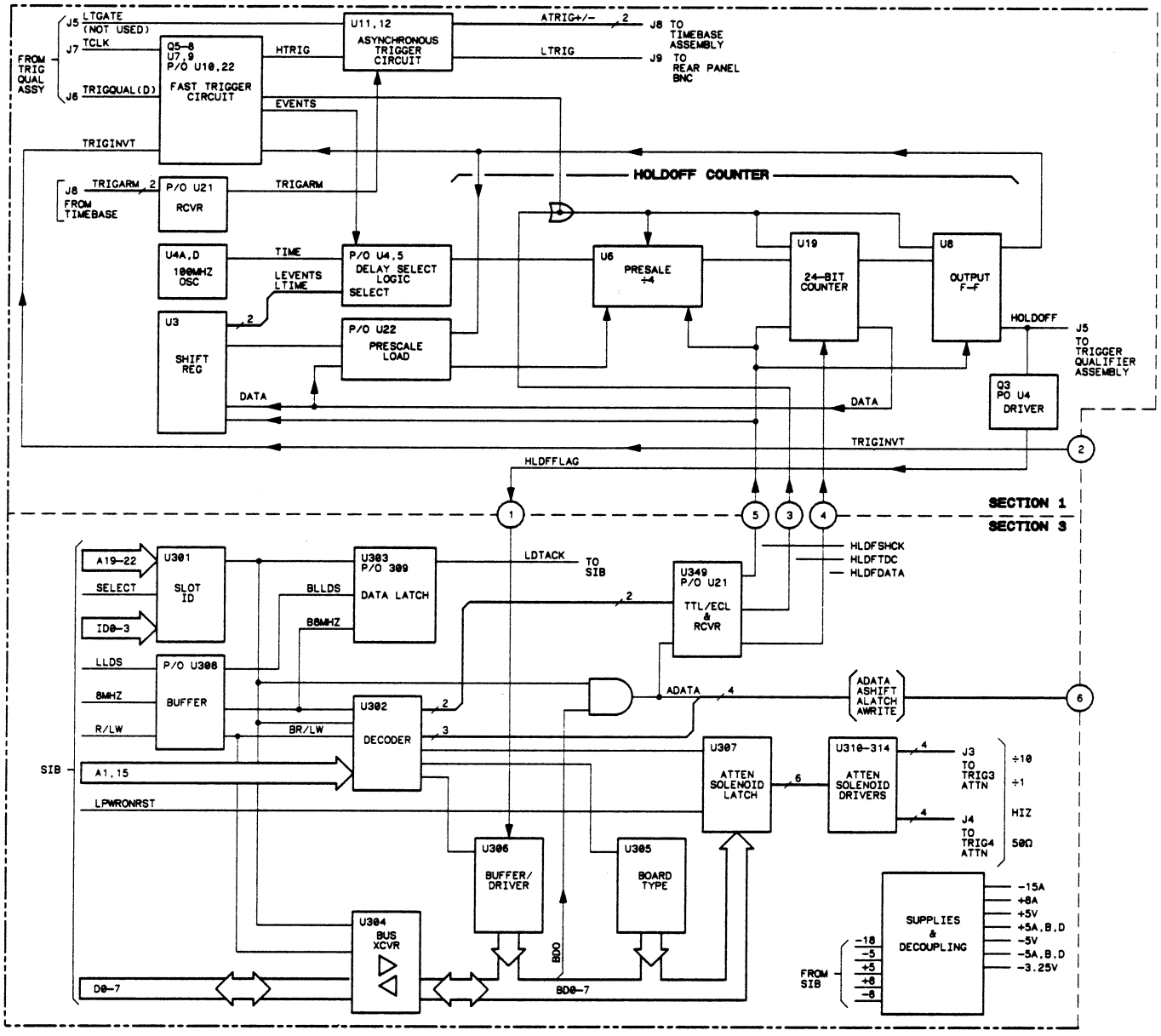



*Figure 6B-10. Trigger Assembly Block Diagram (part 1)*

## 6B-13. TRIGGER ASSEMBLY THEORY

The Trigger assembly establishes the trigger point for an acquisition cycle and establishes the holdoff period. It also provides control and supplies, trigger level, sensitivity, and slope for the TRIG 3 and TRIG 4 attenuators.

Use the Trigger Assembly Block Diagram for the following discussion. The block diagram is laid out in three sections, corresponding to the three schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

### Section 1

**FAST TRIGGER CIRCUIT.** Logically ORs three input lines (only one is used, TCLK) to produce edges representing trigger events. TCLK clocks TRIGQUAL (D) (from the Trigger Qualifier) through the fast trigger circuit. TRIGQUAL (D) functions at the "D" input of the Fast Trigger flip-flop.

The holdoff circuitry keeps the Fast Trig F-F set until the end of the holdoff period. When TRIGQUAL (D) is true, the Fast Trig F-F generates an HTRIG edge on the first TCLK edge after the end of holdoff.

INVERT is used to invert the trigger signal for pattern entered triggering.

**ASYNCHRONOUS TRIGGER FF.** Trigger enable signal TRIGARM enables asynchronous trigger flip-flop U11. U11 then produces ATRIG after it receives the next HTRIG edge.

**HOLDOFF OSCILLATOR.** Generates a crystal controlled 100 MHz signal for holdoff by time.

**HOLDOFF COUNTER.** Counts a 100 MHz signal for time holdoff, or TCLK transistions for events holdoff.

### Section 3

**SLOT ID.** U301 is a 4 bit comparator which compares address lines A19- 22 with slot ID codes ID0-3. Slots are made unique by grounding appropriate pins at the mother board connector. Slots are numbered 0000 to 1001 from left to right. When the slot this assembly is in is addressed, the two codes are equal and U301 output goes high, enabling other circuitry.

**DTA LATCH.** The Data Transfer Acknowledge Latch signals the microprocessor when the Slot ID output is true.

**BUFFER.** Improves the fan-in of several signals to prevent loading of the SIB.

**DECODER.** With address lines A1 and A15 and the R/LW line the read and write functions of this assembly are decoded.

**BUS TRANSCEIVER.** Buffers read/write data from/to the data bus of the SIB.

**TTL/ECL AND RCVR.** The sensitive high frequency trigger circuitry is isolated from the rest of the digital circuitry by the TTL/ECL converter and line receiver. Serial data and control signals pass through this isolation circuitry.

**HOLDOFF FLAG.** Enabling buffer U306 reads HLDFFLAG, the status of the holdoff circuit.

**BOARD TYPE.** When board type is requested by the microprocessor, this assembly responds with a code over the data bus. The input pins of buffer U305 are encoded with the board type. Enabling U305 reads the code.

**ATTENUATOR SOLENOID LATCH.** U307 latches TRIG 3 and TRIG 4 attenuator setup data. This sets the attenuator input impedance, 1MΩ or 50Ω and division ratio, ÷1 or ÷10. A low on the LPWRONRST line keeps the attenuators from changing during power-up.

**ATTENUATOR SOLENOID DRIVERS.** The solenoid drivers provide drive signals to input impedance and division ratio solenoids on the TRIG 3 and TRIG 4 attenuators. The solenoids are magnetically latched, so only a short duration signal is needed to change settings.

**POWER SUPPLIES.** Several power supply voltages are generated on this assembly. They use the supplies on the SIB and isolate circuitry on this assembly from system noise.

## Section 2

Circuitry in this section controls the TRIG 3 and TRIG 4 attenuators. The low frequency amplifiers for the attenuator preamp are also included here.

**SHIFT REGISTERS.** The shift registers convert serial data to parallel for loading in the attenuator control circuitry. U201 and U202 provide a data bus for the DACs and control for loading data. The outputs of U203 and U204 control several attenuator preamp hybrid functions as well as ac/dc and invert functions in the low frequency amp on the Trigger assembly.

**DECODER.** U205 decodes three output lines from U201 and controls the loading of data into shift registers U203 and U204 and DACs U207, 208, and 211.

**DACS.** Single-output DACs U208 and U211 provide the trigger level voltage to the low frequency amplifier. Dual DAC U207 provides trigger sensitivity (gain) signals to the preamp hybrid on the attenuators, for calibration.

**LOW FREQUENCY AMPS.** The low frequency amplifiers are part of the input signal path. The low frequency component of the signal is picked off, amplified, and reinserted at the gate of the FET. The ac/dc coupling and trigger level functions are accomplished in the low frequency amplifier.

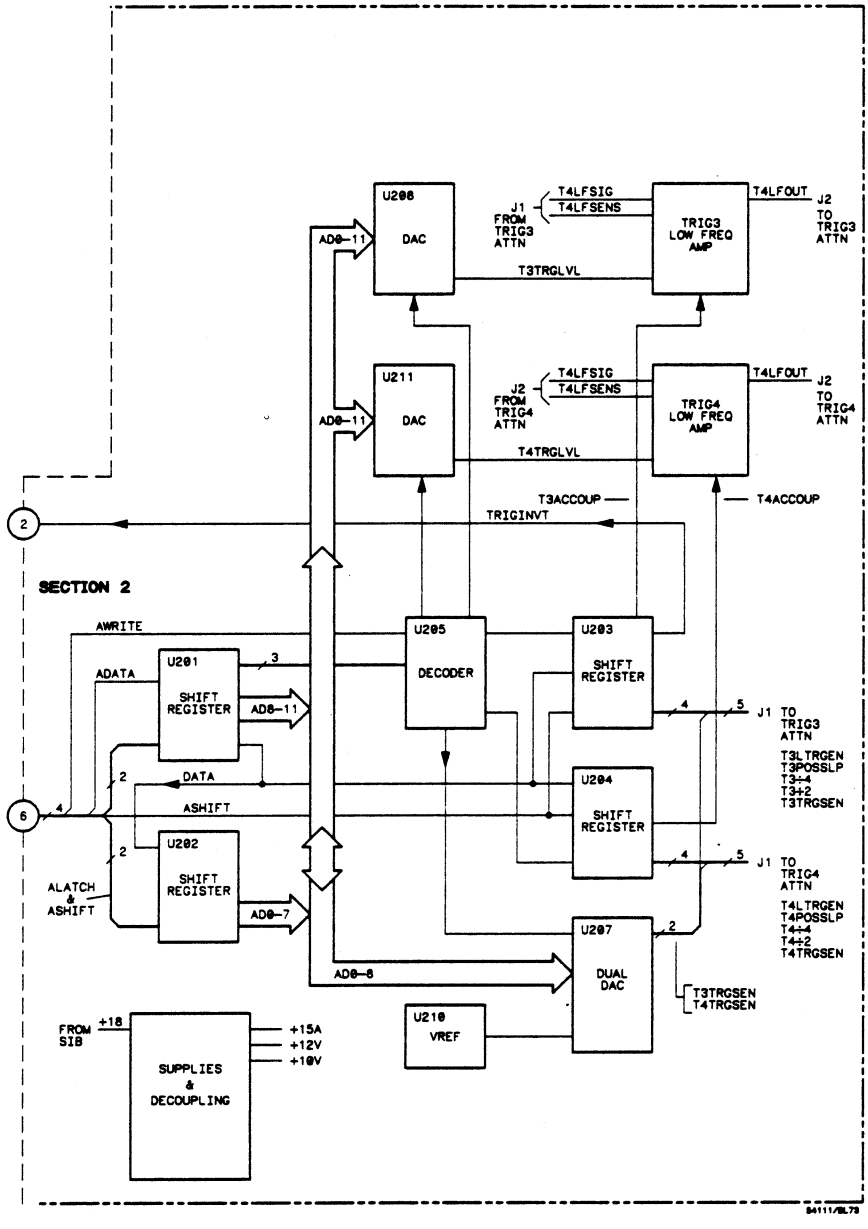



*Figure 6B-11. Trigger Assembly Block Diagram (part 2)*

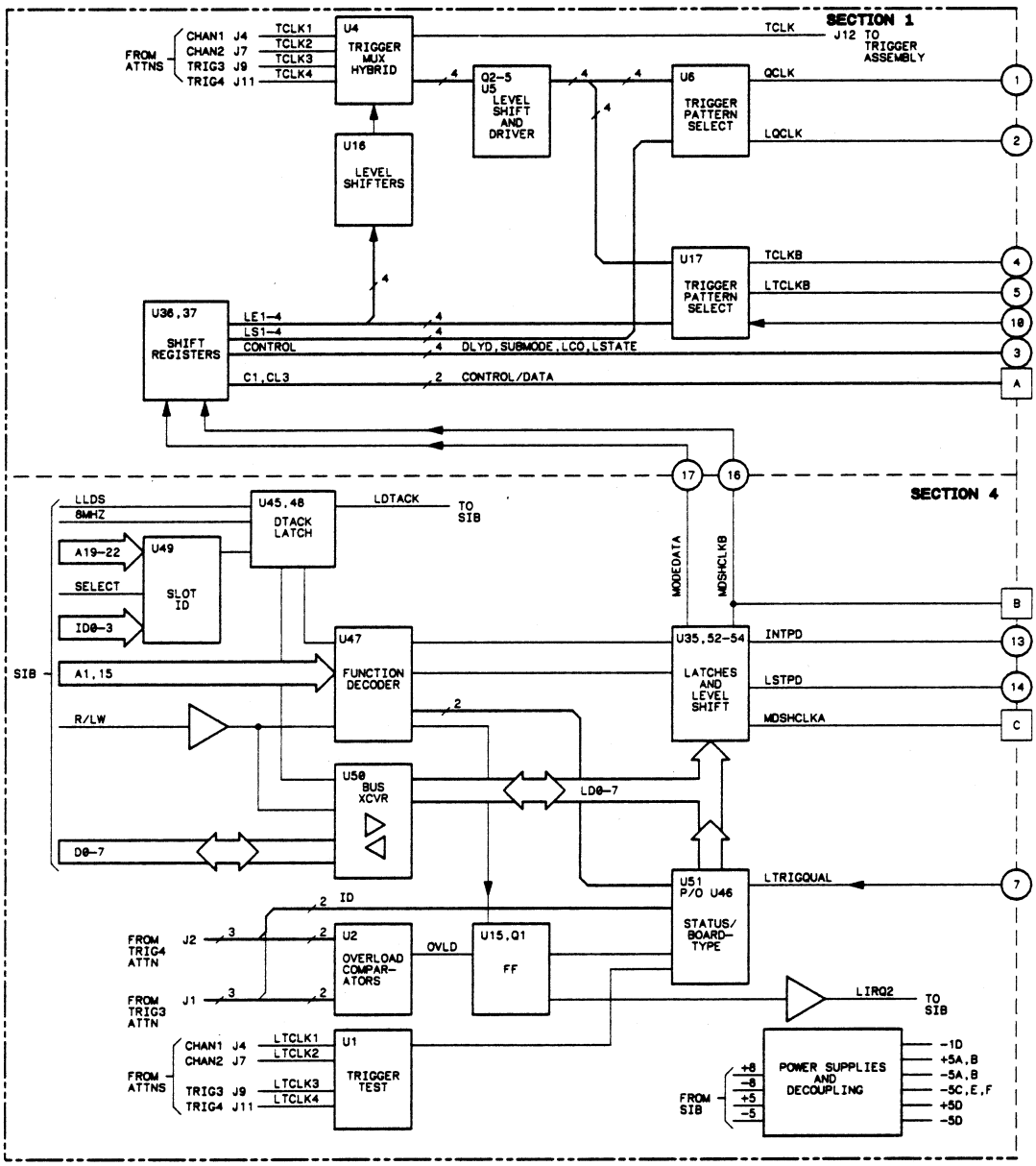



*Figure 6B-12. Trigger Qualifier Assembly Block Diagram (part 1)*

## 6B-14. TRIGGER QUALIFIER ASSEMBLY THEORY

The Trigger Qualifier uses the trigger signals from the channel and trigger attenuators to provide edge and pattern recognition. Trigger delay circuitry is also a part of the Trigger Qualifier.

HOLDOFF is an input from the Trigger assembly. The Trigger Qualifier develops TCLK (trigger clock) and TRIGQUAL (D) (trigger qualifier) for the Trigger assembly circuitry. Probe ID and overload signals are inputs from the attenuators to the Trigger Qualifier.

Use the Trigger Qualifier Assembly Block Diagram for the following discussion. The block diagram is laid out in four sections, corresponding to the four schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

### Section 1

**SHIFT REGISTERS.** The shift registers convert serial data to parallel to provide control functions for trigger selection. Lines LE1-4 and LS1-4 select TCLK1-4 for trigger combinations. The other lines control various functions of the pattern recognition circuitry.

**LEVEL SHIFTERS.** The level shifters convert the levels out of the CMOS shift registers to the level needed by the trigger multiplexer hybrid.

**TRIGGER MULTIPLEXER HYBRID.** The LE1-4 lines, after level shifting, select the combination of TCLK1-4 signals to use as a trigger. This combination becomes TCLK which carries the 500 MHz trigger capability to the Trigger assembly. The transitions of TCLK are used to generate all acquisition triggers. TCLK1-4 signals are also sent through buffers in the multiplexer. These outputs are used for trigger pattern processing.

**LEVEL SHIFT AND DRIVERS.** Transistors Q2-5 level shift and drive the trigger pattern selectors U6 and U17.

**TRIGGER PATTERN SELECT U6.** Trigger select lines LS1-4 select a combination of the buffered TCLK1-4 signals. The QCLK and LQCLK signals are used for event-delay, time-delay and state modes of trigger qualification.

**TRIGGER PATTERN SELECT U17.** Trigger select lines LE1-4 select a combination of the buffered TCLK1-4 signals. The TCLKB and LTCLKB signals, which are logically equivalent to the TCLK signal, are used for event-delay and pattern present modes of trigger qualification.

### Section 4

**SLOT ID.** U49 is a 4 bit comparator which compares address lines A19-22 with slot ID codes ID0-3. The slot is made unique by grounding appropriate pins at the mother board connector. Slots are numbered 0000 to 1001 from left to right. When the slot this assembly is in is addressed, the two codes are equal and U49 output goes high, enabling other circuitry.

**DTACK LATCH.** When this assemblyd is addressed, the latch enables function decoder U47 and bus transceiver U50. The latch also sends out LDTACK over the SIB.

**FUNCTION DECODE.** Decodes R/LW, A1 and A15 to enable various functions on this assembly.

**TRIG INPUT OVERLOAD CIRCUIT.** Lines from the TRIG 3 and TRIG 4 attenuators monitor the signals on the 50Ω input termination resistors. If the signals are too high, overload comparators provide an interrupt to the microprocessor over the IRQ2 line and a flag onto the data bus. When the voltage returns to within limits, the microprocessor sends a clear signal through U47 which resets the circuit.

**TRIGGER TEST.** The complementary trigger outputs from the attenuators, LTCLK1-4, are used for internal testing. A simulated signal is generated in the attenuator circuitry. The trigger test comparators sense activity on the trigger lines and the output of the comparators is

read by the microprocessor. This provides additional information for fault location.

**STATUS/BOARD TYPE.** U51 and parts of U46 function to read status lines or board type onto the data bus. One output of the decoder U47 enables reading status, another enables reading board type. The status lines read are LTRIGQUAL, TRIG 3/TRIG 4 probe IDs, and input overload. A sense ring on the TRIG 3/4 input BNCs pulls the ID line down when a standard 10:1 probe is installed. The instrument automatically adjusts triggering factors for the 10:1 probe.

**LATCHES AND LEVEL SHIFT.** This circuitry controls and loads data into the time and event qualifying circuitry. It is an interface between the TTL bus interface and the ECL and CMOS circuitry it drives. It also isolates the controlled circuitry from the bus environment. The outputs are serial data, two clocks, and two control lines.

**POWER SUPPLIES.** The power supplies and decoupling isolate the trigger qualifier circuitry from the SIB power buses.

## Section 2

**MODE CONTROL LOGIC.** This circuitry controls the set-up of the various resources available for trigger qualification. To control the set-up the microprocessor loads 45 bits of serial data through shift registers U36 and U37 (section 1) and shift register U38 and counter U26 (section 3). Mode control logic set-up is loaded through shift registers U36 and U37.

**100 MHZ TRIGGER.** Dual D flip-flop U19 is used to start the 100 MHz oscillator and 29-bit counter when they are used in time delay or event delay modes.

**STARTABLE OSCILLATOR** This 100 MHz oscillator is used as a reference for delay-by-time and pattern present-for-time functions.

**TRIGGER SELECT AND DRIVERS.** OR/AND gate U7 selects the desired source for the qualified trigger in state and event delay modes. In time delayed modes the output of U8 is the source. The Outputs of U7 and U8 are ORed (effectively) and used to drive common-base transistors Q6 and Q12 which drive the TRIGQUAL (D) and LTRIGQUAL lines respectively.

## Section 3

Section three, a 29-bit counter, is a subfunction of section two. It is a 150 MHz counter used for counting time or events in various trigger modes. It is comprised of a one-bit, a four-bit, and a 24-bit counter. For short counts, the microprocessor uses the control lines to disable unneeded sections of the 29-bit counter.

**RESTART CIRCUIT.** With the restart circuit set, the counter always starts at the beginning of the count sequence, regardless of the previous state of the rest of the logic. This gives a 10 ns reload time.

**CONTROL LOGIC.** The control logic selects the counters to be used for the division ratio.

**PRESCALER.** The prescaler U23B allows a quick response when the count is from 1 to 4. It is only one bit, but counts 3 and 4 are accomplished by how it is set up.

**4-BIT COUNTER.** The 4-bit counter, with the prescaler, is used from counts 5 to 36. The 24-bit counter takes too long to load for these counts.

**24-BIT COUNTER.** The 24-bit counter, with the other counters, is used for counts greater than 36. In this mode all counters are running.

**OUTPUT F-F U20A.** The output flip-flop provides a pulse with a duration dependant on the counting time.

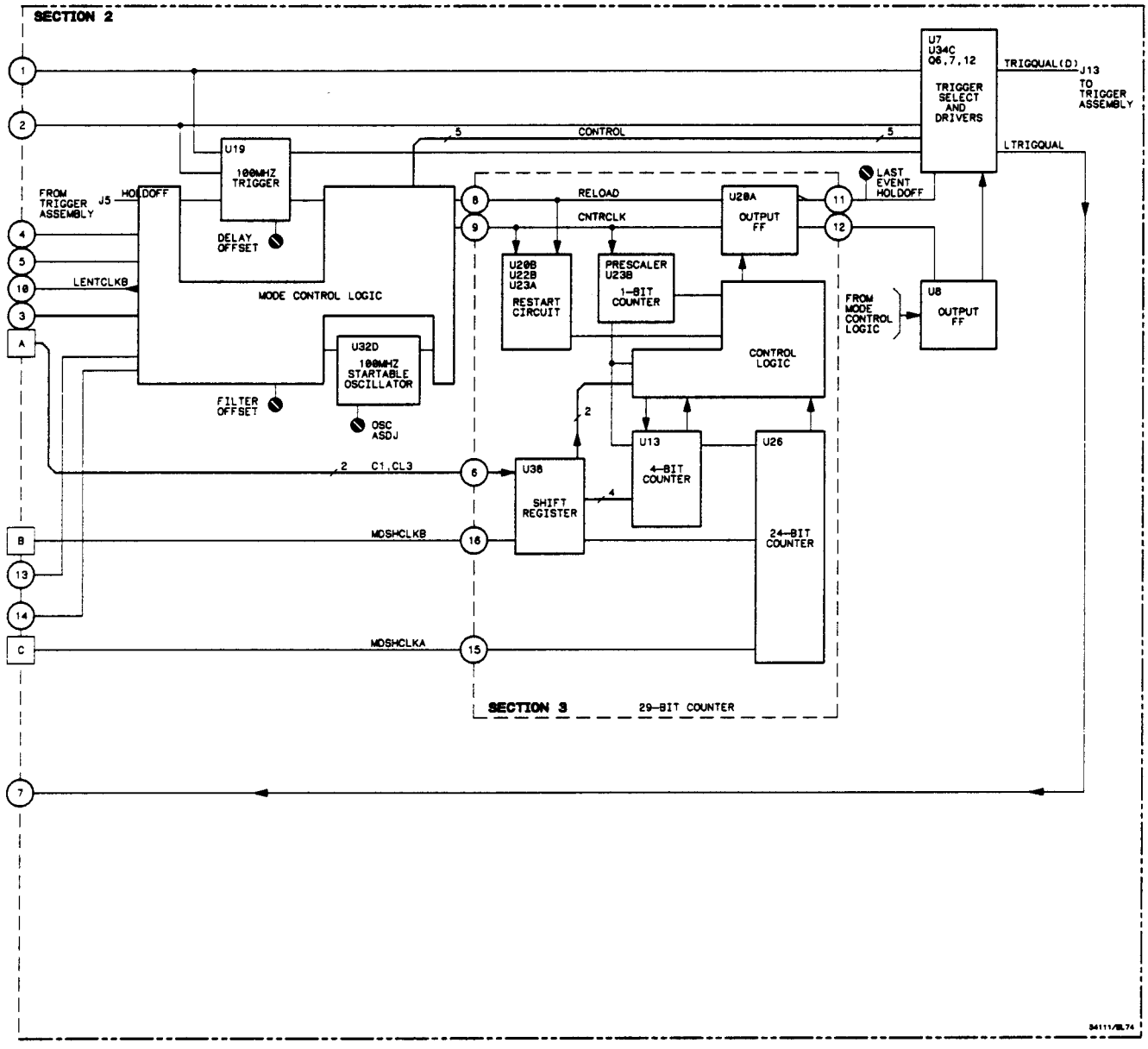



*Figure 6B-13. Trigger Qualifier Assembly Block Diagram (part 2)*

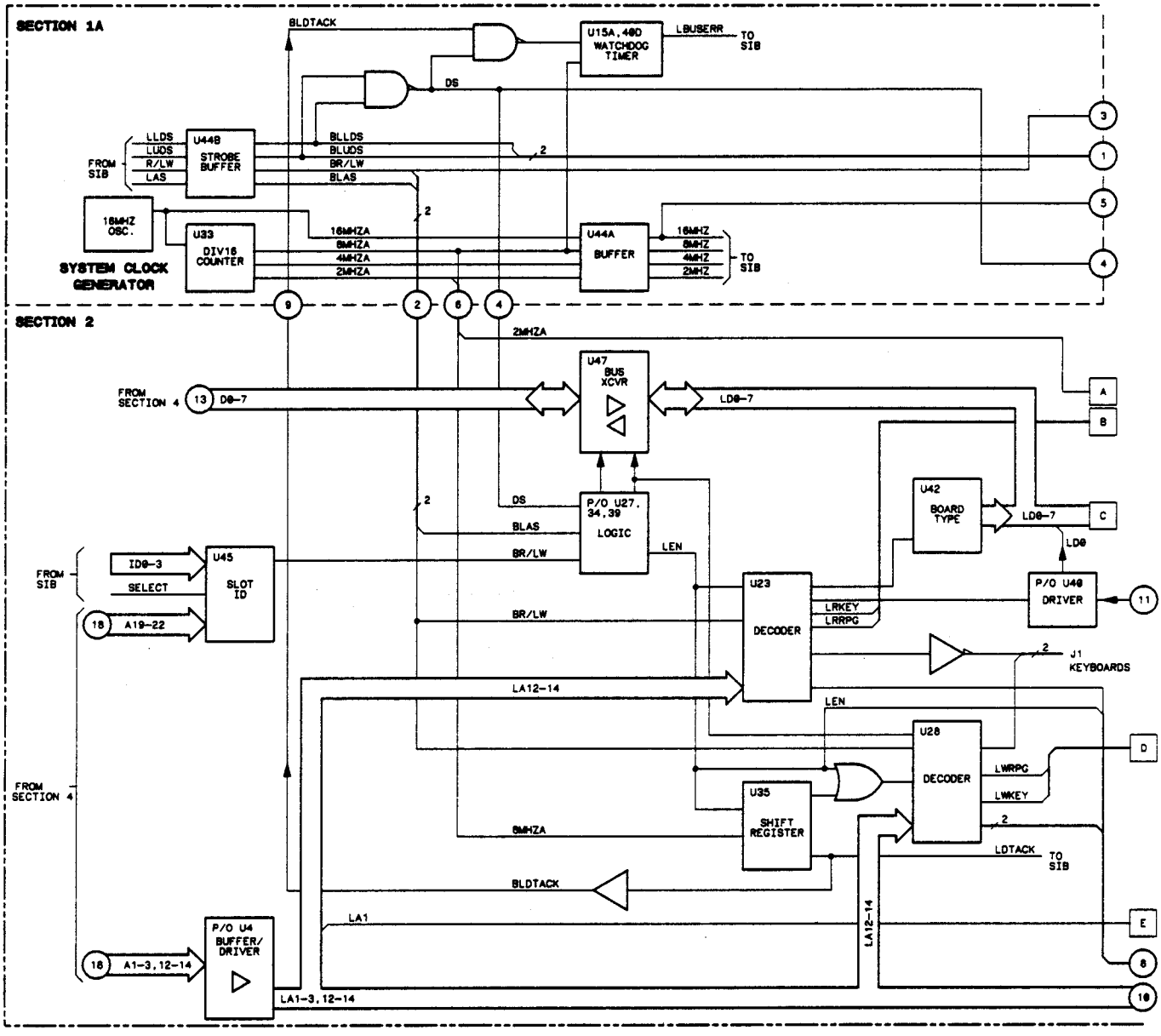



*Figure 6B-14. I/O Assembly Block Diagram (part 1)*

## 6B-15. INPUT/OUTPUT ASSEMBLY THEORY

The I/O assembly serves several purposes. First it provides instrument interface to keyboard and HP-IB through ribbon cables. It provides 256K words of dynamic RAM for waveform storage and other purposes. It provides several system functions, all of which are described below. In addition the I/O provides passive pull-up resistors for data, address, and control lines for the System Interface Bus, (SIB).

Use the I/O Assembly Block Diagram for the following discussion. The block diagram is laid out in five sections, corresponding to the five schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

### Section 1A

**STROBE BUFFER.** Buffer U44B provides increased fan-out for the data and address strobes and the read/write line.

**SYSTEM CLOCK GENERATOR.** A crystal controled 16 MHz oscillator supplies the system clock. A binary counter divides this down into 8 MHz, 4 MHz and 2 MHz. All four signals are buffered onto the System Interface Bus (SIB).

**WATCH DOG TIMER.** Under normal operation U18 should be reset by LDTACK before a time constant set by R19 and C40 times out. If U18 is not reset it generates LBUSERR which keeps the microprocessor from getting hung up in an instruction cycle. This could happen if any addressed assembly does not generate LDTACK or if the microprocessor tries to access a nonexsistent assembly.

### Section 2

**SLOT ID.** U45 is a 4 bit comparator which compares address lines A19-22 with slot ID codes ID0-3. Slots are made unique by grounding appropriate pins at the mother board connector. Slots are numbered 0000 to 1001 from left to right. When the slot this assembly is in is addressed, the two codes are equal and U45 output goes high, enabling other circuitry.

**BUFFER/DRIVER.** Buffer/driver U46 buffers several of the address lines into the control circuitry on this assembly.

**LOGIC CIRCUIT.** The logic circuit of parts of U27, U34, and U39 use several signals to control read and write functions.

**BUS TRANSCEIVER.** U47 buffers data off of and on to the SIB.

**BOARD TYPE.** When board type is requested by the microprocessor, this assembly responds with a code over the data bus. The input pins of buffer U305 are encoded with the board type. Enabling U305 reads the code.

**DRIVER U40.** U40, under control of read decoder U23, buffers the power test signal onto the local data bus.

**DECODERS.** Decoders U23 and U28 decode address lines LA12-14 to provide enables for the various functions on the I/O assembly. U23 provides read enables and U28 write enables.

**SHIFT REGISTER.** U35 generates LDTACK which is sent back to the microprocessor indicating data was received. This signal also resets the watchdog timer (section 1). Another signal from U35 helps enable the write decoder U28.

**KEYBOARD CONTROLLER.** U21 sees a keyclosure and interrupts the microprocessor by IRQ4 line. U21 detects which key was pressed by scanning column lines with pulses and sensing rows for a return path. U21 converts key closure scan data to parallel data and places this on the local data bus when enabled.

**KEYBOARD DMUX.** This demultiplexer drives the keyboard columns using the three scan lines out of the keyboard controller.

**RPG READ.** The RPG outputs two out-of-phase pulses. Direction of rotation is determined by the difference in phase angle

between both pulses. The pulse frequency is a function of rotation speed and this tells the microprocessor what size of incremental steps to take. Part of U13 detects RPG activity, and interrupts the microprocessor by IRQ3 line.

## Section 1B

**HP-IB.** U1 interprets HP-IB commands and controls direction of data flow from an external controller to local data bus. One side of U1, LD0- 7, connects to the local data bus. The other side of U1 connects to two bidirectional data transceivers, U4 for data and U5 for control commands. The data transceivers buffer between the HP-IB and the HP-IB controller.

## Section 3

**POWER TEST.** The power test circuitry monitors all six supplies on the SIB. The CPU reads the output of this circuit during self test.

**POWER ON RESET.** Power on reset circuit provides a glitch-free pulse shortly after power up and power down. This sets many devices to a known state and prevents the microprocessor from taking damaging action during power up. A pushbutton switch also provides a manual means to reset the system without powering down the instrument.

**BATTERY CIRCUITS.** A battery provides power for the non-volitile RAM memory on the microprocessor assembly. It can retain basic setup information and system configuration for several years. The circuit also keeps the battery charged and provides for smooth transfer of power from battery to power supplies after power up.

## Section 4

Section four is comprised of the control circuitry for the dynamic RAM. Dynamic RAM is addressed in rows and columns and must be refreshed to maintain memory.

**RAM ID.** From the CPUs perspective the dynamic RAM is a "slot" by itself, irrespective of the slot for the I/O assembly. The other assemblies are IDd by the slot ID code. U51 is a 4 bit comparator which compares address lines A19-22 with code 10 decimal which is hard-wired on the other comparator input. The CPU sees the dynamic RAM at "slot" 10 no matter which slot the I/O assembly is in.

**BUS XCVRS.** The bus transceivers and associated logic buffer data between the dynamic RAM and the SIB.

**COLUMN STROBES.** The column strobes and associated ciruitry provides the column address strobes, LCAS1-8, for the dynamic RAM.

**ROW STROBES.** The row strobes and associated ciruitry provides the row address strobes, LRAS1-4, for the dynamic RAM.

**ADDRESS MUX.** U30 and U38 multiplex 16 of the SIB address lines into the eight memory address lines of the dynamic RAM.

**CONTROL AND REFRESH.** The control and refresh circuitry provides the necessary timing to write and read from memory while keeping the memory refreshed at the proper interval.

**REFRESH COUNTER.** The refresh counter activates the memory address lines during the refresh cycle.

## Section 5.

Section 5 consists of an array of 16, 64K by 4 bit dynamic RAMs. The addressing and refresh circuitry is covered in section 4.

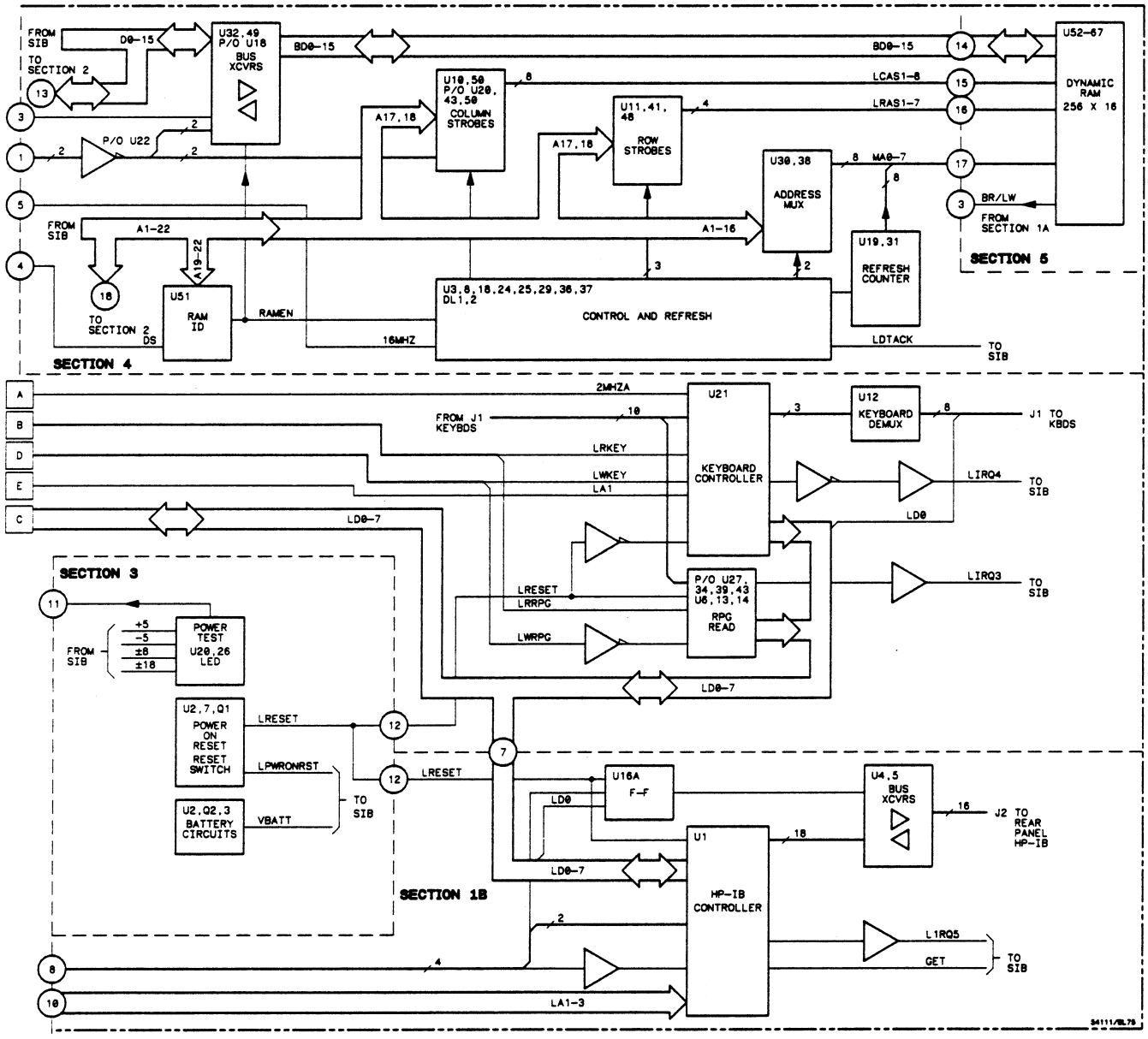



*Figure 6B-15. I/O Assembly Block Diagram (part 2)*

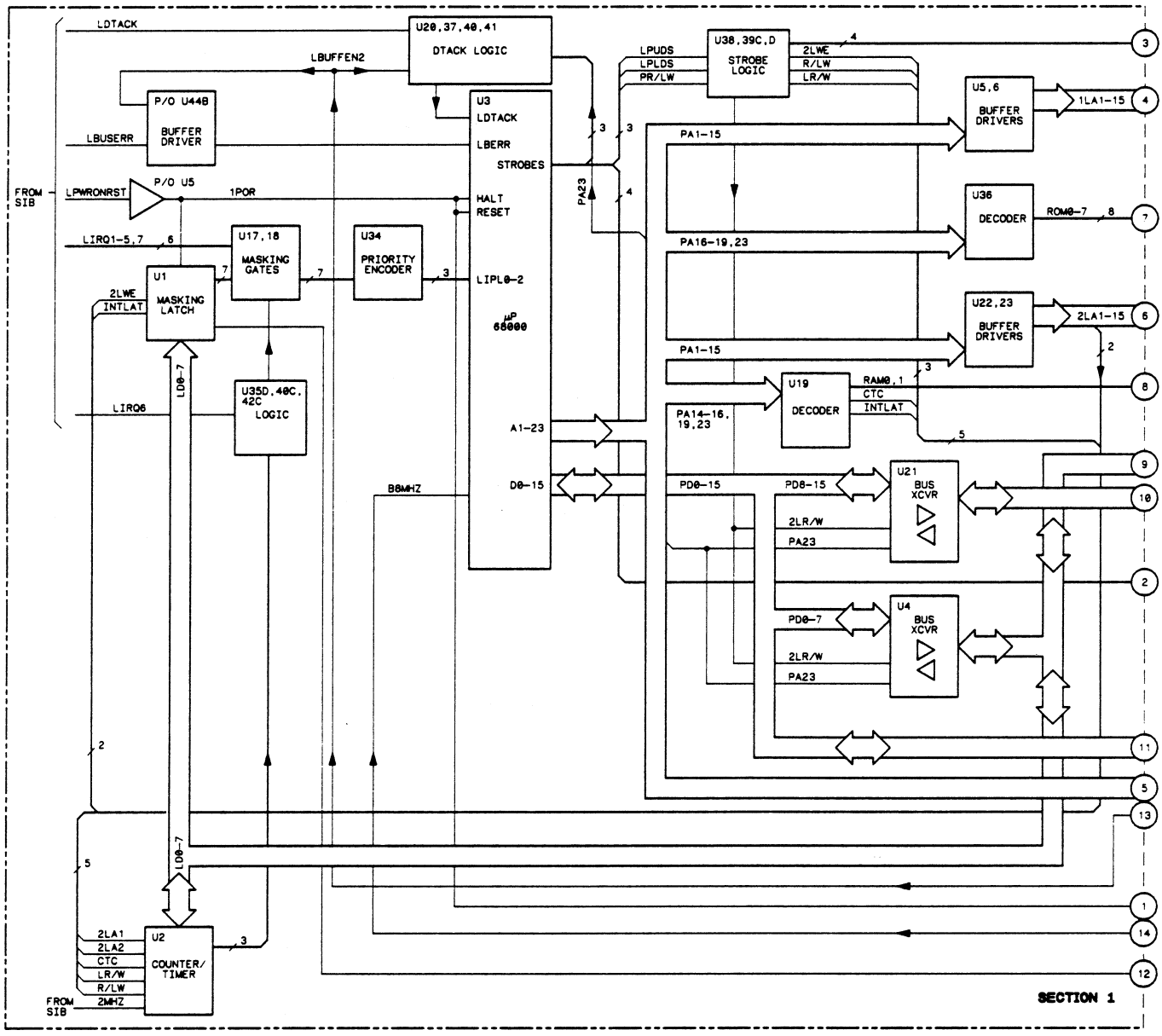



*Figure 6B-16. Microprocessor Assembly Block Diagram (part 1)*

## 6B-16. MICROPROCESSOR ASSEMBLY THEORY

The Microprocessor assembly controls the operation of the instrument. At initial power up, power on reset insures the μP starts up in a known condition. The μP then runs several routines, some of which are: determine which assembly is in which slot, system self diagnostics, and setup display information. The μP then responds to system interrupts, HP- IB, keyboard, or RPG.

Use the Microprocessor Assembly Block Diagram for the following discussion. The block diagram is laid out in three sections, corresponding to the three schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

To the μP, all system assemblies look like memory locations. Address line A23 separates local memory from system memory. When A23 is high system memory is being accessed over the SIB. When A23 is low local processor memory is being accessed. After the μP sends data over the SIB, LDTACK comes back from the addressed assembly, which tells the μP the information was received. This LDTACK also goes to the I/O assembly and resets the watchdog timer. If the watchdog timer is not reset, then BUSERR is sent to the μP which displays an error message on the CRT.

The μP starts a data acquisition cycle by setting a bit on the Timebase assembly. When the acquisition cycle is finished, the microprocessor moves data from ADC memories to display memories. The microprocessor does signal post-processing, making measurements on the signal and digital signal filtering, averaging, etc.

### Section 1

**μP.** The Motorola 68000 microprocessor runs at 8 MHz. Main characteristics are: 16 bit data bus, 23 bit address bus, and 3 interrupt lines.

**INTERRUPT CIRCUITRY.** The μP communicates with the bus through the interrupt circuitry. Any of the seven interrupt lines on the SIB can be masked by the μP.

**Counter/Timer.** The counter/timer contains three programmable counters. It is used primarily as a time-out device. The microprocessor programs and reads each counter over LD0-7 lines. Each counter has an output which is used as an interrupt to the microprocessor. All three counter outputs are ORed through U35 and U42. This result, through U40, shares an interrupt line with LIRQ6 from the SIB.

**Masking Latch.** The masking latch latches data from LD0-7 to set masks on the seven interrupt lines. The output of the latch is OR'ed with the interrupt so a high out of the latch masks the interrupt signal.

**Masking Gates.** The gates of U17 and U18 OR the interrupt with the output of the masking latch. A high from the latch masks the interrupt.

**Priority Encoder.** Encodes all seven incoming interrupt lines into three lines for the microprocessor. If more then one interrupt occurs at the same time, U34 prioritizes them so the interrupt with the highest priority is processed first. When an interrupt occurs, the system is vectored to a predetermined firmware location.

**STROBE LOGIC.** The strobe logic combines the upper and lower data strobes and read/write from the microprocessor into read and write enables for local use.

**BUFFER DRIVERS.** Buffer/drivers U5, 6, 22, and 23 drive the ROM and RAM with address lines LA1-15. U22 also provides 2LA1 and 2LA2 to the counter/timer.

**DECODERS.** U19 and U36 decode certain address lines into RAM and ROM select lines. U19 also provides two control lines to the counter/timer.

**BUS TRANSCEIVERS.** Bus transceivers U4 and U21 control read and write to the ROM and RAM on the microprocessor assembly.

## Section 2

Section two covers the μP ROM and RAM. The ROM and RAM ICs have 8 bit data lines. To acheive 16 bit data words, 16 bit words are divided into a lower portion LD0-7, and an upper portion LD8-15. ROMs or RAMs are read in pairs.

Firmware instructions for the μP are contained in ROM memory. There is space for eight ROM pairs, but some instruments may use fewer ROMs.

The non-volatile battery backed-up RAM contains stack registers, status registers, scratch pad memory, and soft cal information. Several setup registers save front panel setup information.

## Section 3

**BUS ARBITRATION LOGIC.** The microprocessor assembly contains circuitry so it can operate in a multiprocessor system. With only one microprocessor being used, bus request and bus grant signals are tied to the proper logic levels to ensure this board has control over the SIB when required.

**BUFFER DRIVER U44.** U44B buffers the upper and lower data strobes and the address strobe onto the SIB.

**BUS TRANSCEIVERS.** The bus transceivers, U48 and U49, interface the microprocessor data bus and the SIB data bus.

**BUFFER/DRIVERS U45-47.** These buffers isolate the microprocessor address bus from the SIB address bus. LIACK, interrupt acknowledge, and R/LW are buffered by U45.

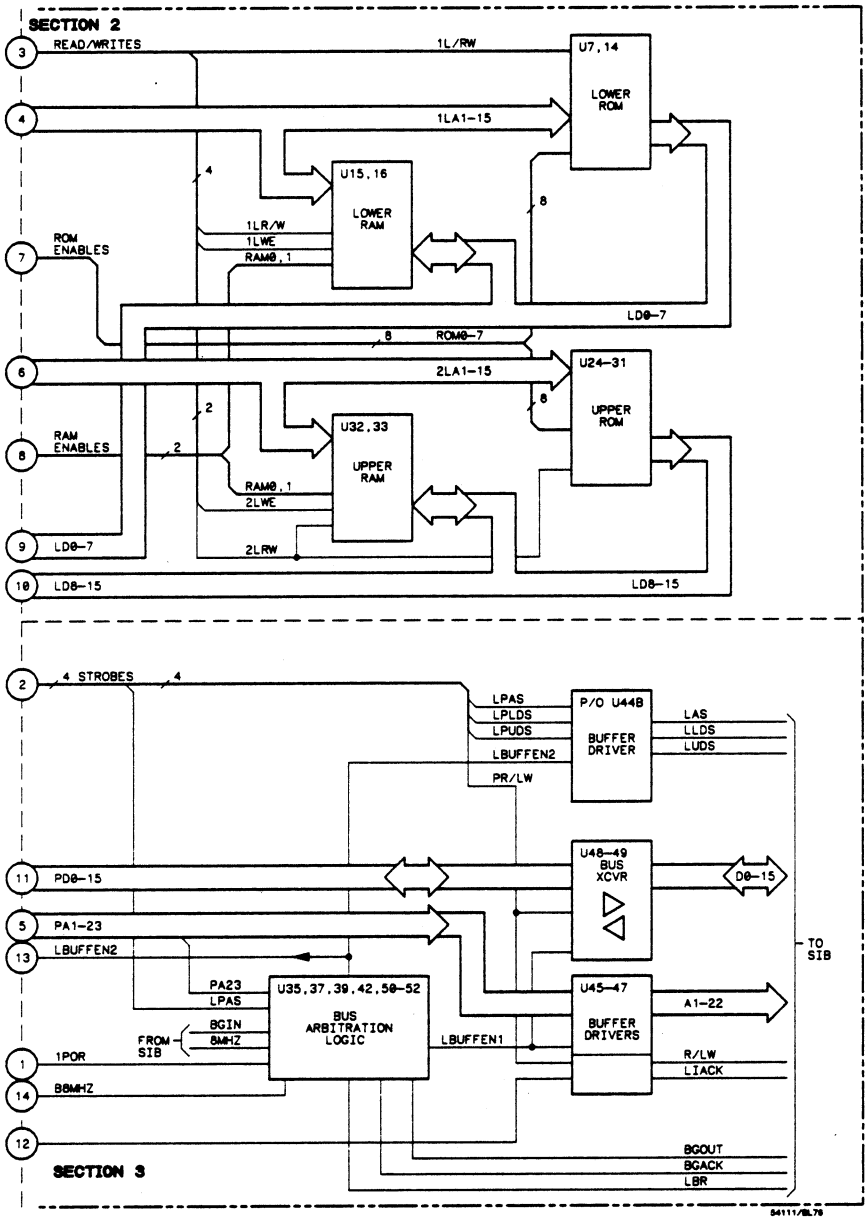



*Figure 6B-17. Microprocessor Assembly Block Diagram (part 2)*

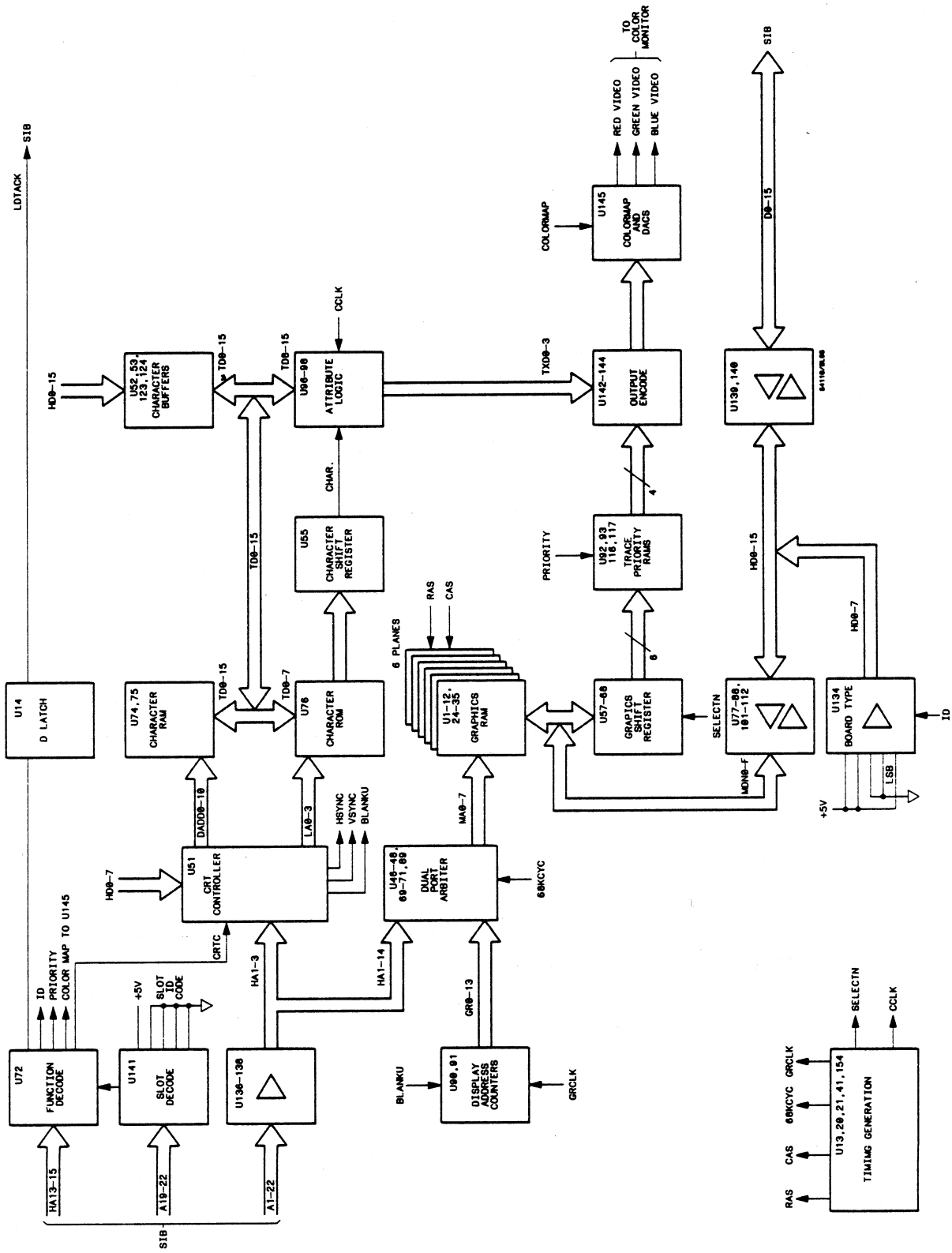



*Figure 6B-18. Color Display Assembly Block Diagram*

## 6B-17. COLOR DISPLAY ASSEMBLY THEORY

This assembly is the interface between the microprocessor and Color CRT Module. It contains graphics memory, timing generator, character generator, prioritization circuitry, color map, and output DACs.

**TIMING GENERATION.** Controls timing functions for the Color Display assembly.

**FUNCTION DECODER.** Decodes HA13-15 to enable various board functions, these are: CRTC for the CRT controller, ID for board type, COLOR MAP for the color map and output DACs, priority for RAM.

**D LATCH.** Outputs LDTACK over the SIB, indicating data was accepted.

**SLOT DECODE.** A 4 bit comparator, U141, compares slot address lines A19-22, to the slot ID code hard wired on the board. When board is addressed, the codes are equal and U141 helps enable the function decoder.

**CRT CONTROLLER.** Controls timing signals for the Color Display Module, blanking, horizontal and vertical drive, and character control.

**CHARACTER RAM.** Characters are stored here as 16 bit words, 8 bits for the character and 8 bits for character attributes.

| Bit number | Function |
|---|---|
| TD0-6 | ASCII character |
| TD7 | Not used |
| TD8 | Inverse video |
| TD9 | Blink |
| TD10 | Underline |
| TD11-14 | Color |
| TD15 | Priority bit |

**CHARACTER ROM.** Functions as a character generator by decoding ASCII data, TD0-7, from character RAM.

**CHARACTER SHIFT REGISTERS.** Converts parallel character data to serial character video.

**ATTRIBUTE LOGIC.** Converts TD8-15 to attributes, 4 bits for color and 4 bits for other attributes. Above table defines these bits.

**DISPLAY ADDRESS COUNTERS.** 4-bit counters which generate address lines GA0-13.

**DUAL PORT ARBITER.** Outputs addresses from either the host microprocessor or an outside controller to place graphics on screen.

**GRAPHICS RAM.** Six planes of dynamic memory which store graphics data.

| Plane | Information |
|---|---|
| 0 | Graticules |
| 1 | Stored Traces |
| 2 | Channel 1 |
| 3 | Channel 2 |
| 4 | Not Displayed |
| 5 | Not Displayed |

**GRAPHICS SHIFT REGISTERS.** Parallel loaded with graphics data and serially outputs graphics video.

**TRACE PRIORITY RAM.** A high speed RAM which maps outputs from the graphics planes into unique address locations for the color map. It also provides arbitration when more then one plane tries to illuminate the same pixel location. Plane 0 has the lowest priority and plane 3 the highest. Planes 4 and 5 are scratch pad memory and not displayed, so have no priority significance.

**OUTPUT ENCODE.** Generate addresses for the color map using graphics data or character and attribute data

**COLOR MAP AND OUTPUT DAC.** Three RAMs convert encoded addresses to a digital color value: red, green, or blue. There is one output DAC for each RAM. The output DACs convert the digital value to red, green, or blue levels for the Color CRT Module.

**BOARD TYPE.** When the microprocessor requests board type, this buffer is enabled and the response is "25" over the LD0-7 lines.

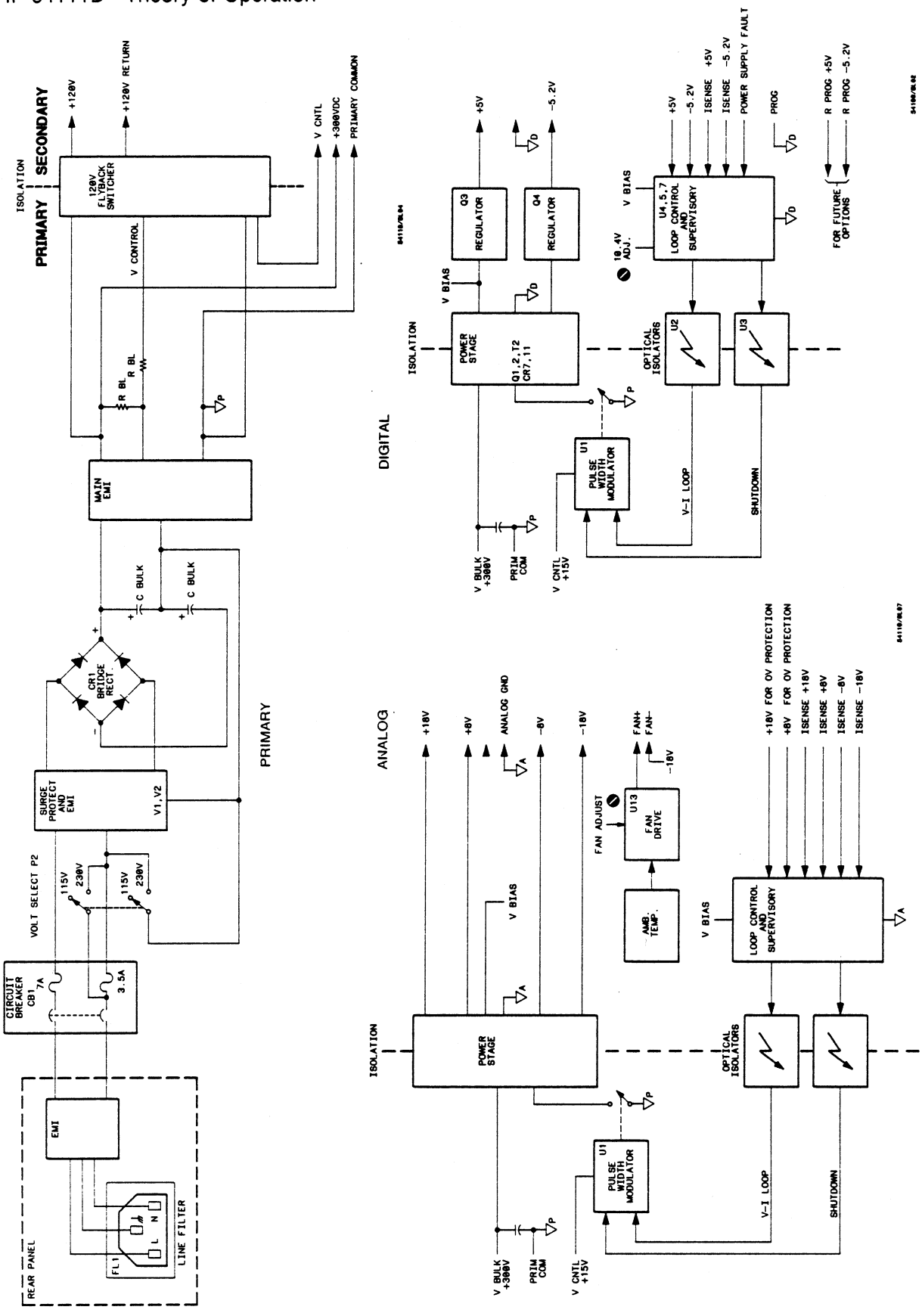



*Figure 6B-19. Power Supply Block Diagrams*

## 6B-18. POWER SUPPLY THEORY

## 6B-19. Primary Power Supply

The primary board rectifies and filters the input ac voltage. When the voltage select switch is in the 230V position, the ac is bridge rectified and filtered to yield approximately 300V dc and 120V dc. 120V dc is generated by an isolating switching regulator, and is used to power the color monitor. 300V dc is used for the digital and analog supplies. The input voltage is doubled in the 115V position to yield the same dc voltages.

The primary board has surge protection circuitry that protects against ac line voltage transients and current surges. Over voltage crowbar devices trip the circuit breaker for sustained input over-voltage conditions.

The pulse width modulator (PWM) circuitry is powered by a bleeder resistor on one of the bulk storage capacitors. The main EMI (electromagnetic interference) filter is located in a dc current path to reduce component size and to increase effectiveness of the filter.

## 6B-20. Digital Power Supply

The digital power supply is a dc to dc converter which converts 300V dc to +5V and -5.2V dc.

**PULSE WIDTH MODULATOR (PWM).** Is used to achieve voltage and current regulation by changing the PWM's turn-on time. It has an operating frequency of 68 kHz.

**POWER STAGE.** Performs the actual conversion of 300V dc to +5V and -5.2V dc. Digital and primary ground planes are kept isolated through transformer T2.

**OPTICAL ISOLATORS.** Isolates the primary and digital ground planes. Voltage and current feedback control is sent through U2, to control the duty cycle of the PWM. Power supply shutdown is sent through U3.

**LOOP CONTROL AND SUPERVISORY.** When excessive output voltage is detected, circuitry sets a latch in the PWM which can only be reset by cycling the circuit breaker off for 60 seconds, or an instantaneous reset by cycling the front panel power switch. Circuitry also senses the current and activates foldback current limiting for excessive current loading.

## 6B-21. Analog Power Supply

The analog power supply is a dc-to-dc converter which converts 300V dc to +18V, +8V, -8V, and -18V dc.

**PULSE WIDTH MODULATOR (PWM).** Is used to acheive voltage and current regulation by changing the PWM's turn on time. It has an operating frequency of 68 kHz.

**POWER STAGE.** Performs the actual conversion of 300V dc to +18V, +8V, -8V, and -18V dc. Plus a fan drive output that increases fan speed with ambient temperature. Analog and primary ground planes are kept isolated through transformer T2.

**OPTICAL ISOLATORS.** Isolates the primary and analog ground planes. Voltage and current feedback control is sent through U2, to control the duty cycle of the PWM. Power supply shutdown is sent through U3.

**LOOP CONTROL AND SUPERVISORY.** When excessive over-voltage is detected, circuitry sets a latch in the PWM which can only be reset instantaneously by cycling the front panel power switch to standby and then to on, or by turning the circuit breaker to the off position for 60 seconds. +18 volts is regulated and the other outputs are semi-regulated outputs which follow the +18 volts. Each output is current limited. The -8 volt output has foldback current limiting.

# SECTION 6C
# SERVICE MENUS/KEYS

## 6C-1. INTRODUCTION

This section describes the service menus and keys that are available for calibration, troubleshooting and CRT display alignment. A basic understanding of these will be helpful in troubleshooting failures, however, Self-Test and Troubleshooting is covered specifically in Section 6D.

## 6C-2. SERVICE MENUS

The service menus are part of the Utility menu, in the second level of the menu softkeys. Once Utility is pressed, six function keys will be displayed: Probe Menu, HP-IB Menu, Cal Menu, Test Menu, Color Menu, and CRT Setup Menu.

**PROBE MENU.** The Probe Menu is used to set the attenuation factor before the input of the instrument. This sets the instrument scaling factors for a special probe or other device. This is not a service menu though the functions may be used during service procedures. Further use of this menu is covered in the Operating and Programming and other user manuals.

**HPIB MENU.** The HPIB Menu provides keys that are used to set the HPIB attributes. These attributes are address number, Talk/Listen, and EOI. This menu is discussed in detail in the Operating and Programming and other user manuals.

**CAL MENU.** The Cal Menu is used to calibrate the instrument. The calibration factors are stored in non-volitle memory. Use of this menu is covered in the *HP 54111D Operating and Programming Manual*. Basic functions of the Cal menus are covered in this section.

**TEST MENU.** The Test Menu provides several functions used to set up and run internal diagnostics test and view the results. Use of these functions is covered briefly in following paragraphs and comprehensively in the Self-Tests/Troubleshooting, section 6D.

**COLOR MENU.** The Color Cal Menu provides functions used to set the characteristics of the colors displayed. These characteristics include hue, saturation, and luminosity. This menu is covered in detail in the Operating and Programming and other user manuals.

**CRT SETUP.** The CRT Setup Menu provides several functions that provide confidence testing as well as test patterns for adjusting the Color CRT Module. These functions are discussed in following paragraphs.

## 6C-3. ONE-KEY POWER UP

A one-key power up is often performed to return the instrument setup to default conditions. This is done as follows:

1. Set the front panel POWER switch to STBY,
2. Press and hold one front panel key,
3. Turn front panel POWER switch to ON.
4. Release key when display shows "Powerup Self Test Passed!" or Failed.

## 6C-4. TWO-KEY POWER UP

**CAUTION**

*Using the two-key power up will leave the instrument uncalibrated. Effort needed for recalibration should be considered before using this mode to reset the instrument. Calibration traceability will be lost if a two-key powerup is used.*

A two-key power up is a basic reset of the entire operating system of the HP 54111D. All volatile and non-volatile RAM is cleared. As a result, all calibration factors are purged and the instrument must be recalibrated.

All calibration except the Timebase Cals can be done with just the front panel CAL signal and the self-cal menus. For further information about Timebase Cal read later paragraphs in this section. The two-key power up is performed in much the same way as the one-key power up.

1. Set the front panel POWER switch to STBY.
2. Press and hold the top and bottom keys in the group at the right edge of the display.
3. Turn front panel POWER switch to ON.
4. Release keys when display shows "Powerup Self Test Passed!" or Failed.

## 6C-5. CAL MENUS

## 6C-6. ADC Reference Cal

ADC Reference Cal calibrates the comparator stick references in the ADC hybrid (see theory of operation). Since the ADC is composed of four separate convertors, they must calibrated so they all convert the same input voltage to the same digital value. If they do not, the digitized input will appear in the display as two or more traces.

ADC Reference Cal can be set to manual or automatic modes. It can be performed at any time by pressing ***ADC Reference Cal*** in the Cal menu. It is also done automatically as part of the Vertical Cal.

See the *HP 54111D Operating and Programming Manual*, the chapter on utility menus, for further information about this function.

ADC Reference Cal uses internal hardware to provide a level for digitizing.

## 6C-7. Probe Tip Cal

The Probe Tip Cal uses a triggering technique to measure where the CAL signal from the front panel triggers the system. The front panel CAL signal is calibrated independently from the operating system. The cal factors are stored and used to manipulate acquired data.

The vertical specifications of the HP 54111D are based on calibration of the vertical system through the probe. Changing the probe at an input nullifies the calibration of that channel or trigger. Restoring calibration at that input requires a Probe Tip Cal of that input.

Use of Probe Tip Cal in service procedures is accompanied by instructions appropriate to the procedure. Other information about Probe Tip Cal can be found in the Utility Menu chapter of the *HP 54111D Operating and Programming Manual*.

## 6C-8. Vertical Cal

Vertical Cal sets gain and offset coefficients in firmware for vernier control. Front panel inputs aren't needed. Internal signals are supplied through an internal input to the attenuator preamp.

## 6C-9. Trigger Cal

Trigger Cal is a trigger level and sensitivity calibration. There are no input signals used for this calibration and the user needs only to follow the prompts on the screen to remove any signals before the routine is run.

The firmware sets the trigger level and hysteresis (sensitivity).

## 6C-10. Timebase Cal

### 6C-11. CHANNEL SKEW

Channel Skew compensates the time differences between the channel displays and triggers. A common signal is applied to the CHAN 1 input and the other inputs, CHAN 2, TRIG 3, and TRIG 4 in turn. A measure routine finds the edges of the signals, and the time difference between them is stored and used to time-align displayed signals and triggers.

For the vertical channels, the reference points are the offset voltage (vertical center screen) for the displayed signals and the trigger levels for the triggers.

For the trigger channels, the reference is the trigger level.

The procedure for this calibration is covered in the Adjustment procedures, the *HP 54111D Operating and Programming manual*, or you can follow the prompts on the display in the Channel Skew menu.

### 6C-12. TIMEBASE FREQ CAL

Timebase Frequency Cal is used to improve the accuracy of the instrument timebase. The timebase reference is a 1.001 GHz oscillator. It sets the sample rates for acquisition, and is therefore the timing standard in the instrument.

By measuring this frequency, and entering the measurement at the menu provided, the firmware in the instrument can compensate timing measurements for any error in the oscillator.

Restoring Timebase Frequency Cal may require using a traceable frequency counter if instrument use warrants it. If the cal factor was recorded when the instrument was last calibrated, calibration can be restored by re-entering the cal factor. If the cal factor is not known it is necessary to re-measure the Timebase Cal signal and enter the new value. Use the procedure in this section or follow the directions in the Timebase Freq Cal menu of the instrument.

The frequency measured is nominaly 50.05 MHz, the timebase reference divided by 20. When the Timebase Freq Cal menu is entered the signal is provided at a rear panel connector. The exact frequency should be measured with an accurate frequency counter and the resulting value entered in the menu.

The procedure for this calibration is covered in the Adjustment procedures, the *HP 54111D Operting and Programming Manual*, or you can follow the instructions in the Timebase Freq Cal menu.

## 6C-13. TEST MENU

Five sub-menus are available when the Test Menu is selected. The menus allow the user to access and run internal diagnostics and view the results. In addition, the position of each of the printed circuit boards located in the main card cage can be read and displayed.

Use of the test menus is covered in depth in section 6D, Troubleshooting.

## 6C-14. Repeat Loop/Run From Loop

The top key toggles between REPEAT LOOP and RUN FROM LOOP. These keys in conjunction with Loop # = [0-80], # Repetitions = [1-1000 or Infinite], and Start/Stop Test key will execute internal self-test diagnostic routines. All input signals must be disconnected from the instrument for these tests.

**REPEAT LOOP.** Selecting this mode will continuously execute the Loop # entered at RUN FROM LOOP. Pressing ***Start Test*** will start execution and the loop will continuously run until the ***Stop Test*** key is pressed. Pressing ***Display Errors*** will show how many times the loop was executed and the number times the loop failed.

Entering a value in # Repetitions will cause the firmware to run the designated loop that many times and stop. Start the test at REPEAT LOOP.

There are a number of loops that will blank or over-write the Stop Test key display on the CRT. However, the test can still be terminated by pressing the third function key from the top.

**RUN FROM LOOP.** Selecting this mode will start execution from the loop entered and will proceed to execute all higher numbered loops. Upon reaching the last test, the cycle will be repeated.

If any test should fail, the instrument will change from RUN FROM LOOP to REPEAT LOOP and will repeatedly execute the loop that failed.

Starting tests at RUN FROM LOOP will set the number of repetitions (entered at REPEAT LOOP) to infinite.

## 6C-15. Extended Tests

When this key is pressed, one of twenty-one internal instrument tests may be selected by entering the test number with the entry devices. The tests are numbered 0 through 20. All input signals must be disconnected from the instrument for these tests.

Many of the extended tests are useful only at the factory. Those that are of use to field service personnel are covered in the troubleshooting in section 6D.

## 6C-16. Start/Stop Test

This key is used to initiate any test where a test number is entered by one of the entry devices. Once the test number is entered, pressing ***Start Test*** initiates the test and the key toggles to ***Stop Test***. Pressing ***Stop Test*** stops the test in progress and the key toggles back to ***Start Test***.

A number of tests will blank or over-write the ***Stop Test*** key display on the CRT. However, the test can still be terminated by pressing the third function key from the top.

## 6C-17. Display Errors

Pressing this key will display the number of any loops which failed while one of the following tests was run:

- Powerup self test
- INTERFACE tests
- REPEAT and RUN FROM LOOP tests
- HP-IB commanded self test

This display shows the current loop or last loop executed, the number of times the loop was executed, and the number of times that it failed. The bottom portion of the display shows all loops that failed starting with the first loop failure.

The four STATUS x = xxxxx lines in the Display Errors field are primarily for factory use. Any field usable information in this part of the display is covered in the troubleshooting, section 6D.

To return to the Test Menu, press ***Exit Display Menu*** key.

## 6C-18. Display Configuration

Most major assemblies used in the HP 54111D have circuitry allowing them to be interrogated directly by the microprocessor. The exceptions are the Analog to Digital Converter (ADC) assemblies. The HP 54111D card cage has 9 slots. When ***Display Configuration*** is pressed, the resulting display shows the location of card cage assemblies, except the ADCs. The Microprocessor assembly will not be noted on the display either.

The display also shows the firmware date, such as Wed April 22 09:07:02 MST 1987.

To return to the Test Menu, press ***Exit Display Menu*** key.

## 6C-19. CRT SETUP MENU

When CRT Setup Menu is selected, four keys are displayed that allow access to CRT setup displays. The keys available are, from top to bottom, Confidence Test, Pattern Off, Light Output Off, Color Purity Off, and at the bottom, Exit CRT Setup Menu.

Even though some of the patterns overwrite the key display, the functions can be selected. The bottom key can be pressed at any time to exit the CRT Setup Menu.

## 6C-20. Confidence Test

This function displays a three-part confidence test pattern. At the top of the screen is a complete character set, in the center is a group of seven color blocks, and at the bottom a seven block grey-scale.

The top four lines of the character set display include the complete character set. The bottom line displays three sets of numerals. The first set is displayed in inverse video, the second set flashes between normal and inverse video and the third set is normal video and underlined.

The seven color blocks displayed at the center are, from left to right; beige, grey, red, yellow, green, amber, and cyan.

**NOTE**

*Since color perception is subjective, any slight variation in colors from what is described here should be disregarded.*

At the bottom of the CRT a seven block grey-scale is displayed, with increasing luminosity from left to right. This grey-scale display is used if Color CRT Module adjustments are necessary.

## 6C-21. Pattern

These patterns are used when Color CRT Module adjustments are necessary. When CRT Setup Menu is selected, this key is initially ***Pattern Off***.

Pressing ***Pattern Off*** once will display a white cross-hatch pattern over the entire CRT and the Pattern Off key changes to Pattern White. Inside the cross-hatch pattern there are dots at the center, corners, and at the 12, 3, 6 and 9 o'clock positions. Additionally, there are test matrices in the center and corners.

Pressing ***Pattern White*** key changes the pattern color to red and the key changes to Pattern Red. Successive pressings of this key will change the color of the pattern to green then blue, the name of the Pattern key is the color displayed.

Pressing ***Pattern Blue*** key changes the display to the white cross- hatch pattern on the top half of the CRT and white with a dark cross-hatch on the bottom. The key then changes to Pattern HV Reg. This test is used primarily by the factory, however it may indicate the need for service if there are severe high voltage problems.

Pressing ***Pattern HV Reg*** changes the display to a solid white screen with dark cross hatch lines. The key changes to Pattern I White. Successive pressing of this key changes the color to red, green and then blue, the name of the Pattern key is again the color of the display.

Pressing ***Pattern I Blue*** changes the display to a white cross- hatch pattern with the inside flashing between solid white and cross- hatch. The key changes to Pattern Bounce. This test is primarily used by the factory, however, it may indicate the need for service if there are severe high voltage problems.

Pressing ***Pattern Bounce*** exits this set of tests and returns the CRT Setup Menu.

## 6C-22. Light Output

These displays are used by the factory.

Pressing ***Light Output White*** displays a horizontal band of white half the height of the display. The key display is not overwritten. Successive pressing of this key will change the color of this band to red, green, blue and then a grey-scale. Each time the key is pressed it also changes to the appropriate description.

Pressing ***Light Output Grey-Scale*** exits this set of tests and returns the CRT Setup Menu.

## 6C-23. Color Purity

Pressing ***Color Purity Off*** displays a full white raster. Successive pressing of this key changes the color of the raster to red, green and then blue. At each color display the name of the key changes to the appropriate description. These displays are used when Color CRT Module adjustments are necessary.

Pressing ***Color Purity Blue*** exits this set of tests and returns the CRT Setup Menu.

# SECTION 6D
# SELF-TESTS/TROUBLESHOOTING

## 6D-1. INTRODUCTION

This section describes the self-tests and troubleshooting routines that service personnel can use to locate failures to the assembly level. A basic understanding of the service menus and keys will be helpful in troubleshooting failures and is covered specifically in Section 6C.

The material presented in this section is in only a general order of importance, or use. Depending on the problem encountered, troubleshooting may progress back and fourth within the section but should start with the Main Troubleshooting Procedure.

Following are the troubleshooting sections in order of appearance:

- Main Troubleshooting
- "No Display" Troubleshooting
- Power Supply Troubleshooting
- Color CRT Module Failure Isolation
- Firmware Troubleshooting
- Core Subsystem Troubleshooting
- Data Acquisition Troubleshooting
- Front End Troubleshooting
- Hints, Tricks, and Arcana

## 6D-2. FAILURE INDICATIONS

The majority of failures in the HP 54111D are initially indicated in one of several ways: improper display (blank, distorted, or random) on the CRT after power-up, the keyboard is locked after power up, or "Powerup Self Test Failed !" is displayed on the CRT.

Other failures may be apparent during normal operation, but most problems are caught by the internal self-test routines and will result in one of the indications mentioned.

Loop failures may occur occasionally due to system or environmental noise. This may result in intermittent power-up failure messages. Loops must fail a certain percentage of the time to be considered a true failure and must be specially tested if random failures are occuring. See Main Troubleshooting for further information and procedures.

**NOTE**

*In addition to the front panel power switch (STBY), there is a main breaker power switch located on the rear panel. Before troubleshooting a "no display" failure, make sure the rear panel switch has not been inadvertently turned off.*

## 6D-3. TEST EQUIPMENT REQUIRED

The HP 54100 Family Product Support Kit consists of assembly and cable extenders and other tools. Some of the parts in this kit are necessary for certain assembly level diagnostic procedures. These procedures aid in troubleshooting, but are not necessary for troubleshooting most failures.

In addition, other than the equipment required for performance tests and adjustments, all that is needed is a general purpose 300 MHz oscilloscope such as the HP 54201A.

## 6D-4. ONE-KEY POWER UP

A one-key power up is often performed to return the instrument setup to default conditions. This is done as follows:

1. Set the front panel POWER switch to STBY,
2. Press and hold one front panel key,
3. Turn front panel POWER switch to ON.
4. Release key when display shows "Powerup Self Test Passed!" or Failed.

## 6C-5. TWO-KEY POWER UP

CAUTION

*Using the two-key power up will leave the instrument uncalibrated. Effort needed for recalibration should be considered before using this method to reset the instrument. Calibration traceability will be lost if a two-key powerup is used.*

A two-key power up is a basic reset of the entire operating system of the HP 54111D. All volatile and non-volatile RAM is cleared. As a result, all calibration factors are purged and the instrument must be recalibrated.

All calibration except the Timebase Cals can be done with just the front panel CAL signal and the self-cal menus. The two-key power up is performed in much the same way as the one-key power up.

1. Set the front panel POWER switch to STBY.
2. Press and hold the top and bottom keys in the group at the right edge of the display.
3. Turn front panel POWER switch to ON.
4. Release keys when display shows "Powerup Self Test Passed!" or Failed.

## 6D-6. MAIN TROUBLESHOOTING

Figure 1, Main Troubleshooting Flow Diagram, should be used as the initial and primary troubleshooting procedure.

CAUTION

*If the instrument you are servicing is traceably calibrated, try to record the TIMEBASE FREQUENCY CALIBRATION FACTOR before the two-key powerup. This procedure deletes this cal factor! Once the instrument is repaired, the traceable calibration can be restored by reentering the cal factor, or recalibration with a traceable frequency counter.*

## 6D-7. Powerup Self Tests

When instrument power is applied the powerup self tests will be initiated, and the message "Power-up Self Test in Progress" will be displayed. As the tests progress, the message "Last Loop Completed nn" will be displayed. The number "nn" is the loop number of the present test. Many tests run too quickly to recognize the number. For firmware dates later than April 22, 1987, the number of any failed test will appear in red and a slight delay will allow the test number to be recognized. If they have been disabled (see extended Test 22), the message "Powerup Self Test Disabled !" will be displayed.

Unless the instrument warmup function has occured (see Instrument Warmup), failed tests result in the message "Powerup Self Test Failed" on the display.

## 6D-8. Instrument Warm-up

Under certain conditions the message "Instrument Warm-up in Progress mm:ss" may appear, in red, in the display. The time, in minutes and seconds, starts at 15:00 and counts down to zero. If the instrument passes all power-up tests at initial turn on there will be no warm-up indication on the display.

This message has no relationship with instrument temperature. If the instrument fails any of certain powerup self tests, specifically loops 26-31 (channel 1) or 35-40 (channel 2), the instrument will first assume that failure is due to lack of warm-up and display the message. If any of test loops 41,42 (channel 1) or 43,44 (channel 2) also fail, and if these additional failures are in the same channel as the first failures, the instrument will assume these failures are connected with the first and treat them the same. The instrument will not display a "Powerup Self Test Failed !" message for warm-up specific failures but will display it if other tests fail.

For example: if any of loops 26-31 and 41 or 42 (channel 1) fail, with no other failures, only the warmup message will be displayed. If

loops 43 or 44 also fail, there will be both warmup and self test failed messages.

At five minute intervals of the timer, the instrument will initiate the power-up self-test routine. If the specific tests pass, the warm-up message will end. If the tests do not pass, the warmup message will stay and the timer will start where it left off before the self-test routine was initiated. If loops 26-31 or 35-40 pass but 41-44 are still failing, the warmup message will end but the self test failed message will be displayed.

There will be a final initiation of powerup self tests at 00:00 of the timer. If the instrument still does not pass these tests, only the "Powerup Self Test Failed !" message will be displayed.

If the Automatic Warmup Retest (Extended Test 10) has been turned OFF, failure of these warmup dependent tests will result in display of "Powerup Self Test Failed !"

## 6D-9. Connectors

Most instruments are sensitive to connectors and assemblies that are not completely seated. So one of the initial steps, before starting troubleshooting, should be to make a mechanical check of all the connectors and assemblies to make sure that everything is properly seated.

Check the coaxial connectors, ensure that the ribbon connectors are completely snapped in place, and press down firmly on card cage assemblies to ensure proper seating.

## 6D-10. System Lock-up

After running the power-up self tests the instrument may be locked up by a system error, it will not respond to the keyboard. This can be a random failure or a hard failure. An error message such as one of the following,

```
SYSTEM  ERROR! Zero Divide XXXXXXH
SYSTEM  ERROR! Bus Error XXXXXXH
SYSTEM  ERROR! Address Error XXXXXXH
```

will be displayed on screen, followed by

```
To clear, cycle power with one front-panel key
pressed. If the error condition remains please
consult the service manual.
```

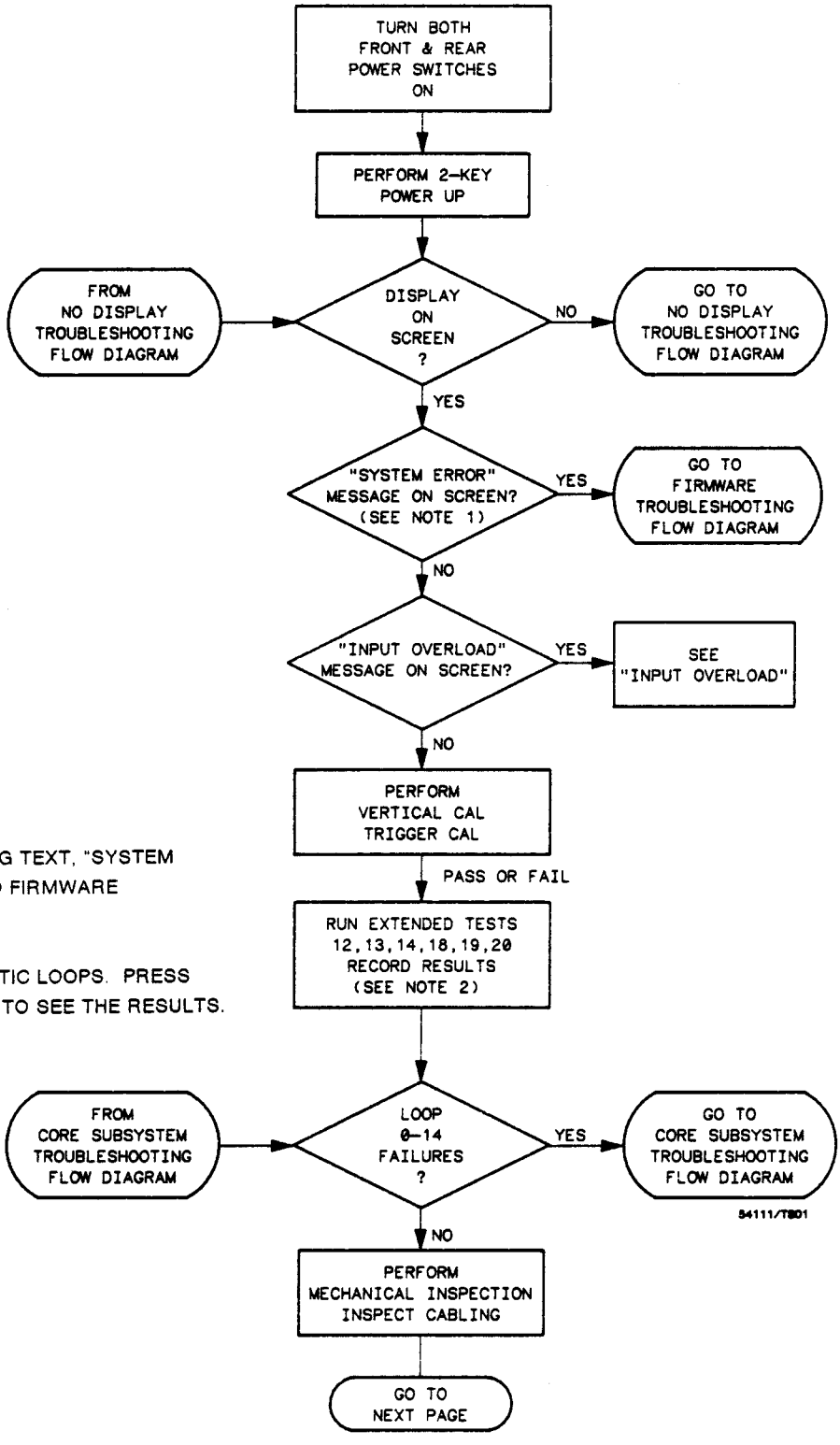
Note the hex number (XXXXXXH) after the error message. This may be useful if help from an HP Service Center is needed later.

Try to use the one key power-up to reset the instrument. If the instrument is failing after a one key power-up and calibration traceability need not be maintained, try a reset using the two key power-up.

**CAUTION**

*Using the two-key power up will leave the instrument uncalibrated. Effort needed for recalibration should be considered before using this mode to reset the instrument. Calibration traceability will be lost if a two-key powerup is used.*

If the instrument is still failing, try to obtain information about the failure mode by "breaking in" to the power-up routine before the system becomes locked. Go to Firmware Troubleshooting for further information.




**NOTES**

1. SEE MAIN TROUBLESHOOTING TEXT, "SYSTEM LOCK-UP", BEFORE GOING TO FIRMWARE TROUBLESHOOTING.

2. TEST 12 RUNS THE DIAGNOSTIC LOOPS. PRESS THE "DISPLAY ERRORS" KEY TO SEE THE RESULTS.

*Figure 6D-1. Main Troubleshooting Flow Diagram (part 1)*

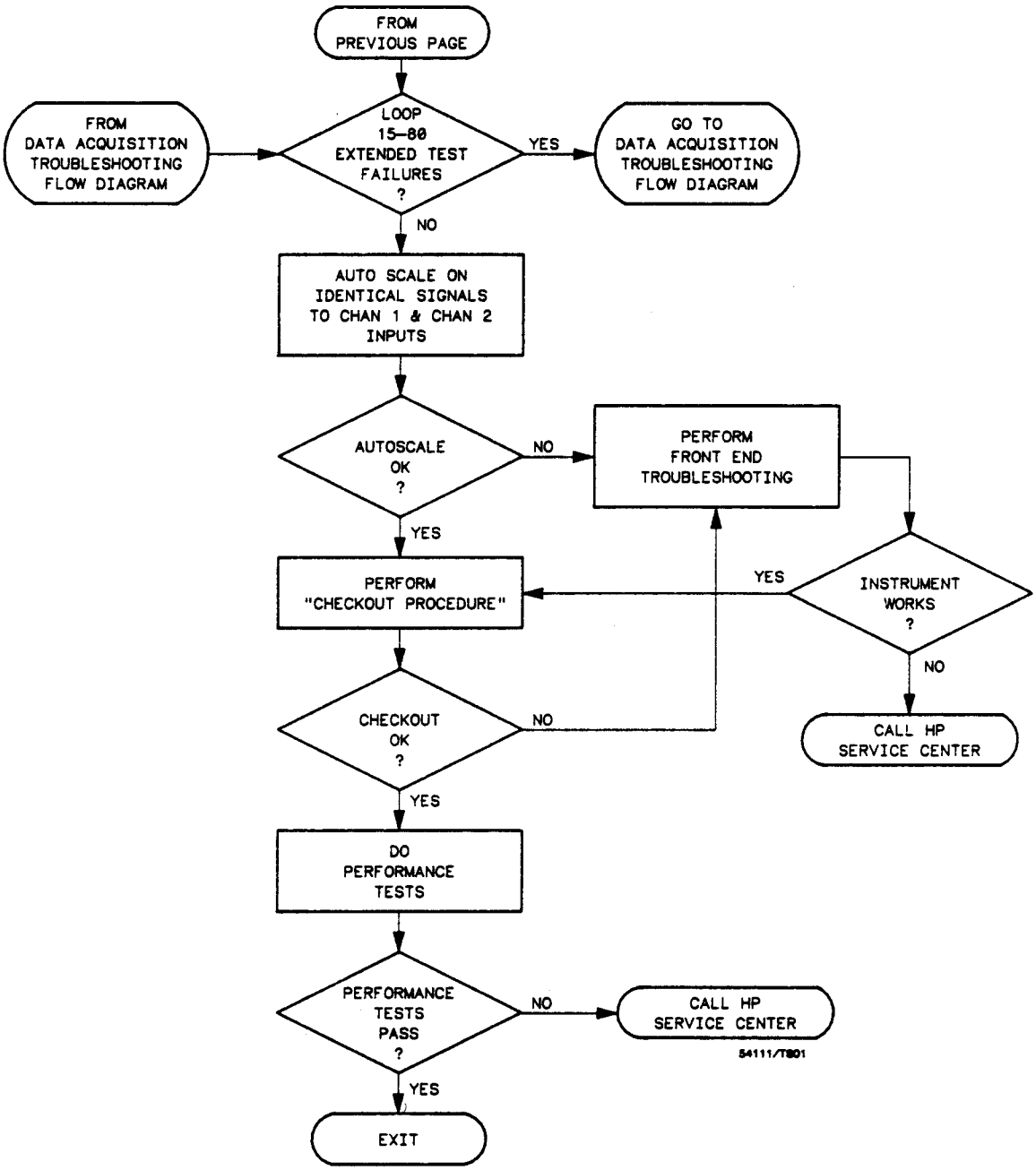



*Figure 6D-2. Main Troubleshooting Flow Diagram (part 2)*

## 6D-11. Input Overload

If an Input Overload message is displayed on screen immediately after power-up the cause is usually an input sense cable that has become disconnected or mis-connected. This failure also results in lock-up of the instrument; there will be no response to the keyboard.

**NOTE**

*Do not do any other troubleshooting until the problem causing this Input Overload message has been corrected.*

**CAUTION**

*Do not perform a two-key powerup. The instrument will be harder to return to proper operation.*

Use the following procedure to check for this problem.

1. Turn the POWER to STBY.
2. Remove the covers (see section 6A).
3. Ensure that all of the input sense cables are properly connected. (See the diagram on the cover of the instrument or at the end of section 6A.)
4. If the instrument still fails to power up properly, continue with troubleshooting based on known symptoms.

If a two-key powerup was performed, it may be necessary to clear the non-volitile RAM manually by using the following procedure.

1. Turn POWER to STBY.
2. Pull the Microprocessor assembly clear of the motherboard. This separates the RAM from its battery supply on the I/O assembly. Leave separated for several seconds.
3. Re-insert Microprocessor assembly and apply power. Instrument should power up and display a message that calibration is needed.

## 6D-12. Intermittent Failures

Loop failures that are intermittent may not be true failures. A loop must fail more than one percent of the time to be considered a true failure. If a loop seems to be intermittent it should be run in the REPEAT LOOP mode to determine the failure percentage.

Use the following procedure to check the failure percentage of a given loop.

1. Press ***more, Utility***, and ***Test menu***.
2. Press the top softkey to get ***RUN FROM LOOP*** and ENTER the Loop # with the ENTRY keys.
3. Press ***RUN FROM LOOP*** to get ***REPEAT LOOP*** and ENTER the # Repetitions with the ENTRY keys. The number of repetitions must be high enough to get a proper sampling. Checking for one percent of errors will need several hundred repetitions for a good sample.
4. Press ***Start Test***. Several hundred samples may take a few minutes to complete. You can press ***Stop Test*** then ***Display Errors*** to check on the progress of the test but starting the test again will start it at the beginning.
5. When the display returns to the test menu press ***Display Errors*** to check the error rate. If ***Failures*** = is greater than one percent of ***Executions*** = the loop has a true failure.

## 6D-13. NO-DISPLAY TROUBLE-SHOOTING

Check to see whether the power supply is functioning correctly by checking the four LEDs that indicate supply function. One is located on the I/O assembly (A3), and the others are located on the primary, digital, and analog power supply assemblies. If any of these LEDs is not lit, proceed directly with the Power Supply Troubleshooting procedures.

Use a voltmeter to check the voltages at the test points on the power supply. If voltages are not correct (see Power Supply Troubleshooting) proceed with the Power Supply Troubleshooting procedure.

If the supplies are correct and there is still no display, cycle the power with the front panel switch. If the display produces a normal flash at powerup and powerdown, the Color CRT Monitor is probably working. If it does not light at all, check if the 120 V LED at the front of the Primary Supply is lit. If it is, outrig a working Color CRT Module (see Color CRT Module Outrigging). Replace Color CRT Module if outrigged module works. If outrigged module does not work, see Power Supply Troubleshooting procedure.

If the display lights, determine whether the problem is in the Color Display assembly or in the Color CRT Module, as follows:

1. Check the voltage on the 120 Volt pin on the Color CRT Module; also check the Red, Blue, and Green Video signals. If these signals are correct (see Color CRT Module Failure Isolation) then outrig a new Color CRT Module and test it. If it works, replace the module.

2. If they are not correct, the display assembly is suspect. Check the +/- 5 Volts on the display assembly and the Vertical and Horizontal Sync signals coming from the display assembly. If these are not present, the Color Display assembly is suspect. Remove assemblies not in the core subsystem and proceed with verifying its operation (see Core Subsystem Troubleshooting).

If you have not been able to find the problem using these techniques, call your HP Service Center.

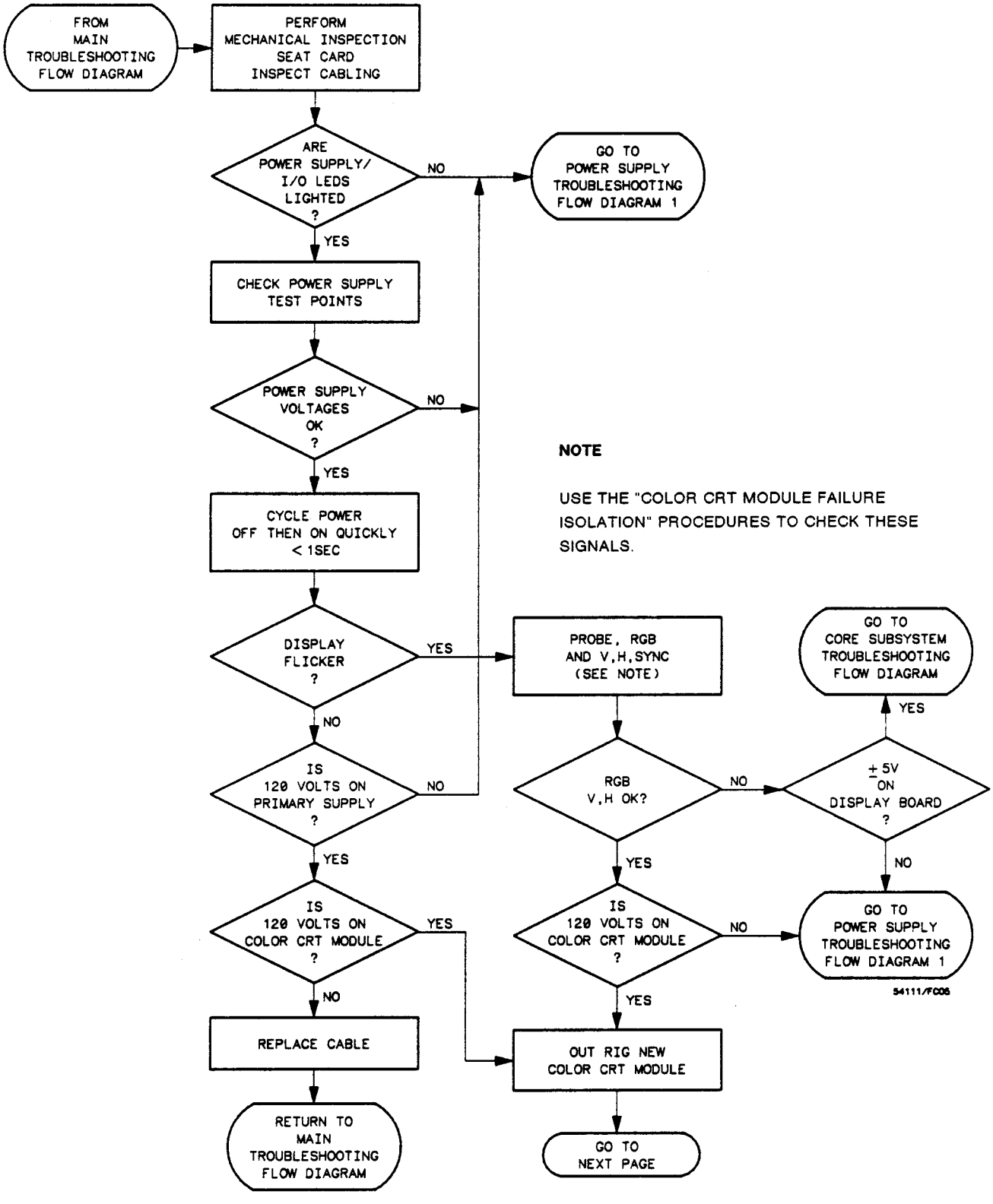



*Figure 6D-3. No Display Troubleshooting Flow Diagram (part 1)*

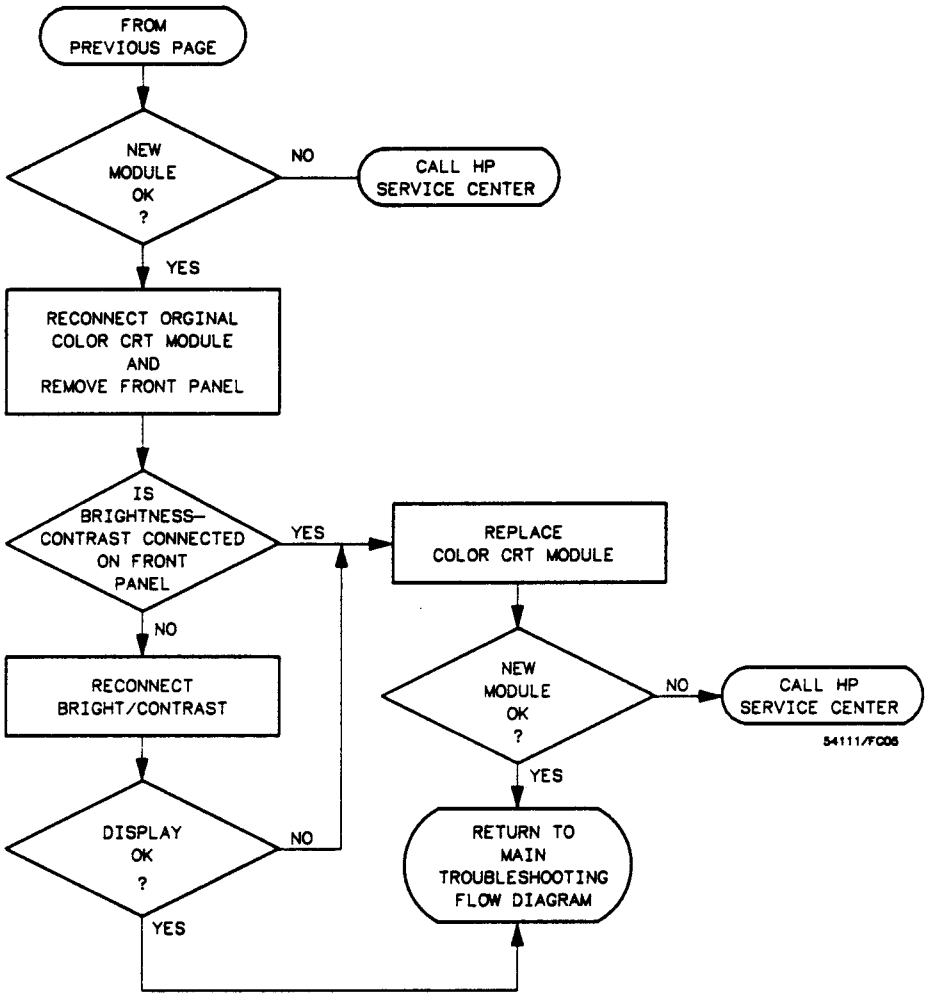



*Figure 6D-4. No Display Troubleshooting Flow Diagram (part 2)*

**NOTES**

## 6D-14. POWER SUPPLY TROUBLE-SHOOTING

When a power supply problem is suspected, it is first important to make sure that no unusual load is keeping the supply in a current limited condition. The table below shows which supplies are used on each assembly.

1. If the 300V LED on the Primary Supply is not lit go directly to the Power Supply Troubleshooting Flow Diagram on the next page.

2. If the 300V LED is lit, find the LEDs on the Analog and Digital supplies and I/O assembly. They are near the top-front of each assembly, so if you cannot see them they are probably not lit.

3. If the LEDs are lit and you still suspect a supply problem, go to the Power Supply Troubleshooting Flow Diagram on the next page.

4. If the LEDs are not lit continue with this procedure before going to the Power Supply Troubleshooting Flow Diagram on the next page.

**CAUTION**

*Always turn front panel POWER to STBY before removing and inserting assemblies and be sure to use proper ESD precautions.*

5. At the right side of the instrument, pull up the Trigger Qualifier assembly until it clears the motherboard connector, about one half inch.

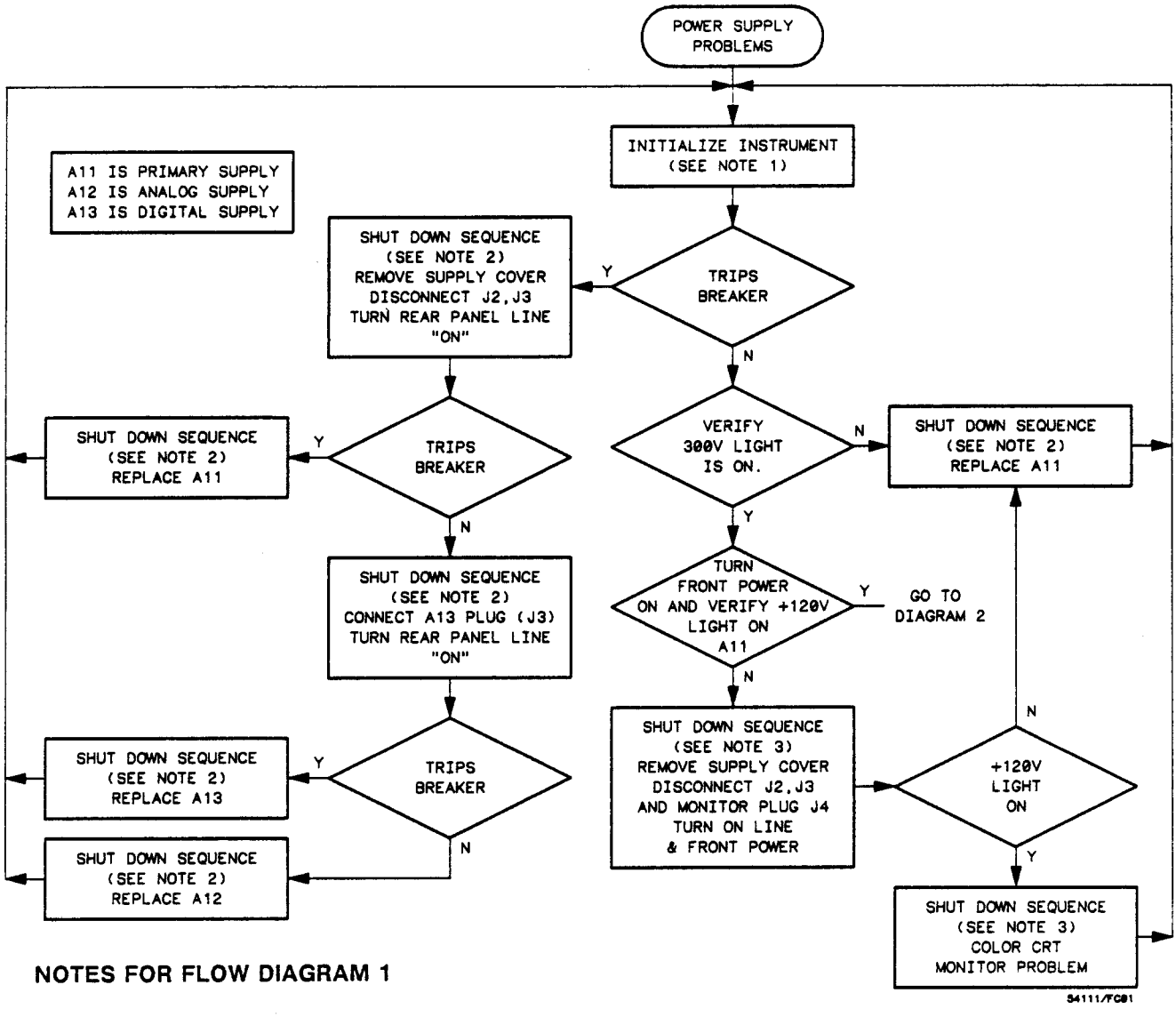
6. Check to see if the LEDs are lit. If the LEDs are lit troubleshoot the Trigger Qualifier for excessive loading. If they are not lit, leave the assembly up and go to the next step.

7. Working from right to left, pull up each card cage assembly while watching for the LEDs to light. If they light, troubleshoot for excessive loading, the last assembly pulled up.

8. After the I/O assembly is pulled up, watch only for the supply LEDs. If all nine card cage assemblies are up, and the supply LEDs are not lit, go to the following Power Supply Troubleshooting Flow Diagram.

*Table 6D-1. Power Supply Distribution.*

| | +5V | -5V | +18V | +8V | -8V | -18V | +120V |
|---|---|---|---|---|---|---|---|
| TIMEBASE | * | | * | * | * | * | |
| MICROPROCESSOR | * | | | | | | |
| INPUT/OUTPUT † | * | * | * | * | * | * | |
| CH1 ADC CONT | * | * | * | * | * | * | |
| CH1 ADC | * | | * | | * | * | |
| CH2 ADC CONT | * | * | * | * | * | * | |
| CH2 ADC | * | | * | | * | * | |
| TRIGGER | * | * | * | * | * | * | |
| TRIGGER QUAL | * | * | | * | * | | |
| COLOR DISPLAY | * | | | | | | |
| COLOR CRT MOD. | | | | | | | * |




## NOTES FOR FLOW DIAGRAM 1

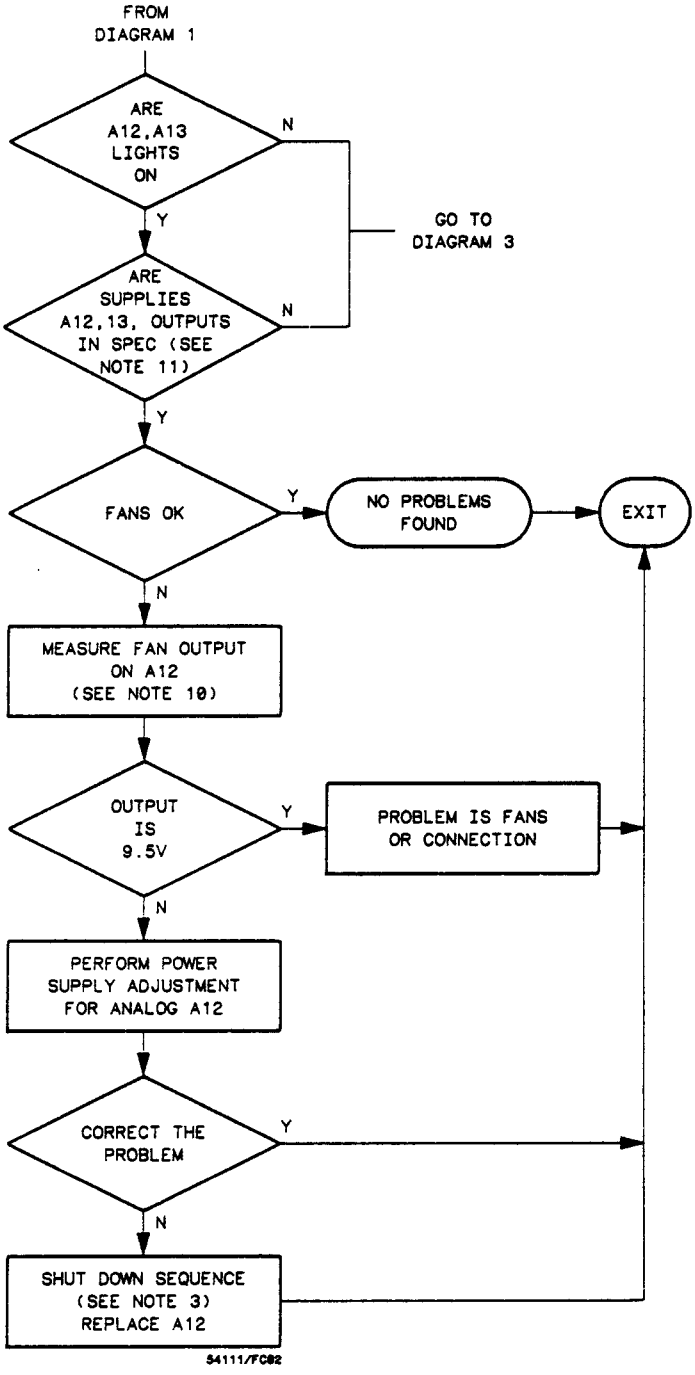
1) A. FRONT PANEL POWER SWITCH SHOULD BE IN STANDBY
   B. REAR PANEL LINE SWITCH SHOULD BE OFF "0"
   C. CONNECT AC POWER SOURCE
   D. TURN REAR PANEL LINE SWITCH TO ON "1"

2) A. TURN REAR PANEL LINE SWITCH TO OFF "0"
   B. ALWAYS UNPLUG AC POWER SOURCE
   C. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

*WARNING*
EXTREME CAUTION MUST BE TAKEN WHEN REMOVING POWER SUPPLY COVER.

3) A. TURN FRONT PANEL SWITCH TO STANDBY
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

*Figure 6D-5. Power Supply Troubleshooting Flow Diagram 1.*




## NOTES FOR FLOW DIAGRAM 2

3) A. TURN FRONT PANEL SWITCH TO STANDBY
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

10) CONNECT THE VOLTMETER (+) LEAD TO THE "FAN" TEST POINT AND THE (-) LEAD TO THE -18V TEST POINT. THE READING SHOULD BE 9.5V. THIS VOLTAGE WILL INCREASE WITH INCREASING AMBIENT TEMPERATURE. SEE THE POWER SUPPLY ADJUSTMENT PROCEDURE FOR THE ANALOG SUPPLY.

11) FOR POWER SUPPLY TEST POINTS AND SPECIFICATIONS SEE TABLE BELOW.

| DIGITAL SUPPLY TST PTS (+) LEAD | (-) LEAD | VOLTAGE |
|---|---|---|
| +5V | GND | +5.10 ±0.1V |
| -5V | GND | -5.30 ±0.1V |
| +14B | GND | >+5V |
| **ANALOG SUPPLY TST PTS (+) LEAD** | **(-) LEAD** | **VOLTAGE** |
| +18V | GND | +18.5 ±0.3V |
| +8V | GND | +8.9 ±1V |
| -8V | GND | -8.5 ±1V |
| -18V | GND | -18.5 ±0.3V |
| FAN | -18V | +9.5 ±0.3V |
| +26B | GND | >+5V |

*Figure 6D-6. Power Supply Troubleshooting Flow Diagram 2.*

## NOTES FOR FLOW DIAGRAM 3

3) A. TURN FRONT PANEL SWITCH TO STANDBY
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

4) THE NOMINAL OUTPUT FOR +14B IS 21V. HOWEVER, WHEN THE SUPPLY IS OPERATING IN THE CURRENT LIMIT MODE, IT CAN BE AS LOW AS +5V. THE NOMINAL OUTPUT FOR +26B IS 26V. IT TOO CAN BE AS LOW AS +5V WHEN IN CURRENT LIMIT.

5) MEASURE OUTPUTS +5V AND -5V ON THE DIGITAL POWER SUPPLY. IF BOTH OUTPUTS ARE LOW, I.E. HALF OF NORMAL OUTPUT OR LESS, THEN DIRECTION TO TAKE IS YES. IF OUTPUTS ARE GREATER THAN HALF THE ANSWER IS NO.

7) MEASURE OUTPUTS ±18V AND ±8V ON THE ANALOG SUPPLY. IF BOTH OUTPUTS ARE LOW, I.E. HALF OF NORMAL OUTPUT OR LESS, THEN DIRECTION TO TAKE IS YES. IF OUTPUTS ARE GREATER THAN HALF THE ANSWER IS NO.

8) THE TEST POINTS TO MEASURE +14.6V ARE AT THE BACK OF THE BOARD CLOSE TO THE TOP. CONNECT THE VOLTMETER COMMON LEAD TO THE COM TEST POINT ON THE BOARD. **CAUTION!!!** ***USE CAUTION WHEN MEASURING THIS VOLTAGE. IT IS NOT ISOLATED FROM THE LINE (MAINS) INPUT AND THE PRIMARY SUPPLY IS EXPOSED WITH THE POWER SUPPLY COVER REMOVED.***

9) BY REMOVING THE CONNECTORS AT J2 AND J3 YOU ARE CHECKING IF EITHER THE ANALOG OR DIGITAL SUPPLY IS LOADING VCNTL.

   EXTREME CAUTION MUST BE TAKEN WHEN MEASURING VCNTL ON THE PRIMARY SUPPLY. THE TOP PIN ON CONNECTORS J2 AND J3 IS VBULK WHICH IS +300V. THE PINS BELOW ARE VCNTL, THEN GROUND.

   TO MEASURE VCNTL, TURN THE POWER OFF AND MAKE SURE THE +300V LAMP (NEAR TOP OF BOARD) IS OFF. CONNECT THE VOLTMETER (+) LEAD TO VCNTL (SECOND PIN FROM TOP) AND THE (-) LEAD TO GROUND (BOTTOM PIN). APPLY POWER AND OBSERVE THE METER READING. WITH ONE SUPPLY CONNECTED THE READING SHOULD BE ABOUT +25V AND WITH NEITHER CONNECTED ABOUT +42V. TURN OFF POWER (+300V LAMP IS OFF) BEFORE REMOVING THE VOLTMETER LEADS.

---

6) WHEN THE SUPPLIE(S) ARE RUNNING IN THE CURRENT MODE THIS MEANS THAT AN EXTERNAL LOAD IS PULLING DOWN THE SUPPLY OUTPUT(S). AN EXTERNAL LOAD COULD BE AN ASSEMBLY IN THE CARD CAGE OR THE COLOR DISPLAY ASSEMBLY (NOT THE COLOR CRT MODULE). THE ONLY WAY TO ISOLATE THE COLOR DISPLAY ASSEMBLY IS TO COMPLETELY REMOVE IT FROM THE MAINFRAME. THE FANS CAN ALSO PUT THE ANALOG SUPPLY INTO THE CURRENT MODE. YOU CAN DISCONNECT THE FANS BY REMOVING THE BOTTOM COVER AND DISCONNECTING THE FAN CABLE.

| | +5V | -5V | +18V | +8V | -8V | -18V | +120V |
|---|---|---|---|---|---|---|---|
| TIMEBASE | * | | * | * | * | * | |
| MICROPROCESSOR | * | | | | | | |
| INPUT/OUTPUT † | * | * | * | * | * | * | |
| CH1 ADC CONT | * | * | * | * | * | * | |
| CH1 ADC | * | | * | | * | * | |
| CH2 ADC CONT | * | * | * | * | * | * | |
| CH2 ADC | * | | * | | * | * | |
| TRIGGER | * | * | * | * | * | * | |
| TRIGGER QUAL | * | * | | * | * | | |
| COLOR DISPLAY | * | | | | | | |
| COLOR CRT MOD. | | | | | | | * |

†ONLY THE +5V IS USED FOR POWER. THE OTHER SUPPLIES CONNECT FOR POWER TEST ONLY AND ARE HIGH IMPEDANCE POINTS. LIKELYHOOD OF LOADING THESE SUPPLIES IS LOW.

TO ISOLATE A CURRENT PROBLEM, REMOVE ONE LOAD AT A TIME UNTIL THE PROBLEM IS FOUND. PROBLEMS COULD INCLUDE BENT PINS ON THE MOTHERBOARD OR A BAD COMPONENT ON A PC ASSEMBLY. SEE THE ADJACENT TABLE FOR POWER DISTRIBUTION TO THE VARIOUS ASSEMBLIES.

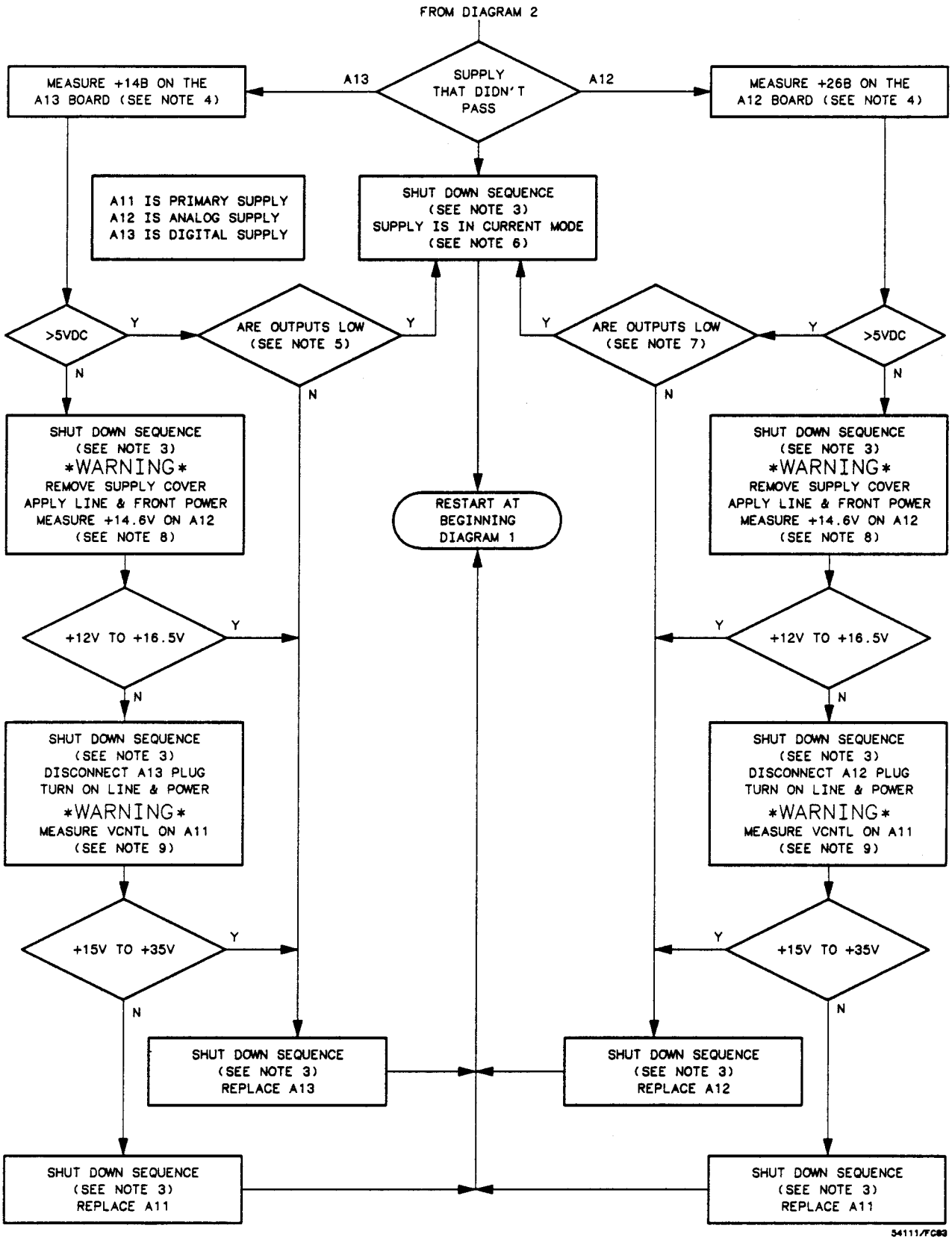



*Figure 6D-7. Power Supply Troubleshooting Flow Diagram 3.*

## 6D-15. COLOR CRT MODULE FAILURE ISOLATION

The following procedure causes the processor to write a known pattern of video to the module. The video waveforms, the vertical and horizontal sync signals, and the +120V primary module power are checked at the module inputs. If the inputs are present and correct, use the Color CRT Module Outrigging procedure to ensure that replacement of the module will correct the problem.

## 6D-16. Troubleshooting Procedure

1. Turn instrument to STBY using the front panel power switch.

2. Remove covers (see Instrument Disassembly, section 6A).

3. Turn power on and check the +120 V module power at the module power input connector (see next figure). The correct voltage will be between +118 and +122 volts. If the +120 V supply voltage is incorrect, see the power supply troubleshooting procedures.

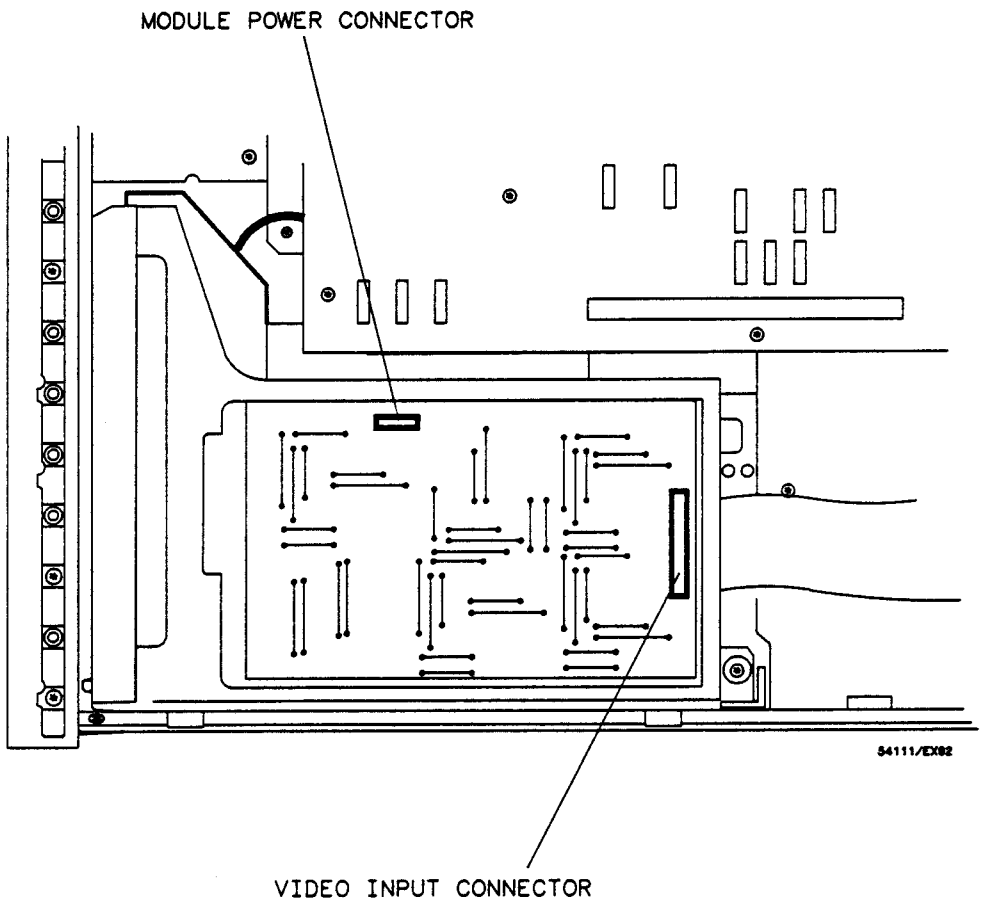



*Figure 6D-8. Color CRT Module Input Connections*

4. Move clear plastic board shield on bottom of Color CRT Module by pushing rearward until it clears front frame and hinge it away from the board.

5. With 10:1 divider probes, connect channel 1 of the monitor oscilloscope to vertical sync test point VD (located on module video input connector, pin 3) and channel 2 of the monitor oscilloscope to horizontal sync test point HD (located on module video input connector, pin 7). These test points are located on the Color CRT Module (A19). The vertical and horizontal sync signals are TTL levels and should resemble the waveforms in the following figure. The vertical sync is on the top and the horizontal sync on the bottom.

6. To see if the Color CRT Module is loading the signals, disconnect the wide ribbon cable at the Color Display assembly and check the signals at the two labled test points (VSYNC, HSYNC near U119) on the Color Display assembly.

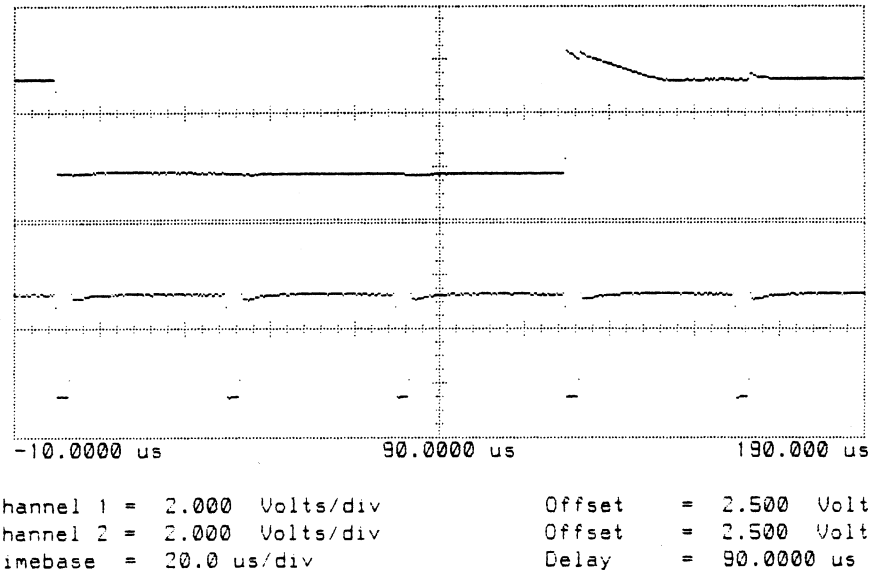



*Figure 6D-9. Vertical and Horizontal Sync Waveforms*

7. It is helpful to try to get a known display before checking the video waveforms. If the display is operating, press ***more, Utility, CRT Setup Menu***, and ***Color Purity***. This will give a white raster so all video signals will be at maximum.

   If there is no display, try to get the same signals using the following procedure.

   a. Turn instrument off, then on, then press the following softkeys, in order given.

   b. In bottom row press:
      Key at extreme right
      Key second from right
   c. In vertical column press:
      Key at bottom
      Key third from bottom

8. Check the red, green, and blue video signals at the module video input connector at pins 21, 29, and 37 respectively (see Color CRT Module Input Connections drawing).

   The video signals have a 0 V baseline and will vary in amplitude from 0 V to approximately +600 mV, depending on the characteristics of the colors displayed.

9. Video signals can be adversely loaded by input circuit failures within the Color CRT Display Module. Therefore, before assuming Color Dispaly assembly failures, repeat this test with the video cable disconnected from the Color CRT Module and the measurements taken at the pins of U145 on the Color Display assembly. The red, green, and blue signals are on U145 pins 14, 18, and 22 respectively.

## 6D-17. Incorrect Display Color

Using the CRT Setup Menu, then pressing the ***Color Purity*** key it is easy to locate a potentially defective CRT write gun or associated electronics. By pressing the ***Color Purity*** key several times the primary colors will be displayed. The colors displayed on the measurement screens are user definable, while the color purity check displays fixed primary colors.

## 6D-18. Module Outrigging Procedure

Due to the amount of work and time involved in changing the Color CRT Module it is prudent to verify the defective module diagnosis by outrigging a good module. Required parts which are part of the 54100 Family Support Kit are: Color CRT Module power cable, Display Control assembly, and Display Control Cable. Also necessary is a working Color CRT Module which is not part of the service kit.

1. Turn power off and remove instrument power cable.

2. Remove covers (see Instrument Disassembly, section 6A).

3. Disconnect Color CRT Module power cable at the primary power supply.

4. Connect the Color CRT Module power cable from the support kit to the primary power supply.

5. On the bottom of the instrument, disconnect the wide ribbon cable from the the suspect Color CRT Module and extend it as far as possible from the instrument when it is in a normal operating position.

6. Set the working Color CRT Module next to the instrument.

7. Connect the wide ribbon cable to working module.

8. Connect the module power cable to the mating connector towards the front of the CRT Module. This connection can be verified by noting that the connector is labled B-4 on the bottom of the PC board at the connector.

9. Connect the Display Control Cable from the support kit to the mating connector which is toward the rear of the module. This connector is labled B-2 on the bottom of the PC board.

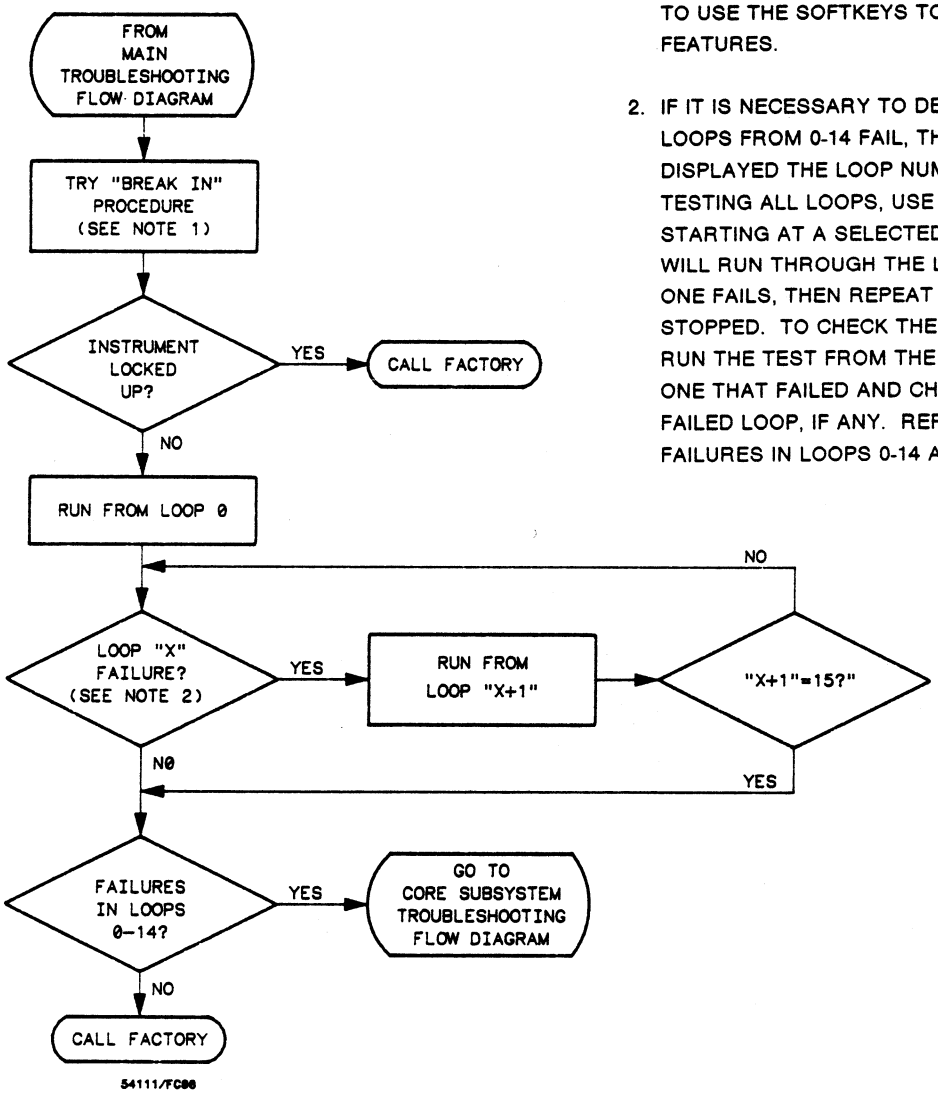
10. Connect the CRT Brightness Control from the support kit to the other end of the Display Control Cable.

11. Re-connect the power cord and turn instrument on.

12. Verify display operation.

## 6D-19. FIRMWARE TROUBLE-SHOOTING

Firmware troubleshooting is used to evaluate a firmware problem that prevents the instrument from displaying self-test information by locking up the keyboard. This routine is entered from the Main Troubleshooting Flow Diagram.




**NOTES**

1. THIS PROCEDURE MAY ALLOW YOU TO "BREAK IN" TO AN INSTRUMENT THAT IS LOCKING UP DURING THE POWERUP CYCLE. IT IS NECESSARY TO INTERRUPT THE POWERUP CYCLE BEFORE IT LOCKS UP THE INSTRUMENT.

   IF THE INSTRUMENT IS LOCKING UP, CYCLE THE POWER WITH THE STBY SWITCH. JUST AFTER "LAST LOOP . . . " DISAPPEARS, DURING THE POWERUP ROUTINE, PRESS THE STOP/SINGLE KEY. TIMING IS IMPORTANT HERE AND IT MAY TAKE SEVERAL TRIES TO "BREAK IN".

   WHEN BREAK IN IS SUCCESSFUL, YOU WILL BE ABLE TO USE THE SOFTKEYS TO ACCESS THE SELF TEST FEATURES.

2. IF IT IS NECESSARY TO DETERMINE WHICH OF THE LOOPS FROM 0-14 FAIL, THE INSTRUMENT HAS NOT DISPLAYED THE LOOP NUMBERS OR STOPS BEFORE TESTING ALL LOOPS, USE "RUN FROM LOOP". STARTING AT A SELECTED LOOP, THE INSTRUMENT WILL RUN THROUGH THE LOOPS UNTIL THE NEXT ONE FAILS, THEN REPEAT THAT LOOP UNTIL STOPPED. TO CHECK THE REST OF THE LOOPS, RUN THE TEST FROM THE LOOP AFTER THE LAST ONE THAT FAILED AND CHECK FOR THE NEXT FAILED LOOP, IF ANY. REPEAT THIS UNTIL ALL FAILURES IN LOOPS 0-14 ARE FOUND.

*Figure 6D-10. Firmware Troubleshooting Flow Diagram*

## 6D-20. CORE SUBSYSTEM TROUBLE-SHOOTING

### GENERAL

It is best to attempt to get the instrument to pass all the Core Tests before going on to fix more complex loops. Occasionally, bent motherboard pins or defects in other system elements will cause these loops to fail. By making a system of the Microprocessor assembly, I/O assembly and one other assembly, it is possible to determine which socket or assembly may be causing an interaction that causes one of the core loops to fail. Using this technique, seat each assembly into the motherboard one at a time. Be sure to turn the power off before raising or seating an assembly into the motherboard.

If only the Microprocessor and I/O assemblies are seated, the system will go into a repeating multicolored routine with about a two second cycle. This is useful in certain troubleshooting situations but no loop error information will be available.

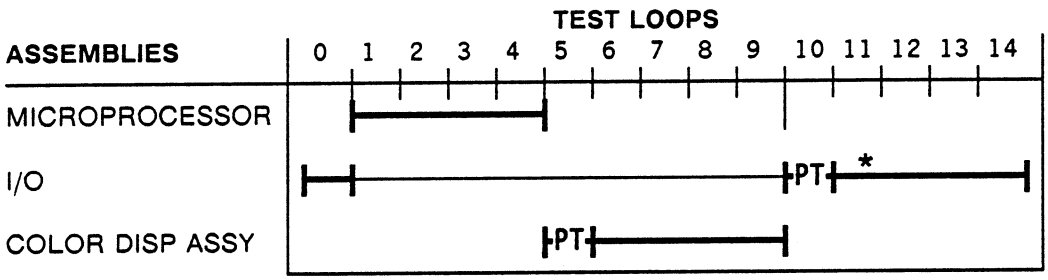
### LOOP 11

Loop 11, which can test every addressable location in the DRAM on the I/O assembly, is a special case. Using RUN FROM LOOP does not completely execute this test because that would take about 18 minutes to complete. Instead, RUN FROM LOOP tests a random block of this memory.

The REPEAT LOOP mode will run the complete Loop 11 test, but only once due to its length. A complete test of DRAM should be done only if the I/O assembly is suspected of failing and there is not enough proof, or if loop 11 has an intermittent failure. This test takes about 18 minutes to run.

*Table 6D-2. Core Subsystem Diagnostic Routines.*

**NOTE:** *For the Core Subsystem tests to be available and meaningful, the power supplies, Color CRT Module, and Color Display assembly must be working, and the Microprocessor, I/O, and one other assembly must be present with partial function.*



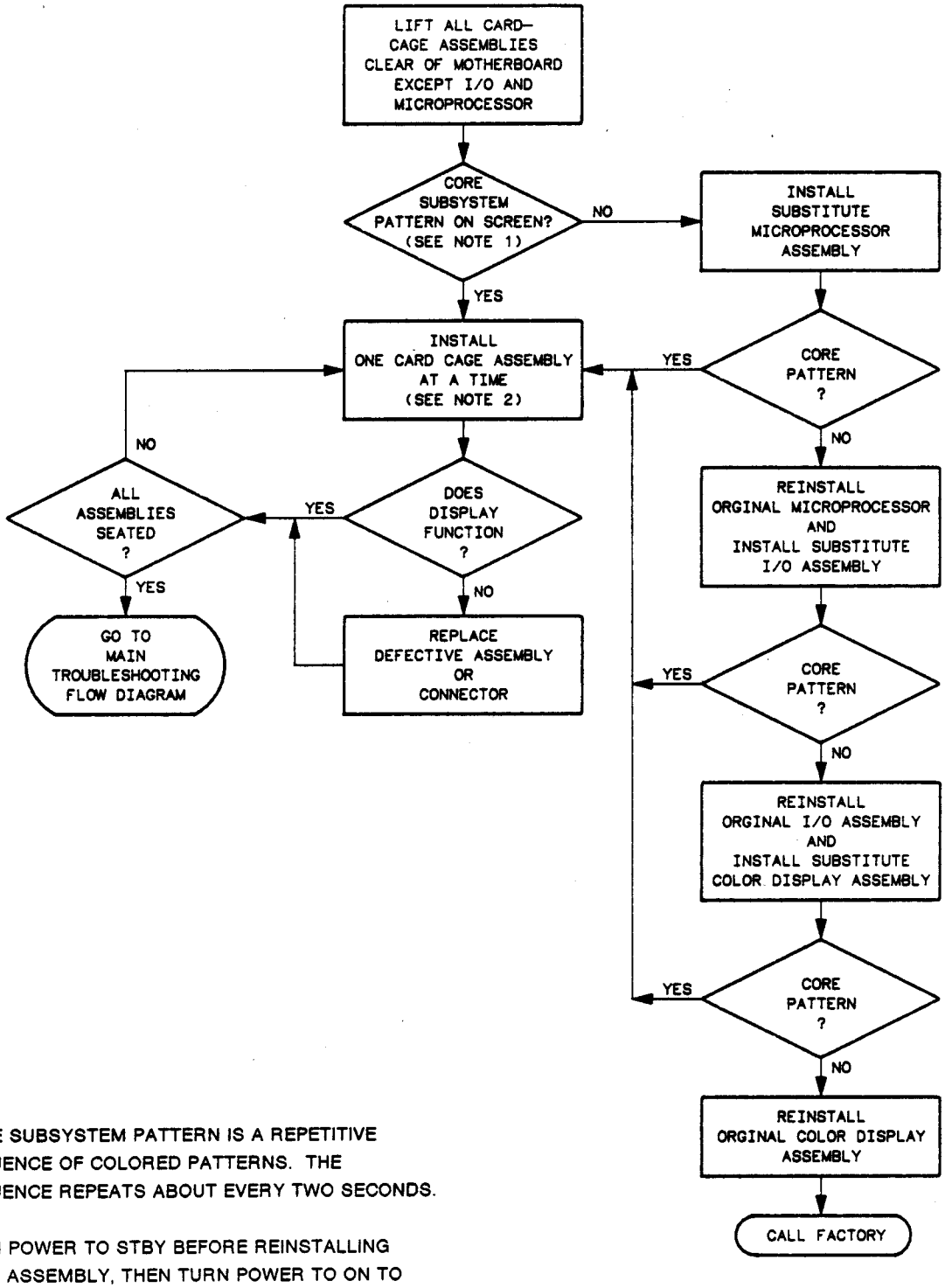

**KEY:**

|PT| Presence test. If the diagnostic firmware fails to find the assembly, this loop fails and all other self tests that include this assembly are skipped.

This assembly must work for the test to be successful. The test will be skipped and will not show a failure if the assembly is not present.

The I/O assembly provides the system clock which must work for any test to be run. It also provides the watchdog timer, which must work or Loop 0 will lock up the instrument.

* See Loop 11 text above.




**NOTES**

1. CORE SUBSYSTEM PATTERN IS A REPETITIVE SEQUENCE OF COLORED PATTERNS. THE SEQUENCE REPEATS ABOUT EVERY TWO SECONDS.

2. TURN POWER TO STBY BEFORE REINSTALLING EACH ASSEMBLY, THEN TURN POWER TO ON TO CHECK DISPLAY.

*Figure 6D-11. Core Subsystem Troubleshooting Flow Diagram*

## 6D-21. DATA ACQUISITION SUBSYSTEM TROUBLESHOOTING PROCEDURE

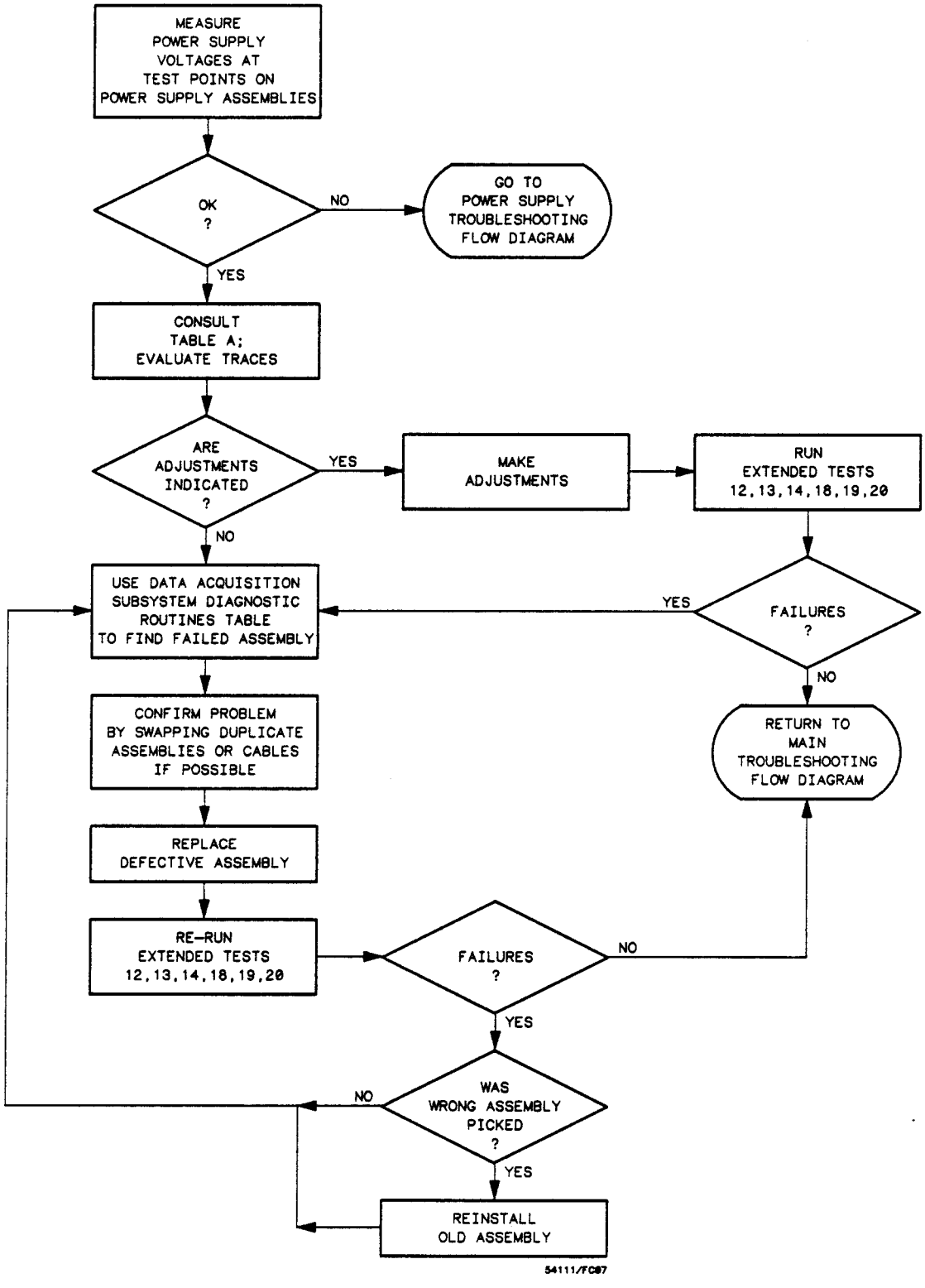



*Figure 6D-12. Data Acquisition Subsystem Troubleshooting Flow Diagram.*

## 6D-22. Data Acquisition Subsystem Diagnostic Routines

The Data Acqusition Diagnostics consists of several groups of tests:

- Timebase Assembly Tests
- ADC Control Assembly Tests
- ADC (Digitizing) Assembly Tests
- Offset Tests

- Factory Test
- Trigger Assembly Tests
- Trigger Qualifier Assembly Tests
- Extended Tests

The tests are arranged in a meaningful order. The more complex and complete tests are located at the end of the group. The firmware executes the tests in numerical order.

Troubleshooting the Data Acquisition Subsystem is based on the Data Acquisition Subsystem Diagnostic Routines table, table 6D-3. The areas tested are shown across the top of the table. Various letters indicate a function of the card in a particular test. If a particular card is not present, its presence test fails, and the tests for that assembly are skipped. Loop numbers are shown at the top and bottom of the table.

Information about instrument loop errors is accessed by pressing ***Utility, Test Menu,*** and ***Display Errors***. The display shows only the numbers of failed loop tests. Once an error appears on the Display Errors screen the error will stay until the power is cycled or until extended test 12 is run, even if the fault has been corrected.

**NOTE**

*It is best to disconnect all front panel inputs from the instrument while using the self-test loops for troubleshooting. Some of the loops can be affected by a signal at a front panel BNC.*

Some loop failures may be caused by misadjustment. use the following table to check for these failures.

TABLE A

| Loop | Adjustments |
|---|---|
| 03 | Self-calibration required: Probe Tip, Vertical, Trigger, and Timebase Cals |
| 26-31 | Channel 1 CLK, GAP |
| 35-40 | Channel 2 CLK, GAP |
| 41/42 | Channel 1 GAIN, FLAT, CLK, GAP |
| 43/44 | Channel 2 GAIN, FLAT, CLK, GAP |
| 78 | Trigger Qual: DELAY/PATT oscillator |

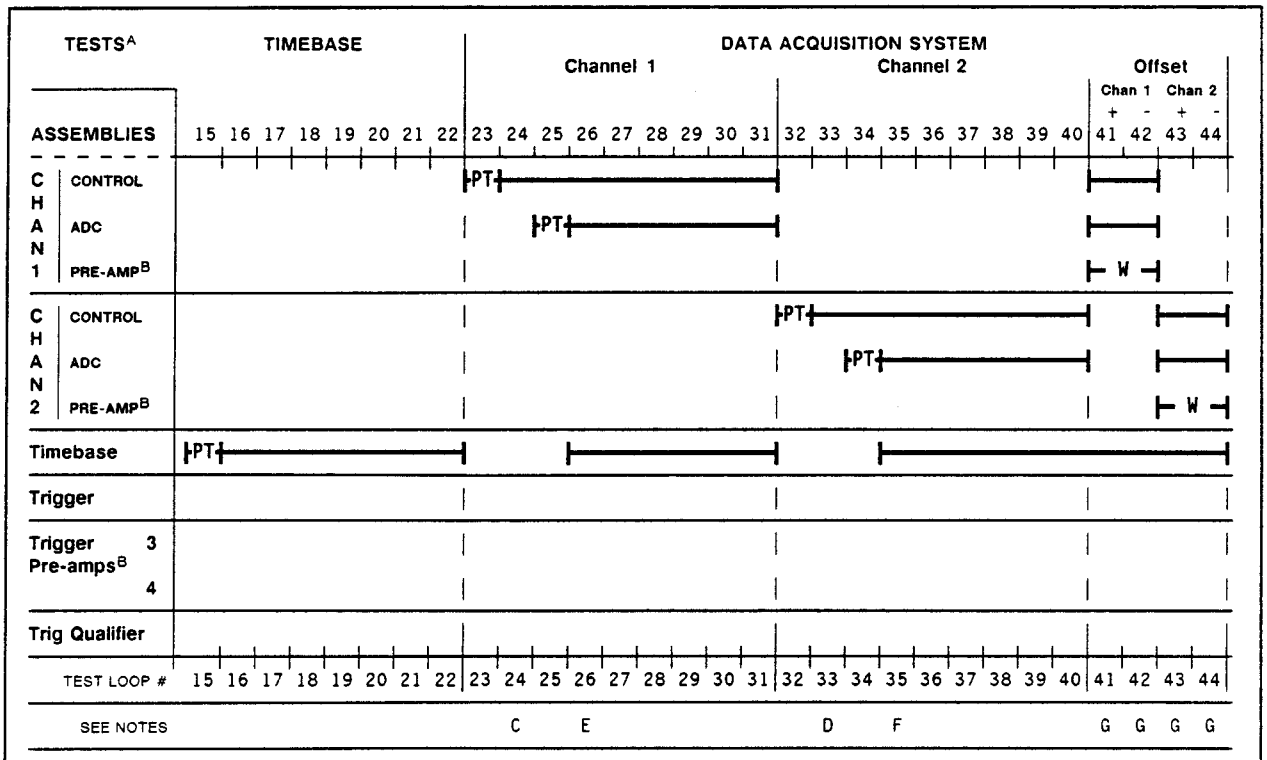
## 6D-23. How To Use The Diagnostic Routines Table

This table relates diagnostic loop test and extended test results to replaceable assemblies. It provides a technique for rapidly and correctly identifying an assembly to replace when loop failures have occurred. Most true hardware failures result from the failure of a single circuit element on a single assembly, though they can cause several loops to fail. The correct use of this table allows the reader to confidently determine the most probable cause of the observed set of loop failures.

After running the powerup self-tests (or extended test 12) and extended tests 13, 14, 18, 19, and 20, you will have a set of test results, consisting of a "pass" or "fail" for each loop. It is important to emphasize that passing a loop test is valuable information, even though only failures are displayed. If a loop is not listed in the "Loop failures" list on the DISPLAY ERRORS screen, it has passed all the times it was run since power-up or Extended Test #12 was run.

Comparing these test results to the information in the table often yields an immediate, clear indication of the most probable cause of failure. For example, when loops 24 through 31 have failed, and all other loops and extended tests have passed, the most probable cause is failure of the channel 1 ADC Control assembly. This can be verified by swapping the channel 1 and channel 2 ADC Control assemblies (carefully recabling). Then you should see loops 33 through 40 fail, and all others pass. In this case, replacement of the defective ADC Control assembly is clearly indicated.

*Table 6D-3. Data Acquisition Subsystem Diagnostic Routines*




**KEY:**

- ⊢PT⊣ Presence test. If the diagnostic firmware fails to find the assembly, this loop fails and all other self tests that include this assembly are skipped.
- ⊢—⊣ This assembly must work for the test to be successful. The test will be skipped and will not show a failure if the assembly is not present.
- ⊢W⊣ This assembly must work for the test to be successful. However, in this test there is no presence test for this assembly; the diagnostics assume that it is there. If the assembly is not present, then the loop will fail just as if the assembly functions failed.
- ⊢O⊣ Only one of the input pre-amplifiers will be used for the input signal during this test. Starting from the top of the table, the test selects the first pre-amp that has passed all previous tests and uses it for the test. The pre-amp that is used can be determined from the status of the particular loop.

**NOTES:**

A. The Microprocessor, I/O, and Color Display assemblies must work for these tests to be valid.

B. The Pre-amp is part of the Attenuator assembly.

C. This test must pass for the results of test loops 25-31, 41, and 42 to be valid.

D. This test must pass for the results of test loops 34-40, 43, and 44 to be valid.

E. This test must pass for the results of test loops 27-31, 41, and 42 to be valid.

F. This test must pass for the results of test loops 36-40, 43, and 44 to be valid.

G. The ADC assembly (A4 and A6) adjustments, GAIN, CLK, and GAP must be adjusted fairly well for these test loops to consistently pass.

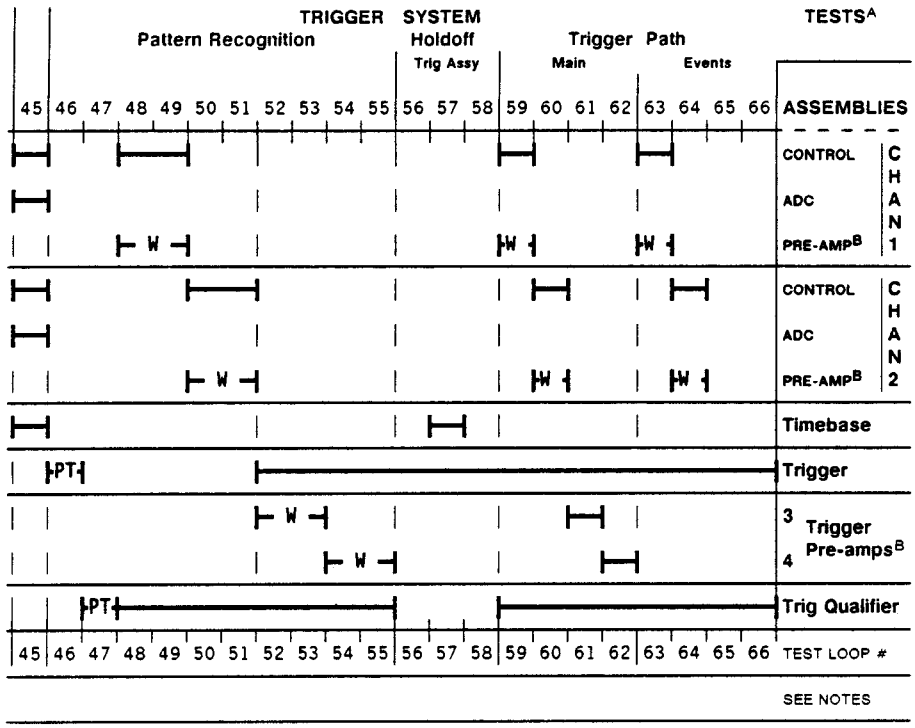
H. This test loop usually fails due to incorrect adjustment of the Delay/Pattern Time oscillator on the Trigger Qualifier assembly. Adjust the oscillator and repeat the test.

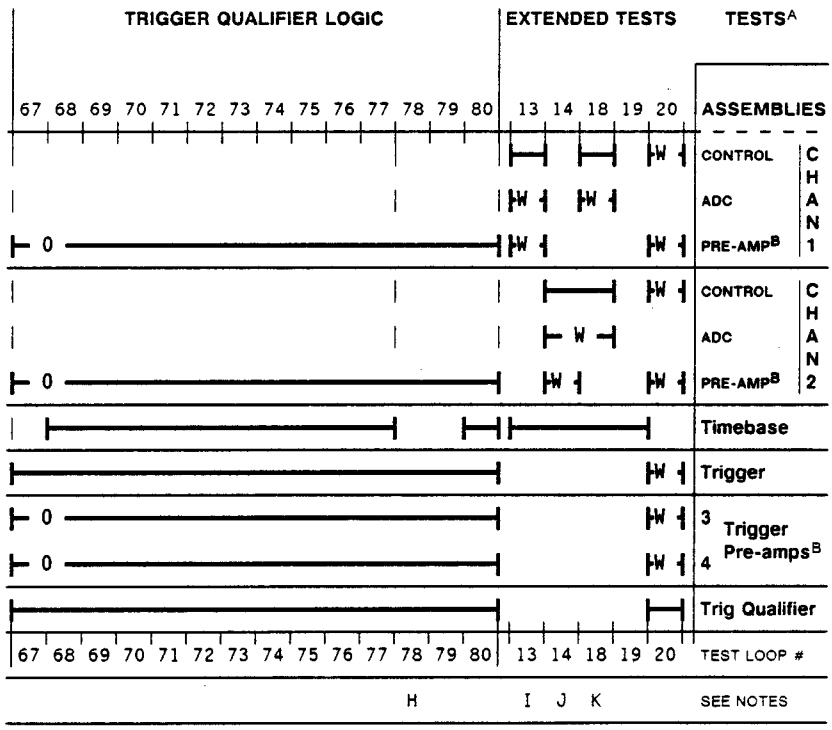
I. For the results of this test to be valid, loop 26 must pass.

J. For the results of this test to be valid, loop 35 must pass.

K. For the results of this test to be valid, loops 26 and 35 must pass.

*Table 6D-4. Data Acquisition Subsystem Diagnostic Routines (con't.)*



In some cases, several assemblies appear to be suspect from looking at the list of loop failures. In such cases, noting which loops have successfully completed before the first failure often allows you to conclude that at least part of one of the suspect assemblies is working. For example, when loops 41 and 42 fail, the Timebase, ADC, ADC Control and channel attenuator assembles for channel 1 all are suspect. However, if no other loops have failed, the extended test results (particularly 13, 18, and 20) are helpful. In this case, loops 23 through 31 testing channel 1 ADC and ADC Control assemblies have successfully completed before loops 41 and 42 ran. This means that two assemblies that might be suspect are in some sense working. Thus, it is best at this point to focus attention on the channel attenuator assembly, perhaps swapping with channel 2 to see whether loops 43 and 44 then fail.

In any case, if unexpected failures, or no changes result from swapping two assemblies, the cause is probably elsewhere. Factory experience has shown that careful rechecking of the interconnections of the swapped assemblies, or restoring the orginal setup and swapping related assemblies (the ADC assemblies in the example immediately preceeding), are the most effective courses in this situation.

Sometimes the loop failures will not make any sense at all. Try The Core System Plus One (following) to isolate individual assemblies into a "suspect bad" or "known good" status.

If the failure still cannot be isolated, more information is available from the status fields for each loop, and can be analyzed by the factory. If you can not resolve your loop test results, we encourage you to call your nearest HP Service Center. They will help you or obtain information from the factory to resolve the problem.

## 6D-24. The Core System Plus One

Occasionally, the indications from the loop errors, the extended tests and the display can be so confusing that it is difficult to determine where to start the trouble shooting process. When this happens, it's sometimes best to start with the Core System which means that all assemblies are pulled up except the I/O assembly, microprocessor assembly and one other assembly, usually the Timebase.

**CAUTION**

*Always turn power OFF when seating an assembly, and be sure to use proper ESD precautions.*

Once you get this system working with no loop errors associated with the Timebase assembly, then one more assembly or a pair of assemblies, like an ADC and its control assembly, can be reinserted. Again, check for associated loop errors with these particular assemblies.

Once a small system is successful other assemblies can be put down one at a time. Always rerun extended test 12 to write the current loop failures into display memory.

Another useful technique is to put the core subsystem in place, plus one assembly, and check it. If it functions correctly, then remove that assembly and reinsert another assembly (or a pair of assembies) and check them. Using the diagnostic table you should be able to quickly draw some good conclusions about the status of all the assemblies in the system.

Note that if an assembly is not present, after it fails its presence test none of the remaining tests that include that assembly are run.

## 6D-25. Timebase Tests — Self Test Loops 15 - 22

The system interface circuitry must be functioning properly for most of the rest of the loops (15 -- 80) to be meaningful. The Timebase test uses the 1GHz Oscillator, the Mux/Sync, and the Timebase IC, all of which are on the Timebase assembly. The 100 MHZ originates at the Mux/Sync. Loop 20 tests the 62.5 MHz path, all others test the 100 MHz Mux/Sync path (except 15).

15 Test for Timebase Presence Only
16 Test the Operation of the Pre-Trigger Delay Clock on the Timebase IC
17 Test the Pre-Trigger Delay Time in the Timebase IC
18 Test the Reset of the Coarse and Fine Interpolators
19 Test the Count of the Fine Interpolator at 100 MHZ
20 Test the Count of the Fine Interpolator at 62.5 MHZ
21 Test the Count of the Coarse Interpolator on the Timebase IC at 100 MHZ
22 Test the Count of the Post Delay Counter at 100 MHZ

## 6D-26. ADC Control Assembly Tests — Self Test Loops 23, 24, 32, 33

The ADC Control assembly performs most of interface and control functions for the ADC assembly. The ADC assembly does not have an address in the same sense as the other assemblies; its address is handled through the Contol 1 cable. The ADC assembly SIB slot locations are not shown in the Display Configuration Screen. There are two control assembly tests for each channel. The interface circuitry to the control assembly and status registers that control the pre-amps (in the attenuator assemblies) are checked in these tests. If either 24 or 33 fail the additional failures associated with the appropriate ADC Assembly are meaningless.

23 Test for ADC Control Assembly 1 Presence Only
24 Test ADC Control Assembly 1 Interface
32 Test for ADC Control Assembly 2 Presence Only
33 Test ADC Control Assembly 2 Interface

## 6D-27. ADC (Digitizing) Assembly Test — Self Test Loops 25 - 31, 34 - 40

Two identical sets of loops tests both ADC assemblies. Loops 25 - 31 are associated with Channel 1 and loops 35 - 40 are associated with Channel 2. The first test is for presence. The second loop (26, 33) resets the ADC assembly and reads and checks the FISO (Fast In Slow Out memory) phases. These two tests (26, 33) must pass before the remaining ADC tests are meaningful. If both channels have identical failures, then the timebase may be at fault (SEE Diagnostic Table). While it is not imperative that the CLK, GAP and GAIN adjustments are perfect it is a good idea to check them when these loop failures are encountered. The cables can also cause these loops to fail. The remaining loops test the ADC assembly at ever increasing frequency. The higher the frequency, the more critical the clock and gap adjustments become.

| Chan 1 | Chan 2 | Test |
|---|---|---|
| 25 | 34 | Presence only |
| 26* | 35* | FISO low speed reset and read ** |
| 27 | 36 | ADC at 10 MHZ |
| 28 | 37 | ADC at 100 MHZ |
| 29 | 38 | ADC at 250 MHZ |
| 30 | 39 | ADC at 500 MHZ |
| 31 | 40 | ADC at 1 GHZ |

* Must pass before the remaining loops in this section and Extended Tests 13, 14, and 18 are valid.

** For Firmware Codes after Apr 22 1987 also tests dither bit fan-out.

## 6D-28. Offset Tests — Self Test Loops 41 - 44

This is a more complete test of the data acquisition subsystem. The firmware starts this test with an ADC Reference Cal. Then a DAC on the ADC Control assembly outputs a signal to the pre-amp (in the Attenuator assembly). The ADC assembly digitizes the signal which is compared to the "right answer". The tests consist of a negative and positive signal for each vertical channel.

For firmware date Apr 22 1987 this test can catch stuck FISO Fan-out, ADC or gray-code converter bits. The test does not test the entire FISO memory; this is done using Extended Test 18. For firmware dates after Apr 22 1987 the FISO fan-out test is moved to Extended tests 13 and 14 for data bits and loops 26 and 35 for dither bits.

41 Test Channel 1 with Positive Offset
42 Test Channel 1 with Negative Offset
43 Test Channel 2 with Positive Offset
44 Test Channel 2 with Negative Offset

**NOTE:** The CLK, GAP, and GAIN must be adjusted properly for these loops to pass. Passing the test does not guarantee that the adjustments are optimal.

## 6D-29. Factory Test — Self Test Loop 45

45 This test is useful only at the Factory

## 6D-30. Trigger Tests — Self Test Loops 46 - 66

Each of the four triggers in the HP 54111D has four paths to follow. Three of these paths are associated with the TCLK (TCLOCK_) path: State, Pattern, and Edge.

The fourth path is the trigger complement, LTCLK (LTCLOCK_), brought to the Trigger Qualifier assembly to reduce system noise and for testing. This signal does not go beyond the Trigger Qualifier assembly. The LTCLOCK signals from each trigger source are wire-anded together. A malfunction (or miscabling) of one may, depending on failure mode, generate a self test loop error on all of the LTCLOCK test paths and control circuitry on the Trigger assembly.

The holdoff tests are rather unique in that only the core subsystem and the Trigger assembly are involved (56, 58). This loop tests the system's ability to transmit a signal from the pre-amp (in Attenuator assembly) through the Trigger Qualifier assembly over to the Trigger assembly (via the TCLK cable). If any of the loop tests labeled TCLOCK1 pass, then the signal is arriving at the Trigger Qualifier input and any other loop failure involving that path is a problem other than the pre-amp and cable.

Failure of loops 63-66 only indicates that the Trigger Qualifier assembly is defective.

**TRIGGER TESTS**

46 Test for Trigger Assembly Presence
47 Test for Trigger Qualifier Assembly Presence
48 Test Channel 1 Trigger through State Mode
49 Test Channel 1 Trigger through LTCLK Status
50 Test Channel 2 Trigger through State Mode
51 Test Channel 2 Trigger through LTCLK Status
52 Test Trigger 3 Trigger through State Mode
53 Test Trigger 3 Trigger through LTCLK Status
54 Test Trigger 4 Trigger through State Mode
55 Test Trigger 4 Trigger through LTCLK Status

**ATRIG CABLE TEST**

57 Test the interface between the Time base and the Trigger assembly (ATRIG)

**HOLDOFF TESTS**

56 Test the events hold off counter on the Trigger assembly
58 Test the hold off by time counter on the Trigger assembly

**MAIN TRIGGER PATH TESTS**

| | | |
|---|---|---|
| 59 | Test the main trigger path from Channel 1 to the Trigger flip-flop on the Trigger Assembly. | TCLOCK1 Path |
| 60 | Test the Main trigger path from Channel 2 to the Trigger flip-flop | TCLOCK2 Path |
| 61 | Test the main trigger path from Trigger 3 to the Trigger flip-flop | TCLOCK3 Path |
| 62 | Test the main trigger path from Trigger 4 to the Trigger flip-flop | TCLOCK4 Path |

**EVENTS DELAY TESTS**

| | | |
|---|---|---|
| 63 | Test Channel 1 events delay path | TCLOCK1 Path |
| 64 | Test Channel 2 events delay path | TCLOCK2 Path |
| 65 | Test Trigger 3 events delay path | TCLOCK3 Path |
| 66 | Test Trigger 4 events delay path | TCLOCK4 Path |

## 6D-31. Trigger Qualifier Tests — Self-Test Loops 67 - 80

This series of loops tests various modes on the Trigger Qualifier assembly. The diagnostics select the first attenuator assembly that passes it's tests, as a signal source for these tests. The selected source must have passed its three previous tests for the true side of the trigger (TCLK). In the unlikely event that all 4 sources failed the previous tests, this series of tests is not run.

Failure of loop 78 usually indicates that the 100 MHZ Oscillator needs to be adjusted. Loop 78 has the tightests specification, but test failures of 79 and 80 could also indicate a similar adjustment problem.

67 Test State Not Present (State Present Tested Previously)
68 Test Zero-Hold Time of State Present/Not Present
69 Test Delayed by Events = 0
70 Test Delayed by Events = 1
71 Test Delayed by Events = 2
72 Test Delayed by Events = 3
73 Test Delayed by Events = 4
74 Test Delayed by Events = 5
75 Test Delayed by Events = 36
76 Test Delayed by Events = 37
77 Test Delayed by Events = 69
78 Test Delayed by Time = 500 us. Failure is usually due to adjustment problem
79 Test Pattern Present > 100 us (Same as 63 -66)
80 Test Pattern Present < 200 us

## 6D-32. Extended Tests

Not all Extended Tests are of use to field service personnel. Also, only a few tests are part of the diagnostic table.

The extended tests must be individually executed by the service person. The Extended Tests are part of the Test Menu. To select a test, press ***Extended Test***, ENTER the test number, and press ***Start Test***. The results of the test appear in a few seconds. To exit the test, press ***Stop Test***. Errors or problems appear in red on the screen after the test.

**TESTS 0-9.** These tests check the interface between the microprocessor and other assemblies and are for factory use.

**TEST 10.** Test 10 is not really a test but the control of a special function of the warm-up cycle. If certain loop failures occur at initial power up, and continue during the next 15 minutes, a warmup message will be displayed. Every five minutes the instrument will initiate the powerup self test routine (see Instrument Warm-up).

Extended Test 10 can turn the warm-up function on or off. Pressing ***Start Test*** for Extended Test 10 will toggle the function to ***OFF*** or ***ON***, depending on the previous state. Press ***Stop Test*** to return to the test menu.

The default setting is ON. When the warmup function is OFF, failure of the warmup dependent loops will result in the message "Powerup Self Test Failed !", rather than "Instrument Warm-up in Progress mm:ss".

**TEST 11.** Extended Test 11 is used to verify that all front panel keys and RPG are working. When the test is entered and initiated a keyboard mockup is displayed on the CRT. The mockup consists of boxes corresponding to each key on the front panel. A box lights when it's key is pressed. The RPG mockup consists of a set of radial lines representing a circle. When the RPG is rotated, an O cursor rotates around the circle.

To exit this test at any time the third key from the top, along the right edge of the display, must be pressed twice.

**TEST 12.** Test 12 resets the system and initiates the powerup self test. The test ends with the instrument in the acquisition menus. If the advisory message "Powerup Self Test Failed" should appear on the display, the failing loops may be found by pressing ***Utility***, ***Test Menu***, then ***Display Errors*** keys.

**TESTS 13, 14.** These tests (13 and 14 for Channels 1 and 2 respectively) check for stuck bits in the acquisition circuitry. The offset DAC is incremented slowly and the output of the ADC is checked for proper progression of codes. The acquisition circuitry must be working and fairly closely calibrated to obtain valid results from these tests.

For firmware codes later than April 22, 1987, additional data is collected during the test that checks fan-out in the FISO IC. Fan-out is slowing the speed and widening the format of data before storage. Failure of the fan-out test indicates a problem with a FISO or another problem in the data path.

**TEST 15.** This test is for factory use. It slews all of the DAC outputs so that they can be checked for smooth outputs. Checking DAC outputs is only usefull for component level troubleshooting which is not supported in this document.

**TEST 16.** Test 16 repeats loops 6-9 continually. It is similar to the test that runs when all of the acquisition assemblies are removed. This is an alternative to removing the assemblies; however it is usually better to remove the assemblies while troubleshooting the core subsystem because the CPU interface to the data acquisition subsystem is eliminated.

**TEST 17.** This test is for factory use only.

**TEST 18.** The FISO Test (18) checks the core memory of each FISO. A few errors in a FISO indicates a FISO problem. However, if a whole FISO fails or all FISO bits on one channel, another cause should be suspected; for example, a defective FFCLOCK signal or ADC assembly. The only part of the digitizing hybrid used is the clock signal. Loop 26 must pass for the FISO test information to be valid on Channel 1 and loop 35 for Channel 2.

**TEST 19.** Test 19 evaluates only the Timebase assembly.

**TEST 20.** Test 20 uses the pattern recognition path on the Trigger Qualifier assembly to determine which trigger source (channels or triggers) is connected to which trigger clock input and with what polarity (differential signals).

This test also checks the FET at the input of the Attenuator assembly preamp. It uses the offset path (channels) or trigger level path (triggers) and checks for a change at the trigger out of the Attenuator assembly. If a problem exists in the signal path in front of the FET, (the passive attenuators) test 20 will not show a defect.

## Changes

The following two tests are included in instruments with a firmware code date after April 22, 1987.

**TEST 21.** Test 21 is for factory use.

**TEST 22.** Test 22 is not really a test but the control of the powerup self test function. When power is applied the instrument automatically runs all the self tests. This takes time and may not be necessary if the instrument was off for only a short time and is known to be functioning properly.

Extended Test 22 will disable or enable the powerup self tests. The default setting is ENABLED. Pressing ***Start Test*** for Extended Test 22 will toggle the function to ***ENABLED*** or ***DISABLED***, depending on the previous state. Press ***Stop Test*** to return to the test menu.

When the self tests are disabled, the message in the display after powerup self tests are attempted is "Powerup Self Test Disabled!", rather than "Powerup Self Tests Passed!" or Failed.

It should be noted that disabling the tests will also prevent catching warmup failures (see Instrument Warmup).

unless other loops have begun to fail. Check for other loop failures and if any are found, refer to the Data Acquisition System Troubleshooting Procedures. If none are found, perform a Probe Tip Cal. If this fails to solve the problem, contact HP Customer Support.

**TRIGGER ATTENUATOR TEST**

Using the front panel CAL signal and HP 10033A probes, trigger the instrument from triggers 3 and 4. Use a vertical channel for the display. Ensure that positive and negative trigger slopes both work on high sensitivity. It may be necessary to adjust the trigger level to about 400 mV to get the instrument to trigger.

If the instrument will not trigger on triggers 3 or 4, the most probable cause is miscabling of the trigger assembly. Check cabling after referring to cabling diagram. Check for unconnected or misconnect solenoid control cables.

**CLICK TESTS**

This tests the operation of the solenoid operated switches in the passive dividers of the attenuator assembly.

1. Check to see that the 50Ω/1MΩ switches work. Remove probes from front panel, and switch between 50 and 1M ohm at each channel or trigger menu. A click should come from the attenuator assembly as impedance is switched.

2. If there is no click, check the attenuator cabling for loose, miscabled, or detached connectors, and for debris such as loose screws or other conductive material on top of the attenuators.

3. Check the operation of the vertical sensitivity solenoids on the channel attenuators by varying the vertical sensitivity on each channel, as follows:

   Be sure the probes are disconnected and attenuation factors are 1:1. With a single display, and when using the increment/decrement (arrow) keys, clicks will occur on the channel attenuator assemblies when switching between vertical sensitivities of 20 and 50 mV/div and between 200 and 500 mV/div.

   Normally a click is heard when switching both ways through these transitions. Different circuitry is used when switching up than when switching down. However, if one switching direction is faulty the solenoid will stay in the first direction it switches to and no clicks will be heard at that range transition. If any clicks are not present, check cabling and look for debris in the solenoids.

4. Check the sensitivity solenoids on the trigger attenuators by changing between LO SENS and HI SENS in the trigger menu. Select the appropriate channel as the trigger source and use the arrow keys. Clicks should be heard when sensitivity is changed. Failure modes would be the same as those for channel attenuators.

It is usually not be necessary to remove attenuators while determining if the attenuator, cable, or control is causing a failed click test. Use swapping techniques to isolate the fault. Swap one end of the solenoid cables (connected at the top of the Acquisition assembly) and try to control the suspect attenuator with a different channel menu; or swap the entire cable.

## 6D-36. Attenuator Outrigging

It is possible to quickly check the effect of replacing a channel or trigger attenuator by outrigging a substitute. The following procedure shows how this is done. The required cables are in the 54100 Family Support Kit.

**NOTE**

*If necessary, use the cabling diagram on the top cover of the instrument or the end of section 6A to recable the instrument during or after this procedure.*

1. Turn off power and remove top cover.
2. Remove Power Cable from suspect assembly at the attenuator and card cage assembly.
3. Connect two or three (depending on attenuator) Coaxial Cables to the good attenuator assembly.
4. Disconnect the Solenoid Cable at the suspect attenuator.
5. Connect the Solenoid Control Cable to the good attenuator.
6. Extend the Attenuator Power Cable using the extender cable from the support kit.
7. Connect the extended power cable to the proper card cage assembly.
8. Connect the signal and trigger coaxial cables to the proper locations
9. Verify proper operation.

## 6D-37. HINTS, TRICKS, AND ARCANA

## 6D-38. Multiplicity of Function

Many parts of the HP 54111D are duplicated. This allows part swapping to troubleshoot for a defective assembly. There are two ADC assemblies, two ADC Control assemblies, and two channel and two trigger attenuator assemblies. Multiple inputs and outputs on these assemblies allow part swapping or recabling to be effective troubleshooting tools.

### CLOCK SIGNALS

Two pairs of clock signals (FFCLKs) originate at the Timebase assembly. If the timebase assembly is suspected as a probable cause for a defect and only one channel is affected, it is easy to switch pairs of timebase outputs to the ADC assembly and see whether the symptoms change. If the problem follows the change, then you have correctly identified the Timebase assembly as defective.

The converse is also true, if the problem stays at the same channel, then you have identified the potential problem in either channel. Naturally, it is a good idea to check the CLK, GAIN, and GAP adjustments with any ADC assembly problem.

### CONNECTORS AND CABLES

The many identical cables on the HP 54111D can be interchanged to test suspected defective cables.

### TRIGGERS

Two signals per channel are used as trigger signals to the Trigger Qualifier assembly. Channel pairs can be interchanged isolate a potential Trigger Qualifier problem or a potential triggering problem in an Attenuator assembly.

For example, suppose you suspect a problem with the channel 1 trigger on the Trigger Qualifier assembly. If Extended Test 20 passed, the channel attenuators must work. If Extended Test 20 failed because of no TCLK #1, swap the trigger pair coaxes for the channel attenuators and run the test again. If the test still fails TCLK #1 the problem is the Trigger Qualifier. If TCLK #1 passes but TCLK #2 fails, the problem is in the channel 1 Attenuator assembly or its control. Swap

entire Attenuator assemblies (by recabling) to finalize the fault location.

The TCLK signals can also be checked with an oscilloscope, comparing the suspect attenuator assembly to a known good one.

#### DIGITIZING SUBSYSTEM

The digitizing subsystem is composed of the ADC assembly and the ADC Control assembly. At times it is difficult to tell which of the two assemblies is defective. Swapping is a quick and easy way of separating cause.

#### TRIGGER ATTENUATORS

It is relatively simple to verify a defective trigger attenuator by simply interchanging the cabling, all of it, going to the trigger attenuators. This cabling interchange consists of the trigger solenoid cable, the input sense cables, the TCLOCK and the LTCLOCK cables, as well as the attenuator power cables. The result of this cable interchange will be that the system thinks that Trigger 4 is really Trigger 3. Keeping this in mind and viewing the screen for the symptoms, it's easy to track where the defect moves. The channel attenuators can be interchanged similarly, but the VIN cable location on the ADC assembly makes the process slightly more complicated.

## 6D-39. System Interface Bus

All the slots in the motherboard are identical except for the slot ID and have identical voltages or signals associated with each pin. This means that defective motherboard slots can be found by rearranging the assemblies in the card cage. The assemblies have been arranged in the order that gives the lowest system noise, but any of the assemblies can work in any of the slots.

Rearranging the assemblies is of course limited by the cabling, which may not accomodate some arrangements.

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