HEWLETT PACKARD

SERVICE MANUAL

HP 54121A

Four Channel Test Set

SERIAL NUMBERS

This manual applies directly to instruments
prefixed with serial number:

2926A

With changes described within, this manual also
applies to instruments with serial prefixes:

2714A
2802A
2845A

For Additional Information about serial numbers see
INSTRUMENTS COVERED BY THIS MANUAL
in Section 1.

Manual Part No. 54121-90905
Microfiche Part No. 54121-90805

Printed in U.S.A.: July 1989

Herstellerbescheinigung

Hiermit wird bescheinigt, dass das Gerät/System HP 54121A in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist.

Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes/Systems angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Zusatzinformation für Mess- und Testgeräte

Werden Mess- und Testgeräte mit ungeschirmten Kabeln und/oder in offenen Messaufbauten verwendet, so ist vom Betreiber sicherzustellen, dass die Funkentstörbestimmungen unter Betriebsbedingungen an seiner Grundstücksgrenze eingehalten werden.

Manufacturer's declaration

This is to certify that this product HP 54121A meets the radio frequency interference requirements of directive 1046/84. The German Bundespost has been notified that this equipment was put into circulation and was granted the right to check the product type for compliance with these requirements.

Additional Information for Test and Measurement Equipment

Note: If test and measurement equipment is operated with unshielded cables and/or used for measurements on open set-ups, the user must insure that under these operating conditions, the radio frequency interference limits are met at the border of his premises.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CWA388

Safety Considerations

General Operation

This is a Safety Class I instrument (provided with terminal for protective earthing). BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

General Warnings and Cautions

- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

Safety Symbols

Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.

Indicates Hazardous Voltages

Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

Warning 

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

Caution 

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software and/or firmware code may be printed before the date; this indicates the version level of the software and/or firmware of this product at the time of the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Edition 1 July 1989 54121-90905

List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in Printing History and on the title page.

Pages	Effective Date
all	July 1989

Contents

Section4

Adjustments

Section5

Replaceable Parts

Section 6A

Disassembly

Section 6B

Section 6C

List of Illustrations

List of Tables

Table Of Contents

General Information

General Information 1

Introduction

This service manual contains information necessary to test, adjust and service the Hewlett-Packard 54121A Four Channel Test Set.

This manual is divided into 8 sections as follows:

- 1 - General Information
- 2 - Installation
- 3 - Performance Tests
- 4 - Adjustments
- 5 - Replaceable Parts
- 6A - Disassembly
- 6B - Theory
- 6C - Troubleshooting

Information on operating and interfacing the HP 54121A is contained in the *Front-Panel Reference* supplied with the HP 54120B Digitizing Oscilloscope Mainframe.

The "General Information" Section includes a description of the HP 54121A, its specifications, operating characteristics, general characteristics, safety considerations, instruments covered by this manual, options, accessories supplied, and recommended test equipment.

Also listed on the title page of this manual is a microfiche part number. This number can be used to order 4 x 6 inch microfilm transparencies of this manual. Each microfiche contains up to 96 photo-duplicates of manual pages. The microfiche package also includes the latest Manual Changes supplement as well as pertinent Service Notes.

Description

The HP 54121A is a 20 GHz Four Channel Test Set. The HP 54121A contains four input channels, a trigger input, and a TDR step generator. The HP 54121A is designed to operate with the HP 54120B (previously HP 54120A) Digitizing Oscilloscope Mainframe.

Safety Considerations

The appropriate sections contain safety information relevant to the service procedure it describes. Both the HP 54121A and this manual should be reviewed for safety markings and instructions before work is begun. Refer to the pages following the title page. They include a safety summary and safety considerations.

Instruments Covered By This Manual.

The HP 54121A's serial number is on the rear panel. Hewlett-Packard uses a two-part serial number consisting of a four-digit prefix and a five-digit suffix separated by a letter (0000A00000). The prefix is the same for all identical oscilloscopes and changes only when a modification is made that affects parts compatibility. The suffix differs for each oscilloscope. This manual applies directly to instruments with the serial prefix shown on the title page.

Options

The following options are available for the HP 54121A.

- Option 090 - Delete RF Accessory Kit
- Option 908 -Rack mount kit
- Option 910 -Additional copies of operating manuals

Accessories Supplied

The following accessories are supplied with the HP 54121A.

- This Service manual
- RF Accessory kit HP part number 54121-68701
- Connectors savers HP part number 5061-5311 - Quantity 5
- Coaxial shorts HP part number 0960-0055 - Quantity 5

List of RF Accerssory kit devices	Qty	HP Part Number
APC 3.5 (f-m) 20 dB attenuators	5	33340C/020
50 Ω load SMA (f)	1	250-2151
Coaxial Short SMA (f)	1	1250-2152
50 Ω load SMA (m)	1	1250-2153
SMA (m) to BNC (f) adapters	2	1250-1200
SMA (m-m) 36 inch coaxial cables	3	8120-4948

Accessories Available

The following accessories are available for the HP 54121A

- Accessory kit HP 54007A
- 6 GHz Probe kit HP 54006A
- 22 ns Delay Line HP 54008A
- 0.5 to 18 GHz Trigger HP 54118A

Systemizing

At the factory the HP 54120B Digitizing Oscilloscope Mainframe and the HP 54121A Four Channel Test Set are calibrated together as a system called the HP 54121T. This system will meet all published specifications when shipped from the factory. If the system is split up, (a different HP 54121A Four Channel Test Set is used with the HP 54120B Mainframe), the system will meet all specifications except for the dc accuracy specifications for single voltage and dual voltage markers. The single voltage marker specification will change from ±0.4% of full scale ±2 mV to ±1.0% of full scale ±2 mV. The dual voltage marker specification will change from ±0.8% of full scale to ±2% of full scale. To obtain the original factory specifications, perform the sampler bias and offset adjustments in section 4, (Adjustments) of this manual.

Specifications

The following specifications for the HP 54121A are the performance standards against which the instrument is tested.

Channels (Vertical)[1]

20 GHz Bandwidth[2]

−3 dB dc to 20 GHz channels 2-4 (channel 1 is -3.5 dB at 20 GHz)
dc to 18 GHz channel 1

12.4 GHz Bandwidth

−3 dB dc to 12.4 GHz channels 1-4

20 GHz Transition Time (10% to 90% calculated from, $T_r = 0.35/BW$)

≤ 17.5 ps channels 2-4
≤ 19.4 ps channel 1

12.4 GHz Transition Time (10% to 90% calculated from, $T_r = 0.35/BW$)

≤ 28.2 ps channels 1-4

20 GHz Maximum Noise ≤ 2 mV RMS

12.4 GHz Maximum Noise ≤ 1 mV RMS

Scale Factor (full scale is 8 divisions)

Minimum 1 mV/div
Maximum 80 mV/div

dc Accuracy single voltage marker[3]

Average mode ±0.4% of full-scale or marker reading (whichever is greater) ±2 mV
20 GHz Persistence mode ±0.4% of full-scale or marker reading (whichever is greater) ±2 mv ±3.0% of (reading − channel offset)
12.4 GHz Persistence mode ±0.4% of full-scale or marker reading (whichever is greater) ±2 mv ±1.5% of (reading − channel offset)

dc Difference Voltage Accuracy with two voltage markers on same channel[3]

Average mode ±0.8% of full-scale or Delta V reading (whichever is greater)
20 GHz Persistence mode ±0.8% of full-scale or Delta V reading (whichever is greater) ±3.0% of delta marker reading
12.4 GHz Persistence mode ±0.8% of full-scale or Delta V reading (whichever is greater) ±1.5% of delta marker reading

Programmable dc Offset[4] ±500 mV

Inputs

Number	Four
Dynamic Range	±320 mV relative to channel offset
Maximum Input V	±2 V dc + ac peak (16 dBm)
Impedance	50 Ω (Nominal)
Percent Reflection	±5% for 30 ps risetime
Connectors	3.5 mm (m)

1. When operated within ±5° C (±9° F) of the temperature of the last front-panel calibration.
2. The input samplers are biased differently for increased bandwidth in the 20 GHz bandwidth mode.
3. When driven from a 0 Ω source
4. An effective offset of ±820 mV can be achieved by using the ±500 mV of channel offset and adding ±320 mV of offset with the waveform math offset scaling function.

TDR System

Risetime combined oscilloscope and TDR performance
≤ 45 ps[1] (measured at 12.4 GHz bandwidth in average mode)

Flatness combined oscilloscope and TDR performance
≤ ±1% after 1 ns from edge
≤ +5%, −3% to 1 ns from edge (measured at 12.4 GHz bandwidth in average display mode)

Levels combined oscilloscope and TDR performance

Low	0 V ±2 mV
High	200 mV ±2 mV

1. The risetime of the generator is less than 35 ps, as calculated by
$(T_{r\ system})^2 = (T_{r\ generator})^2 + T_{r\ oscilloscope})^2$

Timebase (Horizontal)

Scale Factor full-scale is 10 divisions

Minimum	10 ps/div
Maximum	1 s/div

Delay time offset relative to trigger

Minimum	16 ns
Maximum	1000 screen diameters or 10 seconds, whichever is smaller

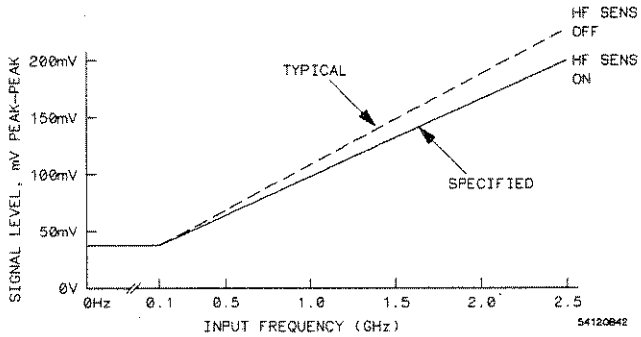
Time Interval Accuracy dual marker measurement ≤ 10 ps ±0.1% of reading

Time Interval Resolution 0.25 ps[1] or 0.02 divisions, whichever is larger

1. At 10 ps/division, data points are plotted at 0.2 ps intervals to match the display pixel resolution.

Trigger External Input Only

Sensitivity
dc to 100 MHz 40 mV peak-to-peak; increasing linearly from 40 mV at 100 MHz to 200 mV peak-to-peak at 2.5 GHz



Graph Illustrating Trigger Sensitivity Specification

Pulse Width 200 ps for pulses >200 mV

Trigger Level Range ±1 V

Jitter trigger and timebase combined (one standard deviation)
<2.5 ps + 5E-5 x delay setting. Tested using 2 GHz synthesized source at 200 mV peak-to-peak with high frequency sensitivity on and high frequency reject off.

Trigger Input

Maximum Input V	±2 V dc + ac peak (16 dBm)
Nominal Impedance	50 Ω
Percent Reflection	≤ 10% for 100 ps risetime
Connector	3.5 mm (m)

Operating Characteristics

The following operating characteristics for the HP 54121A are not specifications, but are typical characteristics included as additional information only.

Channels (Vertical)

Scale Factors: Adjustable from 1 mV/div to 80 mV/div in a 1-2-5-10-20-50-80 sequence from the RPG control or the increment decrement keys. Also adjustable over the range in 1 mV increments from the numeric keypad.

Attenuation Factors: Factors may be entered to scale the oscilloscope for external attenuators connected to the channel inputs.

Noise: Averaging reduces noise by $1/\sqrt{n}$ where n is the number of averages, until a system limitation of approximately 35 μV is reached.

Typical noise is:

Display Mode	**Noise** (RMS)
20 GHz bandwidth, Avg = 1	1.2 mV
20 GHz bandwidth, Avg = 256	80 μV
20 GHz persistence	1 mV
12.4 GHz bandwidth, Avg = 1	500 μV
12.4 GHz bandwidth, Avg = 256	35 μV
12.4 GHz bandwidth, persistence	400 μV

Channel-to-channel Isolation: 60 dB

Timebase (Horizontal)

Delay Between Channels: The difference (up to 100 ns) in delay between channels can be nulled out in 1 ps increments to compensate for differences in input cables or probe length.

Reference Location: The reference point can be located at the left edge or center of the display. The reference point is that point where the time is offset from the trigger by the delay time.

Triggered Mode: Causes the oscilloscope to trigger synchronously to the trigger input signal.

Free Run Mode: Causes the oscilloscope to generate its own triggers at a user specified rate (between 15.3 Hz and 500 kHz). Used with the Channel 1 step generator for TDR and transmission measurements. The channel 1 step may also be used to trigger a device under test for viewing information prior to the trigger.

Trigger

Attenuation Factors: Factors may be entered to scale the oscilloscope for external attenuators connected to the trigger input.

Edge Trigger: Triggers on the positive or negative edge of the trigger source.

HF Reject: Limits trigger bandwidth to approximately 100 MHz.

Display

Data Display Resolution: 501 points horizontally x 256 points vertically.

Data Display Formats

Full screen: All channel displays are superimposed and are eight divisions high.

Split screen: With four graphs, channels are displayed separately and are two divisions high; or with two graphs, channels 1 and 3 are superimposed and channels 2 and 4 are superimposed and are four divisions high.

Display Modes

Persistence: The time that each data point is retained on the display can be varied from 300 ms to 10 seconds, or it can be displayed infinitely.

Averaging: The number of averages can be specified as powers of 2, up to 2048. On each acquisition, 1/n times the new data is added to (n-1) ÷ n of the previous value at each time coordinate. Averaging operates continuously, except over HP-IB where it terminates at the specified number of averages.

Graticules: The user may choose full grid, axes with tic marks, frame with tic marks, or no graticule.

Bandwidth: When in the average or persistence display modes, the user may select between a 20 GHz bandwidth and a 12.4 GHz bandwidth. The 12.4 GHz bandwidth reduces noise. See channel characteristics for bandwidths and noise levels.

Display Colors: Users may choose a default color selection or select their own colors from the front panel or over HP-IB. Different colors are used for display background, channels, functions, background text, highlighted text, advisories, markers, overlapping waveforms, and memories.

Programmability

Instrument settings and operating modes, including automatic measurements, may be remotely programmed by HP-IB (IEEE-488). HP-IB programming complies with IEEE 488.2 standards. The HP 54121T system can be programmed to take data only at specified time points, or to return only measurement results, (i.e., tr, tf, frequency, etc.,) to speed up data acquisition.

Data Output Transfer Rate: 115 kbytes/s

Typical Measurement Times: 200-700 ms

Data Record Lengths:

Timebase Setting/Histogram Type	Number of points/record
10 ps/div ≤ time/div 20 ps/div	100, or 400
20 ps/div ≤ time/div 50 ps/div	100, 400, or 800
50 ps/div ≤ time/div 200 ps/div	100, 500, or 1000
200 ps/div ≤ time/div ≤ 1 s/div	128, 256, 500, 512, or 1024
Voltage Histogram	256
Time Histogram	501

Histograms

Time and voltage histograms may be taken with a user-specified number of samples (between 100 and 655,000,000) within a user-specified voltage window (time histogram) or time window (voltage histogram). To accelerate throughput when taking voltage histograms, take samples only in the user-specified time window.

Distribution markers: Two markers, labeled Upper and Lower Distribution Limits, indicate the cumulative occurrences of samples from the edge of the display to a given time (time histogram) or voltage (voltage histogram).

Mean and Standard Deviation: Calculates the mean and standard deviation of a distribution on screen, or between the distribution limits, assuming a Gaussian distribution.

Measurement Aids

Markers: Dual voltage or time markers can be used for a variety of time and voltage measurements. Voltage markers can be assigned to channels, memories, or functions.

Automatic Level Set: Voltage markers may be preset to 10%-90%, 20%-80%, 50%-50%, or to user specified levels.

Automatic Edge Find: The time markers can be assigned automatically to any displayed edge of either polarity on any channel. The voltage markers establish the reference, on the edge, for the time markers in this mode.

Automatic Pulse Parameter Measurements: The HP 54121T system automatically takes ten pulse parameter measurements, (as defined by IEEE standard 194-1977, IEEE Standard Pulse Terms and Definitions). The standard measurement thresholds are 10%, 50%, and 90%. The measurement modes are frequency, period, positive pulse width, negative pulse width, duty cycle, risetime, falltime, preshoot, overshoot, and RMS voltage, peak-to-peak voltage.

Waveform Math: Any two of seven waveform math operations may be assigned to two displayable math functions. The available operations are Plus, Minus, Invert, Versus, Max, Min, and Only. Max and Min, which define an envelope about the waveform, are only available in the persistence mode. The vertical channels, or any of the waveform memories can be used as operands for the waveform math. Function sensitivity and offset may be adjusted independently of the channel display settings.

Waveform Save: Four waveforms may be stored and displayed in four non-volatile waveform memories. Waveform memories are typically used in the average display mode. Screen displays may be stored in two volatile pixel memories. Pixel memories are typically used in the persistence display mode.

TDR System

Normalized information is a characteristic not a specification. The information is presented here for comparision purposes only. Normalization characteristics are achieved only with the use of the normalization calibrations and firmware routine.

Risetime: adjustable, allowable values based on timebase setting.
Minimum - 10 ps or 0.08 x time/div, whichever is greater
Maximum - 5 x time/div

Flatness: $\leq \pm 1\%$

Levels:

Low	0 V $\pm$2 mV
High	200 mV $\pm$2 mV

Networks

Reflection measurements

Source: Measurements are made using the Channel 1 step source or a user-supplied external source.

Calibration: A reference plane is defined by calibrating the reflection channel with a short placed at the point where the device under test will be connected. The short calibration is followed with a 50 Ω calibration. These calibrations are used to derive the normalization filter.

Cursor: Reads out the percent reflection, impedance, time, and distance from the reference plane to the cursor. See note 1.

Percent Reflection: Automatically calculates the maximum and minimum percent reflection of the waveform shown on screen.

Normalization Filter: Applies a firmware digital filter to the measured data and stores the resulting waveform in memory 1. The risetime of the filter may be varied to allow the user to simulate the edge speeds which would be seen by the device under actual operation. Normalization also removes errors caused by discontinuities prior to the reference plane.

Note 1: Percent reflection measurements should be used to quantify reactive peaks and valleys of the TDR display. Impedance measurements are valid only for resistive, horizontal flat line TDR displays. Because the accuracy depends on the measurement being made, percent reflection and impedance accuracies are not specified. Percent reflection and impedance measurements are ratios of voltage measurements whose accuracies are specified.

Percent Reflection (Rho) = $(V_{cursor} - V_{top}) \div (V_{top} - V_{base})$

Impedance (Z) = $50\ \Omega \times (1 + \text{Rho}) \div (1\text{-Rho})$

Vcursor = voltage at the cursor

V_{top} = high level of calibration reflected step and is determined during the reflection calibration.

V_{base} = low level of calibration reflected step and is determined during the reflection calibration.

Distance measurements are subject to the accuracy of the velocity factor or dielectric constant entered by the user. Since the HP 54121T system has no control over the accuracy of these numbers, distance accuracy is not specified. Distance is derived from time interval measurements whose accuracies are specified.

Distance (d) = one half times the quantity (Δt divided by the velocity constant)

Where Δt = time from the reference plane to the cursor.

Dielectric Constant = $(3 \times 10^8 \text{m/s})^2$ (Velocity Constant)^2

Where the user enters either a relative Dielectric Constant or a velocity constant. The TDRs ability to resolve the distance between two discontinuities is limited to 1/2 the system risetime. Without normalization, this is approximately 1/2 of 45 ps or 7 mm in air. For the distance resolution in your media, divide 7 mm by the the square root of the effective dielectric constant of your media. With normalization, the system risetime can be 10 ps yielding 1.5 mm of resolution in air. The maximum length the TDR can measure is subject to media loss. For a lossless vacuum, and with a 15.3 Hz TDR repetition rate, the HP 54121T system can measure 4,900 km. Actual maximum lengths will generally be limited by the losses of the media under test.

Transmission measurements

Source: Measurements are made using the channel 1 step source or a user-supplied external source.

Calibration: A calibration with a straight-through path or through a users standard device determines reference amplitude levels, reference time, and distances of the signal path. These reference levels are used for gain and propagation delay measurements.

Cursor: Reads out time referenced to the calibration edge and gain referenced to the transmission calibration results. (See Note 2.)

Propagation Delay and Gain: Automatically calculates the difference in time and distance between the calibration signal path and the test signal path. Also calculates the ratio of the test signal amplitude to the calibration signal amplitude. (See Note 2.)

Normalization Filter: Applies a firmware digital filter to the measured data and puts the resulting waveform in memory 2. The risetime of the filter may be varied to allow the user to simulate the edge speeds which would be seen by the device under actual operation. See TDR output specifications for allowable risetime values.

Note 2:

Δt = Time of the cursor - Time of reference edge (50%)

Gain = $(V_{top} - V_{base})$ signal ÷ $(V_{top} - V_{base})$ reference

Prop Dly = Time of test edge (50%) - Time of reference edge (50%)

Distance (d) = Prop Dly ÷ Velocity Constant

V_{top} = High level of waveform

V_{base} = Low level of waveform

Setup Aids

Auto-Scale: Pressing the Auto-Scale key automatically adjusts the vertical and horizontal scale factors and the trigger level for a display appropriate to the signals applied to the inputs. Auto-Scale requires a signal with a duty cycle greater than 2%, a frequency greater than 50 Hz, and an input level of 5 mV for low bandwidth mode or 20 mV for high bandwidth mode. Auto-Scale is operative for relatively stable input signals, and the signal applied to the external trigger input must meet the minimum trigger specifications.

Save/Recall: Up to ten front-panel setups may be saved in non-volatile memory.

Preset Reflection Channel: Sets up the instrument for making TDR measurements.

Documentation Aids

Waveforms, scaling information, and measurement results can be transferred directly to HP-GL compatible digital plotters and HP-IB raster graphics printers, including the HP 2225A ThinkJet printer and the HP 3630A printer.

Digitizer

Converter: 12-bit successive approximation A/D converter.

Resolution: The useable full-scale range of the A/D is 640 mV. One LSB of the A/D converter equals 250 μV. This gives one part in 2560, or slightly more than 11 bits of resolution. Averaging can extend the resolution to 32 μV. This increased resolution of around 14 bits can be seen at more sensitive ranges or over the HP-IB.

Digitizing Rate: The signal is sampled and digitized at a rate dictated by the trigger rate, repetition rate, timebase range, display mode, and number of channels turned on. If data acquisition is not limited by trigger rate, the actual sampling and digitizing rate will vary within the following range:

a. Maximum of 10k samples per second at 10 ns/div or faster with one channel on while the HP 54121T system is in infinite persistence display mode.

b. Minimum of 1k samples per second at timebase ranges of 46 μs/div or slower, regardless of number of channels turned on or the display mode.

A typical sample rate is 4500 samples per second.

General Characteristics

The following general characteristics are not specifications, but typical characteristics included as additional information only.

Environmental Conditions

Temperature Operating: +15° C to +35° C (+59° F to +95° F).

Temperature Non-operating: -40° C to +70° C (-40° F to +158° F).

Humidity Operating: Up to 90% relative humidity at +35° C (95° F).

Humidity Non-operating: Up to 95% relative humidity at +65° C (+149° F).

Altitude Operating: Up to 4600 metres (15,000 ft).

Altitude Non-operating: Up to 15,300 metres (50,000 ft).

Vibration Operating: Random vibrations 5-500 Hz, 10 minutes per axis, ~0.3 g (rms).

Vibration Non-operating: Random vibration 5-500 Hz, 10 minutes per axis, =2.41 g (rms); and swept sine resonant search, 5-500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Power Requirements

Power requirements listed are for the combined HP 54121T system. The HP 54121A Four Channel Test Set obtains its power over the provided interface cable from the HP 54120B Digitizing Oscilloscope Mainframe.

Weight

HP 54121A Net: Approximately 3.2 kg (7 lb).

Dimensions

Dimensions are for general information only. If dimensions are required for building a special enclosure, contact your local HP sales office. Dimensions are in millimetres and (inches). Refer to figure 1-1.

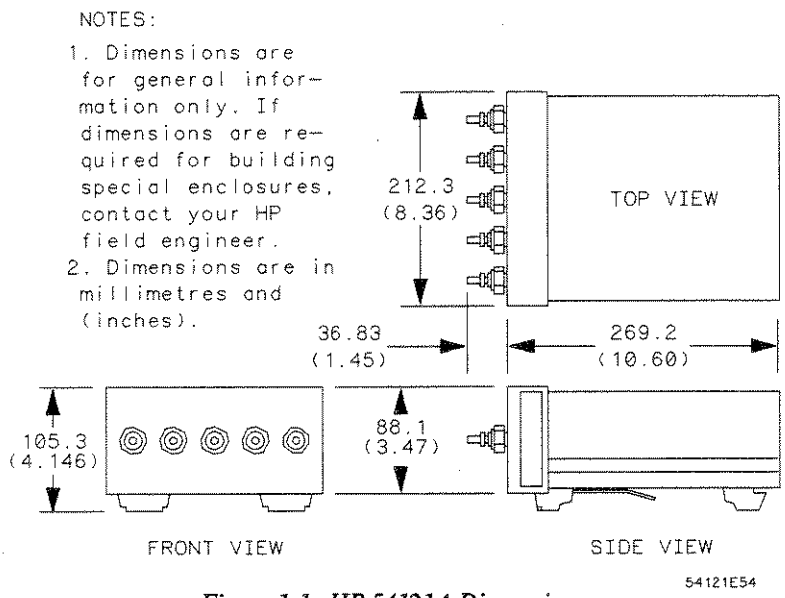


Figure 1-1. HP 54121A Dimensions

Recommended Test Equipment

The test equipment recommended for maintaining the HP 54121A is listed in table 1-1. The three sections requiring test equipment are

- Performance Tests (section 3)
- Adjustments (section 4)
- Troubleshooting (section 6C)

Table 1-1. Recommended Equipment List

Instrument	Critical Specifications	Model	Use*
Synthesized sweeper**	20 GHz, +12 dBm, -6 dBm, Stability 0.25 ppm/yr -25 dBc Harmonics	HP 8341A/B/003	P,A
Power splitter	APC 3.5 connectors	HP 11667B	P,A
DMM	5 1/2 digits	HP 3478A	P,A
Power meter	20 GHz	HP 436A	P
Power sensor	20 GHz	HP 8485A	P
50 Ω load	APC 3.5 (m)	HP 909D	P,A
50 Ω load	APC 3.5 (f)	HP 909D/011	P
Calculator	Log base 10 function	HP 11C	P
6 dB pad	APC 3.5 connections	HP 33340C/006	P
10 dB pad	APC 3.5 connections	HP 33340C/010	P
20 dB pad	APC 3.5 connections	HP 33340C/029	P,A,T
RF amplifier	Gain 20 dB at 10 MHz, flatness ±0.7 dB, noise < 6 dB harmonic distortion -32 dB	HP 8447A	P
Frequency synthesizer	100 kHz to 10 MHz, Frequency stability 0.05 ppm/yr 200 mV output level, sine and square wave outputs dc mode 1/2 V output, 100 μV resolution	HP 3325A/001	P,A,T
Oscilloscope	300 MHz bandwidth, general purpose	HP 54100A	T
Delay line	22 ns, 20 GHz	HP 54008A	A P

* P = Performance Tests A = Adjustments T = Troubleshooting
** For adjustments and systemizing, only 250 MHz, +12 dBm, synthesized sine wave generator is required.

Table 1-1. Recommended Equipment List (continued)

Accessories	Critical Specifications	HP Part Number	Use*
Adapter	BNC (m-m)	1250-0216	A
Adapter	BNC (f) to SMA (m), 2 needed	1250-1200	P,A
Adapter	APC 3.5 (m-m)	1250-1864	P
Adapter	APC 3.5 (f-f) Neither end precise**	1250-1865	A
Adapter	APC 3.5 (f-f) 26.5 GHz, both ends precise	1250-1865	P
Adapter	APC 3.5(m-f) 26.5 GH both ends precise	1250-1866	P,A
Adapter	APC 3.5 (m-f) 26.5 GHz, male end precise, 6 needed	1250-1866	P,A
Adapter	APC 3.5 (m-f) 26.5 GHz, female end precise	1250-1866	A
Adapter	N (m) to APC 3.5 (m)	1250-1743	P
Adapter	N (m) to APC 3.5 (f) 26.5 GHz	1250-1744	P,A
BNC Tee	1 (m) end, 2 (f) ends	1250-0781	P,A,T
Coaxial cable	APC 3.5 (m-f) 26.5 GHz	8120-4942	P,A
Coaxial cable	APC 3.5 (m-m 18 GHz, 3 needed	8120-4948	P,A,T
Coaxial cable	BNC connectors, length 48 inches, 2 needed	10503A	P,A,T
Coaxial short	APC 3.5 (f)	1250-2127	P
Coaxial short	APC 3.5 (m)	1250-2128	P
Adapter	Banana to BNC (f)	1250-2277	P,A
Cable	Semi-rigid U shaped	54121-61601	P,A
Cable	Semi-rigid S shaped	54121-61602	P,A
Cliplead	Alligator to alligator	N/A	A
Screwdriver	Jewelers, 0.01 inches thick, 0.04 inches long	N/A	A
Alignment tool	Non-metallic	8710-1355	A
Torque wrench	5 in/lb	8710-1582	P,A,T
Torque wrench	8 in/lb	8710-1765	P,A,T

* P = Performance Tests A = Adjustments T = Troubleshooting

Table Of Contents

Installation

Installation 2

Introduction

This section contains installation instructions, operating environments, cleaning, storage, and shipment.

Power Requirements

The HP 54121A receives its power from the HP 54120B Mainframe through the umbilical cable.

Four Channel Test Set Connection

Connect the Umbilical Cable to the Interface Cable Ports on the mainframe and four channel test set. See figure 2-1.

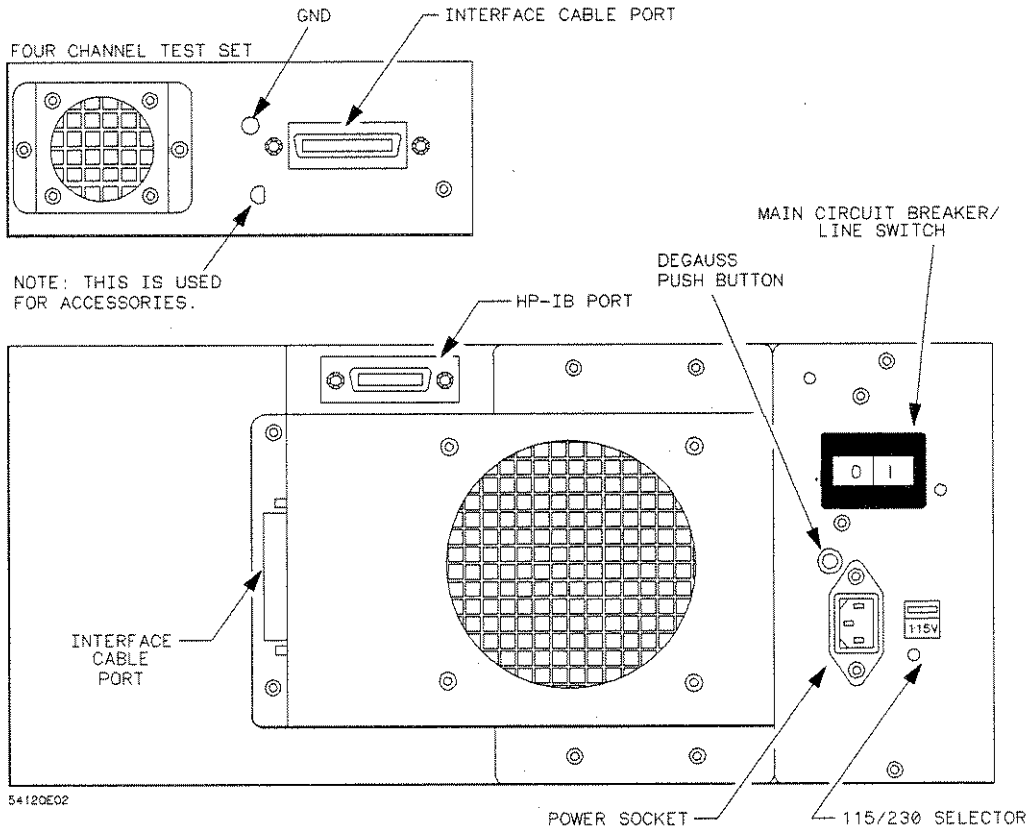


Figure 2-1. Rear Panel of Mainframe and Test Set

Operating Environment

The operating environment is noted in section 1 under general characteristics. Note the non-condensing humidity limitation. Because condensation within the instrument can cause poor operation or malfunction, it should be avoided. The HP 54121A will operate to all specifications with the temperature and humidity range stated in section 1 under general characteristics, except where noted in the specifications.

Cleaning

When cleaning the HP 54121A, CAUTION must be exercised about which cleaning agents are used. USE MILD SOAP AND WATER. If a harsh soap or solvent is used, the water-base paint finish WILL BE DAMAGED.

Storage And Shipment

The instrument may be stored or shipped in environments with the following limits:

Temperature: -40° C to +70° C (-40° F to +158° F)
Humidity: Up to 95% at +65° C (+149° F)
Altitude: Up to 15,300 metres (50,000 feet)

Tagging For Service

The instrument should also be protected from temperature extremes which cause condensation within the instrument. Condensation within the instrument may cause a malfunction.

If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of servicing required, the return address, model number, and full serial number. In any correspondence refer to the instrument by model number and full serial number.

Packaging

Original packaging i.e., containers and material identical to those used in factory packaging are available from Hewlett-Packard. If other packaging is to be used the following general instructions for repackaging with commercially available materials should be followed:

a. Wrap the instrument in heavy paper or plastic. Install SMA shorts on test set's inputs

b. Use a strong shipping container. A double wall carton made of 2.4 MPa (350 psi) test material is adequate.

c. Use a layer of shock absorbing material 75 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside the container. Protect the front panel with cardboard.

d. Seal the shipping container securely.

e. Mark the shipping container FRAGILE to ensure careful handling.

Table Of Contents

Performance Tests

Performance Tests 3

Introduction

The procedures in this section test the instrument's electrical performance using the specifications in Section I as performance standards. All tests can be performed without access to the interior of the instrument.

Recommended Equipment

Equipment recommended for performance tests is listed in table 1-1. Any equipment that satisfies the critical specifications stated in table 1-1 may be substituted.

Test Record

Results of performance tests may be tabulated on the Performance Test Record (table 3-1) at the end of the procedures. The Test Record lists all of the tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison during periodic maintenance, troubleshooting, and after repairs or adjustments.

Performance Test Cycle

This instrument requires periodic verification of performance. The instrument should be checked using the following performance tests at least every twelve months or every 2000 hours of operation. Amount of use, environmental conditions, and the user's experience concerning need for performance checks will contribute in deciding the performance test cycle.

Special Procedures

1. All connectors should be clean and undamaged to ensure accurate measurements. All APC 3.5 (f-f) adapters on the test set should be mechanically and visually checked before inserting any calibration test tool into them. Damaged connectors or loose connections may cause the performance verification tests to fail. See appendix A at the end of the HP 54120B mainframe manual.

2. The system should be allowed to warm up for at least 15 minutes.

3. To avoid damage to the four channel test set connectors, use of the APC 3.5 (f-f) connector savers is encouraged. These connector savers are supplied with the test set. Refer to appendix A at the end of the HP 54120B mainframe manual for more information on mating APC 3.5 connectors with SMA connectors.

4. Avoid sharp bends in the two 17 inch coaxial cables, HP part numbers 8120-4941 and 8120-4942.

5. When mating APC 3.5 connectors to APC 3.5 connectors or devices, torque all connections to 8 in/lbs. When mating APC 3.5 to SMA or SMA to SMA, torque all connections to 5 in/lbs.

6. If possible, minimize connector swapping during the procedures to avoid connector wear. All connectors on test tools and adapter should be inspected both visually and mechanically every few calibrations.

7. The performance test procedures outlined in this section make use of extra connectors. These are used to save expensive parts from repeated excessive wear caused by many reconnections. These parts are not necessary, but their use is highly advised.

8. Throughout the procedures identical connectors are used in different ways. One way is precision at both ends. This means that both ends of the APC 3.5 connector should be precise and should never have been connected to an SMA connector. The other way is precise at one end. This means that one of the APC 3.5 ends may be used with SMA connectors, but the other end should never have been connected to any SMA connectors. Unless otherwise stated, all APC 3.5 connectors should never be connected to SMA connectors.

Note 

Allow instruments to warm up for at least 15 minutes prior to beginning performance tests.

Caution 

The Four Channel Test Set is very sensitive to static discharge. Failure to observe proper antistatic methods may result in damage to the gallium arsenide samplers. All maintenance or operation should be performed with the antistatic mat and wrist strap, which are supplied with the HP 54120B mainframe.

Caution 

Electrostatic discharge can seriously damage the test set's inputs. To eliminate any electrostatic build up from a cable you're connecting to the test set, connect a female short to either end of the cable. Touch the short to an input connector hex nut on the test set to discharge any electrostatic build up to ground. Remove the female short. Use this procedure for all cables before connecting them to the test set.

Bandwidth Test

The following procedure calculates the HP 54121A's bandwidth. The sine wave output of a synthesized sweeper is leveled with a power meter. The sine wave's rms voltage is measured and converted to a power measurement to determine bandwidth. This is done on four frequencies on all four channels. This allows use of the HP 54120B's auto measurement modes to increase the measurement's accuracy.

The specification at 20 GHz is -3 dB, however the generator's vertical output is not synchronized with its 10 MHz reference output at 20.000 GHz. We test the instrument at 19.98 GHz where the specification at 19.98 GHz is -2.99 dB for channels 2 through 4 and -3.49 dB for channel 1.

If this performance test fails, perform the vertical system adjustments in the following order; 10 V reference, step recovery diode, sampler bias, offset gain, and feedthrough compensation adjustments.

Specifications

20 GHz bandwidth at -3 dB
Channel 1 dc to 18 GHz (-3.5 dB at 20 GHz)
Channels 2-4 dc to 20 GHz

12.4 GHz bandwidth at -3 dB
Channels 1-4 dc to 12.4 GHz

Equipment

This is a list of the recommended test equipment for this performance test, however any instrument which satisfies the critical specifications may be used.

Instrument	Critical Specifications	Model
Synthesized sweeper	20 GHz, +6 dBm, 25 dBc subharmonics, noise < 6 dB	HP 8341A/B
RF amplifier	Gain 20 dB at 10 MHz, flatness ±0.7 dB harmonic distortion -32 dB for 0 dBm output	HP 8447A
Power meter	20 GHz	HP 436A
Power sensor	20 GHz	HP 8485A
Calculator	Log base 10 function	HP 11C
20 dB pad	APC 3.5 connections	HP 33340C/020
Accessories	**Critical Specifications**	**HP Part Number**
Adapter	BNC (f) to SMA (m), Quantity needed - 2	1250-1200
Adapter	N (m) to APC 3.5 (m)	1250-1743
Adapter	APC 3.5 (f-f), 26.5 GHz	1250-1865
Adapter	APC 3.5 (m-f), Precise male end	1250-1866
Adapter	APC 3.5 (m-f), Precise both ends	1250-1866
Coaxial cable	APC 3.5 (m-f), 26.5 GHz	8120-4942
BNC cable	Length - 48 inches, Quantity needed - 2	10503A

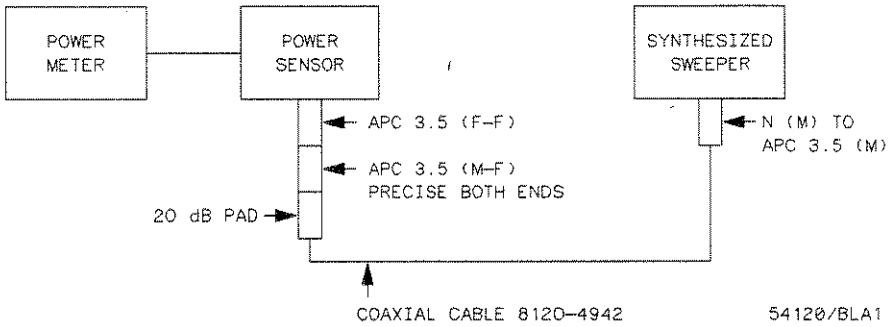
Procedure Characterizing the sweep oscillator's output

Note The sweep oscillator's output will change slightly from one day to the next day. That makes this part of the calibration procedure difficult to repeat. Improperly torqued connectors or the usage of a different 20 dB pad is the most likely source of errors for regaining previously obtained numbers.

Type of Equipment	Model Number	Serial Number
Synthesized sweeper	_____	_____
Power meter	_____	_____
Power sensor	_____	_____

1. Calibrate and zero power meter before connecting sensor to device under test. Use an N type (m) to APC 3.5 (f) adapter.

2. Connect equipment as shown below.



3. Set sweep oscillator's frequency to 50 MHz.

4. Set sweep oscillator's output power to +6 dBm.

5. Set power meter's cal factor to 100%. **DO NOT** change its setting during this procedure.

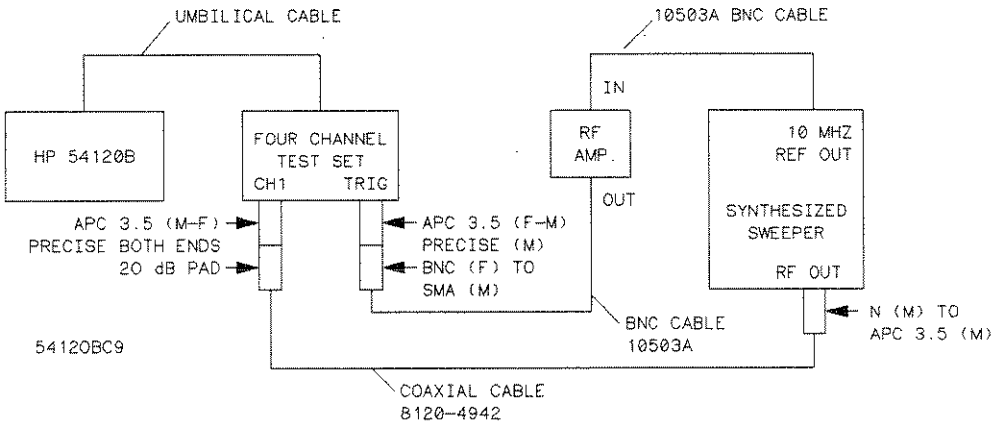
6. Record power meter's reading in μW in step 22 part 1.

7. Set sweep oscillator's frequency to 12.4 GHz, 18 GHz, 19.98 GHz and note power meter's reading in μW in step 22 part 1.

8. Record power sensor's cal factors (CF) in step 22 part 2 (assume 100% for 50 MHz).

Checking the oscilloscope's bandwidth

9. Connect the equipment as shown below.



10. Perform a one-key down power up on the HP 54120B. Hold down any key and cycle the power off and on. Continue to hold the key down until graticules are displayed on screen.

11. Change the oscilloscope's display to 64 averages, bandwidth to 12.4 GHz, and screen to single. Turn channel 1 on and channels 2 through 4 off. Set vertical sensitivity to 20 mV/div on all four channels, and timebase sweep to 5 ns/div.

12. Set sweeper's frequency to 50 MHz.

13. Press **Clear Display** key and wait for 64 averages to accumulate at top left corner of screen.

14. Press **More** key, **Measure** key, **Precision** key until **fine** is highlighted, then RMS Voltage key.

15. Note the VRMS reading on bottom of screen and record the value in step 25 part 3.

16. Change oscilloscope's sweep speed to 15 ps/div.

17. Change sweeper's frequency to 12.4 GHz and repeat steps 13-15.

18. Change display bandwidth mode to 20 GHz.

19A. For channel 1 change sweep oscillator's frequency to 18 GHz and repeat steps 13 through 15.

19B. For channels 1-4 change sweep oscillator's frequency to 19.98 GHz and repeat steps 13 through 15.

20. Change display bandwidth to 12.4 GHz, timebase sweep speed to 5 ns/div.

21. Repeat steps 12 through 20 for channels 2-4.

22. Calculate oscilloscope's three bandwidth gains at 12.4 GHz, 18 GHz, and 19.98 GHz with the values and the formula listed below.

Part 1

Frequency	Sweeper output in μW
50 MHz	37.8 μW
12.4 GHz	38.4 μW
18 GHz	25.9 μW
19.98 GHz	_____ μW

Part 2

Frequency	Power sensor cal. factor
50 MHz	100 %
12.4 GHz	89.0 %
18 GHz	88.3 %
19.98 GHz	_____ %

Part 3

Frequency	Measurement results in RMS volts			
	Ch. 1	Ch. 2	Ch. 3	Ch. 4
50 MHz	43.996 mV	44.543 mV	44.321 mV	44.403 mV
12.4 GHz	11.741 mV	11.416 mV	11.620 mV	11.664 mV
18 GHz	30.455 mV	32.228 N/A	33.225 N/A	33.968 N/A
19.98 GHz	_____ mV	_____ mV	_____ mV	_____ mV

Example: Power Meter Reading at low frequency of 50 MHz = 38.8 μW
Power Meter Reading at high frequency of 20 GHz = 27.6 μW
VRMS of HP 54120A at low frequency of 50 MHz = 43.79 μV
VRMS of HP 54120A at high frequency of 20 GHz = 28.55 μV
CF of power meter at low frequency of 50 MHz = 100%
CF of power meter at high frequency of 20 GHz = 91.7%

$$\text{Gain} = 10 \log_{10} \left[\frac{\text{Power Meter reading 50 MHz}}{\text{Power Meter reading high freq}} \right] \left[\frac{\text{CF high freq}}{\text{CF 50 MHz}} \right] \left[\frac{V_{RMS} \text{ high freq}}{V_{RMS} \text{ 50 MHz}} \right]^2$$

54120BDO

$$-2.6\text{dB} = 10 \log_{10} \left[\frac{38.8\ \mu w}{27.6\ \mu w} \right] \left[\frac{91.7\%}{100\%} \right] \left[\frac{28.55\ \mu V}{43.79\ \mu V} \right]^2$$

DC Voltage Measurement Accuracy and RMS Noise Test

This test checks the offset accuracy, offset gain accuracy, sampler gain accuracy, and the RMS noise level of the HP 54120B and HP 54121A. If this performance test fails, perform the vertical system adjustments in the following order; 10 V reference, step recovery diode, sampler bias, offset gain, and feedthrough compensation adjustments.

Specifications

DC voltage accuracy (50 Ω source)

Single voltage marker
Average mode ±0.4% of full-scale or marker reading (whichever is greater) ±2 mV
20 GHz Persistence mode ±0.4% of full-scale or marker reading (whichever is greater) ±2 mV ±3% of (reading − channel offset)
12.4 GHz Persistence mode ±0.4% of full-scale or marker reading (whichever is greater) ±2 mV ±1.5% of (reading − channel offset)

Dual voltage markers (on same channel)
Average mode ±0.8% of full-scale or delta reading (whichever is greater)
20 GHz Persistence mode ±0.8% of full-scale or delta reading (whichever is greater) ±3% of delta marker reading
12.4 GHz Persistence mode ±0.8% of full-scale or delta reading (whichever is greater) ±1.5% of delta marker reading

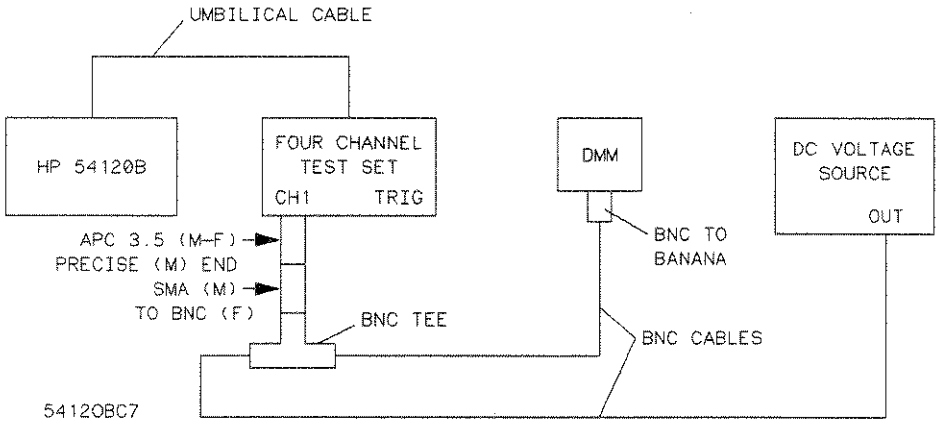
RMS noise in persistence mode (1 sigma)
20 GHz bandwidth mode ≤2 mV (Applies to instruments with HP 54120B firmware dated June 14, 1989 and later)
12.4 GHz bandwidth mode ≤1 mV

Equipment

This is a list of the recommended test equipment for this performance test. However, any instrument which satisfies the critical specifications may be used.

Instrument	Critical Specifications	Model
DC voltage source	±1/2 volt, 100 μV resolution	HP 3325A
DMM	5 1/2 digits	HP 3478A
Accessories	**Critical Specifications**	**HP Part Number**
BNC cable	Length - 48 inches, Quantity needed - 2	10503A
BNC Tee		1250-0781
Adapter	BNC (f) to SMA (m)	1250-1200
Adapter	APC 3.5 (m-f), 26.5 GHz, Precise male end	1250-1866
Adapter	BNC to banana	1250-2277

Equipment Connections



Caution Exceeding ±2 V on the dc power supply may damage the test set's input.

Equipment Setup

DC Voltage Source

Mode	dc
Offset	500 mV
Output	enabled

HP 54120B

Display	
Display Mode	Averaged
No. of Averages	16
Screen	Single
Graticule	Frame
Bandwidth	12.4 GHz

Trigger	
Trigger Level	0 V
Slope	Pos
HF Sens.	Off
HF Reject	Off
Attenuation	1

Channels	
Channels	1-4
Display	Off
Volts/Div	5 mV/div
Offset 0	V
Attenuation	1

Network	
Reflect/Trans/CAL	Reflect
Step Chan 1	Off

Timebase	
Time/Div	1 ms/div
Delay	200 ns
Delay Ref at	Left
Sweep	Freerun
Freerun Rate	10 KHz

Procedure DC Voltage Measurement Accuracy

1. Press **Save Setup** key, then **1** on the HP 54120B.
   This saves the front panel setup in memory location 1.

2. Change vertical sensitivity on channels 1-4 to 80 mV/div, and display mode to a persistence of 300 ms.
   Press **Save Setup** key, then **2** key on oscilloscope.

3. If BNC tee is connected to the four channel test set, remove the tee and leave it disconnected for now.

4. Press **Recall Setup** key, then **1** key.
   This recalls instrument setup from memory location 1.
   Turn channel 1 on.

5. Turn Delta V markers on and overlay both markers on channel 1.
   Press **Preset Levels** until **50%-50%** is highlighted.

6. Press **Clear Display** key and wait for 16 averages to accumulate on top left of screen.

7. Press **Auto Level Set** key and note the V1 value.
   V1 should be 0 V ±2.16 mV. 312.5 uV | 1.8750mV | -156.25uV | 781.2

8. Press **Display** key and change bandwidth to 20 GHz.

9. Press **Clear Display** key and wait for 16 averages to accumulate.
   Press **Delta V** menu key, then **Auto Level Set** key.
   The V1 value should be 0 V ±2.16 mV. -468.75uV | -781.25uV | 156.25uV | 1,406

10. Connect BNC tee to channel 1.

11. Change channel 1 offset to 500 mV.
    Change display bandwidth to 12.4 GHz.

12. Adjust dc source until DMM reads 500 mv ±100 MV.

13. Press **Clear Display** key and wait for 16 averages to accumulate.
    Turn Delta V markers on and overlay marker 2 on trace.
    The V2 value should be 500 mV ±4 mV.

503.90 | 502.96 | 500.46 mV | 501.87

14. Change channel 1 offset to −500 mV.

15. Adjust dc source until DMM reads −500 mV ±100 MV.

16. Press **Clear Display** key and wait for 16 averages to accumulate.
    Turn Delta V markers on and overlay marker 1 on trace.
    The V1 value should be −500 mV ±4 mV. -498.90 | -499.21 | -499.84mV | -500.
    The delta V value should be 1.0000 V ±8 mV. 1.00028 V | 1.0021 | 1.0035V | 1.00

17. Recall instrument setup from memory location 2. Turn channel 1 on.

18. Press **More** key, then press **Wfm Math** key.
    Press **Function** key until **1** is highlighted.
    Press **Display** key until **On** is highlighted.

19. Change **first Chan-Mem** key until **Chan 1** is highlighted.
    Press **Operation** key until **Only** is highlighted.
    Press **Display Scaling** key until **Volts/Div** is highlighted.

20. Adjust sensitivity to 5 mV/div.
    Press **Display Scaling** key until **Offset** is highlighted.
    Adjust offset to 250 mV.

21. Adjust dc source until DMM reads 250 mV ±100 μV.

22. Turn Delta V markers on and overlay both markers on function 1.
    Press **preset levels** until **50%-50%** is highlighted.

23. Manually overlay delta V marker 1 to center of trace.
    The V1 value should be 250 mV ±9.66 mV.
    250 mV | 250 mV | 249.68mV | 251.56mV

24. Press **Wfm Math** key.
    Press **Display Scaling** key until Offset is **highlighted**.
    Adjust offset to −250 mV.

25. Adjust dc source until DMM reads −250 mV ±100 MV.

26. Manually overlay delta V marker 2 to center of trace.
    The V2 value should be −250 mV ±9.66 mV.
    -250 mV | -251.56 | -249.68 | -249.21

27. Press **Recall 2** key. Ensure bandwidth is set to 12.4 GHz

28. Disconnect all signals from channel 1.

29. Change display mode to infinite persistence, and timebase delay to 16 ns.

30. Turn function display off.
    Change channel 1 sensitivity to 2 mV/div and 0 V offset.

31. Press **Histogram** menu key and then press **Window/Acquire/Results** key until **Window** is highlighted.

32. Press **Voltage/Time** key until **Voltage** is highlighted.

33. Set windows to screen's left and right sides.

34. Press **Window/Acquire/Results** key until **Acquire** is highlighted.
    Select 10000 samples and press **Start Acquiring** key.
    Wait until oscilloscope finishes acquiring data.

35. Press **Window/Acquire/Results** key until **Results** is highlighted.
    Press **Sigma** key.
    The sigma value should be ≤ 1 mV.
    317.87 µV | 315.68 µV | 310.58 µV | 287.33 µV

36. Steps 37 and 38 apply to instruments with high bandwidth (20 GHz) persistence mode. To determine if you have high bandwidth persistence, go to the display menu, set display mode to persistence, and toggle the bandwidth key. If the bandwidth toggles between 12.4 GHz and 20 GHz, you have high bandwidth persistence. If you do not have high bandwidth persistence, go to step 39.

NO GOT

37. Press the **More** menu key, then **Display** menu key.
    Change bandwidth to 20 GHz.

38. Repeat steps 31 to 35 for 20 GHz.
    The sigma value should be ≤ 2 mV

39. Repeat steps 3 to 38 for channels 2, 3, and 4.

Time Interval Accuracy Test

This tests the accuracy of all timebase delay counter modes. If this performance test fails, perform these adjustments in the following order; delta current, range, frequency, end, and 4 ns cal adjustments.

Specifications

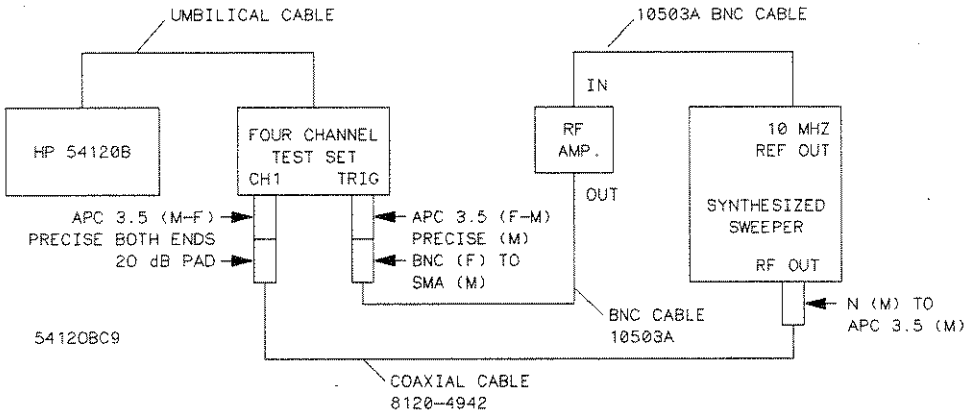
Time interval accuracy 10 ps ±0.1% of reading

Equipment

This is a list of the recommended test equipment for this performance test, however any instrument which satisfies the critical specifications may be used.

Instrument	Critical Specifications	Model
Synthesized sweeper	20 GHz, -25 dBc harmonics, output +6 dBm stability 0.25 ppm/yr	HP 8341A/B
20 dB pad	APC 3.5 connections	HP 33340C/020
RF amplifier	Gain 20 dB at 10 MHz, flatness ±0.7 dB, harmonic distortion -32 dB, for 0 dB output noise 6 dB	HP 8447A
Frequency synthesizer	10 MHz square wave, 120 mV output, stability 0.05 ppm/yr	HP 3325A/001
Accessories	**Critical Specifications**	**HP Part Number**
Adapter	BNC (f) to SMA (m), Quantity needed - 2	1250-1200
Adapter	N (m) to APC 3.5 (m)	1250-1743
Adapter	APC 3.5 (m-f), Precise both ends, 26.5 GHz	1250-1866
Adapter	APC 3.5 (m-f), Male end precise, 26.5 GHz Quantity needed - 2	1250-1866
Coaxial cable	APC 3.5 (m-m), 26.5 GHz	8120-4942
BNC cable	Length - 48 inches, Quantity needed - 2	10503A

Equipment Connections



Equipment Setup

Synthesized Sweeper

Mode	Sine wave
Frequency	19.98 GHz
Amplitude	+6 dBm

Frequency Synthesizer

Mode	Square wave
Frequency	10 MHz
Amplitude	120 mV

HP 54120B

Display

Display Mode	Averaged
No. of Averages	64
Screen	Single
Graticule	Frame
Bandwidth	20 GHz

Channels

Channels	1-4
Display	Off
Volts/Div	20 mV/div
Offset	0 V
Attenuation	1

Timebase

Time/Div	10 ps/div
Delay	16 ns
Delay Ref at	Left
Sweep	Trd's d

Trigger

Trigger Level	0 V
Slope	Pos
HF Sens.	Off
HF Reject	Off
Attenuation	1

Network

Reflect/Trans/CAL	Reflect
Step Chan 1	Off

Procedure Short Delta T

1. Press **Save Setup** key, then 3 key.
   Turn channel 1 on.

2. Press **Clear Display** key and wait until 64 averages accumulate.

3. Press **Measure** menu key.
   Press **Precision** key until **fine** is highlighted.

4. Press **Period** key to measure period of 19.98 GHz sine wave.
   The period should be 50.1 ps ± 10.1 ps.

5. Repeat steps 2 through 4 for timebase delay settings of 18 ns, 19.9 ns, 19.95, 23.95 ns, 27.95 ns, and 55.95 ns.

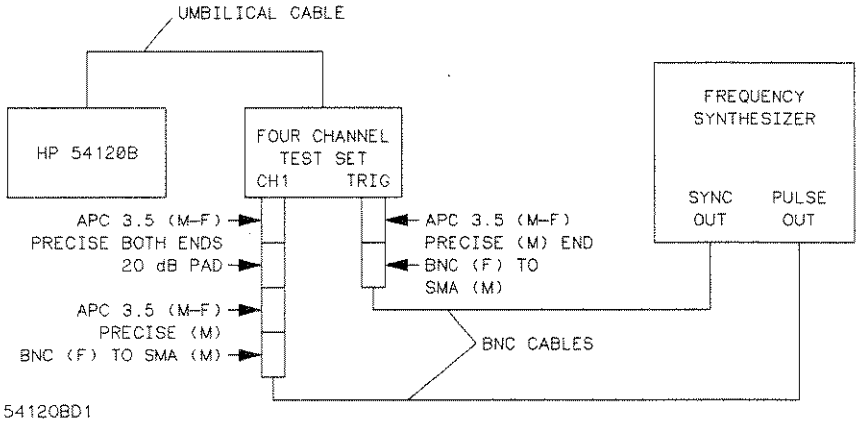
6. Change timebase delay to 16 ns and display bandwidth to 12.4 GHz.

7. Repeat step 2 through 4 for the following oscilloscope timebase settings and sweeper frequency settings. Ensure the measured results are within the allowable limits.

Timebase Setting	Sweeper Setting	Test Limits
50 ps/div	10 GHz	100 ps ± 10.1 ps
10 0 ps/div	5 GHz	200 ps ± 10.2 ps
250 ps/div	2 GHz	500 ps ± 10.5 ps
500 ps/div	1 GHz	1 ns ± 11 ps
1 ns/div	500 MHz	2 ns ± 12 ps
2.5 ns/div	200 MHz	5 ns ± 15 ps
5 ns/div	100 MHz	10 ns ± 20 ps
10 ns/div	50 MHz	20 ns ± 30 ps
25 ns/div	20 MHz	50 ns ± 60 ps

Long Delta T

8. Change the equipment setup as follows.



9. Press **Recall 3**.

10. Change timebase sweep to 20 ns/div and trigger level to 500 mV.

11. Press Clear Display key and wait until 64 averages accumulate.

12. Press **Measure** menu key.
    Press **Precision** key until **fine** is highlighted.

13. Press **Period** key and wait for oscilloscope to measure period of a 10 MHz sine wave. The period should be 100 ns ±110.0 ps.

14. Repeat steps 10 through 13 for the following settings. Ensure the measured values are within the allowable limits.

Timebase Setting	Sweeper Setting	Test Limits
100 ns/div	5 MHz	200 ns ±210 ps
250 ns/div	2 MHz	500 ns ±510 ps
500 ns/div	1 MHz	1 µs ±1.01 ns
1 µs/div	500 kHz	2 µs ±2.01 ns
2.5 µs/div	200 kHz	5 µs ±5.01 ns
5 µs/div	100 kHz	10 µs ±10.01ns
10 µs/div	50 kHz	20 µs ±20.01 ns
25 µs/div	20 kHz	50 µs ±50.01 ns (0.05001 µs)
50 µs/div	10 kHz	100 µs ±100.01 ns (0.10001 µs)

Trigger Sensitivity and Jitter Tests

The sensitivity test measures the high and low frequency trigger sensitivities by applying a 100 MHz sine wave and a 2.5 GHz sine wave. If the oscilloscope triggers at 2.5 GHz, it will also trigger on a 200 ps pulse width at 200 mV. If this performance test fails, adjust the trigger hysteresis and trigger offset adjustments in section 4, adjustments, of this manual.

The jitter test measures the oscilloscope's internal jitter with a 2.0 GHz sine wave. The instrument's jitter is less with fast risetime input signals. If a generator is substituted, careful consideration of the generator's horizontal jitter and vertical noise is important.

Some HP 54121A test sets with serial prefix 2714 and 2802 may still use the 500 MHz trigger hybrid. If you are unsure which trigger hybrid your instrument has, remove the test set's bottom cover and locate the trigger hybrid on the horizontal board's front left side (refer to figure 4-12 in section 4, adjustments of this manual). The 500 MHz trigger hybrid HP part number is 1NB7-8160. The 500 MHz trigger specifications are, sensitivity: dc to 100 MHz 40 mV p-p, 100 MHz to 500 MHz 100 mV p-p.
jitter: trigger and timebase combined (one standard deviation) $\leq$ 5 ps + (5E-5 x delay setting).

Specifications

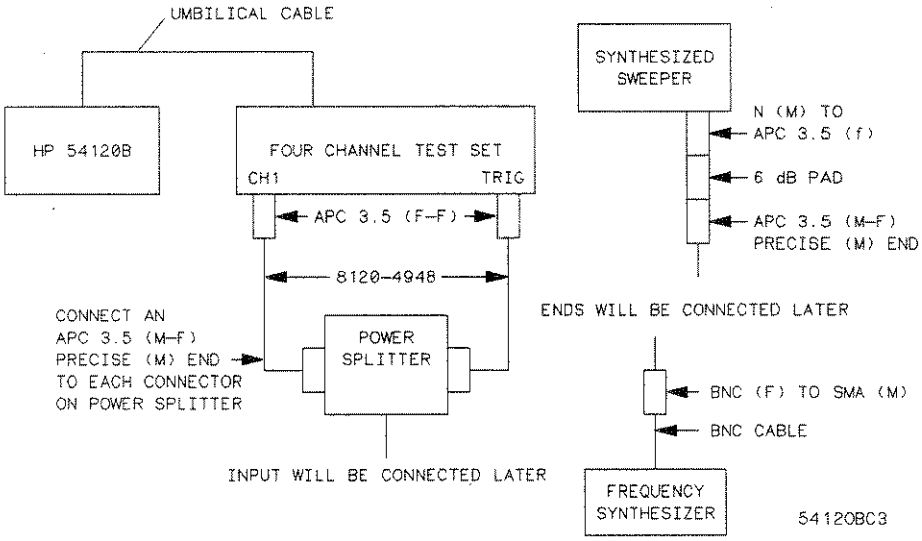
Sensitivity: dc to 100 MHz 40 mV peak-to-peak, increasing linearly to 200 mV peak-to-peak at 2.5 GHz
Jitter: Trigger and timebase combined (one standard deviation)
< 2.5 ps + 5 E-5 x delay setting. Tested using 2 GHz synthesized source at 200 mV peak-to-peak with high frequency sensitivity on and high frequency reject off.

Equipment

This is a list of the recommended test equipment for this performance test. However, any instrument which satisfies the critical specifications may be used.

Instrument	Critical Specifications	Model
Synthesized sweeper	20 GHz, +6 dBm	HP 8341/003
Power splitter	> 10 GHz bandwidth	HP 11667B
Frequency synthesizer	100 kHz sine wave, 200 mV output	HP 3325A
Delay line	22 ns, < 6 dB attenuation at 2 GHz	HP 54008A
Accessories	**Critical Specifications**	**HP Part Number**
Adapter	APC 3.5 (m-m) both ends precise	1250-1864
Adapter	APC 3.5 (m-f) Both ends precise, 26.5 GHz Quantity needed - 6	1250-1866
Adapter	N (m) to APC 3.5 (f)	1250-1744
Adapter	SMA (m) to BNC (f)	1250-1200
Adapter	SMA (f-f)	1250-1158
Coaxial cable	APC 3.5 (m-m) 18 GHz, Quantity needed - 3	8120-4948
BNC cable	48 inches	10503A
6 dB pad	APC 3.5 connectors	33340C/006

Equipment Connections



Equipment Setup

Frequency Synthesizer

Frequency	100 KHz
Power output	200 mV
Mode	Sine wave

Synthesized Sweeper

Frequency	100 MHz
Power output	0 dBm

HP 54120T

Display

Display Mode	Averaged
No. of Averages	4
Screen	Single
Graticule	Frame
Bandwidth	12.4 GHz

Trigger

Trigger Level	0 V
Slope	Pos
HF Sens.	Off
HF Reject	Off
Attenuation	1

Channels

Channels	1-4
Display	Off
Volts/Div	20 mV/div
Offset	0 V
Attenuation	1

Timebase

Time/Div	1 µs/div
Delay	16 ns
Delay Ref at	Left
Sweep	Trg'd

Network

Reflect/Trans/CAL	Reflect
Step Chan 1	Off

Procedure

Low Frequency Trigger Hysteresis

Values in brackets are used only for the 500 MHz trigger hybrid.

1. Connect frequency synthesizer to power splitter.

2. Turn channel 1 on.

3. Adjust frequency synthesizer until signal on screen is exactly 100 mV p-p.

4. Slowly adjust trigger level greater than 0 V until oscilloscope just stops triggering. This is indicated on screen by pressing the **Clear Display** key each time the trigger level is changed. If the oscilloscope is triggered, the waveform will be displayed on screen. Note the trigger level, this is V_{pos}.

5. Return trigger level to 0 V. Slowly adjust trigger level less than 0 V until oscilloscope just stops triggering. This is V_{neg}.

6. Calculate hysteresis. $V_{hysteresis} = 100\ mV - (V_{pos} - V_{neg})$ The value should be ≤ 40 mV.

100 MHz/2.5 GHz Trigger Sensitivity

7. Change oscilloscope's timebase sweep speed to 2 ns/div, trigger level to 0 V. Turn HF Reject off and HF Sens. off.

8. Connect synthesized sweeper (set to 100 MHz) to power splitter.

9. Adjust sweeper's amplitude to exactly 150 mV amplitude as displayed on screen.

10. Slowly adjust trigger level greater than 0 V until oscilloscope just stops triggering. This is V_{pos}.

11. Return trigger level to 0 V. Slowly adjust trigger level less than 0 V until oscilloscope just stops triggering. This is V_{neg}.

12. Calculate sensitivity. $V_{sense} = 150\ mV - (V_{pos} - V_{neg})$. The value should be ≤ 40 mV.

13. Turn HF Reject on and repeat steps 10 through 12 [HF reject is not active with the 500 MHz trigger so proceed to step 14]. The value should be ≥ 57 mV (+3 dB).

14. Change oscilloscope's sweep speed to 100 ps/div, sensitivity to 50 mV/div, and trigger level to 0 V. Turn HF Sens. on and HF Reject off.

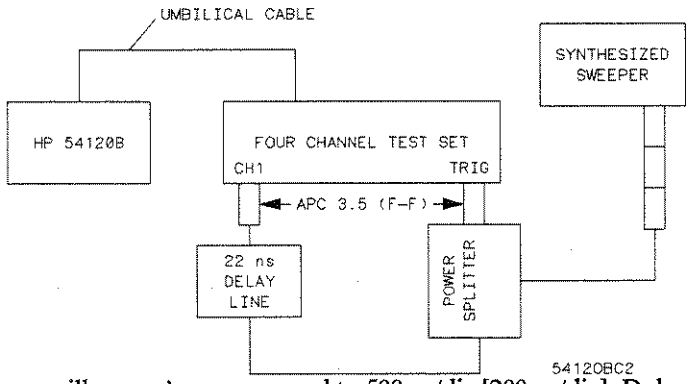
15. Change sweeper's frequency to 2.5 GHz [500 MHz] and adjust sweeper's amplitude to exactly 200 mV [100 mV] as displayed on screen. Oscilloscope should be triggered.

16. Slowly adjust trigger level greater than 0 V until oscilloscope just stops triggering. This is V_{pos}.

17. Return trigger level to 0 V. Slowly adjust trigger level less than 0 V until oscilloscope just stops triggering. This is V_{neg}.

18. Calculate sensitivity. $V_{sense} = 200\ mV - (V_{pos} - V_{neg})$. The value should be ≤ 200 mV [100 mV].

19. Change sweeper's frequency to 2.0 GHz [500 MHz]. The amplitude should still be set to 200 mV p-p [100 mV]. Add delay line and change equipment setup as shown below.



20. Change oscilloscope's sweep speed to 500 ps/div [200 ps/div], Delay Ref at center, and delay to 20 ns.

21. Slightly vary the sweeper's frequency and select the trigger point which does not expand or contract with the sweeper's frequency changes (using infinite persistence may you help find the trigger edge).

22. Turn Delta V markers on.
Press **Preset Levels** key until **50%-50%** is highlighted. Press **Auto Level Set** key.

23. Turn Delta T markers on, and set start marker on 50% point of selected trigger point's positive slope.

24. Change sweep speed to 200 ps/div [100 ps/div] and delay to start marker's value.

25. Adjust oscilloscope's delay to center waveform's positive edge on screen.
Delay = _____ ns

26. Change oscilloscope's sweep speed to 10 ps/div [20 ps/div] and sensitivity to 5 mV/div.

27. Press **Histogram** menu key.
Press **Window/Acquire/Results** key until **Window** is highlighted.
Press **Time/Voltage histogram** key until **Time** is highlighted.
Set window marker 1 to −0.25 mV and window marker 2 to 0.25 mV.

28. Press **Window/Acquire/Results** key until **Acquire** is highlighted, enter number of samples as 1000. Press **Start acquiring** key. Wait until acquire cycle is 100% complete.

29. Press **Window/Acquire/Results** key until **Results** is highlighted. Press **Sigma** key. Sigma value should be < 2.5 ps + (5E-5 x delay setting from step 26) [≤ 5 ps + (5E-5 x delay setting)]. If the instrument does not meet the jitter specification, it is allowable to adjust trigger level for best jitter. You would then need to repeat steps 20 through 29. Example with delay setting of 20.5 ns:
$\leq 2.5\text{ ps} + [(5 \times 10^{-5}) \times (20.5 \times 10^{-9})] = 2.5\text{ ps} + 1.025\text{ ps} \leq 3.525\text{ ps}$

TDR System Tests

This test verifies correct operation of the TDR system by checking the specifications of both the TDR system and the oscilloscope. The final value of the TDR step generator's amplitude is controlled by the the dc resistance of the 50 Ω termination. Since all of the flatness specifications depend on the final value measured in this test, the effects of using a nonperfect 50 Ω termination are accounted for during the procedure.

The dc resistance of a nonperfect 50 Ω termination will effect the on-screen final value. Figure 3-1 shows the first 1 ns after the incident step using two different 50 Ω terminations. Notice the two traces are coincident for approximately the first 500 ps until the 50 Ω termination is encountered. The two traces finally settle with a constant level shift between them. The amount of the level shift is dependent on the dc resistance variation between the 50 Ω terminations used.

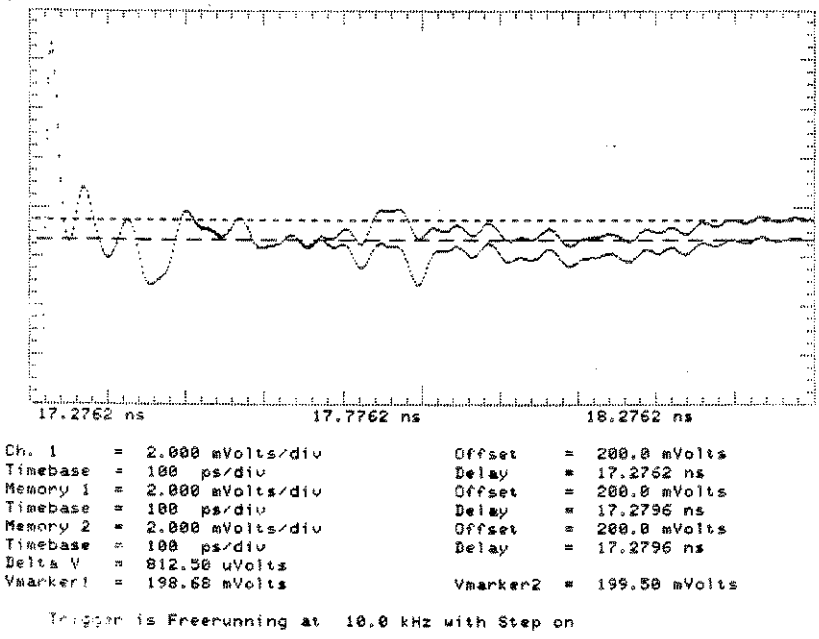


Figure 3-1. Incident Step With Two Different 50 Ω Terminations, Top Trace dc Resistance = 50.34 Ω, Bottom Trace dc Resistance = 49.91 Ω

The final value recorded in the procedure is the final value that a perfect 50 Ω termination would present. This number is calculated based on the actual dc resistance of the 50 Ω termination used.

There are two sets of flatness specifications, both are referenced to 1 ns after the incident step. One specification is before the 1 ns reference point.
The other specification is after the 1 ns reference point.

For the ±1% tests (> 1 ns after edge) a delta V measurement is made between the actual on-screen final value and the reflections from the 50 Ω termination. This delta V measurement will be independent of the dc resistance of the 50 Ω termination. This value is divided by the final value calculated for a 50 Ω termination's final value and multiplied by 100%.

For the +5%, −2% tests (<1 ns after edge) a different approach must be used. If the −2% reflection appears before the 50 Ω termination in time, then a delta V measurement using the on-screen final value and voltage value of that reflection will be dependent on the dc resistance of the 50 Ω termination . This is not true if the reflection appears after the 50 Ω termination in time.

Reflection appears before the termination The recorded final value is subtracted from the reflection's voltage value, then divided by the recorded final value and than multiplied by 100%.

Reflection appears after the termination The on-screen final value is subtracted from the reflection's voltage value, then divided by the recorded final value and multiplied by 100%.

The overshoot (+5% at <1 ns after edge) calculation is identical to the −2% test (reflections before the 50 Ω termination) since the overshoot appears before the termination in time.

If this performance test fails, perform the TDR adjustments in paragraph 4-15.

Specifications:

Combined oscilloscope and TDR risetime performance ≤45 ps[1]
(measured in 12.4 GHz bandwidth, averaged mode)

Combined oscilloscope and TDR flatness performance
(measured in 12.4 GHz bandwidth, averaged mode)
After 1 ns from edge ±1%
+5%, −3% to 1 ns from edge

Combined oscilloscope and TDR levels performance
Low - 0 V ±2 mV
High -200 mV ±2 mV

Equipment

This is a list of the recommended test equipment for this performance test, however any instrument which satisfies the critical specifications may be used.

Instrument	Critical Specifications	Model
Termination	50 Ω, APC 3.5 (f)	HP 909D/011
DMM	5 1/2 digits	HP 3478A
Accessory	**Critical Specifications**	**HP Part Number**
Adapter	BNC (m-m)	1250-0216
Adapter	BNC (f) to banana	1250-2277
Adapter	BNC (f) to SMA (m)	1250-1200
Adapter	APC 3.5 (m-f) male end precise	1250-1866
Coaxial short	APC 3.5 (f)	1250-2127

1. The risetime of the generator is less than 35 ps, as calculated by
$(T_{r\ system})^2 = (T_{r\ generator})^2 + (T_{r\ oscilloscope})^2$

Equipment setup: Perform a one-keydown power up. Hold down any key and cycle the oscilloscope's power off and on. Continue to hold the key down until graticules are displayed on screen. Make the following changes to the oscilloscope's setup.

HP 54120B

Display		**Timebase**	
Display Mode	Averaged	Time/Div	50 ps/div
No. of Averages	16	Delay	16 ns
Screen	Single	Delay Ref at	Left
Graticule	Frame	Sweep Freerun	
Bandwidth	12.4 GHz	Rate	10 kHz
Channels		**Network**	
Channel	1	Reflect/Trans/CAL	Reflect
Display	On	Step & Chan 1	On
Volts/Div	5 mV/div		
Offset	0 V		
Channels	2-4		
Display	Off		

Note If there is a rising edge on screen, the "TDR Step Adjustments" in section 4 must be performed before continuing with this procedure.

Procedure:

1. Assemble a fixture by connecting a banana to BNC (f) adapter to a BNC (m-m) adapter. Connect this to a BNC (f) to SMA (m) adapter. Connect this to an APC 3.5 (m-f) adapter (male end precise and connect fixture to DMM . Connect an APC 3.5 (f) precise 50 Ω termination to fixture.
   Record dc resistance of 50 Ω termination here 51.34 Ω Example 50.390 Ω

2. Remove 50 Ω termination and connect the APC 3.5 (f) short to fixture.
   Record dc resistance of fixture here .03 Ω Example 0.050 Ω

3. Subtract fixture's resistance (step 2) from termination resistance (step 1).
   Step 1 51.34 Ω − Step 2 .03 Ω = Z_L 51.31 Ω Example 50.340 Ω

4. Solve for E_R using this formula (E_R may be a negative number).
   $E_R = 200((Z_L - 50) \div (Z_L + 50))$ (round to nearest 0.01 mV)Example 0.68 mV (1.31 ÷ 101.31) = .0129306
   2.586216 mV
   Install 50 Ω termination on channel 1.

5. Select Delta V menu and press **V Markers** key until **On** is highlighted.
   Press **Preset Levels** key until **50%-50%** is highlighted.
   Press **Auto Level Set** key.
   V(1) should read 0 V ±2 mV.
   Record V(1) here 937.5 µV ~~mV~~.Example 156.25 µV

6. Change oscilloscope's sweep speed to 1 ns/div, channel 1 vertical sensitivity to 80 mV/div, and offset to 200 mV.

7. Select Delta V menu and press **Preset Levels** key until **50%-50%** is highlighted.
   Press **Auto Level** Set key.

8. Select Delta T menu and press **T Markers** key until **On** is highlighted.
   Press **START ON EDGE** key until **POS 1** is highlighted.
   Press **STOP ON EDGE** key until **POS 1** is highlighted.
   Press **Precise Edge Find** key.

9. Change Stop marker's value to the Start marker's value plus 1 ns.
   17.5138 ns

10. Change oscilloscope's sweep speed to 100 ns/div, delay to Stop marker's value, and channel 1 vertical sensitivity to 2 mV/div.

11. Select Delta V menu and overlay marker 1 on trace at right edge of screen.
    Record V(1), on-screen final value, here 200.43 mVExample 200.37 mV

12. Subtract the value of E_R (from step 4) from V(1) and record that value, recorded final value, here 199.843 mV Example 199.69 mV
    This value should be 200 mV ±2 mV.

13. Allow 16 averages to accumulate.
    Adjust marker 2 to signal's highest point on the screen.
    Divide the delta V reading by the final value obtained in step 12 and multiply by 100%.
    (delta V reading 875.01uV ÷ step 12 199.843mV)100% = .43784 %
    Example (812.50 µV ÷ 199.69 mV) 100% = 0.41%
    The absolute value of this number should be less than 1% (+1% at <1 ns after edge).

14. Adjust marker 2 to signal's lowest point on the screen.

15. Select Timebase menu and press **TIME/DIV** key.
    Press front panel increment key to select the next fastest sweep speed.
    If there is a point on the screen lower than marker 2's previous position, readjust marker 2 to that lowest point,
    Repeat this step until a sweep speed of 1 ns/div is reached.

16. Divide the absolute value of delta V by the final value obtained in step 12 and multiply by 100%.
    (delta v reading -1.99mV ÷ step 12 199.843mV) 100% = 1.376
    Example (−1.8125 mV ÷ 199.69 mV) 100% = 0.91%
    The absolute value of of this number should be ≤1% (−1% at <1 ns after edge).

17. Change timebase sweep speed to 200 ps/div, delay reference to center, and delay equal to Start marker's value. Change channel 1 sensitivity to 80 mV/div.

18. Remove the 50 Ω termination and place the APC 3.5 (f) short on channel 1.

19. Select Delta V menu and press **Preset Levels** key until **50%-50%** is highlighted.
Press **Auto level** set key.

20. Select Delta T menu.
Press **START ON EDGE** key until **POS 1** is highlighted.
Press **STOP ON EDGE** key until **NEG 1** is highlighted.
Press **Precise Edge Find** key.

21. Remove short from channel 1 and connect 50 Ω termination to channel 1.
Change timebase Delay Ref to Left and delay equal to Start marker's value.
Adjust Stop marker to value of Start marker plus 0.5 ns (500 ps).
Change sweep speed to 100 ps/div and vertical sensitivity to 2 mV/div.

12 = 199.947 mV

22. Select Delta V menu and adjust marker 2 to the signal's lowest point on the screen. **DO NOT** include the signal's rising edge. If this point is to the left of the Stop marker, then subtract the final value obtained in step 12 from V(2) and record that value in step 23.
Refer to figure 3-2. V(2) 200.0 mV mV Example 196.75 mV

Otherwise subtract the value obtained in step 11 from V(2) and record that value in step 24
(round to nearest 0.01mV).

23. -2% test -.157 mV.Example -2.94 mV

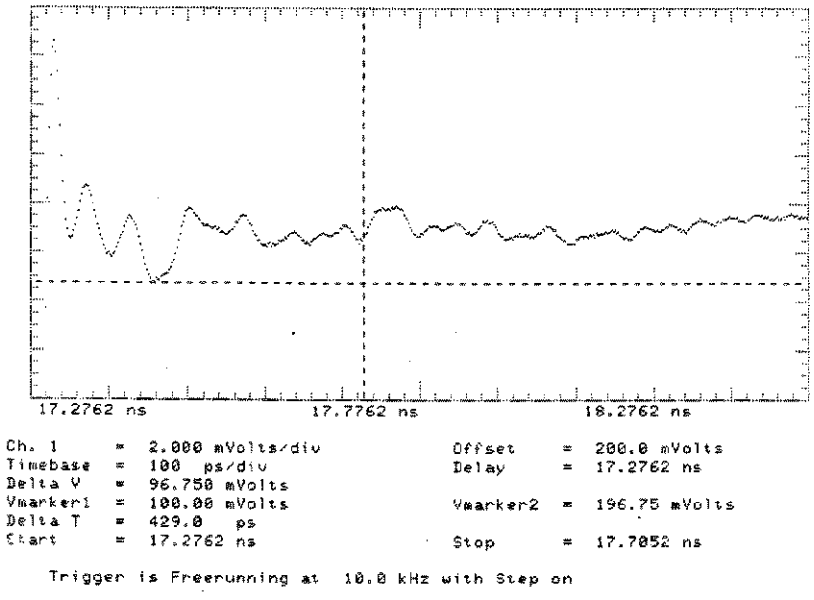


Figure 3-2. -2% Test., The Reflection Appears Before the Termination

24. Divide the value obtained step 23 by the final value obtained in step 12 and multiply by 100%.
(step 23 .157mV ÷ step 12 199.843mV) 100% = .07856
Example (−2.94 mV ÷ 199.69 mV) 100% = −1.47 %
The absolute value of this number should be less than 3% (−3% at < 1 ns after edge).

25. Adjust marker 2 to the signal's highest point on the screen V(2)
205.60 .Example 206.56 mV
Subtract the final value obtained in step 12 from V(2) and record that value in step 26.

26. +5% test 5.157 mV.Example 6.87 mV

27. Divide the value obtained step 26 by the final value obtained in step 12 and multiply by 100%.
(step 26 5.157mV ÷ step 12 199.843mV) 100% = 2.58
Example (6.87 mV ÷ 199.69 mV) 100% = 3.44%
The absolute value of this number should be less than 5% (+5% at < 1 ns after edge).

28. Using the keypad, adjust marker 2 to value obtained in step 11.
Using the keypad, change marker 1's value equal to the value recorded in step 5 above.

29. Change sweep speed to 30 ps/div.
Press **Delay Ref at** key until **Center** is highlighted.

30. Change delay value equal to Start marker's value.
Change channel 1 vertical sensitivity to 30 mV/div and offset to 100 mV.

31. Select Delta V menu.
Press **Preset Levels** key until **10%-90%** is highlighted.
DO NOT touch the Auto Level Set key.

32. Select Delta T menu.
Press **START ON EDGE** key until **POS 1** is highlighted.
Press **STOP ON EDGE** key until **POS 1** is highlighted.

33. Press **Precise Edge Find** key.
The measured risetime (delta T) should be ≤ 45 ps. 36.2 ps

Input Reflection Test

This test uses a calibrated four channel test set channel to measure the amount of reflection each channel reflects back to the test line when pulsed with a fast edge signal.

Specifications:

Percent Reflection
Channels 1-4 $\pm 5\%$ for 30 ps risetime
External Trigger $\leq 10\%$ for 100 ps risetime

Equipment

This is a list of the recommended test equipment for this performance test, however any instrument which satisfies the critical specifications may be used.

Instrument	**Critical Specifications**	**Model**
Termination	50 Ω, APC 3.5 (f)	HP 909D/011
Accessories	**Critical Specifications**	**HP Part Number**
Adapter	APC 3.5 (m-m) 26.5 GHz	1250-1864
Adapter	APC 3.5 (f-f) 26.5 GHz	1250-1865
Coaxial short	APC 3.5 (f)	1250-2127
Coaxial short	APC 3.5 (m)	1250-2128
Cable	Semi-rigid U shaped	54121-61601
Cable	Semi-rigid S shaped	54121-61602

Connections:

1. Do not tighten the following connections until step 5.
2. Connect short end of semi-rigid U cable to short end of semi-rigid S cable through an APC 3.5 (f-f) adapter.
3. Connect semi-rigid U cable's other end to channel 1.
4. Without bending or damaging the semi-rigid cables, bring the semi-rigid S cable's other end toward channel 2. You will be told to connect the semi-rigid cable to channel 2 later in the procedure.
5. Tighten all cable connections.

Equipment Setup:

Perform a one-keydown power up. Hold down any key and cycle the oscilloscope's power off and on. Continue to hold the key down until graticules are displayed on screen. Change the following oscilloscope settings.

HP 54120B

Display		**Timebase**	
Mode	Averaged	Time/Div	350 ps/div
No. of averages	16	Delay	23.5 ns
Screen	Single		
Channels		**Network**	
Channel	1	Reflect/Trans/CAL	Reflect
Display	On	Step & Chan 1	On
Volts/Div	5 mV/div		
Offset	200 mV		
Channels	2-4 Off		

Procedure

1. Adjust delay so that the signal's second rising edge (representing an open circuit condition) is 4 divisions left of center screen.
   Press **Network** menu.
   Press **Reflect/Trans/CAL** key until **Cal** is highlighted.

2. Press **Reflect Cal** key.
   Connect a coaxial short with an APC 3.5 (f) connector to the semi-rigid cable.
   Press **Reflect Cal** key again.

3. Remove coaxial short from semi-rigid cable and connect a 50 Ω termination APC 3.5 (f) to semi-rigid cable.
   Press **Reflect Cal** key again.

4. Remove 50 Ω termination from semi-rigid cable and connect semi-rigid cable to channel 2.
   Press **Clear Display** key and wait for 16 averages to accumulate.

5. Press **Network** menu key.
   Press **Reflect/Trans/Cal** key until **Reflect** is highlighted.

6. Set normalized risetime to 30 ps.
   Press **Normalize to mem 1** key.

7. Press **Stop** key.
   Press **Clear Display** key.

8. Press **Cursor** key until **mem 1** is highlighted.

9. Press **Min & Max Reflect** key.
   The absolute value of Rho minimum and Rho maximum should be $< 5\%$.

10. Press **Run** key.

11. Loosen connection where semi-rigid S and U cables join together. Move semi-rigid cable from channel 2 to channel 3 and press **Clear Display** key. Retighten connection where semi-rigid S and U cables join together.

12. Repeat steps 6 through 10 for channel 3.

13. Loosen connection where semi-rigid S and U cables join together. Move semi-rigid from channel 3 to channel 4 and press **Clear Display** key. Retighten connection where semi-rigid S and U cables join together.

14. Repeat steps 6 through 10 for channel 4.

15. Loosen joint where semi-rigid S and U cables join together. Move semi-rigid cable from channel 4 to external trigger input and press **Clear Display** key. Retighten connection where semi-rigid S and U cables join together.

16. Repeat steps 6 through 10 for external trigger input except change normalize risetime from 30 ps to 100 ps and change the RHO limits from 5% to 10%.

17. Remove the semi-rigid S and U cables from the oscilloscope. Connect the precision short to channel 1's input APC 3.5 connector.

18. Select waveform save menu. Press **WAVEFORM MEMORY** key until 1 is highlighted. Press **Display key** until **On** is highlighted.

19. Change channel 1 offset to 0 V. Change sweep speed to 2 ns/div and delay to 35 ns.

20. Select Delta V menu and overlay both V markers on channel 1.

21. Press **MARKER 1 POSITION** and overlay this marker on the center of the trace.

22. Press **MARKER 2 POSITION** and overlay this marker on the highest portion of ringing which occurs near center screen and is greater than marker 1.

23. The delta V value should be < 10 mV, ($+5\%$).

24. Reposition marker 2 to the highest portion of ringing which occurs near center screen and is less than marker 1.

25. The absolute value of Delta V should be < 10 mV, ($+5\%$).

Table 3-1. Performance Test Record

Four Channel test Set HP 54121A	Tested by _____
HP 54120A/B Serial No. _____	Work Order No. _____
HP 54121A Serial No. _____	Date Tested _____
	Test Interval _____ months

Test		Results		
Low bandwidth 12.4 GHz			Actual	Maximum
	channel 1		_____	−2.99 dB
	channel 2		_____	−2.99 dB
	channel 3		_____	−2.99 dB
	channel 4		_____	−2.99 dB
High bandwidth 18 GHz	channel 1		_____	−2.99 dB
High bandwidth 20 GHz	channel 1		_____	−3.49 dB
	channel 2		_____	−2.99 dB
	channel 3		_____	−2.99 dB
	channel 4		_____	−2.99 dB
Channel 1 dc Accuracy Test		Minimum	Actual	Maximum
	12.4 GHz BW mode 0 V offset	−2.16 mV	_____	2.16 mV
	20 GHz BW mode 0 V offset	−2.16 mV	_____	2.16 mV
	+ Offset Gain 500 mV offset	496 mV	_____	504 mV
	− Offset Gain 500 mV offset	−504 mV	_____	−496 mV
	Delta V Offset Gain	992 mV	_____	1.0080 V
	+ Sampler Gain 250 mV offset	240.34 mV	_____	259.66 mV
	− Sampler Gain −250 mV offset	−259.66 mV	_____	−240.34 mV
	RMS noise 0 V offset 12.4 GHz		_____	1 mV
	* RMS noise 0 V offset 20 GHz		_____	2 mV
Channel 2 dc Accuracy Test				
	12.4 GHz BW mode 0 V offset	−2.16 mV	_____	2.16 mV
	20 GHz BW mode 0 V offset	−2.16 mV	_____	2.16 mV
	+ Offset Gain 500 mV offset	496 mV	_____	504 mV
	− Offset Gain 500 mV offset	−504 mV	_____	−496 mV
	Delta V Offset Gain	992 mV	_____	1.0080 V
	+ Sampler Gain 250 mV offset	240.34 mV	_____	259.66 mV
	− Sampler Gain −250 mV offset	−259.66 mV	_____	−240.34 mV
	RMS noise 0 V offset 12.4 GHz		_____	1 mV
	* RMS noise 0 V offset 20 GHz*		_____	2 mV

Table 3-1. Performance Test Record (continued)

Test			Results		
Channel 3 dc Accuracy Test			Minimum	Actual	Maximum
	12.4 GHz BW mode 0 V offset		−2.16 mV	_____	2.16 mV
	20 GHz BW mode 0 V offset		−2.16 mV	_____	2.16 mV
	+ Offset Gain 500 mV offset		496 mV	_____	504 mV
	− Offset Gain 500 mV offset		−504 mV	_____	−496 mV
	Delta V Offset Gain		992 mV	_____	1.0080 V
	+ Sampler Gain 250 mV offset		240.34 mV	_____	259.66 mV
	− Sampler Gain −250 mV offset		−259.66 mV	_____	−240.34 mV
	RMS noise 0 V offset 12.4 GHz			_____	1 mV
	* RMS noise 0 V offset 20 GHz			_____	2 mV
Channel 4 dc Accuracy Test					
	12.4 GHz BW mode 0 V offset		−2.16 mV	_____	2.16 mV
	20 GHz BW mode 0 V offset		−2.16 mV	_____	2.16 mV
	+ Offset Gain 500 mV offset		496 mV	_____	504 mV
	− Offset Gain 500 mV offset		−504 mV	_____	-496 mV
	Delta V Offset Gain		992 mV	_____	1.0080 V
	+ Sampler Gain 250 mV offset		240.34 mV	_____	259.66 mV
	− Sampler Gain −250 mV offset		−259.66 mV	_____	−240.34 mV
	RMS noise 0 V offset 12.4 GHz			_____	1 mV
	* RMS noise 0 V offset 20 GHz			_____	2 mV
* Does not apply to instruments with firmware datecode March 3, 1989 and earlier					
Short Delta T			Minimum	Actual	Maximum
	Delay Setting	16 ns	40.0 ps	_____	60.2 ps
		18 ns	40 ps	_____	60.2 ps
		19.9 ns	40 ps	_____	60.2 ps
		19.95 ns	40 ps	_____	60.2 ps
		23.95 ns	40 ps	_____	60.2 ps
		27.95 ns	40 ps	_____	60.2 ps
		55.95 ns	40 ps	_____	60.2 ps

Table 3-1. Performance Test Record (continued)

Test			Results		
Short Delta T (continued)			Minimum	Actual	Maximum
	Frequency	10 GHz	89.9 ps	_____	110.1 ps
		5 GHz	189.8 ps	_____	210.2 ps
		2 GHz	489.5 ps	_____	510.5 ps
		1 GHz	0.9890 ns	_____	1.011 ns
		500 MHz	1.988 ns	_____	2.012 ns
		200 MHz	4.985 ns	_____	5.015 ns
		100 MHz	9.980 ns	_____	10.02 ns
		50 MHz	19.97 ns	_____	20.03 ns
		20 MHz	49.95 ns	_____	50.06 ns
Long Delta T		10 MHz	99.89 ns	_____	100.11 ns
		5 MHz	199.79 ns	_____	200.21 ns
		2 MHz	499.49 ns	_____	500.51 ns
		1 MHz	.99899 µs	_____	1.00101 µs
		500 kHz	1.99799 µs	_____	2.00201 µs
		200 kHz	4.99499 µs	_____	5.00501 µs
		100 kHz	9.98999 µs	_____	10.01001 µs
		50 kHz	19.97999 µs	_____	20.02001 µs
		20 kHz	49.94999 µs	_____	50.05001 µs
		10 kHz	99.89999 µs	_____	100.10001 µs
Trigger Sensitivity Test			Minimum	Actual	Maximum
	Trigger Hysteresis	V_{pos}		_____	
		V_{neg}		_____	
		V_{hyst}		_____	40 mV
	100 MHz Trigger Sens.	V_{pos}		_____	
		V_{neg}		_____	
		$V_{sens.}$		_____	40 mV
(2.5 GHz trigger only)	HF Reject On	V_{pos}		_____	
		V_{neg}		_____	
		$V_{sens.}$	57 mV	_____	
	2.5 GHz Trigger Sens.	V_{pos}		_____	
		V_{neg}		_____	
		$V_{sens.}$		_____	200 mV

Table 3-1. Performance Test Record (continued)

Test			Results		
(Trigger Sensitivity Test Continued)					
	500 MHz Trigger Sens.	V_{pos}		_____	
	(500 MHz Trigger only)	V_{neg}		_____	
		$V_{sens.}$			100 mV
Jitter Test			Minimum	Actual	Maximum
	2.5 GHz Trigger (only)			_____	See Specs.
		Example	< 3.525 ps with 20.5 ns delay setting		
	500 MHz Trigger (only)			_____	See Specs.
		Example	< 5.8 ps with 20.5 ns delay setting		
TDR System Test			Minimum	Actual	Maximum
		Low level	−2 mV	_____	2 mV
		High level	198 mV	_____	202 mV
	Flattness > 1 ns	+1%		_____	+1%
		−1%	−1%	_____	
	< 1 ns	−2%	−2%	_____	
		+5%		_____	+5%
	Risetime			_____	45 ps
Input Reflection Test				Actual	Maximum
	Channel 2	pos		_____	5%
		neg		_____	5%
	Channel 3	pos		_____	5%
		neg		_____	5%
	Channel 4	pos		_____	5%
		neg		_____	5%
	External Trigger	pos		_____	10%
		neg		_____	10%
	Channel 1	pos		_____	5%
		neg		_____	5%

Table Of Contents

Adjustments

Adjustments 4

Introduction

This section describes the adjustments for returning the instrument to peak operating capabilities after repairs have been made, during routine preventive maintenance, or after performance test have been done (refer to section 3, performance test cycle paragraph).

Warning 

Read the "Safety Summary" at the front of this manual before performing adjustment procedures. The instrument should be disconnected from all voltage sources before it is opened for any adjustments, replacements, maintenance, or repairs.

Caution 

The four channel test set is very sensitive to static discharge. Failure to observe proper antistatic procedures may result in damage to the gallium arsenide samplers. Perform all maintenance or operation while using the antistatic mat and wrist strap supplied with the instrument.

Recommended Test Equipment

Table 1-1 lists the recommended test equipment to use for the adjustment procedures. Any equipment that satisfies the critical specifications may be used.

Adjustment Sequence

The following list is the factory recommended sequence of adjustments. The mainframe adjustments must be performed before the test set adjustments.

- Range
- Step Recovery Diode (SRD) Adjustments
- Frequency and TB Fine Tune Adjustments
- END and 4 ns CAL Adjustments
- Sampler Bias Adjustments
- Vertical Soft Cal
- Offset Gain Adjustments
- TDR Step Adjustments
- Feedthrough Compensation Adjustments
- Trigger Hysteresis and Offset Null Adjustments
- Channel Skew Calibration

Special Procedures

1. All connectors should be clean and undamaged to ensure accurate measurements. Check all test set APC 3.5 (f-f) connectors mechanically and visually before inserting any calibration test tool in them. Damaged connectors or loose connections may cause unreliable adjustment results. Refer to Appendix A in the mainframe manual.

2. The instruments should be allowed to warm up for at least 15 minutes.

3. To avoid damage to the HP 54121A Four Channel Test Set connectors, use of the APC 3.5 (f-f) connector savers is encouraged. These connector savers are supplied with the HP 54121A. Refer to Appendix A in the HP 54120B Mainframe manual for information on mating APC 3.5 connectors to SMA connectors.

4. Avoid sharp bends in the two 17-inch coaxial cables, HP part numbers 8120-4941 and 8120-4942.

5. When mating APC 3.5 connectors to APC 3.5 connectors or devices, torque all connections to 8 in/lbs. When mating APC 3.5 to SMA or SMA to SMA, torque all connections to 5 in/lbs.

6. Do as little connector swapping as possible during the procedures. APC 3.5 and SMA connectors wear out with repeated use. All test tool connectors should be inspected both visually and mechanically every few calibrations.

7. The adjustment procedures outlined in this section make use of extra connectors. These are used to save expensive parts from repeated excessive wear caused by many reconnections. These parts are required, but their use is highly advised. They will not interfere with measurement capabilities.

8. Throughout the procedure identical connectors are used in different ways. One way is precision at both ends. This means that both ends of the APC 3.5 connector should be precise and should never be connected to an SMA connector. The other way is precise at one end. This means that one of the APC 3.5 ends may be used with SMA connectors, but the other end should never be connected to any SMA connectors. Unless otherwise stated, all APC 3.5 calibration test connectors should never be connected to SMA connectors.

Caution

Electrostatic discharge can seriously damage the test set's inputs. Use the antistatic mat and wrist strap supplied with the mainframe. To eliminate any electrostatic build up from a cable you're connecting to the test set, connect a female short to either end of the cable. Touch the short to an input connector hex nut on the test set to discharge any electrostatic build up to ground. Remove the female short. Use this procedure for all cable before connecting them to the test set.

Range Adjustment

This adjustment matches the linear input range of the timebase hybrid to the linear output range of operational amplifier U8 on the Horizontal assembly. Anytime this adjustment is performed, you must also do the frequency, end and 4 ns cal adjustments in the test set manual. If this adjustment fails, perform the timebase delta current adjustment in the mainframe manual.

Equipment

This is a list of the recommended test equipment for this adjustment. However, any instrument which satisfies the critical specifications may be used.

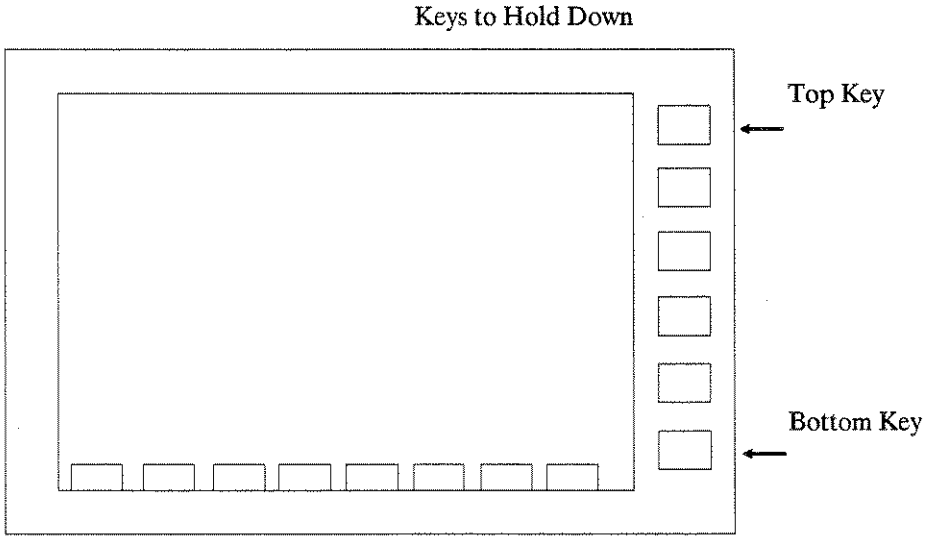
Instrument	Critical Specifications	Model
DMM	Better than 0.3% accuracy	HP 3478A

Procedure

The adjustment locations are shown on page 4-30.

1. Remove top and bottom covers from four channel test set.

2. Perform two key-down power up. This must be performed to ensure the value on TP1 is correct, otherwise the adjustment may drift on the next trigger event. Turn oscilloscope's power switch to STBY. Hold down top and bottom function keys immediately to right of screen. Turn oscilloscope's power switch to ON. Continue holding function keys until graticule display is on screen. Ignore "Front Panel Cals Lost" warnings on top of screen; CALs will be performed later.



3. Change timebase delay to 18 ns, and sweep to Trg'd mode.

4. Connect positive DMM lead to Horizontal Board (A1) TP1. The horizontal assembly is on the test set's bottom side. Connect negative DMM lead to chassis ground near TP1.

5. Adjust RANGE (R52) for a reading of +5 V ±1 V on DMM.

Step Recovery Diode (SRD) Adjustments

The sampler hybrids for each channel contain step recovery diodes. The bias on these diodes is adjusted for optimum performance. SRD BIAS adjusts the bias of the step recovery diode for a zero temperature coefficient. SRD DRIVE adjusts the output level of the sample pulse generator. SRD DRIVE affects the bandwidth of all four channels simultaneously. Anytime this adjustment is performed, SBIAS and offset gain must also be performed. If this adjustment fails, perform the 10 V reference adjustment in the mainframe manual.

Note 

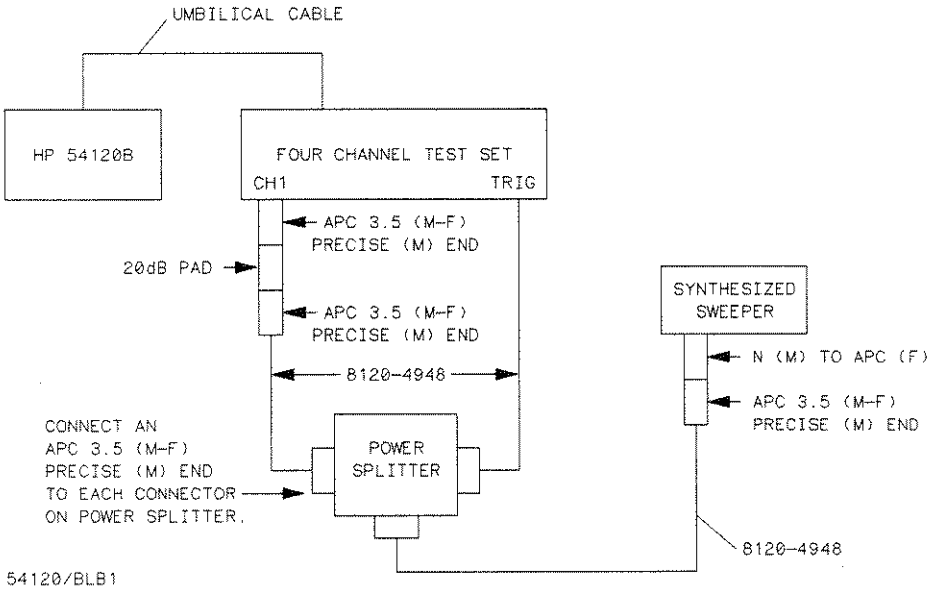
If this adjustment is performed out of the factory recommended adjustment sequence, a two key-down power up must be performed first.

Equipment

This is a list of the recommended test equipment for this adjustment. However, any instrument which satisfies the critical specifications may be used.

Instrument	**Critical Specifications**	**Model**
Synthesized sweeper	20 GHz + 12 dBm	HP 8341B/003
Power splitter	APC 3.5 connectors	HP 11667B
20 dB pad	APC 3.5 connectors	HP 33340C/020
Accessories	**Critical Specifications**	**HP Part Number**
Adapter	APC 3.5 (m-f) male end precise, 26.5 GHz Quantity needed - 6	1250-1866
Adapter	N (m) to APC 3.5 (f)	1250-1744
Coaxial cable	APC 3.5 (m-m), 18 GHz, Quantity needed - 3	8120-4948

Equipment Connections



Equipment Setup

Signal Source

Frequency	250 MHz
Amplitude	+12 dBm

HP 54120B

Display		**Timebase**	
Display Mode	Averaged	Time/Div	500 ps/div
No. of Averages	4	Delay	16 ns
Screen	Single	Delay Ref. at	Left
Graticule	Grid	Sweep	Trg'd
Bandwidth	12.4 GHz		
Channels		**Trigger**	
Channel 1	On	Trigger Level	0 V
Volts/Div	20 mV/div	Slope	Pos
Offset	Center signal	Attenuation	1
Channels 2-4	Off	HF Sens.	Off
Attenuation	1.0	HF Reject	Off

Procedure The adjustment locations are shown on page 4-30.

Note It is mandatory that step 1 in this procedure be performed, otherwise the SBIAS adjustment performed later in this procedure will fail.

1. Preset LB1 (R153) and OG1 (R113) on Vertical assembly (A2) to mechanical center. The Vertical assembly is on top side of four channel test set.
2. Readjust channel offset to recenter signal on screen.
3. Press **Delta V** key.
4. Turn V Markers on and overlay them on channel 1.
5. Press **Preset Levels** until **Preset Levels 0–100%** is highlighted.
6. Use oscilloscope's offset to center signal.
7. Press **Auto Level Set** key.
8. Press **Display Mode** key.
9. Set Display Mode to a persistence of 300 ms.
10. Preset SRD BIAS (R168) on Horizontal assembly (A1) to mechanical center.
11. Adjust SRD DRIVE (R167) (A1) for a signal amplitude of 0% and +100% on screen.

Note An offset may exist in the signal during this portion of the adjustments. If the signal peaks do not overlay the 0% and 100% markers, adjust SRD DRIVE for equal amounts of signal above or below the markers in the following steps. The offset level may be adjusted any time during this procedure.

12. Slowly adjust SRD BIAS (R168) for maximum signal amplitude. The waveform will compress and slightly increase in amplitude, R168 must be adjusted slowly to see the slight amplitude increase.
13. Readjust steps 11 and 12 until maximum signal amplitude is 0% and +100%.
14. Turn V Markers Off.

Frequency Adjustments

This adjusts the 250 MHz timebase oscillator inside the timebase hybrid. A trimmer cap (FREQ) on the timebase hybrid is a coarse adjustment, and TB FINE TUNE (A1R54) is a fine adjustment. Anytime this adjustment is performed, the END and 4 ns cal adjustments must also be performed. If this adjustment fails, perform the timebase delta current adjustment in the mainframe manual and the range adjustment in this manual.

Equipment & Connections

Refer to step recovery diode adjustment. There is a coarse frequency adjustment on the timebase hybrid (FREQ). This coarse adjustment normally only needs adjusted if the timebase hybrid has been replaced. Normally the TB FINE TUNE adjustment should have enough range to compensate for slight variances in the coarse adjustment. If the coarse adjustment needs to be performed, a non-metallic tool with a blade 0.010 inches thick and 0.040 inches wide is used. HP part number 8710-1300 adjustment tool filed down to fit the adjustment size is adequate.

Equipment Setup

Signal Source

Frequency	250 MHz
Amplitude	+12 dBm

HP 54120B

Display		**Timebase**	
Display Mode	Averaged	Time/Div	500 ps/div
No. of Averages	4	Delay	16 ns
Screen	Single	Delay Ref at	Left
Graticule	Grid	Sweep	Trg'd
Bandwidth	12.4 GHz		
Channels		**Trigger**	
Channel 1	On	Trigger Level	0 V
Volts/Div	20 mV/div	Slope	Pos
Offset	0 V	Attenuation	1
Channels 2-4	Off	HF Sens.	Off
Attenuation	1	HF Reject	Off

Procedure

The adjustment locations are shown on page 4-30.

Note

For best results with this procedure, perform all adjustments with the test set in a normal operating position.

1. Adjust oscilloscope's offset to center signal vertically.
2. Adjust oscilloscope's trigger level until trace's positive or negative slope begins near center horizontal graticule on the screen's left side and remains triggered.
3. Press **Measure** key, then **Frequency** key.
   If the results are 250 MHz ± 250 kHz, go to step 6. Otherwise go to step 4.
4. Remove tape from FREQ (frequency) adjustment (trimmer capacitor on U9) on horizontal assembly.
5. Remeasure the frequency while making small incremental adjustments to the FREQ adjustment capacitor on the timebase hybrid with a 40/1000 inch non-metallic alignment tool. After the frequency measures 250 MHz ± 250 kHz, proceed with step 6.
6. Change timebase time/div to 200 ns/div.
7. Observe a nearly flat horizontal trace on screen. If the trace is horizontally flat ± 1 major division go to step 12. Otherwise, go to step 8.
8. Preset TB FINE TUNE (R54) on Horizontal assembly to mechanical center.
9. Adjust FREQ adjustment on timebase hybrid until the trace is flat ± 1 major division.
10. Replace tape over FREQ. adjustment on U9. Masking tape or electrical tape may be used if the original tape is misplaced or damaged. The tape is needed to prevent air currents from upsetting the thermal stability of the timebase hybrid.
11. Allow 10 minutes for U9 to stabilize its temperature, with tape over Freq. adjustment hole.
12. Change timebase time/div to 1 μs/div.
13. Adjust TB FINE TUNE (R54) for flattest trace possible on screen.

END and 4 ns CAL Adjustments

The timebase hybrid operates at 250 MHz which is a 4 ns period. END adjusts the timebase ramp's ending point to the next timebase ramp's beginning point. The 4 ns CAL adjusts the discontinuity which occurs at 4 ns intervals after 16 ns. The END adjustment must be performed before the 4 ns CAL adjustment. If this adjustment fails, perform the timebase delta current adjustment in the mainframe manual, the range adjustment, and the frequency adjustments in this manual.

Equipment & Connections

Refer to Step Recovery Diode Adjustments.

Equipment Setup

Signal Source

Frequency	250 MHz
Amplitude	+12 dBm

HP 54120T

Display		**Timebase**	
Display Mode	Averaged	Time/Div	500 ps/div
No. of Averages	4	Delay	16 ns
Screen	Single	Delay Ref. at	Left
Graticule	Grid	Sweep	Trg'd
Bandwidth	12.4 GHz		
Channels		**Trigger**	
Channel 1	On	Trigger Level	0 V
Volts/Div	20 mV/div	Slope	Pos
Offset	Center signal	Attenuation	1
Channels 2-4	Off	HF Sens.	Off
Attenuation	1.0	HF Reject	Off

Procedure

The adjustment locations are shown on page 4-30.

1. Preset 4 ns CAL (R62) on Horizontal assembly (A1) to fully counterclockwise.

2. Adjust END (R61) for a small amount of trace discontinuity at beginning of eighth vertical graticule division. Refer to figure 4-1. If necessary, adjust oscilloscope's trigger level to center trace discontinuity vertically on screen.

3. Change timebase time/div to 10 ps/div and delay to 59.95 ns.

4. Change volts/div to 2 mV/div.

5. If necessary, adjust oscilloscope's trigger level in order to center trace discontinuity vertically on screen. Refer to figure 4-2.

6. Readjust END (R61) to eliminate trace discontinuity. Refer to figure 4-3.

7. Change timebase delay to 19.95 ns.

8. Adjust 4 ns cal (R62) on Horizontal assembly from counterclockwise limit to first null point (minimum trace discontinuity). Adjusting to the second null point may cause timebase errors..

9. Change timebase delay to 59.95 ns. If necessary repeat steps 6 through 8 until discontinuity at both 19.95 ns and 59.95 ns is minimized.

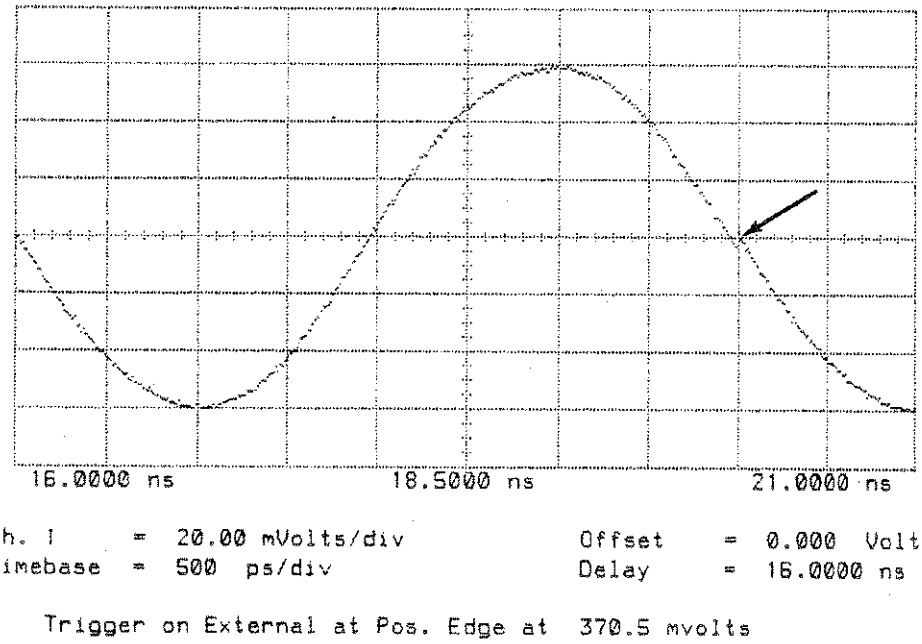


Figure 4-1. Trace Discontinuity at Eighth Graticule

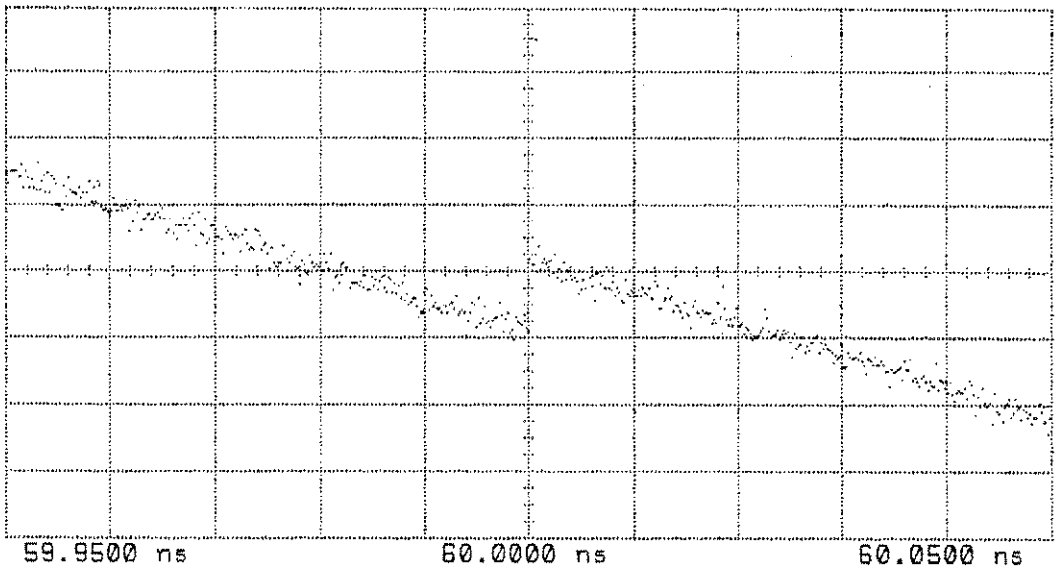


Figure 4-2. Expanded Trace Discontinuity

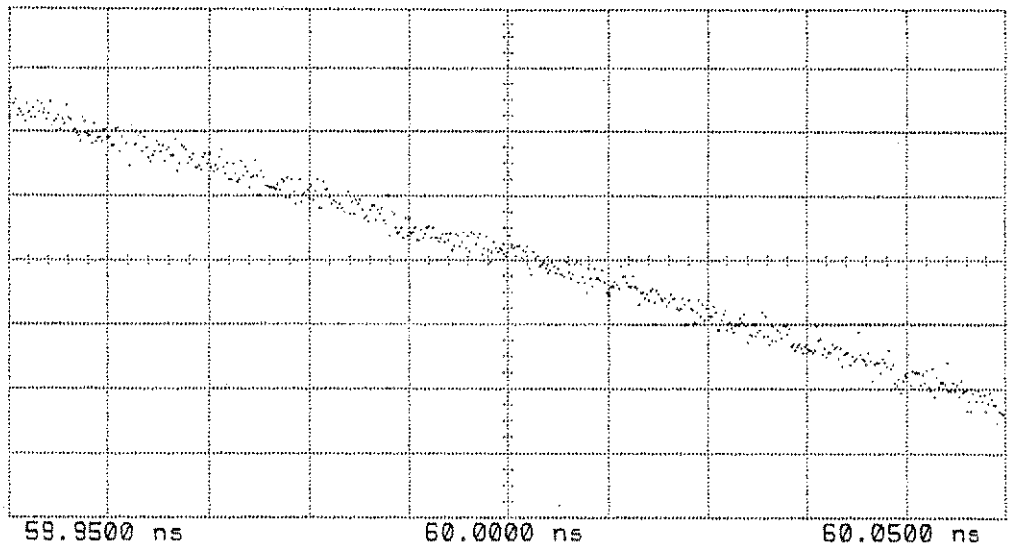


Figure 4-3. Correct End Adjustment, No Discontinuity

Sampler Bias Adjustments

This procedure adjusts the bandwidth of individual channels for low bandwidth (12.4 GHz) and for high bandwidth (20 GHz). If this adjustment fails, perform the 10 V reference adjustment in the mainframe manual, and the SRD bias adjustments in this manual.

Equipment & Connections

Refer to step recovery diode adjustments.

Note

If this adjustment is performed out of the normal adjustment sequence, a two key-down powerup must be performed first.

Equipment Setup

Signal Source

Frequency	250 MHz
Amplitude	+12 dBm

HP 54120B

Display		**Timebase**	
Display Mode	Averaged	Time/Div	1 ns/div
No. of Averages	4	Delay	16 ns
Screen	Single	Delay Ref. at	Left
Graticule	Grid	Sweep	Trg'd
Bandwidth	12.4 GHz		
Channels		**Trigger**	
Channel 1	On	Trigger Level	0 V
Volts/Div	20 mV/div (on all 4 channels)	Slope	Pos
		Attenuation	1
Offset	Center signal	HF Sens.	Off
Channels 2-4	Off	HF Reject	Off
Attenuation	1.0		

Procedure

The adjustment locations are shown on page 4-30.

1. Press **Delta V** key.
2. Turn V Markers on and overlay them on channel 1.
3. Press **Preset Levels** until **0-100%** is highlighted.
4. Press **Auto Level Set** key.
5. Change Display Mode to 300 ms persistence.
6. Adjust LB1 (R153) on Vertical assembly (A2) for a signal amplitude of 0 to 100%. Adjustment LB1 is Low Bandwidth for channel 1 only. Refer to figure 4-4. If the signal does not line up with the markers, adjust for equal amounts above or below the markers.

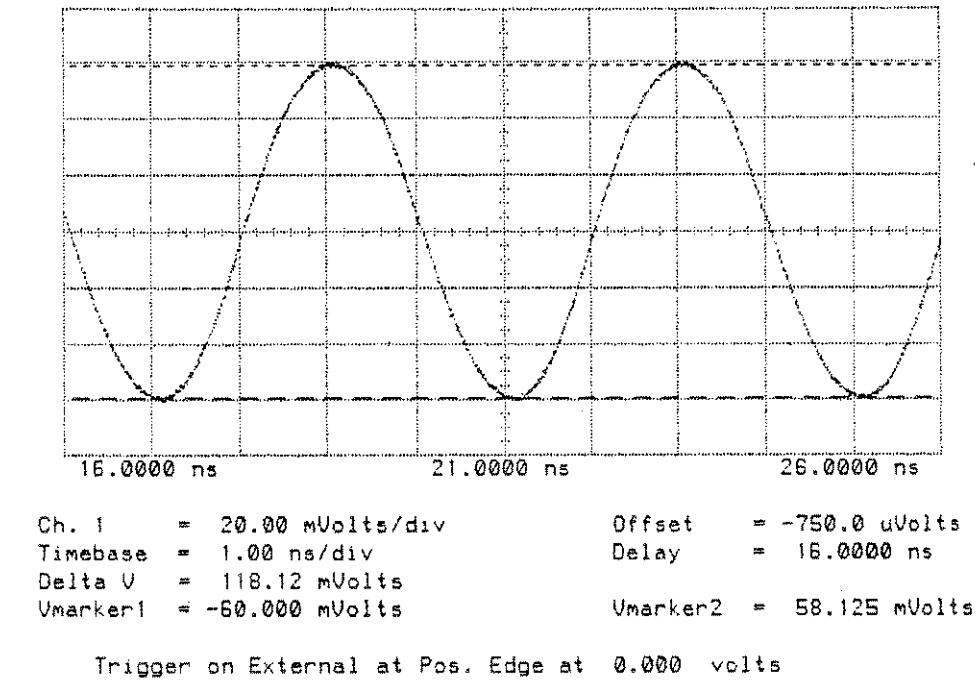


Figure 4-4. Low Bandwidth Adjustment with Markers

7. Change Display Mode to Averaged and bandwidth to 20 GHz

8. Press **Delta V** key.

9. Press **Preset Levels** key until **variable** is highlighted.

10. Press **Variable** key and set levels to 30%-70%.

11. Press **Auto Level Set** key.

12. While in the persistence bandwidth mode, toggle the bandwidth key. If your instrument toggles between 12.4 GHz and 20 GHz perform step 13A; otherwise perform step 13B.

13A. Change display mode to 300 ms persistence, bandwidth to 20 GHz.

13B. Change display to average and bandwidth to 20 GHz. Press **Clear Display** key and notice that trace on screen temporarily decreases in size. Continue to press **Clear Display** key (about 2 times a second) while making small adjustment increments in step 14.

14. Adjust HB1 (R161) until signal amplitude overlays the 30% and 70% markers. Refer to figure 4-5. Adjustment HB1 is High Bandwidth adjustment for channel 1 only.

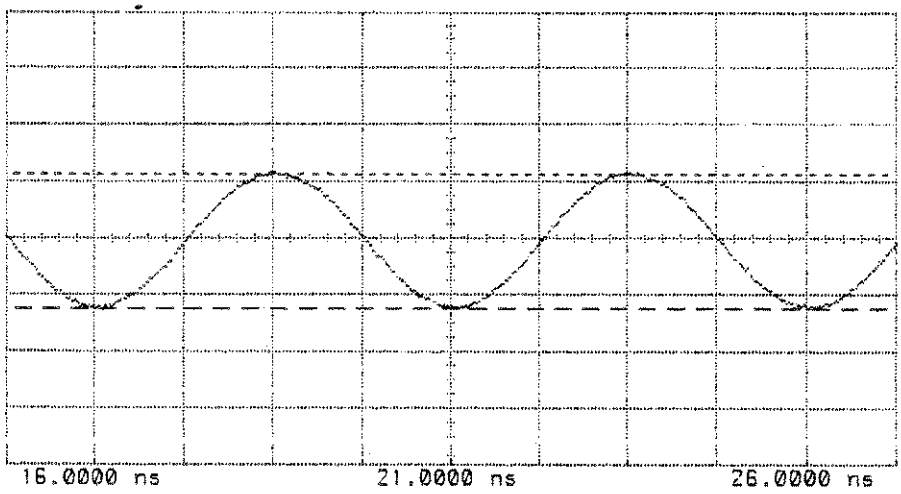


Figure 4-5. High Bandwidth Adjustment with Markers

15. Turn channel 1 display off and channel 2 display on. Change Bandwidth to 12.4 GHz and display mode to averaged.

16. Move input signal from channel 1 to channel 2.

17. Repeat steps 1-14 for channel 2 except use adjustments LB2 (R154) and HB2 (R162).

18. Turn channel 2 display off and channel 3 display on. Change Bandwidth to 12.4 GHz and display mode to averaged.

19. Move input signal from channel 2 to channel 3.

20. Repeat steps 1-14 for channel 3 except use adjustments LB3 (R155) and HB3 (R163).

21. Turn channel 3 display off and channel 4 display on. Change Bandwidth to 12.4 GHz and display mode to averaged.

22. Move input signal from channel 3 to channel 4.

23. Repeat steps 1-14 for channel 4 except use adjustments LB4 (R156) and HB4 (R164).

24. Turn Delta V Markers Off.

25. Press **Utility** key.

26. Press **Cal Menu** key.

27. Press **Vertical Cal** key and follow instructions on screen.

Offset Gain Adjustments

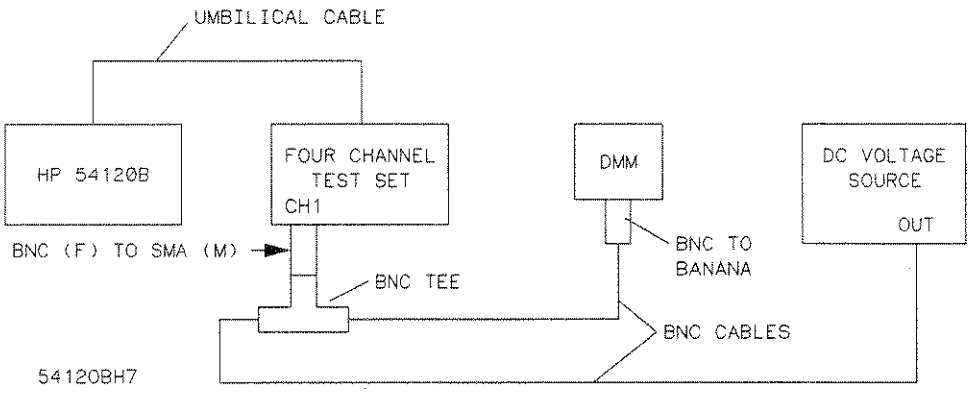
With the oscilloscope set to the same offset value as a dc voltage source, the OFFSET GAIN for each channel is adjusted until the trace overlays center screen.

Equipment

This is a list of the recommended test equipment for this adjustment. However, any instrument which satisfies the critical specifications may be used.

Instrument	Critical Specifications	Model
voltage source	1 mV resolution, less than 100 μV ripple	HP 3325A/001
DMM	10 mV accuracy	HP 3478A
Accessories	**Critical Specifications**	**HP Part Number**
Adapter	BNC (f) to SMA (m) (Adapt dc voltage source to APC 3.5)	1250-1200
Adapter	BNC to banana	1250-2277
BNC Tee	1 (m) end and 2 (f) ends	1250-0781
BNC cables	Quantity needed - 2	10503A

Equipment Connections



Equipment Setup

HP 54120T

Display		**Timebase**	
Display Mode	Averaged	Time/Div	1 μs/div
No. of Averages	8	Delay	200 ns
Screen	Single	Delay Ref. at	Left
Graticule	Grid	Sweep	Freerun
Bandwidth	12.4 GHz	Freerun Rate	10 KHz
Channels		**Network**	
Channel 1	On	Reflect/Trans/Cal	Reflect
Volts/Div	1 mV/div	Step& Chan 1	Off
Offset	0 V		
Channels 2-4	Off		
Attenuation	1.0		

Procedure The adjustment locations are shown on page 4-30.

Caution Exceeding 2 V on the dc power supply may damage the oscilloscope's input.

1. Disconnect all input signals from oscilloscope and perform a vertical CAL routine.
   Press **Utility** menu key, **Cal Menu** key, **Channel Vertical Cal** key, and follow the screen's instructions.

2. Set dc voltage source for approximately 490 mV.

3. Connect input signals to HP 54121A channel 1.

4. Read dc voltage source's output on DMM to 100 μV accuracy.

5. Change oscilloscope's offset to within 100 μV of reading obtained on DMM.

6. Adjust OG1 (R113) on Vertical assembly (A2) until trace is on center graticule.
   adjustment OG1 is Offset Gain adjustment for channel 1 only.
   Adjust OG1 slowly in small increments, and wait for averages to accumulate.

7. Turn channel 1 off and channel 2 on, then move signal to channel 2's input.

8. Repeat steps 4-6 for channel 2 except adjust OG2 (R114).

9. Turn channel 2 off and channel 3 on, then move signal to channel 3's input.

10. Repeat steps 4-6 for channel 3 except adjust OG3 (R115).

11. Turn channel 3 off and channel 4 on, then move signal to channel 4's input.

12. Repeat steps 4-6 for channel 4 except adjust OG4 (R116).

13. Press **Utility** key.

14. Press **Cal Menu** key.

15. Press **Vertical Cal** key and follow instructions on screen.

TDR Step Adjustments

This procedure adjusts the TDR pulse for a risetime of approximately 45 ps, an overshoot between 2.5% and 3.5% in the average mode, and a flat pulse top.

The final value in this procedure is adjusted so that when a 50.0 Ω termination is connected to channel 1, the final value will measure 200 mV. The first part of this procedure measures the actual dc resistance of the 50 Ω termination you are using. A compensation value is than added to 200 mV so you are performing the adjustment to the actual dc resistance of your 50 Ω termination.

Equipment

This is a list of the recommended test equipment for this adjustment. However, any instrument which satisfies the critical specifications may be used.

Instrument	Critical Specifications	Model
Termination	APC 3.5 (f), 50 Ω	HP 909D/011
DMM	5 1/2 digits	HP 3478A
Accessories	**Critical Specifications**	**HP Part Number**
Adapter	BNC (m-m)	1250-0216
Adapter	BNC (f) to banana	1250-2277
Adapter	BNC (f) to SMA (m)	1250-1200
Adapter	APC 3.5 (m-f)	1250-1866
Coaxial short	APC 3.5 (f)	1250-2127

Equipment Setup

HP 54120B

Display		**Timebase**	
Display Mode	Averaged	Time/Div	200 ps/div
No. of Averages	16	Delay	16 ns
Screen	Single	Delay Ref at	Left
Graticule	Frame	Sweep	Freerun
Bandwidth	12.4 GHz	Freerun Rate	10 KHz
Channels		**Network**	
Channel 1	On	Reflect/Trans/CAL	Reflect
Volts/Div	30 mV/div	Step & Chan 1	On
Offset	100 mV		
Channels 2-4	Off		
Attenuation	1		

Note Repeatedly pressing the Clear Display key will help in performing the adjustments.

Procedure The adjustment locations are shown on page 4-30.

1. Assemble a fixture by connecting a banana to BNC (f) adapter to a BNC (m-m) adapter. Connect this to a BNC (f) to SMA (m) adapter. Connect this to an APC 3.5 (m-f) adapter (male end precise). Connect fixture to DMM . Connect an APC 3.5 (f) precise 50 Ω termination to fixture.
   Record dc resistance of 50 Ω termination here _____Ω Example 50.390 Ω

2. Remove 50 Ω termination and connect the APC 3.5 (f) short to fixture.
   Record dc resistance of fixture here _____ Ω Example 0.050 Ω

3. Subtract fixture's resistance (step 2) from termination resistance (step 1).
   Step 1 _____Ω − Step 2 _____Ω = Z_L _____Ω Example 50.340 Ω

4. Solve for E_R using this formula (E_R may be a negative number).
   $E_R = 200 ((Z_L - 50) \div (Z_L + 50))$ (round to nearest 0.01 mV)
   Example 0.68 mV

5. Add 200 mV to the value obtained in step 4 and round to the nearest 0.01 mV.
   E_R (step 4) _____ + 200 mV = _____ mV Example 200.68 mV

6. Connect the APC 3.5 precise (f) 50 Ω termination to channel 1.

7. Adjust timebase delay until rising edge is approximately two divisions from left side of screen. Refer to figure 4-6.

8. Preset TDR DRIVE (R44) on Horizontal assembly (A1) fully clockwise. Reposition the delay setting to place the edge two divisions from the screen's left side.

9. Preset TDR BIAS (R45) fully counterclockwise, then slowly adjust TDR BIAS clockwise until pulse overshoot just starts to appear (first overshoot). Refer figure 4-6. If the overshoot is already on screen with TDR BIAS fully counterclockwise, turn TDR DRIVE slightly counterclockwise until overshoot disappears. Then increase TDR BIAS clockwise until overshoot reappears.

10. Press **Delta T** key and turn markers on.

11. Set Start Marker to step's leading edge and set Stop Marker 500 ps to right of Start Marker. Refer to figure 4-6.

12. Adjust TDR BIAS until step's rising edge coincides with Stop Marker. Refer to figure 4-7. If this adjustment does not line up with the Stop Marker, return to step 9 and turn TDR DRIVE slightly more counterclockwise.

13. Adjust TDR DRIVE so pulse overshoot is between 2.5 to 3.5%, use the Measure menu to check your adjustment. If the TDR DRIVE adjustment moves the edge off screen, reposition the edge with more delay in the timebase menu.

14. Select Delta V menu and press **Preset Levels** key until **50-50%**is highlighted. Press **Auto Level Set** key.

15. Select Delta T menu and press **START ON EDGE** key until **POS 1** is highlighted.
Press **STOP ON EDGE** key until **POS 1** is highlighted.
Press **Precise Edge Find** key.

16. Turn channel 1 off, than turn channel 1 back on again.
Change Channel 1 sensitivity to 2 mV/div and offset to 0 V.

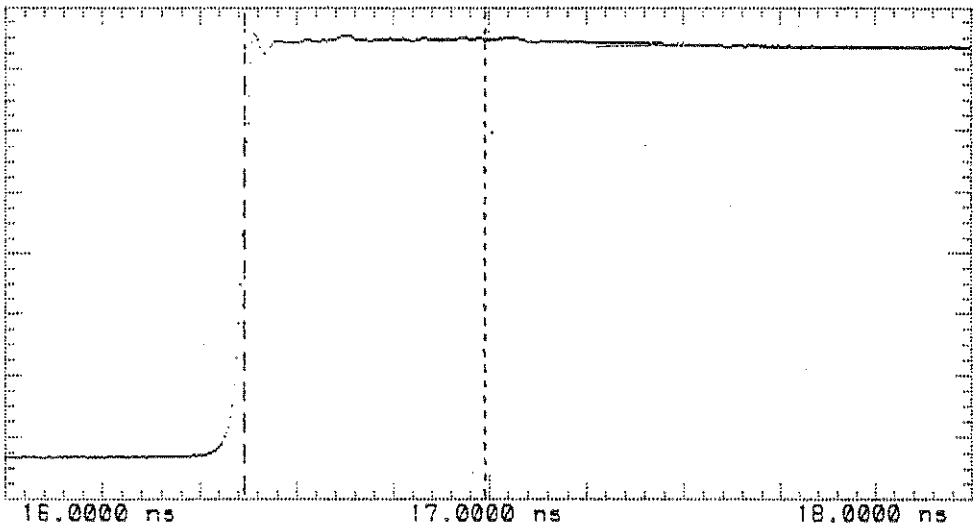


Figure 4-6. Setting Start and Stop Markers on Pulse

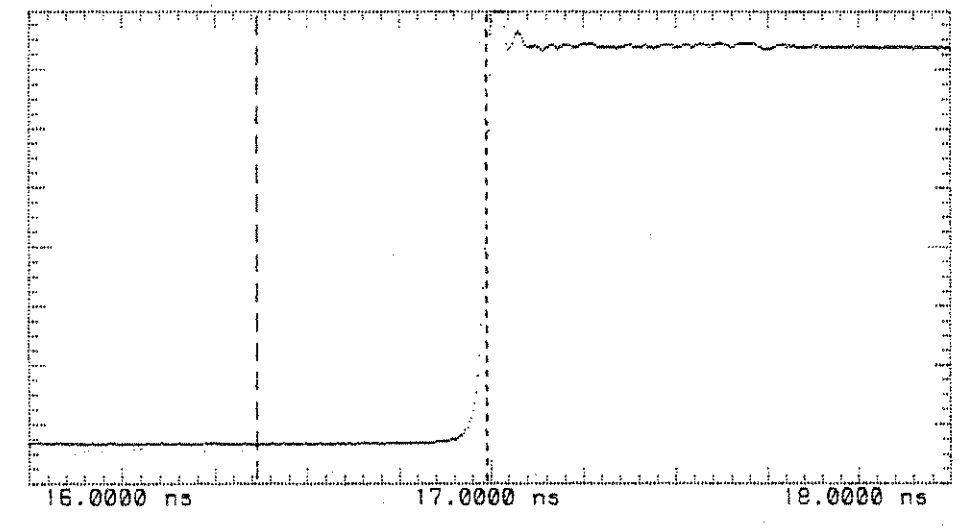


Figure 4-7. Adjusting TDR Pulse to Stop Marker

17. Select Delta V menu and press **Preset Level** key until **50-50%** is highlighted. Press **Auto Level Set** key. If V(1) is > 0.5 mV, perform a vertical cal. Change marker 2's value to 200 mV. Adjust front panel RPG control until Delta V equals the value recorded in step 5 from previous page (marker resolution limits this to within 0.06 mV at this sensitivity).

18. Select Network menu and press **Reflect/Trans/Cal** key until **Reflect** is highlighted. Press **Step & Chan 1** key until **On** is highlighted.

19. Select Delta T menu and change Stop marker's value to Start marker's value plus 1 ns.

20. Change timebase sweep speed to 100 ns/div, delay to Stop marker's value, and channel 1 offset to 200 mV.

21. Select Delta V menu and ensure that marker 2's position is highlighted.

22. Adjust TOP (R169) on Horizontal Assembly (A1) until trace on right edge of screen coincides with marker 2's position. Refer to figure 4-8.

23. Change timebase sweep speed to 50 ps/div, delay to 16 ns, and channel 1 offset to 0 V.

24. Select Delta V menu and ensure marker 1's position is highlighted.

25. Adjust BOTTOM (R170) on Horizontal Assembly (A1) until trace coincides with marker 1's position.

26. Change timebase delay to Start marker's value, and channel 1 offset to 200 mV.

27. Select Delta V menu. Change marker 1's value equal to the value obtained in step 5 on the previous page.
    Press **MARKER 2** key until that cursor is highlighted.
    Adjust front panel RPG control for a Delta V reading of between 5 to 7 mV (this will correspond to an overshoot of about 2.5 to 3.5%).

28. Slowly adjust TDR DRIVE (R44) on Horizontal Assembly (A1) until the peak of the overshoot coincides with marker 2's position. Refer to figure 4-9.
    If the overshoot moves off screen, reposition the waveform with delay.
    If this adjustment fails, repeat the TOP and BOTTOM adjustments.

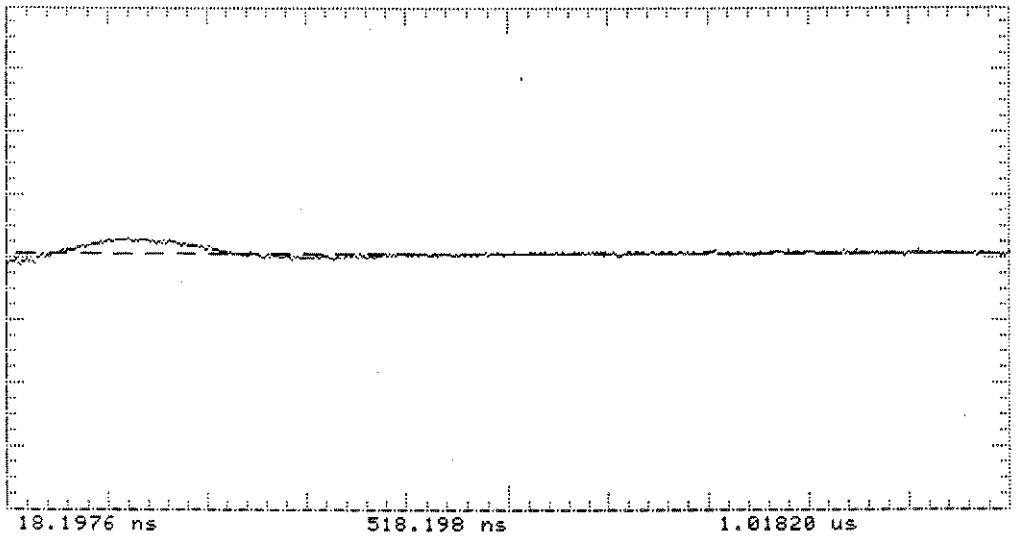


Figure 4-8. TOP Adjustment

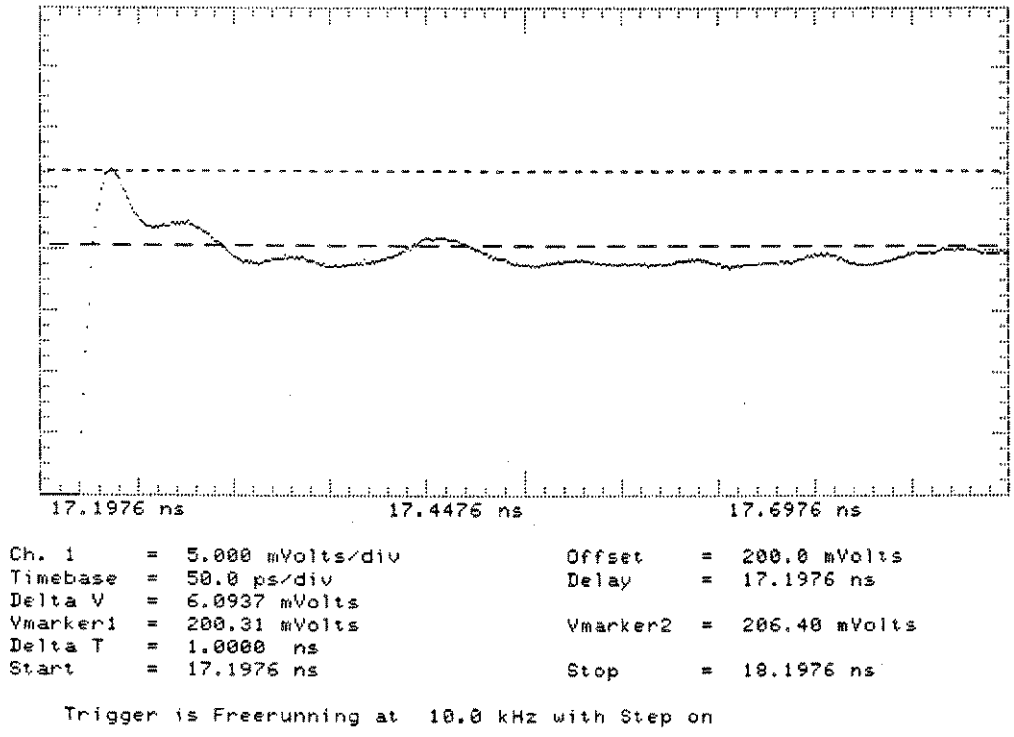


Figure 4-9. Overshoot Fine Adjustment

Feedthrough Compensation Adjustments

When the sampler's are turned off, there is a small amount of parasitic (unwanted) feedthrough of signals or noise through the samplers. This is caused by parasitic capacitive and resistive coupling near the samplers. This procedures nulls passive feedthrough of the input signal through the samplers.

Equipment

This is a list of the recommended test equipment for this adjustment. However, any instrument which satisfies the critical specifications may be used.

Accessories	Critical Specifications	HP Part Number
U cable	Semi-rigid	54121-61601
S cable	Semi-rigid	54121-61602

Equipment Setup

HP 54120B

Display		**Timebase**	
Display Mode	Persistence	Time/Div	20 μs/div
Display Time	500 ms	Delay	16 ns
Screen	Single	Delay Ref at	Left
Graticule	Grid	Sweep	Freerun
Bandwidth	12.4 GHz	Freerun Rate	3 KHz
Channels		**Network**	
Channel 1	On	Reflect/Trans/CAL	Reflect
Volts/Div	10 mV/div	Step & Chan 1	On
Offset	200 mV		
Channels 2-4	Off		
Attenuation	1		

Procedure

The adjustment locations are shown on page 4-30.

1. Connect the semi-rigid S and U cables from channel 1 to channel 2.
2. Preset eight adjustments on Vertical assembly (A2), RC1-4 (R5-8) and CC1-4 (R9-12) fully counter-clockwise.
3. Signal on screen should resemble figure 4-10.

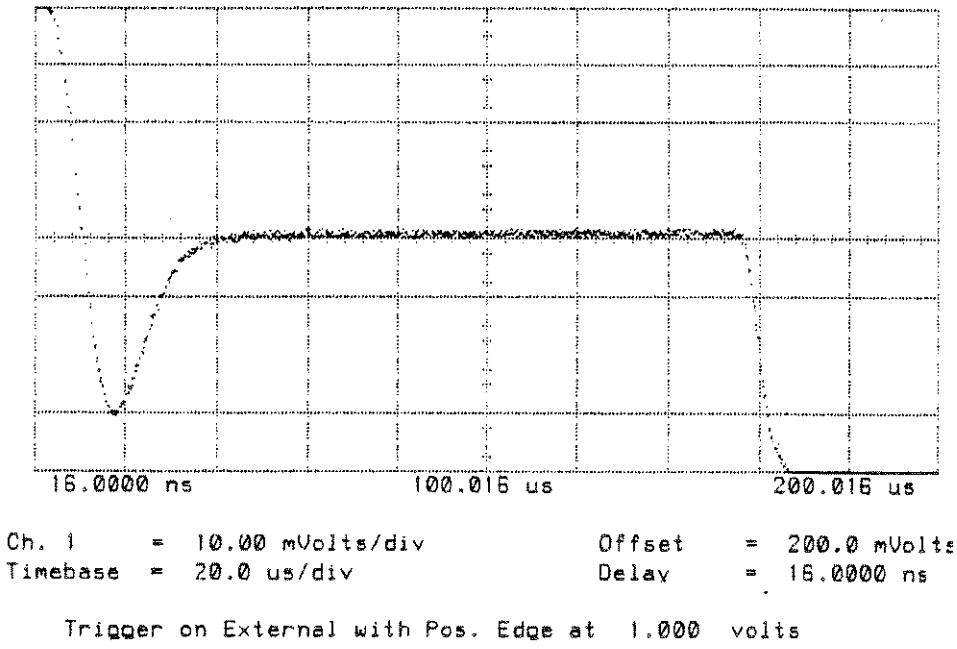


Figure 4-10. Feedthrough Not Compensated

4. Adjust RC1 (R5) until the positive and negative pulse peaks are equidistant from the flat portion of the pulse, $V_P = V_N$. The Delta V markers may help determine when the pulse peaks are equidistant. Refer to figure 4-11.

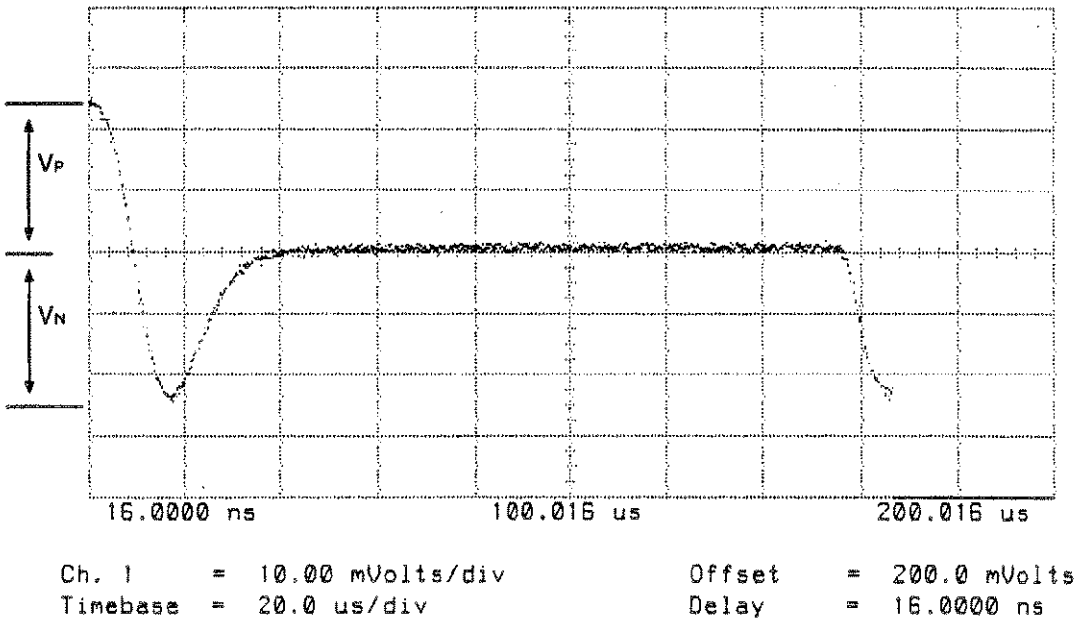


Figure 4-11. Adjusting RC1 for Equidistant Pulse Peaks.

5. Adjust CC1 (R9) until the positive and negative pulse peaks are the lowest in amplitude.
   Re-adjust RC1 and CC1 until pulse top is as flat as possible.

6. Set channel 1 to 1 mV/div and offset to 300 mV (do not turn channel 1 off).
   Turn channel 2 on.

7. Repeat steps 4-5 except use adjustments RC2 (R6) and CC2 (R10).

8. Turn channel 2 off and channel 3 on.
   Move semi-rigid cables from channel 2 to channel 3's input.

9. Repeat steps 4-5 except use adjustments RC3 (R7) and CC3 (R11).

10. Turn channel 3 off and channel 4 on.
    Move semi-rigid cables from channel 3 to channel 4's input.

11. Repeat steps 4-5 except use adjustments RC4 (R8) and CC4 (R12).
    Remove semi-rigid cables from oscilloscope.

Trigger Adjustments

HYSTERESIS and OFFSET are adjusted by observing the voltage level where the displayed waveform crosses the time reference, which is set to the screen's left side.

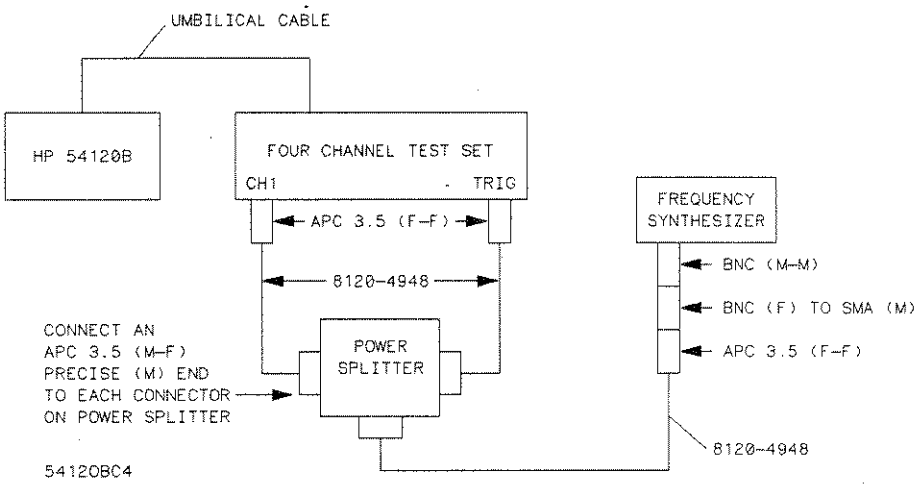
Some HP 54121A test sets with serial prefix 2802 may still use the 500 MHz trigger hybrid. If you are unsure which trigger hybrid your instrument has, remove the test set's bottom cover and locate the trigger hybrid on the horizontal board's front left side (refer to figure 4-12). The 500 MHz trigger hybrid's HP part number is 1NB7-8160.

Equipment

This is a list of the recommended test equipment for this adjustment. However, any instrument which satisfies the critical specifications may be used.

Instrument	Critical Specifications	Model.
Power divider	> 10 GHz Bandwidth	HP 11667B
Frequency Synthesizer	100 kHz at 100 mV p-p amplitude	HP 3325A
Accessories	**Critical Specifications**	**HP Part Number**
Adapter	BNC (f) to SMA (m)	1250-1200
Adapter	APC 3.5 (m-f) male end precise, 26.5 GHz Quantity needed - 5	1250-1866
Adapter	APC 3.5 (f-f)	1250-1865
Adapter	BNC (m-m)	1250-0216
Coaxial cable	APC 3.5 (m-m), 18 GHz, Quantity needed - 3	8120-4948

Equipment Connections



Equipment Setup

Signal Source

Function	Sine Wave
Frequency	100 kHz
Amplitude	100 mV p-p

HP 54120B

Display		**Timebase**	
Display Mode	Averaged	Time/Div	1 µs/div
No. of Averages	4	Delay	16 ns
Screen	Single	Delay Ref at	Left
Graticule	Grid	Sweep	Trg'd
Bandwidth	12.4 GHz		
Channels		**Trigger**	
Channel 1	On	Trigger Level	0 V
Volts/Div	10 mV/div	HF Sens.	Off
Offset	0 mV	HF Reject	Off
Channels 2-4	Off	Attenuation	1
Attenuation	1		
Network			
Reflect/Trans/CAL	Reflect		
Step & Chan 1	Off		

Procedure

The adjustment locations are shown on page 4-30. Information in brackets applies only to the 500 MHz trigger hybrid.

1. Connect signal generator to oscilloscope's input.

2. There should be one period of a 100 kHz sine wave with an amplitude of approximately 50 mV p-p. If not, adjust HYST (R4) fully counterclockwise and adust OFFSET (R47) to center starting point on the screen's left side.

3. While switching trigger slope between positive and negative, adjust trigger hysteresis (R48 HYST) on the Horizontal assembly (A1) until there is 15 mV [If your HP 54121A contains the 500 MHz trigger hybrid, HP Part Number 1NB7-8160, the hysteresis is set to 20 mV four minor divisions or 1 major division] (six minor divisions or 1.5 major divisions) between the sine wave's starting point for positive slope vs the starting point for negative slope at the screen's left side.

4. Continue switching slope between positive and negative as you adjust OFFSET NULL (R47) until the sine wave's starting point is centered vertically around center screen.

Channel Skew Calibration

For routine calibration, the channel skew calibration need not be done. It is recommended that the operator do a channel skew calibration with signals and cables similar to those with which the oscilloscope will be used.

Equipment & Connections

Refer to step recovery diode adjustments.

Equipment Setup

Signal Source

Frequency	250 MHz
Amplitude	+ 12 dBM

HP 54120B

Channels		**Timebase**	
Channels	1-4	Time/Div	20 ps/div
Display	On	Delay	19.9 ns
Volts/Div	2 mV/div	Delay Ref at	Left
Offset	0 V	Sweep	Trg'd
Attenuation	1		
Trigger		**Display**	
Trigger Level	0 V	Display Mode	Averaged
Slope	Pos	No. of Averages	64
Network			
Reflect/Trans/Cal	Reflect		
Step & Chan. 1	Off		

Procedure

1. Press **Utility** key.
   Press **Cal Menu** key.
   Press **Channel Skew Cals** key.

2. Verify "Channel Skew Chan 1" is highlighted.

3. Adjust channel skew with RPG knob or arrow keys in order to align trace's 0 V crossing at center screen.

4. Move input to next channel and press **Channel Skew** key until the next channel's number is highlighted.

5. Repeat steps 5 and 6 until all channels have been skewed.

6. Press Exit Cal Menu key.

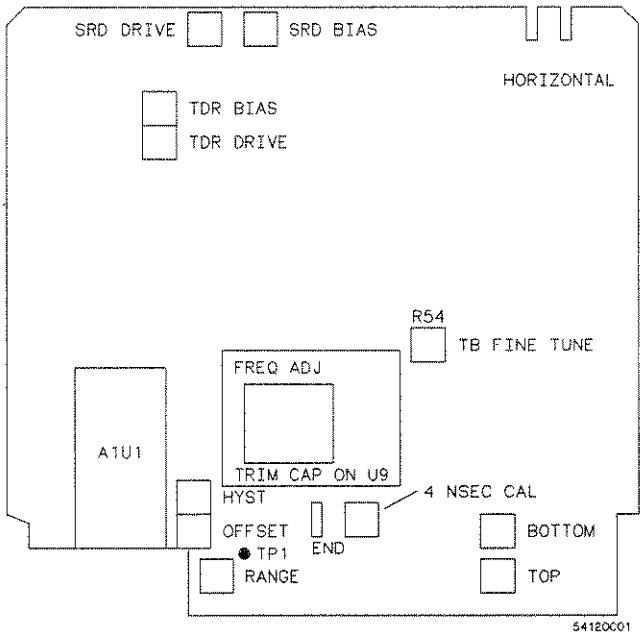


Figure 4-12. Horizontal Assembly (A1) Adjustments

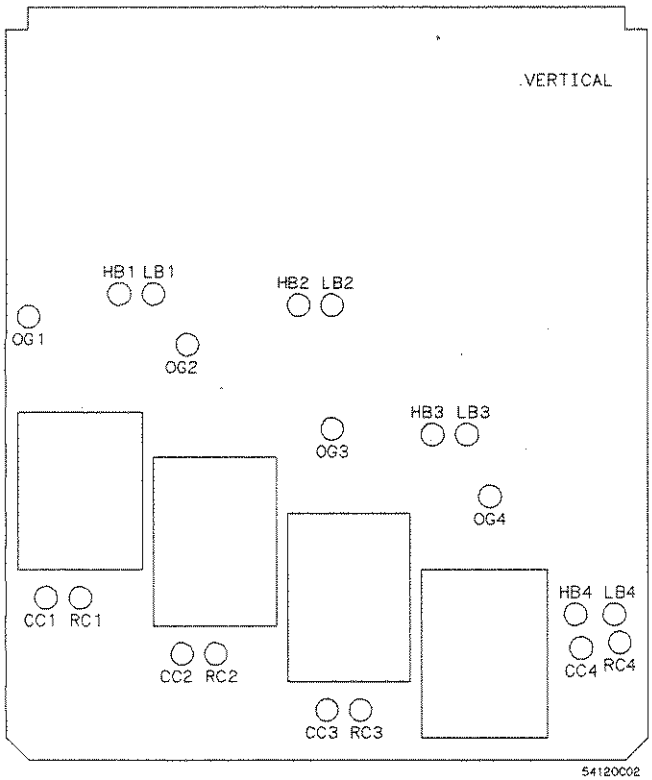


Figure 4-13. Vertical Assembly (A2) Adjustments

Table Of Contents

Replaceable Parts

Replaceable Parts 5

Introduction

This section contains information for ordering parts. Table 5-1 lists the names and addresses that correspond to the manufacturers' code numbers. Table 5-2 lists the abbreviations used in the parts list and throughout this manual. Figures 5-1 through 5-6 are drawings with reference designators included. Table 5-3 is the replaceable parts list.

Abbreviations

Table 5-2 lists the abbreviations used in the replaceable parts list. Abbreviations in the replaceable parts list are always in capital letters. In other sections of this manual abbreviations may be in capital or lower case letters.

Replaceable Parts List

Table 5-3 is a list of replaceable parts and is organized as follows:

a. Electrical assemblies in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

Information given for each part consists of the following:

a. Hewlett-Packard part number and the check digit (for HP internal use).

b. Total quantity (Qty) in the instrument, given only once at the part number's first appearance in the list.

c. Description of part.

d. A typical manufacturer of a given part in a five digit code. Refer to table 5-1 for a cross reference from code number to manufacturer name.

e. The manufacturers' part number.

Exchange Assemblies

Some of the assemblies used in this instrument have been set up on the exchange program. This allows the customer to exchange his faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Exchange assemblies are listed at the beginning of the replaceable parts table with a star (*) before the reference designator. They have a part number in the form XXXXX-695XX.

Before ordering an exchange assembly, check with your local parts or repair organization for the procedures associated with the exchange assembly program.

Ordering Information

To order a part listed in the replaceable parts table, indicate the Hewlett-Packard part number, check digit, and quantity required. Send the order to the nearest Hewlett-Packard office.

To order a part that is not listed in the replaceable parts table, include the instrument model number, serial number, description and function of part, and total quantity required. Address an order to the nearest Hewlett-Packard sales office.

Direct Mail Order System

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are as follows:

a. Direct ordering and shipment from HP Parts Center in Mountain View, California. Call your local Hewlett-Packard office for the toll free number.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through local HP offices when orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, check or money order must accompany each order.
Mail order forms and specific ordering information are available through your local HP offices.

Table 5-1. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address	Zip Code
04713	Motorola Semi Conductor Products	Phoenix Az	85008
06915	Pan Asian Paper Product Mfg SDN BHD	Pinang	Malaysia
28480	Hewlett-Packard Co. Corporate HQ	Palo Alto Ca	94304
86928	Seastrom Mfg Co.	Glendale Ca	91201

Table 5-2. Reference Designator and Abbreviations

REFERENCE DESIGNATOR

A	= assembly	F	= fuse	Q	= transistor;SCR; triode thyristor	U	= integrated circuit; microcircuit
B	= fan;motor	FL	= filter	R	= resistor	V	= electron tube; glow lamp
BT	= battery	H	= hardware	RT	= thermistor	VR	= voltage regulator; breakdown diode
C	= capacitor	J	= electrical connector (stationary portion);jack	S	= switch;jumper	W	= cable
CR	= diode;diode thyristor; varactor	L	= coil;inductor	T	= transformer	X	= socket
DL	= delay line	MP	= misc. mechanical part	TB	= terminal board	Y	= crystal unit(piezo-electric or quartz)
DS	= annunciator;lamp;LED	P	= electrical connector (moveable portion);plug	TP	= test point		
E	= misc. electrical part						

ABBREVIATIONS

A	= amperes	DWL	= dowel	MFR	= manufacturer	RND	= Round
A/D	= analog-to-digital	ECL	= emitter coupled logic	MICPROC	= microprocessor	ROM	= read-only memory
AC	= alternating current	ELAS	= elastomeric	MINTR	= miniature	RPG	= rotary pulse generator
ADJ	= adjust(ment)	EXT	= external	MISC	= miscellaneous	RX	= receiver
AL	= aluminum	F	= farads;metal film (resistor)	MLD	= molded	S	= Schottky-clamped; seconds(time)
AMPL	= amplifier			MM	= millimeter		
ANLG	= analog	FC	= carbon film/ composition	MO	= metal oxide	SCR	= screw;silicon controlled rectifier
ANSI	= American National Standards Institute	FD	= feed	MTG	= mounting		
		FEM	= female	MTLC	= metallic	SEC	= second(time);secondary
ASSY	= assembly	FF	= flip-flop	MUX	= multiplexer		
ASTIG	= astigmatism	FL	= flat	MW	= milliwatt	SEG	= segment
ASYNCHRO	= asynchronous	FM	= foam;from	N	= nano(10^{-9})	SEL	= selector
ATTEN	= attenuator	FR	= front	NC	= no connection	SGL	= single
AWG	= American wire gauge	FT	= gain bandwidth product	NMOS	= n-channel metal-oxide-semiconductor	SHF	= shift
BAL	= balance					SI	= silicon
BCD	= binary-code decimal	FW	= full wave	NPN	= negative-positive-negative	SIP	= single in-line package
BD	= board	FXD	= fixed	NPRN	= neoprene	SKT	= skirt
BFR	= buffer	GEN	= generator	NRFR	= not recommended for field replacement	SL	= slide
BIN	= binary	GND	= ground(ed)			SLDR	= solder
BRDG	= bridge	GP	= general purpose	NSR	= not separately replaceable	SLT	= slot(ted)
BSHG	= bushing	GRAT	= graticule			SOLD	= solenoid
BW	= bandwidth	GRV	= groove	NUM	= numeric	SPCL	= special
C	= ceramic;cermet (resistor)	H	= henries;high	OBD	= order by description	SQ	= square
		HD	= hardware	OCTL	= octal	SREG	= shift register
CAL	= calibrate;calibration	HDND	= hardened	OD	= outside diameter	SRQ	= service request
CC	= carbon composition	HG	= mercury	OP AMP	= operational amplifier	STAT	= static
CCW	= counterclockwise	HGT	= height	OSC	= oscillator	STD	= standard
CER	= ceramic	HLCL	= helical	P	= plastic	SYNCHRO	= synchronous
CFM	= cubic feet/minute	HORIZ	= horizontal	P/O	= part of	TA	= tantalum
CH	= choke	HP	= Hewlett-Packard	PC	= printed circuit	TBAX	= tubeaxial
CHAM	= chamfered	HP-IB	= Hewlett-Packard Interface Bus	PCB	= printed circuit board	TC	= temperature coefficient
CHAN	= channel			PD	= power dissipation	TD	= time delay
CHAR	= character	HR	= hour(s)	PF	= picofarads (10^{-12})	THD	= thread(ed)
CM	= centimeter	HV	= high voltage	PI	= plug in	THK	= thick
CMOS	= complementary metal-oxide-semiconductor	HZ	= Hertz	PL	= plate(d)	THRU	= through
		I/O	= input/output	PLA	= programmable logic array	TP	= test point
CMR	= common mode rejection	IC	= integrated circuit			TPG	= tapping
		ID	= inside diameter	PLST	= plastic	TPL	= triple
CNDCT	= conductor	IN	= inch	PNP	= positive-negative-positive	TRANS	= transformer
CNTR	= counter	INCL	= include(s)			TRIG	= trigger(ed)
CON	= connector	INCAND	= incandescent	POLYE	= polyester	TRMR	= trimmmer
CONT	= contact	INP	= input	POS	= positive;position	TRN	= turn(s)
CRT	= cathode-ray tube	INTEN	= intensity	POT	= potentiometer	TTL	= transistor-transistor
CW	= clockwise	INTL	= internal	POZI	= pozidrive	TX	= transmitter
D	= diameter	INV	= inverter	PP	= peak-to-peak	U	= micro(10^{-6})
D/A	= digital-to-analog	JFET	= junction field-effect transistor	PPM	= parts per million	UL	= Underwriters Laboratory
DAC	= digital-to-analog converter			PRCN	= precision		
		JKT	= jacket	PREAMP	= preamplifier	UNREG	= unregulated
DARL	= darlington	K	= kilo(10^{3})	PRGMBL	= programmable	VA	= voltampere
DAT	= data	L	= low	PRL	= parallel	VAC	= volt,ac
DBL	= double	LB	= pound	PROG	= programmable	VAR	= variable
DBM	= decibel referenced to 1mW	LCH	= latch	PSTN	= position	VCO	= voltage-controlled oscillator
		LCL	= local	PT	= point		
DC	= direct current	LED	= light-emitting diode	PW	= potted wirewound	VDC	= volt,dc
DCDR	= decoder			PWR	= power	VERT	= vertical
DEG	= degree	LG	= long	R-S	= reset-set	VF	= voltage,filtered
DEMUX	= demultiplexer	LI	= lithium	RAM	= random-access memory	VS	= versus
DET	= detector	LK	= lock			W	= watts
DIA	= diameter	LKWR	= lockwasher	RECT	= rectifier	W/	= with
DIP	= dual in-line package	LS	= low power Schottky	RET	= retainer	W/O	= without
DIV	= division	LV	= low voltage	RF	= radio frequency	WW	= wirewound
DMA	= direct memory access	M	= mega(10^{6});megohms; meter(distance)	RGLTR	= regulator	XSTR	= transistor
DPDT	= double-pole, double-throw			RGTR	= register	ZNR	= zener
		MACH	= machine	RK	= rack	°C	= degree Celsius (Centigrade)
DRC	= DAC refresh controller	MAX	= maximum	RMS	= root-mean-square		
DRVR	= driver					°F	= degree Fahrenheit
						°K	= degree Kelvin

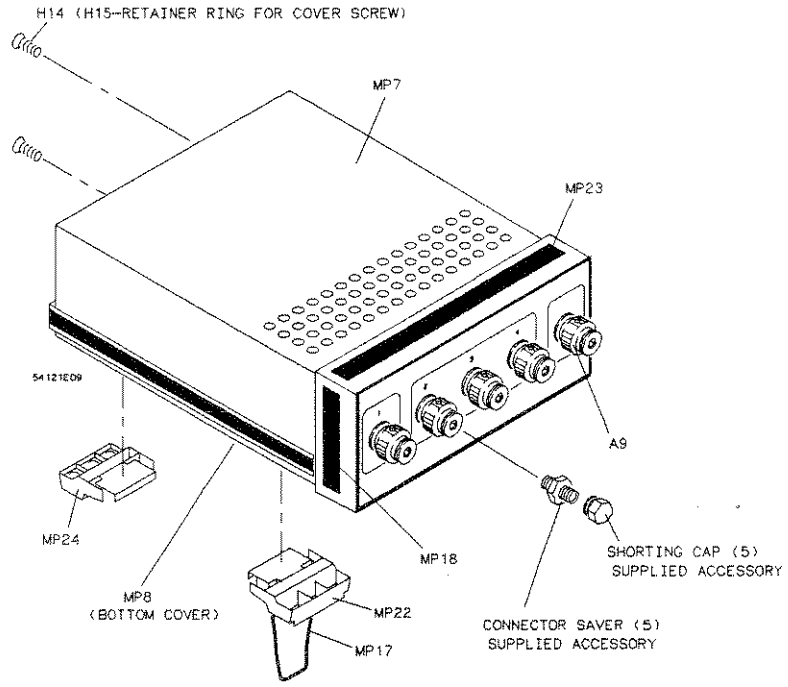


Figure 5-1. Assembled View

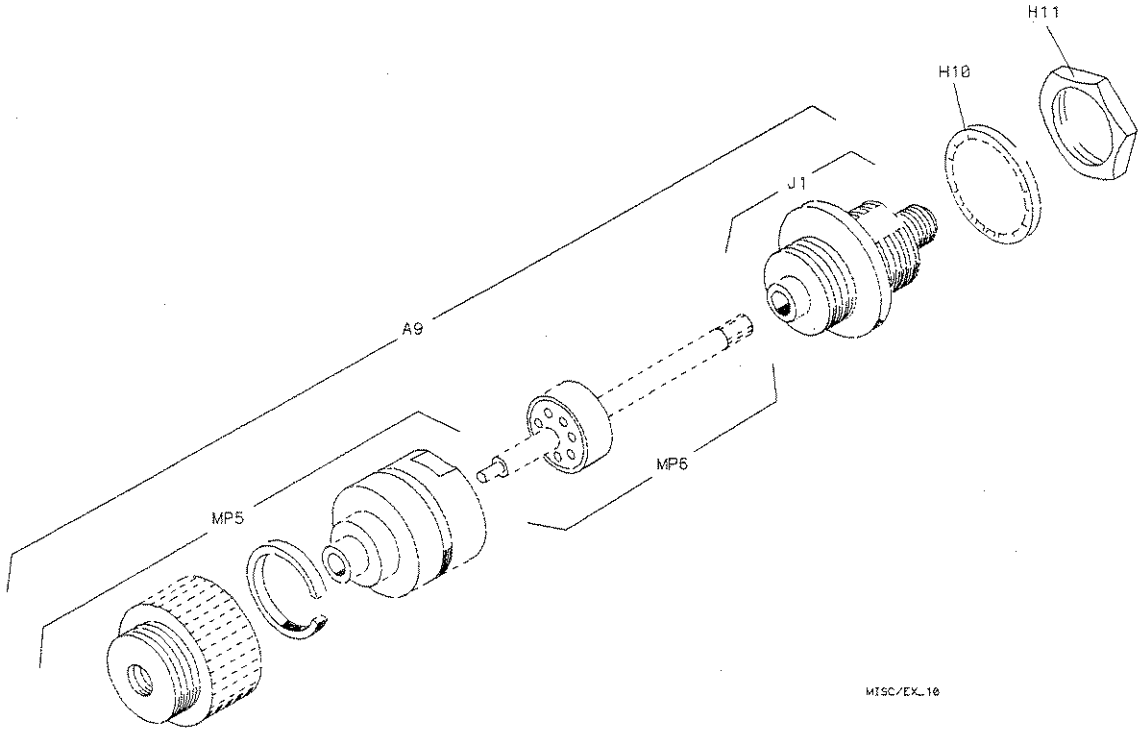


Figure 5-2. APC 3.5 Connector Exploded View

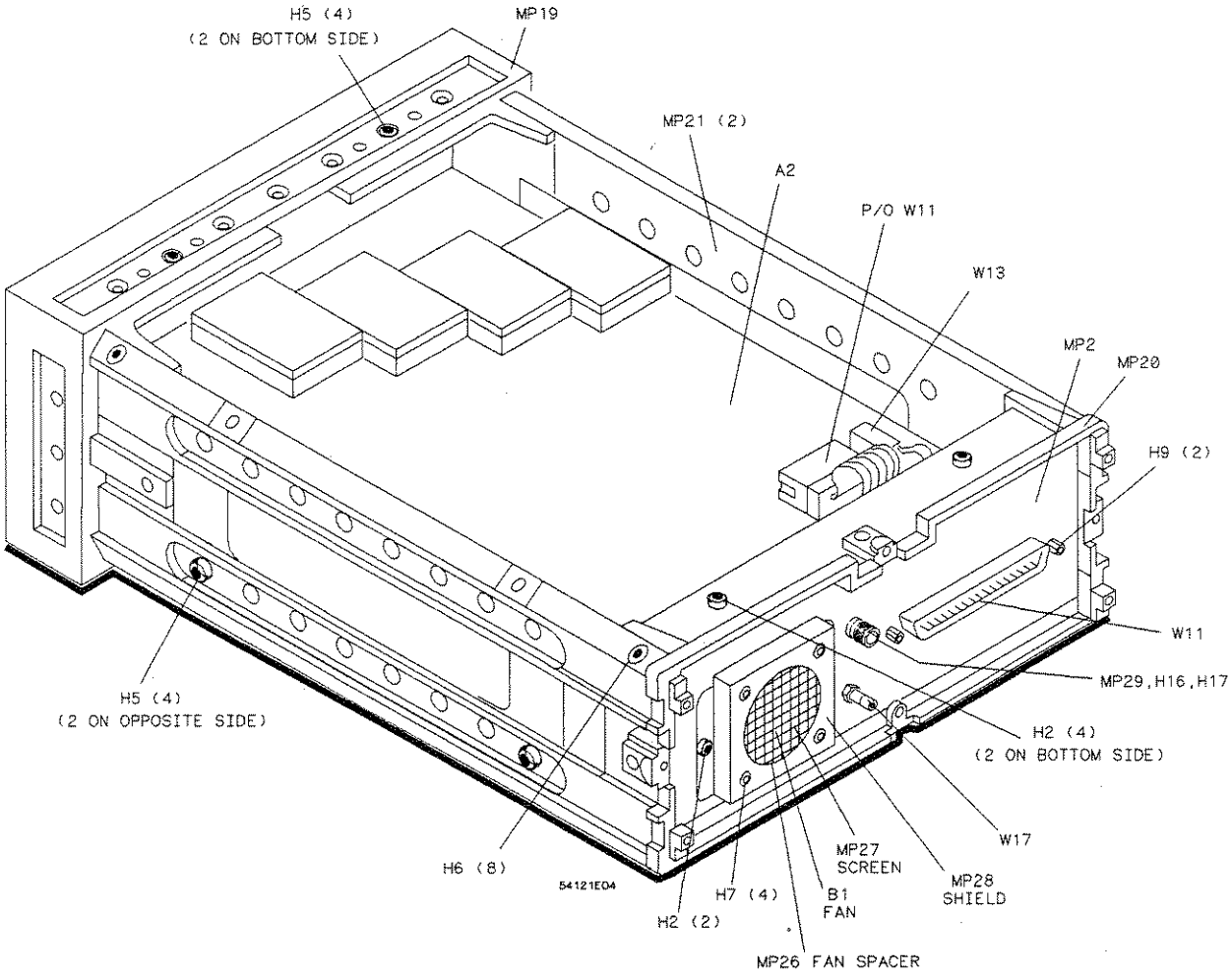


Figure 5-3. Top View

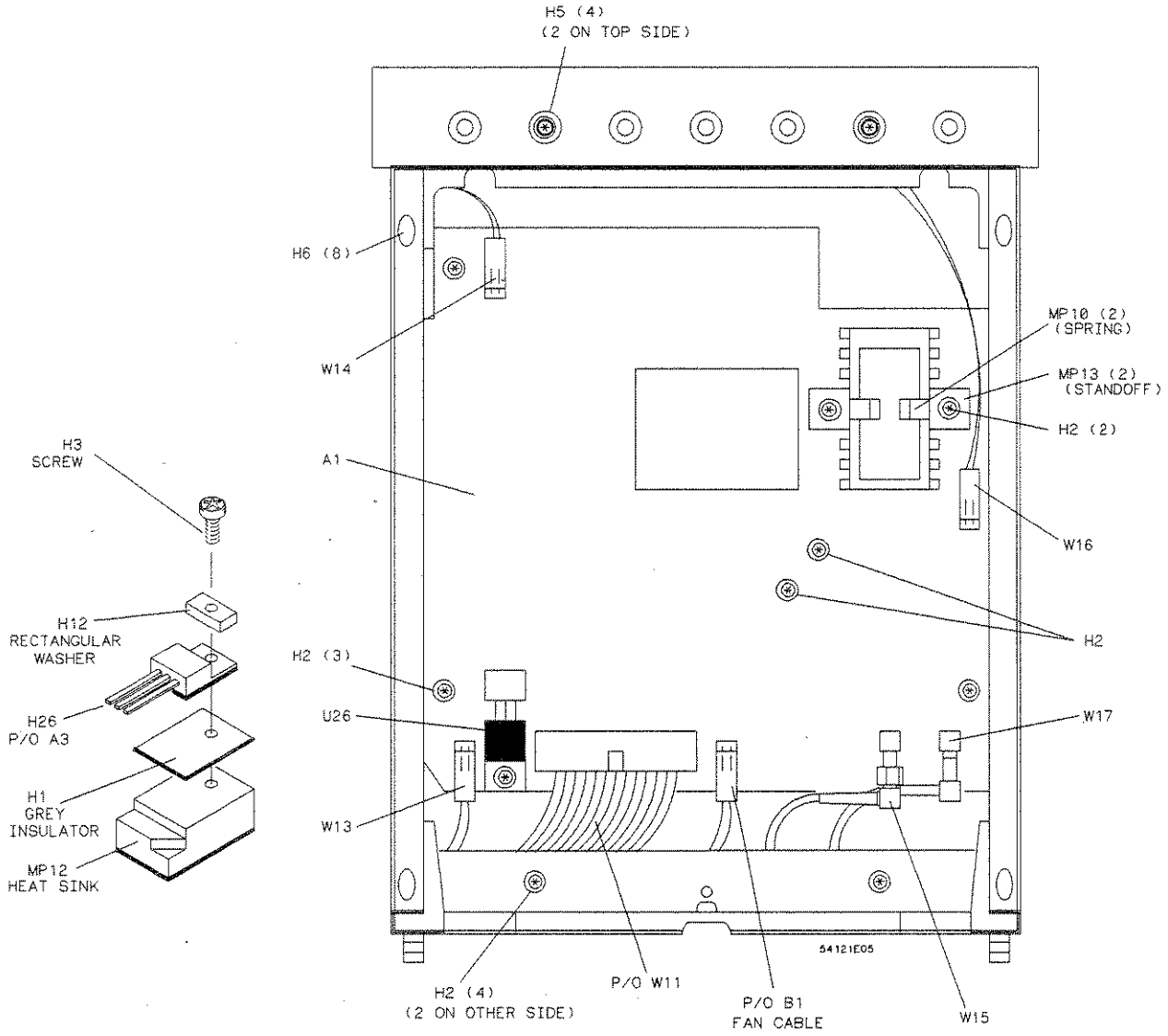


Figure 5-4. Bottom View

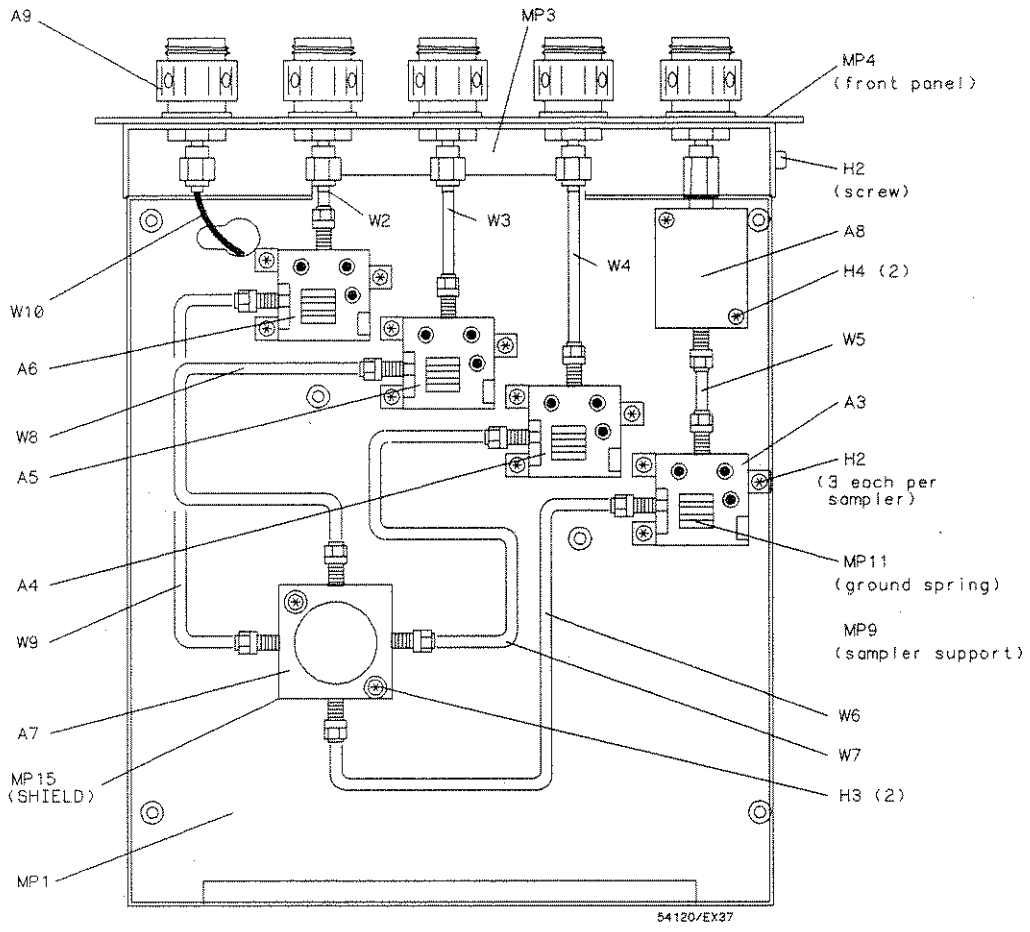


Figure 5-5. Main Deck without Vertical Assembly

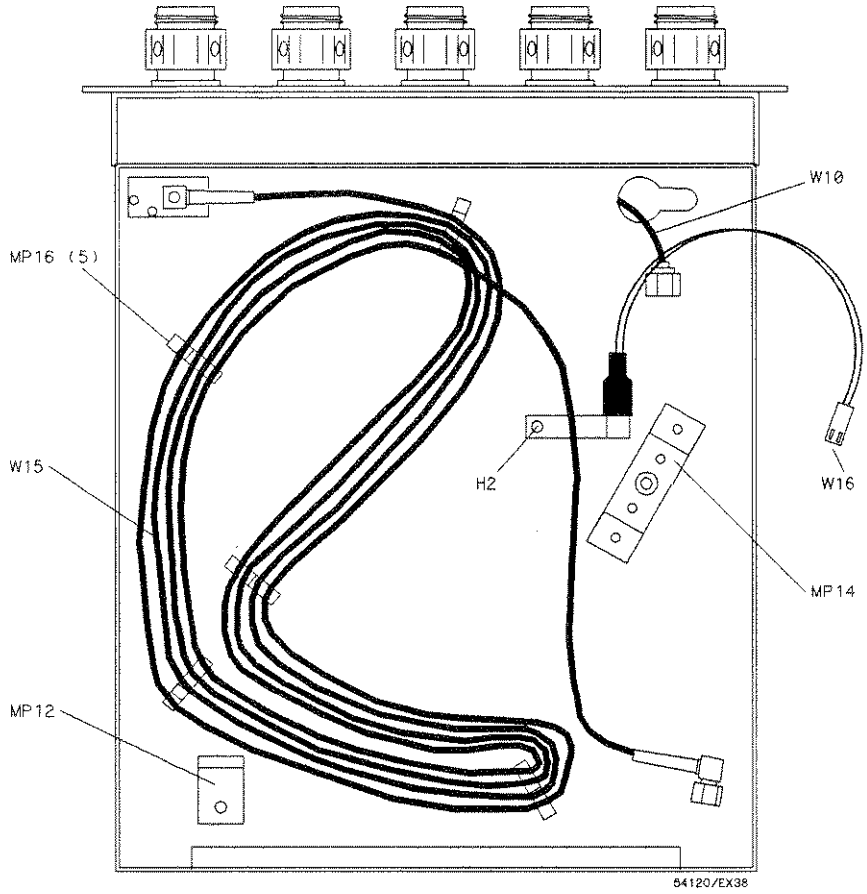


Figure 5-6. Main Deck without Horizontal Assembly

Table 5-3. Replaceable Parts List

Reference Designator	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
*EXCHANGE ASSEMBLIES						
*A1	54120-69510	5	0	HORIZONTAL ASSEMBLY	28480	54120-69510
*A2	54120-69506	9	0	VERTICAL ASSEMBLY	28480	54120-69506
A1	54120-66510	9	1	HORIZONTAL ASSEMBLY	28480	54120-66510
A2	54120-66506	3	1	VERTICAL ASSEMBLY	28480	54120-66506
A3	5086-7460	7	4	SAMPLER	28480	5086-7460
A4	5086-7460	7		SAMPLER	28480	5086-7460
A5	5086-7460	7		SAMPLER	28480	5086-7460
A6	5086-7460	7		SAMPLER	28480	5086-7460
A7	5086-7461	8	1	PULSE FILTER	28480	5086-7461
A8	5086-7471	3	1	TDR STEP GENERATOR	28480	5086-7471
A9	5062-1247	6	5	APC 3.5 CONNECTOR	28480	5062-1247
A1U1	INB7-8130	6	1	2.5 GHZ TRIGGER HYBRID	28480	INB7-8130
B1	54121-88501	5	1	FAN-TUBAXIAL WITH CONNECTOR	28480	54121-88501
H1	0340-1074	2	1	INSULATOR-XSTR THRM-CNDCT	28480	0340-1074
H2	0515-03722	3	5	SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-LG	28480	0515-0372
H3	0515-0664	5	6	SCREW-MACHINE ASSEMBLY M3 X 0.5 12MM-LG	28480	0515-0664
H4	0515-0666	7	2	SCREW-MACHINE ASSEMBLY M3 X 0.5 18MM-LG	28480	0515-0666
H5	0515-1031	2	4	SCREW-MACH M3 X 0.5 6MM-LG 90-DEG-FLH-HD	28480	0515-1031
H6	0515-1403	2	8	SCREW-SPCL M4 X 0.7 6MM-LG 90-DEG-FLH-HD	28480	0515-1403
H7	0515-1038	9	4	M3 PANHEAD 35L	28480	0515-1038
H7-8	NOT ASSIGNED					
H9	1251-2942	7	2	SCREW LOCK KIT-SUBMIN D CONN	28480	1251-2942
H10	2190-0914	0	5	WASHER-LK INTL T 7/16 IN .472-IN-ID	28480	2190-0914
H11	2950-0132	6	5	NUT-HEX-DBL-CHAM 7/16 (THD .094-IN-THK	28480	2950-0132
H12	3050-1071	7	1	WASHER-RECTANGULAR 10.28 MM LG; 5.59 MM	04713	3050-1071
H13	NOT ASSIGNED					
H14	0515-1245	0	2	COVER SCREW	28480	0515-1245
H15	0515-1253	0	2	RETAIN RING FOR COVER SCREW	28480	0515-1253
H16	2950-0072	3	1	NUT 1/4 - 32 .062	28480	2950-0072
h17	2190-0027	6	1	WASHER-LK INTL .256 .478 .02	28480	2190-0027
J1	08513-20017	6	5	APC 3.5 BULKHEAD CONNECTOR P/O A9	28480	08513-20017
MP1	54120-00102	7	1	MAIN DECK	28480	54120-00102
MP2	54120-00206	3	1	REAR PANEL	28480	54120-00206
MP3	54120-00204	0	1	SUB PANEL LOWER BRACKET	28480	54120-00204
MP4	54120-00205	1	1	FRONT PANEL	28480	54120-00205
MP5	5062-1245	4	5	APC 3.5 CONNECTOR BODY P/O A9	28480	5062-1245
MP6	5062-1243	2	5	APC 3.5 CENTER CONDUCTOR P/O A9	28480	5062-1243
MP7	54120-04104	7	1	TOP COVER	28480	54120-04014
MP8	54120-04105	8	1	BOTTOM COVER	28480	54120-04105
MP9	54120-04701	0	4	SAMPLER SUPPORT	28480	54120-04701
MP10	54120-09101	4	2	TRIGGER SPRING	28480	54120-09101
MP11	54120-09102	5	4	SAMPLER GROUND SPRING	28480	54120-09102

Table 5-3. Replaceable Parts List

Reference Designator	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP12	54120-21102	1	1	HEATSINK	28480	54120-21102
MP13	0380-1949	4	2	TRIGGER STANDOFF	28480	0380-1949
MP14	54120-24701	2	1	PULSE FILTER GROUND BLOCK	28480	54120-24701
MP15	54120-45401	3	1	PULSE FILTER SHIELD	28480	54120-45401
MP16	1400-0866	7	5	CLAMP-CABLE .187-DIA .25-WD NYL	28480	1400-0866
MP17	1460-1345	5	2	TILT STAND SST	28480	1460-1345
MP18	5001-0438	7	2	SIDE TRIM STRIP	28480	5001-0438
MP19	5021-5813	4	1	FRONT FRAME	28480	5021-5813
MP20	5021-5814	5	1	REAR FRAME	28480	5021-5814
MP21	5021-5884	9	2	SIDE STRUT	28480	5021-5884
MP22	5040-7201	8	2	BOTTOM FEET	28480	5040-7201
MP23	5040-7203	0	1	TOP FRONT TRIM STRIP284805040-7203		
MP24	5040-7222	3	2	NON SKID FOOT	28480	5040-7222
MP25	0960-0055	1	5	CAP-COAX TO FIT F-SMA SHTG	28480	0960-0055
MP26	54121-04701	1	1	FAN SPACER	28480	54121-04701
MP27	54120-00604	4	1	FAN SCREEN	28480	54120-00604
MP28	54120-00605	5	1	FAN SHIELD	28480	54120-00605
MP29	1510-0038	2	1	BINDING POST	28480	1510-0038
W1	NOT ASSIGNED					
W2	54120-61602	0	1	SEMI-RIGID CABLE CH4 SAMPLER TO FRONT PANEL	28480	54120-61602
W3	54120-61603	1	1	SEMI-RIGID CABLE CH3 SAMPLER TO FRONT PANEL	28480	54120-61603
W4	54120-61604	2	1	SEMI-RIGID CABLE CH2 SAMPLER TO FRONT PANEL	28480	54120-61604
W5	54120-61605	3	1	SEMI-RIGID CABLE CH1 SAMPLER TO TDR	28480	54120-61605
W6	54120-61606	4	1	SEMI-RIGID CABLE CH1 SAMPLER TO PULSE FILTER	28480	54120-61606
W7	54120-61607	5	1	SEMI-RIGID CABLE CH2 SAMPLER TO PULSE FILTER	28480	54120-61607
W8	54120-61608	6	1	SEMI-RIGID CABLE CH3 SAMPLER TO PULSE FILTER	28480	54120-61608
W9	54120-61609	7	1	SEMI-RIGID CABLE CH4 SAMPLER TO PULSE FILTER	28480	54120-61609
W10	54120-61610	0	1	SEMI-RIGID CABLE TRIGGER TO FRONT PANEL	28480	54120-61610
W11	54120-61611	1	1	TEST SET CABLE ASSEMBLY	28480	54120-61611
W12	NOT ASSIGNED					
W13	54120-616133	1	2	WIRE INTERCONNECT CABLE VERTICAL TO HORIZON	28480	54120-61613
W14	54120-616144	1	2	WIRE CABLE TDR TO HORIZONTAL ASSEMBLY	28480	54120-61614
W15	54120-61615	5	1	TDR DELAY LINE COAXIAL CABLE-ON MAIN DECK	28480	54120-61615
W16	54120-61616	6	1	2 WIRE CABLE TEMPERATURE SENSE TO HORIZON	28480	54120-61616
W17	54120-61617	7	1	TRIGGER CABLE-REAR PANEL	28480	54120-61617

Table Of Contents

Disassembly

Disassembly 6A

Introduction

This section contains removal and replacement procedures for HP 54121A Four Channel Test Set assemblies.

Safety Considerations

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

These procedures are used while repairing an instrument that has protective covers removed and may have had power applied. Maintenance should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock). Read the Safety Summary in the front of this manual.

Do not remove or replace any of the circuit board assemblies in the instrument unless instrument power is removed. The boards contain components which may be damaged if the board is removed or replaced when instrument power is applied.

The HP 54121A Four Channel Test Set is very sensitive to static discharge. Failure to observe proper antistatic methods may result in damage to the gallium arsenide samplers. All maintenance or operation should be performed while using an antistatic mat and wrist strap which are supplied with the HP 54120B Mainframe.

Tools Required

The hardware requires TORXI type tools for removal and replacement. Sizes required for the procedures in this section are #10 and #15. A medium posi drive is used for the covers. The other tools used in this section are: 5/16 inch open end wrench, 9/16 inch open end wrench (this wrench is a thin wrench HP part number 8710-1770, used in paragraph 6A-31), 1/4 inch nut driver, 5 mm nut driver, and torque wrench set to 5 in/lbs.

Fan

Removal

1. Disconnect power cable.
2. Remove bottom cover.
3. Remove two screws holding fan assembly to rear panel. Refer to figure 6A-1
4. Unplug fan cable from J6 on the horizontal assembly.
5. Slowly pull fan assembly away from test set while feeding fan cable through fan opening in rear panel.
6. Remove four screws which hold fan to fan assembly.

Replacement

1. Reverse removal procedure to install fan.

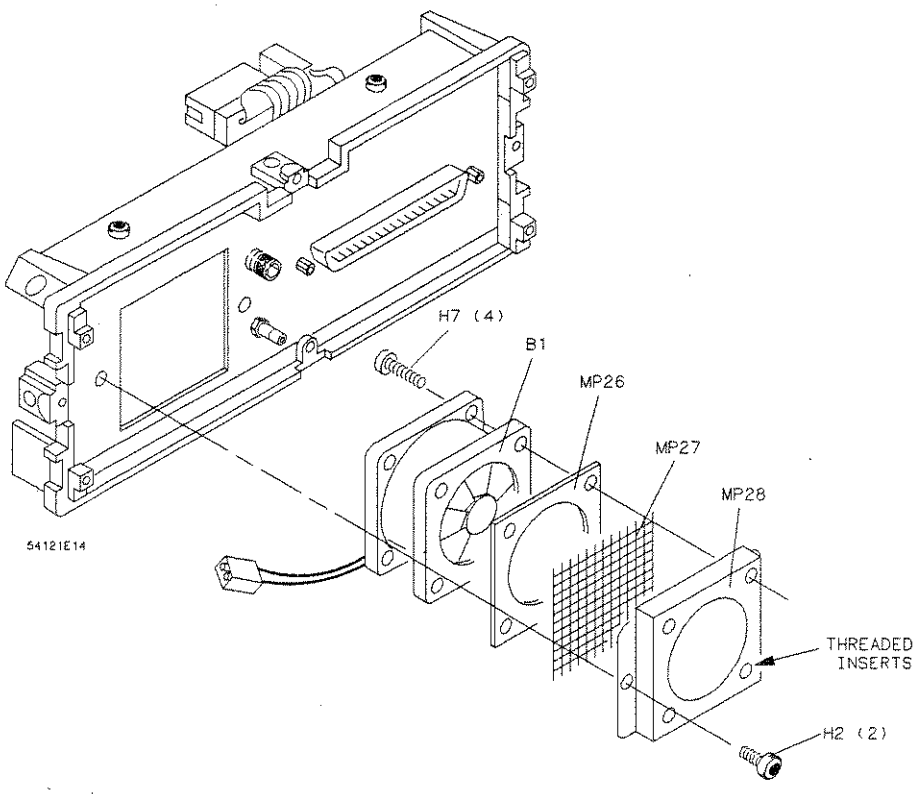


Figure 6A-1. Fan Removal

Rear Panel

Removal

1. Disconnect power cable.
2. Remove top and bottom covers.
3. Remove four screws from top and bottom of rear casting. Refer to figure 6A-2.
4. Disconnect fan cable from J6 on the horizontal assembly.
5. Disconnect ribbon cables from J7 on the horizontal assembly and J1 on the vertical assembly.
6. Disconnect trigger power cable from connector J3 on the horizontal assembly.
7. Pull rear panel away from test set.

Replacement

1. Reverse removal procedure to install rear panel.

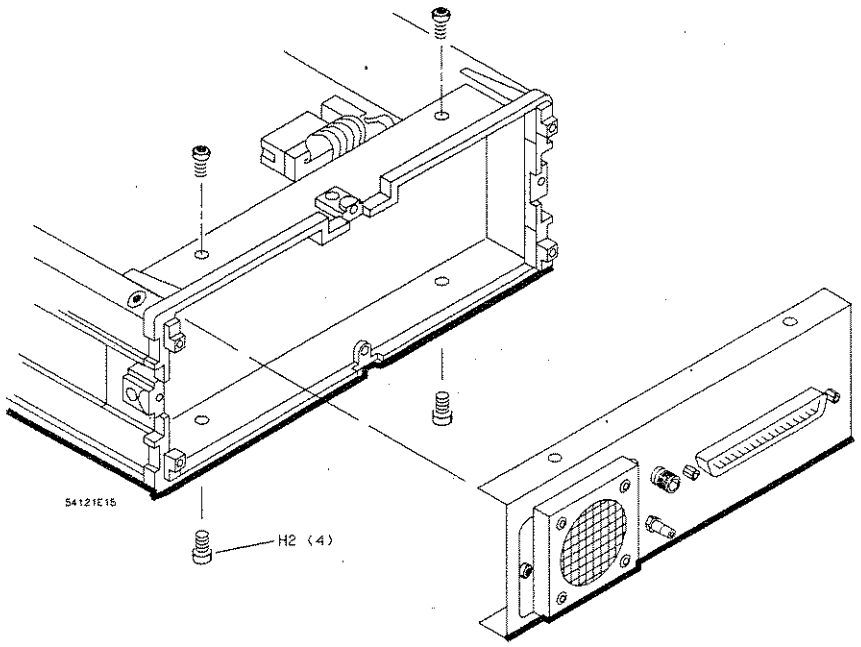


Figure 6A-2. Rear Panel Removal

Test Set Cable Assembly

Removal

1. Disconnect power cable.
2. Remove umbilical cable from the test set.
3. Remove rear panel from test set. Refer to rear panel removal.
4. Remove two screws which attach test set cable assembly to the rear panel with a 5 mm nut driver or wrench. Refer to figure 6A-3.

Replacement

1. Reverse removal procedure to install cable.

Note

The factory applies a small amount of loctite on each screw's threads before installing screws. This prevents the screws from loosening after repeated removal and installing of the umbilical cable.

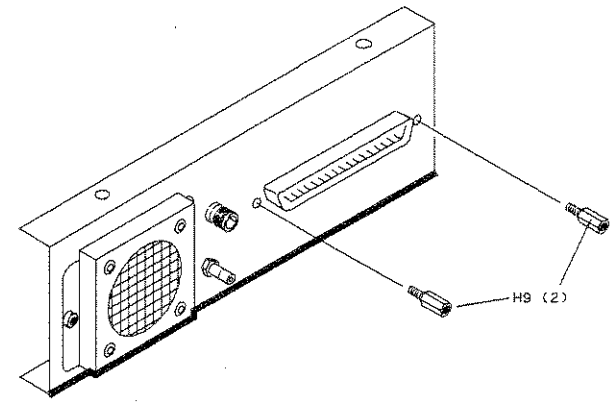


Figure 6A-3. Test Set Cable Assembly Removal

Trigger Power Cable

Removal

1. Disconnect power cable.

2. Remove rear panel from test set. Refer to paragraph 6A-5.

3. Use a 1/4" nut driver or wrench to remove hex nut and washer which attach the trigger power cable to the rear panel. Refer to rear panel removal.

Replacement

1. Reverse removal procedure to install cable.

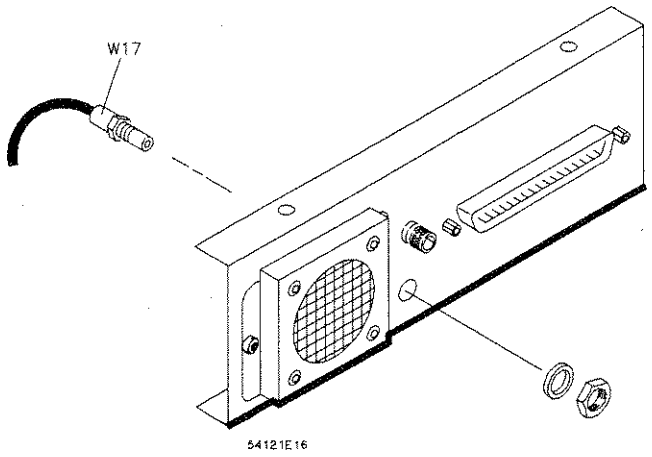


Figure 6A-4. Trigger Power Cable Removal

Main Deck Assembly

Removal

1. Disconnect power cable.
2. Remove top and bottom covers.
3. Remove two screws from each side rail. Refer to figure 6A-5.
4. Remove four screws from top and bottom of front casting. Refer to figure 6A-5.
5. Disconnect fan assembly cable from J6 on horizontal assembly.
6. Disconnect TDR delay line from connector J4 on the horizontal assembly.
7. Disconnect ribbon cables from J1 on vertical and J7 on horizontal assembly.
8. Slowly pull main deck assembly out of frame, to avoid snagging parts on frame.

Replacement

1. Reverse removal procedure to install main deck assembly.

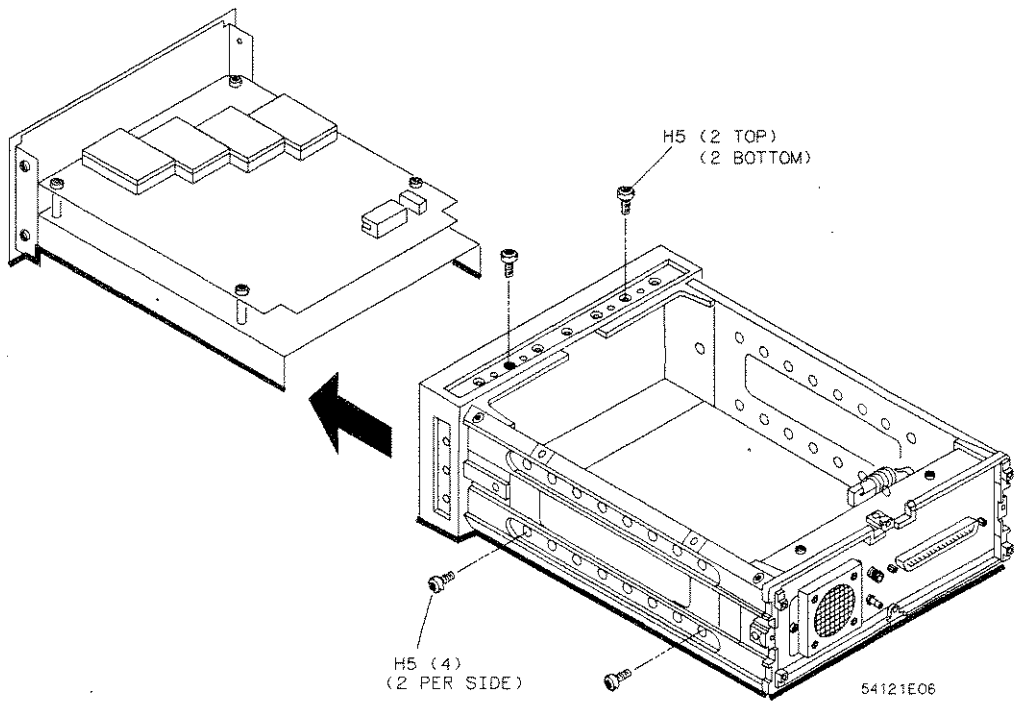


Figure 6A-5. Main Deck Assembly Removal

Vertical Assembly

Removal

1. Disconnect power cable.
2. Remove main deck assembly. Refer to main deck removal.
3. Remove six screws holding vertical assembly to main deck. Refer to figure 6A-6.
4. Disconnect interconnect cable connected to J2 on vertical assembly.
5. Slowly pull vertical assembly straight up, while gently rocking assembly from side to side, until assembly is free of main deck. The rocking motion will help free the assembly from the sampler pins.

Caution 

The exposed sampler pins are very sensitive to electrostatic damage (ESD).

Replacement

1. Reverse removal procedure to install main deck assembly. Be very careful not to bend any of the sampler hybrid pins when pushing the vertical assembly onto the main deck.

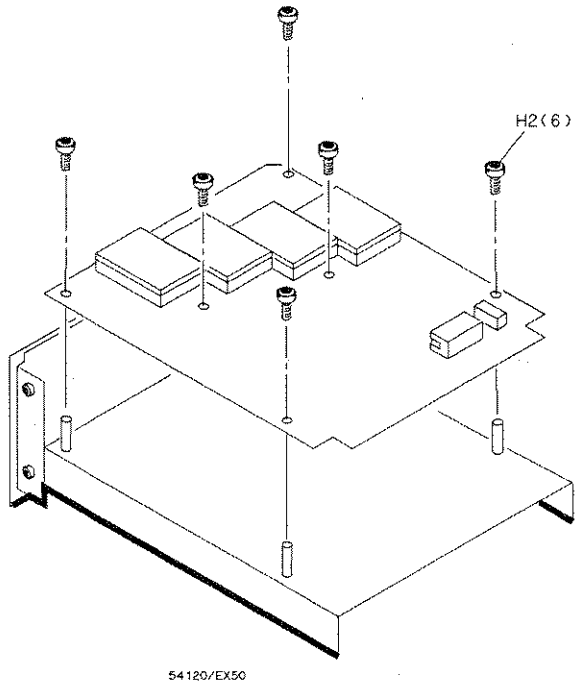


Figure 6A-6. Vertical Assembly Removal

Sampler, Pulse Filter Assemblies

Removal

1. Disconnect power cable.

2. Remove main deck assembly and vertical assembly. Refer to main deck and vertical assembly removal.

Caution

The exposed sampler, pulse filter, and TDR pins are very sensitive to electrostatic damage (ESD). All maintenance should be performed while using an antistatic mat and wrist strap which are supplied with the instrument.

3. Use a 5/16" open end wrench to unscrew rigid cables from assembly. Do not disconnect the semi-rigid cables from the assembly yet. The semi-rigid cables should not be stressed or bent. Refer to figure 6A-7.

4. Loosen screws holding assembly to main deck. The semi-rigid cables can now be slipped out of the assembly.

Replacement

1. Attach replacement assembly to main deck with screws but do not tighten screws.

2. Install semi-rigid cable into assembly. When pushing semi-rigid cables into connectors, a definite slight snap sound will be heard as the cable and connector are seated together.

3. Tighten assembly screws.

4. Torque semi-rigid cables to 5 in/lbs.

5. Reverse remainder of assembly removal to complete installation of the assembly.

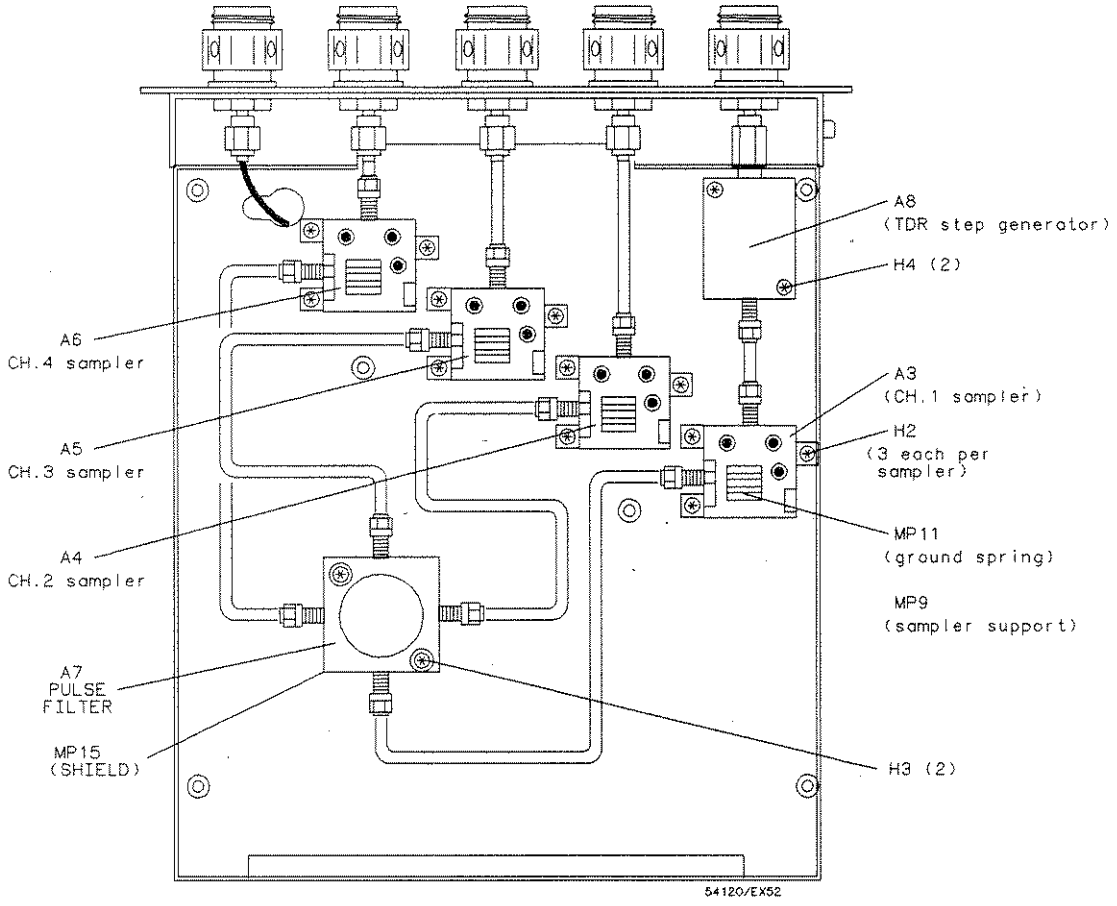


Figure 6A-7. Sampler and Pulse Filter Assembly Locations

TDR (Step Generator)

Removal

1. Remove channel 1's sampler. Refer to sampler removal procedure.
2. Remove delay line from TDR (step generator) with a 5/16 inch open end wrench. If you require additional room for the wrench, the horizontal assembly may be removed. To remove the horizontal assembly refer to horizontal assembly removal..
3. Disconnect TDR levels cable (W14) from TDR.
4. Loosen connection between the TDR and the front panel bulk head connector with a 5/16 inch open end wrench.
5. Remove two screws holding the TDR to main deck.
6. Gently pull TDR from the bulkhead connector and lift the TDR from the main deck.

Replacement

1. Install TDR into bulkhead connector and loosely connect to TDR.
2. Install two screws which hold TDR to main deck, do not tighten screws.
3. Reconnect TDR levels cable to TDR and loosely connect TDR delay line to TDR.
4. Reinstall channel 1's sampler. Refer to sampler replacement procedure above.
5. Tighten screws which hold TDR to main deck.
6. Tighten bulkhead and delay line SMA connectors to 5 in/lbs.

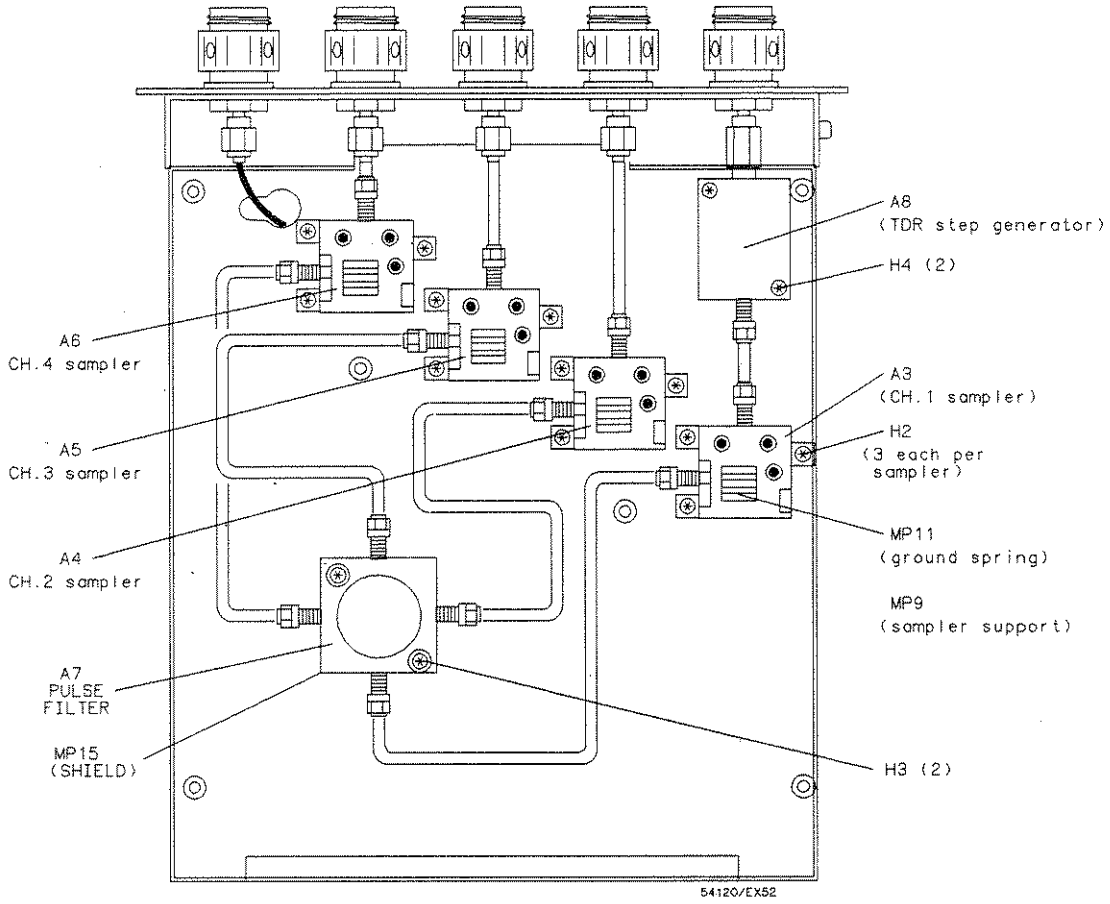


Figure 6A-8. Sampler and TDR Assembly Locations

Trigger Hybrid

Removal

1. Disconnect power cable.

2. Remove bottom cover.

3. Use a 5/16" wrench to disconnect SMA connector from trigger hybrid.

4. Remove two screws and two springs which hold trigger hybrid in place.

Caution

The exposed hybrid pins are very sensitive to electrostatic damage (ESD). All maintenance should be performed while using an antistatic mat and wrist strap which are supplied with the HP 54120B Mainframe.

5. Gently lift trigger hybrid from horizontal assembly. Refer to figure 6A-9. There will be some resistance from the socket holding the trigger hybrid in place. Gently rocking the trigger hybrid while lifting may help in removal. There is a large heat sink on the bottom side of the trigger hybrid.

Replacement

1. Reverse removal procedure to install trigger hybrid. Torque the SMA connector to 5 in/lbs.

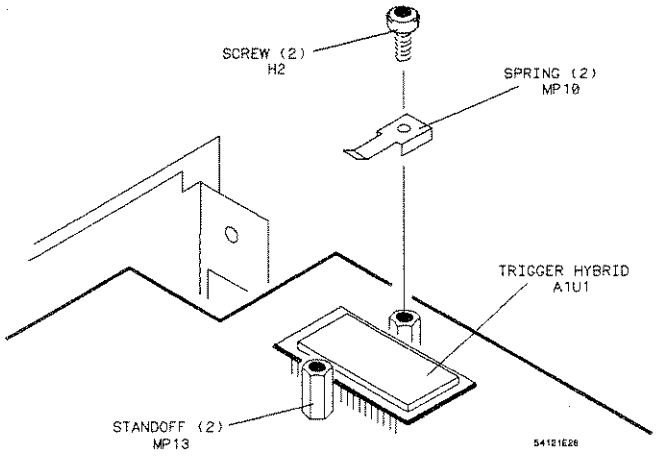


Figure 6A-9. Trigger Hybrid Removal

Horizontal Assembly

Removal

1. Disconnect power cable.

2. Remove main deck. Refer to main deck removal.

3. Remove trigger assembly. Refer to trigger assembly removal.

4. Remove five screws and two standoffs which hold the horizontal assembly to the main deck. Refer to figure 6A-10.

5. Disconnect interconnect cable connected to J9 and disconnect temperature cable connected to J2 on the horizontal assembly.

6. Use a 5/16" wrench to disconnect TDR delay line cable from SMA connector J4 on horizontal assembly.

7. Disconnect TDR levels cable from J8 on the horizontal assembly.

8. Slowly pull horizontal assembly straight up until free of main deck.

Replacement

1. Reverse removal procedure to install horizontal assembly. The SMA connectors are torqued to 5 in/lbs.

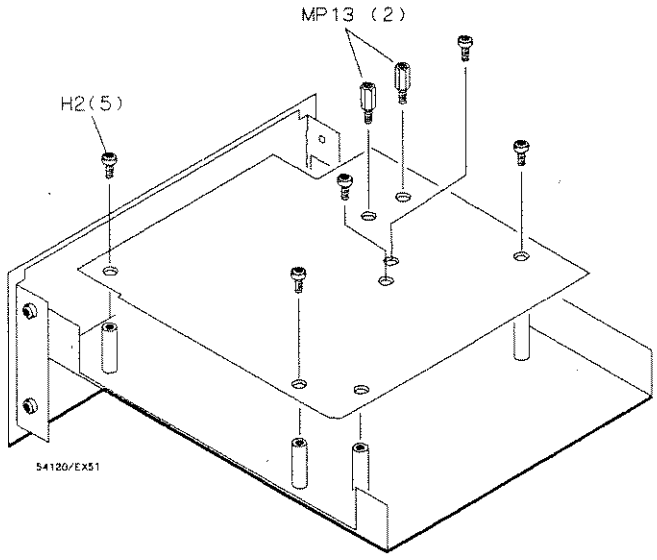


Figure 6A-10. Horizontal Assembly Removal

Temperature Sense Thermistor

Removal

1. Disconnect power cable.
2. Remove main deck. Refer to main deck removal.
3. Remove horizontal assembly. Refer to horizontal assembly removal.
4. Disconnect thermistor from main deck. Refer to figure 6A-11.

Replacement

1. Apply a small amount of thermal compound to the thermistor.
2. Reverse removal procedure to install thermistor. All SMA connectors are torqued to 5 in/lbs.

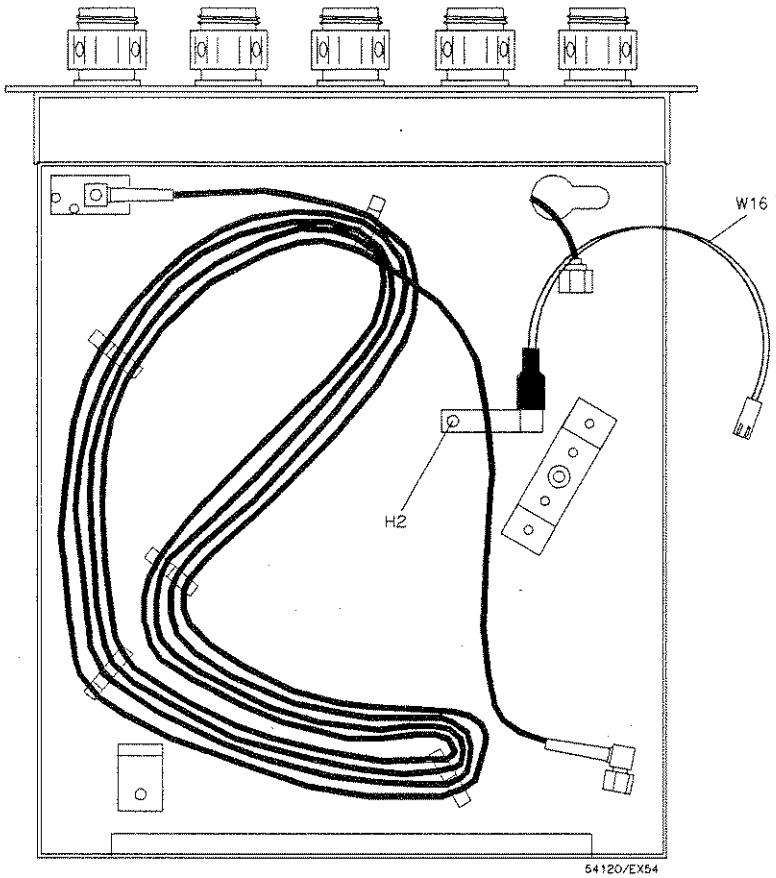


Figure 6A-11. Temperature Sense Thermistor Removal

TDR Delay Line

Removal

1. Disconnect power cable.
2. Remove main deck. Refer to main deck removal.
3. Remove horizontal assembly. Refer to horizontal assembly removal.
4. Use a 5/16" wrench to disconnect TDR delay line connected to TDR on main deck. Refer to figure 6A-12.
5. Unwind TDR delay line while paying attention to how delay line was wound. It will be rewound in the same fashion.

Replacement

1. Reverse removal procedure to install TDR delay line. All SMA connectors are torqued to 5 in/lbs.

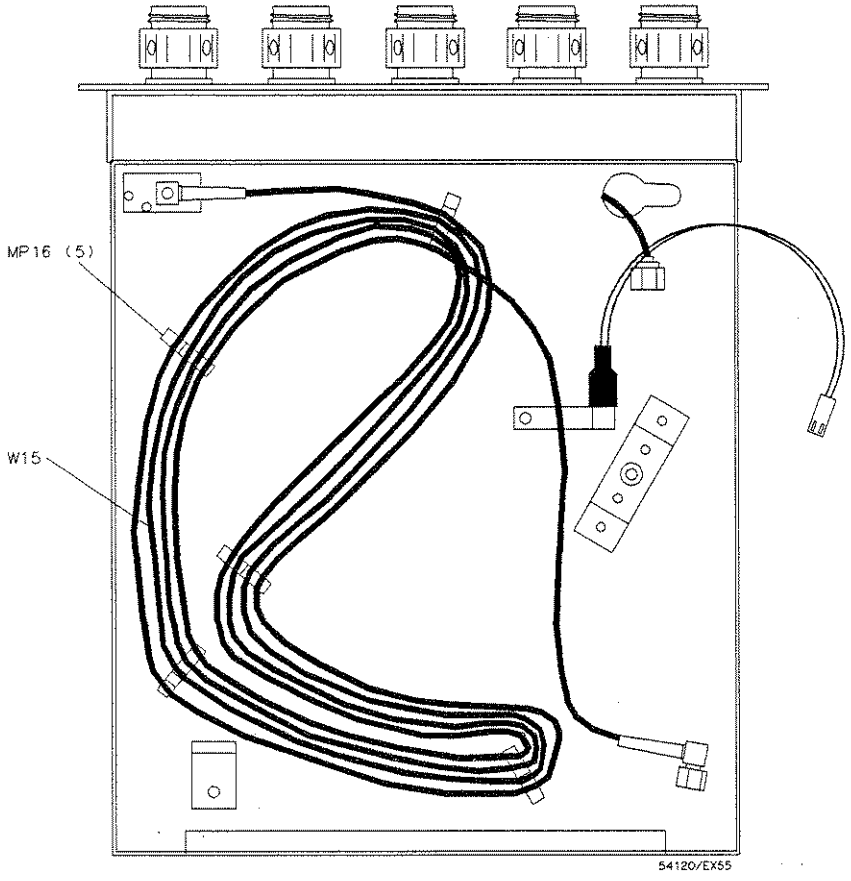


Figure 6A-12. TDR Delay Line Removal

APC 3.5 Center Conductor Replacement

Caution 

The APC 3.5 center conductor assembly connect directly to either a sampler or trigger hybrid input. These inputs are very sensitive to electrostatic damage (ESD). All maintenance should be performed while using an antistatic mat and wrist strap which are supplied with the instrument.

Removal

1. Use antistatic mat with wrist strap to avoid damage to the gallium arsenide samplers, pulse filter, or TDR assemblies.
2. Use a thin 9/16 inch open end wrench (HP part number 8710-1770) to turn brass nut between APC 3.5 connector and front panel counter-clockwise. Refer to figure 6A-13.
3. Remove front portion of APC 3.5 connector from front panel.
4. Remove center conductor assembly from front panel.

Replacement

1. Place center conductor assembly into APC 3.5 connector.
2. Thread APC 3.5 connector onto front panel and tighten with a 9/16" wrench.

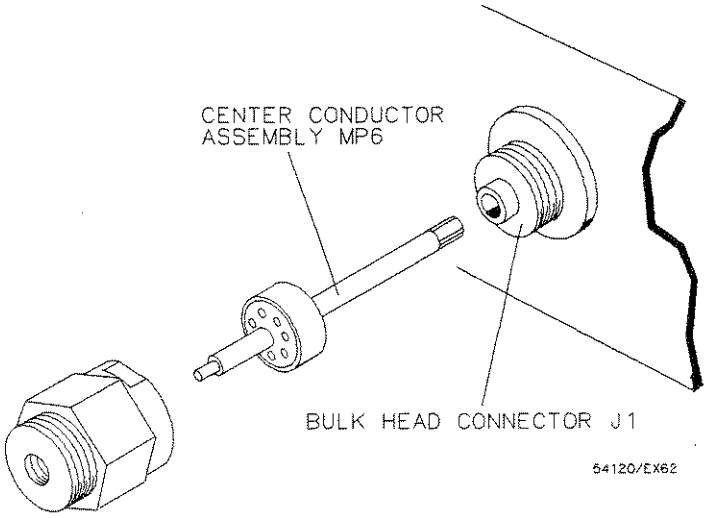


Figure 6A-13. APC 3.5 Center Conductor Removal

APC 3.5 Connector

Caution 

The APC 3.5 center conductor assemblies connect directly to the sampler and trigger hybrid inputs. These inputs are very sensitive to electrostatic damage (ESD). All maintenance should be performed while using an antistatic mat and wrist strap which are supplied with the instrument.

Removal

1. Use antistatic mat with wrist strap to avoid damage to the gallium arsenide samplers, pulse filter, TDR, and trigger hybrid.
2. Disconnect power cable.
3. Remove main deck. Refer to main deck removal.
4. Remove vertical assembly from main deck. Refer to vertical assembly removal.
5. Use a 5/16" open end wrench to unscrew semi-rigid cable from defective APC 3.5 connector. Refer to figure 6A-14.
6. Use a 9/16" open end wrench to unscrew damaged APC 3.5 connector.
7. Remove APC 3.5 connector from front panel.

Replacement

1. Reverse removal procedure to install APC 3.5 connectors. When pushing semi-rigid cables into connectors, a definite slight snap sound will be heard as the cable and connector are seated together. The semi-rigid cables are torqued to 5 in/lbs.

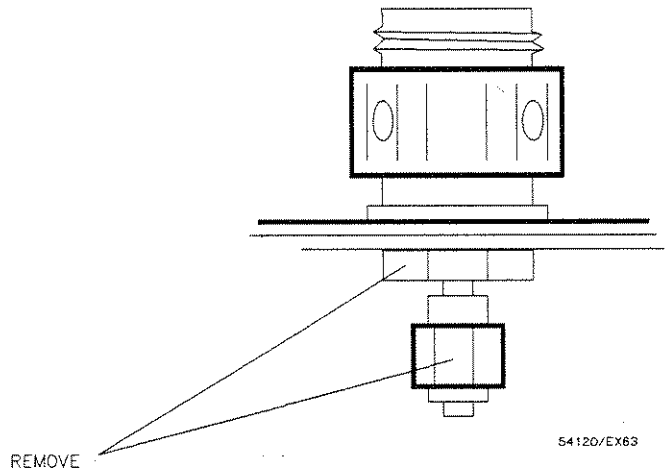


Figure 6A-14. APC 3.5 Connector Removal

Front Panel

Removal

1. Disconnect power cable.
2. Remove main deck. Refer to main deck removal.
3. Remove vertical assembly. Refer to vertical assembly removal.
4. Remove all five APC 3.5 connectors. Refer to APC 3.5 connector removal.
5. Remove two screws from each side of front panel. Refer to figure 6A-15.

Replacement

1. Reverse removal procedure to install front panel.

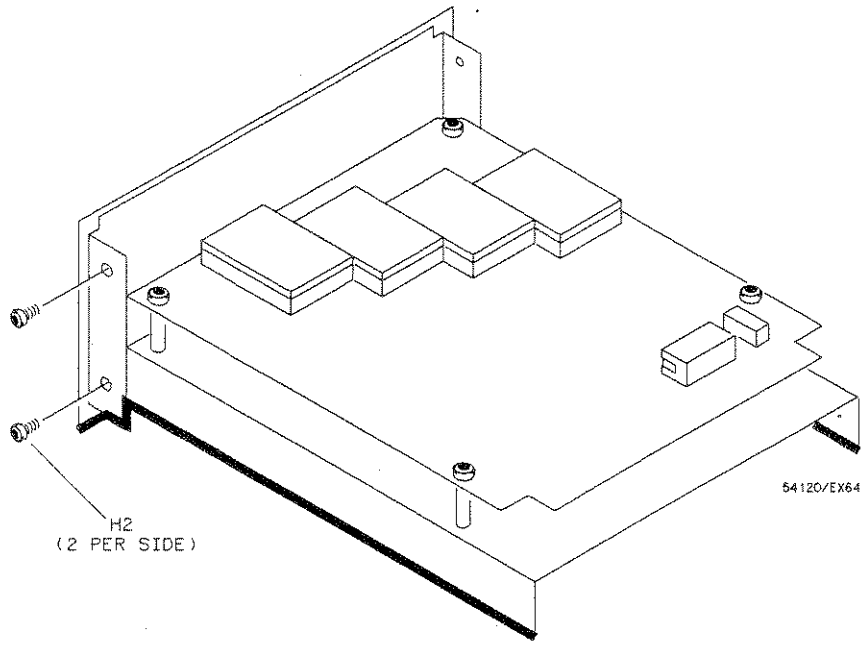


Figure 6A-15. Front Panel Removal

Table Of Contents

Theory

Theory 6B

Introduction

This section is the theory of operation for the HP 54121A Four Channel Test Set. It includes printed circuit assembly (PCA) block diagrams and PCA block level theory of operation. For overall system theory and simplified signal flow, refer to the HP 54120B Mainframe service manual.

Simplified Signal Flow

The following theory refers to figure 6B-1 Simplified Signal Flow Diagram and tracks a signal through the system. The signal flow only refers to channel 1 and the external trigger path. Channels 1-4 operate identically except channel 1 has the TDR hybrid in its input signal path. The TDR is discussed at the end of the simplified signal flow theory.

An acquisition cycle is defined as the sequence of events that must occur in order to acquire a SINGLE data point per enabled channel. It will normally be the case that several acquisition cycles will be required to adequately display a waveform.

The microprocessor (CPU) starts an acquisition cycle by programming the fine delay DAC and the coarse delay counters. The CPU then enables the trigger hybrid. The next external trigger edge which meets the criteria set by the trigger criteria latches will cause the trigger hybrid to output an edge. This edge enables the timebase hybrid to start the fine delay ramp. The fine delay DAC signal sets the starting point for the fine delay ramp. This fine delay ramp represents fine delay, which has a range from 0 to 3.99975 ns. When the fine delay ramp reaches 0 volts, the 250 MHz startable oscillator starts running. The sample pulse generator drive is enabled when all the coarse delay counters reach terminal count. The 250 MHz signal clocks the coarse delay counters on the horizontal assembly. These counters continue recounting to zero which results in the output line toggling at a 7.8 MHz rate. The 7.8 MHz clocks the remainder of the coarse delay counters on the horizontal control assembly. When these counters reach terminal count, they output a signal called terminal count back to the horizontal assembly. This is one of the enable signals for the sample pulse generator drive circuit. The coarse delay counters on the horizontal assembly continue to count until they reach terminal count also.

This terminal count is the last enable for the sample pulse generator drive circuit. With all the coarse delay counters at terminal count, one pulse of the 250 MHz is allowed through the sample pulse generator drive circuit. This circuit places 1 A of current for 1 ns into the sample pulse generator. This causes the sample pulse generator to momentarily turn on the sampler hybrids.

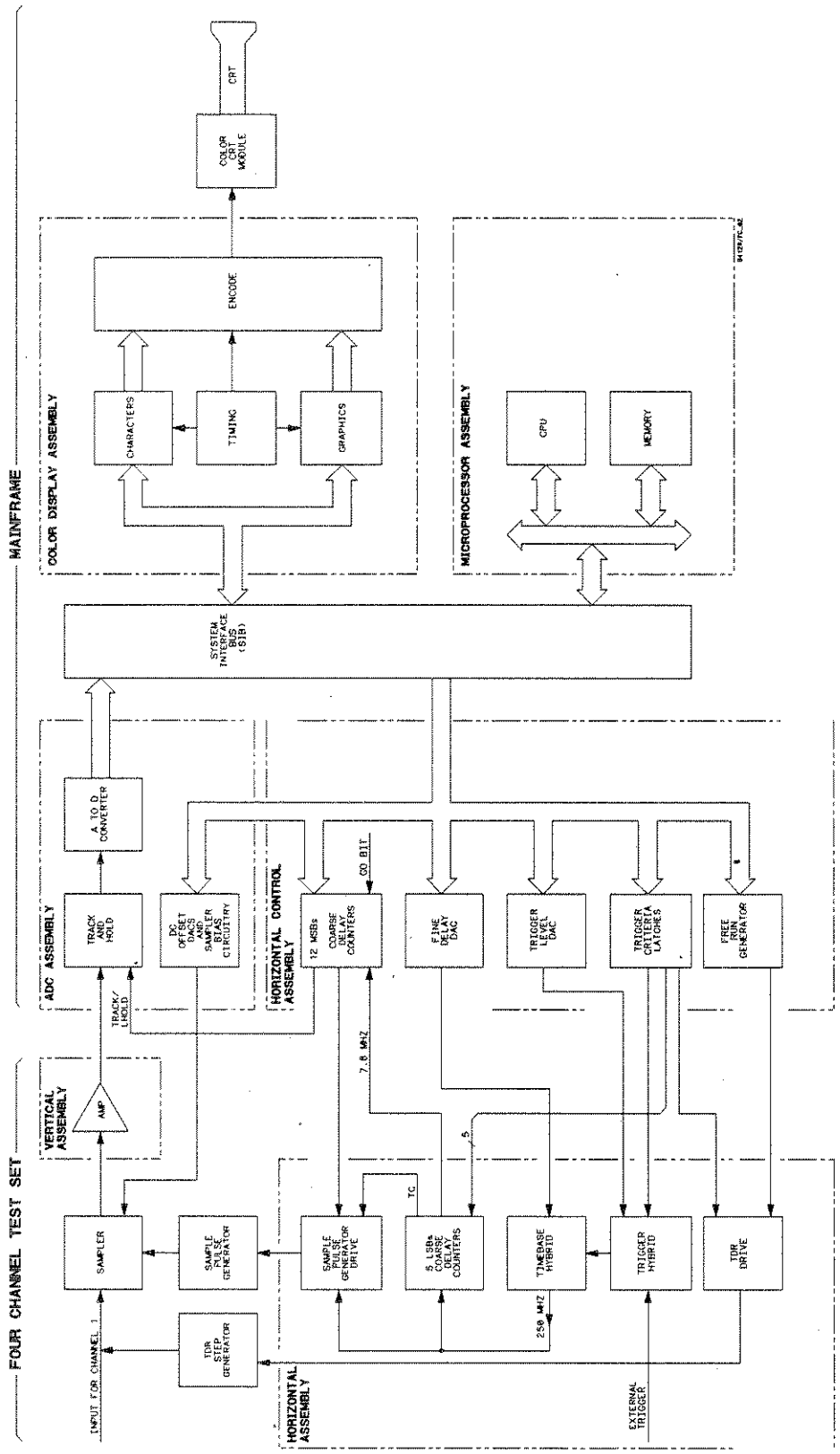


Figure 6B-1. Simplified Signal Flow

The sampler measures the difference between the input signal's present amplitude and the DC offset DAC's level. The difference is amplified and converted to a bipolar pulse. A bipolar pulse is shown in figure 6B-3. It is important to remember that only one data point is digitized for each enabled channel during each acquisition cycle. The bipolar pulse on the vertical assembly represents only the sampled portion of the incoming signal during a very narrow time window of 17 ps.

The track and hold circuit follows the amplitude of the bipolar pulse. When the bipolar pulse reaches peak amplitude, the track and hold circuit holds the peak analog value. The A to D converter converts the track and hold's level to a 12-bit digital word.

The CPU reads the output of the A to D converter and either uses the digital word in waveform math functions or sends it to the color display assembly.

The display assembly sends the digitized input waveform to the graphics section of the display assembly. The graphics and any associated characters are sent to the CRT display module where they are displayed on the CRT. Another acquisition cycle will then be started.

The TDR generates a fast step pulse for TDR applications. When the TDR is disabled, incoming signals pass unaffected through the TDR, except channel 1's bandwidth is lowered slightly. When the TDR is enabled, it outputs a fast edge pulse which splits two ways. First, the TDR pulse is applied to channel 1's sampler input and is digitized as any other incoming signal. Second, the TDR pulse is an output from channel 1's APC 3.5 input connector.

An important point to remember is that external trigger is not used when the TDR is enabled. Circuitry on the horizontal assembly generates the trigger signal when trigger is enabled. If the external trigger signal is left connected it may cause false triggering.

Another important point about this system is that there is no provision for an internal sync pickoff in the samplers. Only an external trigger is used when incoming signals are to be digitized.

Vertical Assembly

The following block level theory of operation refers to the vertical assembly block diagram in figure 6B-2.

TDR

The time domain reflectometry (TDR) step generator is a thru-line current switching circuit. It is used to create a fast step for TDR applications.

Sampler

A pulse from the sample pulse generator momentarily turns the sampler diodes on. The sampler measures the difference between an input signal and dc offset at a specific point in time (approximately 17 ps window) and converts this difference to a differential charge on both IF outputs.

Sampler Bias Network

This circuitry combines the offset, bias and temperature compensation inputs to produce the proper voltages to bias the sampler IF pins. H/LL selects either the high or low bandwidth bias modes.

Feedthrough Compensation Network

When the sampler is turned off, there will be passive feedthrough of the input signal through the sampler by parasitic capacitive and resistive coupling. The circuit corrects for this passive feedthrough of the sampler diodes to a bandwidth greater than the matched filter's bandwidth.

Charge Sensitive Amps

The charge sensitive amps measure the differential charge on the IF outputs and converts this to differential tail pulses with time constants of approximately 100 µs.

Summation Amp

The summation amp combines the differential tail pulses from the charge sensitive amps into a single-ended tail pulse. It also subtracts effects of changes in dc offset signal on the charge sensitive amps.

Amp And Matched Filter

The matched filter converts and amplifies the tail pulse from the summation amp and converts the tail pulse to a bipolar pulse which drives the track and hold circuitry on the ADC assembly.

Mnemonics	Definition
CC1	Capacitive Compensation for channel 1
HB1	High Bandwidth adjust for channel 1
LL/H	Low enables Low bandwidth bias adjust and a High enables High bandwidth bias adjust
LB1	Low Bandwidth bias adjust for channel 1
OG1	Offset Gain adjust for channel 1
RC1	Resistive Compensation for channel 1
VHB	High Bandwidth bias enable
VLB	Low Bandwidth bias enable
V Temp	Temperature compensation voltage from horizontal assembly
10.000	V Precise 10 volts from horizontal assembly

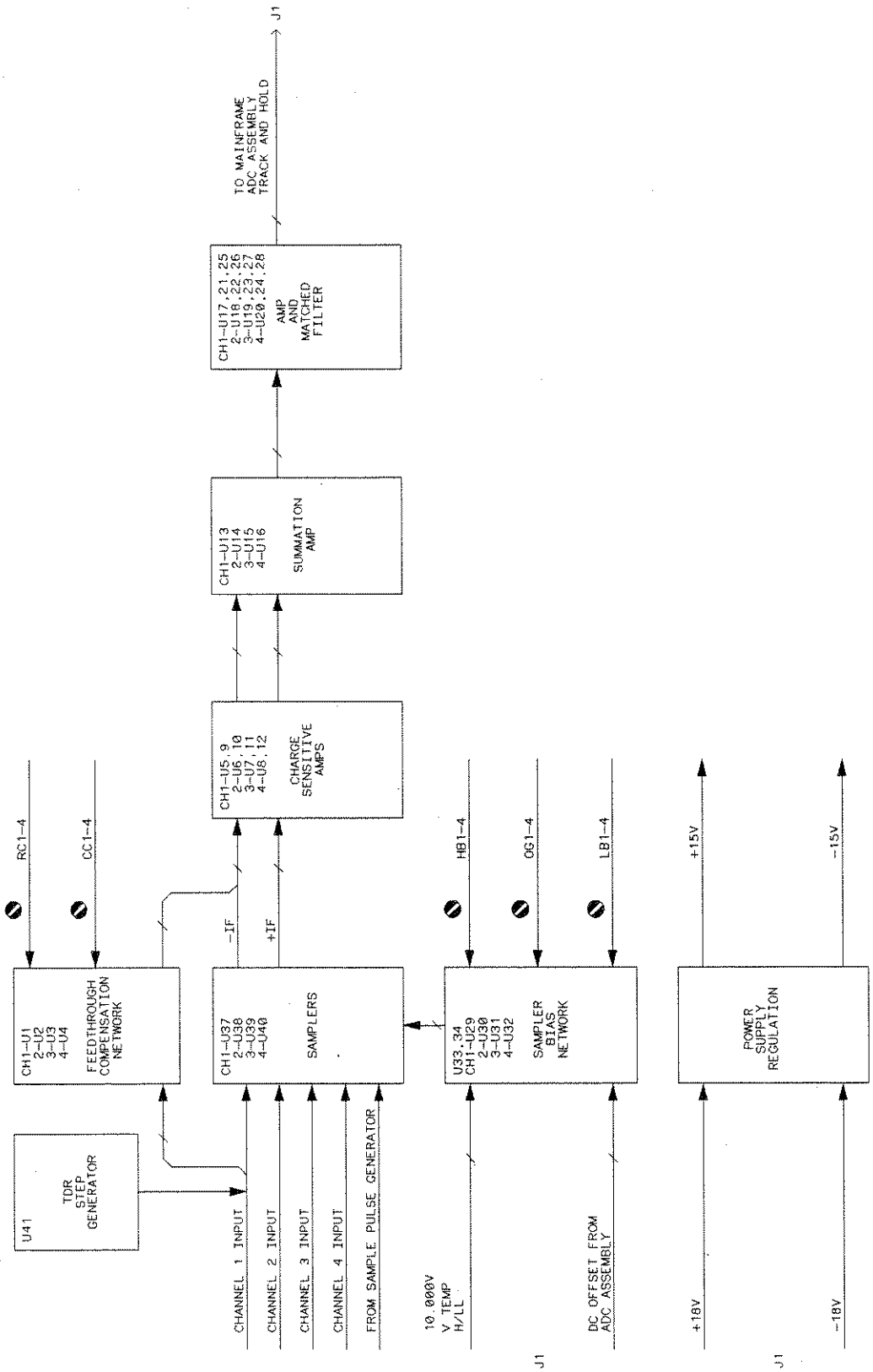


Figure 6B-2. Vertical Assembly Block Diagram

Horizontal Assembly

The following block level theory of operation refers to the horizontal assembly block diagram in figure 6B-3.

Trigger Hybrid

When the TDR is disabled, the trigger enable line enables the trigger hybrid. The next external trigger edge which meets the criteria set up by the trigger criteria signals will cause the trigger hybrid to output an edge. The trigger criteria signals are: trigger slope select, high frequency reject, hysteresis on or off, and a separate signal called trigger level. Trigger level sets a threshold which the incoming trigger signal must cross for a trigger to occur. When the trigger hybrid triggers, it outputs an edge to the timebase hybrid.

Trigger Source For TDR Mode

When the TDR is enabled, external trigger pulses are inhibited from causing U1 to trigger. The CPU sets the trigger level high enough so that any incoming external trigger pulses would not be expected to cross the trigger level threshold. This keeps any external trigger pulses from causing the trigger hybrid to trigger. It is essential that when the TDR is enabled all external trigger sources be disconnected from the instrument, otherwise the instrument will not trigger properly and will appear inoperative. When the trigger enable line enables U2 and U3, the next positive edge of freerun clock will cause the trigger hybrid to trigger. The trigger hybrid will output an edge to the timebase hybrid.

TDR Drive

When the TDR OFF/LON line is low, U4 and Q2 allow the freerun clock signal to drive the TDR on and off at the freerun clock rate. The freerun clock rate is determined by the freerun rate selected in the front-panel timebase menu.

Timebase Hybrid

Fine delay sets the starting point for the fine delay ramp. This fine delay ramp represents a fine delay range from 0 to 3.99975 ns. When the timebase hybrid receives the trigger edge from the trigger hybrid, it starts the fine delay ramp. When the fine delay ramp reaches 0 volts, the 250 MHz startable oscillator inside the timebase hybrid will start running. The timebase hybrid outputs 250 MHz to the sample pulse generator drive circuitry and to the coarse delay counters on the horizontal board.

Coarse Delay Counters

The part of the coarse delay counters, which counts the 5 LSB's of the 17-bit coarse delay word is on the horizontal assembly. The 250 MHz signal from the timebase hybrid clocks these counters. Each time the 5 LSBs are counted and the counters roll over, the output of the counter's last stage toggles at a rate of 7.8 MHz (250 MHz divided by five counter stages is 7.8 MHz). The 7.8 MHz clocks the rest of the coarse delay counters which are on the horizontal control assembly. They count the 12 MSBs of the coarse delay word. Eventually all the counters reach terminal count and pull the LTC2 line to a logic low level. The next time the 5 LSB counters reach terminal count, they pull their own terminal count line to a logic low level. With all the coarse delay counters momentarily reaching terminal count at the same time, the sample pulse drive circuitry will pass one cycle of the 250 MHz.

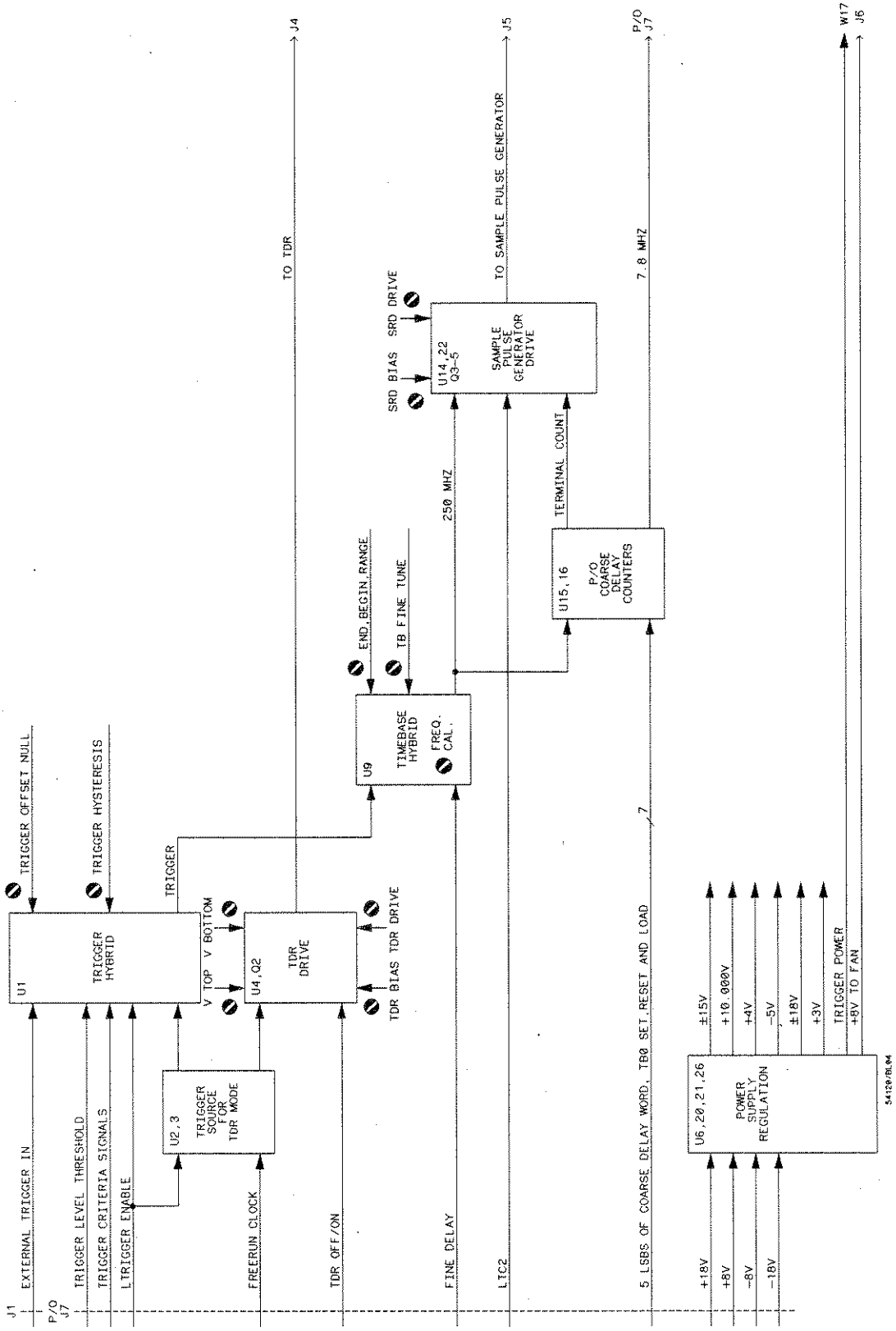


Figure 6B-3. Horizontal Assembly Block Diagram

Sample Pulse Generator Drive

When all 17 bits of the coarse delay word have reached terminal count, the sample pulse generator drive circuitry will allow one pulse of the 250 MHz to pass. The sample pulse generator drive circuitry places 1 amp of current for 1 ns in the sample pulse generator. The sample pulse generator outputs a fast edge pulse (rise time of about 50 ps), which momentarily turns on all four samplers at the same time.

Mnemonics	Definition
HF REJECT	Trigger High Frequency Reject
LSB	Least Significant Bit
LTC2	Low Terminal Count line 2
MSB	Most Significant Bit
NEG/LPOS	Trigger Slope Select Negative or Positive
SRD	Step Recovery Diode (part of sample pulse generator)
TB0 SET	Timebase Bit 0 Set (TB0-4 are the 5 LSB's of the)
TB0 RESET	Timebase Bit 0 Reset (17 bit coarse delay word)
TB LOAD	Timebase Bit Load
TB1-4	Timebase Bits 1-4
TDR OFF/LON	Turns TDR Generator Off and On
LENABLE/RESET	Trigger Low Enable/Reset

Table of Contents

Troubleshooting

Troubleshooting 6C

Introduction

This section contains internal diagnostics (Self-Tests) and troubleshooting information for fault location to the PC assembly level. Reading section 6B, theory of operation, and section 6D, troubleshooting, in the HP 54120B Service Manual will help in understanding this section.

Note

This section assumes you have already performed all troubleshooting procedures in the HP 54120B Service Manual section 6D.

Safety Considerations

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

Warning

Maintenance described in this section is performed with power supplied to the instrument and with protective covers removed. Maintenance should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the power should be removed. Read the Safety Summary in the front of this manual.

Caution

The HP 54121A is very sensitive to static discharge. Failure to observe proper antistatic methods may result in damage to the gallium arsenide samplers. All maintenance or operation should be performed while using an antistatic mat and wrist strap, which are supplied with the instrument.

Caution

Do not remove or replace any of the circuit board assemblies in this instrument unless instrument power is removed. The boards contain components which may be damaged if the board is removed or replaced when instrument power is applied.

Recommended Test Equipment

Equipment recommended for service is listed in section 1, table 1-1. Any equipment that satisfies the critical specifications stated in the table may be substituted.

Logic Families Used

Two different logic families are used in the HP 54121A, ECL and EECL. The horizontal assembly used ECL and EECL, and the vertical assembly uses EECL.

- ECL ranges from -0.9 V to -1.7 V and is used more often in the data acquisition circuitry where speed is of great importance.
- EECL ranges from 0 V to -0.8 V and is used on the outputs of many custom IC's.

Because the ECL high and the EECL low share about the same voltage level, it's possible that a misinterpretation of a logic level could occur. Extra care should be taken when dealing with these levels. Typical monitor oscilloscope offset levels are -1.3 V for ECL and -0.4 V for EECL.

Diagnostic Overview

This section is divided into two sub-sections for ease of use, internal diagnostic loop tests and extended service test. Start the diagnostics by first verifying the failure mode. The data acquisition troubleshooting will refer to paragraphs in the extended service tests.

Data Acquisition Troubleshooting

Data acquisition troubleshooting involves three processes: preliminary investigation, internal diagnostic loop test evaluation, and extended service test evaluation.

Note 

The HP 54121A contains gallium arsenide samplers that are very sensitive to electrostatic discharge (ESD) damage. The samplers may be the cause of many data acquisition problems. Before analyzing other data acquisition failures, the extended service sampler test should be run first.

Preliminary Investigation

Preliminary investigation involves three processes: determining which data acquisition assemblies are operating properly, making an informed decision on which assembly or assemblies might be causing the fault, checking some common failure mechanisms. To achieve these results loop test failures are compared against the assemblies which might cause the failure, loop failure patterns are compared against a known set of loop failure patterns, and the functional block diagram is used to decide the fault's probable location.

Internal Diagnostic Loop Test

Internal diagnostic loop tests evaluate why a particular loop failed. The preliminary investigation may indicate which loop to evaluate first; however, the lowest numbered loop is usually evaluated first. When evaluating loop failures, first decide why this loop failed and why others may have passed. This will often indicate the possible failing assembly. Second, use the loop failure status codes to indicate why this loop is failing. Third, probe specific interconnect points to verify which assembly is faulty.

Extended Service Test

Extended service tests execute routines which check if assemblies are supplying the correct signals to other assemblies. This may indicate why a loop failed and the probable faulty assembly. Executing all the extended service tests would take more time than an analysis of the internal individual diagnostic loop tests. There are two reasons for the extended service tests. First, for persons familiar with the oscilloscope it may be a troubleshooting short cut because they sometimes can predict which extended service test to execute for particular failure symptoms. Second, internal diagnostic loop tests do not cover all instrument failures.

Analyzing Failures

1. Analyze the functional block diagram and the simplified assembly interconnect diagram, figures 6C-1 and 6C-2, to determine which assemblies could cause the failure.

2. Analyze the failing loop tests and refer to tables 6C-1 and 6C-2 to determine which assembly might be failing.

3. Eliminate working assemblies and eliminate assemblies that appear to fail but are failing because of a different problem.

4. Refer to the following troubleshooting hints.

Not Triggering

This could be caused by the trigger hybrid, timebase hybrid, A/D assembly, pulse filter, interconnecting ribbon cables, horizontal assembly, or horizontal control assembly.

Vertical Problems

This could be caused by the sampler, vertical assembly, A/D assembly, or interconnecting cables.

Horizontal Problems

This could be caused by the trigger hybrid, horizontal assembly, horizontal control assembly, or interconnecting cables.

Multiple Channel Failures

If the oscilloscope is triggering and the horizontal is working, the problem could be the A/D assembly. If the oscilloscope is not triggering, the fault may be the trigger hybrid, horizontal assembly, horizontal control assembly, or interconnecting cables.

One Channel Failure

This could be caused by the sampler, vertical assembly, A/D assembly, umbilical cable, pulse filter, or semi-rigid cables.

Channel 1 Failure Only

In addition to the single channel failures listed above, possibly the TDR step generator.

TDR Problem

This could be caused by the TDR step generator, horizontal assembly, horizontal control assembly, umbilical cable, and two ribbon cables which connect the umbilical cable to the vertical and horizontal assemblies.

One Channel Offset Problem

Probably caused by the sampler hybrid. Other failures may be the A/D assembly, vertical assembly, umbilical cable, or interconnecting cables.

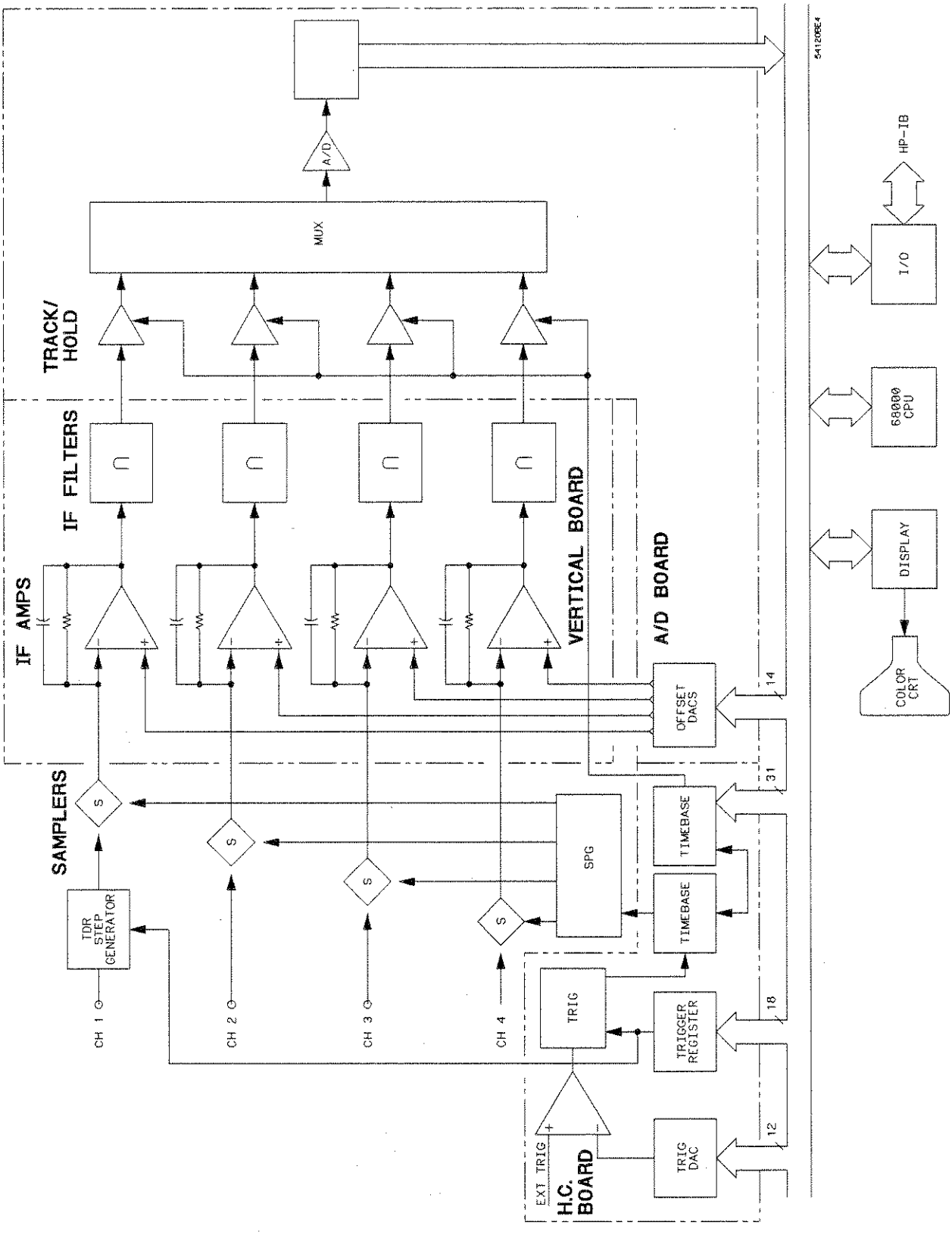


Figure 6C-1. HP 54120 System Functional Block Diagram

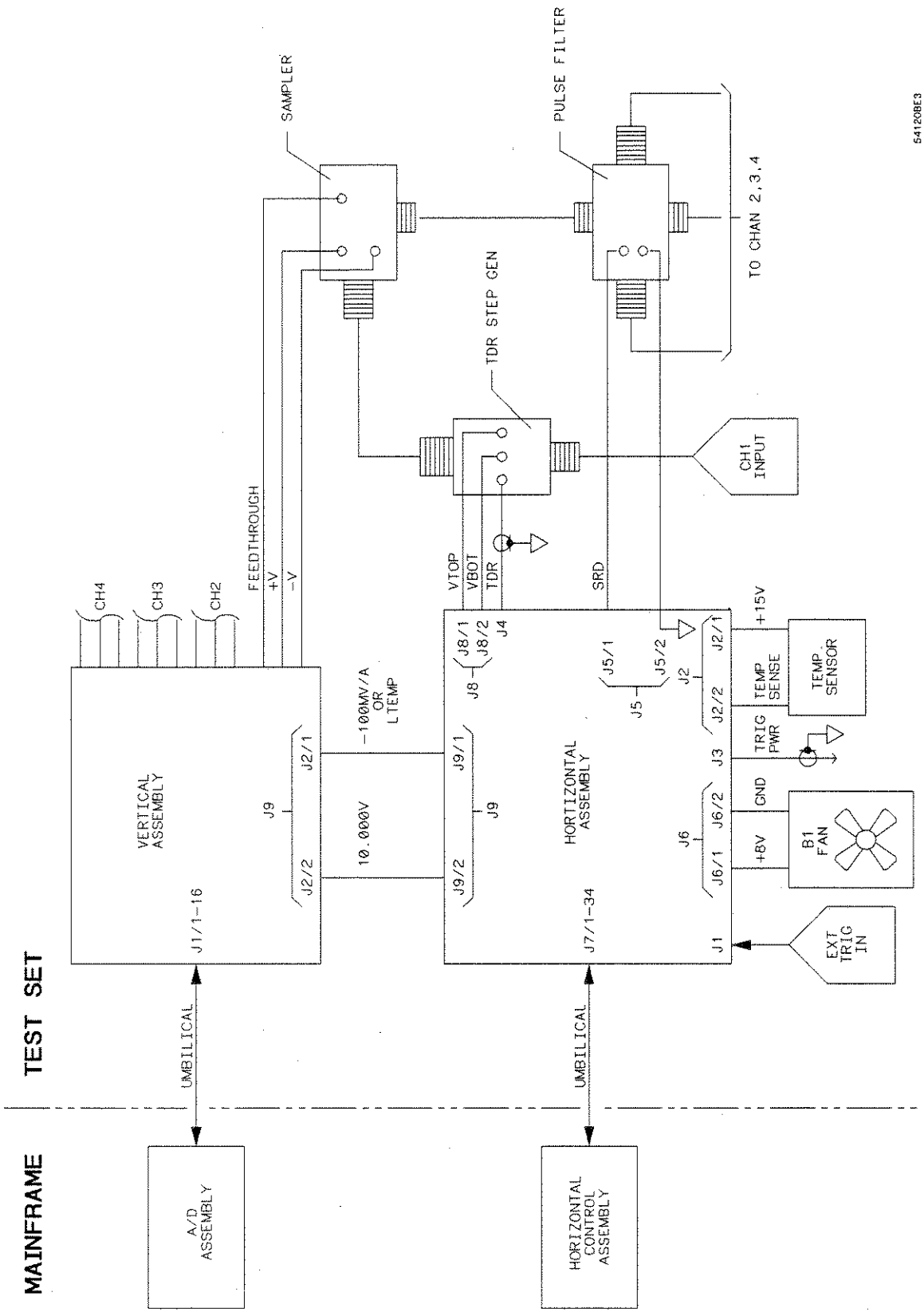


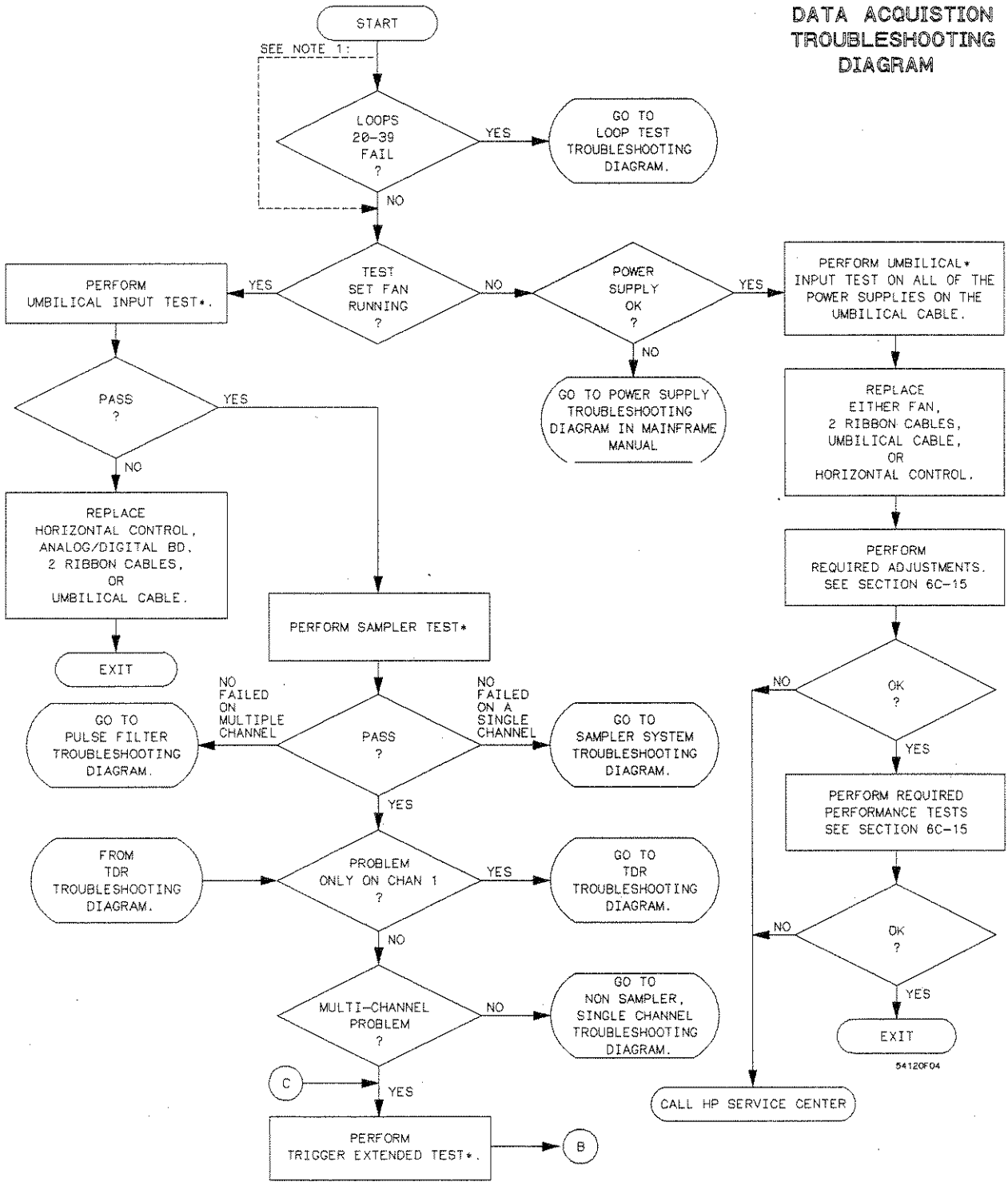
Figure 6C-2. Simplified Signal Interconnect Diagram

Table 6C-1. Which Assemblies are Tested By Loop Tests

Assembly	Loop No.
TDR	39
A/D	16, 28-39
Horizontal control	17, 20, 22-30
Vertical	35-38
Horizontal	20, 22-29
Samplers	31-39
Pulse filter	31-39
Trigger hybrid	20, 21-38
Display	5-9, 41, 42
I/O	10-15, 43
CPU	0-4, 40
RPG	15

Table 6C-2. Adjustments That May Cause Loop Failures

Loop No.	Adjustment
1-17	None
18-19	Loop not used
20	Hysteresis
21	None
22-25	Hysteresis (loop 24 - trigger offset also)
26	None
27-30	Hysteresis (loop 30 - offset gain also)
31-34	SRD Drive and Sampler Bias, Hysteresis
35	SRD Drive and Sampler Bias, Hysteresis, LB1, HB1
36	SRD Drive and Sampler Bias, Hysteresis, LB2, HB2
37	SRD Drive and Sampler Bias, Hysteresis, LB3, HB3
38	SRD Drive and Sampler Bias, Hysteresis, LB4, HB4
39	SRD Drive and Sampler Bias, V top and bottom
40-43	None



* SEE EXTENDED SERVICE TEST SECTION
NOTE 1: DEPENDING ON THE FAILURE AND THE EXPERIENCE OF THE TECHNICIAN, THE DECISION BOX MAY BE SKIPPED.

Figure 6C-3. Data Acquisition Troubleshooting Flowchart 1

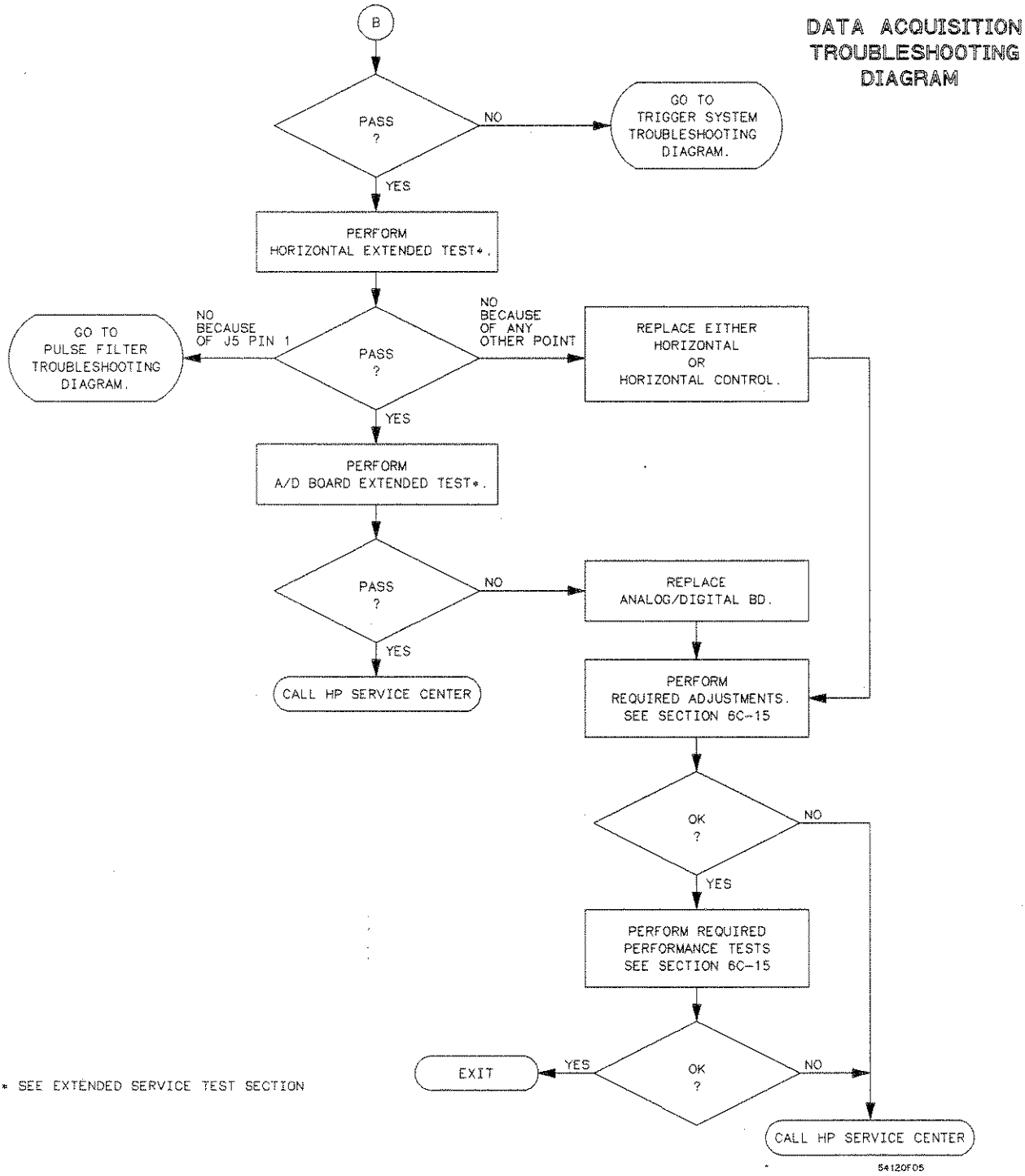


Figure 6C-4. Data Acquisition Troubleshooting Flowchart 2

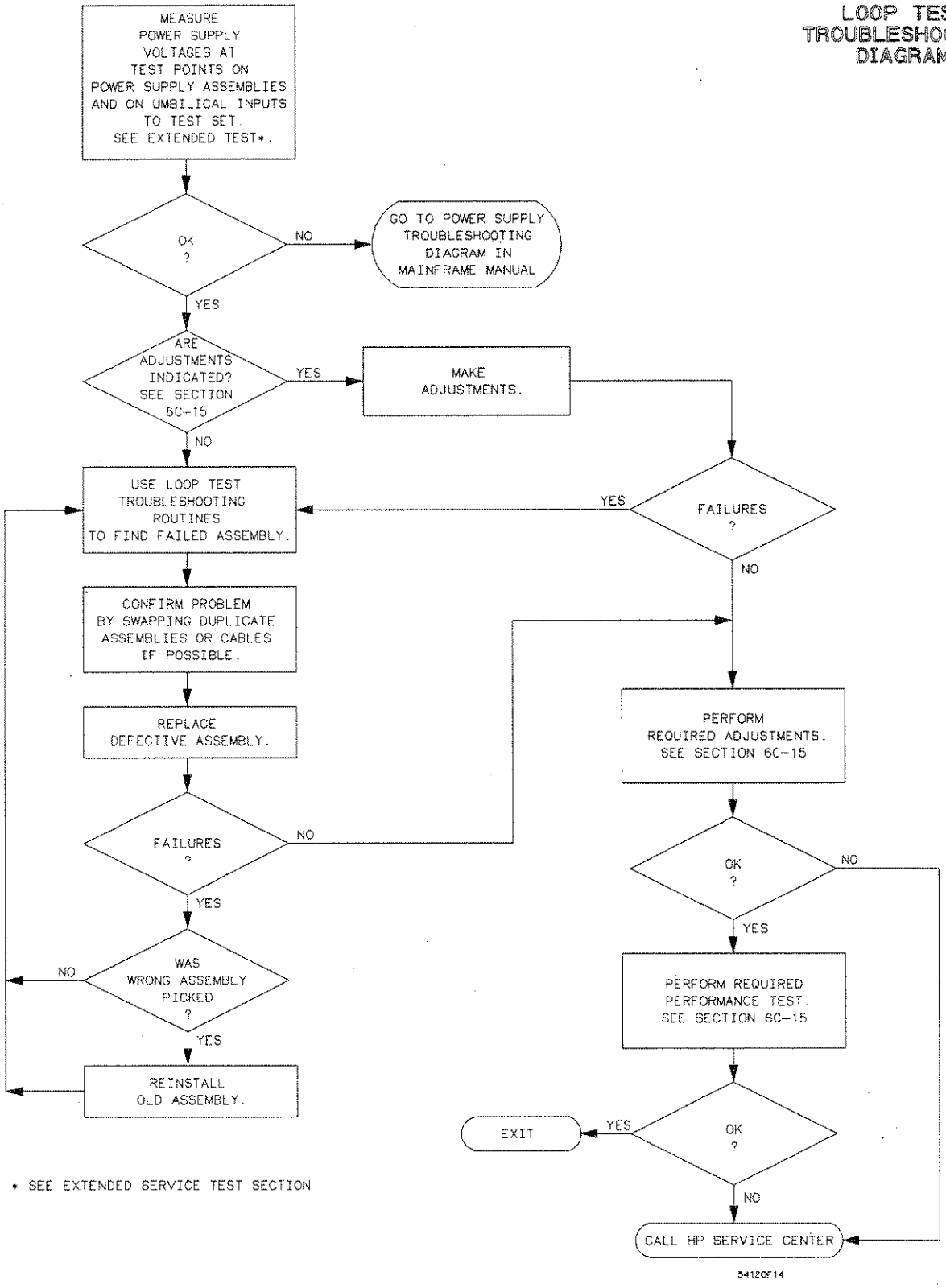


Figure 6C-5. Loop Test Troubleshooting Flowchart

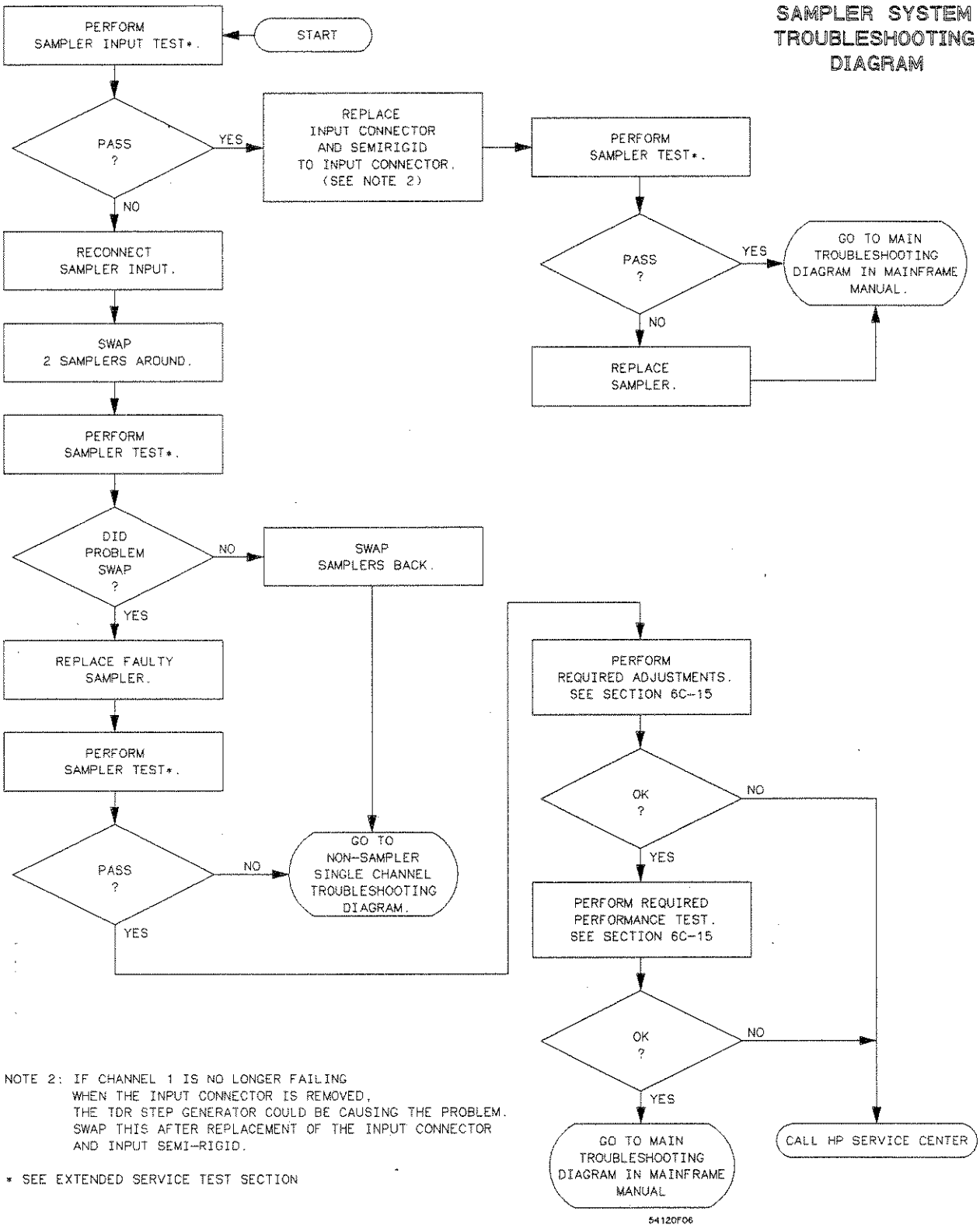
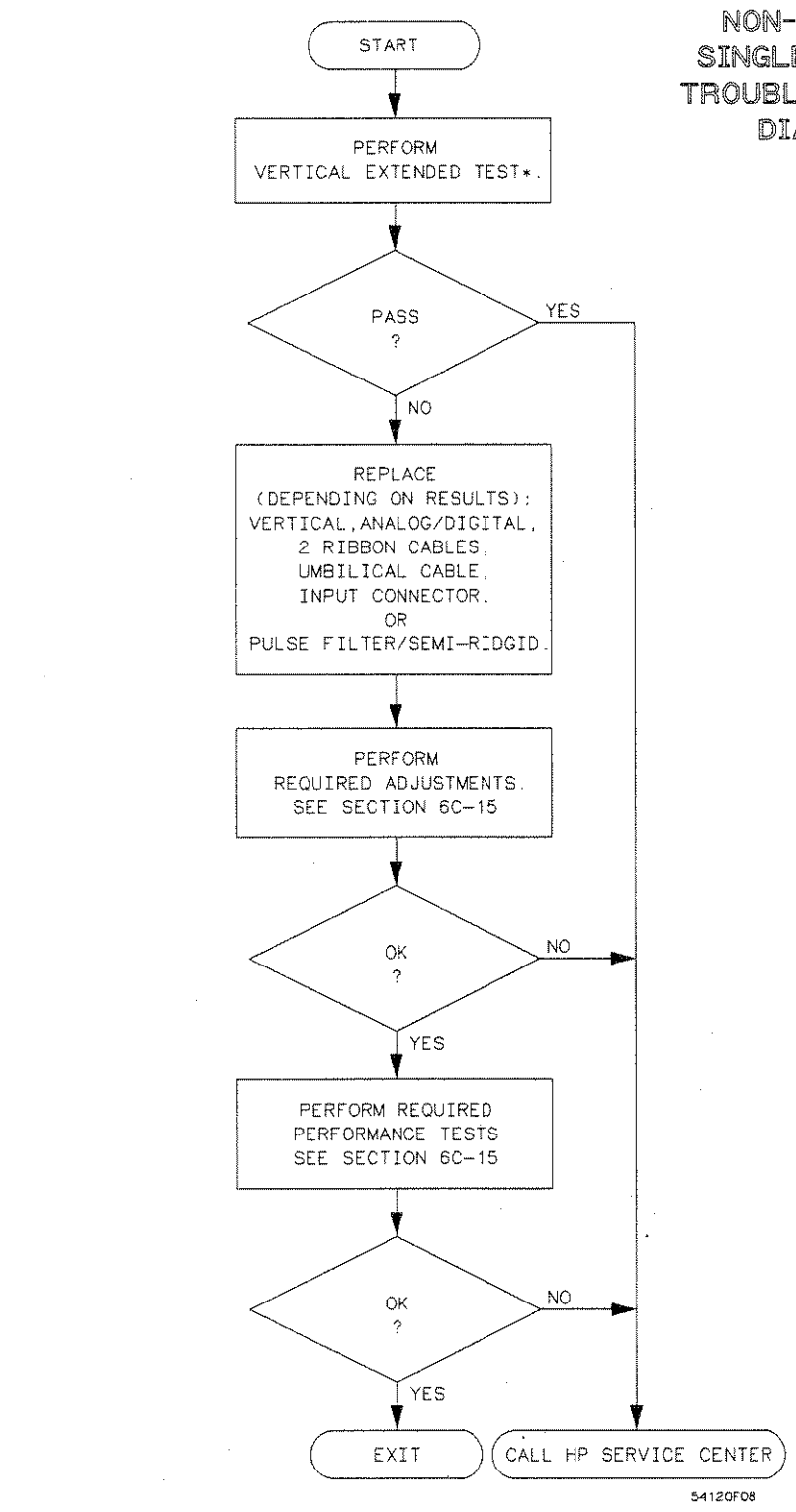


Figure 6C-6. Sampler Troubleshooting Flowchart



* SEE EXTENDED SERVICE TEST SECTION

Figure 6C-7. Single Channel Troubleshooting Flowchart

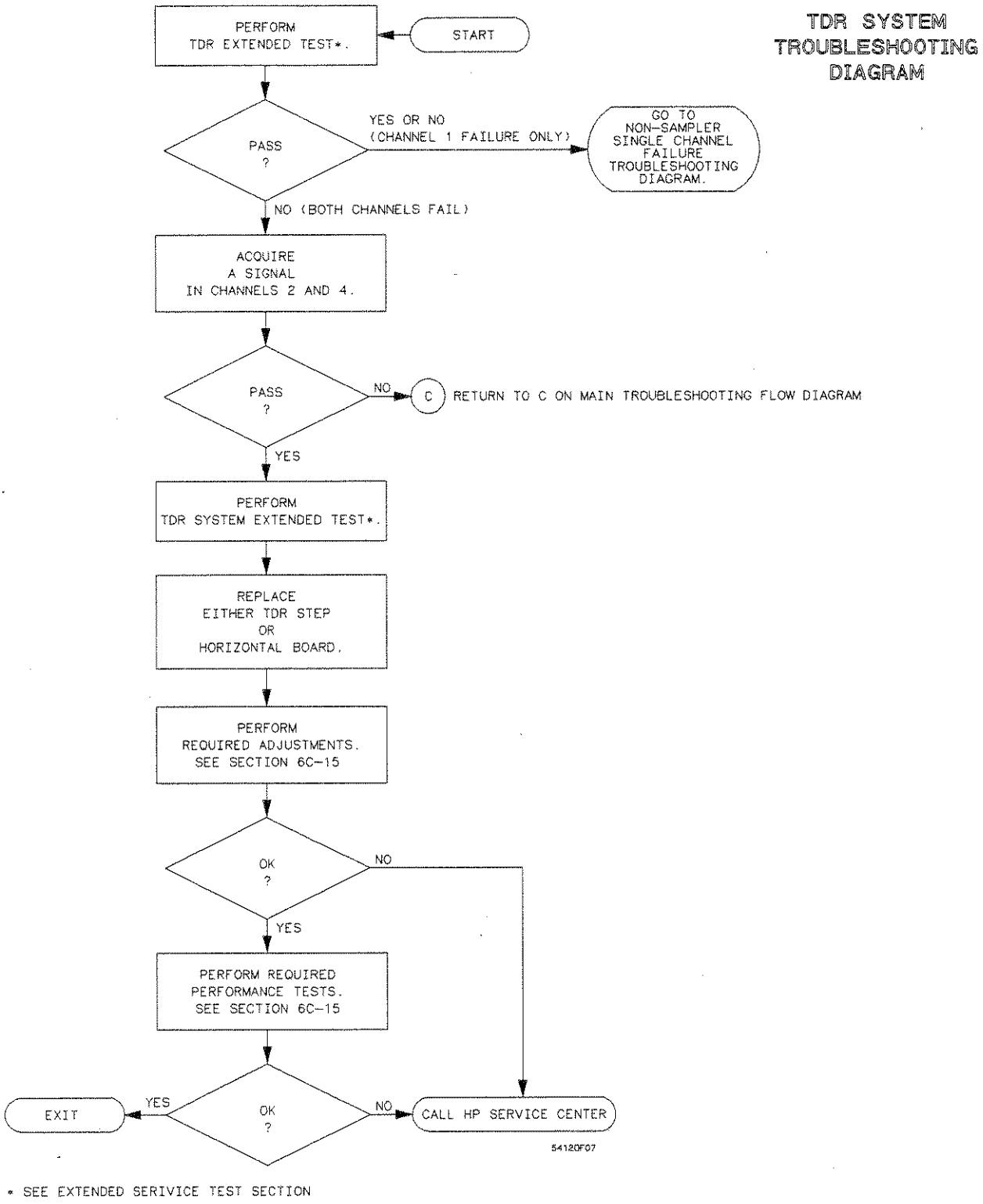


Figure 6C-8. TDR Troubleshooting Flowchart

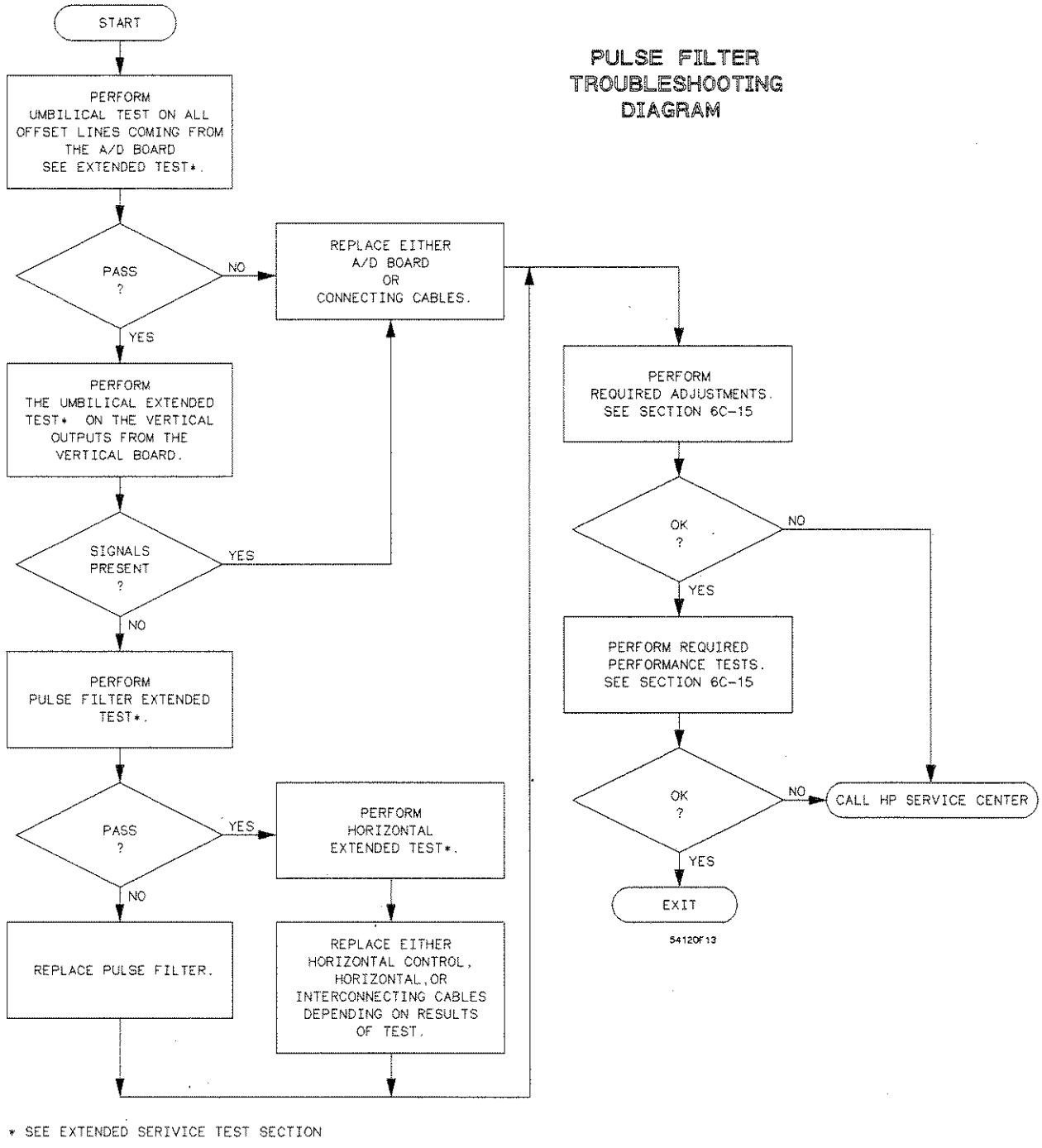


Figure 6C-9. Pulse Filter Troubleshooting Flowchart

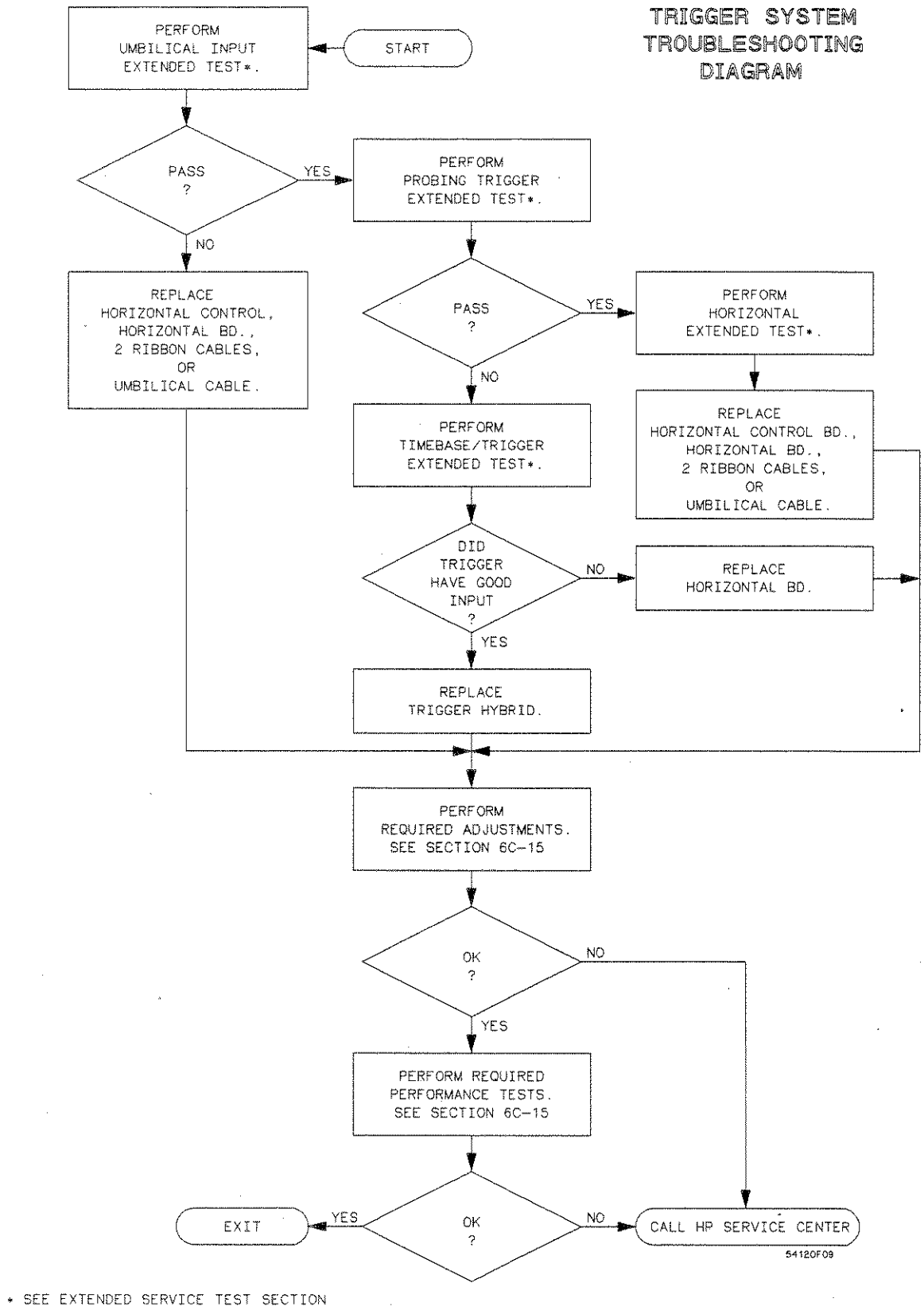


Figure 6C-10. Trigger Troubleshooting Flowchart

After Repairs are Made

After the faulty assembly has been found, the following three tables should be used. Table 6C-3 cross references which adjustments to perform after replacing an assembly. Table 6C-4 cross references which performance tests to check after doing the adjustments. Table 6C-5 cross references which performance tests to perform after replacing an assembly.

Table 6C-3. Adjustments to Check After Assembly Repairs

Assembly Replaced	Adjustments that should be performed
A/D Assembly	10 V reference, Software calibration
Horizontal Control	Delta Current, Software calibration
Horizontal Assembly	All horizontal adjustments, vertical adjustments, software calibration
Vertical Assembly	LB1-4, HB1-4, OG1-4, RC1-4, CC1-4, Software calibration
Sampler	LB, HB, OG, RC, CC, and Softcal (only on channel where sampler was replaced)
TDR Step Generator	TDR Bias and Drive, V top and bottom, Software calibration
Pulse Filter	SRD Drive and Bias, Sampler Bias, Offset Gain, vertical software calibration
Display Assembly	No adjustments need to be performed
I/O	Software calibration
CPU	Software calibration
Color CRT Assembly	No adjustments need to be performed
Trigger Hybrid	Trigger hysteresis and offset null

Table 6C-4. Performance Tests to Check after Adjustments

Adjustment Made	Performance Test to Perform
Power Supply	None
Delta Current	Timebase accuracy
10 V reference	dc measurement accuracy
Range	Timebase accuracy
SRD	Bandwidth, dc measurement accuracy
Frequency, END, 4 ns cal	Timebase accuracy
Sampler Bias	Adjusted channel only: bandwidth, dc measurement accuracy
TDR	TDR
Feedthrough compensation	Adjusted channel only: bandwidth, dc measurement accuracy
Trigger	Trigger sensitivity, jitter
Channel Skew Cals	None
Vertical Vertical Cal	None
Display	Color confidence test

Table 6C-5. Performance Tests to Check after Repairs

Assembly Replaced	Performance Tests That Should Be Performed
Vertical	Bandwidth, dc Measurement Accuracy, Input Reflection on channels only
A/D	Bandwidth, dc Voltage Measurement Accuracy
Horizontal	Timebase Accuracy, Input Reflection on external trigger input only, Trigger Sensitivity, Jitter, TDR
Horizontal Control	Timebase Accuracy
Sampler	Bandwidth, dc Voltage Measurement Accuracy, Input Reflection, Jitter (perform these tests on channel with replaced sampler)
TDR Step Generator	TDR
Pulse Filter	Jitter
Trigger Hybrid	Input Reflection on external trigger input only
CPU	None
I/O	None
Display	Color Confidence Test
Color CRT Assembly	Color Confidence Test

Table 6C-6. Adjustment's Effect on Displayed Performance.

Several adjustments directly influence the performance of the waveform displayed on the screen. The followingis a list of common symptoms which are caused by misadjustments. Many adjustments interact with other adjustments and should not be varied without first referring to the description of each adjustment.

Symptom	Adjustment to check
Unstable out of specification timebase measurements	Range
Stable out of specification timebase measurements	Frequency
Discontinuites on sine waves >250 MHz	END and 4 ns cal
TDR levels not 0 V and 200 mV	TDR top and bottom
TDR overshoot not between 2.5% and 3.5%	TDR bias and drive
TDR pulse response not flat	TDR bias and drive
Channel to channel skew off	Timebase software calibration
Gain difference between the 12.4 GHz and 20 GHz or between persistence and average modes	Vertical software calibration
Minimum trigger sensitivity >1 division	Trigger
Trigger offset problems	Trigger
Not triggering at center screen (remember there is always 16 ns minimum delay)	Trigger
Faulty color purity	Color monitor
Faulty contrast or brightness	Front panel display controls
Faulty low frequency square wave response	Feedthrough compensation
Faulty gain tracking between 12.4 GHz and 20 GHz bandwidth modes	Sampler bias
Loops 31-38 failing	Sampler bias

Table 6C-7. Loops Affected by Hardware Failures

Hardware	Loop	Status Line
A to D converter on A/D assembly	28	STS 1 = -4
	29	
	30	
	31-34	STS = -4, STS 3 = -4
	35-38	STS = -5, STS 3 = -6
A/D assembly output wrong bit pattern	39	STS = -6, STS 4 = 0
Offset DAC on A/D assembly Chan 1	28	STS = 2, read pattern
Offset DAC on A/D assembly Chan 2	31, 35	STS = -4, -5, STS 3 = -4, -5
Offset DAC on A/D assembly Chan 3	32, 36	STS = -4, -5, STS 3 = -4, -5
Offset DAC on A/D assembly Chan 4	33, 37	STS = -4, -5, STS 3 = -4, -5
Bandwidth bias	34, 38	STS = -4, -5, STS 3 = -4, -5
Sampler Chan 1	35-38	STS 1 = -4
Sampler Chan 2	31, 35, 39	STS 1 = -4
Sampler Chan 3	32, 36	
Sampler Chan 4	33, 37	
SRD not generating a pulse	34, 38	
	31, 34-38	STS 1, 3 = -4, STS 2, 4 = 0
TDR pulse not getting to samplers	39	STS 1 = -5, STS 4 = 0
Timebase on horizontal or horizontal control assemblies	39	STS 1 = -5, STS 4 = 0
	20, 24, 27, 28, 31-39	STS 1 = -2
	22, 26	STS 1 = -3
	23	STS 1 = -3, STS 2 = -3
	25	STS 1 = -2, STS 2 = -2
	29	STS 1 = 8002H, STS 2-4 = 8002H
	30	STS 1 = 8002H
Freerun clock not being generated	26	STS 1 = -3
	39	STS 1 = -2
Trigger hybrid slope not changing	20, 27, 28, 31-38	STS 1 = -2
	23	STS 1 = -3 or STS 2 = -3
	25	STS 1 = -2 or STS 2 = -2
	29	STS 1 = 8002H, STS 2-4 = 8002H
	30	STS 1 - 8002H
Trigger level DAC output not changing or trigger hybrid not responding to a change in trigger level	22	STS 1 = -3
	23	STS 1 = -3, STS 2 = -3
	24, 27	STS 1 = -2
RPG cannot be reset	15	STS 1 = -1
Static RAM's	2	Chip problems
	40	Address line problem
Graphics RAM's	8	Chip problems
	41	Address line problem
I/O RAM's	11	Chip problems
	43	Address line problem
Priority RAM's	9	Chip problems
	42	Address line problem
Character RAM's.	7	Chip problems

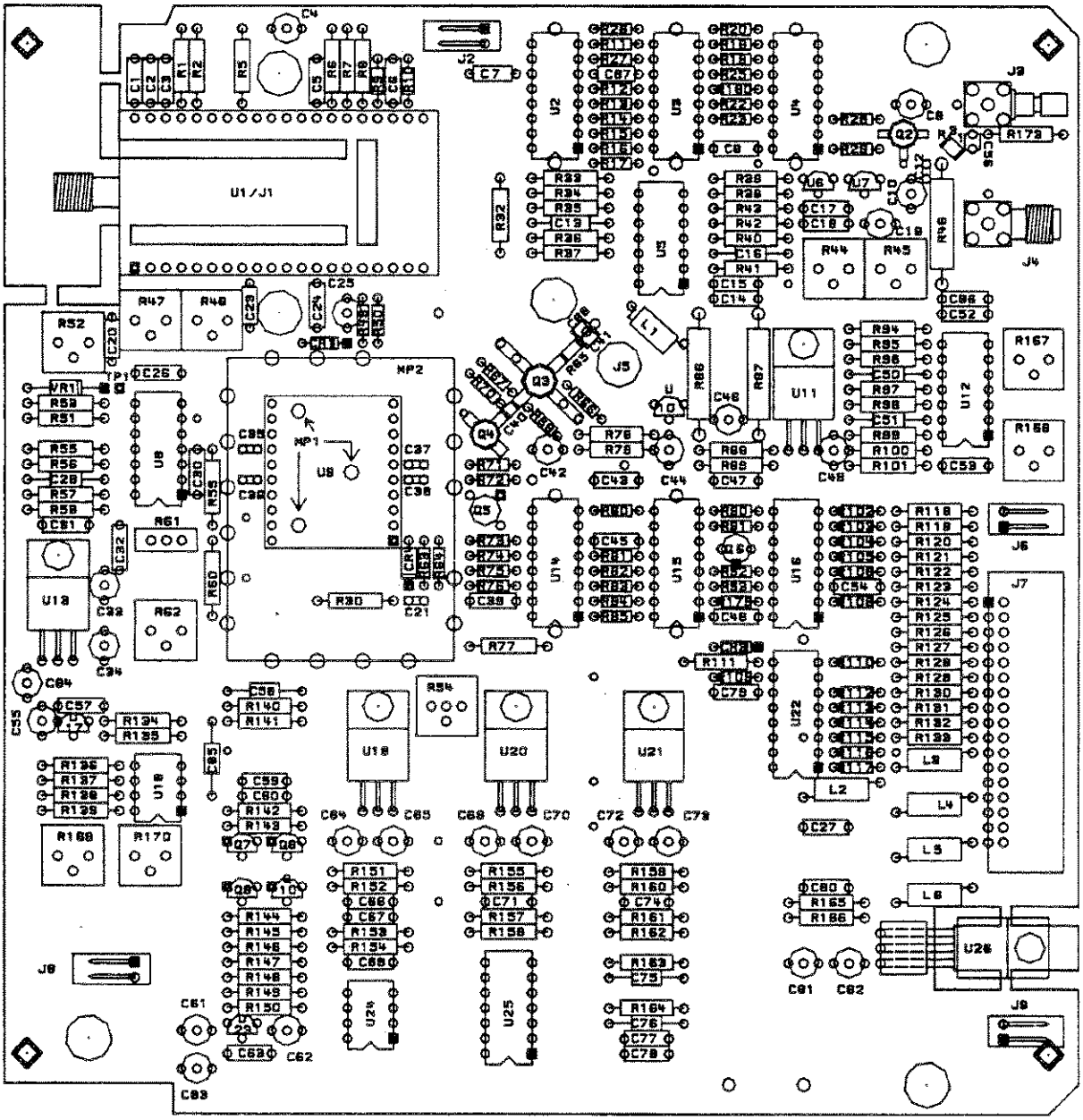


Figure 6C-11. Horizontal Assembly Component Locator

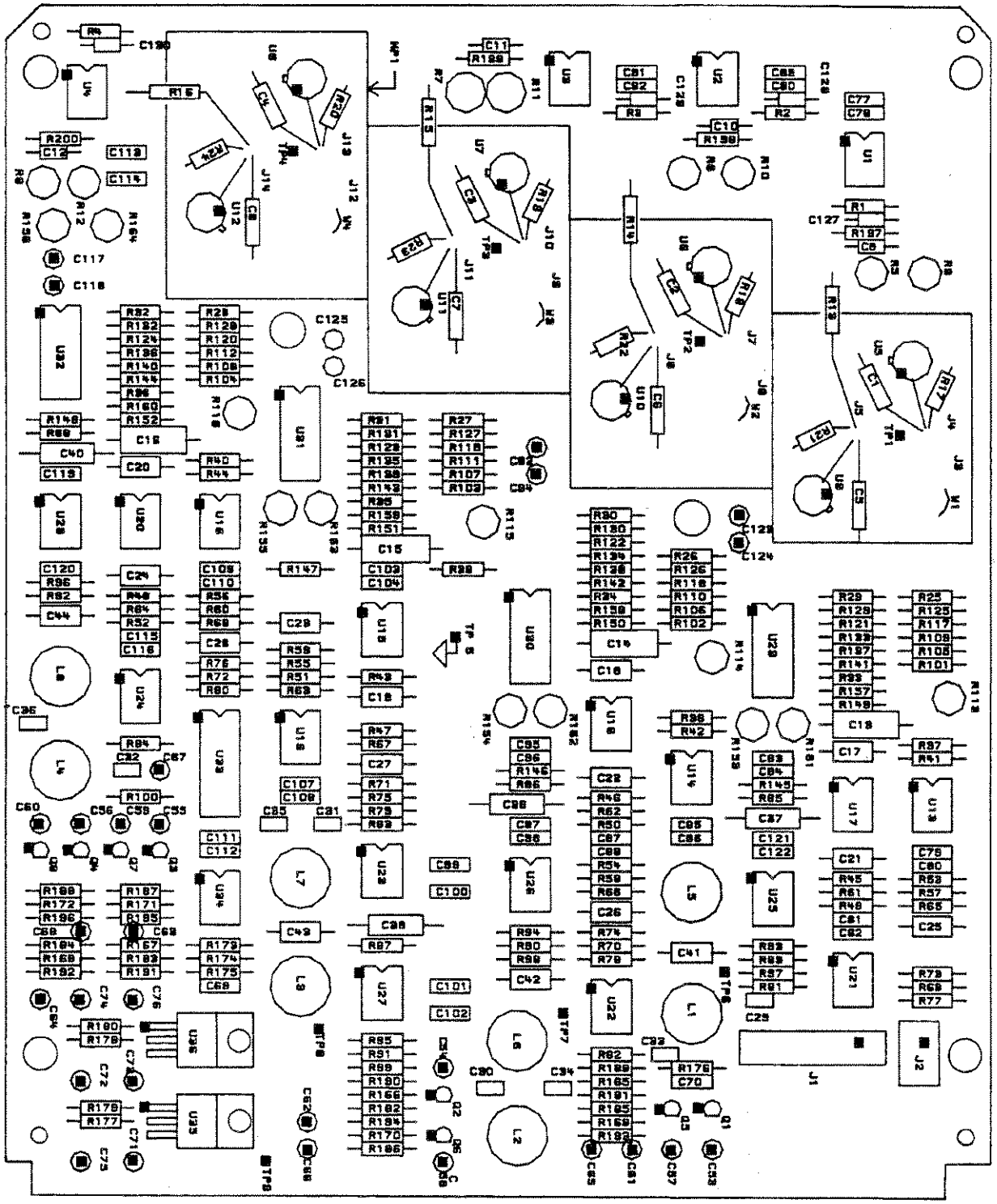


Figure 6C-12. Vertical Assembly Component Locator

Temperature Failures

The four channel test set contains two temperature compensation networks. The first is a temperature sensor attached to the main deck and is used to vary some operating bias levels with changing instrument temperatures. The second is a temperature sensing network for keeping the timebase hybrid working consistently with changes in temperature.

When a temperature problem occurs in the four channel test set, first verify that the fan is operating by visually checking to see if its blades are turning. If the fan seems inoperative, than measure between J6 pins 1 and 2 on the horizontal assembly. The voltage level should be approximately 8 V dc.

If the fan is operating, replace temperature sensor and cable W16 fastened to the test set's main deck. If temperature problems persist, then monitor U5 pins 6 and 13 on the horizontal control assembly while using a heat source and cool spray on the timebase hybrid (U9) on the horizontal assembly in the test set. U5 pin 6 should change -100 mV per degree C, and U5 pin 13 will change +100 mV per degree C.

Internal Diagnostic Loop Tests

The HP 54120B and HP 54121A are tested by 44 (numbered 0-43) internal diagnostic loop tests. When these loop tests pass, the instrument is considered functionally operational to a 90% confidence level. The loop tests are also a major troubleshooting tool for the instrument. To run the loop tests follow these five steps.

1. Remove the SMA short from channel 1 (if one is installed) and perform a one key-down powerup.

2. Press the **More** menu key, **Utility** menu key, **Test Menu** key, and **Extended Tests** key. Press keys numbered **1** and **2** on the keyboard, than press the **Enter** key. Press the **Start Test** key.

3. The instrument will run loops 0-43 executing each loop once whether they pass or fail.

4. Wait a few seconds until the oscilloscope displays graticules on the screen.

5. Press the **More** menu key, **Utility** menu key, and **Test Menu** key, and press **Display Errors** key. The failing loops will be displayed on the screen.

Repeat Loop

Selecting this mode continuously executes the Loop number entered at REPEAT LOOP. Pressing Start Test will start execution and the loop will continuously run until the Stop Test key is pressed. Pressing Display Errors will show how many times the loop was executed and the number of times the loop failed.

There are a number of loops that will blank or over-write the Stop Test key display on the CRT. However, the test can still be terminated by pressing the third function key from the top.

Run From Loop Selecting this mode starts execution from the loop entered and will proceed to execute all higher numbered loops. Upon reaching the last test, the cycle will be repeated.

If any test should fail, the instrument will change from **RUN FROM LOOP** to **REPEAT LOOP** and will repeatedly execute the loop that failed until the Stop Test key is pressed.

Test Loop Considerations

Troubleshoot the lowest loop numbers first. Higher loop numbers are usually dependent on lower loop numbers passing. Table 6C-9 cross references which assemblies are tested by which loops.

Some loops may fail if the adjustments are misadjusted. Before replacing costly assemblies refer to table 6C-8 to find out if any adjustments are causing loop failures.

The powerup self test routine includes only loops 0-17.

Before analog loops 20-39 are executed, loops 16 and 17 must pass. Loops 20-39 also require a trigger pulse for the samplers and A/D. There are three ways to generate this trigger.

1. FR - Freerun clock
2. SL - switching the trigger slope, this toggles the trigger slope line to the trigger comparator
3. TL - Changing the trigger level, this changes the trigger level DAC's output. Table 6D-15 describes which of these trigger generation methods is used for each of the loop tests.

If the SMA short is not removed from channel 1's input connector, loop 39 will fail and display a caution message on the screen.

Loops 20-24 test the oscilloscope's triggering capability. For these loops to pass, the following must be operating: horizontal control assembly, umbilical cable, ribbon cables connecting umbilical cable to horizontal and vertical assemblies, trigger hybrid, trigger input, and horizontal assembly. The vertical assembly, A/D assembly, samplers, pulse filter, and vertical input circuitry are not checked by these loops.

Loops 25-26 test the oscilloscope's horizontal assembly. Loops 20-24 must pass before loops 25-26 will pass. The circuitry tested and not tested for loops 25-26 are the same as loops 20-24.

Loop 27 tests the operation of HF reject and trigger sensitivity. For this loop to pass, loops 20-26 must pass. The circuitry tested and not tested in loop 27 are the same as loops 20-24.

Loops 28-30 test the vertical signal path with signals at ground levels. This requires that all the data acquisition modules are functional. If loops 20-27 pass, then the failure of loops 28-30 usually indicates the failure is in the vertical signal path: sampler, vertical assembly, A/D assembly. Loop 28 also checks the A/D assembly timing between channels during the A to D conversion.

Loops 31-38 test the data acquisition system's ability to acquire data. It tests the samplers, vertical assembly, and A/D assembly.

Loop 39 tests the TDR step's high and low levels. This loop requires all the data acquisition loops to pass. If only this loop fails, it probably indicates a failure in the TDR step generator system, horizontal assembly's TDR bias circuitry, or possibly a problem in channel 1. Loop 39 will fail if channel 1 is terminated.

Table 6C-8. Adjustments Which May Cause Loop Failures

Loop No.	**Adjustment**
1-17	None
18-19	Loop not used
20	Hysteresis
21	None
22-25	Hysteresis (loop 24 - trigger offset also)
26	None
27-30	Hysteresis (loop 30 - offset gain also)
31-34	SRD Drive and Sampler Bias, Hysteresis
35	SRD Drive and Sampler Bias, Hysteresis, LB1, HB1
36	SRD Drive and Sampler Bias, Hysteresis, LB2, HB2
37	SRD Drive and Sampler Bias, Hysteresis, LB3, HB3
38	SRD Drive and Sampler Bias, Hysteresis, LB4, HB4
39	SRD Drive and Sampler Bias, V top and bottom
40-43	None

Table 6C-9. Assemblies Which are Tested by Loop Tests

Assembly	**Loop Number**
TDR	39
A/D	16, 28-39
Horizontal control	17, 20, 22-39
Vertical	31-39
Horizontal	20, 22-39
Samplers	31-39
Pulse filter	31-39
Trigger hybrid	21-39
Display	5-9, 41, 42
I/O	0-43, especially 10-15, 43
CPU	0-43, especially 0-4, 40
RPG	15

Table 6C-10. Loop Descriptions

Loop No.	Loop Name	Trigger Source
0	Bus error check	N/A
1	ROM checksum	N/A
2	Static RAM R/W	N/A
3	N/A	N/A
4	CTC (counter timer chip)	N/A
5	Display assembly ID	N/A
6	CRTC (CRT controller)	N/A
7	Character RAM R/W	N/A
8	Graphics RAM R/W	N/A
9	Priority RAM R/W	N/A
10	I/O assembly ID	N/A
11	I/O RAM R/W	N/A
12	HP-IB chip	N/A
13	Keyboard controller chip	N/A
14	Power detect circuitry	N/A
15	RPG counter reset	N/A
16	A/D assembly ID	N/A
17	Horizontal control assembly ID	N/A
18	N/A	N/A
19	N/A	N/A
20	Data Acquisition (1)	SL
21	Trigger off/freerun off	N/A
22	Trigger level (1)	TL
23	Pos/Neg slope	TL
24	Trigger level (2)	TL
25	Coarse delay counters	SL
26	Rate generator/multi sample period	FR
27	Hysteresis band off	TL
28	A/D	SL
29	Feedthrough compensation	SL
30	Data acquisition (2)	SL
31	Channel 1 check	SL
32	Channel 2 check	SL
33	Channel 3 check	SL
34	Channel 4 check	SL
35	Channel 1 sampler gain	SL
36	Channel 2 sampler gain	SL
37	Channel 3 sampler gain	SL
38	Channel 4 sampler gain	SL
39	TDR	FR
40	Static RAM addressing test	N/A
41	Graphics RAM addressing test	N/A
42	Priority RAM addressing test	N/A
43	I/O RAM addressing test	N/A

Loop 20 Data Acquisition

This loop tests if the GO bit can be reset. This is done by toggling the trigger slope bit to create triggers which toggles the GO bit. If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates the time in μs between trigger and the GO bit.

-1 GO bit turns true while the trigger and freerun was off.

-2 GO bit never turns true.

Procedure

Use an oscilloscope to probe the points in figures 6C-13 through 6C-17 on the horizontal assembly.

U1 pin 35 is bad Suspect one of the following: horizontal control assembly, umbilical cable, ribbon cables. Go to the extended service section and perform the umbilical cable test to determine the faulty module.

U1 pin 19 is bad Go to the extended service section and perform the umbilical cable test. If umbilical cable test passes, then perform timebase/trigger test and replace either the trigger hybrid or the horizontal assembly as indicated by the test results. If the umbilical cable test fails, use the following test to determine the faulty module.

Perform umbilical cable extended service test on the trigger level input line only. If this test fails, use the umbilical test to determine the faulty module.

Trigger hybrid's output is bad Probe the following trigger hybrid input pins on the horizontal assembly.

Location	Signal	Signal Name
U1 pin 3	2.8 V	Trigger level
U1 pin 33	-0.8 V	High frequency reject
U1 pin 32	-0.8 V	Sensitivity
U1 pin 22	See figure 6C-17	Enable/disable
U1 pin 24	-0.6 V	Freerun on/off
U1 pin 35	See figure 6C-17	Trigger slope

Trigger hybrid inputs are good Replace the trigger hybrid; otherwise replace the horizontal assembly.

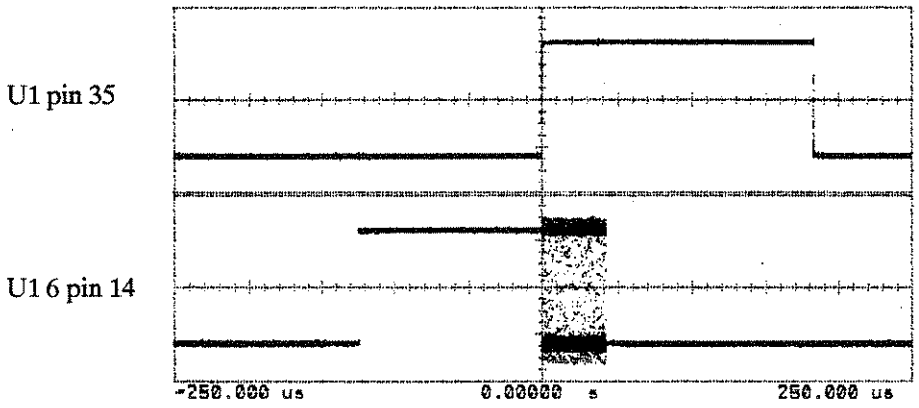


Figure 6C-13. Test Loop 20 Troubleshooting Waveform on the Horizontal Assembly

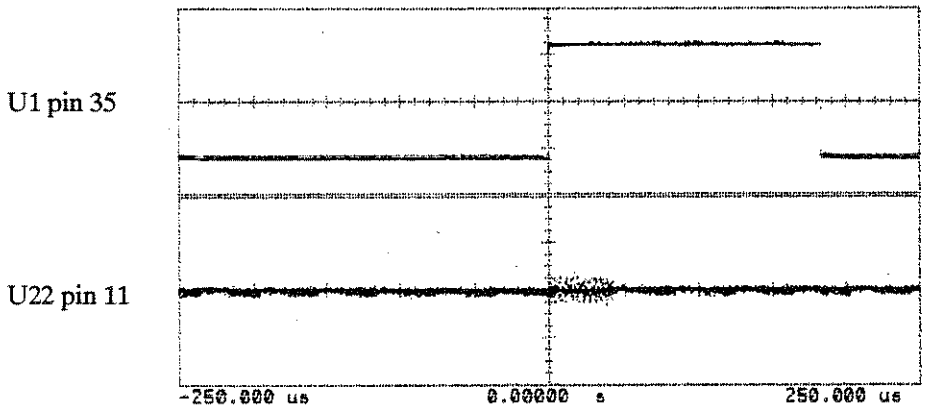


Figure 6C-14. Test Loop 20 Troubleshooting Waveform on the Horizontal Assembly

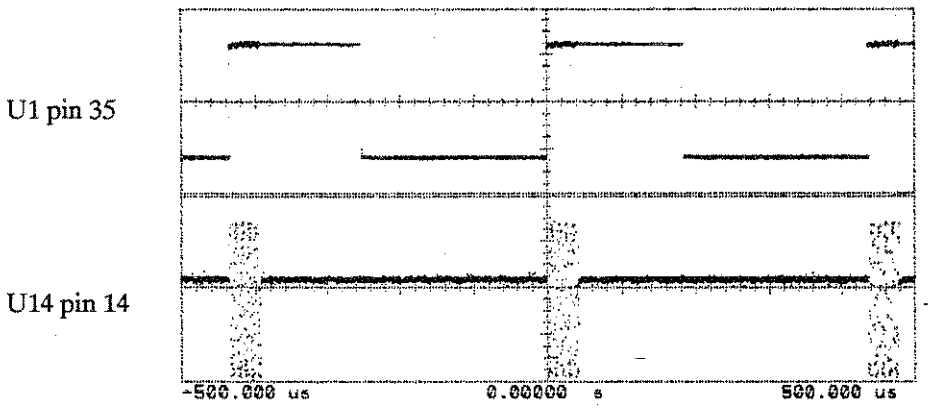


Figure 6C-15 Test Loop 20 Troubleshooting Waveform on the Horizontal Assembly

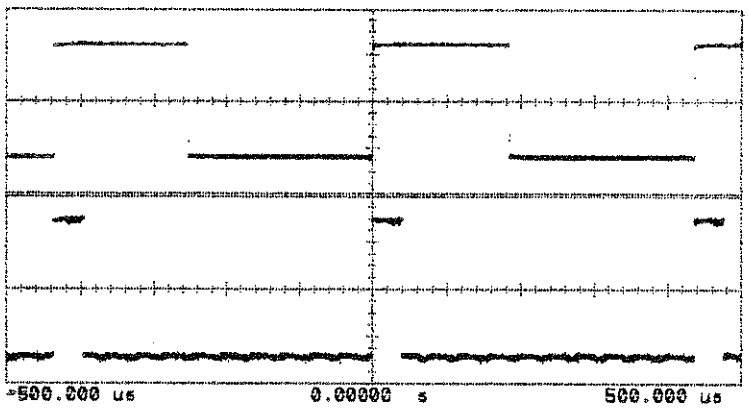


Figure 6C-16. Test Loop 20 Troubleshooting Waveform on the Horizontal Assembly

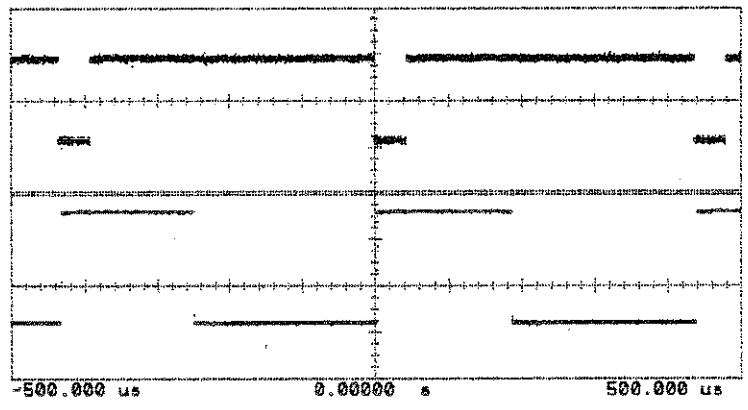


Figure 6C-17. Test Loop 20 Troubleshooting Waveform on the Horizontal Assembly

Loop 21 Trigger Off/Freerun Off

This loop tests triggers are not generated when either the trigger is disabled and freerun is enabled, or when trigger is enabled and freerun is disabled. If any lower numbered loops fail, troubleshoot them first. When this loop passes, status lines 1 and 2 should contain zero.

Status line 1 indicates the following

-1 GO bit turned true while the trigger was disabled and freerun was enabled. There should not be a trigger pulse in this case.

Status line 2 indicates the following

-2 GO bit turned true while the trigger hybrid was enabled and freerun was disabled. This would mean freerun cannot be turned off.

Procedure

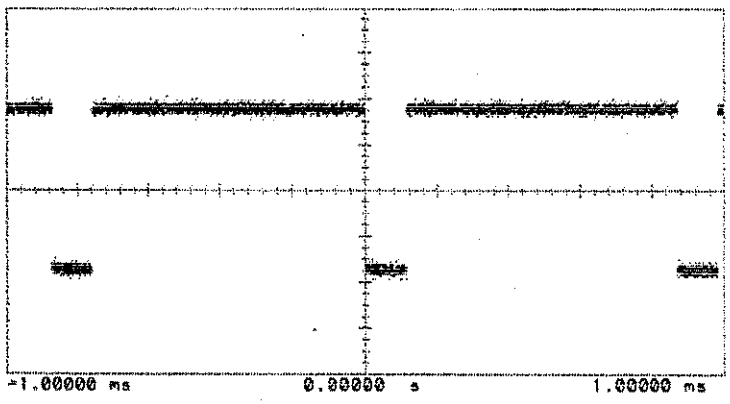
Use an oscilloscope to probe the following trigger hybrid inputs from the horizontal control assembly.

Location	Signal	Signal Name
U1 pin 3	2.8 V	Trigger level
U1 pin 33	0 -.8 V	High frequency reject
U1 pin 32	-0.8 V	Sensitivity
U1 pin 22	See figure 6C-18	Enable/disable
U1 pin 24	-0.6 V	Freerun on/off
U1 pin 35	0 V	Trigger slope

If any of the above signals are bad, perform the extended service umbilical cable test on trigger level input line only. This will determine if the test set is receiving the correct signals from the horizontal control assembly.

Probe U1 pin 19 with an oscilloscope. The level should be about 0.8 V with no pulse activity. If this signal is bad, replace the trigger hybrid.

U1 pin 22



Channel 1 = 200.0 mV/div
Offset = -420.0 mV

Channel 2 Off

Timebase = 200 µs
Delay = 0.00000 s

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -420.0 mV
Holdoff = 70.000 ns

Figure 6C-18. Test Loop 21 Troubleshooting Waveform on the Horizontal Assembly

Loop 22 Trigger Level (1)

This loop tests if the trigger level can be changed. This is done by toggling the trigger level from +1 V to -1 V and back to +1 V (slope is not important). The trigger is enabled before the level is changed to -1 V which should allow the instrument to trigger. If any loops below 22 fail, troubleshoot them first.

Status line 1 indicates if the instrument triggered.

- 0 The loop passed.
- -1 GO bit turned true while trigger and freerun were disabled.
- -2 GO bit turned true without changing the trigger level.
- -3 GO bit never turned true when the trigger level changed.

Procedure

Perform extended service umbilical cable test on trigger level input line only.

If the umbilical cable test passes, perform the timebase/trigger test. If the trigger hybrid's output is bad (no activity on U1 pin 19), probe the following trigger input points on the horizontal assembly.

Location	Signal	Signal Name
U1 pin 3	See figure 6C-19	Trigger level
U1 pin 33	-0.8 V	High frequency reject
U1 pin 32	-0.8 V	Sensitivity
U1 pin 22	See figure 6C-19	Enable/disable
U1 pin 24	-0.6 V	Freerun on/off
U1 pin 35	0 V	Trigger slope

If the inputs to the trigger hybrid are good, replace the trigger hybrid; otherwise replace the horizontal assembly.

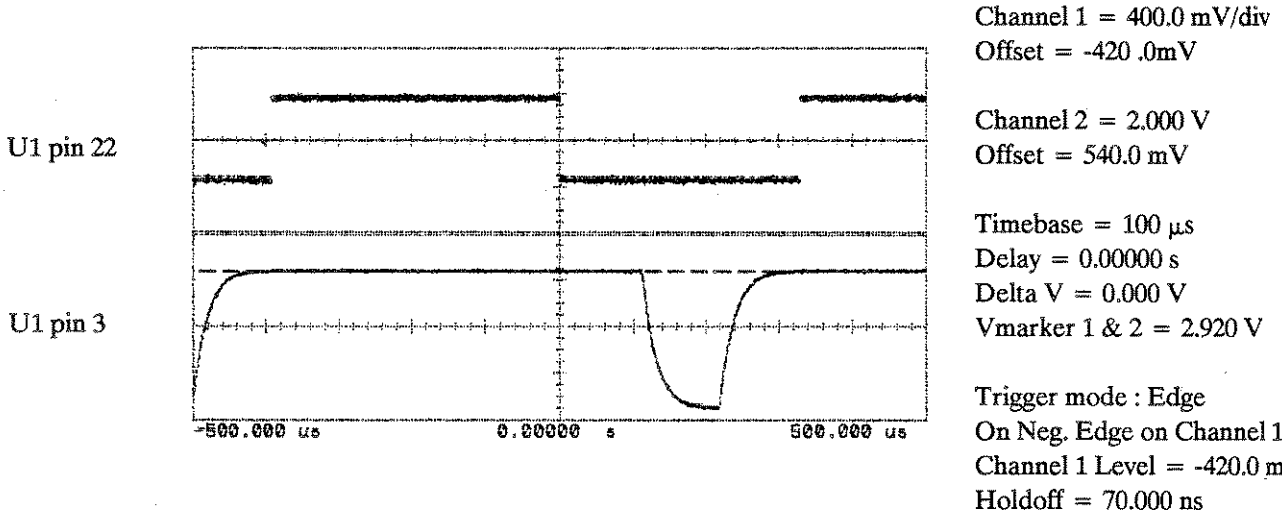


Figure 6C-19. Test Loop 22 Troubleshooting Waveform on the Horizontal Assembly.

Loop 23 Pos/Neg Slope

This loop tests that triggers are generated by toggling the Pos/Neg slope line when trigger is enabled and trigger level is toggled. If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates the following

- 0 Positive level triggering works properly.
- -1 GO bit turned true while trigger was disabled, freerun was off, and slope was positive.
- -2 GO bit turned true before the trigger level was toggled from +1V to -1 V.
- -3 GO bit never turned true by toggling the trigger level from +1 V to -1 V. (slope cannot be set positive)

Status line 2 indicates the following

- 0 Positive level triggering works properly.
- -1 GO bit turned true while trigger was disabled, freerun was off, and slope was negative.
- -2 GO bit turned true before the trigger level was toggled from -1 V to +1V.
- -3 GO bit never turned true by toggling the trigger level from -1 V to +1 V. (slope cannot be set to negative)

Procedure

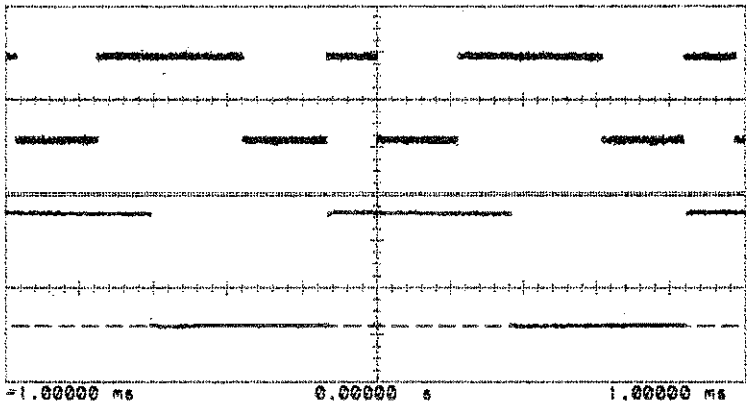
Perform the input umbilical cable extended service test on the trigger slope line.

Umbilical cable test passes Perform the timebase/trigger test.

Trigger hybrid's output is bad No activity on U1 pin 19, probe the following points on the horizontal assembly.

Location	Signal	Signal Name
U1 pin 3	See figure 6C-21	Trigger level
U1 pin 33	-0.8 V	High frequency reject
U1 pin 32	-0.8 V	Sensitivity
U1 pin 22	See figures 6C-20, 6C-21	Enable/disable
U1 pin 24	-0.6 V	Freerun on/off
U1 pin 35	See figure 6C-21	Trigger slope

If the inputs to the trigger hybrid are good, replace the trigger hybrid; otherwise replace the horizontal assembly.



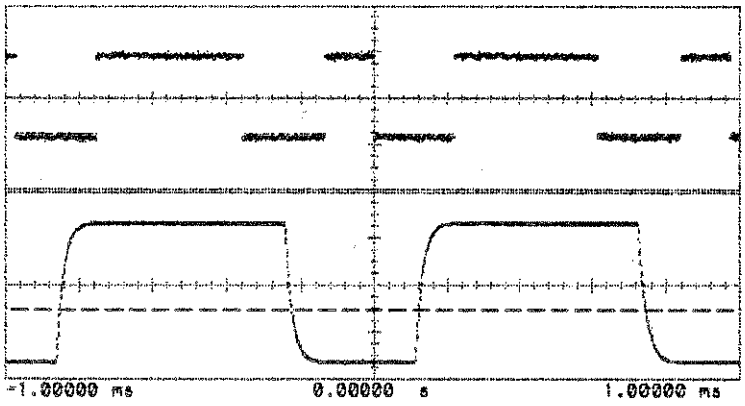
Channel 1 = 400.0 mV/div
Offset = -420 .0mV

Channel 2 = 2.000 V
Offset = 1.600 V

Timebase = 200 µs
Delay = 0.00000 s
Delta V = 0.000 V
Vmarker 1 & 2 = -20 mV

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -420.0 mV
Holdoff = 3 Events

Figure 6C-20. Test Loop 23 Troubleshooting Waveform on the Horizontal Assembly.



Channel 1 = 400.0 mV/div
Offset = -420 .0mV

Channel 2 = 2.000 V
Offset = 340.0 mV

Timebase = 200 µs
Delay = 0.00000 s
Delta V = 0.000 V
Vmarker 1 & 2 = -720.0 mV

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -420.0 mV
Holdoff = 3 Events

Figure 6C-21. Test Loop 23 Troubleshooting Waveform on the Horizontal Assembly.

Loop 24 Trigger Level (2)

This loop tests the trigger offset and trigger hysteresis band. If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates the following.

- 0 The Loop passed.
- -1 GO bit turned true while trigger was disabled and freerun was off.
- -2 GO bit never turned true by changing the trigger level.
- -3 Hysteresis offset is out of range.
- -4 Hysteresis band is out of range.

Status line 2 indicates the trigger offset range, valid range = 0 V ± 12 mV.

Status line 3 indicates the trigger hysteresis band, valid range = 20 mV ±12 mV.

Procedure

When this loop fails, perform the "Trigger Adjustments" in section 4 of this manual.

Perform the umbilical cable extended service test on the trigger slope line. If the umbilical cable test passes, perform the timebase/trigger test in this section.

If the trigger hybrid's output is bad (no activity on U1 pin 19), probe the following trigger hybrid input points on the horizontal assembly.

Location	Signal	Signal Name
U1 pin 3	See figure 6C-22	Trigger level
U1 pin 33	-0.8 V	High frequency reject
U1 pin 32	-0.8 V	Sensitivity
U1 pin 22	See figure 6C-23	Enable/disable
U1 pin 24	-0.6 V	Freerun on/off
U1 pin 35	See figure 6C-22	Trigger slope

If the trigger hybrid inputs are good, replace the trigger hybrid; otherwise replace the horizontal assembly.

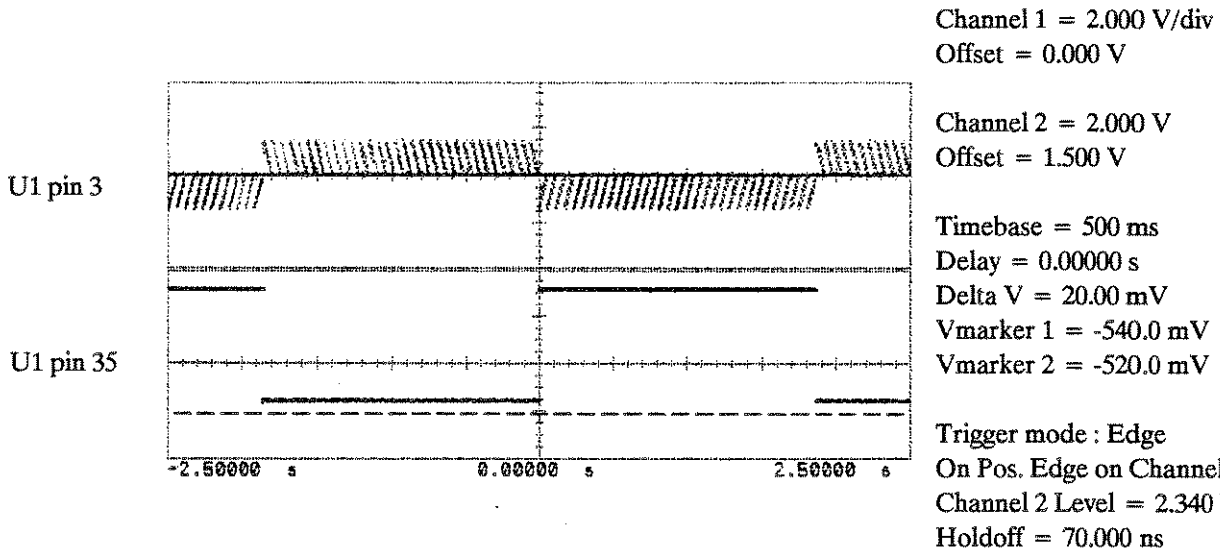


Figure 6C-22. Test Loop 24 Troubleshooting Waveform on the Horizontal Assembly.

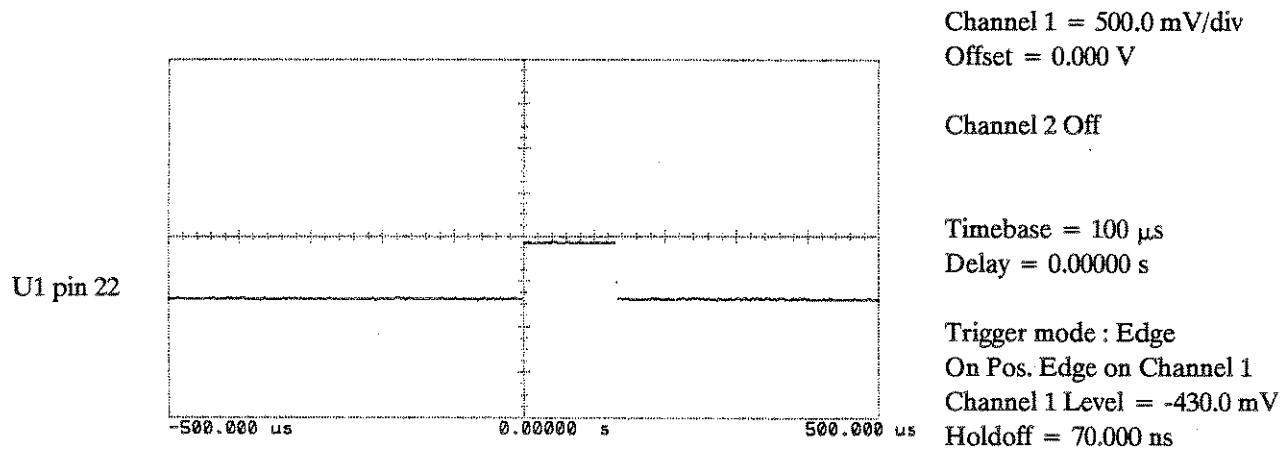


Figure 6C-23. Test Loop 24 Troubleshooting Waveform on the Horizontal Assembly.

Loop 25 Coarse Delay Time

This loop tests the coarse delay timer by timing how long it takes for the GO bit to become true after a trigger pulse occurs at two states. First, when the coarse delay counters are loaded with 4 ns. Second, when the coarse delay counter is loaded with 458.752 µs.

Status line 1 indicates the following.

0 The loop passed.
-1 GO bit turned true while trigger was disabled and freerun was off.
-2 GO bit never turned true when delay = 4 ns.
-3 Difference between short and long delay times is out of range. The valid range is 450 µs to 470 µs.

Status line 2 indicates the following.

-2 GO bit never turned true when delay was set to 458.752 µs.

Status line 3 indicates the time in ms between the trigger occurrence and the GO bit going true for 4 ns of delay.

Status line 4 indicates the time in µs between the trigger occurrence and the GO bit going true for 458.752 µs of delay.

Procedure

If this test fails, perform the frequency adjustments in section 4, adjustments, in this manual. Perform the umbilical cable extended service test, in this section, on the test set's inputs only. Probe the following signals and refer to figures 6C-24 and 6C-25.

Location	Signal Name	Assembly
U1 pin 19	Trigger clock	horizontal assembly
U8 pin 9		horizontal control assembly
U6 pin 2	pin 3 inverted	horizontal control assembly
U8 pin 9	GO bit	horizontal control assembly

Trigger clock signal is bad A previous loop should have failed also.

No signal at U8 pin 9 but U6 pins 2 and 3 are good Replace the horizontal control assembly.

No signal at U8 pin 9 and U6 pins 2 and 3 are bad Check the continuity of the umbilical cable and interconnect ribbon cable.

If the cable continuity test passes, probe the following points on the horizontal assembly and refer to figures 6C-26 and 6C-27 (U14 pin 14 is single shot measurement).

If any of these points test faulty, replace the horizontal assembly; otherwise call an HP service center.

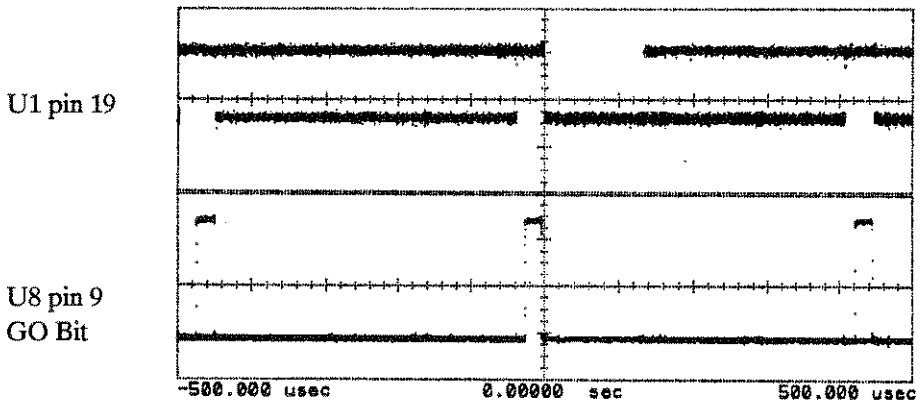


Figure 6C-24. Test Loop 25 Troubleshooting Waveforms on the Horizontal Assembly and on the Horizontal Control Assembly.

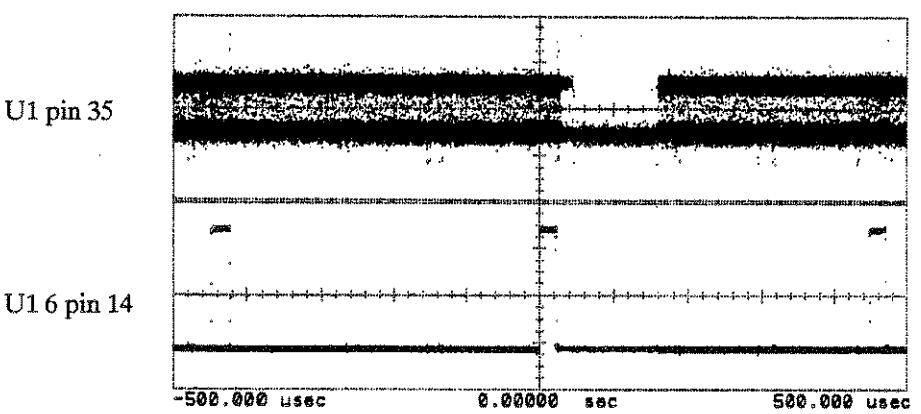


Figure 6C-25. Test Loop 25 Troubleshooting Waveforms on the Horizontal Control Assembly.

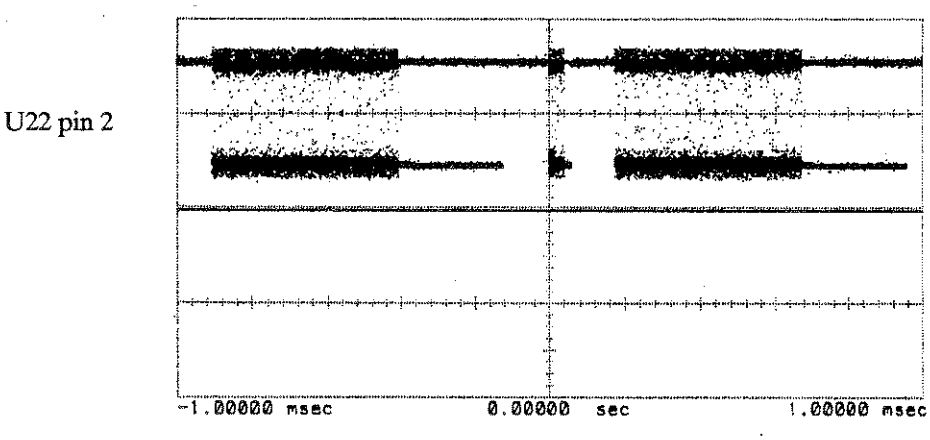
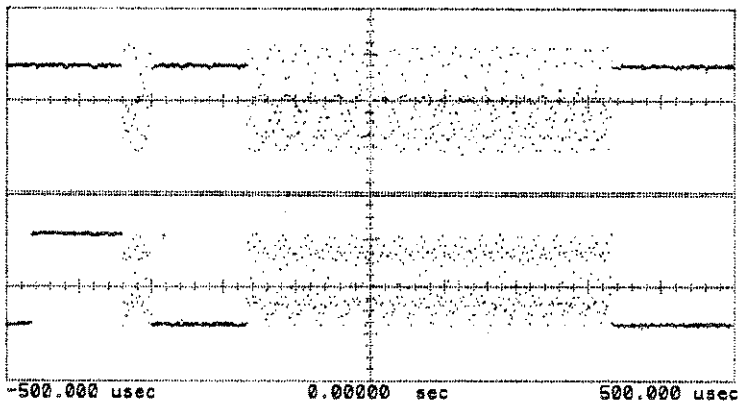


Figure 6C-26. Test Loop 25 Troubleshooting Waveform on the Horizontal Assembly.

U14 pin 14
Single Shot
Measurement

U15 pin 6



Channel 1 = 400.0 mV/div
Offset = -316.0 mV

Channel 2 = 400.0 mV
Offset = -460.0 mV

Timebase = 100 µs
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 2
Channel 2 Level = -492 mV
Holdoff = 70.000 ns

Figure 6C-27. Test Loop 25 Troubleshooting Waveform on the Horizontal Assembly.

Loop 26 Rate Generator

This test checks if the rate generator operates at a particular frequency as expected. The freerun clock is set to 1 kHz. The time between GO bit toggles is approximately 1 ms. It is possible for multiple samples to occur per trigger event at this frequency. The minimum time between samples is 458.752 μs. Therefore, in 1 ms two A/D conversions could occur. Each time a sample is taken, a trigger must start the process. Troubleshoot all lower number loops first.

Status line 1 indicates the following.

-1 GO bit turned true while trigger was disabled and freerun was off.
-2 GO bit turned true while trigger was enabled and freerun was off.
-3 GO bit never turned true.
-4 GO bit never turned true after the first trigger event.
-5 GO bit never turned true after the second trigger event.
-6 Rate generator frequency cannot be calculated.
-7 Rate generator frequency is out of range.

Status line 2 indicates the frequency of the freerun generator, the valid range is 990 Hz to 1010 Hz.

Status line 3 indicates the following

-6 Sampling period cannot be calculated.
-7 Sampling frequency is out of range.

Status line 4 indicates the period of multi-samples in μs, the valid range is 448 μs to 468 μs.

Procedure

Frequency in status 2 is incorrect Perform the extended service input umbilical cable test. The umbilical cable and interconnect ribbon cables could cause this problem. If the test set is not receiving the proper signals and the cables are good, replace the horizontal control assembly.

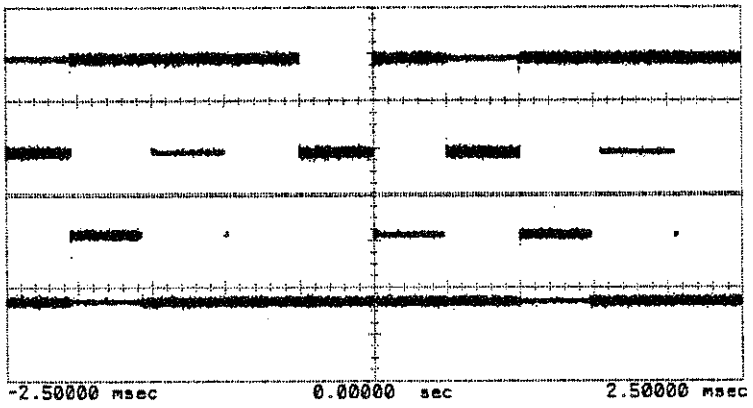
Status 4 out of range Probe the following points and refer to figures 6C-28 to 6C-31

Location	Signal Name	Assembly
U3 pin 8	Freerun clock	horizontal assembly
U1 pin 19	Trigger clock	horizontal assembly
U8 pin 9	GO bit	horizontal control assembly
U1 pin 19	Trigger clock	horizontal assembly
U14 pin14	L250 MHz	horizontal assembly
U1 pin 19	Trigger clock	horizontal assembly
U22 pin 2	7.8 MHz	horizontal assembly
U1 pin 19	Trigger clock	horizontal assembly

If you are this far in the troubleshooting procedure, than U3 pin 8 and U1 pin 19 should be good If U8 pin 9 is bad, check for 7.8 MHz at U6 pin 2. If 7.8 MHz is present at U6 pin 2, replace the horizontal control assembly; otherwise check the continuity of the umbilical cable and the interconnect ribbon cables. If the cable continuity is good and U22 pin 2 is bad, replace the horizontal assembly; otherwise call an HP service center. If U22 pin 2 is bad, replace the horizontal assembly.

U3 pin 8

U1 pin 19



Channel 1 = 400.0 mV/div
Offset = -316.0 mV

Channel 2 = 400.0 mV
Offset = -460.0 mV

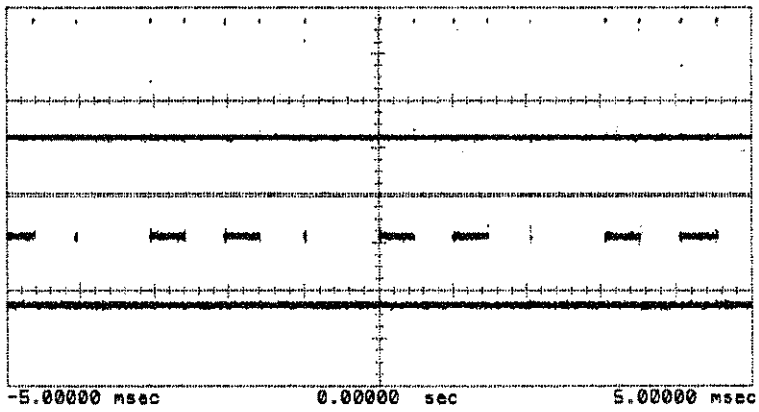
Timebase = 500 µs
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 2
Channel 2 Level = -492.0 mV
Holdoff = 70.000 ns

Figure 6C-28. Test Loop 26 Troubleshooting Waveform on the Horizontal Assembly.

U8 pin 9

U1 pin 9



Channel 1 = 2.000 V/div
Offset = 1.600 V

Channel 2 = 400.0 mV
Offset = -460.0 mV

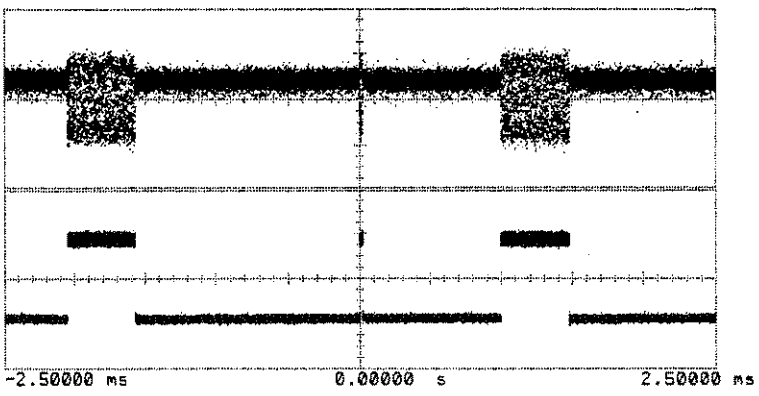
Timebase = 1.00 ms
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 2
Channel 2 Level = -492.0 mV
Holdoff = 70.000 ns

Figure 6C-29. Test Loop 26 Troubleshooting Waveform on the Horizontal Assembly.

U14 pin 14

U1 pin 19



Channel 1 = 200.0 mV/div
Offset = -326.0 mV

Channel 2 = 400.0 mV
Offset = -344.0 mV

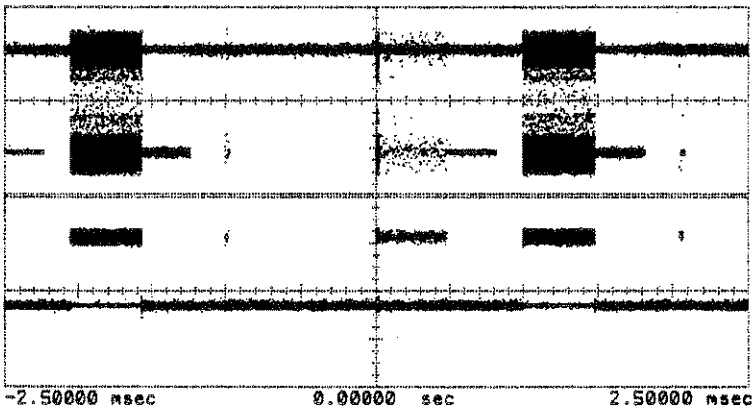
Timebase = 500 µs
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 2
Channel 2 Level = -360.0 mV
Holdoff = 70.000 ns

Figure 6C-30. Test Loop 26 Troubleshooting Waveform on the Horizontal Assembly.

U22 pin 2

U1 pin 19



Channel 1 = 400.0 mV/div
Offset = -1.300 V

Channel 2 = 400.0 mV
Offset = -460.0 mV

Timebase = 500 µs
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 2
Channel 2 Level = -492.0 mV
Holdoff = 70.000 ns

Figure 6C-31. Test loop 26 Troubleshooting Waveform on the Horizontal Assembly.

Loop 27 Hysteresis Band Off

This loop is similar to loop 24. It checks the trigger hysteresis band and trigger level with the HF sensitivity turned on (hysteresis is at minimum). This loop requires that loops 20-26 pass. If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates the following.

- 0 The loop passed.
- -1 GO bit turned true while trigger was disabled and freerun was off.
- -2 GO bit never turned true while changing trigger level.
- -3 Trigger offset is out of range.
- -4 Trigger hysteresis is out of range.

Status line 2 indicates trigger offset in mV, valid range 0 V ± 12 mV.

Status line 3 indicates trigger hysteresis band in mV, valid range -5 mV ± 12 mV.

Procedure

Perform the input umbilical cable extended service test on the HF sense and HF reject lines to eliminate the umbilical cable or interconnect ribbon cables as the possible problem. If the test set is not receiving the proper signals and the cables are good, replace the horizontal control assembly.

Probe the following points. If any are bad, replace the horizontal assembly.

U1 pin 3
U1 pin 33
U1 pin 32
U1 pin 24
U1 pin 35
U1 pin 19

If all of these pins are correct except for U1 pin 19, replace the trigger hybrid.

Loop 28 A/D Conversion

This loop measures the time it takes from the reading of channel 3's A/D conversion to the acquisition complete status when acquiring four channels of data. The loop then reads the A/D value on channel 4. If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates the following.

0	The loop passed.
-1	GO bit is always high while trigger is disabled.
-2	GO bit is always low while forced trigger occurs.
-3	A/D status bit is always busy for channels 1-3 conversions.
-4	A/D status bit is always complete for channel 4's conversion.
-5	A/D status bit is always busy for channel 4's conversion.
-6	Wrong A/D bit pattern from channel 4's conversion.
-7	A/D conversion time took too long (limit is 30 μs).

Status line 2 indicates the channel 4 A/D output bit pattern. The expected pattern is 111X XXXX XXXX XXX0.

Status line 3 indicates the A/D conversion time in μs. The expected time is 20 μs.

Procedure

Measure the dc voltage at TP1 on the A/D assembly. If it's not approximately 10 V, perform the "10 V Reference Adjustment" in section 4 of this manual.

If status line 3 is in error, probe the following points on the A/D assembly. Refer to figures 6C-32 through 6C-36.

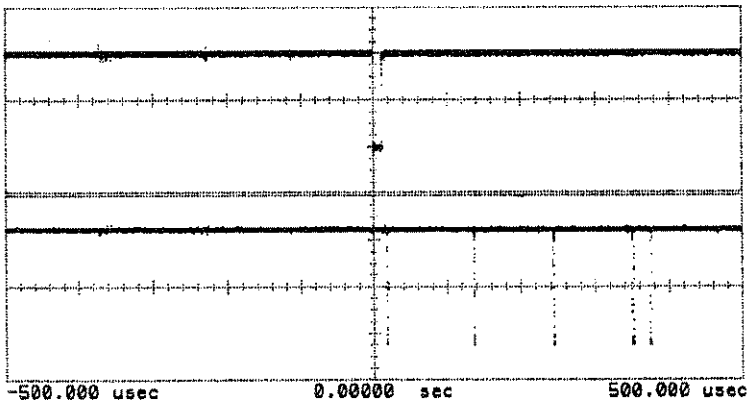
U44 pin 1	U21 pin 28	U44 pin 1
U42 pin 6	U44 pin 1	U42 pin 3
U21 pin 5	U21 pin 6	
U42 pin 8	U42 pin 11	

If U44 pin 1 is bad and there are no lower numbered loop failures, call an HP service center. If any other points are bad, replace the A/D assembly.

If status line 2 is in error, check to see if loops 29-38 fail. If any of these loops did fail, troubleshoot them first; otherwise perform the vertical extended service test on channel 4.

U44 pin 1

U21 pin 5



Channel 1 = 2.000 V/div
Offset = 2.220 V

Channel 2 = 2.000 V
Offset = 2.280 V

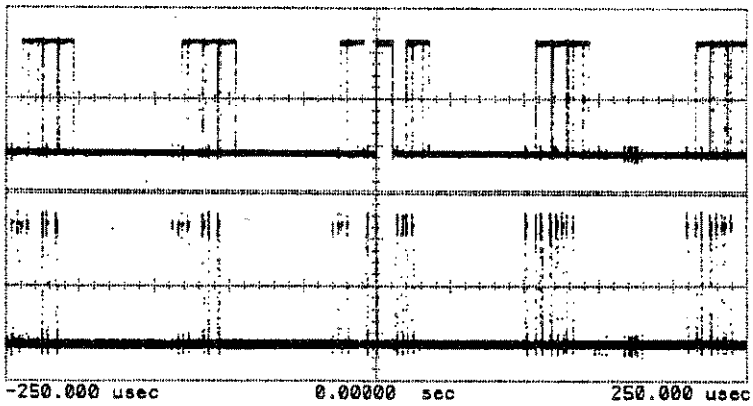
Timebase = 100 µs
Delay = 0.00000 s

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = 2.200 V
Holdoff = 70.000 ns

Figure 6C-32. Test Loop 28 Troubleshooting Waveform on the A/D Assembly.

U21 pin 28

U21 pin 6



Channel 1 = 2.000 V/div
Offset = 2.380 V

Channel 2 = 2.000 V
Offset = 2.600 V

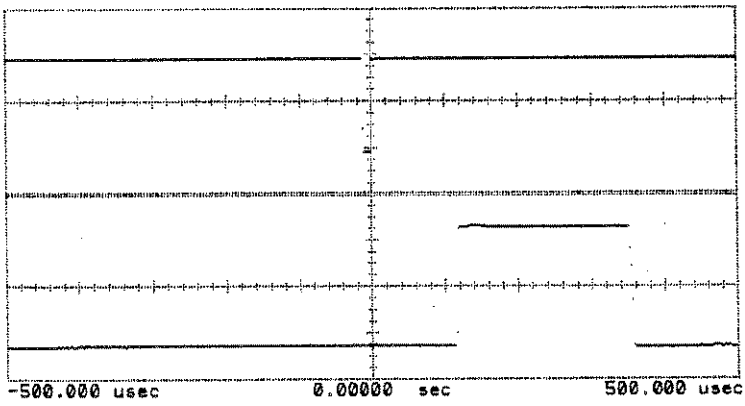
Timebase = 50.0 µs
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 1
Channel 1 Level = 2.380 V
Holdoff = 70.000 ns

Figure 6C-33. Test Loop 28 Troubleshooting Waveform on the A/D Assembly.

U44 pin 1

U42 pin 3



Channel 1 = 2.000 V/div
Offset = 2.380 V

Channel 2 = 2.000 V
Offset = 2.600 V

Timebase = 100 µs
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 1
Channel 1 Level = 2.380 V
Holdoff = 70.000 ns

Figure 6C-34. Test Loop 28 Troubleshooting Waveform on the A/D Assembly.

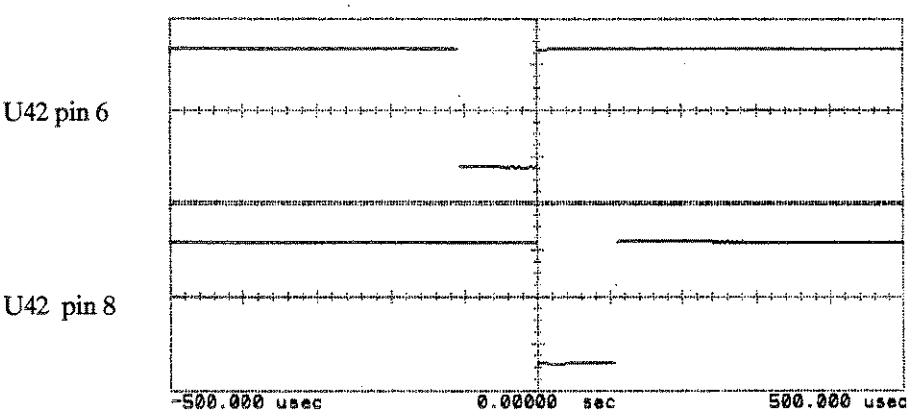


Figure 6C-35. Test Loop 28 Troubleshooting Waveform on the A/D Assembly.

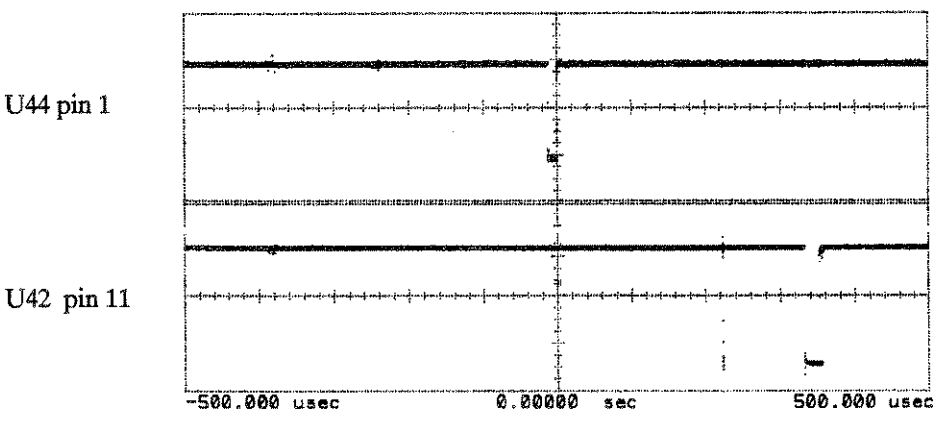


Figure 6C-36. Test Loop 28 Troubleshooting Waveform on the A/D Assembly.

Loop 29 Feedthrough

The sampler feedthrough is measured by performing an A/D conversion with the samplers turned off, and then turned on. The difference is sampler feedthrough. Trigger events are forced by changing the trigger slope, this causes a data acquisition process to take place. If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates the A/D output for channel 1 when data can read.

8001H	GO bit turned true while trigger was disabled and freerun was off.
8002H	GO bit never turned true by changing the trigger slope.
8003H	A/D status always busy, valid range for all A/D values is 800H ±140H.

Status line 2 indicates the A/D output for channel 2 when data can be read.

Status line 3 indicates the A/D output for channel 3 when data can be read.

Status line 4 indicates the A/D output for channel 4 when data can be read.

Procedure

When status line 1 contains 8001H through 8003H, this should cause lower numbered loops to fail also. Troubleshoot these lower numbered loops first. If lower numbered loops did not fail, call the HP service center.

Loops 29 and 30 should be analyzed together. If loop 30 passes but loop 29 fails, replace the vertical assembly.

Register out of tolerance Refer to table 6C-8, adjustment vs loop failures.

One channel fails Swap samplers to verify that the sampler is not causing the failure.

Swapping samplers does not fix the problem Troubleshoot single channel failures with the vertical extended service test and input umbilical extended service test. Possible failures are: vertical assembly, A/D assembly, ribbon cables, umbilical cable. If loops 31 through 34 or 35 through 38 are also failing, it may be helpful to troubleshoot these loops first.

All four channels fail Use the pulse flow diagram. If the pulse filter tests pass, replace the A/D assembly.

Loop 30 Data Acquisition (2)

This loop checks the A/D conversion on each channel with the samplers turned on and no input signals are applied. Each channel is checked 64 times and the results are averaged. Trigger pulses start the data acquisition process. Trigger pulses are forced by toggling the trigger slope line. If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates channel 1's A/D output.

8001H	GO bit turned true while trigger was disabled and freerun was off.
8002H	GO bit never turned true by changing the trigger slope.
8003H	A/D status is always busy, valid range for all A/D values is 800H ±140H (0 V ±80 mV).

Status line 2 indicates channel 2's A/D output.

Status line 3 indicates channel 3's A/D output.

Status line 4 indicates channel 4's A/D output.

If status line 1 contains 8001H through 8003H, this should cause lower numbered loops to fail also. Troubleshoot these lower numbered loops first. If lower numbered loops do not fail, call the HP service center.

Procedure

Multiple status register failures Refer to table 6C-8, adjustment vs loop failures.

Loop 30 fails but loop 29 passes Check the status registers. If only one status register is out of range, suspect a faulty sampler; otherwise suspect a faulty pulse filter.

Single channel failures Troubleshoot with the vertical extended service test and input umbilical extended service test. Possible failures are vertical assembly, A/D assembly, ribbon cables, umbilical cable. If loops 31 through 34 or 35 through 38 are also failing, it may be helpful to troubleshoot these loops first.

All four channels fail Use the pulse filter extended service test. If the pulse filter test passes, replace the A/D assembly.

Loops 31-34 Channels 1-4 Check

All inputs must be disconnected from the test set, this ensures the sampler input to be 0 V. The sampler measures the difference between the input signal and offset. The sampler input is expected to be 0 V, therefore the sampler will read the offset voltage. The offset voltage is set to 0 V. The sampler is turned on and the offset voltage is averaged 64 times. The process is repeated at 250 mV and -250 mV. The averaged results are compared to the following values. Troubleshoot lower numbered loops first.

250 mV Offset 80% ≤ | averaged 250 mV offset voltage minus averaged 0 V offset voltage | ≤ 120%

Status line 1 indicates

- 0 The loop passes on the first measurement.
- -1 False trigger occurs when trigger is disabled.
- -2 GO bit always low while forcing triggers.
- -3 A/D status always busy.
- -4 Value out of range (too small)
- -5 Value out of range (too large)

Status line 2 is the result of status line 1 changed to a percentage of 250 mV. The limits are 1 ±0.2

-250 mV Offset 80% ≤ | averaged -250 mV offset voltage minus averaged 0 V offset voltage | ≤ 120%

Status line 3 indicates the pass/fail

- 0 The loop passes on the second measurement.
- -1 False trigger occurs when trigger is disabled.
- -2 GO bit always low while forcing triggers.
- -3 A/D status always busy.
- -4 Value out of range (too small)
- -5 Value out of range (too large)

Status line 4 is the result of status line 3 changed to a percentage of 250 mV. The limits are 1 ±0.2

Procedure

Value of status lines 1 and 3 are close to passing Perform the sampler bias adjustments and the offset and gain adjustments in section 4 of this manual.

All four channels fail and the status registers contain -1, -2, or -3, the trigger loops 21 through 24 should also be failing. If the trigger loops are not failing, call an HP service center.

Single channel failures Swap samplers to verify they are not causing the problem. Perform the A/D extended service test to verify that the offset DAC's are operating correctly. If the offset DAC's are good and the problem stays in the original channel after swapping samplers, perform the vertical extended service test to determine the faulty module.

Loops 35-38 Channels 1-4 Sampler Gain

All inputs must be disconnected from the test set which causes the sampler input to be 0 V. The sampler measures the difference between the input signal and offset. The sampler input is expected to be 0 V, therefore the sampler will read the offset voltage. The offset voltage is set to 0 V. The sampler is turned on and the offset voltage is averaged 64 times. The process is repeated at 250 mV, and -250 mV. The averaged results are compared to status line values. Troubleshoot lower numbered loops first.

250 mV Offset

$$27\% \leq \left| \frac{\text{Gain at } +250 \text{ mV at high bandwidth bias mode}}{\text{Gain at } +250 \text{ mV at low bandwidth bias mode}} \right| \leq 58\%$$

Status line 1 indicates

- 0 The loop passes on the first measurement.
- -1 GO bit always high while trigger is disabled.
- -2 GO bit always low while forcing triggers.
- -3 A/D status always busy.
- -4 Value out of range (too small)
- -5 Value out of range (too large)
- -6 Gain at +250 mV low bandwidth mode = 0

Status line 2 indicates the percent error of status line 1.

-250 mV Offset

$$27\% \leq \left| \frac{\text{Gain at -250 mV at high bandwidth bias mode}}{\text{Gain at -250 mV at low bandwidth bias mode}} \right| \leq 58\%$$

Status line 3 indicates

- 0 The loop passes on the second measurement.
- -1 GO bit always high while trigger is disabled.
- -2 GO bit always low while forcing triggers.
- -3 A/D status always busy.
- -4 Value out of range (too small)
- -5 Value out of range (too large)
- -6 Gain at -250 mV low bandwidth mode = 0

Status line 4 indicates the percent error of status line 3.

Procedure

All four channels fail and the status registers contain -1, -2, or -3, the trigger loops 21 through 24 should also be failing. If the trigger loops are not failing, call an HP service center.

Value of status lines 1 and 3 are close to passing Perform sampler bias adjustments and offset and gain adjustments, section 4 of this manual.

Single channel failures Swap samplers to verify that they not causing the problem. Perform the A/D extended service test to verify that the offset DAC's are operating correctly. If the offset DAC's are good and the problem stays in the original channel after swapping samplers, perform the vertical extended service test to determine the faulty module.

Loop 39 TDR

This loop tests the TDR step's low value (V_L) by delaying 1.5 μs from the trigger event and high value (V_H) by delaying 2.5 μs from the trigger event. Freerun clock is the trigger event. V_H and H_L are averaged 64 times. $V_V = V_H - V_L$ and should be between 225 mV and 600 mV. Troubleshoot lower numbered loops first.

Note If there is an SMA short on channel 1's input connector, the SMA short must be removed before this test will pass.

Status line 1 indicates the following

-1 False triggers occurred when trigger is disabled.
-2 Trigger does not occur when sampler is turned on.
-3 Trigger does not occur when sampler is turned off.
-4 A/D status bit is always busy.
-5 ΔV is out of range.

Status line 2 indicates V_H in hex – expected >800H

Status line 3 indicates V_L in hex – expected <800H

Status line 4 indicates V_V in mV – expected 412 mV ±188 mV.

Procedure

Status line 1 Contains -1, -2, -3, or -4 and no lower numbered loops are also failing, call an HP service center.

Perform TDR adjustments in section 4 of this manual.

Perform the TDR extended service test.

Channels 1 and 3 fail Perform the TDR system extended service test. If both channels 1 and 3 still fail, call an HP service center.

Channel 1 fails Perform the vertical extended service test.

Extended Service Tests

The internal diagnostic loop tests find a very large number of instrument failures and some gross parametric failures. Because of the interaction of many assemblies it may be difficult to troubleshoot the instrument using only the loop tests. Several extended service tests have been developed as an aid in troubleshooting.

The extended service tests are used in two ways. First, when a loop test fails, the troubleshooting information usually refers to one of the extended service tests. Second, with experience the extended service tests may be used without the loops tests for quicker isolation of the problem.

A few of the extended service tests are executed at only some instrument settings. If your instrument is failing at other instrument settings, you may want to adjust the test settings to correlate with your failure.

The extended service test are listed as a procedure with steps. If a step fails, replace the indicated part. If there are no indications on what part to replace, return to the flow diagrams for instructions. If a step passes, continue on with the next step in the procedure.

Figure 6C-37 illustrates the pin locations for the umbilical cable and the ribbon cables. Umbilical cable pins 1-16 correspond with pins 1-16 (respectively) on the ribbon cable connecting to the vertical assembly and A/D assembly. Umbilical cable pins 17-50 correspond with ribbon cable pins 34-1 (respectively) connecting to the horizontal assembly and horizontal control assembly.

Figure 6C-38 illustrates the pin definition of various three pin devices which may require probing.

Sampler Test

This is a front panel test which looks for the ability of each sampler to increment and decrement in offset with no signal applied. It also checks if each channel passes the 12.4 GHz bandwidth mode noise specification. If either test fails, a sampler is the first suspected module.

Umbilical Cable Test

This test checks the signals which interconnect the test set to the mainframe. The input and output lines to the test set are checked, and a test is provided to check the functioning of each line.

Umbilical Cable Input Test

This test checks if the A/D assembly, horizontal control assembly, and umbilical cable are delivering the proper signals to the test set. This is done by exercising various front panel controls on the mainframe and probing points in the test set. This test is similar to the umbilical cable test, but only the input lines to the test set are checked.

Sampler Input Test

This test ensures that the input connectors and channel 1's TDR generator are not causing apparent sampler failures. The sampler input connectors are disconnected and the sampler test is performed.

Sampler Swap Test This tests swaps a suspected bad sampler with a known good sampler and then performs the sampler test. If the failure follows the suspected bad sampler, then that sampler is actually faulty. If the problem stays with the original channel, swap the samplers back and perform the vertical test to determine the faulty module.

Vertical Test This test checks if the A/D assembly, vertical assembly, or an interconnecting cable is causing a vertical problem. Various points on the failing channel are compared to the other three channels to help isolate the problem. The four channel paths on the vertical assembly follow separate paths and it would be a very rare problem where more than one channel on the vertical assembly had the same problem (except for multiple faulty samplers).

A/D Assembly Test This test checks two major circuits on the A/D assembly. First, it checks that the A/D assembly is generating outputs for the other assemblies and that the offset DAC circuitry is operating. Second, it checks the analog switch and ADC clocking circuitry. If either of these circuit tests fail, the A/D assembly is suspected as faulty.

Pulse Filter System Test This test determines what part of the sample pulse generator circuitry is preventing sample pulses from arriving at the samplers. The suspected faulty components are the pulse filter and horizontal assembly.

TDR Test This is a front panel test which determines if the TDR system is working properly. For this test to work, it requires at least one channel of channels 2 through 4 to operate properly. The TDR specifications are checked in channel 1 and the known good channel. If either channel fails, suspect a faulty channel. If both channels fail, suspect a faulty TDR system.

TDR System Test This test determines which part of the TDR system is faulty. The suspect modules are: TDR step generator, TDR drive circuitry on the horizontal assembly, or TDR delay line.

Trigger Test This is a quick front panel test is see if the instrument is receiving triggers in both the triggered mode and freerun mode. The message "Running" on the screen's top left corner does not indicate the instrument is receiving triggers, it indicates the RUN key has been pressed.

Probing Trigger Test This test verifies that the trigger hybrid is functioning properly. External triggers are applied to the instrument and the trigger hybrid's output line is checked. If this test fails, the timebase/trigger test should be run to determine if the trigger hybrid is functioning correctly. If this test passes, the horizontal test should be run to find out why the trigger signal is not being received.

Timebase/Trigger Test This test verifies that the horizontal assembly is applying the proper signals to the trigger hybrid. If this test passes, the probing trigger test should be run to see if the trigger hybrid is good. If this test fails, the umbilical input test should be run to determine if the horizontal assembly is receiving the correct signals from the mainframe.

Horizontal Test This test checks for a timebase fault in either the horizontal assembly, horizontal control assembly, or interconnect cable. The instrument is setup in a known operating state, and the interface between the two boards is probed.

Sampler Test

This is a front panel test which looks for the ability of each sampler to increment and decrement in offset with no signal applied. It also checks if each channel passes the 12.4 GHz bandwidth mode noise specification. If either test fails, suspect a faulty sampler first. This test is performed on all four channels. However, if only one channel is suspected as faulty, it may be performed on only that channel.

1. Perform one key-down powerup routine.

2. Change display mode to 500 ms persistence, single screen, and grid graticules.
   Turn one channel on and other channels off.
   Set channel which is on to 10 mV/div.
   Change timebase to freerun mode.

3. Use the RPG control to change the channel's offset in a positive direction and a negative direction. If the trace only moves in one direction or not at all, or the dc level drifts, this test fails. Return to the flow diagram for instructions.

4. Press **Histogram** menu key. Press **Time/Voltage** key until **Voltage** is highlighted.
   Press **Window/Acquire/Results** key until **Acquire** is highlighted.
   Set number of samples to 10000.
   Press **Start Acquiring** key.
   Press **Window/Acquire/Results** key until **Results** is highlighted.
   Press **Sigma** key.

5. If sigma is >1 mV, this test fails. Return to the flow diagram for instructions on the failed channel. If the sigma is <1 mV, this channel passes. Continue with the procedure.

6. Turn channel 1 off and channel 2 on. Set channel 2 to 10 mV/div and repeat steps 3-5 for channel 2.

7. Repeat step 6 for channels 3 and 4.

8. If all the channels pass, this test passes.

Umbilical Cable Test

This test checks the interface between the test set and the mainframe. This is done by exercising various front panel controls on the mainframe and probing points for expected results. This test should be used to verify the umbilical interface test. Probable faulty assemblies are: ribbon cables, umbilical cable, horizontal control assembly, and A/D assembly,

Note

Most signals originate at the mainframe, check these signals first. If the mainframe signals are failing the test set cannot be expected to operate properly. If a signal is faulty (except for current signals), disconnect the umbilical cable from the signal source and probe the signal again.

1. Perform one key-down powerup routine.
2. Remove top and bottom covers from test set.
3. Start at the top of table 6C-11 and perform each test while probing the test set.
4. If all the probing points test good, then either the vertical assembly or the horizontal assembly is faulty. Return to the flow diagram.
5. Check the continuity of the umbilical cable. If the continuity check fails, replace the umbilical cable and return to the flow diagram; otherwise continue with step 6.
6. Check the continuity of the ribbon cable connecting the umbilical cable to the vertical assembly and horizontal assembly in the test set on the lines that failed. If the continuity check fails, replace the ribbon cable and return to the flow diagram; otherwise continue with step 7.
7. Check the continuity of the ribbon cable connecting the umbilical cable to the A/D assembly and horizontal control assembly in the mainframe, on the lines that failed. If the continuity check fails, replace the ribbon cable and return to the flow diagram; otherwise continue with step 8.
8. Replace assembly that is a source for the failing signals and return to flow diagram.

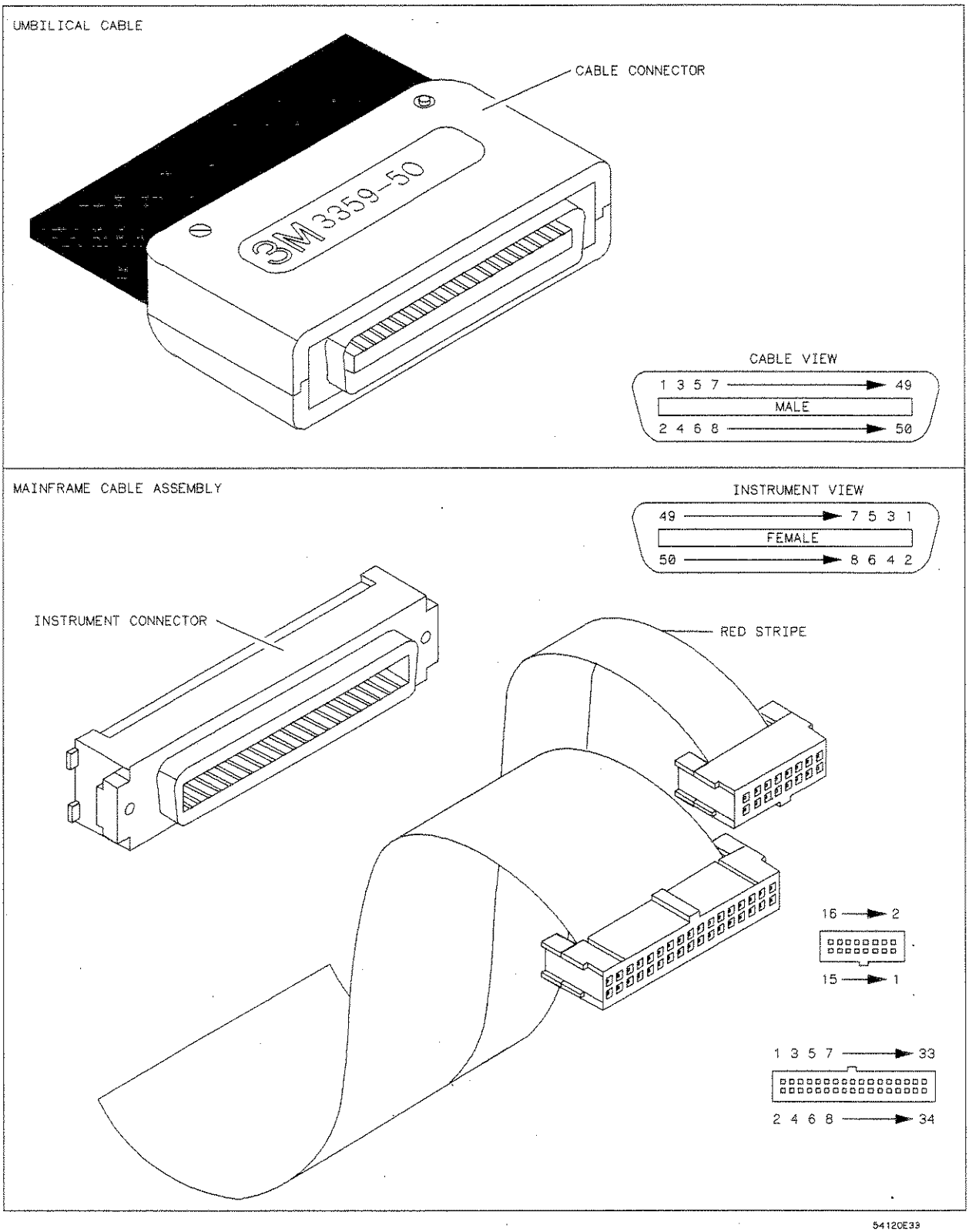


Figure 6C-37. Umbilical Cable and Ribbon Cable Pin Locations

16 Pin Ribbon Cable	UmbilicaCable Pin No.	Description	Test Set Vert Assy Location	Mainframe A/D Assy Location	Source	Test Description
1	1	Ch 1 offset	R105 & R109*	Current Sig	A/D	**Infit perst, freerun mode. Vary offset from +100 mV to -100 mV, points will vary from +100 mV to -100 mV.
2	2	AGND	TP5			
3	3	Ch 2 offset	R106 & R110*	Current Sig	A/D	Same as channel 1
4	4	AGND	TP5			
5	5	Ch 3 offset	R107 & R111*	Current Sig	A/D	Same as channel 1
6	6	AGND	TP5			
7	7	Ch 4 offset	R108 & R112*	Current Sig	A/D	Same as channel 1
8	8	AGND	TP5			
9	9	AGND	TP5			
10	10	Ch 4 Vert Sig	U28 pin 6	U12 pin 2	Vert.	**Infit perst, freerun mode, offset = +300 mV, probe for fig. 6C-39, Vary offset, pulse height should vary.
11	11	LL/H	U33 pin 15	U44 pin 1	Vert.	
12	12	Ch 3 Vert Sig	U27 pin 6	U11 pin 2	Vert.	Same as channel 4
13	13	-18 V	U36 pin 3	U18 pin 3	A/D***	DMM
14	14	Ch 2 Vert Sig	U26 pin 6	U10 pin 2	Vert.	Same as channel 4
15	15	+18 V	U35 pin 2	U17 pin 1	A/D***	DMM
16	16	Ch 1 Vert Sig	U25 pin 6	U9 pin 2	Vert.	Same as channel 4
34 Pin Ribbon Cable	**UmbilicaCable Pin No.**	**Description**	**Test Set Horz Assy Location**	**Mainframe Horz Cntl Location**	**Source**	**Test Description**
34	17	TDR on/Loff	U4 pin 8	U1 pin 10	H.C.	****Toggle step on/off, OFF = 0 V, ON = -0.8 V
33	18	NC				
32	19	NC				
31	20	AGND				
30	21	AGND				
29	22	AGND				
28	23	Freerun clock	U3 pin 8	U7 pin 10	H.C.	****freerun on, ECL freerun rates
27	24	AGND				
26	25	LEN/RESET	U3 pin 16	U7 pin 2	H.C.	****Trg'd mode, Probe for figure 6C-42
25	26	AGND				
24	27	Slope	U1 pin 35	U1 pin 16	H.C.	****Toggle slope, POS = 0 V, NEG = 5 V
23	28	Trig hysteresis	U1 pin 32	U1 pin 15	H.C.	****Toggle HF sens. ON = 0 V, OFF = -0.7 V
22	29	Trig level	U1 pin 3	Current Sig	H.C.	****Trg'd mode, Refer to table 6C-13.
21	30	Fine delay	R140 & R141*	Current Sig	H.C.	See fine delay test on next page.
20	31	LTC2	U22 pin 11	U3 pin 6	H.C.	Refer to fig 6C-43
19	32	LTBLOAD	U16 pin 5	U5 pin 4	H.C.	This test applies to umbilical pins 33-38 also Refer to
18	33	TB4	U16 pin 11	U11 pin 9	H.C.	figures 6C-43 through 6C-47.
17	34	TB3	U16 pin 10	U11 pin 11	H.C.	****Trg'd mode Probe figures 6C-43 and 6C-44, U16
16	35	TB2	U16 pin 9	U11 pin 14	H.C.	pins 9-11 are all high levels until particular delay settings
15	36	TB1	U16 pin 7	U11 pin 1	H.C.	are selected. Refer to figure 6C-45. The delay settings
14	37	TB0 reset	U15 pin 8	U5 pin 6	H.C.	are approximate. Set delay to 16 ns and probe for
13	38	TB0 set	U15 pin 12	U5 pin 10	H.C.	figures 6C-46 and 6C-47.
12	39	HF reject	U1 pin 33	U2 pin 9	H.C.	****Toggle HF reject, ON = 0 V, OFF = -0.7 V
11	40	-18 V	U20 pin 3	U16 pin 3	H.C.	DMM Refer to Figure 6C-38 for pinouts.
10	41	-8 V	U26 pin 3	U18 pin 3	H.C.	DMM Refer to Figure 6C-38 for pinouts.
9	42	-8 V	U26 pin 3	U18 pin 3	H.C.	DMM Refer to Figure 6C-38 for pinouts.
8	43	AGND				
7	44	+18 V	U21 pin 2	U15 pin 1	H.C.	DMM Refer to Figure 6C-38 for pinouts.
6	45	AGND				
5	46	+8 V	U11 pin 2	U17 pin 1	H.C.	DMM Refer to Figure 6C-38 for pinouts.
4	47	AGND				
3	48	L7.8 MHz	U22 pin 2	U6 pin 3	Horz	****Freerun mode, figures 6C-40 and 6C-41.
2	49	7.8 MHz	U22 pin 3	U6 pin 2	Horz	Same as U22 pin 2 except inverted.
1	50	AGND				

*Measurement is made at the junction of these two resistors.

**Perform a one key-down powerup routine before starting this procedure.

*** Refer to figure 6C-37 for pinouts.

Fine Delay Test

1. Perform one key-down powerup routine.

2. Set to freerun mode.

3. Change timebase to 10 ps/div.

4. Probe between R140 and R141 on the horizontal assembly. The signal will be noisy and untriggerable with the signal's bottom at 0 V and top at 7 mV.

5. Probe the signals in table 6C-12

Table 6C-12. Fine Delay Test Signals

Sweep Speed	Signal's low level	Signal's high level
20 ps/div	0 V	125 mV
50 ps/div	0 V	250 mV
100 ps/div	0 V	500 mV
200 ps/div	0 V	1 V
500 ps/div and above	0 V	2 V

6. If the above signals are good, this test passes.

Table 6C-13. Trigger Level Settings vs Measured Results

On Screen TriggerLevel Value	Measured Value
0 V	0 V
+100 mV	+290 mV
-100 mV	-290 mV
+1 V	+2.9 V
-1 V	-2.9 V

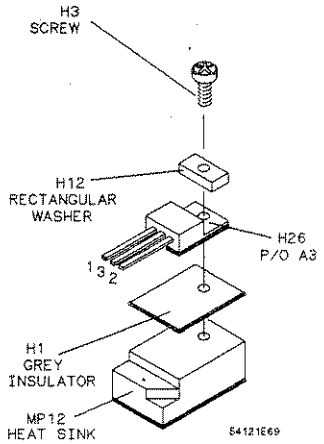
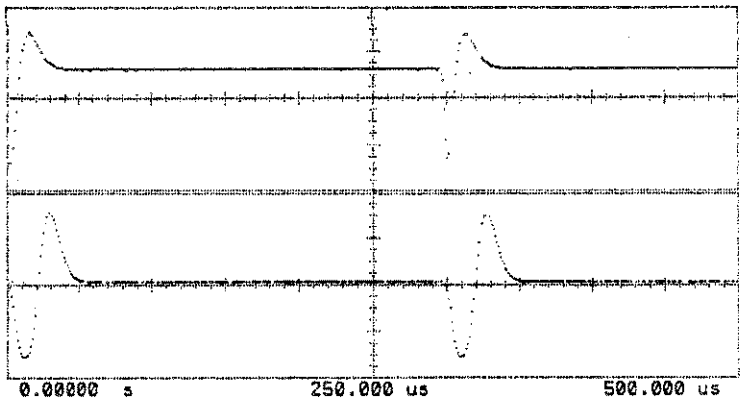


Figure 6C-38. Package Pin Locations

U24 pin 6

U26 pin 6



Channel 1 = 2.000 V/div
Offset = -1.240 V

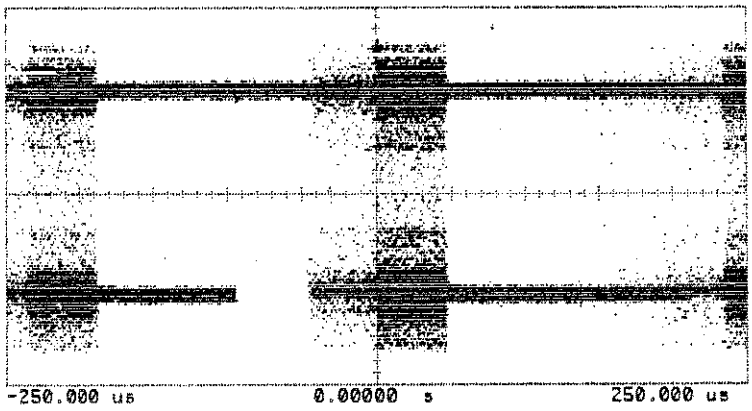
Channel 2 = 4.000 V
Offset = -200.0 mV

Timebase = 50.0 µs/div
Delay = 0.00000 s

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -1.240 V
Holdoff = 70.000 ns

Figure 6C-39. IKDPU, Infinite Persistence, Single Channel Display, Freerun Channel 4 Offset = +300 mV on the Vertical Assembly.

U22 pin 2



Channel 1 = 200.0 mV/div
Offset = -1.324 V

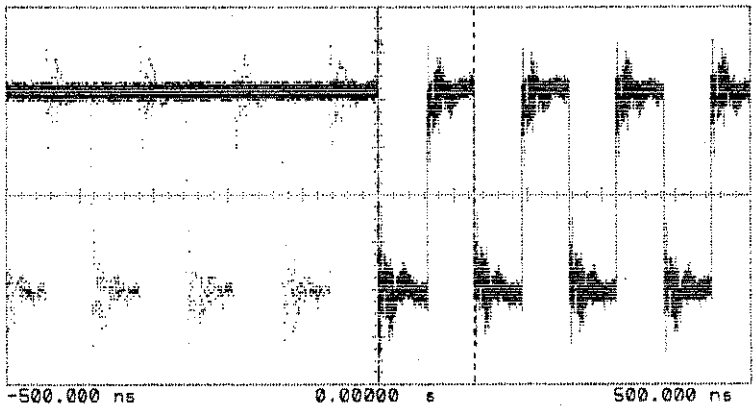
Channel 2 Off

Timebase = 50.0 µs/div
Delay = 0.00000 s

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -1.324 V
Holdoff = 70.000 ns

Figure 6C-40. On the Horizontal Assembly.

U22 pin 2



Channel 1 = 200.0 mV/div
Offset = -1.324 V

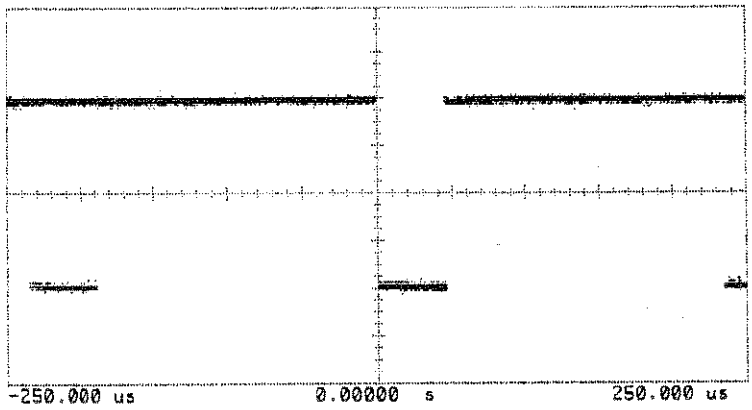
Channel 2 Off

Timebase = 100 ns/div
Delay = 0.00000 s
Delta T = 128.000 ns
Start = 0
Stop = 128.000 ns

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -1.324 V
Holdoff = 70.000 ns

Figure 6C-41. On the Horizontal assembly.

U3 pin 16



Channel 1 = 200.0 mV/div
Offset = -368.0 mV

Channel 2 Off

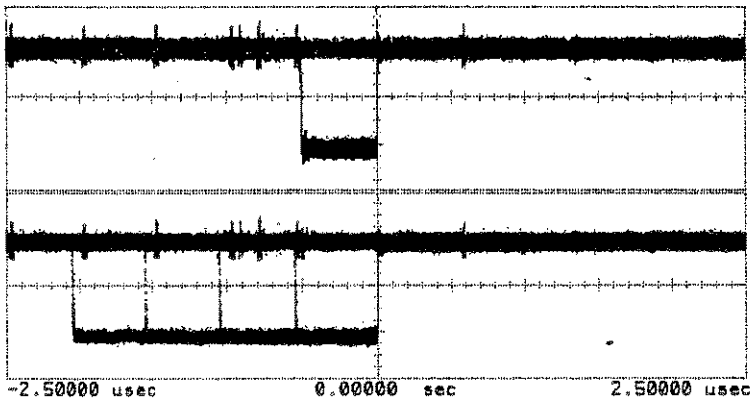
Timebase = 50.0 µs/div
Delay = 0.00000 s

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -368.0 mV
Holdoff = 70.000 ns

Figure 6C-42. 1KDPU, Freerun, on the Horizontal Assembly.

U16 pin 5

U22 pin 11



Channel 1 = 400.0 mV/div
Offset = -1.300 V

Channel 2 = 400.0 mV
Offset = -1.300 V

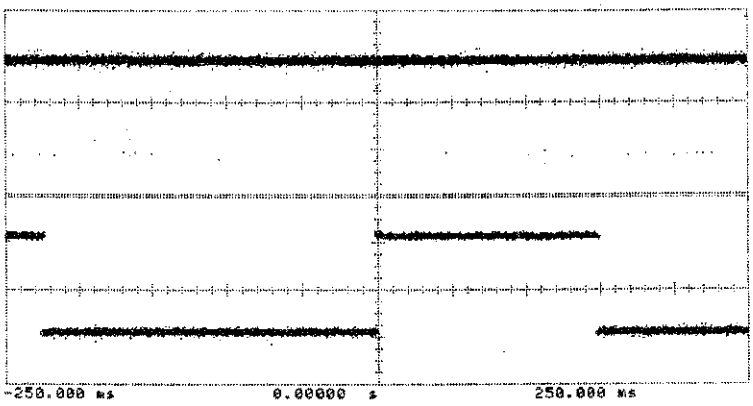
Timebase = 500 ns/div
Delay = 0.00000 s

Trigger mode : Pattern
On Pattern [HHXX] when
entered
Channel 1 Level = -1.300 V
Channel 2 Level = -1.300 V
Holdoff = 70.000 ns

Figure 6C-43. 1KDPU, Freerun, Trigger Mode Pattern HHXX, on the Horizontal Assembly.

U16 pin 5

U1 6 pin 7



Channel 1 = 400.0 mV/div
Offset = -1.224 V

Channel 2 = 400.0 mV
Offset = -1.300 V

Timebase = 50.0 ms/div
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 2
Channel 2 Level = -1.300 V
Holdoff = 70.000 ns

Figure 6C-44. On the Horizontal Assembly.

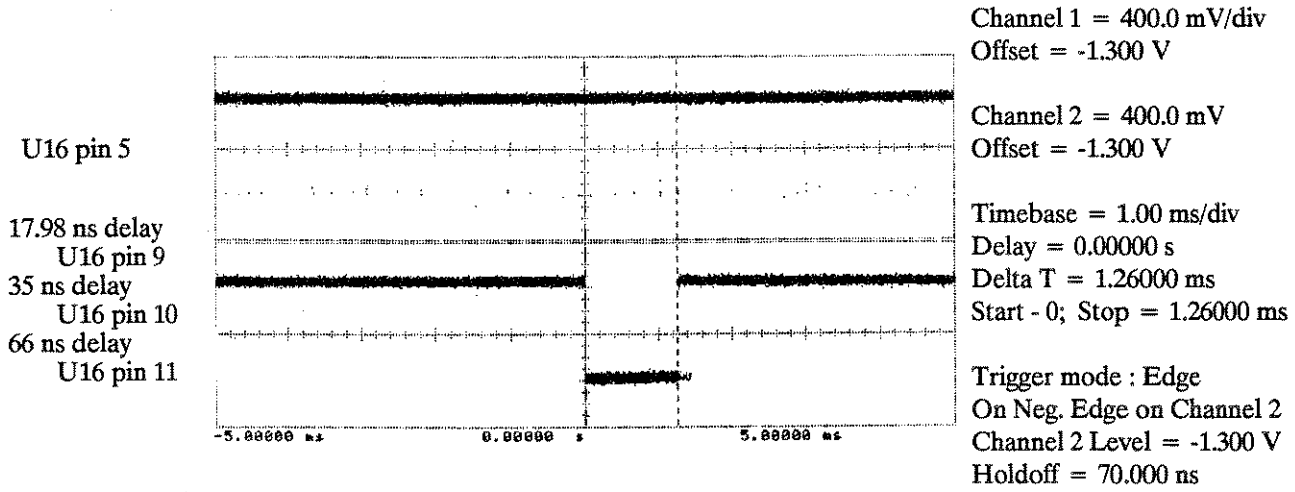


Figure 6C-45. On the Horizontal Assembly.

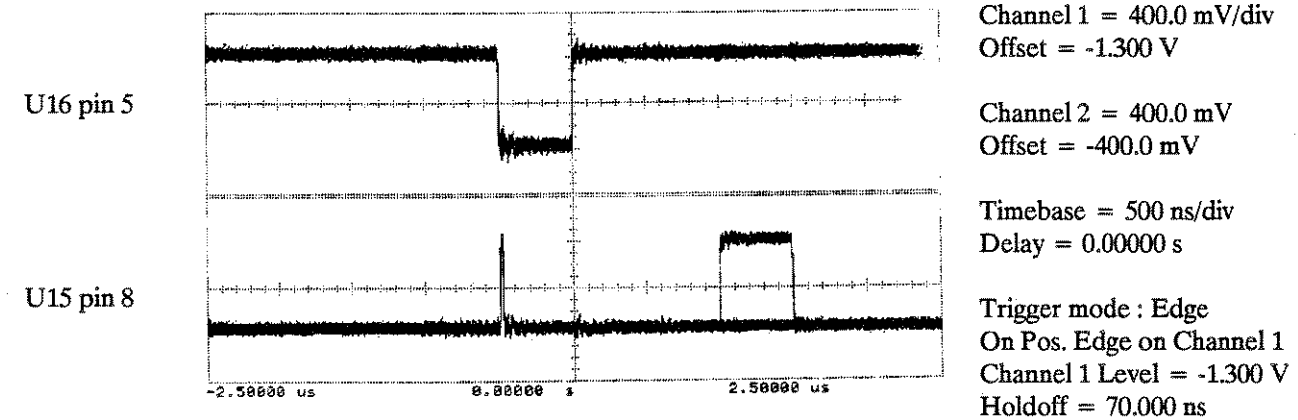


Figure 6C-46. Delay = 16 ns. On the Horizontal Assembly.

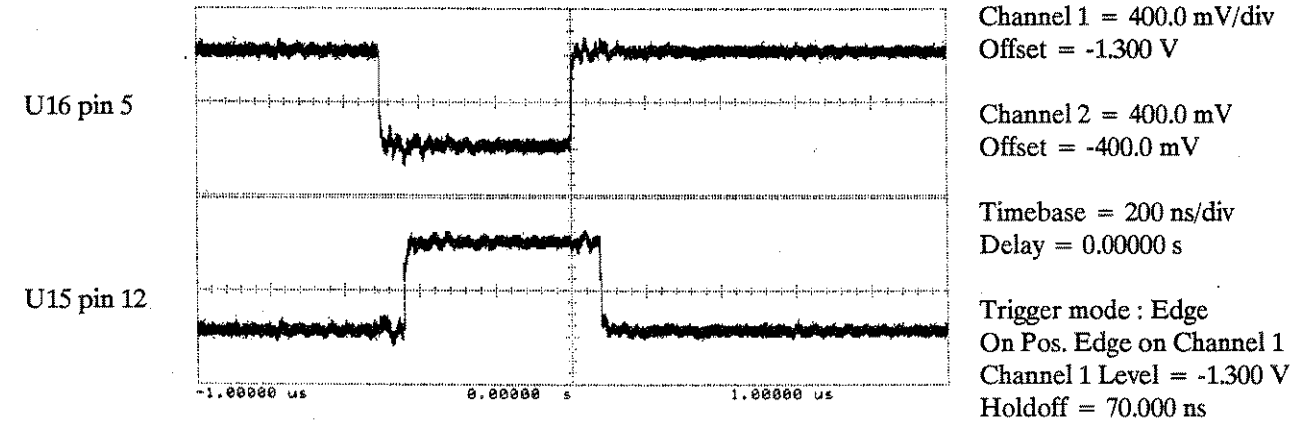


Figure 6C-47. On the Horizontal Assembly.

Sampler Input Test

This test ensures that each of the channel input connectors and channel 1's TDR generator are not causing apparent sampler failures. The sampler inputs are disconnected and the sampler test is performed.

1. Remove the sampler inputs using a torque wrench on the sampler, refer to sampler removal procedure in section 6A.
2. Reinstall the sampler.
3. Perform sampler test.
4. Return to flow diagrams.

Sampler Swap Test

This tests swaps a suspected faulty sampler with a known good sampler and then performs the sampler test. If the failure follows the suspected faulty sampler, then that sampler should be replaced. If the problem stays with the original channel, swap the samplers back and ensure the original operating channel is still good. If the channel that was operating before the swap is still good, perform the vertical test on the faulty channel; otherwise, replacement of both samplers, vertical assembly, and pulse filter may be required.

Vertical Test

This test checks if the A/D assembly, vertical assembly, or an interconnecting cable is causing a vertical problem. Various probing points on the bad channel are compared to the other three channels to help isolate the problem. The four channel paths on the vertical assembly follow separate paths and it would be a very rare problem where more than one channel on the vertical assembly had the same problem (except for multiple faulty samplers). Usually a multiple channel failure is caused by a faulty trigger hybrid, horizontal control assembly, horizontal assembly, A/D assembly, pulse filter, or pulse filter interconnects.

1. Perform one key-down powerup routine.

2. Change channel under test to the following settings and turn other channels off: display to single screen, persistence to infinite, offset to 320 mV, timebase to freerun.

3. Remove the test set's top and bottom covers.

4. Probe the following points on the vertical assembly. Refer to figures 6C-48 through 6C-52.

Figure	Point No.	Channel 1	Channel 2	Channel 3	Channel 4
6C-48	A	U21 pin 6	U22 pin	U23 pin 6	U24 pin 6
	B	U25 pin 6	6U26 pin	U27 pin 6	U28 pin 6
6C-49	C	U17 pin 6	6U18 pin 6	U19 pin 6	U20 pin 6
	D	U25 pin 6	U26 pin 6	U27 pin 6	U28 pin 6
6C-50	E	U13 pin 6	U14 pin 6	U15 pin 6	U16 pin 6
	F	U25 pin 6	U26 pin 6U	U27 pin 6	U28 pin 6
6C-51	G	U5 pin 6 - R25	6 pin 6 - R26	U7 pin 6 - R27	U8 pin 6 - R28
	H	U25 pin	U26 pin 6	U27 pin 6	U28 pin 6
6C-52	I	U9 pin 6 - R29	U10 pin 6 - R30	U11 pin 6 - R31	U12 pin 6 - R32
	J	U25 pin 6	U26 pin 6	U27 pin 6	U28 pin 6

5. If points G and I are bad and the sampler has been proven good by swapping it into another channel, then suspect either the pulse filter or semi-rigid cable connecting the pulse filter to the sampler (there is a very slight chance that the vertical assembly may still be at fault). Return to the flow diagram.

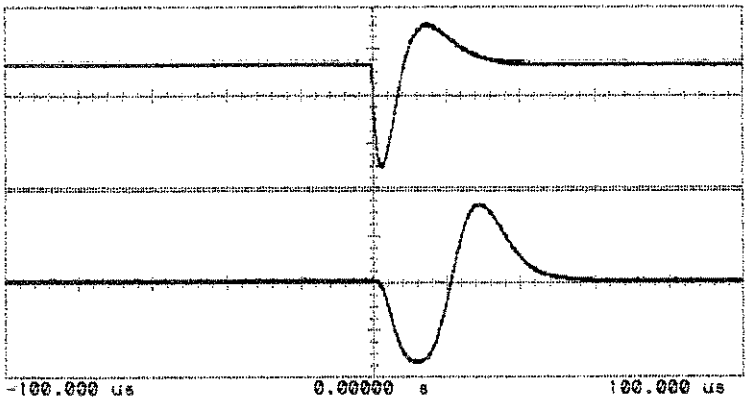
6. If any of the above test points are faulty for any of the channels, replace the vertical assembly and return to the flow diagram.

7. If all of the test points are good, then suspect either the A/D assembly, umbilical cable, or ribbon cables connecting to the umbilical cable. Probe the following points on the A/D assembly. If the points on the A/D assembly are not identical to the vertical assembly points, replace either the umbilical cable or the ribbon cables and return to the flow diagram; otherwise replace the A/D assembly and return to the flow diagram. Adjustments affect the pulse height.

Channel	Vertical Assembly	A/D Assembly
1	U25 pin 6	U9 pin 2
2	U26 pin 6	U10 pin 2
3	U27 pin 6	U11 pin 2
4	U28 pin 6	U12 pin 2

Point A
U21 pin 6

Point B
U25 pin 6



Channel 1 = 2.000 V/div
Offset = -1.340 V

Channel 2 = 4.000 V/div
Offset = -200.0 mV

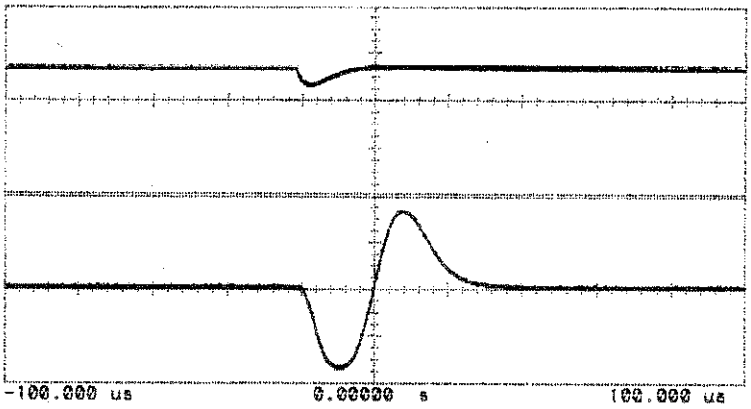
Timebase = 20.0 µs/div
Delay = 0.00000 s

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -1.340 V
Holdoff = 70.000 ns

Figure 6C-48. U21 Pin 6 and U25 Pin 6 on the Vertical Assembly.

Point C
U17 pin 6

Point D
U25 pin 6



Channel 1 = 2.000 V/div
Offset = -1.340 V

Channel 2 = 4.000 V/div
Offset = -200.0 mV

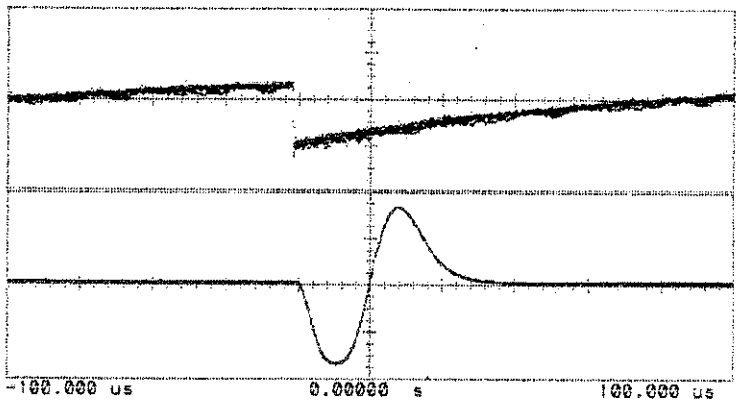
Timebase = 20.0 µs/div
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 2
Channel 2 Level = -200.0 mV
Holdoff = 70.000 ns

Figure 6C-49. U17 Pin 6 and U25 Pin 6 on the Vertical Assembly.

Point E
U13 pin 6

Point F
U25 pin 6



Channel 1 = 200.0 mV/div
Offset = 630.0 mV

Channel 2 = 4.000 V/div
Offset = -200.0 mV

Timebase = 20.0 µs/div
Delay = 0.00000 s

Trigger mode : Edge
On Neg. Edge on Channel 2
Channel 2 Level = -200.0 mV
Holdoff = 70.000 ns

Figure 6C-50. U13 Pin 6 and U25 Pin 6 on the Vertical Assembly.

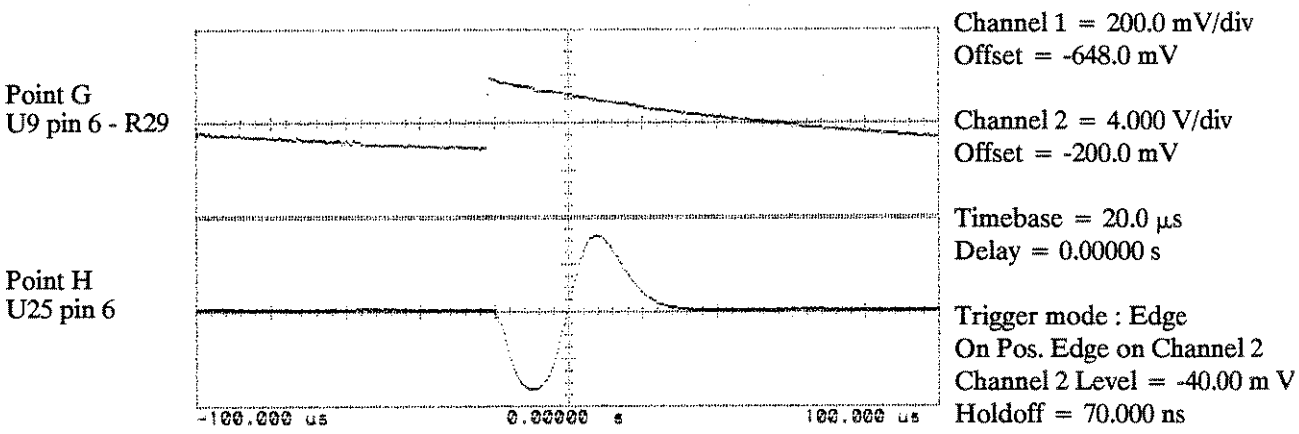


Figure 6C-51. U9 Pin 6 - R29 and U25 Pin 6 on the Vertical Assembly.

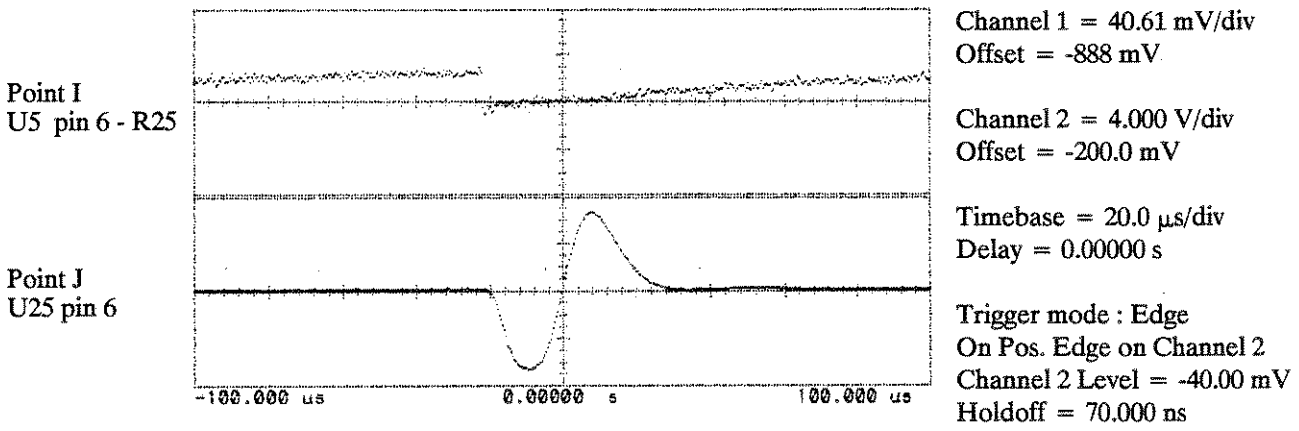


Figure 6C-52. U5 Pin 6 - R25 and U25 Pin 6 on the Vertical Assembly.

A/D Test

This test verifies the operation of three A/D assembly circuits: offset circuitry, analog switch, and clocking circuitry.

1. Remove umbilical cable from mainframe.

2. Perform one key-down powerup routine and change persistence to 300 ms.

3. Adjust each channel's offset in a positive and a negative direction. Probe the following points and verify the dc values vary linearly with changing offset values. When the offset is set to 500 mV and -500 mV the point under test should measure approximately 500 mV and -500 mV respectively.
   A/D - U1 pin 13 for channel 1
   A/D - U2 pin 13 for channel 2
   A/D - U3 pin 13 for channel 3
   A/D - U4 pin 13 for channel 4
   If these points fail, replace the A/D assembly.

4. Reconnect the umbilical cable to the mainframe and perform the umbilical test on the four offset lines going to the test set.

5. If the four offset lines are good, go to step 7

6. If the four offset lines are bad, check the continuity of the umbilical cable.

7. If the umbilical cable is good, perform a one key-down powerup, set to freerun mode, turn all channels on, and probe the following points on the A/D assembly. Refer to figures 6C-53 through 6C-56.

U44 pin 1 and U42 pin 3	Infinite persistence
U42 pin 6 and U42 pin 8	Infinite persistence
U42 pin 11 and U44 pin 1	Infinite persistence
U21 pin 28 and U21 pin 6	Single shot, varies depending on trigger position

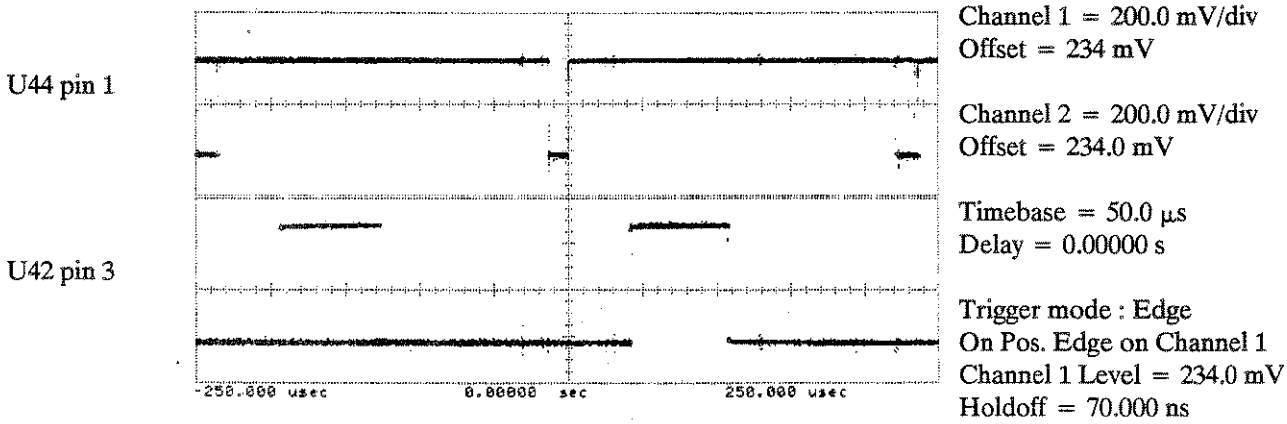
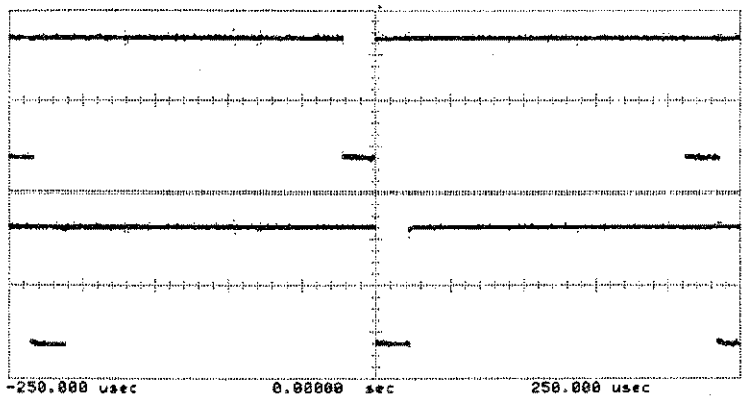


Figure 6C-53. On the A/D Assembly.

U42 pin 6

U42 pin 8



Channel 1 = 200.0 mV/div
Offset = 234.0 mV

Channel 2 = 200.0 mV/div
Offset = 234.0 mV

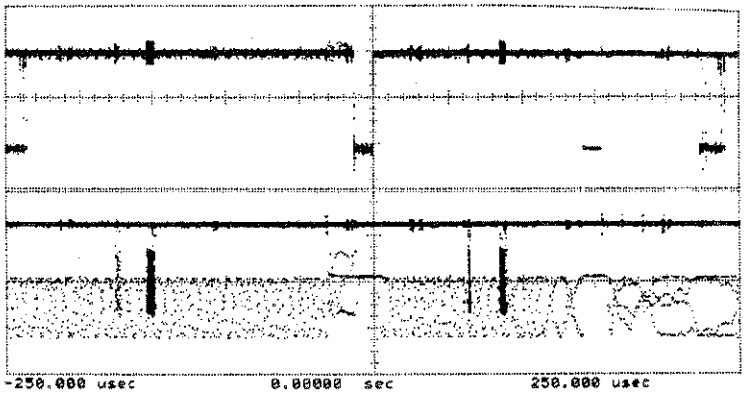
Timebase = 50.0 µs/div
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 1
Channel 1 Level = 234.0 mV
Holdoff = 70.000 ns

Figure 6C-54. On the A/D Assembly.

U42 pin 11

U44 pin 1



Channel 1 = 200.0 mV/div
Offset = 234.0 mV

Channel 2 = 200.0 mV/div
Offset = 234.0 mV

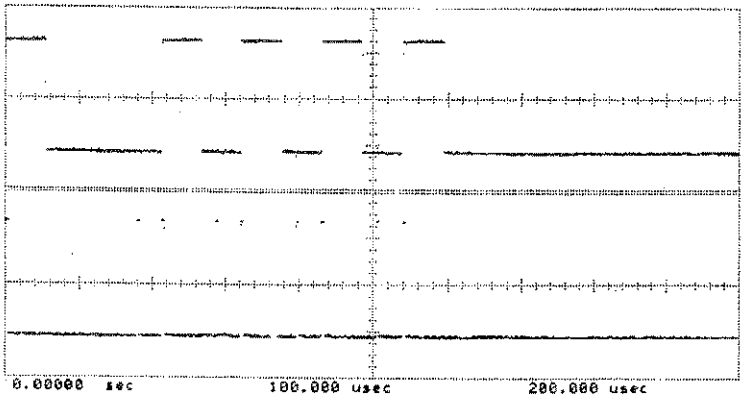
Timebase = 50.0 µs/div
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 1
Channel 1 Level = 234.0 mV
Holdoff = 70.000 ns

Figure 6C-55. On the A/D Assembly.

U21 pin 28

U21 pin 6



Channel 1 = 200.0 mV/div
Offset = 234.0 mV

Channel 2 = 200.0 mV/div
Offset = 234.0 mV

Timebase = 20.0 µs/div
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 1
Channel 1 Level = 234.0 mV
Holdoff = 70.000 ns

Figure 6C-56. On the A/D Assembly.

Pulse Filter Test

This test determines if the pulse filter or its bias circuit is faulty.

1. Perform one key-down powerup routine and place in "FreeRun" mode.

2. Probe the following points on the horizontal assembly and compare to figures 6C-57 through 6C-60.

   Between L1 and C41 at 100 ns/div and 2 μs/div
   Between collector of Q3 and R66

   U14 pin 11 at 20 ns/div and 50 μs/div
   Between collector of Q5 and R72

3. Lift the legs of C41 and C88, on the oppsite side of Q3, from the board.

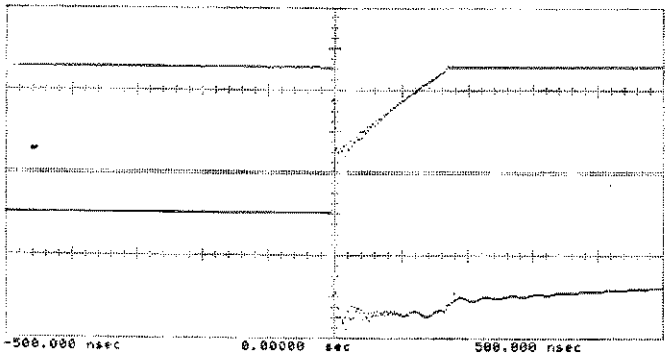
4. Probe the points listed in step 2 above but use figures 6C-61 through 6C-64.

5. If the waveforms in step 2 were bad and the waveforms in step 4 were good, replace the pulse filter; otherwise replace the horizontal assembly.

6. Reinstall the legs of C41 and C88 into the board and return to the flow diagram.

Between
L1 and C41

Between Collector
of Q3 and R66



Channel 1 = 400.0 mV/div
Offset = -128.0 mV

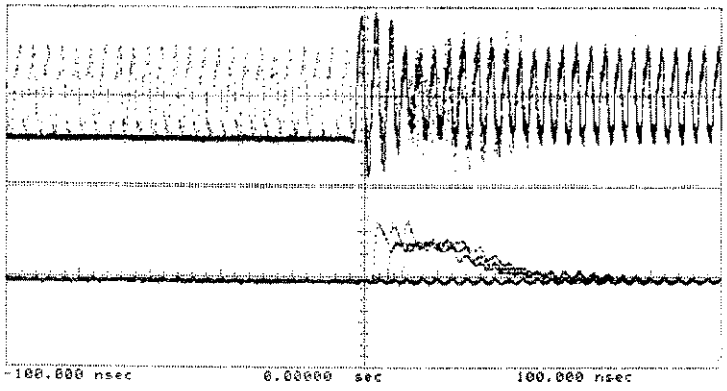
Channel 2 = 400.0 mV/div
Offset = 552.0 mV

Timebase = 100 ns/div
Delay = 0.00000 s
Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -380.0 mV
Holdoff = 70.000 ns

Figure 6C-57. With Pulse Filter Installed in Test Set, on the Horizontal Assembly, 100 ns/div.

U14 pin 11

Between Collector
of Q5 and R72



Channel 1 = 40.0 mV/div
Offset = -37.60 mV

Channel 2 = 400.0 mV/div
Offset = -436.0 mV

Timebase = 20.0 ns/div
Delay = 0.00000 s

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -48.00 mV
Holdoff = 70.000 ns

Figure 6C-58. With Pulse Filter Installed in Test Set, on the Horizontal Assembly, 20 ns/div .

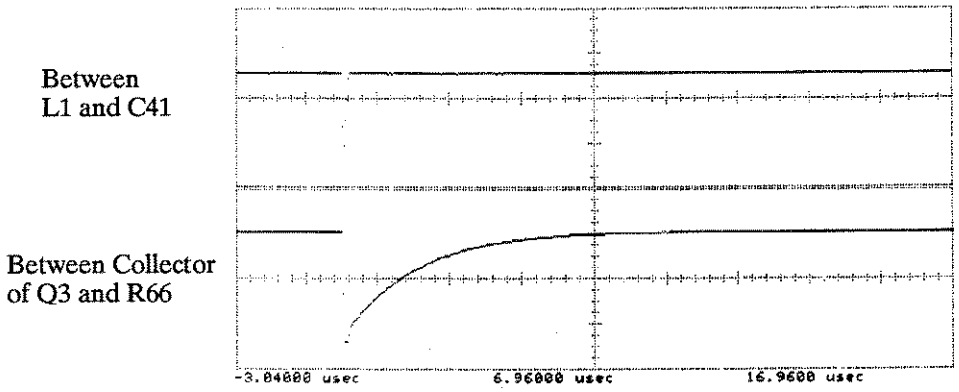


Figure 6C-59. With Pulse Filter Removed from Test Set, on the Horizontal Assembly, 2 µs/div.

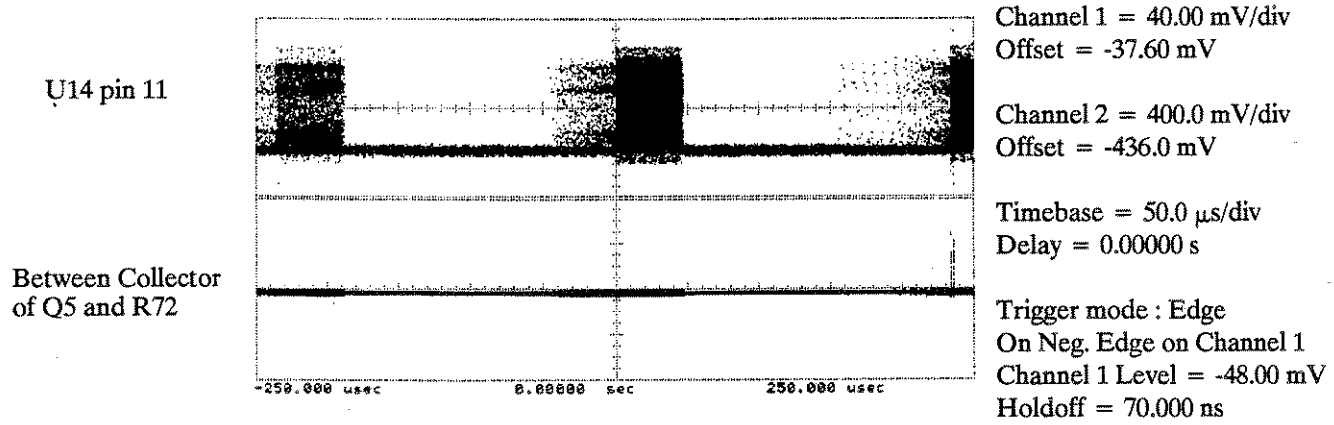


Figure 6C-60. With Pulse Filter Removed from Test Set, on the Horizontal Assembly, 50 µs/div.

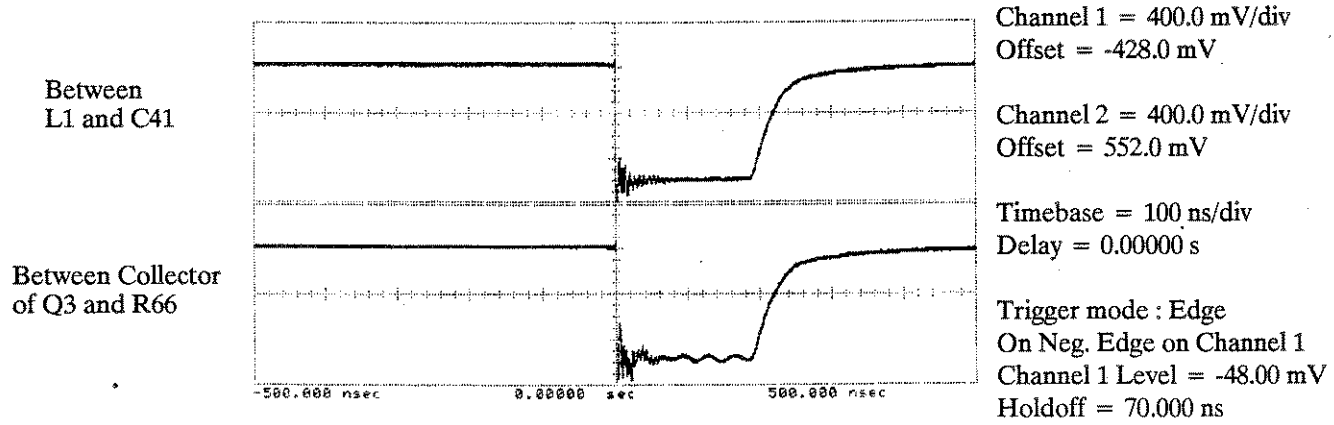


Figure 6C-61. With Pulse Filter Installed in Test Set, on the Horizontal Assembly, 100 ns/div.

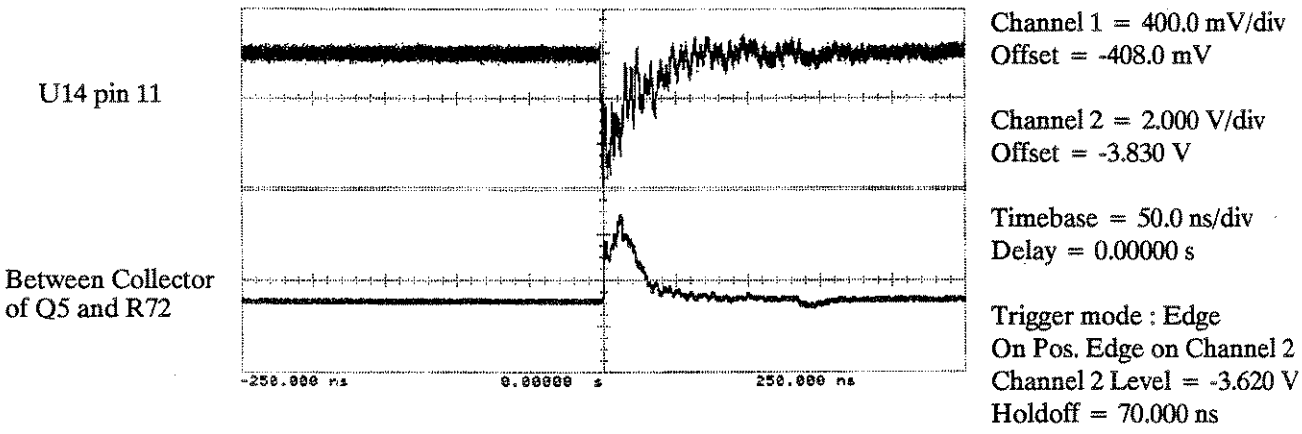


Figure 6C-62. With Pulse Filter Installed in Test Set, on the Horizontal Assembly, 20 ns/div, Trigger Mode Channel 2 Edge.

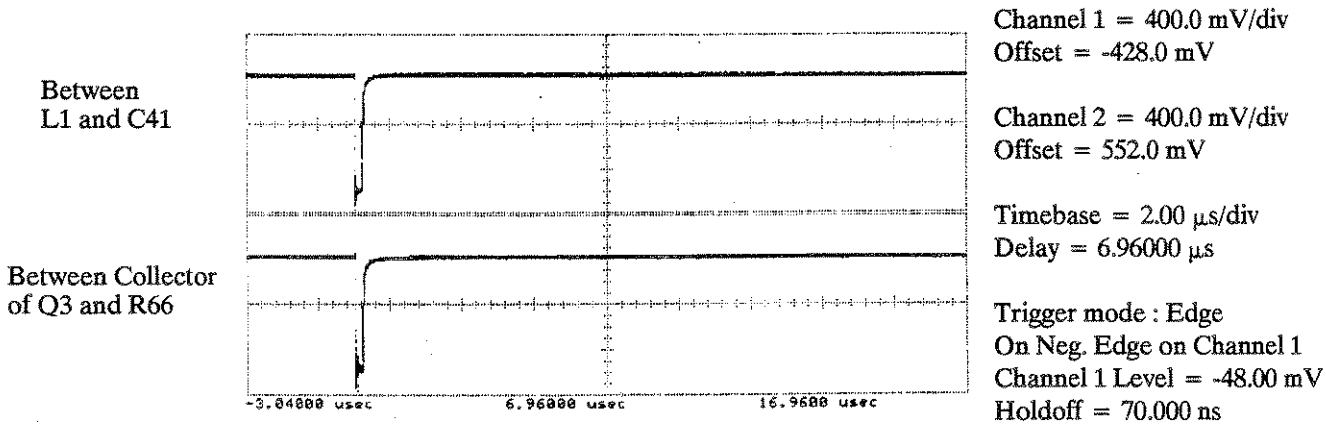


Figure 6C-63. With Pulse Filter Removed from Test Set, on the Horizontal Assembly, 2 µs/div.

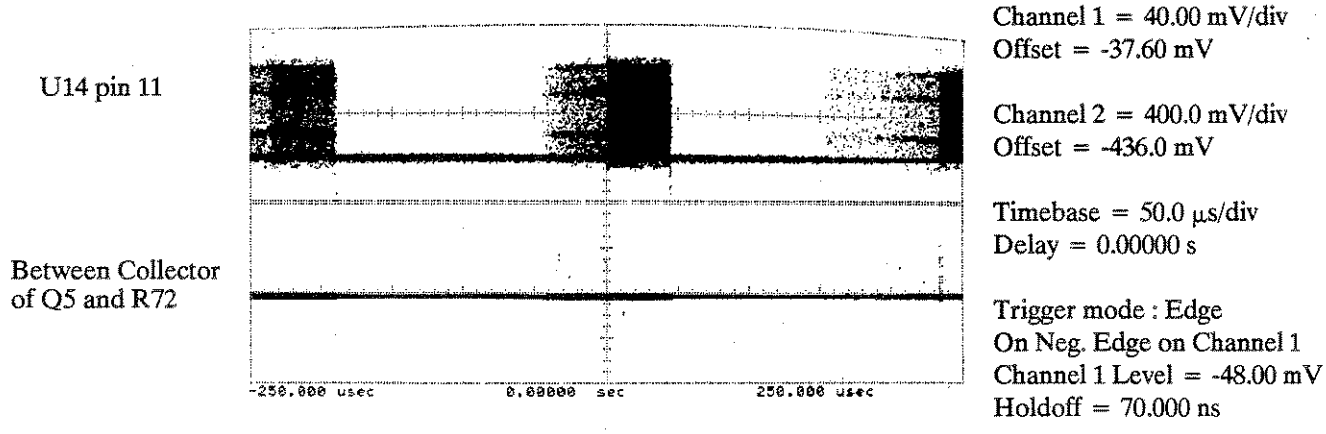


Figure 6C-64. With Pulse Filter Removed from Test Set, on the Horizontal Assembly, 50 µs/div.

TDR Test

This is a front panel test which determines if the TDR system is working properly. For this test to work, it requires at least one good channel other than channel 1. The TDR specifications are checked in channel 1 and the good channel. If either channel fails, suspect a faulty channel. If both channels fail, suspect a faulty TDR system.

1. Perform one key-down powerup routine. Change display to single screen.

2. Press **Network** menu key and press **Reflect/Trans/Cal** key until **Cal** is highlighted. Press **Preset Reflect Channel** key.

3. Measure the following pulse parameters on channel 1.

Parameter	**Approximate Expected Results**
Risetime	45 ps
Vtop	200 mV
Vbottom	0 V
Overshoot	3 %
Preshoot	3 %

4. If the measured results are within 100% of the expected results, perform the TDR step generator adjustments, than repeat this procedure's steps 1-4. If the measured results are still off, perform vertical adjustment, than repeat this procedure's steps 1-5.

5. If the measured results are still more than 100% off, than this channel fails. Continue with step 7.

6. Connect a semi-rigid S and U cable through an APC 3.5 (f-f) adapter from channel 1 to channel 3.

7. Turn channel 3 on. Press Preset Reflect Channel key.

8. Change sweep speed to 1 ns/div and channel 1 offset to -500 mV.

9. Measure the following pulse parameters on channel 3.

Parameter	**Approximate Expected Results**
Risetime	60 ps
Vtop	200 mV
Vbottom	0 V
Overshoot	4 %
Preshoot	4 %

10. If the measured results are more than 100% off, this channel fails.

11. Return to the flow diagram.

TDR System Test

This test determines which TDR part is faulty: TDR step generator, TDR drive circuitry, or delay line.

1. Perform one key-down powerup routine.

2. Change display to single screen, and turn channels 2-4 off.

3. Press **Network** menu key, press **Reflect/Trans/Cal** key until **Cal** is highlighted, press **Preset Reflect Channel** key.

4. If a pulse appears on channel 1, go to step 5; otherwise go to step 8.

5. Perform TDR step adjustments in section 4.

6. If the TDR step adjustments do not work properly, replace the TDR generator. Repeat the TDR step adjustment. If the adjustments still do not work properly, replace the horizontal assembly.

7. Return to flow diagrams.

8. Remove the test set's top and bottom covers.

9. Probe the following points. If they are good, the TDR system is probably good. If they are bad, the timebase or trigger system is bad; return to the flow diagram.

   U4 pin 6 — U4 pin 8 — Figure 6C-65

   Junction of R173-R31 — U4 pin 4 — Figure 6C-66

10. Disconnect TDR delay line (W15) from horizontal assembly.

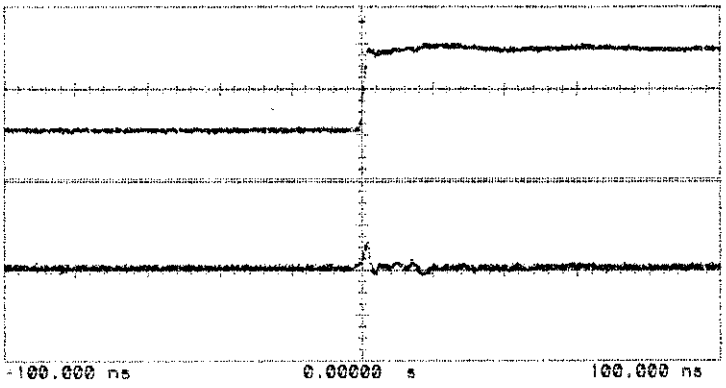
11. Probe the following points. If they are good, replace the TDR step generator; otherwise replace the horizontal assembly.

    U4 pin 6 — U4 pin 8 — Figure 6C-67

    Junction of R173-R3 — U4 pin 4 — Figure 6C-68

U4 pin 6

U4 pin 8



Channel 1 = 400.0 mV/div
Offset = -388.0 mV

Channel 2 = 200.0 mV/div
Offset = -756.0 mV

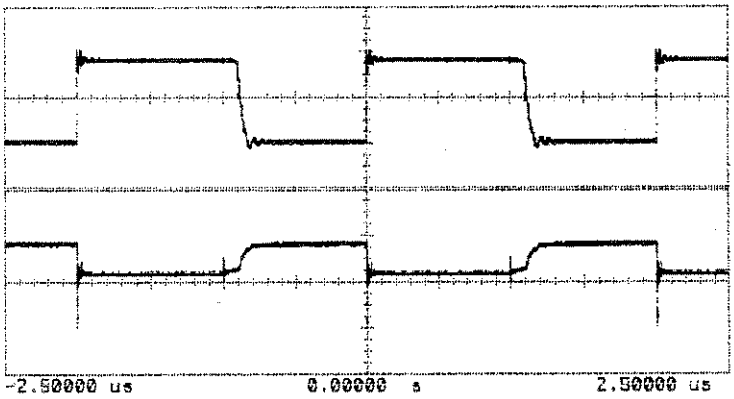
Timebase = 20.0 ns/div
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 1
Channel 1 Level = -388.0 mV
Holdoff = 70.000 ns

Figure 6C-65. On the Horizontal Assembly.

Junction of
R173 and C56

U4 pin 4



Channel 1 = 2.000 V/div
Offset = 720.0.0 mV

Channel 2 = 1.000 V/div
Offset = 1.360 V

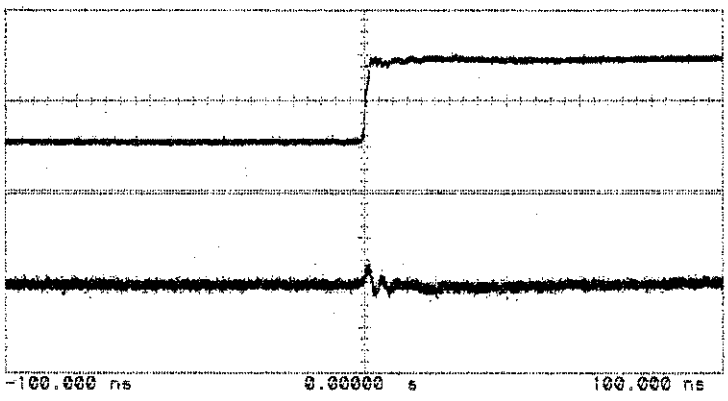
Timebase = 500 ns/div
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 1
Channel 1 Level = 720.0 mV
Holdoff = 70.000 ns

Figure 6C-66. On the Horizontal Assembly.

U4 pin 6

U4 pin 8



Channel 1 = 400.0 mV/div
Offset = -382.0 mV

Channel 2 = 200.0 V/div
Offset = -738.0 mV

Timebase = 20.0 ns/div
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 1
Channel 1 Level = -382.0 mV
Holdoff = 70.000 ns

Figure 6C-67. On the Horizontal Assembly.

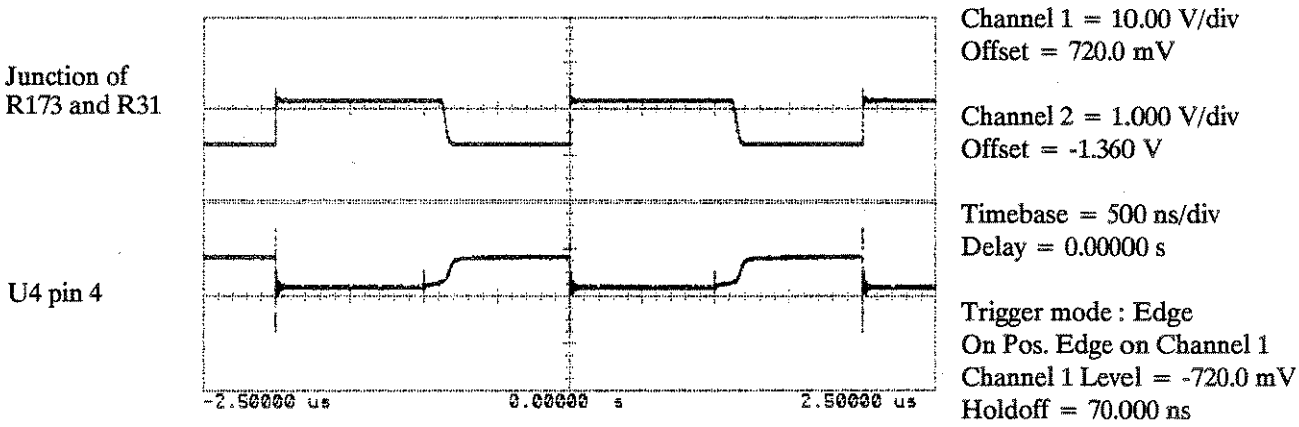


Figure 6C-68. On the Horizontal Assembly.

Trigger Test

This is a quick front panel test to see if the instrument is receiving triggers in both the triggered and freerun modes. The message "Running" on the screen's top left corner DOES NOT indicate the instrument is receiving triggers, it indicates the RUN key has been pressed.

1. Apply a 100 kHz sine wave with an amplitude of 100 mV and offset of 0 V to the external trigger input and press the Autoscale key.
2. Change to trg'd mode and 0 V trigger level, average mode with 2048 averages.
3. Press **Clear Display** key.
4. If the number of averages increases, the instrument is receiving triggers in the trg'd mode.
5. Remove the signal from the external trigger input and attach an SMA short to the external trigger input.
6. Change the timebase mode to freerun and press the Clear Display key.
7. If the number of averages increases, the freerun mode is operational.

Probing Trigger Test

This test verifies the trigger hybrid is functioning properly. External triggers are applied to the instrument and the trigger hybrid's output lines are checked. If this test fails, the timebase/trigger test should be performed to determine if the trigger hybrid is functioning properly. If this test passes, the horizontal test should be performed to find out why the trigger signal is not being received.

1. Remove the test set's top and bottom covers.

2. Apply a 20 MHz sine wave with an amplitude of 300 mV and an offset of 0 V to a power splitter. Connect the power splitter to channel 1 and to the external trigger input.

3. Perform a one key-down powerup routine. Press the **Autoscale** key. Change display persistence to 300 ms, trigger mode to trg'd.

4. Probe U1 pin 19 and expand the timebase to see the edge with high resolution. When trying to determine if this is a good signal, look for a clear stable trigger. If there are many misplaced dots to the edge's left or right side, or if there appears to be two edges, then the signal is faulty. The jitter test should be executed to determine if the quantity of misplaced dots are within specification.

5. Change the applied signal to 500 MHz. Probe U1 pin 19 Use the same criteria as step 4 to determine if the trigger is operating correctly.

6. If steps 4 and 5 are good, then the trigger circuit's normal triggered mode is good.

7. Remove the signal from the oscilloscope. Change the timebase mode to freerun and set freerun rate to 500 kHz.

8. Probe U1 pin 19 checking for stable signals. Change the freerun rate to each range possible and verify the trigger event rate is correct and the output is stable as defined in step 4. If all the trigger event rates are correct, the trigger circuit's freerun mode is good.

9. If both the triggered and freerun modes are correct, this test passes; otherwise it fails.

10. Return to the flow diagram.

Timebase/Trigger Test

This test verifies the horizontal assembly is applying the proper signals to the trigger hybrid. If this test passes, the probing trigger test should be run to see if the trigger hybrid is good. If this test fails, the umbilical input test should be run to determine the faulty module.

1. Perform one key-down powerup routine. Perform the umbilical input test for the following points: freerun clock, trig LEN/RESET, trigger slope, trigger hysteresis, and trigger level. If the above points are good proceed to step 3; otherwise this test fails and return to the flow diagrams.

2. Perform the umbilical input test for the following points. Refer to figure 6C-69.

In place of	Probe on trigger hybrid
U3 pin 16	U1 pin 22 (level shifted)
U3 pin 8	U1 pin 24 (less gain)

3. If these points are good, the trigger hybrid is receiving good signals and this test passes. Return to the flow diagrams.

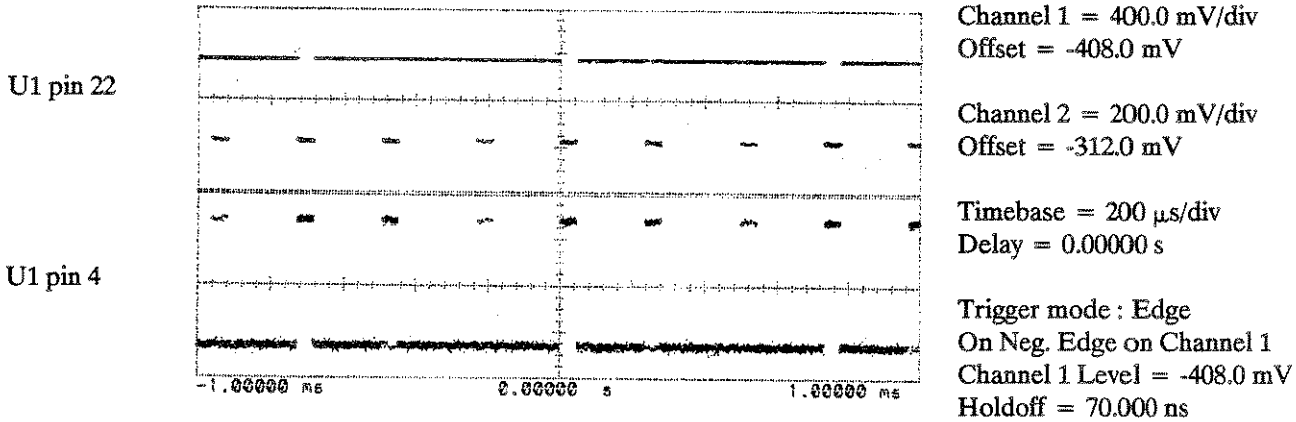


Figure 6C-69. On the Horizontal Assembly.

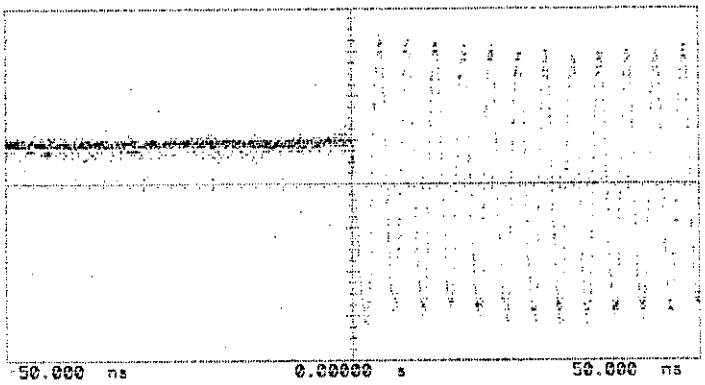
Horizontal Test

This test checks for a timebase fault in either the horizontal assembly, horizontal control assembly, or interconnect cable. The instrument is setup in a known operating state, and the interface between the two boards is probed.

1. Perform one key-down powerup routine.

2. Probe the points indicated on figures 6C-70 through 6C-77. If either U22 pin 11 or U3 pin 8 is bad, replace the horizontal control assembly. If J5 pin 11 is bad, go to the pulse filter troubleshooting flow diagram. If any of the remaining points are bad, replace the horizontal assembly.

U14 pin 4



Channel 1 = 100.0 mV/div
Offset = -362.0 mV

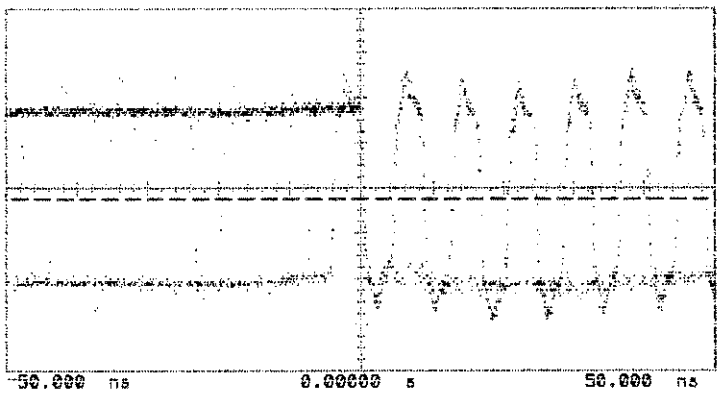
Channel 2 Off

Timebase = 10.0 ns/div
Delay = 0.00000 s

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -362.0 mV
Holdoff = 70.000 ns

Figure 6C-70. On the Horizontal Assembly, 1KDPU, Freerun

U15 pin 6

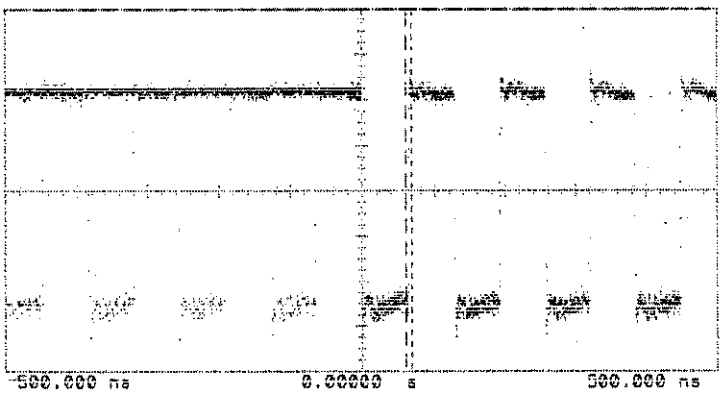


Channel 1 = 200.0 mV/div
Offset = -362.0 mV
Channel 2 Off

Timebase = 10.0 ns/div
Delay = 8.000 ns
Delta T = 8 ns
Start = 80.600 ns
Stop = 88.600 ns
Delta V = 0.000 V
Vmarker 1 & 2 = -412.0 mV
Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -362.0 mV
Holdoff = 70.000 ns

Figure 6C-71. On the Horizontal Assembly.

U16 pin 14



Channel 1 = 200.0 mV/div
Offset = -1.300 V
Channel 2 Off

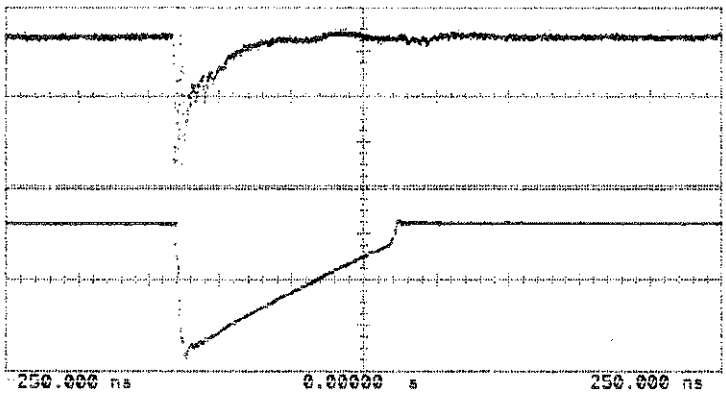
Timebase = 100 ns/div
Delay = 0.00000 s
Delta T = 8.000 ns
Start & Stop = 88.800 ns
Delta V = 0.000 V
Vmarker 1 & 2 = -412.0 mV

Trigger mode : Edge
On Neg. Edge on Channel 1
Channel 1 Level = -1.300 V
Holdoff = 70.000 ns

Figure 6C-72. On the Horizontal Assembly.

U14 pin 11

U22 pin 11



Channel 1 = 400.0 mV/div
Offset = -544.0 mV

Channel 2 = 4.000 V/div
Offset = -3.880 V

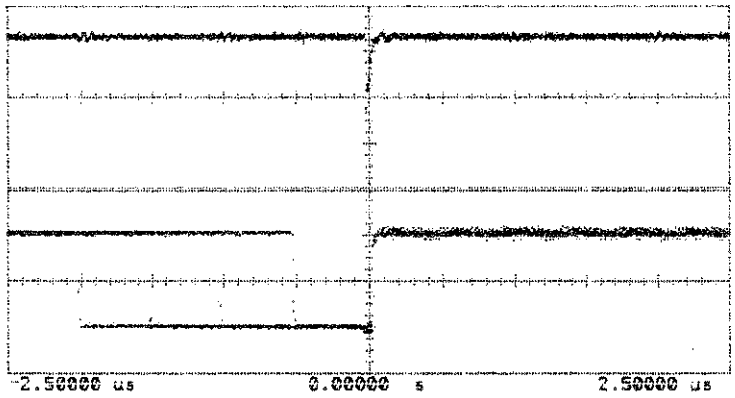
Timebase = 50.0 ns/div
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 2
Channel 1 Level = -2.180 V
Holdoff = 70.000 ns

Figure 6C-73. On the Horizontal Assembly.

U14 pin 11

U22 pin 11



Channel 1 = 400.0 mV/div
Offset = -544.0 mV

Channel 2 = 400.0 mV/div
Offset = -1.304 V

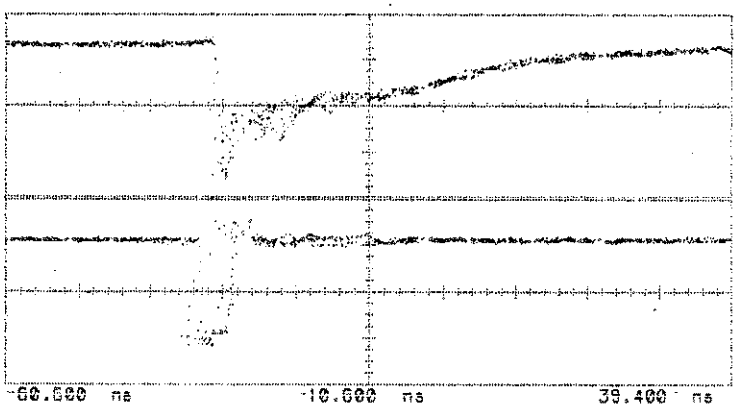
Timebase = 500 ns/div
Delay = 0.0000 s

Trigger mode : Edge
On Pos. Edge on Channel 1
Channel 1 Level = -372.0 mV
Holdoff = 70.000 ns

Figure 6C-74. On the Horizontal Assembly.

U14 pin 11

U22 pin 7



Channel 1 = 400.0 mV/div
Offset = -544.0 mV

Channel 2 = 400.0 mV/div
Offset = -1.304 V

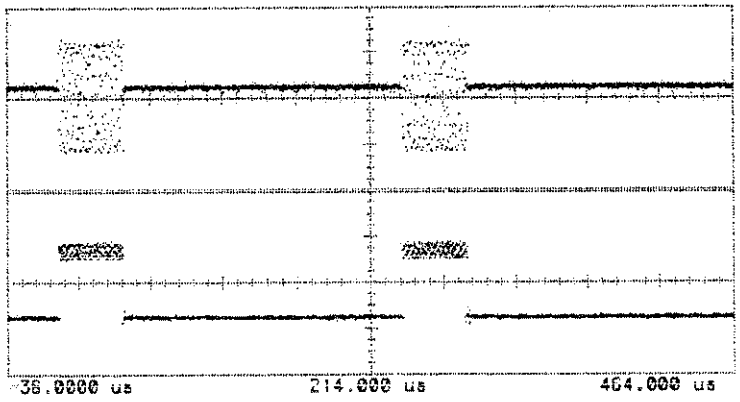
Timebase = 10.0 ns/div
Delay = 10.600 ns

Trigger mode : Edge
On Pos. Edge on Channel 1
Channel 1 Level = -324.0 mV
Holdoff = 70.000 ns

Figure 6C-75. On the Horizontal Assembly.

U14 pin 14

U1 pin 19



Channel 1 = 400.0 mV/div
Offset = -364.0 mV

Channel 2 = 400.0 mV/div
Offset = -276.0 mV

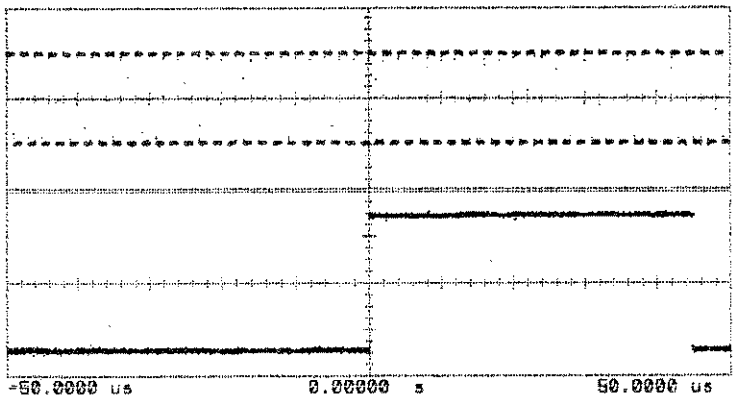
Timebase = 50.0 µs/div
Delay = 36.0000 µs

Trigger mode : Edge
On Pos. Edge on Channel 2
Channel 2 Level = -280.0 mV
Holdoff = 70.000 ns

Figure 6C-76. On the Horizontal Assembly.

U3 pin 8

U1 pin 19



Channel 1 = 400.0 mV/div
Offset = -368.0 mV

Channel 2 = 200.0 mV/div
Offset = -290.0 mV

Timebase = 10.0 µs/div
Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Channel 2
Channel 2 Level = -280.0 mV
Holdoff = 70.000 ns

Figure 6C-77. On the Horizontal Assembly.

HEWLETT PACKARD

SERVICE MANUAL

HP 54120B

Digitizing Oscilloscope Mainframe

SERIAL NUMBERS

This manual applies directly to instruments
prefixed with serial number:

2944A

With changes described within, this manual also
applies to instruments with serial prefixes:

2926A
2909A

For Additional Information about serial numbers see
Instruments Covered By This Manual
in Section 1.

Manual Part No. 54120-90908
Microfiche Part No. 54120-90808

Printed in U.S.A.: July 1989
Updated: October 1989

Herstellerbescheinigung

Hiermit wird bescheinigt, dass das Gerät/System HP 54120B in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist.

Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes/Systems angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Zusatzinformation für Mess- und Testgeräte

Werden Mess- und Testgeräte mit ungeschirmten Kabeln und/oder in offenen Messaufbauten verwendet, so ist vom Betreiber sicherzustellen, dass die Funkentstörbestimmungen unter Betriebsbedingungen an seiner Grundstücksgrenze eingehalten werden.

Manufacturer's Declaration

This is to certify that this product HP 54120B meets the radio frequency interference requirements of directive 1046/84. The German Bundespost has been notified that this equipment was put into circulation and was granted the right to check the product type for compliance with these requirements.

Additional Information for Test and Measurement Equipment

Note: If test and measurement equipment is operated with unshielded cables and/or used for measurements on open set-ups, the user must insure that under these operating conditions, the radio frequency interference limits are met at the border of his premises.

GEWERBEAUFSICHTSAMT STUTTGART

- Zentrale Stelle für Sicherheitstechnik und Vorschriftenwesen in Baden-Württemberg -

Gewerbeaufsichtsamt · Jägerstr. 89 · Postfach 703 · 7000 Stuttgart 1

Hewlett-Packard GmbH
Herrenberger Straße 110

7030 Böblingen

Stuttgart, den 02.06.1986
Fernsprecher
(0711) 2 05 01 (Behördenzentrum)
Durchwahl 2050 - 4798
Aktenzeichen: Z 5108/Hewlett-Packard/Ws/Vg
(Bitte bei Antwort angeben)

Betr.: Durchführung der Röntgenverordnung (RöV)
hier: Bauartzulassung gem. § 7 Abs. 2 RöV

Bezug: Ihr Antrag vom 22.05.1986; PSD US-ab

N a c h t r a g 1

zum Zulassungsschein Nr. BW/218/86/Rö

Aufgrund des § 7 Abs. 2 der Röntgenverordnung vom 1.3.1973 (BGBl. I S. 173) wird die der Firma Hewlett-Packard GmbH, Herrenberger Straße 110, 7030 Böblingen, erteilte Zulassung Nr. BW/218/86/Rö vom 16.01.1986 wie folgt erweitert:

Gegenstand:	Digital-Oszilloskop
Firmenbezeichnung:	HP Typ 54 111 D HP Typ 54 112 D HP Typ 54 120 A
Bauartunterlagen:	Service Manuals Nr. 54 111 - 90 902 vom 21.94.86 Nr. 54 112 - 90 902 vom 24.04.86 Nr. 54 120 - 90 902 vom 26.04.86

Die für den Strahlenschutz wesentlichen Merkmale entsprechen der bereits zugelassenen Ausführung.

Typenbezeichnung der Bildröhre, Auflagen, Hinweise und Befristung ergeben sich aus dem Zulassungsschein Nr. BW/218/86/Rö vom 16.01.1986.

Dieser Nachtrag gilt nur im Zusammenhang mit dem vollständigen Text des o.g. Zulassungsscheins.

Reutter

GEWERBEAUFSICHTSAMT STUTTGART

Dieses Gerät wurde nach den Auflagen der Zulassungsbehörde einer Stückprüfung unterzogen und entspricht in den für den Strahlenschutz wesentlichen Merkmalen der Bauartzulassung. Die Beschleunigungsspannung beträgt maximal 22,3 kV.

Hewlett-Packard
1900 Garden of the Gods Road
Colorado Springs
Colorado 80907, USA

GEWERBEAUFSICHTSAMT STUTTGART

- Zentrale Stelle für Sicherheitstechnik und Vorschriftenwesen in Baden-Württemberg -

Gewerbeaufsichtsamt · Jägerstr. 22 · Postfach 703 · 7000 Stuttgart 1

Stuttgart, den 16.01.1986
Fernsprecher
(0711) 2 05 01 (Behördenzentrum)
Durchwahl 2050 - 4798
Aktenzeichen: Z 5108/HP/Ws/Hh
(Bitte bei Antwort angeben)

Firma
Hewlett Packard GmbH
Herrenberger Str. 110/130

7030 Böblingen

Zulassungsschein Nr. BW/218/86/Rö

Gemäß § 9 der Röntgenverordnung vom 01.03.1973 (BGBl. I S. 173) wird die Zulassung der Bauart durch den Bauartzulassungsbescheid vom 16.01.1986 mit Aktenzeichen Z 5108/HP/Ws/Hh für den nachfolgend aufgeführten Störstrahler bescheinigt:

Gegenstand	:	Digital-Oszilloskop
Firmenbezeichnung	:	HP Typ 54110D
Bildröhre	:	Sony Typ M23 JHU 15X
Hersteller	:	Hewlett-Packard 1900 Garden of the Gods Road Colorado Springs Colorado 80907, USA
Betriebsbedingungen	:	Hochspannung: max. 22,3 kV Strahlstrom: max. 0,4 mA
Zulassungskennzeichen	:	BW/218/86/Rö

Die Bauartzulassung ist befristet bis 16.01.1996.

Für den Strahlenschutz wesentliche Merkmale

1. Die Art und Qualität der Bildröhre,
2. die der Hochspannungserzeugung und -stabilisierung dienenden Bauelemente.

Auflagen:

1. Die Geräte sind bezüglich der für den Strahlenschutz wesentlichen Merkmale entsprechend den vorgestellten und geprüften Mustern und Antragsunterlagen herzustellen.

2. Die Geräte sind einer Stückprüfung daraufhin zu unterziehen, ob sie bezüglich der für den Strahlenschutz wesentlichen Mermale der Bauartzulassung entsprechen.

   Die Prüfung muß umfassen:

   a) Kontrolle der Hochspannung an jedem einzelnen Gerät,

   b) Messung und Dosisleistung nach Festlegung im Bauartzulassungsbescheid.

3. Die Herstellung und die Stückprüfung sind durch den von der Zulassungsbehörde bestimmten Sachverständigen überwachen zu lassen.

4. Die Geräte sind deutlich sichtbar und dauerhaft mit dem Kennzeichen

   BW/218/86/Rö

   zu versehen sowie mit einem Hinweis folgenden Mindestinhalts:

   "Die in diesem Gerät entstehende Röntgenstrahlung ist ausreichend abgeschirmt. Beschleunigungsspannung maximal 22,3 kV."

Hinweis für den Benutzer des Geräts:

Unsachgemäße Eingriffe, insbesondere Verändern der Hochspannung oder Auswechseln der Bildröhre können dazu führen, daß Röntgenstrahlung in erheblicher Stärke auftritt. Ein so verändertes Gerät entspricht nicht mehr dieser Zulassung und darf infolgedessen nicht mehr betrieben werden.

Reutter

GEWERBEAUFSICHTSAMT STUTTGART

Dieses Gerät wurde nach den Auflagen der Zulassungsbehörde einer Stückprüfung unterzogen und entspricht in den für den Strahlenschutz wesentlichen Merkmalen der Bauartzulassung. Die Beschleunigungsspannung beträgt maximal 22,3 kV.

Hewlett-Packard
1900 Garden of the Gods Road
Colorado Springs
Colorado 80907, USA

X-RAY RADIATION NOTICE

ACHTUNG Model **54111D/54112D/54120A** **WARNING**

Während des Betriebs erzeugt dieses Gerät Röntgenstrahlung. Das Gerät ist so abgeschirmt, daß die Dosisleistung weniger als 36 pA/kg (0,5 mR/h) in 5cm Abstand von der Oberfläche der Katodenstrahlröhre beträgt. Somit sind die Sicherheitsbestimmungen verschiedener Länder, u.A. der deutschen Röntgenverordnung eingehalten.

Die Stärke der Röntgenstrahlung hängt im Wesentlichen von der Bauart der Katodenstrahlröhre ab sowie von den Spannungen, welche an dieser anliegen. Um einen sicheren Betrieb zu gewährleisten, dürfen die Einstellungen des Niederspannungs— und Hochspannungsnetzteils nur nach der Anleitung in Kapitel Einstellvorschriften des Service Handbuches vorgenommen werden.

Die Kathodenstrahlröhre darf nur durch die gleiche Type ersetzt werden. (Siehe Kapitel Ersatzteile für HP-Teilenummern.)

Das Gerä ist in Deutschland zugelassen unter

der Nummer: **BW/218/86/ROE**

When operating, this instrument emits x-rays; however, it is well shielded and meets safety and health requirements of various countries, such as the X-ray Radiation Act of Germany.

Radiation emitted by this instrument is less than 0.5 mR/hr at a distance of five (5) centimeters from the surface of the cathode-ray tube. The x-ray radiation primarily depends on the characteristics of the cathode-ray tube and its associated low-voltage and high-voltage circuitry. To ensure safe operation of the instrument, adjust both the low-voltage and high-voltage power supplies as outlined in the Adjustments Section of the Service Manual.

Replace the cathode-ray tube with an identical CRT only. Refer to the Replacement Parts Section for proper HP part number.

Number of German License: **BW/218/86/ROE**

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CWA388

Safety Considerations

General Operation

This is a Safety Class I instrument (provided with terminal for protective earthing). BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

General Warnings and Cautions

- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

Safety Symbols

Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.

Indicates Hazardous Voltages

Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

Warning 

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

Caution 

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software and/or firmware code may be printed before the date; this indicates the version level of the software and/or firmware of this product at the time of the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Edition 1	July 1989	54120-90908
Update 1	October 1989	54120-90908

List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in Printing History and on the title page.

Pages	Effective Date
all	July 1989
Title page, iii, iv, 5-8, 5-9	October 1989

Contents

Section 4

Section 5

Section 6A

Section 6B

Section 6C

Section 6D

Appendix A

List of Illustrations

List of Tables

Table Of Contents

General Information

General Information 1

Introduction

A service manual is supplied with the four channel test set you ordered along with the HP 54120B. To complete the service documentation for your system, unpack the four channel test set service manual and place it in the three ring binder supplied with the HP 54120B service manual.

This service manual contains information necessary to test, adjust and service the Hewlett-Packard 54120B Digitizing Oscilloscope Mainframe. This manual is divided into 9 sections as follows:

- 1 - General Information
- 2 - Installation
- 3 - Performance Tests
- 4 - Adjustments
- 5 - Replaceable Parts
- 6A - Disassembly
- 6B - Theory
- 6C - Service Menu Keys
- 6D - Troubleshooting

Information on operating, programming, and interfacing the HP 54120B is contained in the front panel operation reference supplied with each instrument.

The "General Information" section includes a description of the HP 54120B Digitizing Oscilloscope Mainframe, general characteristics, safety considerations, instruments covered by this manual, options, accessories supplied, recommended test equipment, and X-ray license forms. Specifications and operating characteristics are listed with the service manual for the four channel test set.

Also listed on the title page of this manual is a microfiche part number. This number can be used to order 4 x 6 inch microfilm transparencies of this manual. Each microfiche contains up to 96 photo-duplicates of manual pages. The microfiche package also includes the latest Manual Changes supplement as well as pertinent Service Notes.

Description

The HP 54120B is a fully programmable digitizing oscilloscope mainframe with a nine inch color display. The mainframe is capable of automated measurements and digital storage.

The color display provides several colors which are mapped to provide specific colors for specific display functions. For example, channel 1 is displayed in yellow, channel 2 in green, and error messages are displayed in red.

The HP 54120B contains extensive self-tests to ensure proper functioning of the oscilloscope. These self-tests are in addition to internal diagnostics that help locate faults efficiently and identify repairs, if a failure does occur.

Specifications & Operating Characteristics

All specifications and instrument operating characteristics are listed with the service manual for the four channel test set.

General Characteristics

The following general characteristics are not specifications, but typical characteristics included as additional information only.

Environmental Conditions

Temperature Operating: +15° C to +35° C (+59° F to +95° F).

Temperature Non-operating: -40° C to +70° C (-40° F to +158° F).

Humidity Operating: Up to 90% relative humidity at +35° C (95° F).

Humidity Non-operating: Up to 95% relative humidity at +65° C (+149° F).

Altitude Operating: Up to 4600 metres (15,000 ft).

Altitude Non-operating: Up to 15,300 metres (50,000 ft).

Vibration Operating: Random vibrations 5-500 Hz, 10 minutes per axis, ~0.3 g (rms).

Vibration Non-operating: Random vibration 5-500 Hz, 10 minutes per axis, =2.41 g (rms); and swept sine resonant search, 5-500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Power Requirements

Power requirements listed are for the HP 54120B combined with a four channel test set. The four channel test set obtains its power over the provided interface cable from the HP 54120B.
Voltage: 115/230 Vac, -25% to + 15%, 48-66 Hz.
Power: 200 watts, 400 VA maximum.

Weight

HP 54120B Net: Approximately 20.5 kg (45 lb).

Dimensions

Dimensions are for general information only. If dimensions are required for building a special enclosure, contact your local Hewlett-Packard sales office. Dimensions are in millimetres and (inches). Refer to figure 1-1.

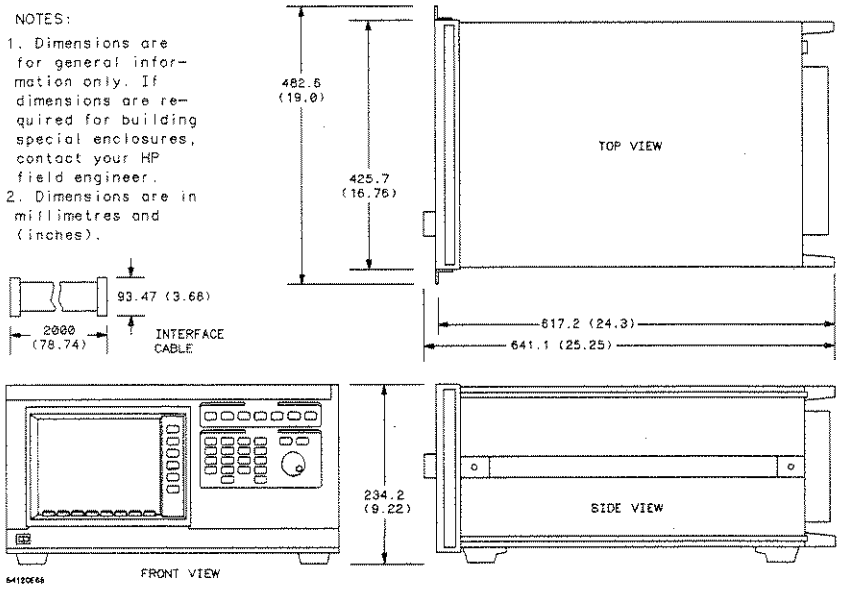


Figure 1-1. HP 54120B Dimensions

Safety Considerations

The appropriate sections contain safety information relevant to the service procedure it describes. Both the HP 54120B and this manual should be reviewed for safety markings and instructions before work is begun. Refer to the pages following the title page for safety summary and safety considerations.

Instruments Covered By This Manual

The HP 54120B's serial number is on the rear panel. Hewlett-Packard uses a two-part serial number consisting of a four-digit prefix and a five-digit suffix separated by a letter (0000A00000). The prefix is the same for all identical oscilloscopes and changes only when a modification is made that affects parts compatibility. The suffix differs for each oscilloscope. This manual applies directly to instruments with the serial prefix shown on the title page.

Options

The following options are available for the HP 54120B:

- Option 908 - Rack mount kit
- Option 910 - Additional copies of front panel operation reference
- Power cord options (see table 2-1)

Accessories Supplied

The following accessories are supplied with the HP 54120B.

- This Service Manual
- Getting Started Guide
- Front Panel Operation Reference
- Programming Reference Manual
- Antistatic mat with wrist strap (HP Part Number 9300-1346)

Accessories Available

The following accessories are available for the HP 54120B:

- Accessory kit HP 54007A
- 6 GHz Probe kit HP 54006A
- 22 ns Delay Line HP 54008A

Recommended Test Equipment

The test equipment recommended for maintaining the HP 54120B is listed in table 1-1. Any equipment which satisfies the critical specificatioins may be used. Section 4, Adjustments, is the only section which requires test equipment.

Table 1-1. Recommended Test Equipment

Instrument	Critical Specifications	Model
DMM	Better than 0.3% accuracy	HP 3478
Clip lead	Aligator to alligator	N/A

Systemizing

At the factory the HP 54120B Digitizing Oscilloscope Mainframe and the four channel test set are calibrated together as a system. This system will meet all published specifications when shipped from the factory. If the system is split up, (a different four channel test set is used with the HP 54120B) refer to the four channel test set service manual, "General Information" section, systemizing paragraph for your instrument.

Table Of Contents

Installation

Installation 2

Introduction

This section contains installation instructions, information about operating environments, cleaning the HP 54120B, storage, and shipment.

Preparation For Use

Caution

To prevent damage to the instrument, make sure the line voltage selector switch is in the correct setting for your AC voltage source.

Power Requirements

The HP 54120B requires a power source of 115 or 230 Vac +15/-25 percent; 48 to 66 Hz single phase. Power consumption is 200 watts or 400 VA maximum.

Line Voltage Selection

A blade-type screwdriver may be used to change the position of the line select switch on the read panel to the correct voltage selection. Correctly setting the line switch sets the correct circuit breaker trip current. For 100 volt line operation, the line switch must be in the 115 V position.

Power Cables

This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. See Table 2-1 for option numbers of available power cables and plug configurations.

Warning

To protect operating personnel from possible injury or death, the chassis must be properly grounded. The proper power cord must be used and the power cord ground must NOT be defeated. Refer to table 2-1 for power cable description and application.

Operating Environment

The operating environment is noted in the General Information section under General Characteristics. Note the non-condensing humidity limitation. Avoid condensation within the instrument because it can cause poor operation or malfunction.

Test Set Connection

Always insure a four channel test set is connected to the HP 54120B before applying power to the HP 54120B.

The HP 54120B Digitizing Oscilloscope Mainframe is connected to a four channel test set by the umbilical cable, HP Part Number 54120-61618. Connect the umbilical cable to the interface cable ports on the mainframe and four channel test set. Refer to figure 2-1. The mainframe supplies all power for the four channel test set over the umbilical cable.

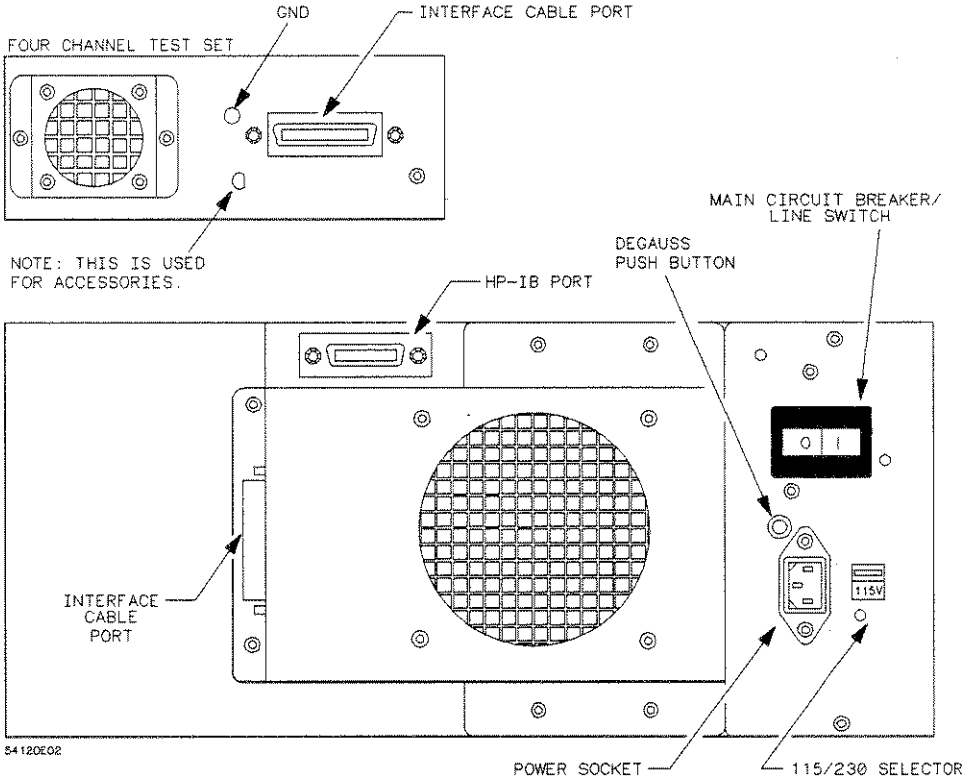


Figure 2-1. Rear Panel of Mainframe and Test Set

Cleaning

When cleaning the HP 54120B, CAUTION must be exercised about which cleaning agents are used. USE MILD SOAP AND WATER. If a harsh soap or solvent is used, the water-base paint finish WILL BE DAMAGED.

Caution

BE CAREFUL when cleaning the keyboard. Water can damage the keyboard circuit if it seeps under the keys.

Storage And Shipment

The instrument may be stored or shipped in environments with the following limits:

Temperature: -40° C to +70° C (-40° F to +158° F)
Humidity: Up to 95% at +65° C (+149° F)
Altitude: Up to 15,300 metres (50,000 feet)

Tagging For Service

The instrument should also be protected from temperature extremes which cause condensation within the instrument. Condensation within the instrument may cause a malfunction.

If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of servicing required, return address, model number, and full serial number. In any correspondence refer to the instrument by model number and full serial number.

Packaging

Original packaging i.e., containers and material identical to those used in factory packaging are available from Hewlett-Packard. If other packaging is to be used the following general instructions for repackaging with commercially available materials should be followed:

a. Wrap the oscilloscope in heavy paper or plastic.

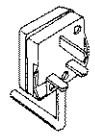
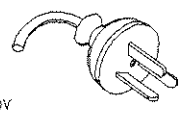
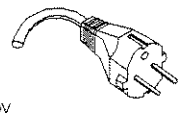
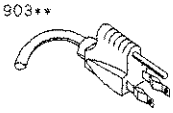
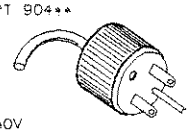
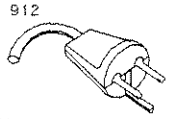
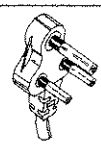
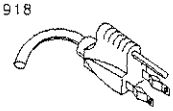
b. Use a strong shipping container. A double wall carton made of 2.4 MPa (350 psi) test material is adequate.

c. Use a layer of shock absorbing material 75 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside the container. Protect the control panel with cardboard.

d. Seal the shipping container securely.

e. Mark the shipping container FRAGILE to ensure careful handling.

Table 2-1. Power Cord Configurations

PLUG TYPE	CABLE PART NO.	PLUG DESCRIPTION	LENGTH IN/CM	COLOR	COUNTRY
OPT 900  250V	8120-1351 8120-1703	Straight *BS1363A 90°	90/228 90/228	Gray Mint Gray	United Kingdom, Cyprus, Nigeria, Zimbabwe, Singapore
OPT 901  250V	8120-1369 8120-0696	Straight *NZSS198/ASC 90°	79/200 87/221	Gray Mint Gray	Australia New Zealand
OPT 902  250V	8120-1689 8120-1692 8120-2857	Straight *CEE7-Y11 90° Straight (Shielded)	79/200 79/200 79/200	Mint Gray Mint Gray Coco Brown	East and West Europe, Saudi Arabia, So. Africa, India (Unpolarized in many nations)
OPT 903**  125V	8120-1378 8120-1521 8120-1992	Straight *NEMA5-15P 90° Straight (Medical) UL544	90/228 90/228 96/244	Jade Gray Jade Gray Black	United States, Canada, Mexico, Phillipines, Taiwan
OPT 904**  250V	8120-0698	Straight *NEMA6-15P	90/228	Black	United States, Canada
OPT 905  250V	8120-1396 8120-1625	CEE22-V1 (System Cabinet Use) 250V	30/76 96/244	Jade Gray	For interconnecting system components and peripherals. United States and Canada only
OPT 906  250V	8120-2104 8120-2296	Straight *SEV1011 1959-24507 Type 12 90°	79/200 79/200	Mint Gray Mint Gray	Switzerland
OPT 912  220V	8120-2956 8120-2957	Straight *DHCK107 90°	79/200 79/200	Mint Gray Mint Gray	Denmark
OPT 917  250V	8120-4211 8120-4600	Straight SABS164 90°	79/200 79/200	Jade Gray	Republic of South Africa India
OPT 918  100V	8120-4753 8120-4754	Straight Miti 90°	90/230 90/230	Dark Gray	Japan

Rev. 11NOV86 ART00019

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP part number for complete cable including plug.

**These cords are included in the CSA certification approval of the equipment.

E=Earth Ground
L=Line
N=Neutral

Performance Tests 3

Introduction

This section normally contains the performance verification tests. Since there are no specifications for the mainframe to test, there are no performance tests for the mainframe. Refer to the four channel test set service manual for the performance tests.

Table of Contents

Adjustments

Adjustments 4

Introduction

This section describes the adjustments for returning the instrument to peak operating capabilities after repairs have been made or during routine preventive maintenance.

Warning 

Read the "Safety Summary" at the front of this manual before performing adjustment procedures. The instrument should be disconnected from all voltage sources before it is opened for any adjustments, replacements, maintenance, or repairs.

Adjustment Interval

Adjustments are needed if the test set fails to pass the performance verification test in the test set service manual. Some or all of these adjustments may need to be made after repairs have been completed. Amount of use, environmental conditions, and the user's experience concerning need for adjustment verification will contribute in deciding the adjustment interval. Also refer to the "Performance Test Interval" in the performance tests section of the test set service manual.

Recommended Test Equipment

Table 1-1 lists the recommended test equipment to use for the adjustment procedures. Any equipment that satisfies the critical specifications may be used.

Adjustment Sequence

This is the factory recommended sequence of adjustments.

Note 

The mainframe adjustments must be performed before the test set adjustments are performed.

- Power Supply Adjustments
- Timebase Delta Current Adjustment
- +10.000 Reference Voltage Adjustment

Power Supply Adjustments

This procedure is for adjusting the power supply voltages in cases when either the power supplies have been inadvertently misadjusted or when repairs have been made.

Note

The power supply voltages are factory set and rarely require readjustment.

Equipment

This is a list of the recommended test equipment for this adjustment. However, any instrument which satisfies the critical specifications may be used.

Instrument	Critical Specifications	Model
DMM	Better than 0.3% accuracy	HP 3478A

Analog Supply

This adjustment was never installed on HP 54120B mainframes. If you have an older HP 54120A mainframe you need to check to see if your instrument contains A12R61 before continuing with this procedure. A12R61 was the only adjustment on the Analog Power Supply assembly. The test point locations are marked on the power supply cover and on the Analog PC assembly (A12). This procedure adjusts the fan supply voltage.

Note

The instrument must be stabilized at ambient temperature with front-panel power switch to STBY before this adjustment is made. The fan voltage will increase with the instrument's internal temperature. If the instrument is not allowed to cool down, the following voltage measurement and adjustment will be inaccurate.

1. Remove two top rear feet from mainframe.
2. Remove top cover from mainframe.
3. Connect positive voltmeter lead to FAN test point.
4. Connect negative voltmeter lead to -18 V test point.
5. Turn instrument on.
6. Before the instrument warms up, adjust A12R61 for a voltmeter reading of 9.5 V $\pm$ 100 mV.

Digital Supply

The test point locations are marked on the power supply cover and on the Digital PC assembly (A13). A13R56 is the only adjustment on the Digital Power Supply assembly. First, the voltage is measured to see if any adjustment is required.

1. Turn instrument on and allow it to warm up for approximately two minutes.
2. Connect positive voltmeter lead to +5 V test point (actual voltage = +5.1 V).
3. Connect negative voltmeter lead to -5 V test point (actual voltage = -5.3 V).
4. The voltmeter should read +10.4 Vdc ±10 mV. If the measurement is within specifications, stop here. If the measurement is out of specifications, then continue with steps 5 through11.
5. Disconnect power cord from rear of instrument and remove voltmeter leads.

Warning 

Hazardous voltages capable of causing injury or death are present on the AC Power Supply assembly (A11) when power is applied and for a period of time after power is removed from the instrument. To avoid this hazard, DO NOT remove the power supply shield until the LED on the AC Power Supply assembly (A11) is extinguished. This LED is visible through an inspection hole in the cover labeled "+300 V WHEN LAMP IS ON".

6. When the +300 V lamp is extinguished, remove the top power supply cover.
7. Reconnect positive voltmeter lead to +5 V test point.
8. Reconnect negative voltmeter lead to -5 V test point.
9. Reconnect power cord and turn instrument on. Allow instrument to warm up for approximately two minutes.
10. Adjust A13R56 for a voltmeter reading of +10.4 Vdc ±10 mV.
11. Disconnect power cord and wait until +300 V lamp is extinguished.
12. Disconnect voltmeter leads before reinstalling power supply cover.

Timebase Delta Current Adjustment

This is a timebase system adjustment. After this adjustment is made, any four channel test set may be used with this mainframe without degrading the timebase accuracy specifications. A3R29, on the Horizontal Control board, is adjusted for proper delta (change) in output current flow from the fine delay DAC on the Horizontal Control board to the four channel test set is, when delay is switched from 16.000 ns to 19.999 ns.

The procedure consists of three main parts.

1. Steps 1 through 6 measure the resistance of A3R46. This is the resistance value in the ohm's law formula $I = E \div R$ used in step 12.

2. Steps 6 through 12 measure the voltage across A3R46 with the oscilloscope's timebase delay set to 16.000 ns. This is the voltage value in the ohm's law formula $I = E \div R$ used in step 12.

3. Steps 13 through 21 calculate the desired delta current across A3R46 when the oscilloscope's timebase delay is changed from 16.000 ns to 19.999 ns. A3R29 is adjusted if the measured delta current does not equal the desired delta current.

Equipment

This is a list of the recommended test equipment for this adjustment. However, any instrument which satisfies the critical specifications may be used.

Instrument	Critical Specifications	Model
DMM	40 μV and 24 milliohm accuracy	HP 3478A
Clip lead	Alligator to alligator	N/A

Procedure

Part 1: Determining R in the ohm's law formula I = E ÷ R

1. Turn mainframe's front-panel power switch to STBY.

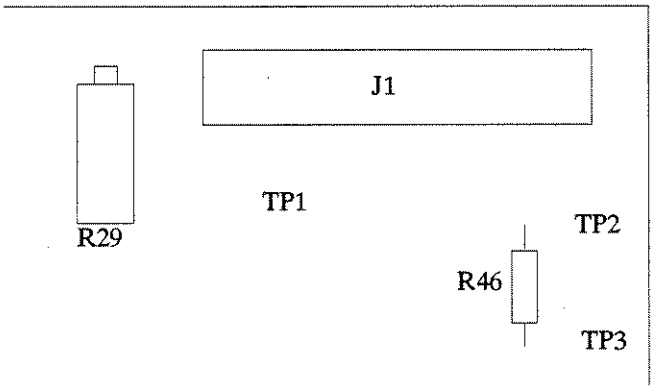
2. Place DMM in four-wire resistance measurement mode.

3. Connect one end of alligator clip lead to (A3) TP2.

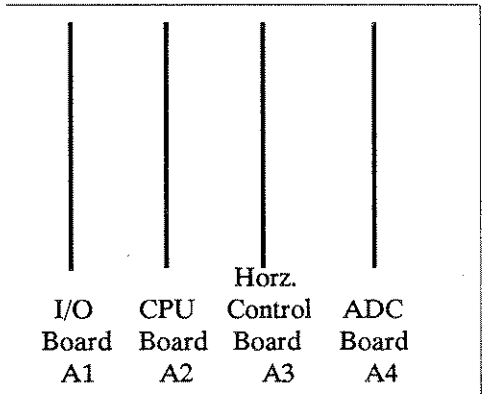
4. Connect both positive DMM leads to other end of alligator clip lead.

5. Connect both negative DMM leads to ground point TP3.

Top-Rear Corner of Horizontal Control Assembly (A3)



Top View of Mainframe's Card Cage



Front of Card Cage Assembly

6. Record resistance reading in steps 12 and 14 (2 places after the decimal are required).
   Example: 200.06 Ω. Leave DMM connected across A3R46.

Part 2: Determining E in the ohm's law formula I = E ÷ R

7. Disconnect the ribbon cables which attach to the rear of the horizontal control and ADC assemblies.

8. Change DMM to make voltage measurements.

9. Short Horizontal Control assembly (A3) test point TP1 to TP2.

10. Turn mainframe power on, and set timebase delay to 16 ns.

11. Record DMM voltage reading in step 12 (5 places after the decimal are required).
    Example: -1.00039 V.

	Example
12. Record DMM voltage reading from step 11 here_____ V	-1.00039 V
Record DMM resistance reading from step 6 here _____ Ω	200.06 Ω
Divide voltage by resistance to obtain current _____ mA	5.0004 mA

(four digits after the decimal are required, and drop the negative sign).

The result of the calculation is the fine delay DAC output current at delay value of 16.000 ns. Record this value in step 13.

Part 3: Steps 13 through 21 calculate the value to which A3R29 should be set.

13. Subtract the current result in step 12 from desired delta current 9.7632 mA. 9.7632 mA - (_____ mA) = _____ mA. Record this value in step 14.

Example: 9.7632 mA - 5.0004 mA = 4.7628 mA

14. Convert calculated current from step 13 to a voltage value by multiplying it by the resistance value in step 6.

	Example
Record calculated current from step 13 here _____ mA	4.7628 mA
Record DMM resistance reading from step 6 here _____ Ω	200.06 Ω
Multiply resistance by current to obtain a voltage _____ V	0.95284576 V

15. Round voltage value from step 14 to 5 decimal places _____V 0.95285 V

16. Change mainframe's timebase delay setting to 19.999 ns.

17. With DMM still connected across TP2 and TP3, check DMM voltage reading. If voltmeter reading is equal to calculated voltage in step 15, then go to step 18. Otherwise, adjust A3R29 for a DMM voltage reading as close as possible to the calculated value in step 15.

18. Turn mainframe's front-panel power switch to STBY.

19. Remove short from TP1 to TP2.

20. Disconnect DMM from mainframe.

21. Reconnect ribbon cable disconnected in step 7.

+10 Volt Reference Adjustment

This is a systemizing adjustment which allows any test set to be used with this mainframe without degrading the vertical gain specifications.

Equipment

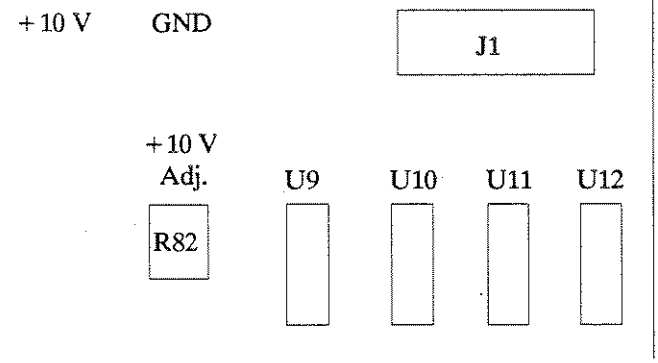
This is a list of the recommended test equipment for this adjustment. However, any instrument which satisfies the critical specifications may be used.

Instrument	Critical Specifications	Model
DMM	0.01% accuracy	HP 3478A

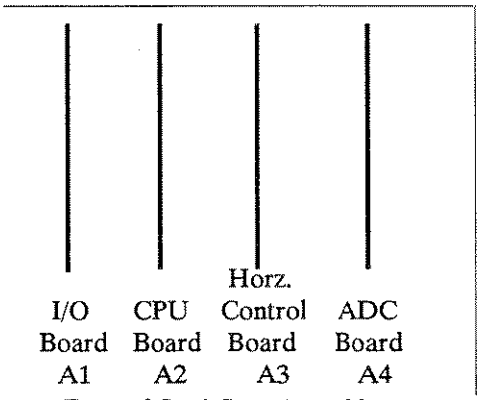
Procedure

1. Turn mainframe's front-panel power switch to STBY.
2. Connect positive DMM lead to +10 V test point on ADC assembly (A4).
3. Connect negative DMM lead to ground test point next to +10 V test point.
4. Turn mainframe's front-panel power switch to ON.
5. Adjust +10 V ADJUST (R82) for +10 V ±1 mV.
6. Disconnect DMM leads from ADC assembly.
7. Reinstall mainframe's top cover and two top rear feet.

Top-Rear Corner of ADC Assembly (A4)



Top View of Mainframe's Card Cage



Front of Card Cage Assembly

CRT Color Module Introduction

The CRT color module requires no adjusting when used in a normal environment. The procedure given here is for CRT color convergence. Do not perform these adjustments as part of regular maintenance. Observe the following rules before making the adjustments:

- Do not perform this procedure as normal maintenance.
- Make adjustments only if the instrument has been subjected to extreme magnetic environments and the colors are incorrect.
- Before making any adjustments, try degaussing the unit using the rear panel degaussing switch or a color television type degaussing coil (refer to Degaussing the Display procedure, this section).
- Only qualified personnel who are familiar with color CRT convergence procedures should perform this adjustment.
- Before adjustments are made, mark the position where potentiometers are. This allows you to return the adjustments to their original starting position.

Degaussing the Display

After the instrument has been used for a while, the CRT may become magnetized and color or other data may become distorted. To correct, press the **Degauss** button on the rear panel several times.

If the instrument has been subjected to strong magnetic fields, it may be necessary to degauss the CRT with a conventional television type degaussing coil.

Safety Considerations

Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with the precautions listed in the Safety Summary at the front of this manual, or with specific warnings given throughout this manual, could result in serious injury or death. Service adjustments should be performed only by qualified service personnel.

Warning 

Read the Safety Summary at the front of this manual before performing adjustment procedures. The apparatus shall be disconnected from all voltage sources before it is opened for any adjustment, replacement, maintenance, or repair.

CRT Color Module Adjustments

The CRT Color Module is adjusted to compensate for external magnetic influences causing misconvergence.

Note

DO NOT PERFORM THESE ADJUSTMENTS DURING ROUTINE CALIBRATION. The earth's magnetic field or the user's environment may cause an unstable display which cannot be corrected by degaussing the screen. The following procedures are provided for those few extreme cases.

Note

DO NOT continue with this procedure before first degaussing the CRT screen with the rear panel degaussing switch. In extreme cases of magnetism, it may be necessary to degauss the CRT with a conventional external television-type degaussing coil. During any of the following adjustments, the CRT module must face west.

Equipment

This is a list of the recommended test equipment for this adjustment. However, any instrument which satisfies the critical specifications may be used.

Accessory	Critical Specifications	HP Part Number
N/A	Alignment tool non-metallic	8710-1355

Note

The following adjustments are broken down into groups. Follow their sequence because they interact and depend on each other. Figure 4-1 is a drawing of the adjustment sequence. In some cases not all the adjustment groups are used. For example, if the Geometry Adjustment Group corrects the problem, this will be the only group used.

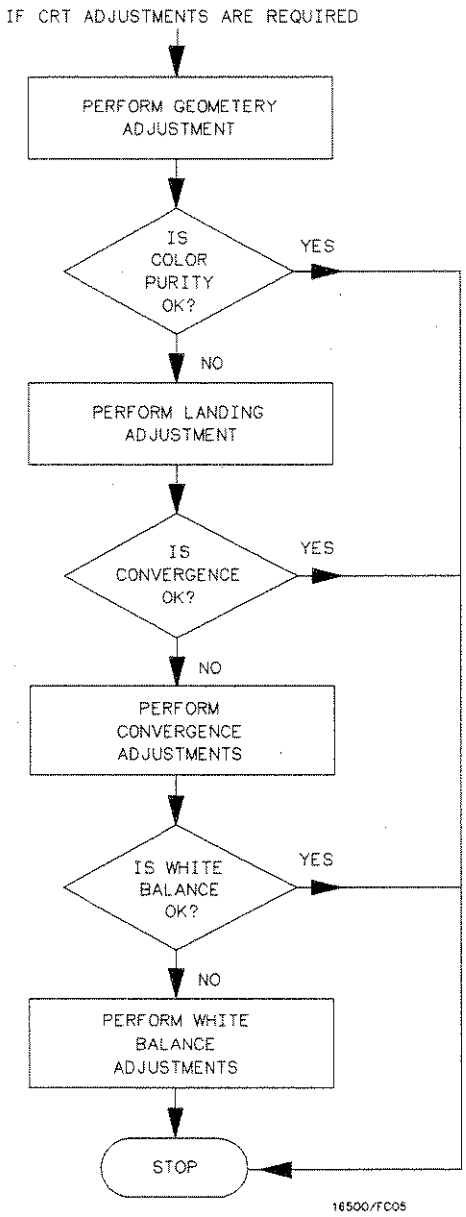


Figure 4-1. CRT Adjustment Sequence

Geometry Adjustments

1. Press **Utility** menu key and **CRT SETUP** key.
   Press **CRT PATTERN** key until a white cross hatch is displayed on CRT.

2. Preset front-panel BACKGROUND control to mechanical center.

3. Preset front-panel CONTRAST control maximum clockwise.

4. Preset H.SUB SHIFT (RV006) and V.SUB SHIFT (RV008) on bottom PC board to mechanical center.

5. With a flexible ruler, adjust H.SIZE (RV504) and V.HEIGHT (RV502) on left hand side PC board so cross-hatch pattern's border displayed on CRT is 120.5 mm (4.74 in.) vertically and 161 mm (6.34 in.) horizontally.

6. Adjust V.CENT (RV510) and H.CENT (RV503) on left hand side PC board to center pattern.

7. Adjust PIN AMP (RV506) on left hand side PC board to eliminate pincushion distortion in the vertical lines of the cross-hatch pattern. Refer to figure 4-2.

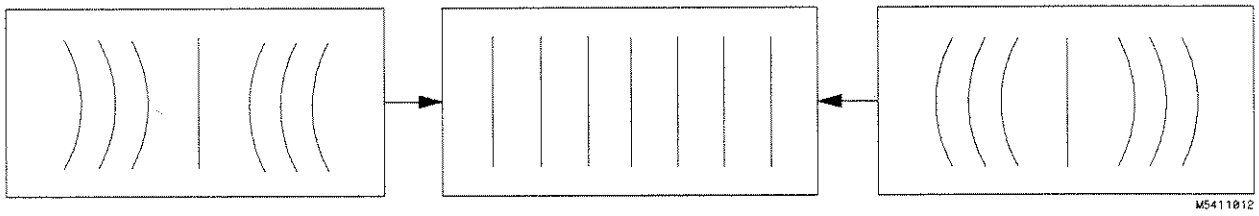


Figure 4-2. PIN AMP Adjustment

8. Adjust PIN PHASE (RV505) on left side PC board to eliminate pin phase distortion in vertical lines of cross-hatch pattern. Refer to figure 4-3.

9. Adjust TOP PIN (RV511) on left hand side PC board until the horizontal line is parallel with center horizontal line.

10. Adjust BOTTOM PIN (RV512) on left hand side PC board until the bottom horizontal line is parallel with center horizontal line.

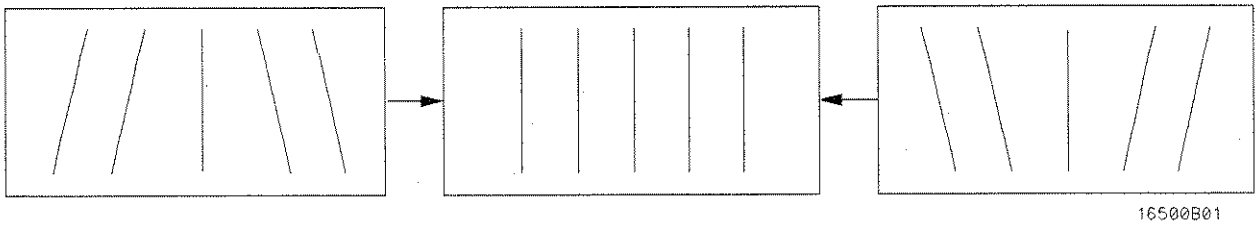


Figure 4-3. PIN PHASE Adjustment

Landing, Convergence, and Focus Adjustment Preparation:

1. Remove CRT Display Module from instrument. See disassembly section 6A-9.

2. Reconnect instrument front panel, install front panel and CRT bezel (using two screws to temporarily hold front panel in place).

Steps 3-5 are performed only when the CRT has been replaced.

3. Loosen deflection yoke clamp screw.

4. With CRT Display Module placed to mainframe's left, reconnect module.

Note

Note the original routing of the module power cable for proper routing when module is installed in instrument. Then, route the module power cable from inside the module to the outside (left side) of module for reconnection to the power supplies.

5. Remove deflection yoke spacers by moving deflection yoke rearward and removing spacers.

Note

The deflection yoke spacers are tapered rubber blocks between front of yoke and rear of CRT funnel.

6. Apply power and allow instrument to thermally stabilize for 20 minutes.

Focus Adjustment

Note

Perform the geometry adjustments before making focus adjustment.

1. Press **Utility** menu key and **CRT SETUP** key.
   Press **CRT PATTERN** key until a white cross-hatch is displayed on CRT.

2. Adjust FOCUS (RV701) on rear PC board for best overall focus.

Landing Adjustment

1. Press **Utility** menu key and **CRT SETUP** key.
   Press **COLOR PURITY** key until a white raster is displayed on CRT.

2. Turn front panel CONTRAST control fully clockwise.

3. Degauss entire CRT screen by pressing DEGAUSSING switch on instrument's rear panel.

Note

In cases where the user's environment or shipping environment has caused high levels of magnetization to take place, it may be necessary to externally degauss the CRT with a conventional television-type degaussing coil to completely degauss the CRT.

4. Set purity magnet tabs to mechanical center. Refer to figure 4-4.

5. Press **COLOR PURITY** key until a green raster is displayed on CRT.

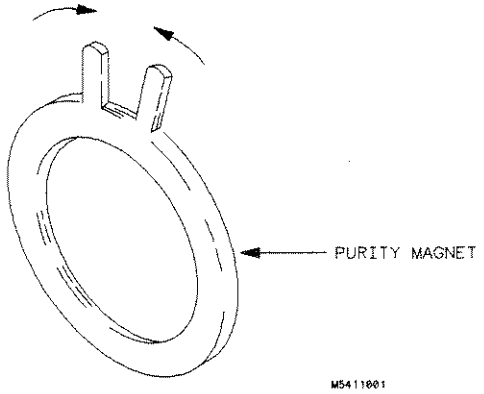


Figure 4-4. Purity Magnet Centering

Step 6 is performed only if the CRT has been replaced.

6. Move deflection yoke rearward until left edge of raster turns red and right side of raster turns blue. Refer to figure 4-5.

7. Adjust purity magnets until green is in center of raster with red and blue bands evenly distributed on sides. Refer to figure 4-5.

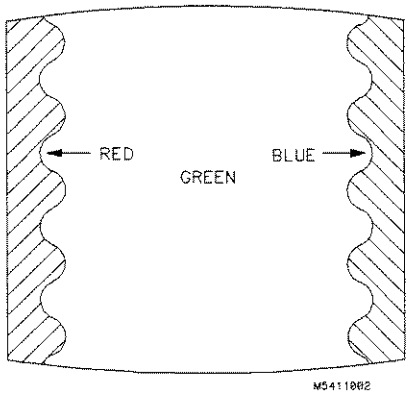


Figure 4-5. Purity Magnet Adjustment Raster

Step 8 is performed only if CRT has been replaced.

8. Move deflection yoke forward until entire raster is green.

Note

Landing adjustment is easier if yoke is moved all the way forward, then moved rearward until raster is completely green.

9. With COLOR PURITY key, replace green raster with red, then with blue raster. Check each raster for proper landing adjustment or color purity.

10. If landing is not correct in step 9, repeat steps 6 through 9 for best compromise. Refer to figure 4-6.

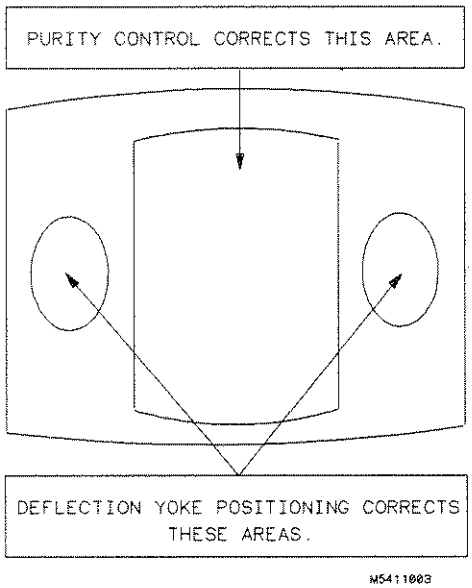


Figure 4-6. Landing and Purity Adjustment Guide

11. If landing is not correct in step 10, readjust purity magnets for best landing of each color.

Step 12 is performed only if the CRT has been replaced.

12. When landing adjustment is complete, tighten deflection yoke clamp screw just enough to keep yoke from moving. **DO NOT** over tighten.

Note

While moving deflection yoke forward and rearward, rotate yoke as necessary to make vertical edges of raster parallel to the sides of the instrument frame.

Static Convergence

1. Preset front-panel BACKGROUND control to mechanical center.

2. Preset front-panel CONTRAST control maximum clockwise.

3. Temporarily disconnect power from instrument and remove PC board shield cover from rear of CRT Display Module by prying evenly on all four sides.

4. Apply power and press Utility menu key and CRT SETUP key.
   Press **CRT PATTERN** key until a white cross-hatch pattern is displayed.

5. Check four dots which are around center intersection of cross-hatch pattern for coincidence of blue, red, and green dots. If the dots are not coincident, adjust H.STAT (RV703) on rear PC board to obtain horizontal coincidence and V.STAT (RV803) on bottom PC board to obtain vertical coincidence. Refer to figure 4-7.

Note

Due to interaction, BEAM LANDING will need to be re-adjusted if either H.STAT or V.STAT adjustments are made. Once BEAM LANDING is readjusted, repeat step 5 above if necessary to obtain center screen coincidence of the dots.

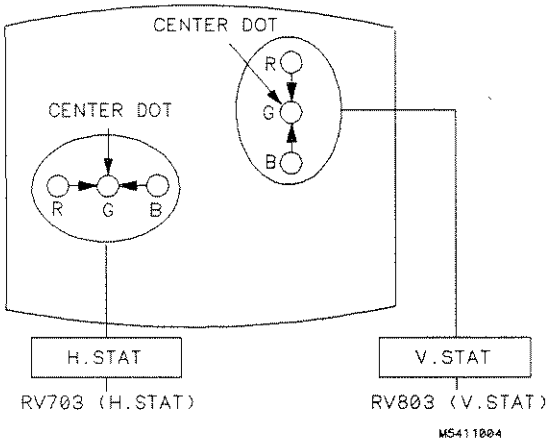


Figure 4-7. Static Convergence

Dynamic Convergence

1. Press **Utility** menu key and CRT **SETUP key.**
   Press **CRT PATTERN** key until a white cross-hatch pattern is on CRT.

2. Adjust Y BOW (RV805) on bottom PC board to eliminate red, green, and blue bowing at top and bottom of center vertical line. Refer to figure 4-8.

3. Adjust Y BOW CROSS (RV804) on bottom PC board to eliminate red, green, and blue orthogonal misalignment at top and bottom of center vertical line. Refer to figure 4-9.

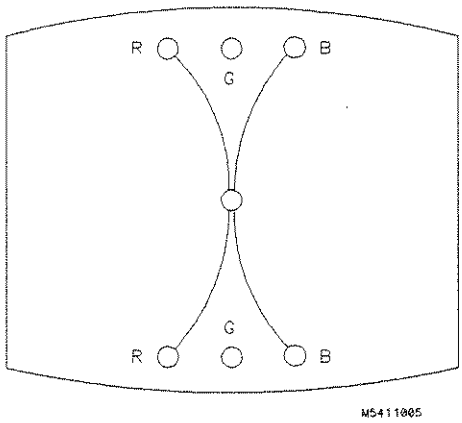


Figure 4-8. Y BOW Adjustment

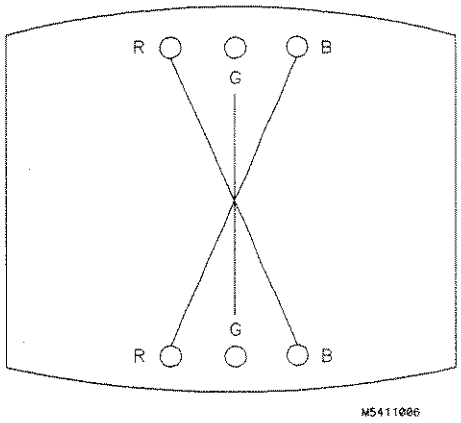


Figure 4-9. Y BOW CROSS Adjustment

4. Adjust V.STAT TOP (RV801) and V.STAT BOTTOM (RV802) on bottom PC board to obtain coincidence of red, blue, and green at intersection of top and bottom horizontal lines with center vertical line. Refer to figures 4-10 and 4-11.

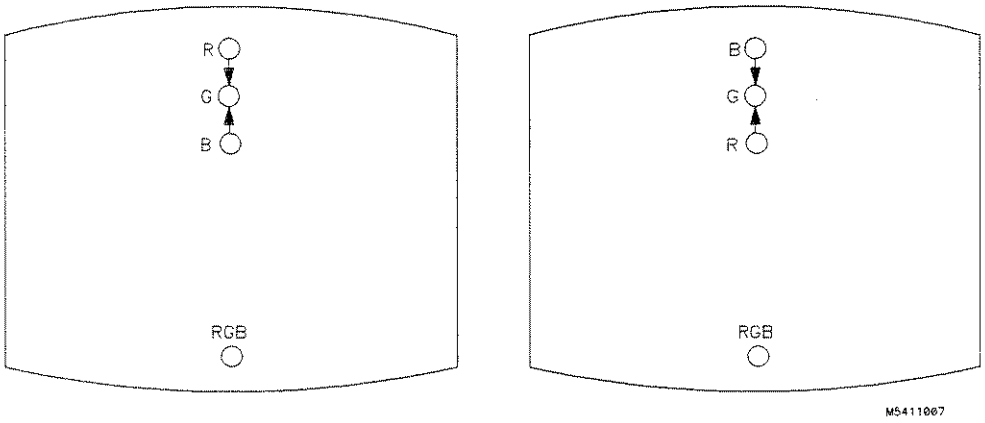


Figure 4-10. V.STAT TOP Adjustment

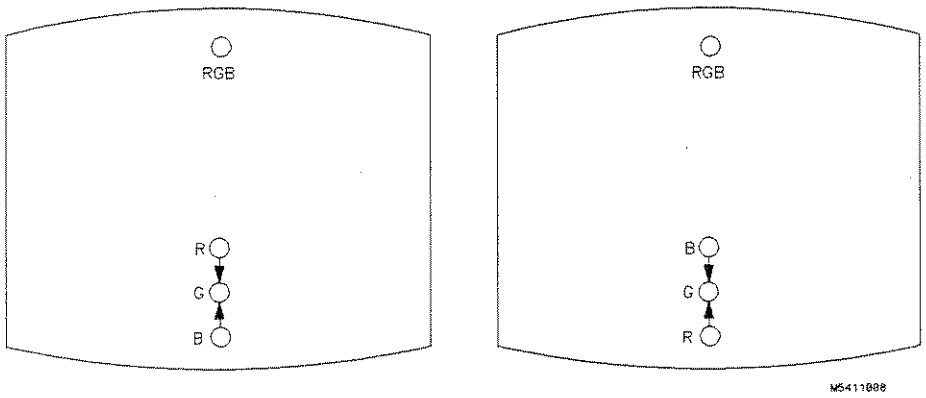


Figure 4-11. V.STAT BOTTOM Adjustment

5. Adjust H.AMP (RV807) on bottom PC board for equal amounts of misconvergence at right and left sides of screen. Refer to figure 4-12.

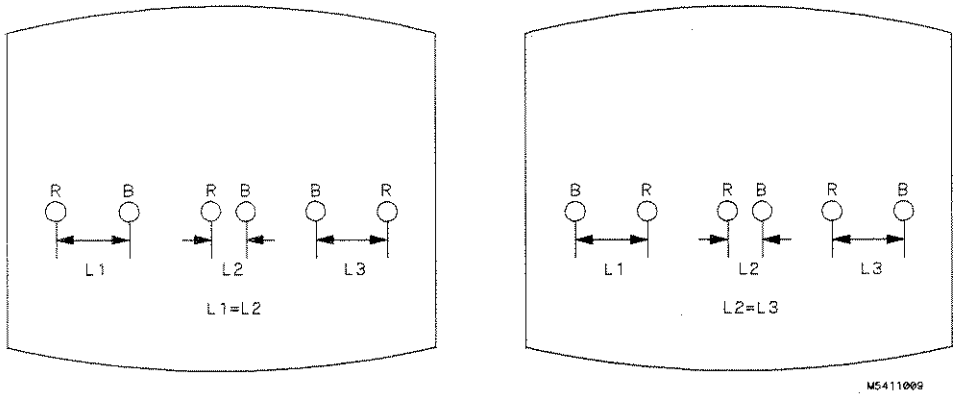


Figure 4-12. H.AMP Adjustment

6. Adjust H.TILT (RV806) on bottom PC board for coincidence of red, green, and blue at right and left sides of screen. Refer to figure 4-13.

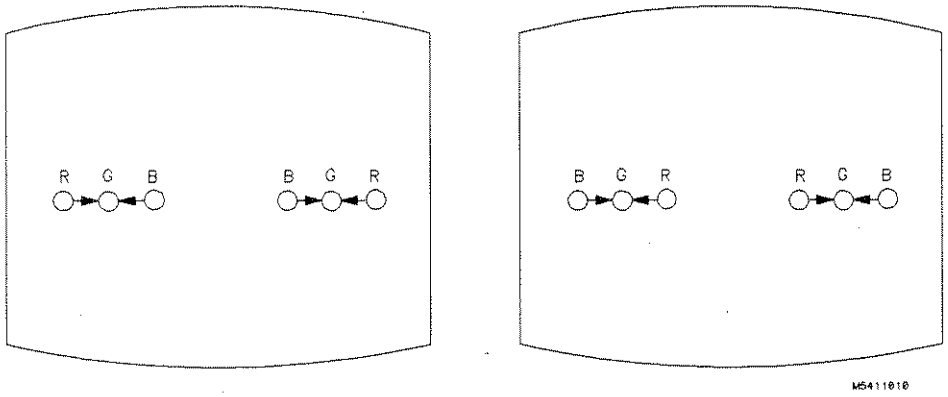


Figure 4-13. H.TILT Adjustment

White Balance

1. Press **Utility** menu key.
   Press **LIGHT OUTPUT** key until a blank raster is on CRT.

Note

The completely blank raster will contain a test for the function keys on the right side of the display. However, it will not affect this adjustment.

2. Set front-panel BACKGROUND and SUB BRT (RV901) on bottom PC board to mechanical center.

3. Set front-panel BRIGHTNESS and SUB CONT (RV902) on bottom PC board to mechanical center.

4. Set G. DRIVE (RV921), B. DRIVE (RV9310), and R. DRIVE (RV911) on bottom PC board to mechanical center.

5. Set G.BKG (RV721), B.BKG (RV731), and R.BKG (RV711) on rear PC board fully counterclockwise (CCW).

6. Adjust SCREEN (RV702) on rear PC board until either a red, green, or blue raster just starts to become visible. Note which color becomes visible first and do not adjust background control (BKG) for that color in the step 7.

7. Adjust other two background (BKG) controls for best white balance.

8. Press **Utility** menu key.
   Press **COLOR PURITY** key until a white raster is on CRT.

9. Set front panel BRIGHTNESS control at maximum.

10. Observe screen and adjust DRIVE controls (RV921, RV931, and RV911) on bottom PC board for best white balance.

Note

White balance is checked in two ways. First, with an average piece of white photocopy paper, compare the white on the CRT to the paper. Second, in the CONFIDENCE TEST function, the gray scale blocks are checked to make sure the block at the far left of the CRT is visible.

11. Repeat steps 1 through 3 and 6 through 10 for best overall white balance.

Table Of Contents

Replaceable Parts

Replaceable Parts 5

Introduction

This section contains information for ordering parts. Table 5-1 lists the names and addresses that correspond to the manufacturers' code numbers. Table 5-2 lists the abbreviations used in the parts list and throughout this manual. Figures 5-1 through 5-6 are drawings with reference designators included. Table 5-3 is the replaceable parts list.

Abbreviations

Table 5-2 lists the abbreviations used in the replaceable parts list. Abbreviations in the replaceable parts list are always in capital letters. In other sections of this manual abbreviations may be in capital or lower case letters.

Replaceable Parts List

Table 5-3 is a list of replaceable parts and is organized as follows:

a. Electrical assemblies in alphanumerical order by reference designation.

b. Chassis mounted parts in alphanumerical order by reference designation.

Information given for each part consists of the following:

a. Hewlett-Packard part number and the check digit (for HP internal use).

b. Total quantity (Qty) in the instrument, given only once at the part number's first appearance in the list.

c. Description of part.

d. A typical manufacturer of a given part in a five digit code. Refer to table 5-1 for a cross reference from code number to manufacturer name.

e. The manufacturers' part number.

Exchange Assemblies

Some of the assemblies used in this instrument have been set up on the exchange program. This allows the customer to exchange his faulty assembly with one that has been repaired, adjusted, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Exchange assemblies are listed at the beginning of the replaceable parts table with a star (*) before the reference designator. They have a part number in the form XXXXX-695XX.

Before ordering an exchange assembly, check with your local parts or repair organization for the procedures associated with the exchange assembly program.

Ordering Information

To order a part listed in the replaceable parts table, indicate the Hewlett-Packard part number, check digit, and quantity required. Send the order to the nearest Hewlett-Packard office.

To order a part that is not listed in the replaceable parts table, include the instrument model number, serial number, description and function of part, and total quantity required. Address an order to the nearest Hewlett-Packard sales office.

Direct Mail Order System

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are as follows:

a. Direct ordering and shipment from HP Parts Center in Mountain View, California. Call your local Hewlett-Packard office for the toll free number

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through local HP offices when orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices. To provide these advantages, check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Hewlett-Packard offices.

Table 5-1. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address	Zip Code
04713	Motorola Semi Conductor Products	Phoenix Az	85008
06915	Pan Asian Paper Product Mfg SDN BHD	Pinang	Malaysia
28480	Hewlett-Packard Co. Corporate HQ	Palo Alto Ca	94304
86928	Seastrom Mfg Co.	Glendale Ca	91201

Table 5-2. Reference Designator and Abbreviations

REFERENCE DESIGNATOR

A	= assembly	F	= fuse	Q	= transistor;SCR; triode thyristor	U	= integrated circuit; microcircuit
B	= fan;motor	FL	= filter	R	= resistor	V	= electron tube; glow lamp
BT	= battery	H	= hardware	RT	= thermistor	VR	= voltage regulator; breakdown diode
C	= capacitor	J	= electrical connector (stationary portion);jack	S	= switch;jumper	W	= cable
CR	= diode;diode thyristor; varactor	L	= coil;inductor	T	= transformer	X	= socket
DL	= delay line	MP	= misc. mechanical part	TB	= terminal board	Y	= crystal unit(piezo-electric or quartz)
DS	= annunciator;lamp;LED	P	= electrical connector (moveable portion);plug	TP	= test point		
E	= misc. electrical part						

ABBREVIATIONS

A	= amperes	DWL	= dowel	MFR	= manufacturer	RND	= Round
A/D	= analog-to-digital	ECL	= emitter coupled logic	MICPROC	= microprocessor	ROM	= read-only memory
AC	= alternating current	ELAS	= elastomeric	MINTR	= miniature	RPG	= rotary pulse generator
ADJ	= adjust(ment)	EXT	= external	MISC	= miscellaneous	RX	= receiver
AL	= aluminum	F	= farads;metal film (resistor)	MLD	= molded	S	= Schottky-clamped; seconds(time)
AMPL	= amplifier			MM	= millimeter		
ANLG	= analog	FC	= carbon film/ composition	MO	= metal oxide	SCR	= screw;silicon controlled rectifier
ANSI	= American National Standards Institute	FD	= feed	MTG	= mounting	SEC	= second(time);secon dary
		FEM	= female	MTLC	= metallic		
ASSY	= assembly	FF	= flip-flop	MUX	= multiplexer	SEG	= segment
ASTIG	= astigmatism	FL	= flat	MW	= milliwatt	SEL	= selector
ASYNCHRO	= asynchronous	FM	= foam;from	N	= nano(10^{-9})	SGL	= single
ATTEN	= attenuator	FR	= front	NC	= no connection	SHF	= shift
AWG	= American wire gauge	FT	= gain bandwidth product	NMOS	= n-channel metal-oxide-semiconductor	SI	= silicon
BAL	= balance					SIP	= single in-line package
BCD	= binary-code decimal	FW	= full wave	NPN	= negative-positive-negative		
BD	= board	FXD	= fixed	NPRN	= neoprene	SKT	= skirt
BFR	= buffer	GEN	= generator	NRFR	= not recommended for field replacement	SL	= slide
BIN	= binary	GND	= ground(ed)			SLDR	= solder
BRDG	= bridge	GP	= general purpose	NSR	= not separately replaceable	SLT	= slot(ted)
BSHG	= bushing	GRAT	= graticule			SOLD	= solenoid
BW	= bandwidth	GRV	= groove	NUM	= numeric	SPCL	= special
C	= ceramic;cermet (resistor)	H	= henries;high	OBD	= order by description	SQ	= square
		HD	= hardware	OCTL	= octal	SREG	= shift register
CAL	= calibrate;calibration	HDND	= hardened	OD	= outside diameter	SRQ	= service request
CC	= carbon composition	HG	= mercury	OP AMP	= operational amplifier	STAT	= static
CCW	= counterclockwise	HGT	= height	OSC	= oscillator	STD	= standard
CER	= ceramic	HLCL	= helical	P	= plastic	SYNCHRO	= synchronous
CFM	= cubic feet/minute	HORIZ	= horizontal	P/O	= part of	TA	= tantalum
CH	= choke	HP	= Hewlett-Packard	PC	= printed circuit	TBAX	= tubeaxial
CHAM	= chamfered	HP-IB	= Hewlett-Packard Interface Bus	PCB	= printed circuit board	TC	= temperature coefficient
CHAN	= channel			PD	= power dissipation	TD	= time delay
CHAR	= character	HR	= hour(s)	PF	= picofarads (10^{-12})	THD	= thread(ed)
CM	= centimeter	HV	= high voltage	PI	= plug in	THK	= thick
CMOS	= complementary metal-oxide-semiconductor	HZ	= Hertz	PL	= plate(d)	THRU	= through
		I/O	= input/output	PLA	= programmable logic array	TP	= test point
CMR	= common mode rejection	IC	= integrated circuit			TPG	= tapping
		ID	= inside diameter	PLST	= plastic	TPL	= triple
CNDCT	= conductor	IN	= inch	PNP	= positive-negative-positive	TRANS	= transformer
CNTR	= counter	INCL	= include(s)			TRIG	= trigger(ed)
CON	= connector	INCAND	= incandescent	POLYE	= polyester	TRMR	= trimmmer
CONT	= contact	INP	= input	POS	= positive;position	TRN	= turn(s)
CRT	= cathode-ray tube	INTEN	= intensity	POT	= potentiometer	TTL	= transistor-transistor
CW	= clockwise	INTL	= internal	POZI	= pozidrive	TX	= transmitter
D	= diameter	INV	= inverter	PP	= peak-to-peak	U	= micro(10^{-6})
D/A	= digital-to-analog	JFET	= junction field-effect transistor	PPM	= parts per million	UL	= Underwriters Laboratory
DAC	= digital-to-analog converter			PRCN	= precision		
		JKT	= jacket	PREAMP	= preamplifier	UNREG	= unregulated
DARL	= darlington	K	= kilo(10^{3})	PRGMBL	= programmable	VA	= voltampere
DAT	= data	L	= low	PRL	= parallel	VAC	= volt,ac
DBL	= double	LB	= pound	PROG	= programmable	VAR	= variable
DBM	= decibel referenced to 1mW	LCH	= latch	PSTN	= position	VCO	= voltage-controlled oscillator
		LCL	= local	PT	= point		
DC	= direct current	LED	= light-emitting diode	PW	= potted wirewound	VDC	= volt,dc
DCDR	= decoder			PWR	= power	VERT	= vertical
DEG	= degree	LG	= long	R-S	= reset-set	VF	= voltage,filtered
DEMUX	= demultiplexer	LI	= lithium	RAM	= random-access memory	VS	= versus
DET	= detector	LK	= lock			W	= watts
DIA	= diameter	LKWR	= lockwasher	RECT	= rectifier	W/	= with
DIP	= dual in-line package	LS	= low power Schottky	RET	= retainer	W/O	= without
DIV	= division	LV	= low voltage	RF	= radio frequency	WW	= wirewound
DMA	= direct memory access	M	= mega(10^{6});megohms; meter(distance)	RGLTR	= regulator	XSTR	= transistor
DPDT	= double-pole, double-throw			RGTR	= register	ZNR	= zener
		MACH	= machine	RK	= rack	°C	= degree Celsius (Centigrade)
DRC	= DAC refresh controller	MAX	= maximum	RMS	= root-mean-square	°F	= degree Fahrenheit
DRVR	= driver					°K	= degree Kelvin

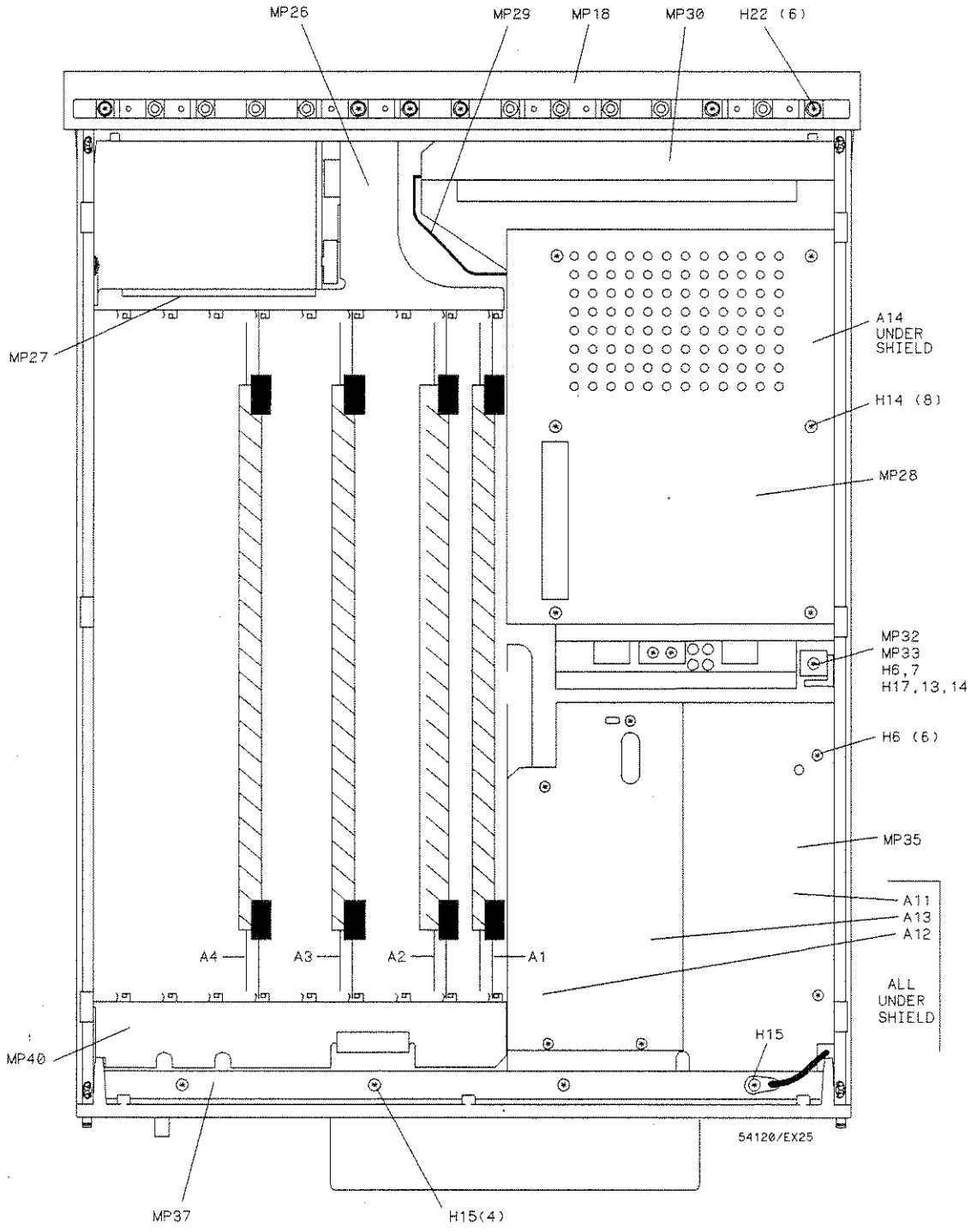


Figure 5-1. Top View

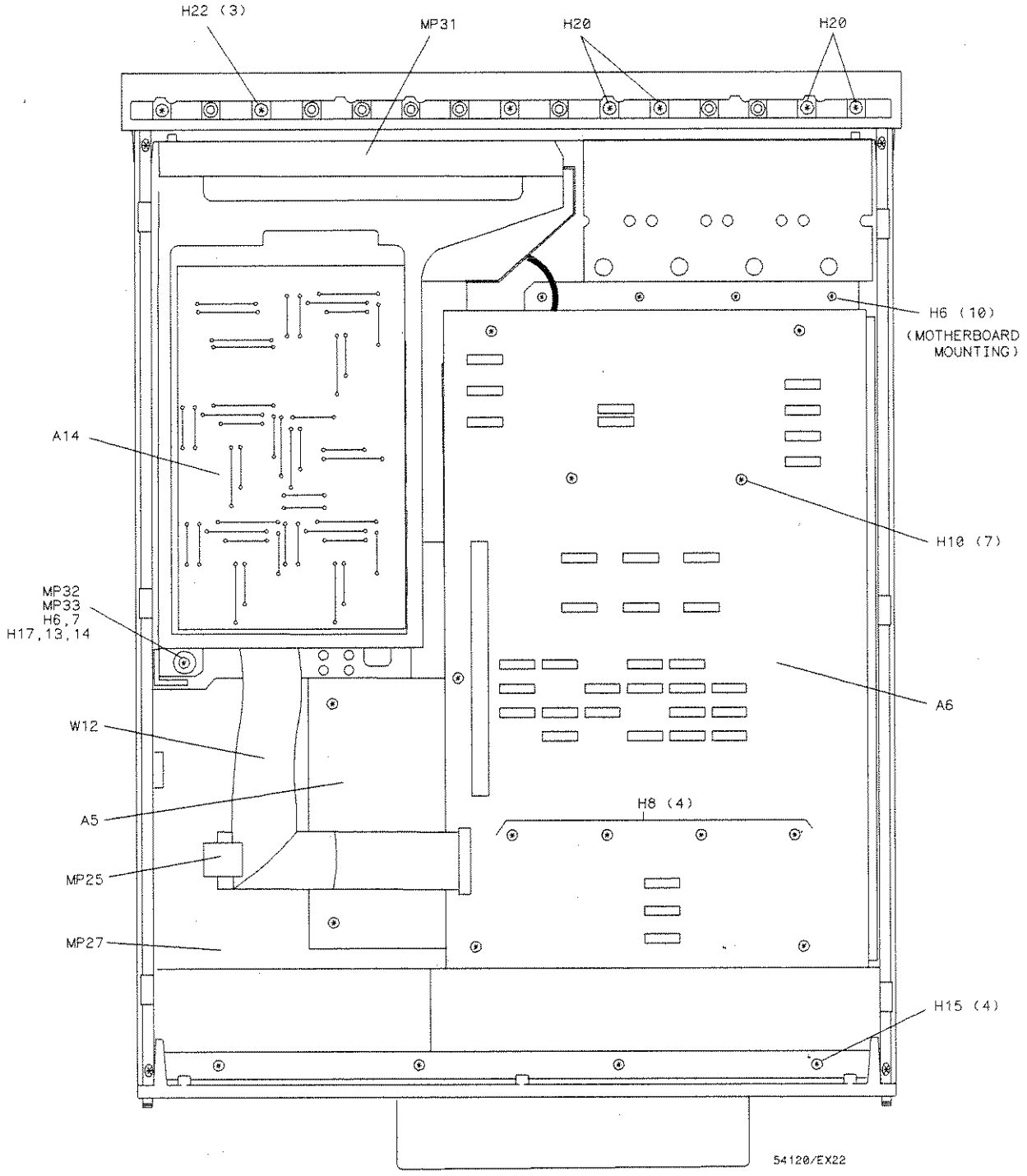


Figure 5-2. Bottom View

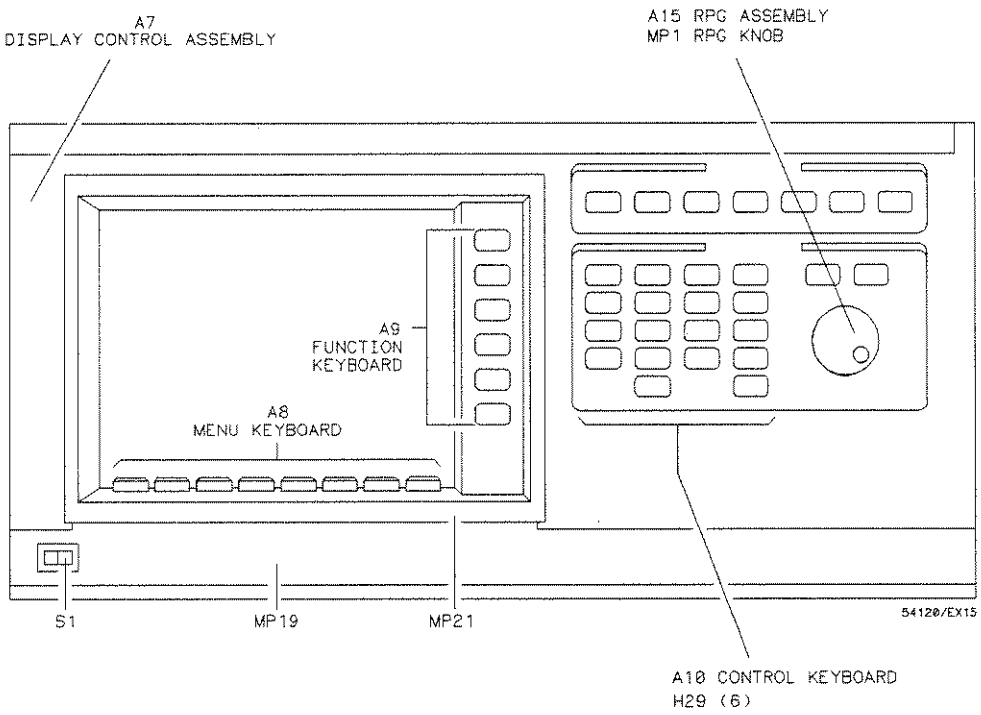


Figure 5-3. Front Panel

H5 Cover screw
H8 Retainer ring for cover screw
H9 Foot screw

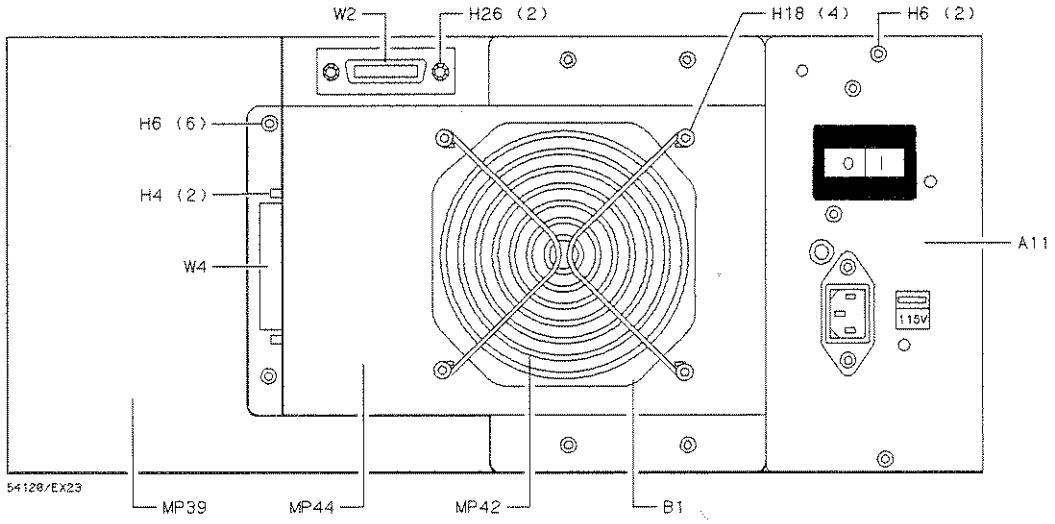


Figure 5-4. Rear Panel

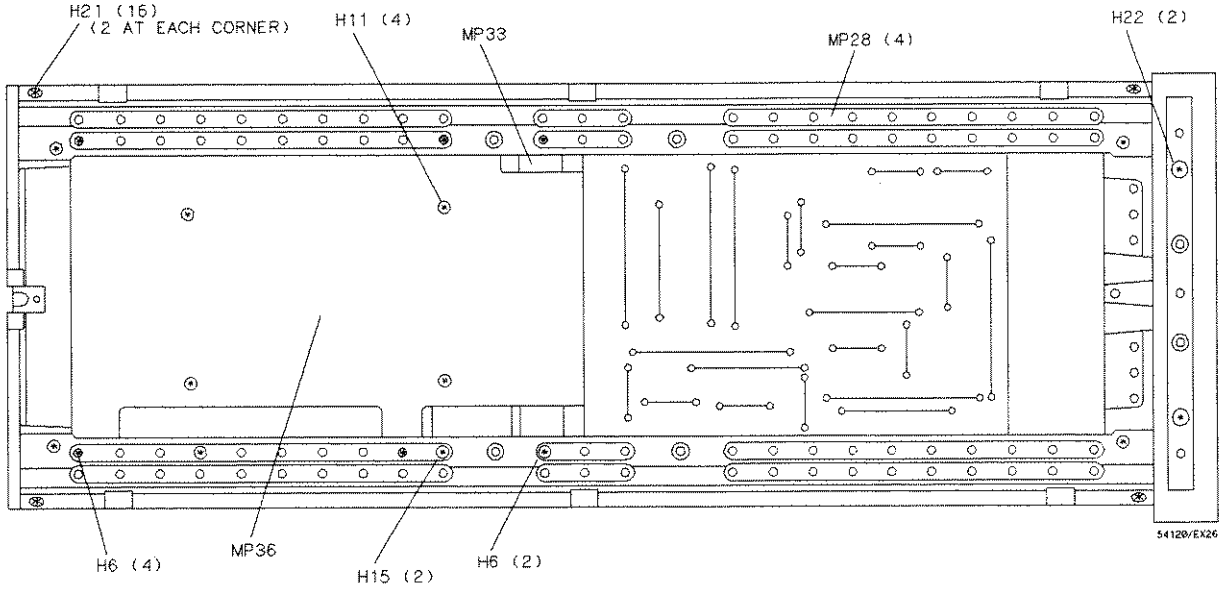


Figure 5-5. Left Side View

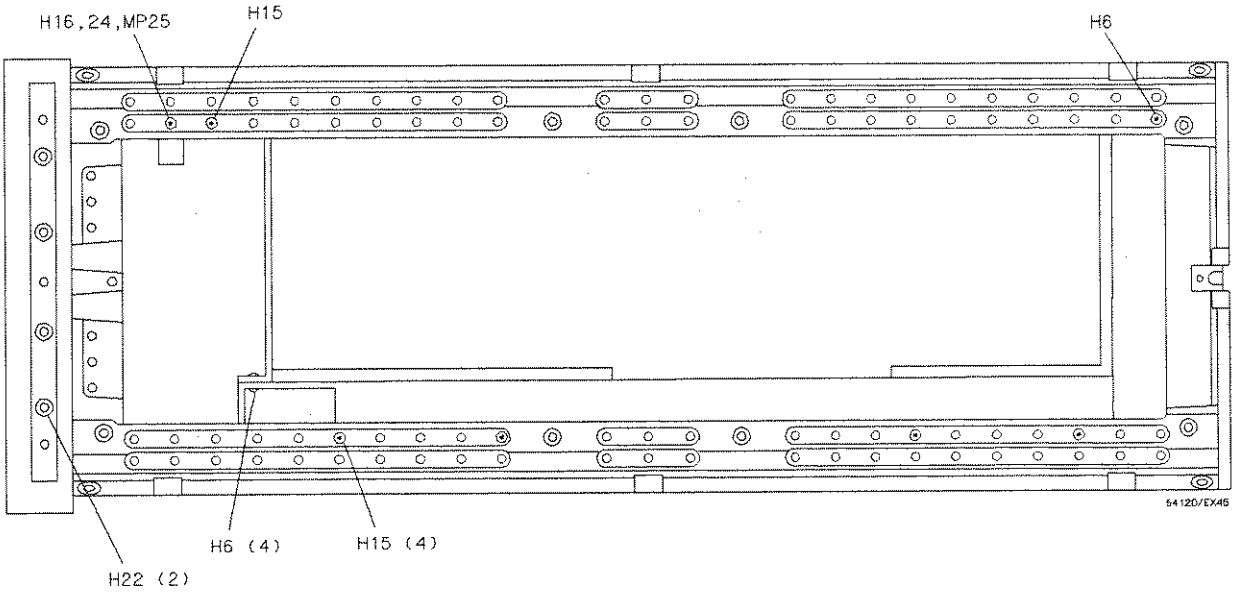


Figure 5-6. Right Side View

Table 5-3. Replaceable Parts List

Reference Designator	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
*EXCHANGE ASSEMBLIES						
*A1	54111-69506	8	0	I/O ASSEMBLY	28480	54111-69506
*A2	54111-69525	1	0	MICROPROCESSOR ASSEMBLY	28480	54111-69525
*A3	54122-69501	6	0	HORIZONTAL CONTROL ASSEMBLY	28480	54122-69501
*A4	54120-69502	5	0	ADC ASSEMBLY	28480	54120-69502
*A6	54110-69514	7	0	COLOR DISPLAY ASSEMBLY	28480	54110-69514
*A11	54110-69513	6	0	PRIMARY POWER SUPPLY ASSEMBLY	28480	54110-69513
*A12	54110-69510	3	0	ANALOG POWER SUPPLY ASSEMBLY	28480	54110-69510
*A13	54110-69506	7	0	DIGITAL POWER SUPPLY ASSEMBLY	28480	54110-69506
A1	54111-66506	2	1	I/O ASSEMBLY	28480	54111-66506
A2	54111-66525	5	1	MICROPROCESSOR ASSEMBLY	28480	54111-66525
A3	54122-66501	0	1	HORIZONTAL CONTROL ASSEMBLY	28480	54122-66501
A4	54120-66502	9	1	ADC ASSEMBLY	28480	54120-66502
A5	54110-66511	8	1	MOTHER BOARD ASSEMBLY	28480	54110-66511
A6	54110-66514	1	1	COLOR DISPLAY ASSEMBLY	28480	54110-66514
A7	54110-66509	4	1	CRT CONTROL ASSEMBLY	28480	54110-66509
A8	54100-66520	7	1	MENU KEYBOARD	28480	54100-66520
A9	54110-66502	7	1	FUNCTION KEYBOARD	28480	54110-66502
A10	54100-66505	8	1	CONTROL KEYBOARD	28480	54100-66505
A11	54110-66513	0	1	PRIMARY POWER SUPPLY ASSEMBLY	28480	54110-66513
A12	54110-66510	7	1	ANALOG POWER SUPPLY ASSEMBLY	28480	54110-66510
A13	54110-66506	1	1	DIGITAL POWER SUPPLY ASSEMBLY	28480	54110-66506
A14	2090-0226	5	1	COLOR CRT MODULE	28480	2090-0226
A15	01980-61062	5	1	RPG ASSEMBLY	28480	01980-61062
B1	3160-0521	3	1	FAN-TUBEAXIAL	28480	3160-0521
E1	8160-0577	4	1	RFI GROUND STRIP	28480	8160-0577
H1	0515-1384	8	2	SCREW-MACH M5 X 0.8 10MM-LG	28480	0515-1384
H2	0515-1444	1	4	SCREW-MACH M3.5 X 0.6 25.4MM-LG PAN-HD	28480	0515-1444
H3	0515-1319	9	8	SCREW-MACH M3 X 0.5 20MM-LG PAN-HD	28480	0515-1319
H4	1251-2942	7	2	SCREW LOCK KIT-SUBMIN D CONN	28480	1251-2942
H5	1251-1245	7	3	COVER SCREW	28480	1251-2945
H6	0515-0372	2	49	SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-LG	28480	0515-0372
H7	NOT ASSIGNED					
H8	0515-1253	0	3	RETAINER RING FOR COVER SCREW2	8480	0515-1253
H9	0515-1444	1	4	FOOT SCREW	28480	0515-1444
H10	0515-1410	1	7	SCREW-MACHINE ASSEMBLY M3 X 0.5 20MM-LG	28480	0515-1410
H11	0515-1025	4	4	SCREW-MACHINE ASSEMBLY M3 X 0.5 26MM-LG	28480	0515-1025
H12	5061-6138	2	4	NUT-INSERT M4 X 0.7 X 4.6 OD	28480	5061-6138
H13	2190-0763	7	2	WASHER-FL MTLC NO. 6 .14-IN-ID .5-IN-OD	28480	2190-0763
H14	3050-1238	8	2	WASHER-FL NM 9/64 .149-IN-ID .478-IN-OD	86928	3050-1238
H15	0515-0433	6	15	SCREW-MACHINE ASSEMBLY M4 X 0.7 8MM-LG	28480	0515-0433

Table 5-3. Replaceable Parts List

Reference Designator	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
H16	NOT ASSIGNED					
H17	0515-0641	8	2	SCREW-THD-RLG M4 X 0.7 10MM-LG PAN-HD	28480	0515-0641
H18	0515-0435	8	4	SCREW-MACHINE ASSEMBLY M4 X 0.7 14MM-LG	28480	0515-0435
H19	NOT ASSIGNED					
H20	0515-1228	9	4	SCREW-MACH M4 X 0.7 6MM-LG 90-DEG-FLH-HD	28480	0515-1228
H21	0515-1403	2	16	SCREW-SPCL M4 X 0.7 6MM-LG 90-DEG-FLH-HD	28480	0515-1403
H22	0515-1269	8	16	SCREW-MACH M4 X 0.7 10MM-LG	28480	0515-1269
H23	0535-0031	2	9	NUT-HEX W/LKWR M3 X 0.5 2.4MM-THK	28480	0535-0031
H24	NOT ASSIGNED					
H25	2950-0043	8	1	NUT-HEX-DBL-CHAM 3/82THD .094-IN-THK	28480	2950-0043
H26	0380-1686	6	2	STANDOFF-HEX 6.5-MM-LG M3 X 0.5-THD	28480	0380-1686
H27	2190-0016	3	1	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
H28	3050-1176	3	1	WASHER-FL NM 3/8 IN .39-IN-ID .562-IN-OD	86928	3050-1176
H29	0515-0664	5	5	SCREW M3 12MN-L6 PAN-HP T10	28480	0515-0664
MP1	01650-47401	7	1	RPG KNOB	28480	01650-47401
MP2	5061-9448	3	1	BOTTOM COVER	28480	5061-9448
MP3	5040-7201	8	2	BOTTOM FEET	28480	5040-7201
MP4	5040-7222	3	2	BOTTOM NON SKID FEET	28480	5040-7222
MP5	1460-1345	5	2	TILT STAND SST	28480	1460-1345
MP6	8160-0590	1	2	GROUND RFI STRIP	28480	8160-0590
MP7	54110-04103	4	1	TOP COVER	28480	54110-04103
MP8	0890-0029	0	1	TUBING-HS .187-IN-D/.093-IN-RCVD	28480	0890-0029
MP9	5001-0441	2	2	TRIM STRIP SIDE	28480	5001-0441
MP10	5040-7202	9	1	TOP TRIM STRIP	28480	5040-7202
MP11	54110-40502	3	4	REAR FOOT	28480	54110-40502
MP12	5060-9948	6	2	SIDE COVERS – PERFORATED	28480	5060-9948
MP13	NOT ASSIGNED					
MP14	5060-9805	4	2	STRAP HANDLE	28480	5060-9805
MP15	5041-6819	4	2	FRONT CAP FOR STRAP HANDLE	28480	5041-6819
MP16	5041-6820	7	2	REAR CAP FOR STRAP HANDLE	28480	5041-6820
MP17	NOT ASSIGNED					
MP18	5021-5807	6	1	FRONT FRAME	28480	5021-5807
MP19	54120-00206	2	1	FRONT PANEL	28480	54120-00206
MP20	54111-00203	8	1	FRONT SUB PANEL	28480	54111-00203
MP21	54110-40501	2	1	DISPLAY BEZEL	28480	54110-40501
MP22	16500-00603	3	1	FAN SCREEN	28480	16500-00603
MP23	0403-0092	6	1	BUMPER FOOT-PRS-IN	28480	0403-0092
MP24	1400-1362	0	2	CLAMP-CABLE .35-DIA .51-WD NYL	28480	1400-1362
MP25	1400-0611	0	2	CLAMP-FL-CA 1-WD	06915	1400-0611
MP26	54111-01203	0	1	FRONT CARD CAGE BRACKET	28480	54111-01203
MP27	54111-00101	5	1	MAIN DECK	28480	54111-00101
MP28	5021-5838	3	4	SIDE STRUT	28480	5021-5838
MP29	NOT ASSIGNED					
MP30	54110-01201	7	1	TOP CRT BRACKET	28480	54110-01201

Table 5-3. Replaceable Parts List

Reference Designator	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP31	54110-01202	8	1	BOTTOM CRT BRACKET	28480	54110-01202
MP32	54110-01210	8	1	BRACKET-COLOR CRT MOD. REAR-ON MODULE	28480	54110-01210
MP33	54110-04702	9	1	BRACKET-COLOR CRT MOD. REAR-ON FRAME	28480	54110-04702
MP34	1400-0679	0	4	CLIP-CABLE 'U' SHP, PNL MTG TYPE	28480	1400-0679
MP35	54111-04104	6	1	POWER SUPPLY COVER-TOP	28480	54111-04104
MP36	54110-04106	7	1	POWER SUPPLY COVER-SIDE	28480	54110-04106
MP37	5021-5808	7	1	REAR FRAME	28480	5021-5808
MP38	54110-94302	4	1	WARNING LABEL	28480	54110-94302
MP39	54120-00201	7	1	REAR PANEL	28480	54120-00201
MP40	54111-05201	6	1	AIR PLENUM	28480	54111-05201
MP41	7120-4835	0	1	LABEL-INFORMATION .75-IN-WD 2-IN-LG PPR	28480	7120-4835
MP42	3160-0092	3	1	FAN GUARD	28480	3160-0092
MP44	54120-04103	6	1	FAN COVER	28480	54120-04103
MP45	54120-04702	1	1	FAN SPACER	28480	54120-04702
S1	3101-2911	5	1	ROCKER SWITCH (STANDBY)	28480	3101-2911
W1	8120-1521	6	1	POWER CABLE	28480	8120-1521
W2	54100-61602	6	1	HPIB CABLE	28480	54100-61602
W3	54120-61618	8	1	UMBILICAL CABLE 2 METRE	28480	54120-61618
W4	54120-61612	2	1	MAINFRAME CABLE ASSEMBLY	28480	54120-61612
W5	54100-61601	5	1	RIBBONCABLE-I/O TO FRONT PANEL	28480	54100-61601
W6	54100-61612	8	2	CABLE AC BD CO ANAL & DIG BD	28480	54100-61612
W7	NOT ASSIGNED					
W8	54110-61601	7	1	3 WIRE CABLE - COLOR DISPLAY MODULE POWE	28480	54110-61601
W9	54111-61610	9	1	POWER SWITCH CABLE 2 WIRE-FRONT PANEL ST	28480	54110-61610
W10	54111-61611	0	1	2 WIRE CABLE-REAR CABLE STBY SWITCH	28480	54111-61611
W11	54110-61611	9	1	DISPLAY CONTROL CABLE	28480	54110-61611
W12	54110-61607	3	1	RIBBON CABLE DISP ASSY TO COLOR MODULE	28480	54110-61607

Table Of Contents

Disassembly

Disassembly 6A

Introduction

This section contains removal and replacement procedures for HP 54120B Digitizing Oscilloscope Mainframe assemblies.

Safety Considerations

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

Warning

This instrument is equipped with a standby switch on the front panel that DOES NOT de-energize the power supply. To avoid shock hazards capable of causing injury or death, the main power switch on the rear panel must be used to de-energize the instrument or the power cable must be disconnected when the instrument must be de-energized.

Warning

These procedures are used while repairing an instrument that has protective covers removed and may have had power applied. Maintenance should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock). Read the Safety Summary in the front of this manual.

Caution

Do not remove or replace any of the circuit board assemblies in the instrument unless instrument power is removed. The boards contain components which may be damaged if the board is removed or replaced when instrument power is applied.

Tools Required

The hardware requires TORX™ type tools for removal and replacement. Sizes required for the procedures in this section are #10 and #15. A medium posi drive is used for the top cover.

If the display must be replaced, an 8 mm wrench or driver is also required.

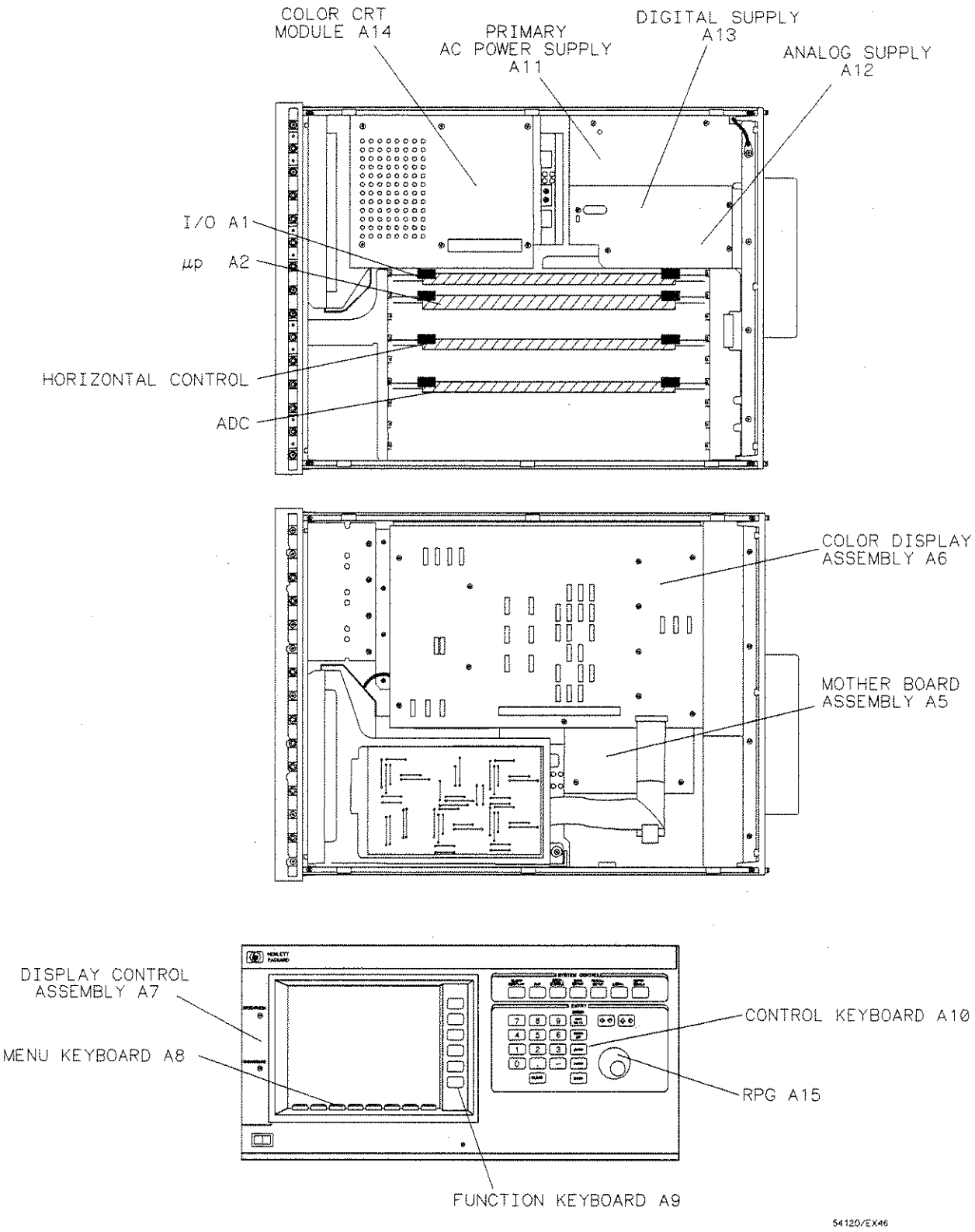


Figure 6A-1. Major Assembly Locations

Card Cage PC Assemblies

The following procedures should be followed when disassembling the instrument. Particular care should be taken when inserting the card cage assemblies into the mainframe to avoid bending the connector pins. There are only four cables connecting to the card cage assemblies. These four cables are different in size and their proper connection is easily determined.

Removal

1. Disconnect power cable.
2. Remove top rear feet and top cover.
3. Disconnect any cables from assembly to be removed.
4. Refer to the illustration on top of the power supply shield. Release PC assembly by pulling the flexible plastic extractors away from the assembly shield, then up.
5. Remove the assembly from the connector by pulling up on the extractors.

Replacement

1. Insert PC assembly shield edges in proper guides.
2. Keep the extractors up while sliding the assembly in.
3. While keeping assembly properly aligned in guides, push it in. As the top edge of the assembly becomes level with the top of the card cage the connector will start to engage. Keep assembly level and apply even pressure until connector is seated.
4. Reconnect all cables which were disconnected from any assemblies.

Caution

Do not use the extractors to lever the assembly into the connector. Using the extractors makes it too easy to apply excessive force that might bend misaligned connector pins. If the connector will not seat, remove the assembly and check for bent pins. Bent pins are very expensive and time consuming to replace on the motherboard SIB connector. Avoid pinching cables between the assembly and the mainframe.

Primary Supply

Removal

1. Disconnect power cable.

2. Remove rear feet from top right corner and left side.

3. Remove top and left side covers.

Caution

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.

4. Through the hole in the top power supply shield, observe the red LED on the primary power supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding (approximately three minutes).

5. Remove top power supply shield (six screws).

6. Remove the screw that attaches the ground wire (green/yellow) to top corner of rear frame.

7. Remove the three cables at the top front of the primary power supply PC assembly.

8. Remove four screws from power supply side cover. Refer to figure 6A-2.

9. Remove two screws which attach power supply assembly to rear panel. Refer to figure 6A-2.

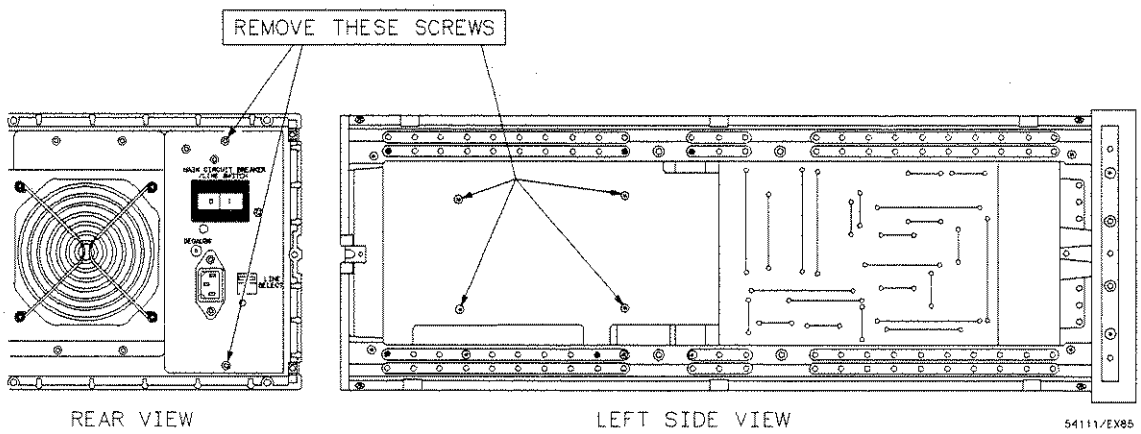


Figure 6A-2. Primary Power Supply Mounting Screws

10. Turn instrument onto its left side. Pull the power supply assembly rearward until the STBY switch cable at the rear of power supply assembly can be disconnected. Disconnect the cable.

11. Pull supply rearward until it clears the instrument.

Replacement

1. Reverse removal procedure to install supply.

Warning

Power supply safety grounding will be defeated if ground wire removed in step 6 above is not reconnected. To avoid a defeated ground, make sure the green/yellow wire is re-attached to top rear corner of the rear frame.

Analog Supply

Removal

1. Disconnect power cable.

2. Remove top rear feet and top cover.

Warning

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.

3. Through the hole in the top power supply shield, observe the red LED on the primary power supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding (approximately three minutes).

4. Remove top power supply shield (six screws).

5. Disconnect the analog power supply input cable from the top front corner of the primary power supply.

6. Use a flat-blade screwdriver to loosen the captive screw at the bottom front of the supply.

7. It may be easier to remove the analog supply by first removing the I/O assembly from the mainframe. However, this will cause a loss of all front panel cals, any stored front panel setups, and all stored waveforms.

8. Release power supply board connector by pulling board straight up and off the guide posts.

Replacement

1. Reverse the removal procedure to install assembly.

Digital Supply

Removal

1. Disconnect power cable.

2. Remove top rear feet and top cover.

Warning

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.

3. Through the hole in the top power supply shield, observe the red LED on the primary power supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding (approximately three minutes)

4. Remove top power supply shield (six screws).

5. Disconnect the Digital Power Supply input cable from the top front corner of the Primary Power Supply.

6. Use a flat-blade screwdriver to loosen the captive screw at the front bottom of the supply.

7. Release power supply board connector by pulling board straight up and off guide posts.

8. Remove the supply from instrument by lifting front edge of board first then rotating board up and out.

Replacement

1. Reverse removal procedure to install board.

CRT Bezel

The keyboards at the side and bottom of the CRT can be removed by first removing the CRT bezel.

Removal

1. While pushing down on top edge of bezel Refer to figure 6A-3, pull top edge away from front panel until holding tabs are clear of the front panel.
2. Lift bezel slightly and pull bottom of bezel away from front panel.
3. Pull bezel away from front panel just far enough to gain access to the ribbon cable connectors on control keyboard. They are just to the right of the bezel opening in the front panel.
4. Disconnect the two ribbon cable connectors from the control keyboard.

Function & Menu Keyboards

5. If either the function or menu keyboard needs replaced, they are each attached to the bezel with two screws.

Replacement

1. Reverse the removal procedure to install bezel.

Note

The ribbon cables must be reconnected as follows: function keyboard cable (right side of bezel) to top connector on control keyboard and menu keyboard cable (bottom of bezel) to bottom connector on control keyboard.

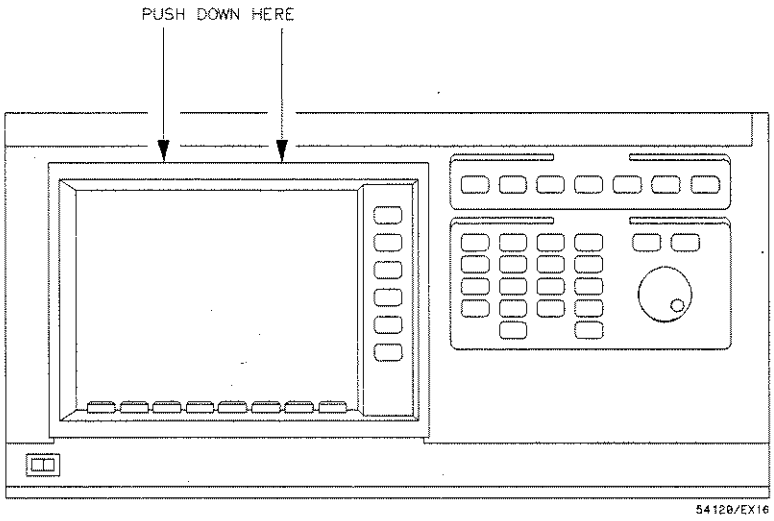


Figure 6A-3. CRT Bezel Removal Pressure Locations

Front Panel

Use steps 1 through 10 to remove front panel, steps 1 through 11 to remove display control, and steps 1 through 10 and steps 12 and 13 to remove control keyboard.

Note

It is not necessary to remove the front panel to remove the keyboards around the CRT bezel. See the previous removal procedure.

Removal

1. Disconnect power cable.
2. Remove rear feet and top, bottom, and side covers.
3. Remove top, and side trim strips from the front frame by carefully prying up at the strip's ends with a flat blade screwdriver.
4. Remove two front panel screws that are under each side trim strip.
5. Remove six front panel screws as shown in figure 6A-4.

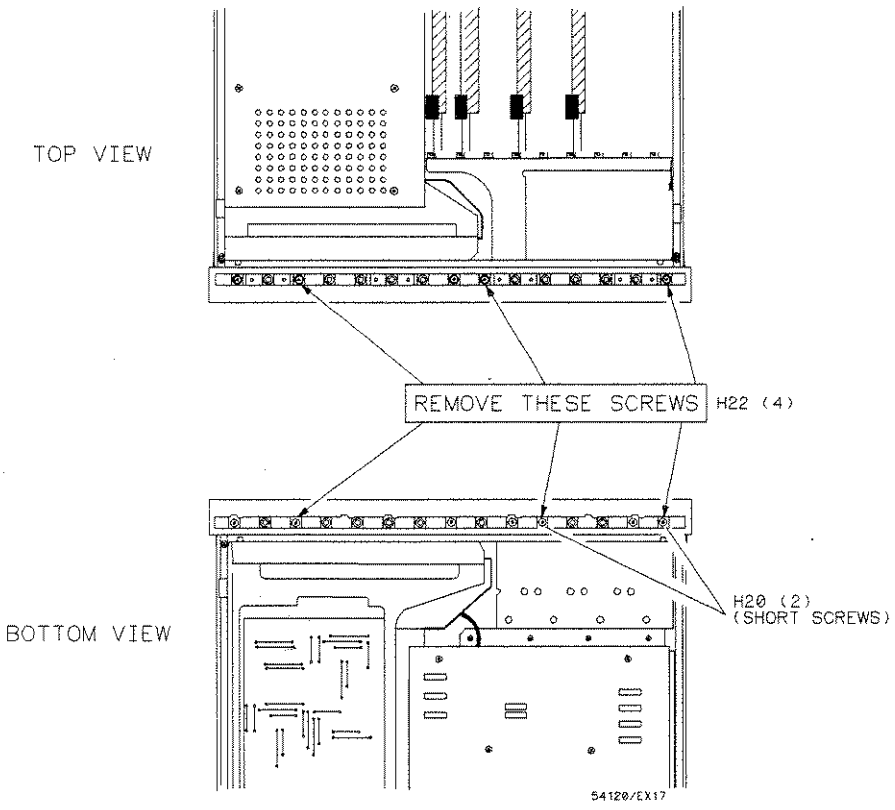


Figure 6A-4. Front Panel Mounting Screws

6. Set instrument in its normal operating position.

7. Disconnect the STBY switch by separating the two-wire interconnect just to the right of the CRT.

8. Pull front panel just far enough to gain access to the cable connector on the CRT control board (left side of front panel) and disconnect the cable.

9. Open the two cable ties: top left, inside front panel and top right of CRT, and remove the cables.

10. Disconnect the large ribbon cable from the control keyboard and remove the front panel from the instrument.

Display Control

11. Remove two screws attaching the display control assembly.

Control Keyboard

12. Disconnect the RPG cable at the control keyboard and the two cables from the CRT bezel keyboards.

Note

The menu keyboard (right side of bezel) cable connects to the top connector and the function keyboard (bottom of bezel) cable connects to the bottom connector on the control keyboard.

13. Remove five screws to remove the board.

14. Pass RPG cable through hole in control keyboard.

Replacement

1. Reverse the procedure to replace any of these assemblies.

Color CRT Module Removal

The color CRT module is replaceable only as a complete unit.

1. Remove front panel. Refer to front panel removal paragraph.
2. Disconnect the flat wide ribbon cable from the color display assembly and remove cable from clip.
3. Remove four screws that attach the color display module to the front frame. Refer to figure 6A-5.
4. Remove two screws attaching side of module to left side corner struts. Refer to figure 6A-5.
5. Slowly pull module forward until the power cable (small three-wire) can be disconnected at the primary power supply board.
6. Continue pulling module forward until it clears the instrument.

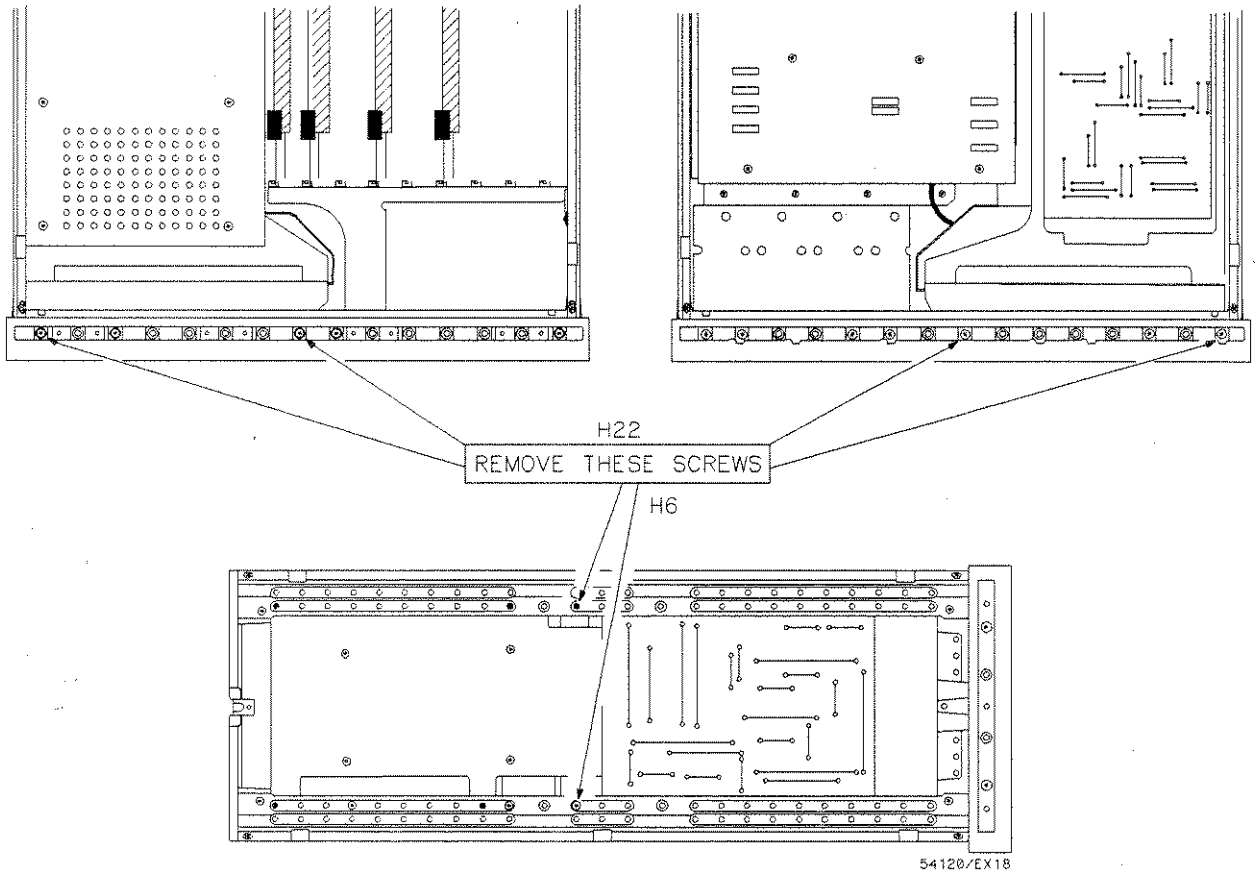


Figure 6A-5. Color CRT Module Mounting Screws

Replacement

It is necessary to use the following procedure to remove several items from the inoperative color CRT module and install them on the new one. These parts are not included with a new color monitor module.

Transfer Parts To New Module

1. Remove the eight small screws that hold the shield to the top and side of the inoperative module.

Note

These screws are special self-tapping screws, different from the screws in the rest of the instrument. They must be used for mounting the shield on the new module. Do not use them for any other purpose.

2. Use an 8 mm wrench to remove the four nuts on the front of the inoperative module and remove the shield.

3. Remove the front mounting brackets and put the 8 mm nuts back on the module.

4. Remove the 8 mm nuts from the new module, do not remove any other hardware, and install the front mounting brackets.

5. Install the shield on the new module. Place it over the two front mounting screws and front mounting brackets.

6. Install the four 8 mm nuts but leave them loose so the shield can move.

7. Use the special self-tapping screws (step 1) to fasten the top and side of the shield. They will be hard to start while they are tapping the holes. Be careful that excessive tightening does not strip the self-tapped holes.

8. Tighten the 8 mm nuts at the front of the module.

9. The rear bracket is two brackets connected together by shock mounting hardware. Remove the two screws that hold the bracket assembly to the rear of the inoperative module.

Note

These screws are special self-tapping screws that must be used for mounting the bracket assembly on the new display. Do not use them for any other purpose.

10. Mount the rear bracket assembly on the new module. The screws will be hard to start because they must self-tap the mounting holes. Be careful that excessive tightening does not strip the self-tapped holes.

11. Note the routing of the power cable and CRT control cable and one at a time, remove them and install them on the new module.

12. Remove the wide flat ribbon cable from the old module and install it on the new one.

Install New Module

13. Install the new module most of the way into the instrument. Avoid pinching cables as module is being installed.

14. Connect the power cable to the appropriate connector at the top front corner of the primary power supply and slide module the rest of the way in.

15. Install, but do not tighten, the two rear and four front mounting screws. Refer to figure 6A-5.

16. Install the front panel. Use the steps given in the front panel procedure except for steps 3, 2, and 1.

17. Push the module forward, closing as much as possible the gap between the CRT and the bezel. Tighten the two rear and four front mounting screws.

18. Complete the rest of the instrument assembly by doing steps 3, 2, and 1 of the front panel procedure.

Fan

Removal

1. Disconnect power cable.
2. Remove bottom rear feet and bottom cover.
3. Disconnect fan power cable from rear corner of motherboard.
4. Remove fan housing mounting screws as shown in in the figure 6A-6.
5. While noting fan cable routing, carefully remove fan housing from instrument.

Replacement

1. Reverse removal procedure to install fan. Be sure fan power cable does not get pinched between fan and rear panel.

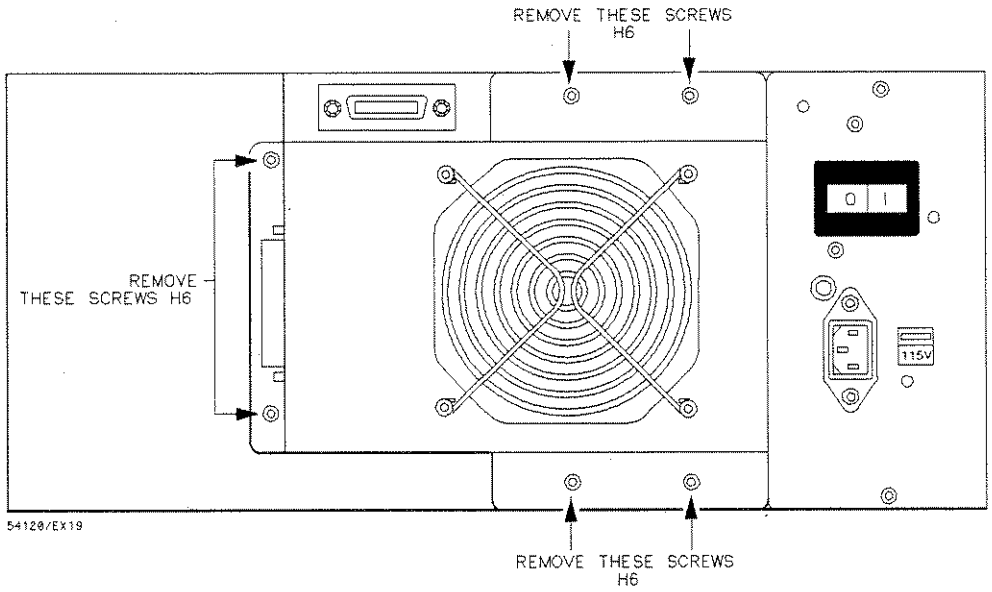


Figure 6A-6. Fan Housing Mounting Screws

Color Display Assembly

Removal

1. Disconnect power cable.
2. Remove bottom rear feet and bottom cover.
3. Disconnect wide ribbon cable from color display assembly.
4. Refer to figure 6A-7 to remove eleven assembly mounting screws.
5. Carefully lift board straight up to disengage motherboard connector.

Note

The display assembly to motherboard connector will exhibit some removal resistance while the board is being removed. It is recommended the major lifting force be exerted on the edge of the color display assembly at the connector.

6. Note the "comb" type connector used between the color display assembly and motherboard. It consists of two separate combs held in place on the color display assembly by a connector guide and two screws. If the assembly is being replaced, this connector guide and the two comb connectors must be removed from the old assembly and installed on the new one. The connector DOES NOT come with the new assembly.

Replacement

1. Install the comb connectors and connector guide on color display Assembly.
2. Reverse removal procedure to install assembly. Use additional care when inserting the connector pins into connector on motherboard.

Note

Power for the color display assembly is obtained from the motherboard by the four short mounting screws. Their positions are marked +5 and GD on the board. These mounting screws must be installed and tightened before proper operation of the instrument can be expected.

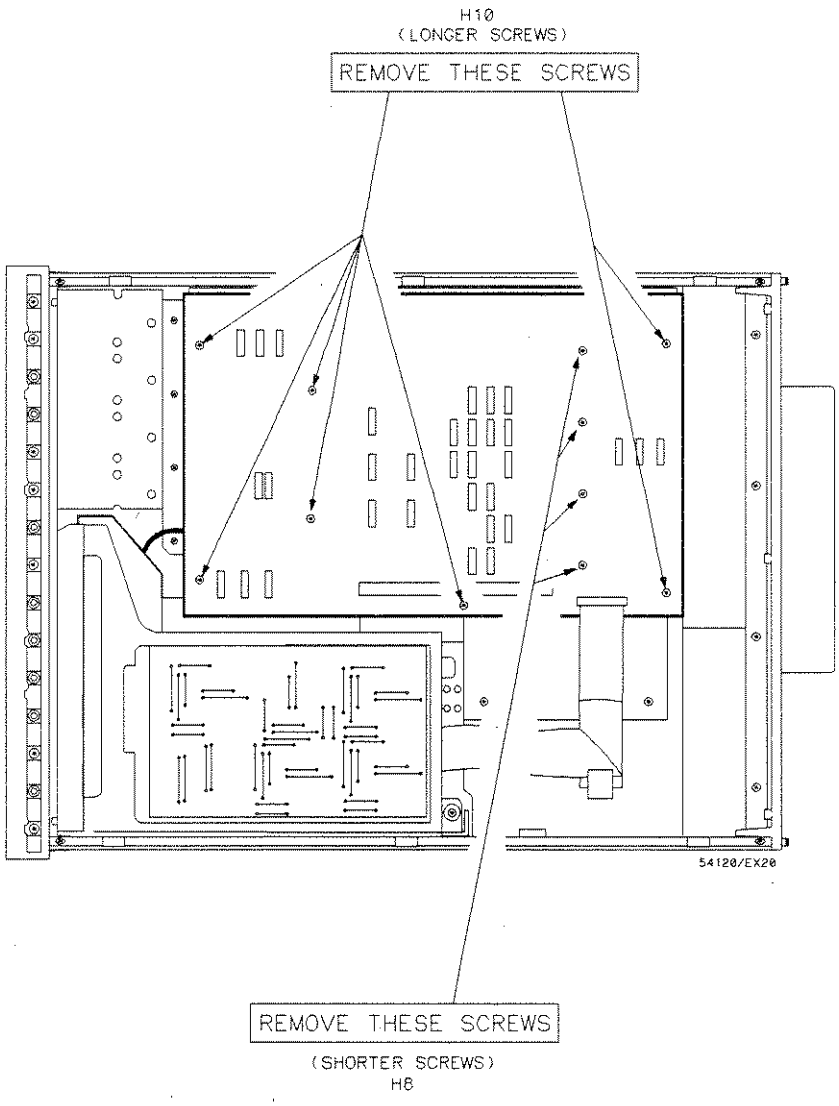


Figure 6A-7. Color Display Assembly Mounting Screws

Motherboard

Removal

1. Disconnect power cable.
2. Remove rear feet and all covers.
3. Remove all card cage PC boards. Refer to card cage assembly removal paragraph.
4. Remove analog power supply and digital power supply. Refer to digital power supply removal paragraph.
5. Remove color display assembly. Refer to color display assembly removal paragraph.
6. Disconnect fan power cable connector from rear corner of motherboard.
7. Loosen the STBY switch cable by removing the two nylon cable clamps from bottom of motherboard. Squeeze the clamps and pull them from the holes in the board.
8. Remove the remaining mounting screws and remove board. Refer to figure 6A-8.

Replacement

1. Reverse removal procedure to install board.

Note

The motherboard and display board share some of the same mounting screws. Therefore, when installing the motherboard install only the screws removed in step 8 above. Refer to figure 6A-8.

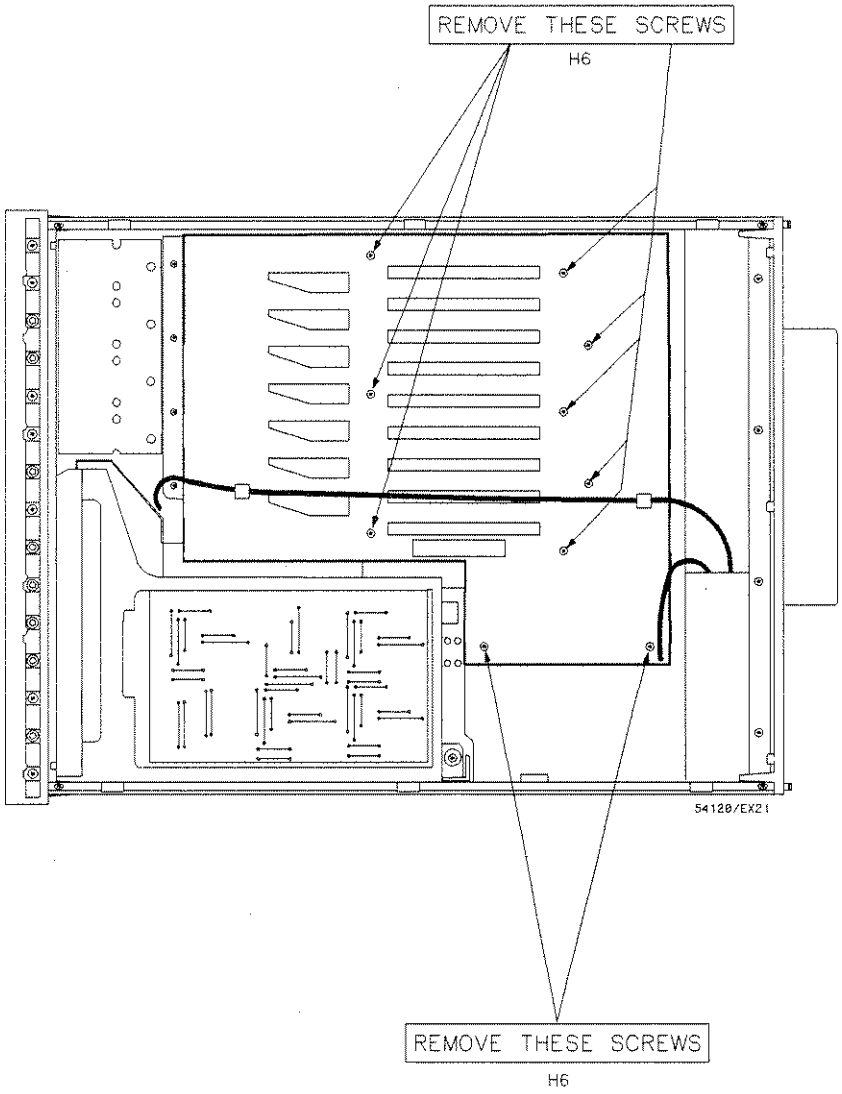


Figure 6A-8. Motherboard Mounting Screws

Table Of Contents

Theory

Theory 6B

Introduction

This section is the theory of operation for the HP 54120B Digitizing Oscillosocpe Mainframe. It includes overall system block diagrams and system theory of operation, printed circuit assembly (PCA) block diagrams and PCA block level theory of operation.

System Theory

This theory of operation refers to the System Block Diagram, figure 6B-1. It includes the mainframe and four channel test set, and is presented in block diagram format with a brief description of each block's basic functions. The theory's purpose is to help give a basic understanding of the instrument's overall operation as an aid in troubleshooting to the board level.

Motherboard

Each of the four card cage assemblies (A1 through A4) plug into the motherboard (A5). The 9 motherboard connectors each have a hard-wired identification code (0 through 8). Each plug-in assembly has a built-in identification code. Therefore, any assembly can be placed in any motherboard connector and the microprocessor (CPU) can identify what type of assembly is in each slot. This information can be displayed on the HP 54120B CRT by pressing **Utility** menu, then **Test menu**, then **Display Configuration**. Note that the microprocessor's position is displayed as an empty slot. The factory configuration is the preferred assembly locations. For troubleshooting purposes, any assembly may be temporarily placed in any location. However, some cables may be too short to reach all motherboard locations.

Power Supplies

There are three power supply assemblies within the HP 54120B mainframe system. The primary power supply (A11) receives its input from the power line on the rear panel. The rear panel contains an EMI (electromagnetic interference) circuit and the main circuit breaker. The primary power supply contains voltage regulation to output 300 volts used by the analog supply (A13) and digital supply (A12), and 120 volts used by the color CRT module A14. The analog power supply regulates the 300 volt input, and supplies ± 18 volts and ± 8 volts for the instrument's analog circuits. The digital power supply regulates the 300 volts to supply ± 5 volts for the instrument's digital circuits. Both of these power supplies have their own ground systems which are isolated from each other. Therefore, voltage measurements must be made to the proper common points.

Front Panel Interface

The front panel contains system control keys, softkeys, a keypad, and a knob. All these devices are on or wired through the control keyboard (A10). All information from the control keyboard is input to the I/O assembly through a large ribbon cable connected near the front of the I/O assembly. The keypad and softkeys are set up in a matrix so that the I/O assembly can scan the lines of keys by outputting a pulse on each line. If a key is closed (pressed), the I/O assembly will detect the return of the pulse on another line. By knowing which line the pulse was output on and which line the pulse was returned on, the I/O assembly can determine which key was pressed. These key scan lines are passed through the large ribbon cable from the I/O assembly.

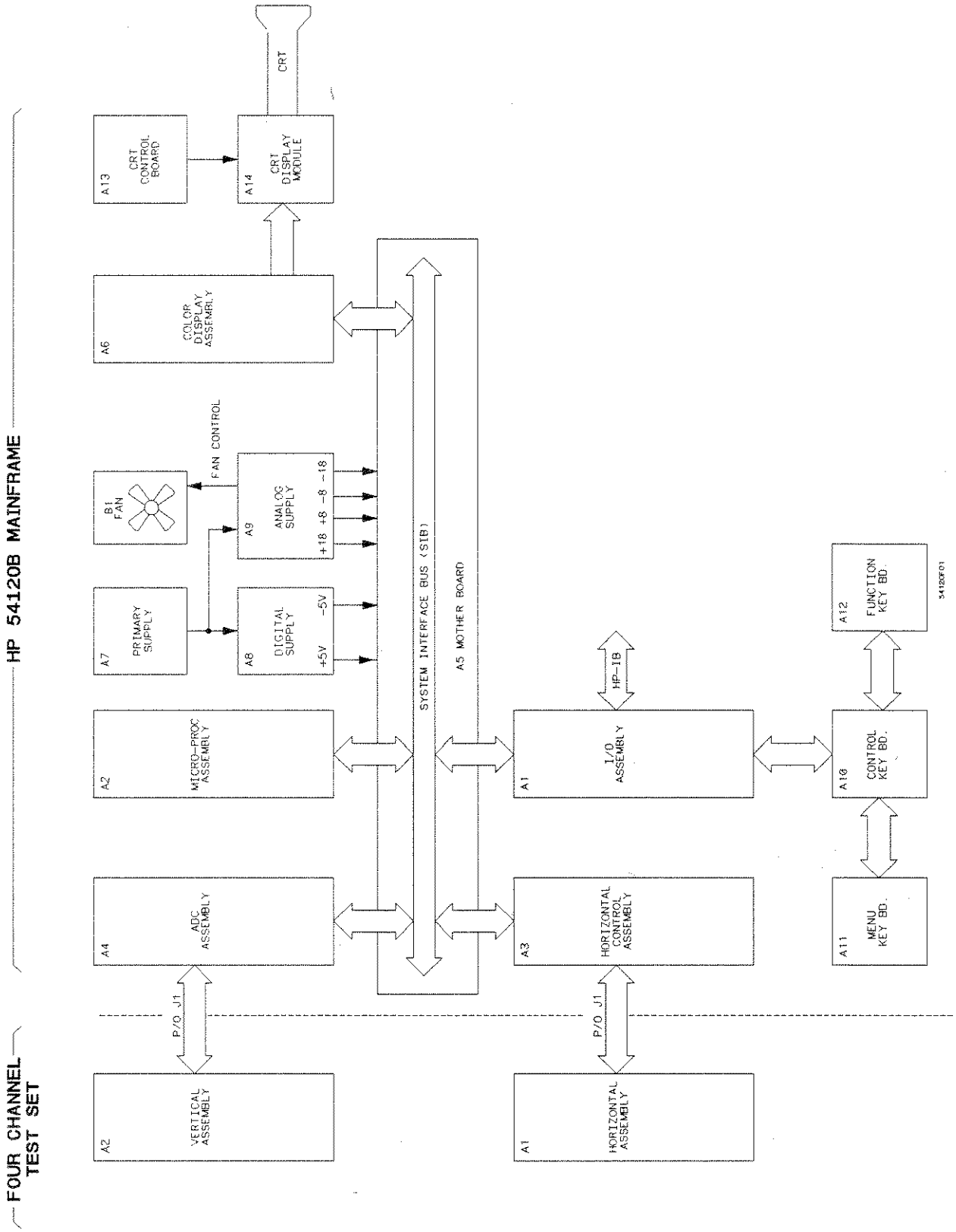


Figure 6B-1. System Block Diagram

Display System

The color CRT module receives horizontal and vertical sync pulses, and character and graphics data from the color display assembly (A6). These signals are connected to the color CRT module through a ribbon cable from the side of the color display assembly. The color CRT module creates the sweep signals, blanking, and voltages required to display information on the CRT.

HP-IB System

The HP-IB connector on the rear panel of the instrument is connected by a ribbon cable to the top rear of the I/O assembly. The I/O assembly contains an HP-IB interface integrated circuit to convert data to proper HP-IB format

System Interface Bus

All digital data is moved between the HP 54120B mainframe assemblies over the system interface bus (SIB). The SIB has data, address, and control lines all under the CPU's control. Many of the assemblies have a local data bus (LDB) which is under the assembly's own control. The SIB and the local data buses must not be confused. In most cases data and addresses are accepted by an assembly from the SIB under CPU control, then the data is manipulated by that assembly on its local data bus.

Microprocessor (CPU) Assembly

The microprocessor assembly has a 68000 microprocessor, 384k bytes of ROM, 32k bytes of non-volatile RAM (battery back-up), programmable timer, and bus request/bus grant circuits. The assembly has an internal data bus, so it can process data without tying up the System Interface Bus. Data is moved on the SIB under control of the 68000 microprocessor. The assembly also has logic circuits so it can operate with another microprocessor on the SIB, in which case the bus request/bus grant circuits would be used. In the HP 54120B only one microprocessor is used, therefore the bus request/bus grant signals are tied to the proper logic levels so the 68000 microprocessor will have control of the SIB when required.

Display Assembly

The display assembly has 128k bytes of dynamic RAM (DRAM) used as the dot memory to store signal data to be displayed. It also has a character generator and character refresh circuits for the characters that will be displayed. The assembly produces vertical and horizontal sync signals so signal and character data are displayed on the CRT at the proper place and time.

I/O Assembly

The I/O assembly has interface circuits to read the front panel devices, including softkeys, knob, system control keys, and keypad. The assembly also has HP-IB interface logic, clock circuit which produces the required microprocessor clocks, power on reset circuit which resets the microprocessor, additional CPU dynamic RAM memory, other logic which starts up the CPU to a known condition, and a battery which powers the non-volatile RAM on the CPU assembly.

Horizontal Control Assembly

A user inputs various timebase and trigger selections to the HP 54120B. The CPU communicates these selections and acquisition control signals to the horizontal control assembly over the SIB. The horizontal control assembly translates these CPU instructions into various trigger and timebase signals for the horizontal and vertical assemblies located in the four channel test set. These signals control the sampling and data acquisition process. An acquisition cycle is defined as the sequence of events that must occur in order to acquire a single data point per enabled channel. It will normally be the case that several acquisition cycles will be required to adequately display a waveform.

Horizontal Assembly (located in test set)

The horizontal assembly has the trigger and timebase hybrids. After a trigger occurs and delay has reached terminal count, the horizontal assembly enables the sample pulse generator. The sample pulse generator momentarily turns the samplers on. Block diagram and theory is in the test set manual.

Vertical Assembly (located in test set)

The vertical assembly momentarily samples incoming signals during a very narrow time window, 17 ps. It then amplifies and converts the sample to a bipolar pulse. A bipolar pulse is easier for the ADC assembly's track and hold circuitry to follow the pulse's peak amplitude. Block diagram and theory is in the test set manual.

ADC Assembly

The ADC assembly has track and hold circuitry which tracks the bipolar pulse's amplitude and holds the peak value. It also contains an analog to digital converter which converts incoming analog signals into a digital word. This digital word is read by the CPU and is either displayed on the CRT or used in waveform math functions.

Acquisition Cycle

The acquisition theory of operation is presented in a program flowchart. The flowchart applies directly to the infinite persistence mode, which is the simplest flowchart. Variable persistence and average modes have a few added steps to the flowchart. The microprocessor (CPU) controls an acquisition cycle with software instructions. The flowchart is presented from the CPU's point of view. The following steps are software instructions, with added indented comments. The comments will tie the software and hardware theories together.

Start: Program timebase delay

Program A/D input control switches.

The user selects which channels he wants on. The CPU will write to the proper switch enable lines 1-4 (SW1-4) which channels are on and which are off. There are four samplers on the vertical assembly and only one A to D converter on the ADC assembly. All four samplers fire at the same time and the track and hold circuitry will hold the analog values of each channel. Logic on the ADC assembly will search the SW1-4 lines looking for which channels are on. The A to D converter will process, one at a time, only the on channels. The analog signals are converted to digital words which the CPU can display on the CRT. Data from the off channels is not used.

Wait for timebase to settle.

The CPU is waiting for the fine delay DAC (U28) on the horizontal control assembly to settle. The wait time is 50 μs.

Go to Enter1

Loop: Program A/D input control switches

As earlier, this step reprograms the SW1-4 switches on the ADC assembly.

Enter1: Reset GO bit

This is the low go reset (LGORESET) on the horizontal control assembly.

Enable trigger, samplers on.

This step enables various lines to latches U1 and U2 on the horizontal control assembly. The trigger enable line will go low. The sampler high on/low off line (ON/LOFF) will go high at the end of coarse delay. This allows the samplers to sample incoming signals.

Wait for GO bit

The horizontal control assembly uses the GO bit to signal the CPU to process sampled data. The CPU will wait on the GO bit signal before it does any other tasks. If the GO bit is held in a disabled mode, the CPU could hang up in a wait loop. Pressing any front-panel key will exit this wait loop.

Reset GO bit

After the CPU sees the GO bit go high, it resets the GO bit low so the GO bit can signal the CPU when the next sample is taken.

Skip sample

The longest coarse delay word represents 458.752 μs of delay. Longer delays are accomplished by using a software counter. Coarse delay will count down from 458.752 μs to zero. The trigger will fire, and a sample will be taken. Software will check to see if enough delay time has passed. If more delay is needed, then the sample is discarded and the coarse delay counters will start over again.

Disable Trigger.

If the trigger is not disabled, then the timebase would continue to count down and enable the trigger every 458.752 μs. This would cause a new set of data points to be acquired by the samplers and the old set of data points would be discarded. By disabling the trigger on the horizontal control assembly, the timebase will be stopped and data points will not be discarded before the CPU has time to process them.

Read A/D.

The CPU will read the output of the A to D converter for the first channel that is on. Then the A to D converter will process the signal from the next channel that is on. The Track and Hold ICs have a capacitor which holds the sampled data value. The acquisition cycle is interrupt driven with the acquisition interrupt (GO bit) having the highest priority.

Program timebase delay for next acquisition.

This is a repeat of the timebase set-up in the Start routine discussed earlier. While the CPU is processing sampled data it allows enough time for the fine delay DAC to settle within the 50 μs time frame.

If channel 1 is on, then Wait for A to D to finish a conversion.

The CPU is monitoring the status line (STS) from the ADC assembly. Status tells the CPU that an A to D conversion is finished, and it is time to read the A to D's digital output word.

Read A to D converter.

After the CPU reads the A to D converter's output, the low chip select analog to digital converter (LCSAD) will signal the A to D to do a conversion on the next channel which is on.

Plot data if appropriate.

The CPU does not always plot digitized data. It depends on what functions the user selected. The data may be used in waveform math and only the results would be plotted on the CRT. Data may also be acquired specifically to be sent over the HP-IB.

If channel 2 is on, then Wait for A to D to finish a conversion.

The steps for channels 2-4 are identical to the steps for channel 1.

Read A to D converter.

Plot data if appropriate.

If channel 3 is on, then Wait for A to D to finish a conversion.

Read A to D converter.

Plot data if appropriate.

If channel 4 is on, then Wait for A to D to finish a conversion.

Read A to D converter.

Plot data if appropriate.

If the trace is at the end of a sweep, then plot any functions which are on.

It takes the CPU a long time to finish plotting functions. The acquisition hardware may have a block of dead time waiting for the CPU to finish plotting functions.

Go to Loop

Variable Persistence

For variable persistence mode there is an added step before the GO to loop step. This step checks if it is time to erase any of the old data points. The CPU may spend as much time erasing old data points as acquiring new data points.

Average Mode

In the average mode software feedthrough compensation is done. With the samplers turned off, the output of the samplers is digitized through the A to D converters. This first value is the result of sampler feedthrough. Then the samplers are turned on and their outputs are digitized again. This second value is the sum of sampler feedthrough and an actual data point. The first value is subtracted from the second, and the result is the actual digitized point.

ADC Assembly

The following block level theory of operation refers to the analog to digital converter (ADC) assembly block diagram in figure 6B-2.

Track and Hold

The track and low hold (T/LH) signal from the horizontal control assembly enables the track and hold circuitry to detect the first half cycle of the bipolar pulse's amplitude and hold its peak analog value. The bipolar pulse comes from the test set.

Analog Switch Enable

The microprocessor (CPU) enables one or more of the four vertical channels by enabling the proper SW1-4 lines. The combinational logic circuit searches for which channels are on by looking at which of the SW1-4 lines were enabled by the CPU.

Combinational Logic

When enabled by T/LH, the combinational logic circuit searches for the first channel that is turned on. After the first on channel is found, the combinational logic circuit enables the A to D to convert that channel's track and hold output to a 12-bit digital word. After the A to D conversion is finished, the CPU reads the A to D's output. The combinational logic circuit then continues to search for the next channel that is on. This process continues until reset by the T/LH signal, at which time the sequence is started over again.

Analog Switch

The analog switch sends the track and hold outputs, one at a time as directed by the combinational logic circuit, to the 12-bit analog to digital converter (A to D).

Status

The CPU waits until status indicates that the A to D is done with a conversion before reading the A to D's digital lines.

A to D

The A to D converts analog signals to a 12 bit digital word. This digital word is sent through bidirectional bus drivers U37 and U38. The CPU transfers these digital words over the system interface bus (SIB) to the display assembly.

Board ID

The CPU knows the location of each card cage assembly by asking each board for its unique ID number during the initial power-up sequence. Each assembly accessed by the CPU over the SIB has a unique board ID number.

Offset Dac Enable

The offset DAC (digital to analog converter) enable decodes address lines A4-6 into four lines called low chip select offset DAC lines 1-4 (LCSOD1-4). The CPU accesses each offset DAC by enabling one of these four lines.

Offset DACs

There is an offset DAC for each of the four channels. The offset DAC converts 14-bit digital (DAD0-13) words to an analog voltage. The analog voltage is then converted to a current with a range of ± 50 mA. Current drive is used to help reduce cable noise pickup while the offset current is sent through the umbilical cable to the vertical assembly.

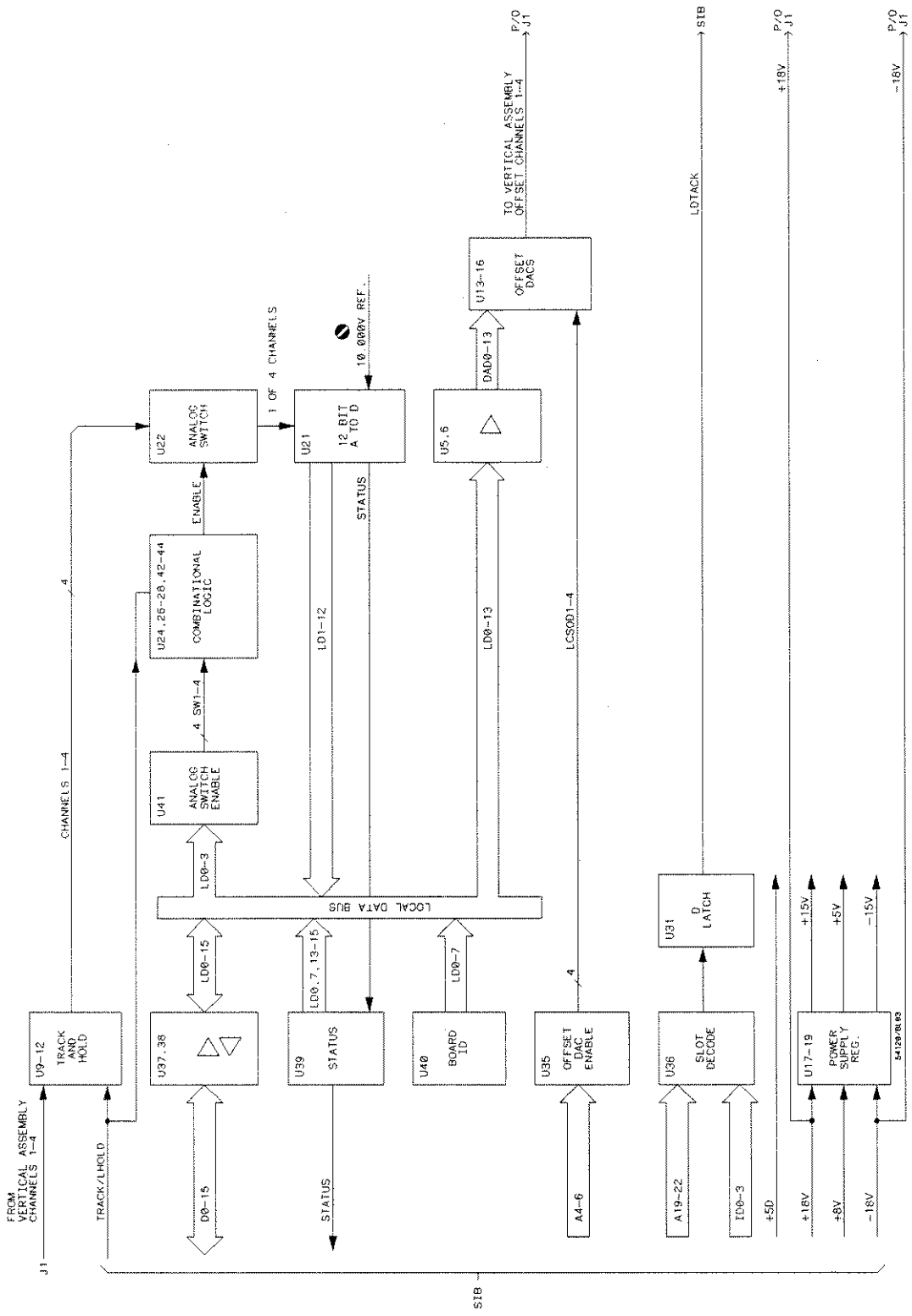


Figure 6B-2. ADC Assembly Block Diagram

Slot Decode The CPU accesses this board by sending out the board's slot ID code over address lines A19-22. U36 is a four bit comparator which compares slot address lines A19-22 with slot ID codes ID0-3. When the two codes are equal, U36 pin 6 enables other circuitry.

D Latch The D Latch signals the CPU that it has received data with the LDTACK (low data acknowledge) line.

Mnemonics	Definition
A19-22	Address lines 19-22
CCLK1	C Clock 1
CCLK2	C Clock 2
LCSAD	Low Chip Select Analog to Digital converter
DAD0-13	Digital to Analog Data lines 0-13
D0-15	Data lines 0-15
DTRC	Delay To Read Convert
H/LL	High for high bandwidth enable, Low for low bandwidth enable
H/LT	Hold/Low Track
LCSOD1-4	Low Chip Select Offset DAC's 1-4
LD0-15	Local Data lines 0-15
LDTACK	Low Data Acknowledge
LNCH	Low Next Channel
R/LC	High Read/Low Convert
STS	Status
SW1-4	Analog Switch lines 1-4

Horizontal Control Assembly

The following block level theory of operation refers to the horizontal control assembly block diagram in figure 6B-3.

Fine Delay DAC

U28 is a 12-bit DAC using LD2-13 to produce a level representing fine delay from 0 to 3.99975 ns. U31 uses LD0 and 1 as sub LSBs to give the DAC more resolution, 1/4 ps steps. This gives the trace a more uniform appearance.

Trigger Level DAC

The trigger level DAC is a 12-bit DAC which generates trigger level as selected by the front-panel. Trigger level is used by the trigger hybrid on the horizontal assembly in the four channel test set.

Freerun Clock Generator

U30 divides a 2 MHz clock to give a frequency range of 15.3 Hz to 500 kHz, selectable by the front-panel controls. The freerun clock signal drives the TDR generator and trigger hybrid located in the four channel test set. The freerun clock frequency directly affects the output frequency of the TDR generator.

Latches

U1 and U2 latch various trigger status signals to the horizontal assembly. These signals are: high frequency reject, trigger enable, TDR on or off, trigger hysteresis, and trigger slope. U11 latches four of the five LSBs of the coarse delay word going to the horizontal assembly. These are timebase bits 1-4 (TB1-4) and correspond to bits 0-3 of the coarse delay word.

Status

Status is the only block which transfers data back to the CPU. The GO bit tells the CPU to process sampled data on the ADC assembly.

Coarse Delay Counters

U10, 12, and U13 use the 12 most significant bits (MSB) of the 17-bit coarse delay word (LD4-15). When the counters have counted down to zero, a low terminal count signal (LTC2) is generated for the horizontal assembly in the four channel test set. The remaining 5 bits of the coarse delay word are used on the horizontal assembly in the four channel test set. The total length of time for the coarse delay counters is 4 ns to 458.752 μs. Longer delay times are achieved with software counters.

4 ns Bit

The fifth LSB of the coarse delay word going to the horizontal assembly is a sub LSB of the coarse delay word. It is TB0 SET and RESET and corresponds to bit 15 of the fine delay word. It is called the 4 ns bit because it is the fourth ns of the coarse delay time interval.

Track And Hold Generator

This circuit generates the track and low hold signal for the ADC assembly. Track means to track the output of vertical assembly. Hold means to hold the peak analog value until the A to D converter has time to do a conversion.

GO Bit Generator

It generates the GO bit which tells the CPU to process sampled data. When the GO bit is high, analog information is being held by the track and hold circuitry on the ADC assembly. This analog information is waiting to be converted into digital information by the A to D converter on the ADC assembly. When the GO bit goes true (low) it generates an interrupt which tells the CPU a sample has been taken (interrupt 7).

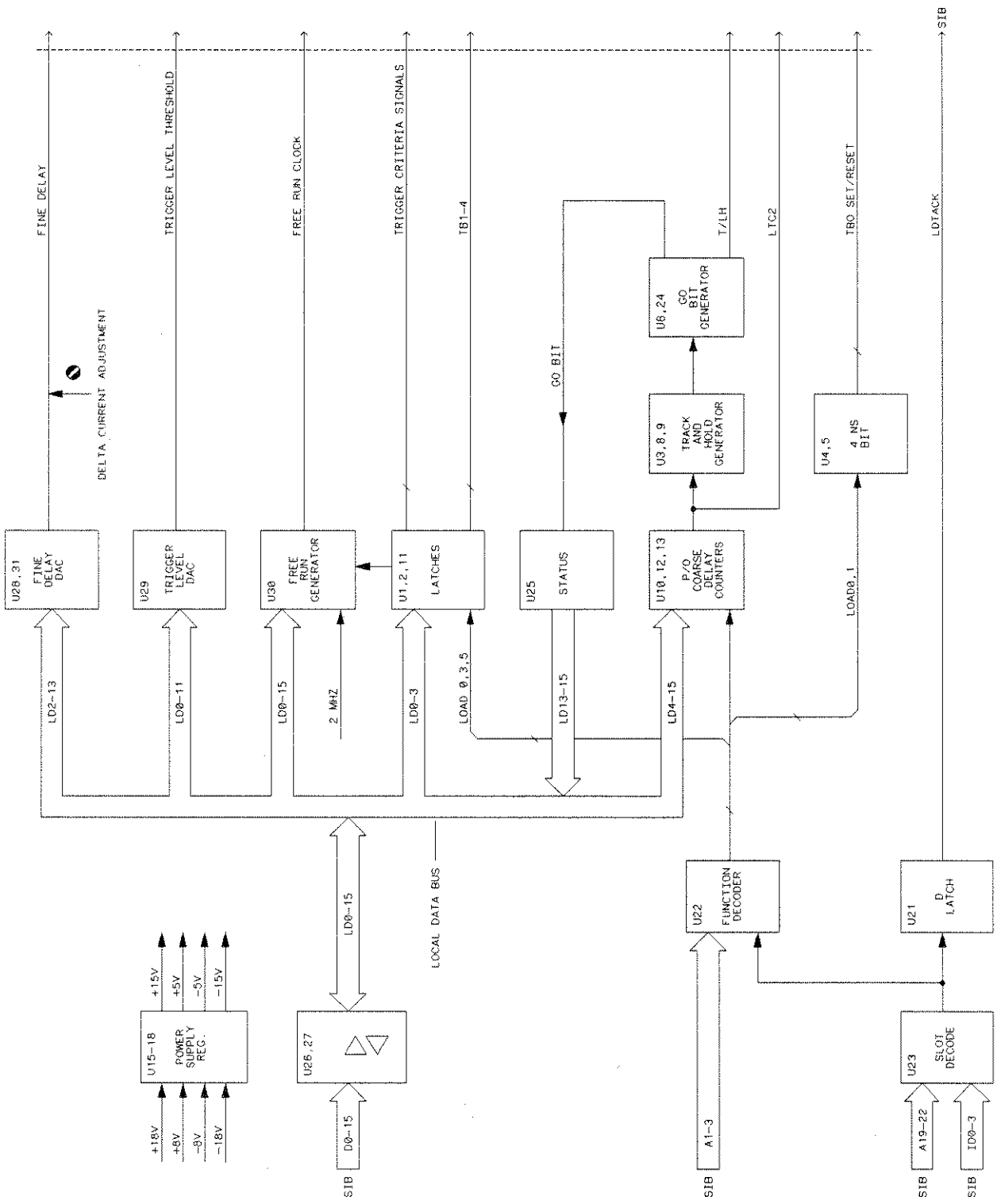


Figure 6B-3. Horizontal Control Assembly Block Diagram

Board ID The microprocessor (CPU) knows the location of each card cage assembly by asking each board for its unique ID number during the initial power-up sequence. Each assembly accessed by the CPU over the SIB has a unique board ID number. The horizontal control assembly generates board ID by pull-up resistors on the LD0-3 data lines, which will be all logic high levels.

Slot Decode The CPU accesses this assembly by sending out the board's slot ID code over address lines A19-22. U23 is a 4-bit comparator which compares slot address lines A19-22 with slot ID codes ID0-3. When the two codes are equal, U23 pin 6 enables other circuitry.

D Latch The D Latch signals the CPU it has received data with the low data acknowledge (LDTACK) line.

Mnemonics	Definition
A19-22	Address lines 19-22
D0-15	Data lines 0-15
GO	Tells the CPU to process sampled data
H/LT	Hold/Low Track
HF REJECT	Trigger High Frequency Reject
ID0-3	Board ID lines 0-3
LD0-15	Local Data Lines 0-15
LLDS	Low Lower Data Strobe
LDTACK	Low Data Acknowledge
LGO	Low GO
LGORESET	Low GO Reset
LIRQ7	Low Interrupt Request Line 7
LPWRONRST	Low Power On Reset
LSB	Least Significant Bit
LTC2	Low Terminal Count line 2
MSB	Most Significant Bit
Neg/LPOS	Trigger slope select high for Negative/low for Positive
OFF/LON	Turns TDR generator Off and On
R/LW	Read/Low Write
SELECT	Board Select
LENABLE/RESET	Trigger Low Enable/Reset
T/LH	Track/Low Hold
Sampler ON/LOFF	Turns Sampler ON and Off
SIB	System Interface Bus

I/O Assembly

The following block level theory applies to figure 6B-4. The I/O Assembly serves two major purposes. First, it provides instrument interface to the keyboard and HP-IB by two ribbon cables. Second, it provides several system functions, all of which are described below. In addition the I/O contains passive pull-up resistors for the data, address, and control lines for the System Interface Bus, (SIB).

Slot Decode

The CPU accesses this board by sending out the board's slot ID code over address lines A19-A22. U45 is a 4-bit comparator which compares slot address lines A19-22 with slot ID codes ID0-3. When the two codes are equal, U45 pin 6 will output a pulse which enables other circuitry.

LDTACK Generator

U35 generates LDTACK, which is sent back to the CPU indicating data was received. This signal also resets the bus error timer.

Bus Error Timer

Under normal operation U18 should be reset by LDTACK before a time constant set by R19 and C40 times out. If U18 is not reset, it will generate LBUSERR. This keeps the CPU from getting hung up in an instruction cycle. This could happen if any addressed board does not generate LDTACK or if the CPU tries to access a nonexistent board.

Board ID

One side of U42 is hardwired to represent the board ID number. When the CPU asks for board type, U42 places a board ID number on the local data bus.

HP-IB

U1 interprets HP-IB commands and controls the direction of data flow from an external controller to the local data bus. One side of U1, LD0-7, connects to the local data bus. The other side of U1 connects to two bidirectional data transceivers, U4 for data and U5 for control commands. Because HP-IB addressing is accomplished by software, no address lines are carried on the ribbon cable.

Function Decoder

Function decoder U10 decodes address lines A12-A14 to enable, keyboard controller, RPG counter, HP-IB controller, board type, and power supply status.

Keyboard Controller

Keyboard controller U21 sees a key closure and interrupts the CPU by the IRQ4 line. U21 detects which key was pressed by scanning column lines with pulses and sensing rows for a return path. When U21 is enabled, it converts key closure scan data to parallel data and places this data on the local data bus.

Dynamic Ram

The I/O assembly provides 256k words of additional CPU memory used for waveform storage and other purposes. The memory is an array of sixteen 64k by 4-bit dynamic RAMs. Dynamic RAM is addressed in rows and columns with low row address strobe (LRAS1-4) and low column address strobes (LCAS1-8). Dynamic memory must be refreshed at regular intervals to maintain memory. This is accomplished with refresh counters U19-31. From the CPU's perspective the dynamic RAM is a slot by itself, irrespective of the slot for the I/O assembly. The other assemblies are identified by their slot ID code. U51 is a 4-bit comparator which compares address lines A19-22 with code 10 decimal which is hardwired on the other comparator input. The CPU sees the dynamic RAM at slot 10 no matter which slot the I/O board is in.

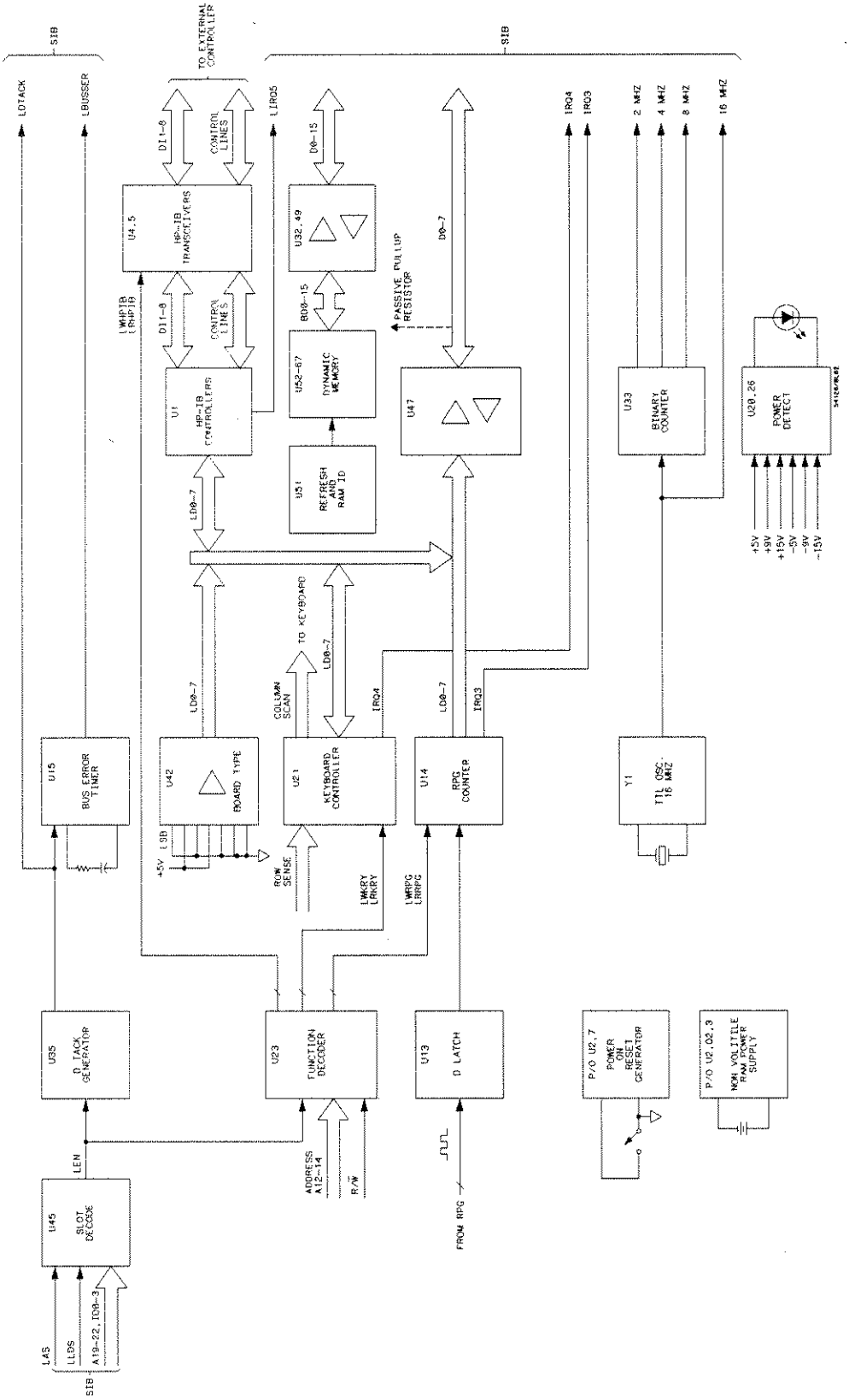


Figure 6B-4. I/O Assembly Block Diagram

RPG Counter

The RPG outputs two out-of-phase pulses. Direction of rotation is determined by the difference in phase angle between both pulses. The pulse frequency is a function of rotation speed and this tells the microprocessor (CPU) what size of incremental steps to take. Part of U13 detects RPG activity and interrupts the CPU by the IRQ3 line.

TTL Oscillator

The TTL oscillator is a crystal controlled 16 MHz oscillator. A binary counter divides this into 8 MHz, 4 MHz and 2 MHz. All four signals are placed on the system interface bus for use by other assemblies.

Power-on Reset

The power-on reset circuit provides a glitch-free pulse shortly after power up and power down. This sets many devices to a known state and prevents the CPU from taking damaging action during power up. This also provides a means to reset the system with a push button, without powering down the instrument.

Power Detect

The power detect circuit samples all six supply voltages. If one or more fails, the LED on top of the I/O assembly will not illuminate.

Non-volatile Ram Power Supply

A battery provides the necessary power for RAM on the CPU assembly to retain basic setup information and system configuration for several years. The circuit also provides for smooth transfer of power from the battery to the power supplies after initial power up.

Mnemonics	Definition
DI1-8	HP-IB Data lines 1-8
D0-7	SIB Data lines 0-7
DS	Data Strobe
IDO-3	Board ID lines 0-3
LIRQ1-7	Low Interrupt Request lines 1-7
LA1-3	Local Address lines 1-3
LAS	Low Address Strobe
LCAS1-8	Low Column Address Strobe lines 1-8
LDTACK	Low Data Acknowledge
LD0-7	Local Data lines 0-7
LEN	Low Enable
LLDS	Low Lower Data Strobe
LRAS1-4	Low Row Address Strobe lines 1-4
LRHPIB	Low Read HP-IB
LRKEY	Low Read Keyboard
LRPWR	Low Read Power
LRRPG	Low Read RPG
LSB	Least Significant Bit
LSTROBE	Low Strobe
LUDS	Low Upper Data Strobe
LWHPIB	Low Write HP-IB
LWKEY	Low Write Keyboard
LWRPG	Low Write RPG
R/LW	Read Low Write
RPG	Rotary Pulse Generator
SIB	System Interface Bus

Microprocessor Assembly

The following theory applies to figure 6B-5. The microprocessor (CPU) has two major functions, data acquisition and I/O interfacing. It starts an acquisition cycle by resetting the GO bit to a logic low level. The CPU then waits for the GO bit to go high again. The GO bit going high tells the CPU to process sampled data. I/O interfacing involves updating display information, interpreting key closure data, RPG data, and HP-IB commands. In remote mode the CPU takes commands from an external controller.

CTC The counter timer chip (CTC) contains three counters. The CPU programs and reads each counter over LD0-7 lines. Each counter has an output which is used as an interrupt to the CPU. All three counter outputs are ORed through U35 and U42. The result is ORed through U40 with LIRQ6 from the SIB and applied to the system interrupt latch.

System Interrupt Latch The system interrupt latch allows the CPU to mask off any or all interrupt lines. The CPU sends data to U1 on LD0-7 lines. For normal operation all outputs of U1 are normally a zero, and all incoming SIB interrupt lines are normally a one. When an interrupt occurs on the SIB that interrupt line will be a zero, the corresponding output of U17 or U18 will also be a zero. The CPU can mask off any interrupt lines by simply writing a one to U17 or U18 through U1. This will guarantee that corresponding output levels of U17 or U18 will also be a one regardless of what the SIB interrupt lines are doing.

Interrupt Priority Encoder This circuit encodes all seven incoming interrupt lines into three lines for the CPU. If more than one interrupt occurs at the same time, U34 will prioritize them so the interrupt with the highest priority will be processed first. When an interrupt occurs, the system is vectored to a predetermined software location.

Bus Arbitration This board contains circuitry so it will operate in a multiprocessor system. Since only one CPU is used, the bus request and bus grant signals are tied to the proper logic levels to ensure this board will have control over the SIB when required.

Bus Buffers They enhance the drive capabilities of the CPU. When enabled, they connect the CPU with the correct bus, these are: U48 and U49 for SIB data bus U45, U46 and U47 for SIB address bus U4 and U21 for local data bus U5, U6, U22 and U23 for local address bus

Decoders U36 decodes PA16-18 to enable ROM pairs 0-7. U19 decodes PA14-16 to enable RAM pairs 0 and 1, interrupt latch, and counter timer chip.

CPU This chip is a Motorola 68000 microprocessor running at 8 MHz. Main characteristics are, 16-bit data bus, 23-bit address bus, and 3 interrupt lines. At initial power up condition, power on reset (POR) insures the CPU will start-up in a known condition. The CPU will then run several routines, some of which are: determine which board type is in which slot, system self-diagnostics, and setup display information. The CPU will now respond to system interrupts, HP-IB, keyboard, or RPG. To the CPU all boards connected to the SIB look like memory locations. When A23 is a logic high level, the CPU is accessing system memory over the SIB. When A23 is a zero, then the CPU is accessing local processor board memory locations. After the CPU sends data over the SIB, LDTACK returns from the addressed board and signals the CPU the information was received. LDTACK also goes to the I/O board and resets a buserror timer. If the buserror timer is not reset, BUSERR is sent to the CPU. The CPU will display a SOFTWARE ERROR message on the CRT.

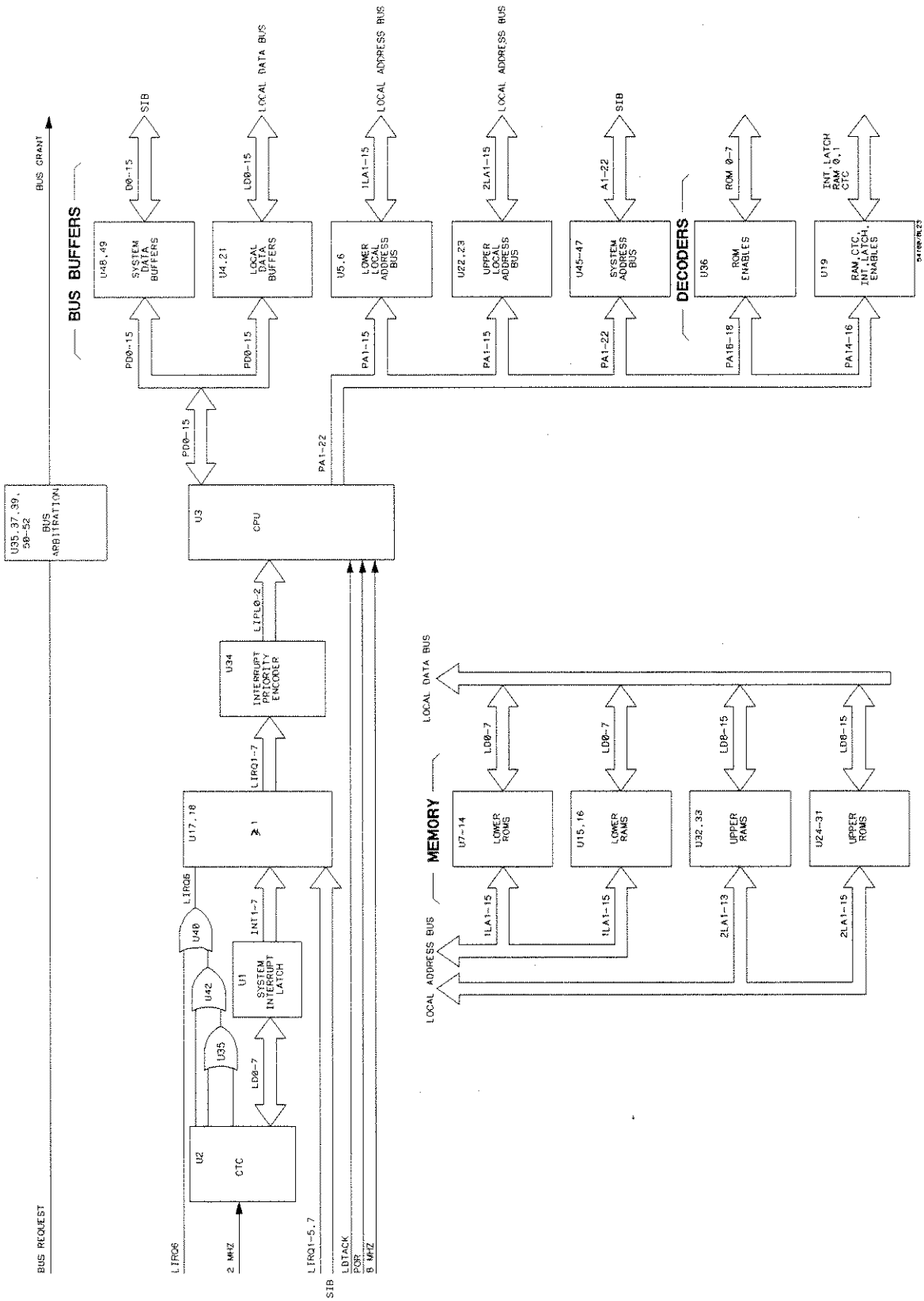


Figure 6B-5. Microprocessor Assembly Block Diagram

Memory

The ROMs and RAMs have 8-bit data lines. The 16-bit words are divided into a lower portion LD0-7, and an upper portion LD8-15. All the ROMs or RAMs are read in pairs. Software instructions for the CPU are contained in ROM memory. There is space for eight ROM pairs, but not all of the space is used. Non-volatile battery backed-up RAM memory contains stack registers, status registers, scratch pad memory, and soft-cal information.

Mnemonics	Definition
CPU	Central Processing Unit
CTC	Counter Timer Chip
LD0-15	Local Data lines 0-15
LDTACK	Low Data Acknowledge
LIRQ1-7	Low Interrupt Request lines 1-7
PA1-22	Microprocessor Address lines 1-22
PD0-15	Microprocessor Data lines 0-15
POR	Power On Reset
SIB	System Interface Bus
1LA1-15	Lower Local Address lines 1-15
2LA1-15	Upper Local Address lines 1-15

Color Display Assembly

This theory refers to figure 6B-6. The board is the interface between the host microprocessor and color monitor. It has graphics memory, timing generator, character generator, prioritizing circuitry, color map, and color output DACs.

Function Decoder

It decodes HA13-15 to enable various board functions, CRTC for the CRT controller, ID for board type, COLOR MAP for the color map and output DACs, priority for RAM.

D Latch

This circuit outputs LDTACK over the SIB indicating data was received from the CPU.

Slot Decode

The CPU accesses this board by sending out the board's slot ID code over address lines A19-22. U141 is a four bit comparator which compares slot address lines A19-22 with slot ID codes ID0-3. When the two codes are equal, U141 pin 6 enables other circuitry.

CRT Controller

The CRT controller controls several board functions, timing signals for the color monitor, blanking, horizontal drive, vertical drive, and character control functions.

Character RAM

Characters are stored in RAM as a 16-bit word, eight bits for an ASCII word and eight bits for character attributes.

Bit Number	Function	Bit Number	Function
TD0-6	ASCII character	TD10	Underline
TD7	Not used	TD11-14	Color
TD8	Inverse video	TD15	Priority bit
TD9	Blink		

Character ROM

It functions as a character generator by decoding ASCII data, TD0-7, from character RAMs and sending it through character shift registers to the encode circuit.

Character Shift Registers

They are parallel loaded with character data and output character video in serial format.

Attribute Logic

It converts TD8-15 to attributes, four bits for color and four bits for other attributes. To define these bits, refer to the table under Character RAM heading discussed earlier.

Dual Port Arbiter

The dual port arbiter outputs addresses from either the host CPU or from an outside controller and places graphics on the CRT.

Display Address Counters

These are 4-bit counters which generate graphic address lines GA0-13.

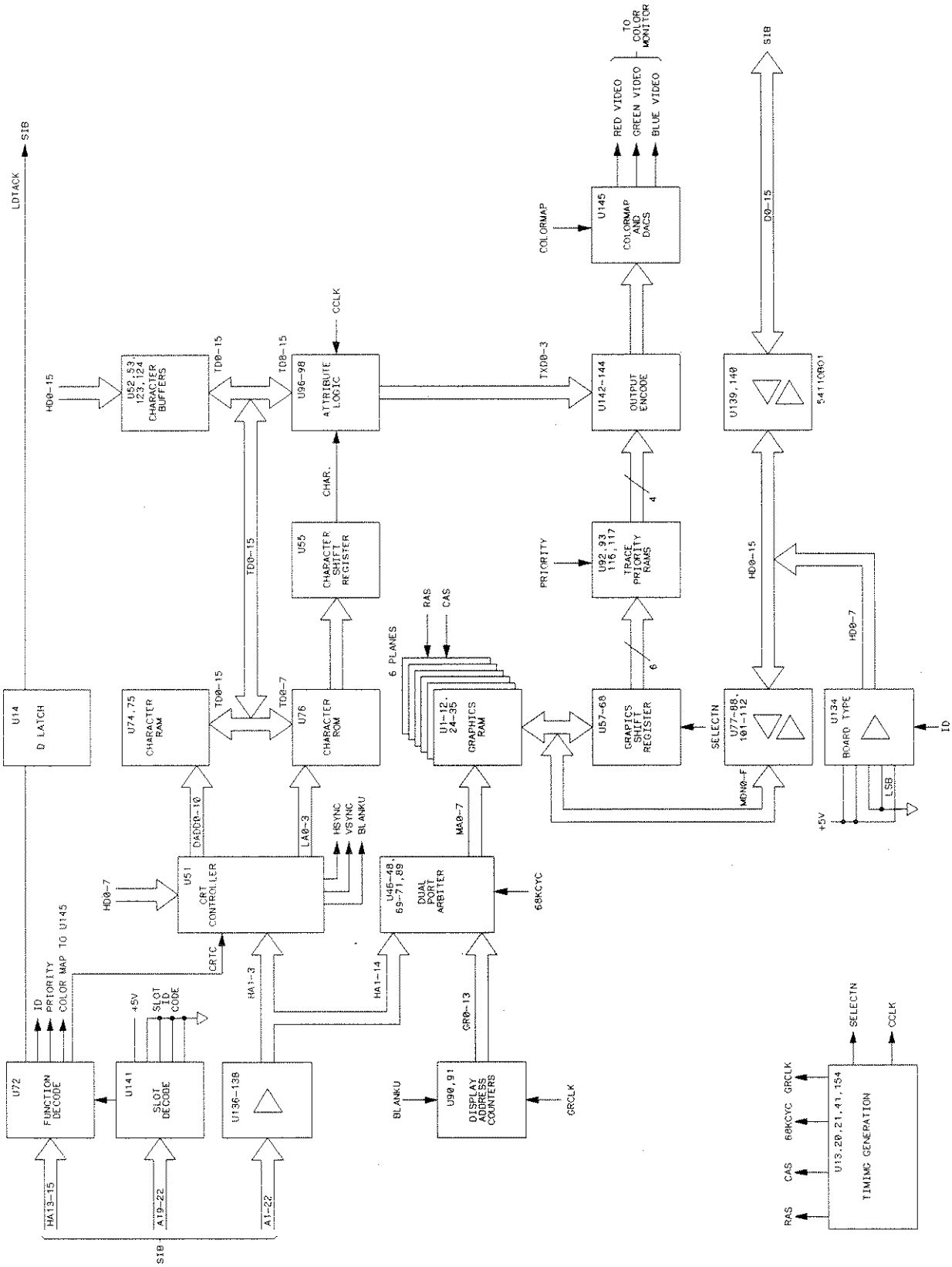


Figure 6B-6. Color Display Assembly Block Diagram

Graphics RAM

There are six planes of dynamic memory where graphics data is stored.

Plane	Information	Plane	Information
0	Graticules	3	Channel 2
1	Stored Traces	4	Channel 3
2	Channel 1	5	Channel 4

Graphics Shift Registers

This circuit is parallel loaded with graphics data and it serially outputs graphics video.

Trace Priority Encode

This is a high speed RAM whose function is to map outputs from the graphics planes into unique address locations for the color map. It also provides arbitration when more than one plane tries to illuminate the same pixel location. Plane 0 has the lowest priority while the other places have equal priority.

Output Encode

This circuit uses either graphics data or character and attribute data to generate addresses for the color map.

Color Map And Output DAC

The color map consists of three color RAMs which convert the encoded addresses to a digital value. There is one output DAC for each color RAM. The output DACs convert this digital value to red, green, or blue levels for the color monitor.

Board ID

When board type is requested by the CPU, this board will respond with 25 over the LD0-7 lines. LD0, 3 and 4 will be pulled high through U134, LD1 and LD2 will be pulled low through U134. LD0 is the least significant bit so adding LD0, 3 and 4 equals 25.

Timing Generation

Timing generation controls timing functions for the display board.

Mnemonics	Definition
A1-22	SIB Address lines 1-22
CAS 0-5	Column Address Strobe lines 0-5
CCLK	Character Clock
D0-15	SIB Data lines 0-15
DADD0-13	Display Address lines 0-13
DP0-5	Display Planes 0-5
GA0-13	Graphics Address lines 0-13
GRCLK	Graphics Clock
HA1-22	Local Address lines 1-22
HD0-15	Local Data lines 0-15
HIP21	High Priority bit 21 (Disables Graphics)
HSYNC	Horizontal Sync
LDS	Lower Data Strobe
LDTACK	Low Data Acknowledge
MA0-7	Memory Address lines 0-7
MD0-15	Memory Data lines 0-15
RAS 0-5	Row Address Strobe lines 0-5
SIB	System Interface Bus
TD0-15	Text and Attribute lines to character ROM
TXD0-3	Text and Attribute lines to encode circuitry
UDS	Upper Data Strobe
VSYNC	Vertical Sync

Power Supply Assemblies

This theory refers to figure 6B-7.

Primary Supply

The primary supply rectifies and filters the input ac voltage. When the voltage select switch is in the 230 V position, the ac is bridge rectified and filtered to yield approximately 300 V dc and 120 V dc. The 120 V dc is generated by an isolating switching regulator, and is used to power the color monitor. The 300V dc is used for the digital and analog supplies. The input voltage is doubled in the 115 V position to yield the same dc voltages. The primary board has surge protection circuitry that protects against ac line voltage transients and current surges. Over-voltage crowbar devices trip the circuit breaker for sustained input over-voltage conditions. The pulse width modulator (PWM) circuitry is powered by a bleeder resistor on one of the bulk storage capacitors. The main EMI (electromagnetic interference) filter is located in a dc current path to reduce component size and to increase the filter's effectiveness.

Digital Supply

The digital power supply is a dc to dc converter which converts 300 V dc to +5 V and -5.2 V dc. The Pulse Width Modulator (PWM) Is used to achieve voltage and current regulation by changing the PWM's turn-on time. It has an operating frequency of 68 kHz. The Power Stage performs the actual conversion of 300 V dc to +5 V and -5.2 V dc. Digital and primary ground planes are kept isolated through transformer T2. The Optical Isolators are used to isolate the primary and digital ground planes. Voltage and current feedback control is sent through U2 to control the duty cycle of the PWM. Power supply shutdown is sent by U3. The Loop Control and Supervisory circuitry detects when excessive output voltage occurs. It sets a latch in the PWM which can only be reset by cycling the circuit breaker off for 60 seconds, or an instantaneous reset by cycling the front panel power switch. It also senses the current and activates foldback current limiting for excessive current loading.

Analog Supply

The analog power supply is a dc-to-dc converter which converts 300 V dc to ±18 Vdc and ±8 Vdc. The Pulse Width Modulator (PWM) is used to achieve voltage and current regulation by changing the PWM's turn on time. It has an operating frequency of 68 kHz. The Power Stage performs the actual conversion of 300 V dc to ±18 Vdc and ±8 Vdc. There is a fan drive output that increases fan speed with ambient temperature. Analog and primary ground planes are kept isolated through transformer T2. The Optical Isolators are used to isolate the primary and analog ground planes. Voltage and current feedback control is sent through U2, to control the duty cycle of the PWM. Power supply shutdown is sent through U3. The Loop Control and Supervisory circuitry detects when excessive over-voltage occurs. It sets a latch in the PWM which can only be reset instantaneously by cycling the front panel power switch to standby and then to on, or by turning the circuit breaker to the off position for 60 seconds. +18 V is regulated and the other outputs are semi-regulated outputs which follow the +18 V. Each output is current-limited. The -8 V output has foldback current limiting.

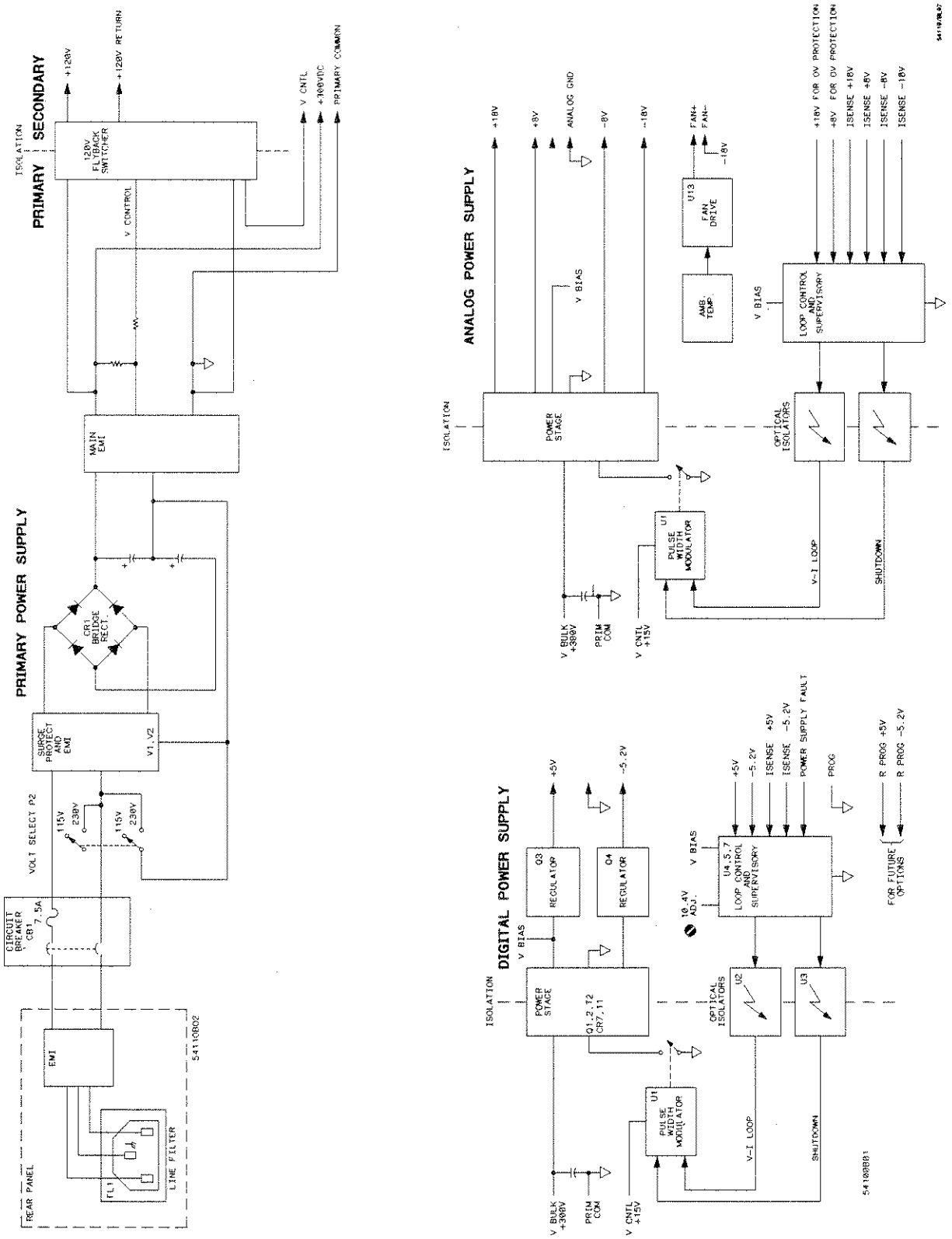


Figure 6B-7. Power Supply Assembly Block Diagrams

Table Of Contents

Service Menus

Service Menus 6C

Introduction

This section describes the service menus and keys that are available for calibration, troubleshooting, and CRT display alignment. A basic understanding of these will be helpful in troubleshooting failures. However, Self-Test and Troubleshooting is covered specifically in Section 6D.

Service Menus

The service menus are part of the Utility menu, in the second level of the menu softkeys. Pressing the **Utility** key will display five other function keys: Cal Menu, Test Menu, CRT Setup, Color Cal Menu, HP-IB Menu.

CAL Menu

The Cal Menu is used to calibrate the instrument. The calibration factors are stored in non-volatile memory. Use of this menu is covered in the "Front Panel Operation Reference". Basic functions of the Cal menus are covered in this section.

Test Menu

The Test Menu provides several functions used to set up and run internal diagnostics test and view the results. Use of these functions is covered briefly in this section and comprehensively in the Self-Tests/Troubleshooting, section 6D.

CRT Setup

The CRT Setup Menu provides several functions that provide confidence testing as well as test patterns for adjusting the Color CRT Module. These functions are discussed in this section.

Color Cal Menu

The Color Cal Menu provides functions used to set the characteristics of the colors displayed. These characteristics include hue, saturation, and luminosity. This menu is covered in detail in the "Front Panel Operation Reference.

HP-IB Menu

The HP-IB Menu provides keys that are used to set the HP-IB attributes. These attributes are address number, Talk/Listen, and EOI. This menu is discussed in detail in the "Front Panel Operation Reference".

One-key Power Up

A one-key power up is performed to return the instrument to a known (default) front panel condition. This is done as follows:

1. Set the front panel POWER switch to STBY.
2. Press and hold any front panel key.
3. Turn front panel POWER switch to ON.
4. Release key when display shows "Powerup Self Test Passed!" or "Failed".

Two-key Power Up

A two-key power up is a basic reset of the entire operating system of the HP 54120B. All volatile and non-volatile RAM is cleared. As a result, all calibration factors are purged, front panel setups are erased, and the instrument must be recalibrated.

Caution

Using the two-key powerup will leave the instrument in an uncalibrated state. Effort needed for recalibration should be considered before using this mode to reset the instrument.

1. Set the front panel POWER switch to STBY.
2. Press and hold the top and bottom function keys.
3. Turn front panel POWER switch to ON.
4. Release keys when display shows "Powerup Self Test Passed!" or "Failed".

Cal Menu

Channel Vertical Cal

Channel Vertical Cal sets software calibration factors to correct for sampler gain and offset errors. The calibration is run by pressing the appropriate menu and function keys. All front panel inputs must be disconnected from the instrument. Refer to the specifications under general information in the test set service manual for a recommended cal interval.

Channel Skew Cals

The channel skew calibration is a user calibration which minimizes the delays between channels and also the external trigger input. If this calibration is performed in a calibration facility, use cables and signals similar to what the user will use with the oscilloscope.

Channel Atten Cals

This key only appears when the HP 54122A Four Channel Test Set is connected to the HP 54120B. The calibration measures the actual attenuation of the step attenuators and performs a software compensation. After a two-key power up, this calibration should be performed to ensure the correct values are stored. A very accurate dc source is required.

Test Menu

Five sub-menus are available when the Test Menu is selected. The menus allow the user to access and run internal diagnostics and view the results. In addition, the position of each card cage printed circuit board can be read and displayed, and the firmware revision date is displayed. Use of the test menus is covered in depth in section 6D, Troubleshooting.

Note

The top key toggles between REPEAT LOOP and RUN FROM LOOP. These keys in conjunction with Loop Number = [0-43] and the Start/Stop Test key will execute internal self-test diagnostic routines. All input signals must be disconnected from the instrument for these tests.

Repeat Loop

Selecting this mode will continuously execute the Loop number entered at RUN FROM LOOP. Pressing **Start Test** will start execution and the loop will continuously run until the **Stop Test** key is pressed. Pressing **Display Errors** will show how many times the loop was executed and the number of times the loop failed.

There are a number of loops that will blank or over-write the Stop Test key display on the CRT. However, the test can still be terminated by pressing the third function key from the top.

Run From Loop

Selecting this mode will start execution from the loop entered and will proceed to execute all higher numbered loops. Upon reaching the last test, the cycle will be repeated.

If any test should fail, the instrument will change from RUN FROM LOOP to REPEAT LOOP and will repeatedly execute the loop that failed until the **Stop Test** key is pressed.

Extended Tests

When this key is chosen there are 13 internal instrument tests that may be selected by entering the test number with the entry devices. These tests are numbered 0 through 12. All input signals must be disconnected from the instrument for these tests. Many of the extended tests are useful only at the factory. Those that are of use to field service personnel are covered in section 6D, troubleshooting.

Start/Stop Test

This key is used to initiate any test where a test number is entered by one of the entry devices. Once the test number is entered, pressing **Start Test** initiates the test and the key toggles to Stop Test. Pressing **Stop Test** stops the test in progress and the key toggles back to Start Test.

There are a number of tests that will blank or over-write the Stop Test key display on the CRT. However, the test can still be terminated by pressing the third function key from the top.

Display Errors

Pressing the **Display Errors** key will display the number of any loops which failed. The tests which test for loop failures are: Powerup self test, EXTENDED tests, REPEAT and RUN FROM LOOP tests, and HP-IB commanded self test. This display shows the current loop or last loop executed, the number of times the loop was executed, and the number of times that it failed. The bottom portion of the display shows all loops that failed starting with the first loop failure. These are cummulative failures and they are erased only on power up or I/O assembly reset.

The four STATUS X = XXXXX lines in the Display Errors field are primarily for factory use. Any field usable information in this part of the display is covered in section 6D, troubleshooting. To return to the Test Menu, press **Exit Display** key.

Display Configuration

Most of the assemblies used in the mainframe have circuitry that allows them to be interrogated directly by the microprocessor. The exception being the microprocessor assembly. The mainframe card cage has 9 slots, but only four assemblies are in the card cage. When the **Display Configuration** key is pressed the resulting display shows the location of the card cage assemblies, except the microprocessor. The display assembly is shown as being in slot 14, this is not part of the card cage but is on the instrument's bottom side. The firmware revision date is also displayed. To return to the Test Menu, press **Exit Display** key.

CRT Setup Menu

When CRT Setup Menu is selected, four keys are displayed that allow access to CRT setup displays. The keys available are, from top to bottom, Confidence Test, Pattern Off, Light Output Off, Color Purity Off, and at the bottom, Exit CRT Setup Menu.

Even though some of the patterns overwrite the key display, the functions can be selected. The bottom key can be pressed at any time to exit the CRT Setup Menu.

Confidence Test

When this function is selected, the confidence test pattern is displayed. The pattern consists of three parts. At the top is a complete character set, in the center is a group of seven color blocks, and at the bottom a seven block grey-scale.

The top four lines of the character set display include the complete character set. The bottom line displays three sets of numerals. The first set is displayed in inverse video, the second set, and the third set is normal video and underlined.

The seven color blocks displayed at the center are, from left to right; beige, grey, red, yellow, green, amber, and cyan.

Note

Since color perception is subjective, any slight variation in colors from what is described here should be disregarded.

At the bottom of the CRT a seven block grey-scale is displayed, with increasing luminosity from left to right. This grey-scale display is used if Color CRT Module adjustments are necessary.

Pattern

These patterns are used when Color CRT Module adjustments are necessary. When CRT Setup Menu is selected, this key is initially Pattern Off.

Pressing **Pattern Off** once will display a white cross-hatch pattern over the entire CRT and the Pattern Off key changes to Pattern White. Inside the cross-hatch pattern there are dots at the center, corners, and at the 12, 3, 6 and 9 o'clock positions. Additionally, there are test matrices in the center and corners.

Pressing **Pattern White** key changes the pattern color to red and the key label changes to "Pattern Red". Repeatedly pressing this key will change the color of the pattern to green then blue. The name of the Pattern key is the color displayed.

Pressing **Pattern Blue** key changes the display to the white cross- hatch pattern on the top half of the CRT and white with a dark cross- hatch on the bottom. The key then changes to Pattern HV Reg. This test is used primarily by the factory, however, it may indicate the need for service if there are severe high voltage problems.

Pressing **Pattern HV Reg** changes the display to a solid white screen with dark cross hatch lines. The key changes to Pattern I White. Successive pressing of this key changes the color to red, green and then blue, the name of the Pattern key is again the color of the display.

Pressing **Pattern I Blue** changes the display to a white cross-hatch pattern with the inside flashing between solid white and cross-hatch. The key changes to Pattern Bounce. This test is primarily used by the factory, however, it may indicate the need for service if there are severe high voltage problems.

Pressing **Pattern Bounce** exits this set of tests and returns the CRT Setup Menu.

Light Output

These displays are used by the factory.

Pressing **Light Output White** displays a horizontal band of white half the height of the display. The key display is not overwritten. Repeatedly pressing this key will change the color of this band to red, green, blue and then a grey-scale. Each time the key is pressed it also changes to the appropriate description.

Pressing **Light Output Grey-Scale** exits this set of tests and returns the CRT Setup Menu.

Color Purity

Pressing **Color Purity Off** displays a full white raster. Repeatedly pressing this key changes the color of the raster to red, green and then blue. At each color display the name of the key changes to the appropriate description. These displays are used when Color CRT Module adjustments are necessary.

Pressing **Color Purity Blue** exits this set of tests and returns the CRT Setup Menu.

Table of Contents

Troubleshooting

Troubleshooting 6D

Introduction

This section contains troubleshooting information for fault location to the PC assembly level for the HP 54120B. Reading sections 6B, theory of operation, and 6C, service menu keys, will help in understanding this section.

Safety Considerations

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

Warning

This instrument is equipped with a standby switch on the front panel that DOES NOT de-energize the power supply. To avoid shock hazards capable of causing injury or death, the main power switch on the rear panel must be used to de-energize the instrument or the power cable must be disconnected when the instrument must be de-energized.

Warning

Maintenance described in this section is performed with power supplied to the instrument and with protective covers removed. Maintenance should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the power should be removed. Read the Safety Summary in the front of this manual.

Caution

Do not remove or replace any of the circuit board assemblies in this instrument unless instrument power is removed. The assemblies contain components which may be damaged if they are removed or replaced when instrument power is applied.

Recommended Test Equipment

Equipment recommended for service is listed in table 1-1. Any equipment that satisfies the critical specifications stated in the table may be substituted.

Logic Family Used

The logic level used on the HP 54120B Mainframe is TTL. TTL ranges from approximately 0 V to 5 V.

Diagnostic Overview

Start all diagnostics by first verifing the failure mode. Then follow the main troubleshooting flowchart, figure 6D-1, to determine if the failure is in the mainframe or data acquisition system. The flowchart covers the mainframe system troubleshooting (CPU, I/O, power supplies, keyboards and display system). Sometimes this section will refer to particular paragraphs in the four channel test set service manual. For data acquisition failures refer to the four channel test set service manual for these troubleshooting procedures.

One Key-down Power Up

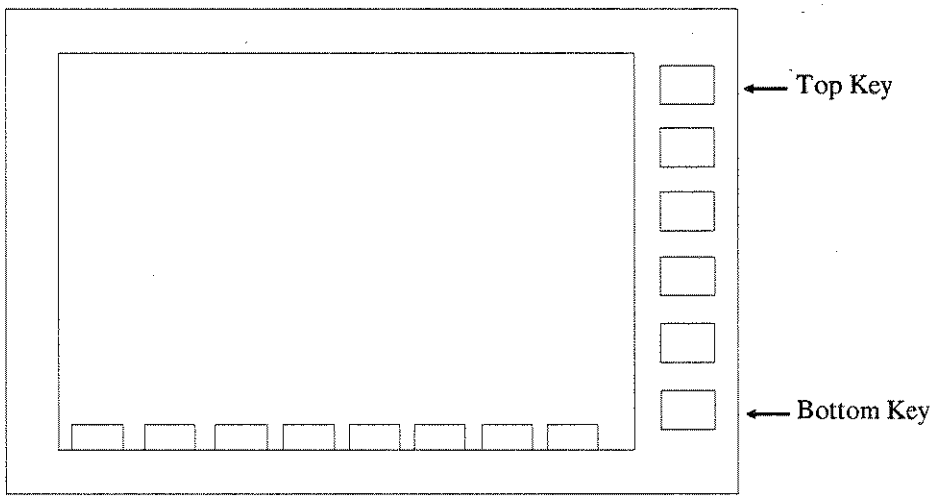
A one key-down power up places the instrument in a default condition. This default condition is identical to sending an HP-IB "RESET" over the bus. This allows users a known starting point to begin their test procedures from. Hold down any key while cycling the oscilloscope's power off and on. Continue to hold the key down until graticules are displayed on the screen.

Two Key-down Power Up

A two key-down power up sets up the instrument identical to a one key-down power up. It also clears all the RAM memory locations, resets all digital storage devices, clears vertical software calibration factors, and clears the channel to channel skew factors (clears channel attenuation cal factors in HP 54122T).

1. Turn oscilloscope's power switch to STBY.
2. Hold down the top and bottom function keys on the screen's rightside.
3. Turn oscilloscope's power switch to ON and continue holding function keys down until graticule display is on screen.
4. Ignore "Front Panel Cals Lost" warnings on top of screen, CALs will be performed later.

Keys to Hold down for two key-down powerup



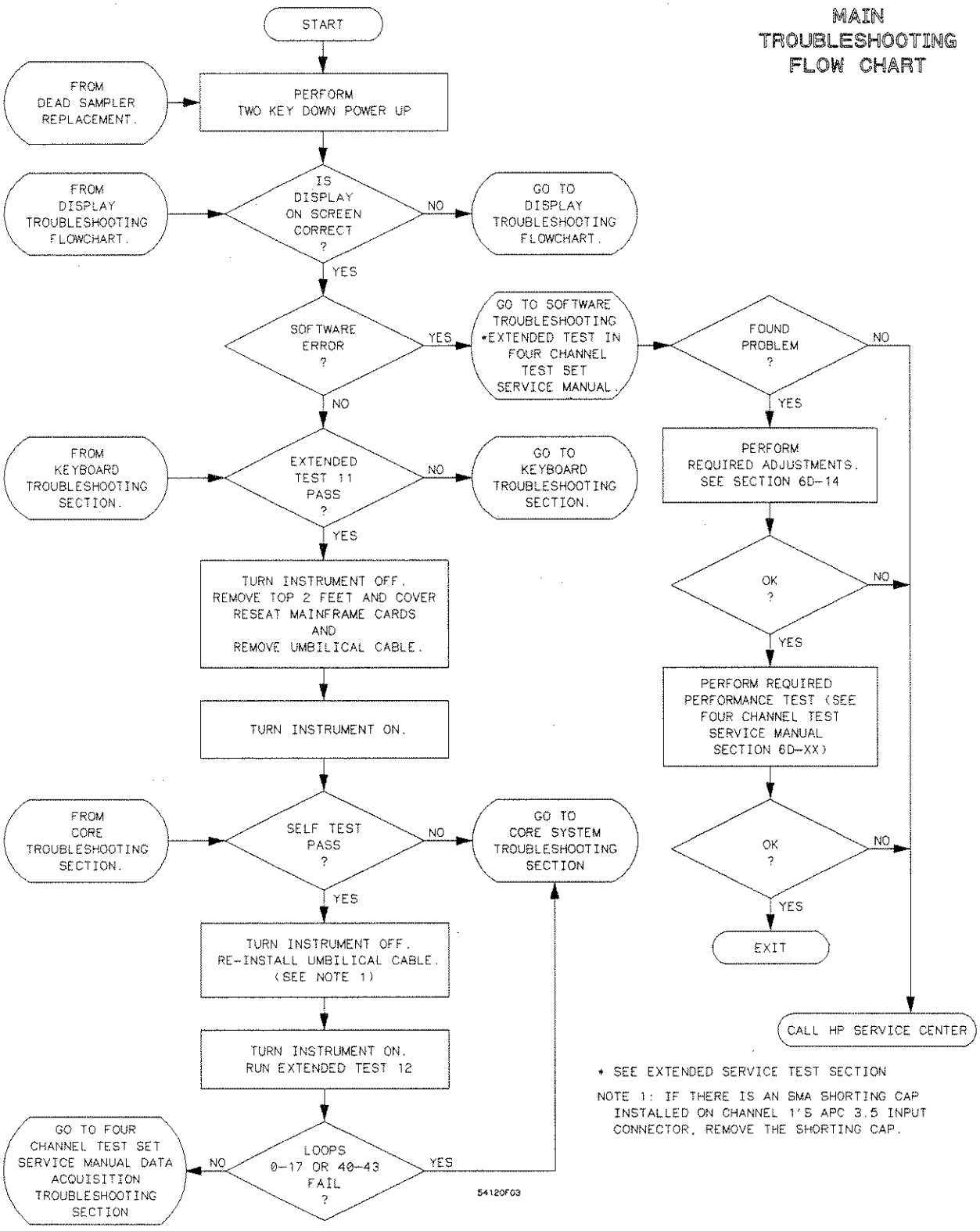


Figure 6D-1. Main Troubleshooting Flowchart

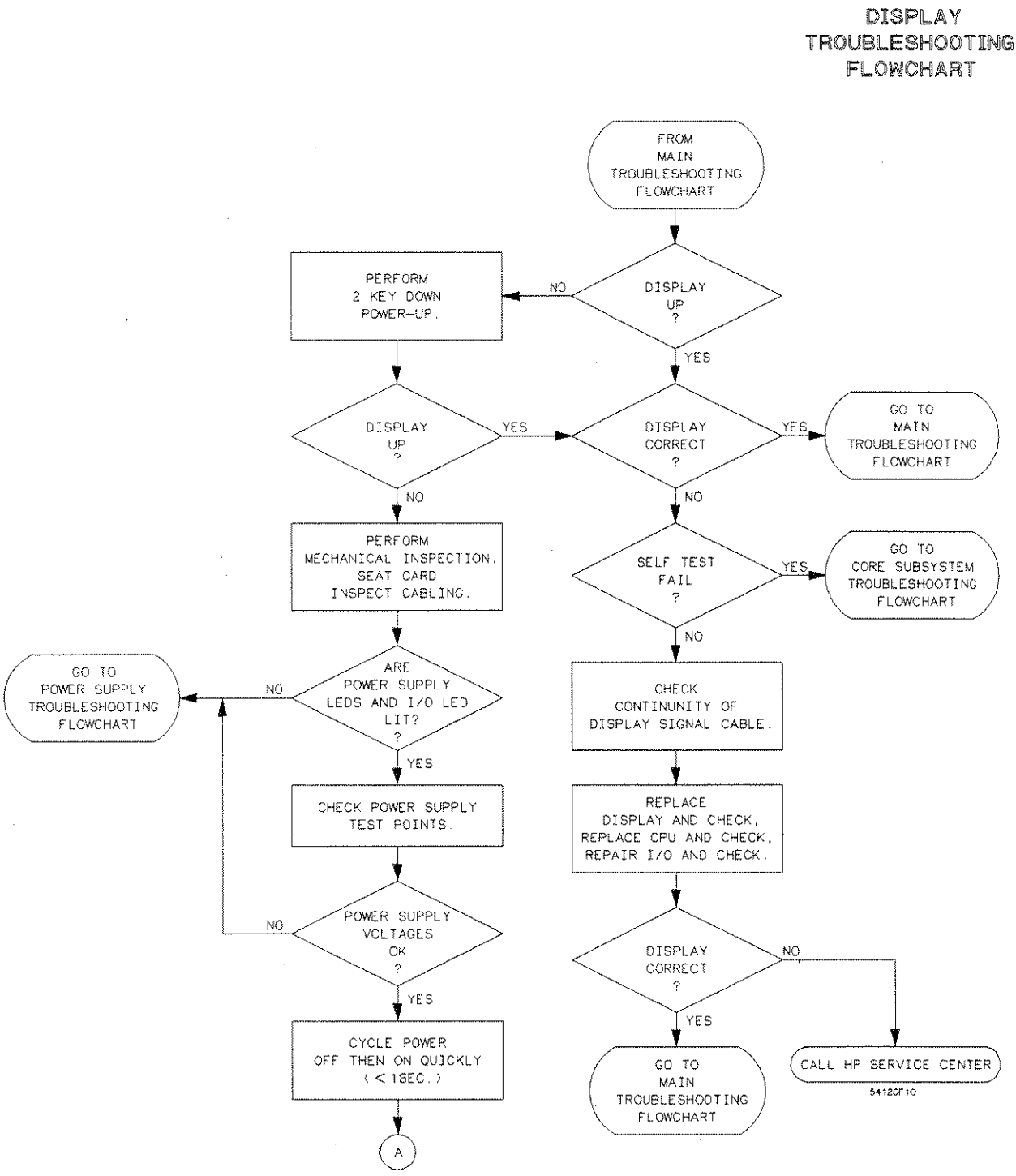


Figure 6D-2. Display Troubleshooting Flowchart Part 1

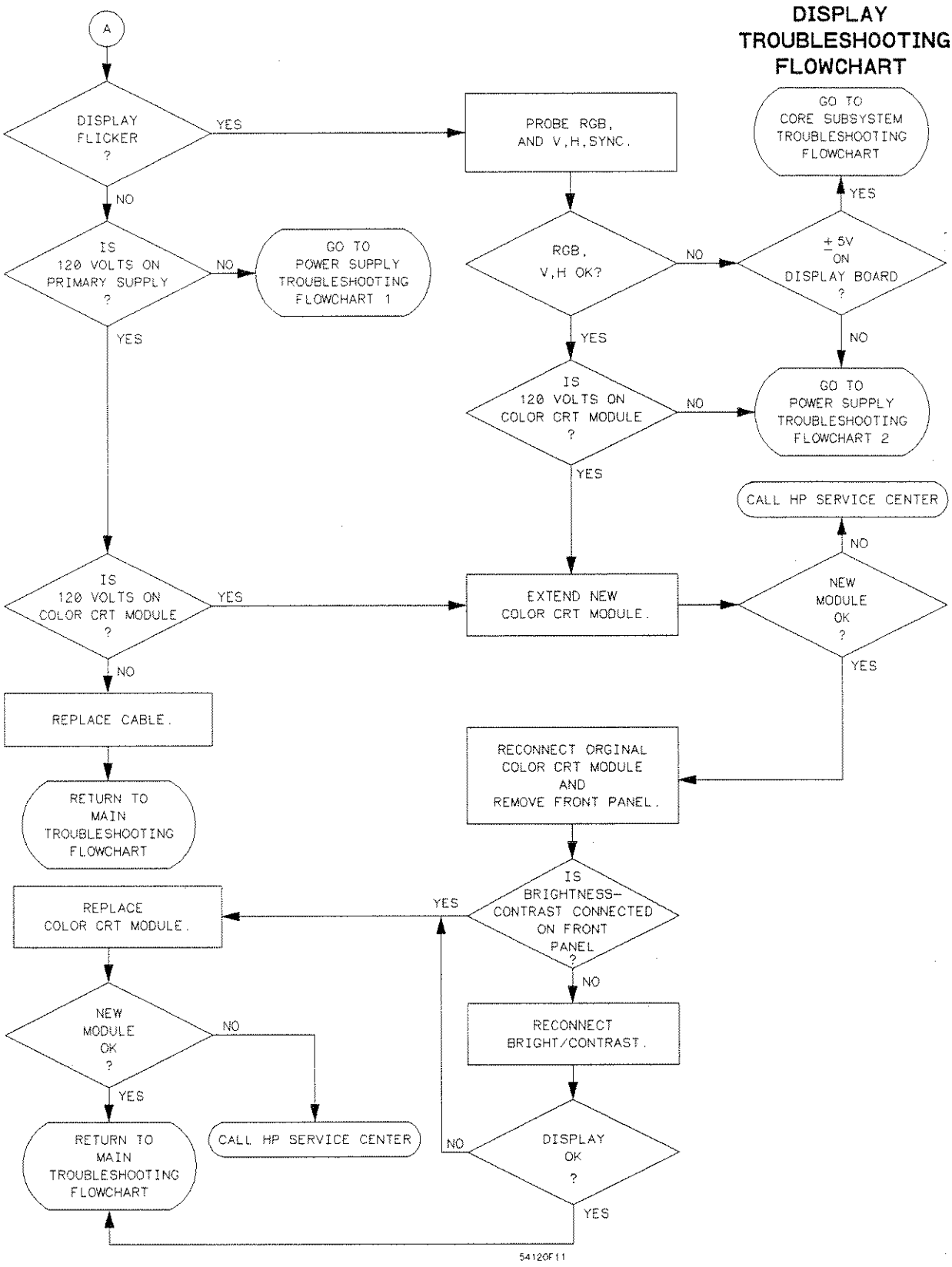


Figure 6D-3. Display Troubleshooting Flowchart Part 2

I/O Assembly Hard Reset

This reset is similar to powering the instrument off and on, except the power supplies are not lowered to 0 V. This reset is useful as a convenient method for resetting the instrument with the top cover removed. It can also be a good troubleshooting aid when there may be a failure with the instrument's normal power up routine.

Anytime the instrument has a power up problem it may help isolate the problem by trying the I/O assembly hard reset. Especially if the instrument has intermittent power up problems.

Keyboard Troubleshooting

Troubleshooting the keyboard uses flow diagram figure 6D-6 to isolate the faulty assembly to the I/O assembly, control keyboard, RPG, function keyboard, menu keyboard, or three interconnecting ribbon cables. Table 6D-2 describes what type signals are on the ribbon cables and figure 6D-5 is the cable's pin descriptions. Table 6D-1 describes which cable row and scan lines are used when the front panel keys are pressed. The softkey name assignments change with the different menu selections. Figure 6D-4 illustrates a numbering scheme for these softkeys.

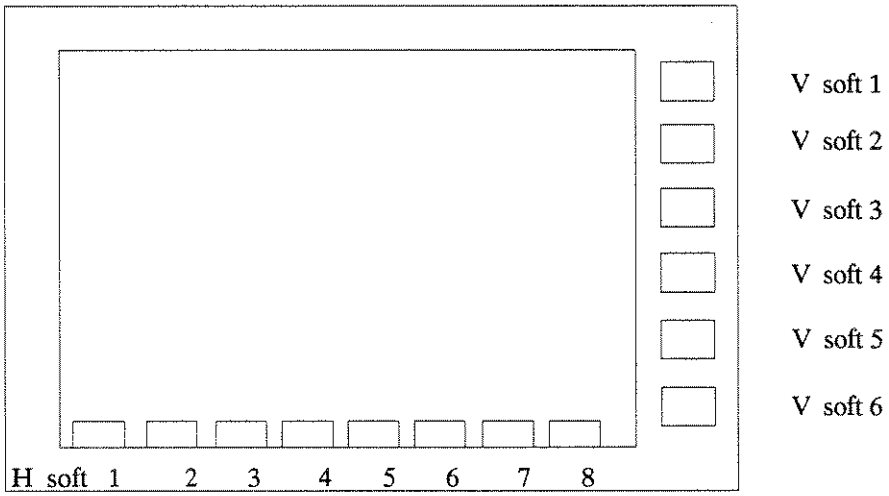


Figure 6D-4. Softkey Number Assignments

Table 6D-1. Row and Column Key Assignments

	SC0	SC1	SC2	SC3	SC4	SC5	SC6	SC7
RL0	H soft 1	H soft 7	Sec/Volt	0	8	Clear	Autoscale	↑ →
RL1	H soft 2	H soft 8	msec/mV	1	9	Run		← ↓
RL2	H soft 3	V soft 6	µs/µV	2		Stop/Single		
RL3	H soft 4	V soft 5	ns	3		Save		
RL4	H soft 5	V soft 4	ps	4		Recall		
RL5	H soft 6	V soft 3		5		Local		
RL6		V soft 2		6				
RL7		V soft 1		7				

Table 6D-2. Keyboard Ribbon Cable Signal Description

Pin Description	Cable Pin No.	I/O Bd Pin No.	Signal
SC0	6	U12 pin 15	195 Hz, 60 mV to 2.8 V, 87% duty cycle, each slightly shifted in phase
SC1	5	U12 pin 14	
SC2	8	U12 pin 13	
SC3	7	U12 pin 12	
SC4	10	U12 pin 11	
SC5	9	U12 pin 10	
SC6	12	U12 pin 9	
SC7	11	U12 pin 7	
RL0	24	U21 pin 38	Single shot when present
RL1	26	U21 pin 39	
RL2	28	U21 pin 1	
RL3	30	U21 pin 2	
RL4	23	U21 pin 5	
RL5	25	U21 pin 6	
RL6	27	U21 pin 7	
RL7	29	U21 pin 8	
RPG	17	U34 pin 2	
RPG	18	U13 pin 12	
Not Used	13	U40 pin 3	
Not Used	16	U39 pin 6	
Not Used	14	U28 pin 11	
+5 V	1-4	U20 pin 13	+5 V
Not Used	33, 34		
DGND	15, 21, 22		0 V
DGND	31, 32		0 V
Not Used	19		
Not Used	20		

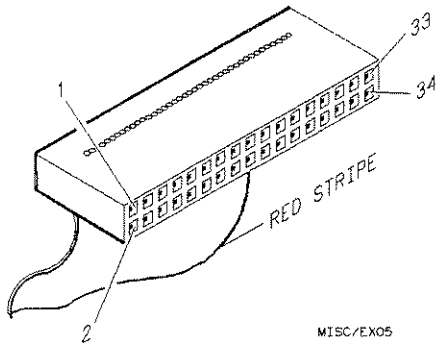


Figure 6D-5. Keyboard Cable Pin Numbers

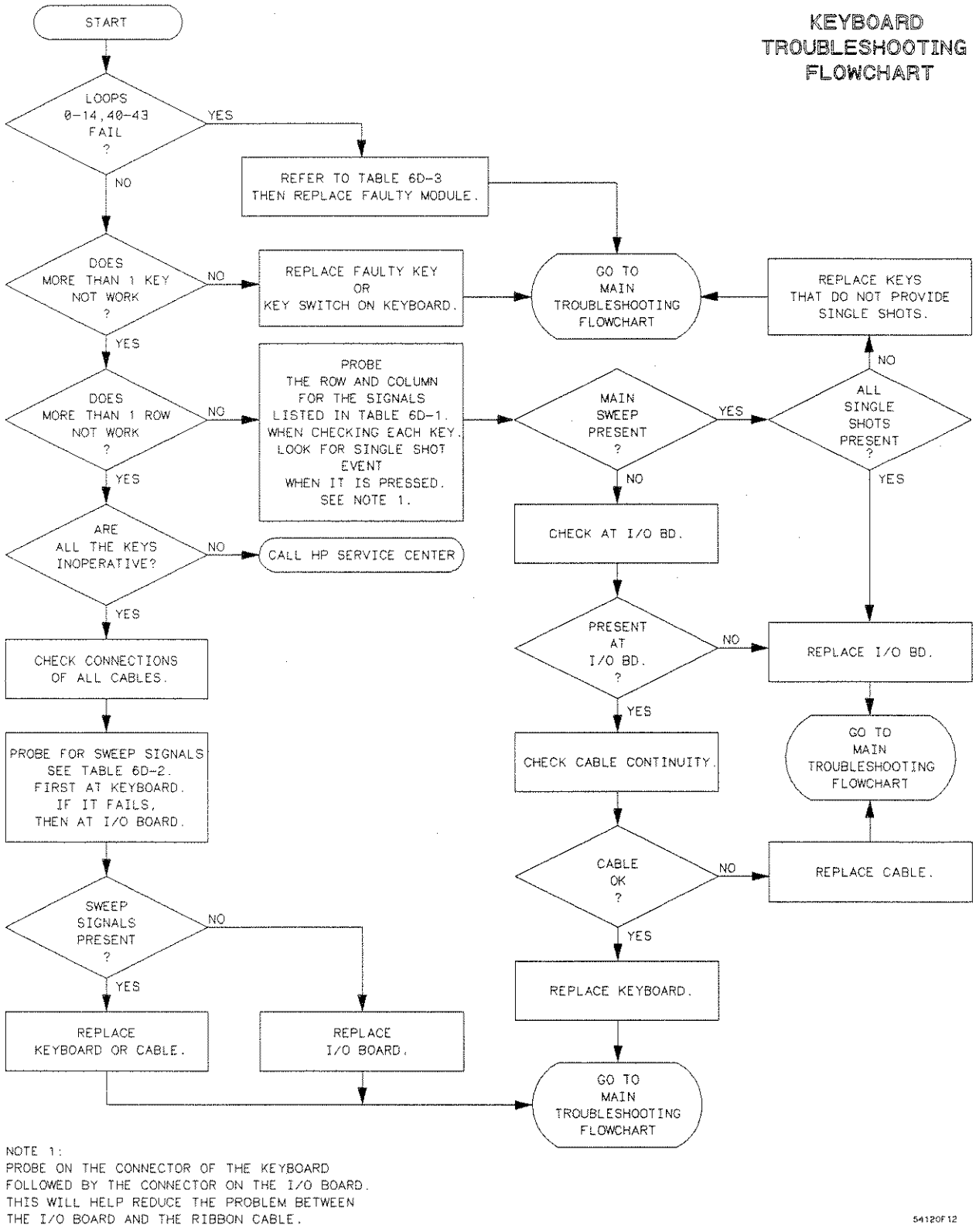


Figure 6D-6. Keyboard Troubleshooting Flowchart

Core Subsystem Troubleshooting

There are two core subsystem troubleshooting methods. If the loop test information is on the screen, use table 6D-3. If the display or keyboard systems are locked up, use figure 6D-7.

It is preferable to get the HP 54120B to pass all the Core Tests before going on to fix more complex loops. Occasionally, bent motherboard pins or defects in other system elements will cause these loops to fail. Make a system of the microprocessor assembly, I/O assembly and one other assembly. It is than possible to determine which socket or assembly may be causing an interaction that causes one of the core loops to fail. Using this technique, seat each assembly into the motherboard one at a time. Be sure to turn the power off before raising or seating an assembly into the motherboard.

If only the microprocessor and I/O assemblies are seated, the system will go into a repeating multicolored routine with about a two second cycle. This is useful in certain troubleshooting situations but no loop error information will be available.

Table 6D-3. Core Subsystem Diagnostic Routines

Test Loop	**Probable Failing Assembly**
0-4	Microprocessor Assembly
5-9	Display Assembly
10-15	I/O Assembly
40	Microprocessor Assembly
41, 42	Display assembly
43	I/O Assembly

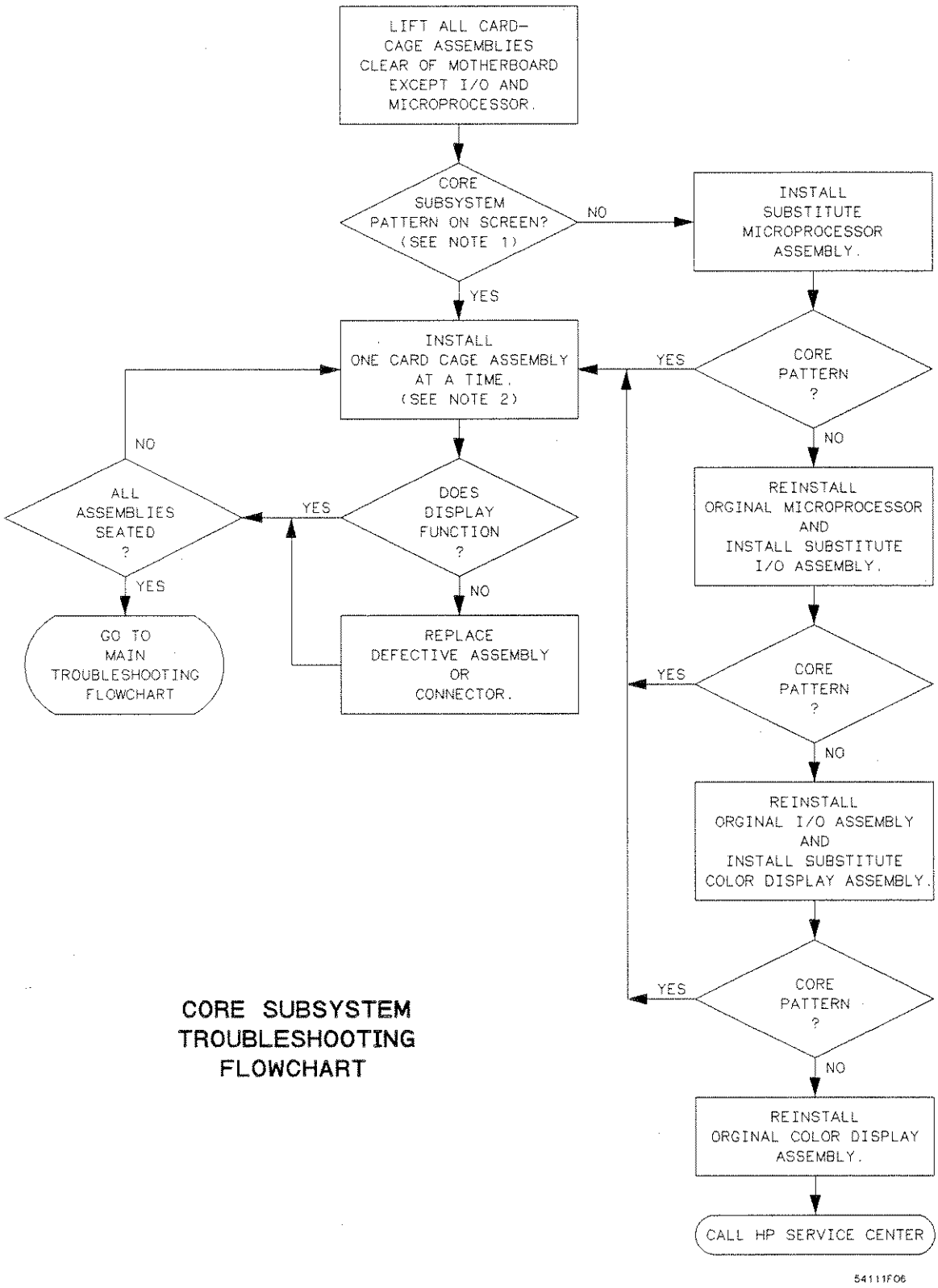
Power Supply Troubleshooting

When a power supply problem is suspected, it is first important to make sure that no unusual load is keeping the supply in a current limited condition. Table 6D-4 indicates which supplies are used on each assembly. Start the power supply troubleshooting with figure 6D-8.

Table 6D-4. Power Supply Distrubution

	+120 V	+18 V	+8 V	+5 V	-5 V	-8 V	-18 V
Microprocessor				*			
Input/Outout †		*	*	*	*	*	*
Horizontal Control		*	*	*		*	*
ADC Assembly		*	*	*		*	*
Color Display				*			
Color CRT Module	*						
To Test Set							
From ADC		*					*
From Horizontal		*	*			*	*

† Only the +5 V is used for power. The other supplies connect for power test only and are high impedance points; the likelihood of loading these supplies is low.



CORE SUBSYSTEM TROUBLESHOOTING FLOWCHART

Figure 6D-7. Core Subsystem Troubleshooting Flowchart

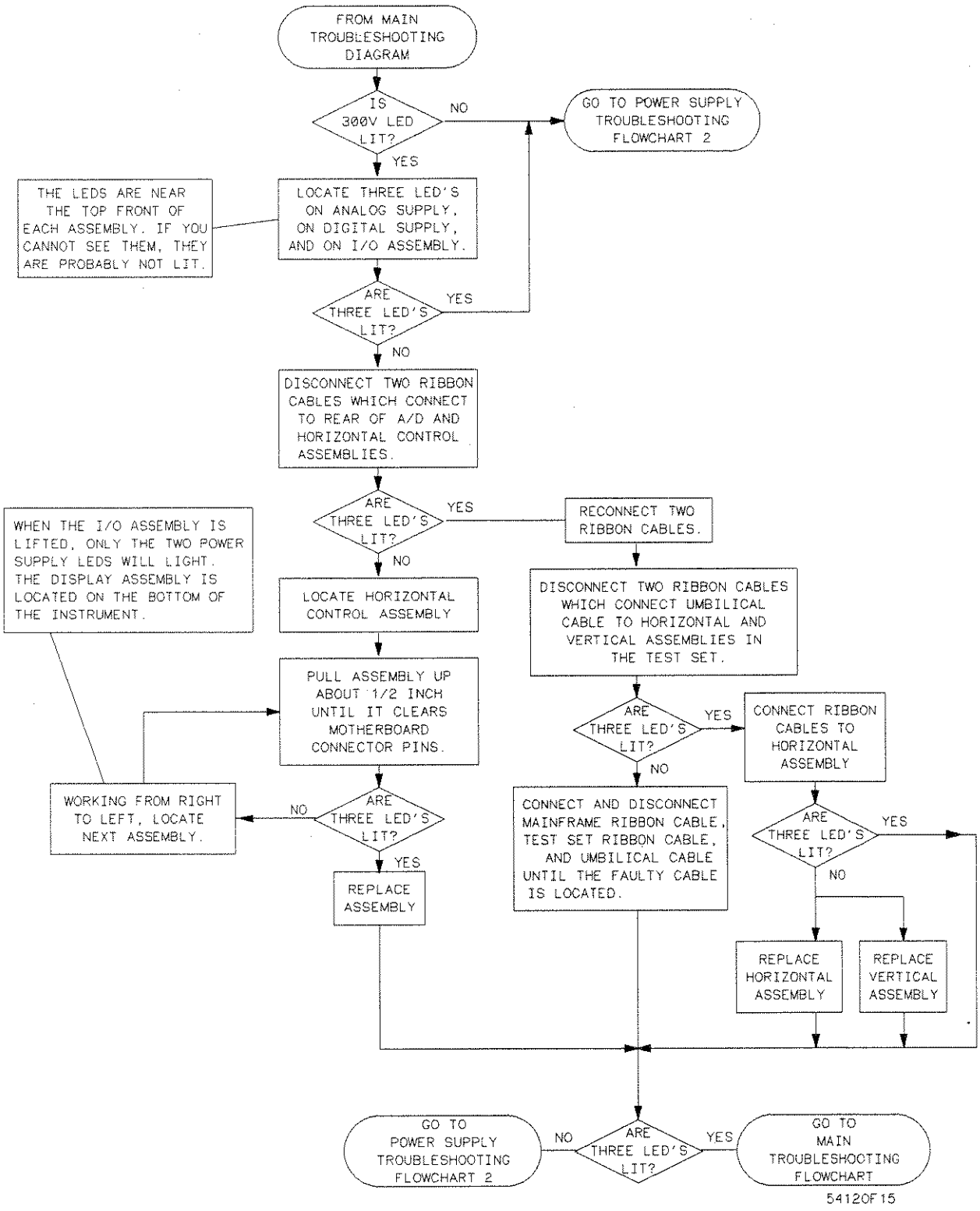
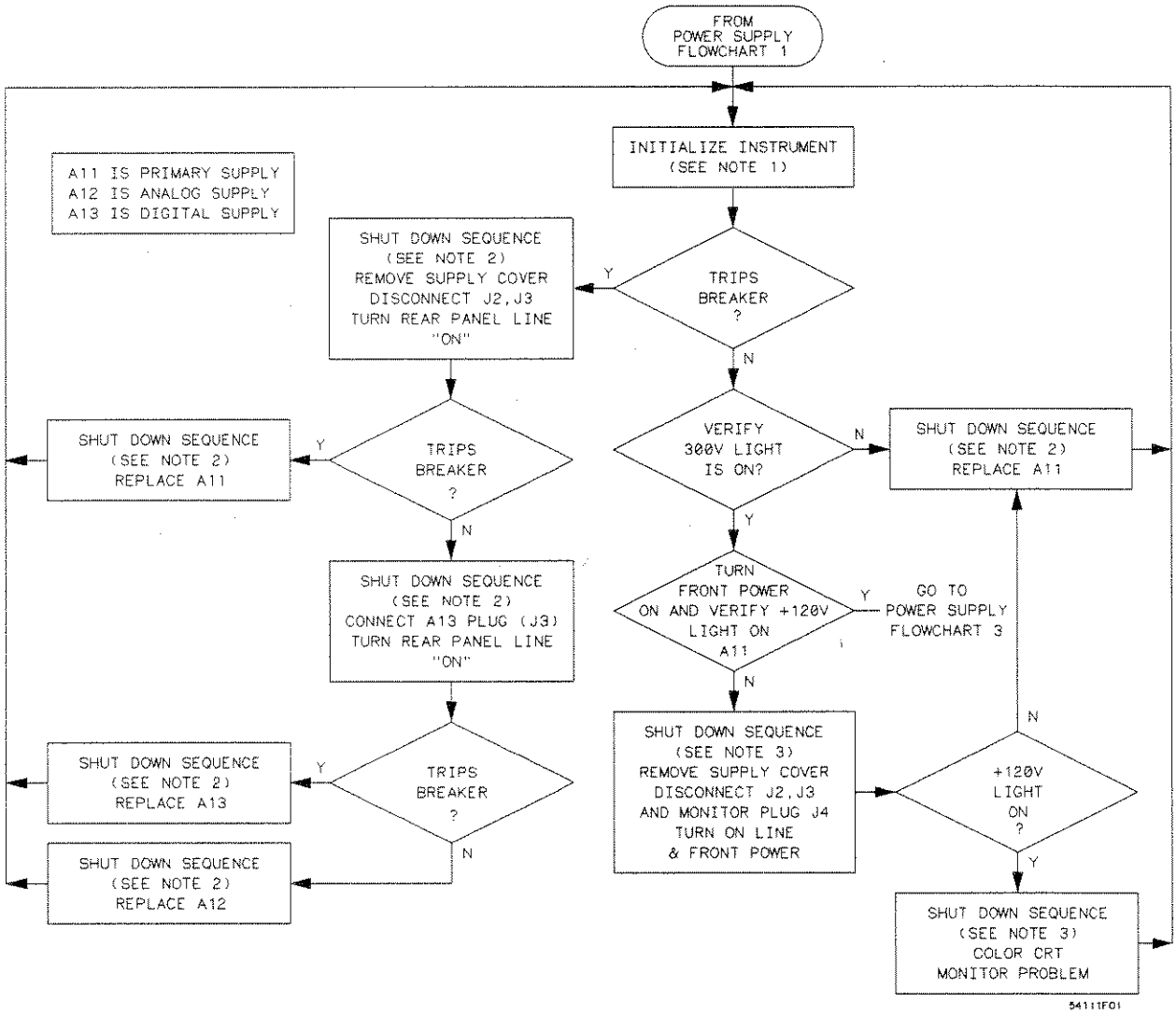


Figure 6D-8. Power Supply Troubleshooting Flowchart 1



Notes for Flowchart 2

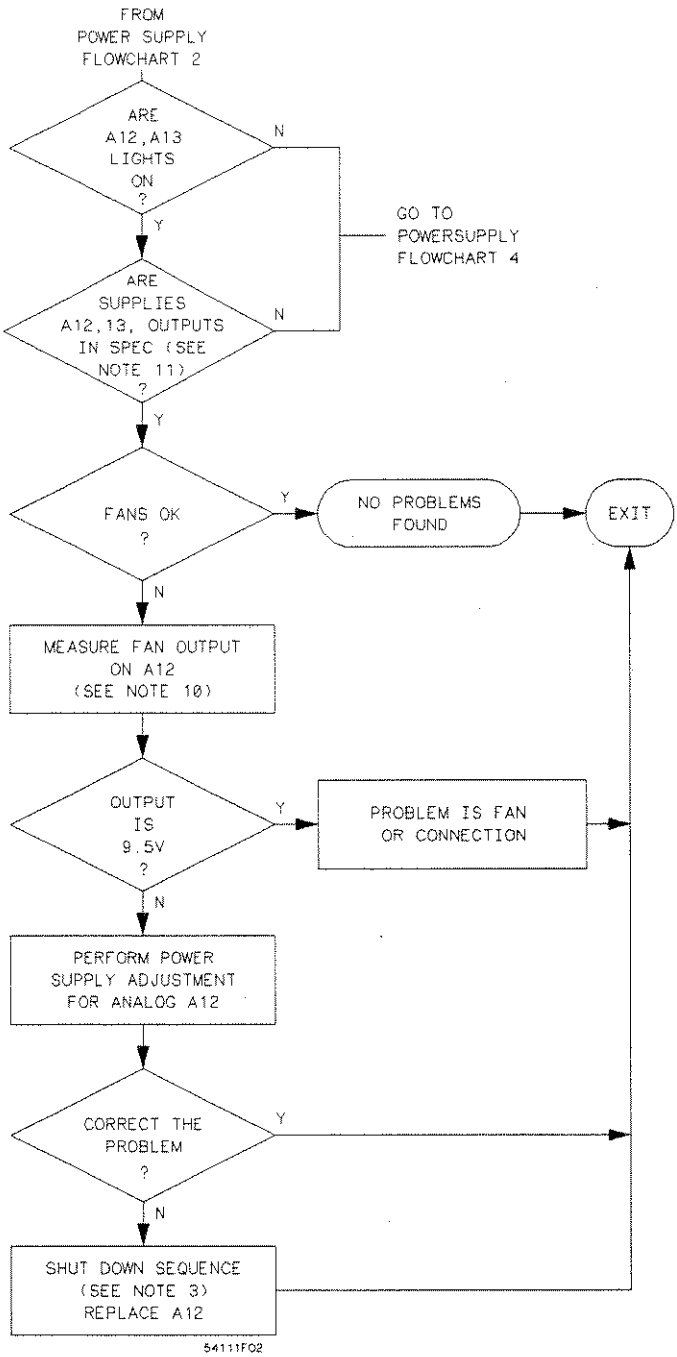
1) A. Turn front panel power switch to standby
   B. Rear panel line switch should be OFF "0"
   C. Connect AC power source
   D. Turn rear panel line switch to ON "1"

2) A. Turn rear panel line switch to OFF "0"
   B. Always unplug AC power source
   C. CAUTION!!! Wait until +300 V light is completely off (about 3 minutes) before proceeding; shock hazard exists and you can cause damage to the instrument

3) A. Turn rear panel switch to standby
   B. Turn rear panel line switch to OFF "0"
   C. Always unplus AC power source
   D. CAUTION!!! Wait until +300 V light is completely off (about 3 minutes) before proceeding; shock hazard exists and you can cause damage to the instrument

Warning
Extreme caution must be taken when removing power supply cover

Figure 6D-9. Power Supply Troubleshooting Flowchart 2



A11 is Primary Supply
A12 is Analog Supply
A13 is Digital Supply

Notes For Flowchart 3

3) A. Turn front panel switch to standby
   B. Turn rear panel line switch to OFF "0"
   C. Always unplug AC power source
   D. **CAUTION!!! Wait until + 300 V ligh is completely off (about 3 minutes) before proceeding; shock hazard exists and you can cause damage to the instrument!!!**

10) Connect the voltmeter (+) lead to the "FAN" test point and the (-) lead to the -18 V test point. The reading should be 9.5 V. This voltage will increase with increasing ambient temperature. See the power supply adjustment procedure for the analog supply.

11) For power supply test points and specifications see table below.

Digital Supply Test Points (+) Lead	(-) Lead	**Voltage**
+5 V	GND	+5.10 V ±0.1 V
-5 V	GND	-5.30 V ±0.1 V
+14B	GND	+5 V
Analog Supply Test Points (+) Lead	(-) Lead	**Voltage**
+18 V	GND	+18.5 V ±0.3 V
+8 V	GND	+8.9 V ±1 V
-8 V	GND	-8.5 V ±1 V
-18 V	GND	-18.5 V ±0.3 V
FAN	-18 V	+9.5 V ±0.3 V
+26B	GND	+5 V

Figure 6D-10. Power Supply Troubleshooting Flowchart 3

Notes For Flowchart 4

3) Turn front panel switch to standby
Turn rear panel line switch to off "0"
Always unplug ac power source

Caution

Wait until +300 V light is completely off (about three minutes) before proceeding; shock hazard exists and you can cause damage to the instrument.

4) The nominal output for +14B is 21V. However, when the supply is operating in the current limit mode, it can be as low as +5 V. The nominal output for +26B is 26 V. It can also be as low as +5 V when in current limit.

5) Measure ±5 V on the digital power supply. If both outputs are ≤ half the normal output, then use the yes path. Otherwise, use the no path.

6) When the supply or supplies are running in the current mode this may mean that an external load is pulling down the supply output(s). An external load could be a board in the card cage or the color display assembly (not the color crt module). the only way to isolate the color display assembly is to completely remove it from the mainframe. The fans can also put the analog board into the current mode. You can disconnect the fans by removing the bottom cover and disconnecting the fan cable.

To isolate a current problem, first disconnect the test set, then remove one load at a time until the problem is found. Problems could include bent pins on the motherboard or a bad component on a PC assembly. Refer to table 6D-4 for power distribution to the various assemblies.

7) Measure ±18 V and ±8 V on the analog supply. If both outputs are ≤ half the normal output, then use the yes path. Otherwise use the no path.

8) The test points to measure +14.6 V are at the back of the board close to the top. Connect the voltmeter common lead to the "COM" test on the board.

Caution

Use caution when measuring this voltage. It is not isolated from the line (mains) input and the primary supply is exposed with the power supply cover removed.

9) By removing the connectors at J2 and J3 you are checking if either the analog or digital supply is loading VCNTL.

Caution

The top pin on connectors J2 and J3 is VBULK which is +300 V. The pins below are VCNTL, then ground.

To measure VCNTL, turn the power off and make sure the +300 V lamp (near top of board) is off. Connect the voltmeter (+) lead to VCNTL (second pin from top) and the (-) lead to ground (bottom pin). Apply power and observe the meter reading. With one supply connected the reading should be about +25 V and with neither connected about +42 V. Turn off power and ensure +300 V LED is off before removing the voltmeter leads.

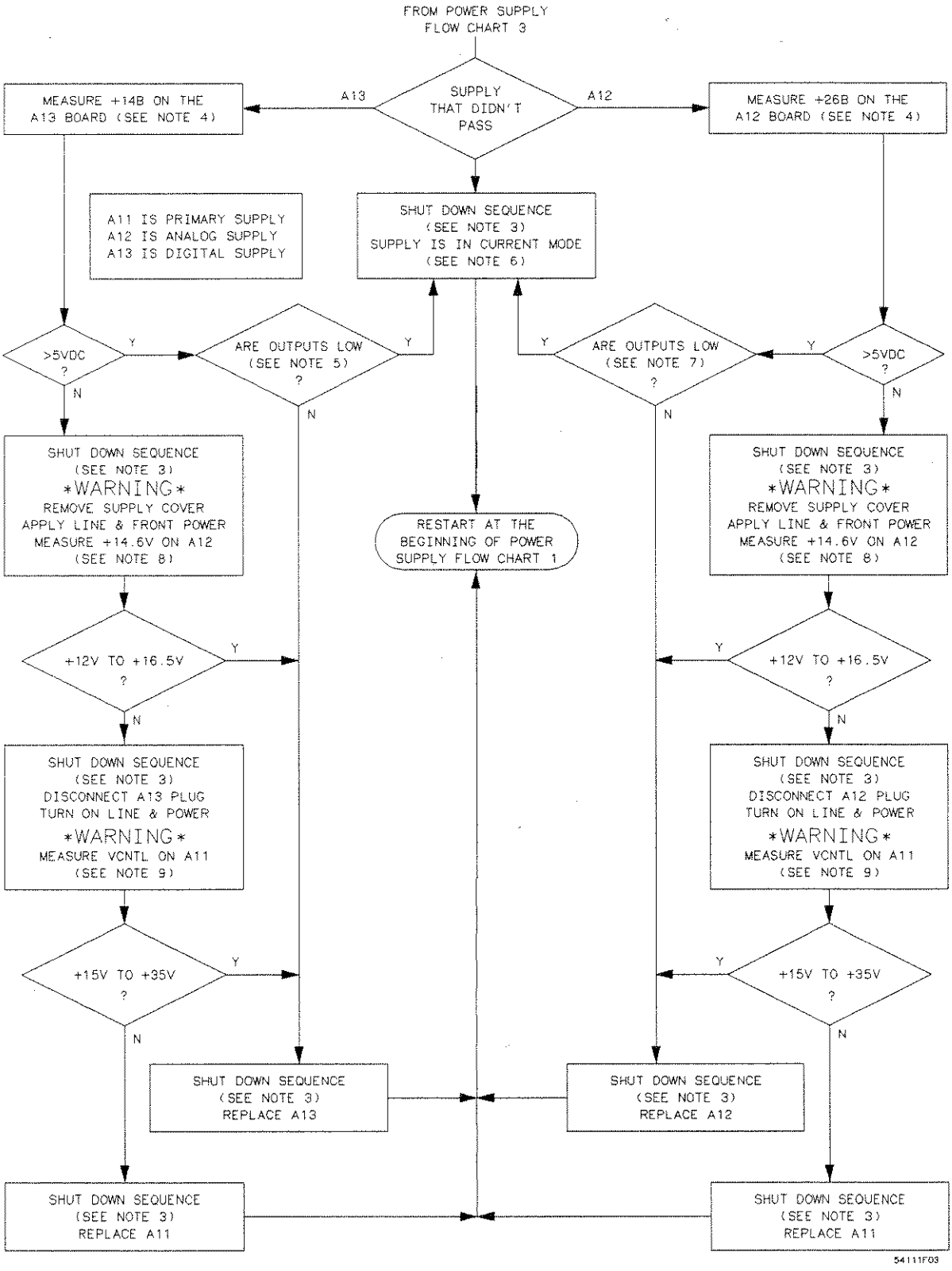


Figure 6D-11. Power Supply Troubleshooting Flowchart 4

Color Monitor Troubleshooting

This test determines if the color monitor is faulty by checking horizontal sync pulses (HSYNC), vertical sync pulses (VSYNC), and color pulses (RGB) at the color monitor's input connector.

1. Turn mainframe's power switch to STBY.
2. Remove the mainframe's top and bottom covers.
3. Turn the mainframe's power switch to ON.
   Check the +120 V at the module power connector. Refer to figure 6D-12. The correct voltage should be between +118 V and +122 V. If the +120 V supply is incorrect, refer to the power supply troubleshooting procedure.

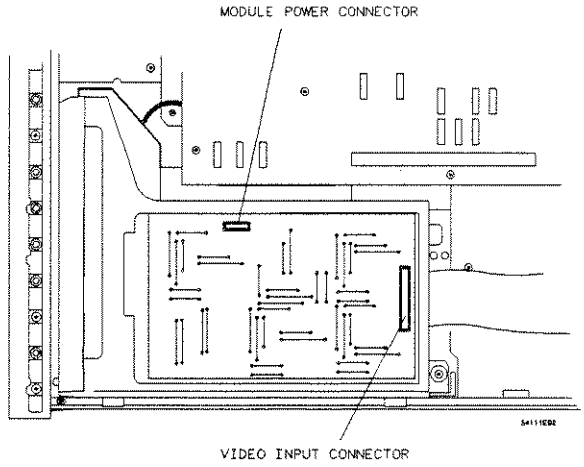
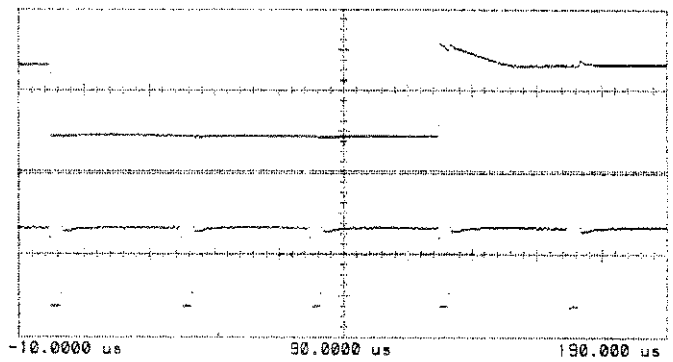


Figure 6D-12. Color CRT Module Input Connections

4. Move the clear plastic shield on the bottom of color CRT module by pushing it rearward until it clears the front frame. Hinge the clear plastic shield away from the board.
5. Connect 10:1 divider probes to monitor oscilloscope. Connect channel 1 to vertical sync test point, pin 3 of video input connector. Connect channel 2 to horizontal sync test point, pin 7 of video input connector. The vertical and horizontal sync pulses are TTL levels and should resemble figure 6D-13.

Vertical Sync Waveform

Horizontal Sync Waveform



Channel 1 = 2.000 V/div
Offset = 2.500 V

Channel 2 = 2.000 V/div
Offset = 2.500 V

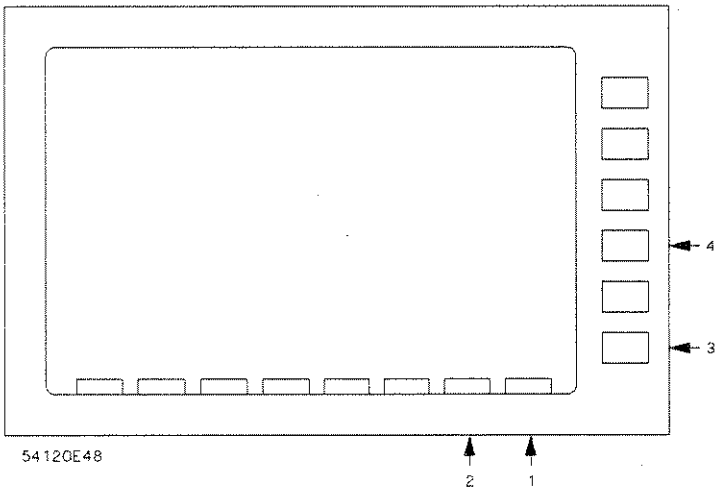
Timebase = 20 µs/div
Delay = 90.0000 µs

Trigger Mode: Edge
On Neg. Edge on Channel 1
Channel 1 level = 2.300 V

Figure 6D-13. Vertical and Horizontal Sync. Waveforms

6. Before checking the video waveforms, try to get a known display on screen. If the display is operating, press the **More, Utility, CRT Setup** menu, and **Color Purity** keys. This will place a white raster on screen which means all video signals will be at maximum levels. If there is no display, try to get the same signals by pressing the following softkeys.

In Bottom Row Press:	**In Vertical Column Press:**
1. Key at extreme right	3. Key at bottom
2. Key second from right	4. Key third from bottom



7. Probe the following points. The video signals have a 0 V baseline and will vary in amplitude from 0 V to approximately 600 mV, depending on the characteristics of the colors displayed.

Video Signal	**Video Input Connector**
red	21
green	29
blue	37

8. The video signals can be loaded down by the color CRT module's input circuits. If the video signals were bad in step 8, disconnect the cable from the video input connector and recheck the signals on the color display assembly.

Video Signal	**J2 on Display Assembly**
red	14
green	18
blue	22
Sync Signals	**On Display Assembly**
Vert. sync	V.Sync TP
Horz. sysn	H.Sync TP

9. If the video signals are now good, replace the color CRT module.

Color CRT Module Troubleshooting

It is time consuming to remove a suspected faulty color CRT module from the instrument. This test connects a good color CRT module outside the instrument without having to remove the suspected faulty monitor. This requires the use of parts from the HP 54100 family product support kit.

Warning

Chassis ground on the color CRT module will be disconnected from the chassis ground of the instrument. This will leave the color CRT module chassis ground floating. Therefore, use an alligator clip lead to connect the monitor's chassis ground to the instrument's chassis ground.

1. Turn mainframe's power switch to STBY and remove power cable.
2. Remove mainframe's top and bottom covers.
3. Disconnect color CRT module power cable from primary power supply.
4. Connect a replacement power cable (54110-61601) from the product support kit to the primary power supply.
5. On instrument's bottom side, disconnect the wide ribbon cable from the suspected faulty color CRT module and extend it away from the instrument.
6. Place the known good color CRT module next to the instrument.
7. Connect the wide ribbon cable to the working color CRT module.
8. On the working color CRT module's bottom PC board is a connector labeled B-4, connect the power cable (from step 4) to this connector.
9. On the working color CRT module's bottom PC board is a connector labeled B-2, connect a display control cable from the product support kit to this connector.
10. Connect the CRT brightness control from the product support kit to the other end of the display control cable.
11. Reconnect the power cord and turn the instrument on.
12. If the display is now operational, the suspected faulty color CRT module in the instrument is bad.

Firmware Troubleshooting

Some failures cause the keyboards to lock up and prevent you from entering the troubleshooting menus. This procedure isolates which assembly is causing the problem. After the problem is repaired, return to the flow diagram.

1. Perform two key-down powerup routine.

2. Turn mainframe's power switch to STBY and remove the horizontal and A/D assemblies from the mainframe. Remove the ribbon cables from the assemblies.

3. Turn mainframe on. If there is a graphics pattern (core troubleshooting pattern) repeated displayed, go to step 4; otherwise go to step 10.

4. Turn mainframe's power switch to STBY and install the horizontal control assembly in the mainframe. Do not connect the ribbon cable.

5. Turn the mainframe's power switch to ON. If the core troubleshooting pattern is displayed on screen and the keyboards and display are still functional, go to step 6; otherwise replace the horizontal control assembly and return to flow diagram.

6. Turn the instrument's power switch to STBY and install the A/D assembly in the mainframe. Do not connect the ribbon cable.

7. Turn mainframe on. If the keyboards and display are still functional, go to step 8; otherwise replace the A/D assembly and return to flow diagrams.

8. Turn the mainframe's power switch to STBY and connect the ribbon cable to the horizontal control assembly only.

9. Turn mainframe on. If the keyboards and display are still functional, go to step 9; otherwise continue with step 8's instructions. Disconnect umbilical cable from test set. If display and keyboards are still functional, replace the horizontal assembly in the test set and return to the flow diagram. Disconnect umbilical cable from the mainframe. If the display and keyboards are still functional replace the umbilical cable and return to the flow diagram; otherwise replace the ribbon cable.

10. Turn the mainframe's power switch to STBY and connect the ribbon cable to the A/D assembly only.

11. Turn mainframe on. If the keyboards and display are still functional, go to step 9; otherwise continue with step 9's instructions. Disconnect umbilical cable from test set. If display and keyboards are still functional, replace the vertical assembly in the test set and return to the flow diagram. Disconnect umbilical cable from the mainframe. If the display and keyboards are still functional replace the umbilical cable and return to the flow diagram; otherwise replace the ribbon cable.

12. Replace the following assemblies in order and check the core troubleshooting pattern each time: CPU assembly, display assembly, I/O.

13. Return to the flow diagram.

Additional Troubleshooting

Data acquisition and internal diagnostic troubleshooting is included in the four channel test set service manual.

Table of Contents

General Information A1

Safety and Handling Precautions

Precautions that apply generally to Hewlett-Packard equipment, including the HP 54007A Accessory Kit, are explained in the Safety Considerations page. The devices in the kit, however, are not mechanically, electrically, or chemically hazardous, so no special safety precautions are necessary.

Extreme care must be taken in handling and storing these devices to protect them from mechanical damage. This is especially true in making connections, in order to avoid damaging the connectors and to avoid damaging the HP 54120 system by electrostatic discharge (ESD). A detailed discussion of connection procedures appears later in this manual.

The devices in the HP 54007A Accessory Kit have very precise mechanical tolerances, some on the order of one ten-thousandth of an inch (a few microns). Therefore, rough handling of any kind must be avoided. Do not permit any of the devices to fall on any hard surface or come in contact with dirt, oils, or abrasives. The connectors must be clean and undamaged to ensure an accurate calibration.

The foam-lined storage case in which you receive the accessory kit is the best place to store the devices. Never store any of the devices loose, in a desk drawer, or place them contact-end down on a table top. The lid of the storage case is detachable and allows convenient storage, even in a shallow desk drawer.

Incoming Inspection

The foam-lined storage case provides enough protection for the accessory kit during shipping. If the case arrives in good condition, the devices are probably in good condition. If the case or devices appear to have been damaged, set aside the accessory kit and all packaging materials, contact the nearest Hewlett-Packard sales/support office.

Hewlett-Packard will arrange for repair or replacement of incomplete or damaged shipments without waiting for a settlement from the transportation company.

Equipment Required But Not Supplied

If you will be using SMA connectors in your calibrations or test setups, a precision connector gauge for measuring the contact pin locations of SMA connectors, as well as for connecting 3.5 mm precision connectors, is recommended. Please read the caution about SMA connectors (see Chapter 3 of this appendix, "Device Specifications"). Precision connector gauges for SMA connectors are available from Maury Microwave Corporation.

A few tools are required to make safe and repeatable connections with either the precision 3.5 mm connectors or SMA connectors.

- Torque wrench (optional) capable of 8 lb-in (90 N-cm) to install precision 3.5 mm devices to each other and the front panel connectors (HP part number 8710-1765).

- Torque wrench (optional) preset to 5 lb-in for mating SMA connectors to precision 3.5 mm connectors (HP part number 8710-1582).

All precision 3.5 mm connectors must be visually inspected before use and cleaned (or replaced) as needed. The following equipment is required for cleaning:

- An illuminated, 4-power magnifying glass for visual inspection of the connectors. The exact power of the glass is not critical, but the type of illumination is. Ordinary room lighting, or oblique lighting from a desk lamp casts shadows that can easily mask the small defects you are trying to see. Therefore, make sure that the magnifying glass has built-in lighting and provides axial, shadowless illumination. Illuminating magnifying glasses are available from most equipment suppliers. Hewlett-Packard does not sell or recommend any particular model.

- Compressed air in a pressurized can, HP part number 92193Y, can be used to blow dust and lint from the connectors. Any source of clean, dry, low-pressure air can be used if it has an effective oil-vapor filter and condensation trap placed just before the air outlet hose.

When using compressed air from a pressurized can, hold the can upright. If the can is tilted or inverted, the liquid propellant sprays out with the air. The propellant evaporates instantly on the connector surface and causes the connector to become too cold for the calibration to continue. If this happens, you must wait until thermal equilibrium is re-established within the allowable temperature range before continuing the calibration. Permanent connector damage from the propellant is unlikely.

- Liquid Freon (trichlorotrifluoroethane), HP part number 8500-1914, CD 7, is the only cleaning solvent recommended by Hewlett-Packard for cleaning 3.5 mm connectors. Several types of liquid Freon exist, so make sure that the kind you use contains only trichlorotrifluoroethane. Some other types contain harmful compounds which can damage precision connectors. A liquid is preferred over spray because the liquid can be applied sparingly and selectively. If a spray must be used, spray the cleaning swab only, not the connector.

Do not use any solvents other than liquid Freon. They can leave residues that react destructively with the metal plating on the connectors, or erode essential plastic dielectric supports. Along with your supply of solvent, keep a microscope slide or a similar piece of clear glass to check the solvent periodically for contamination.

- Plastic foam swabs, HP part number 9300-0468 CD 1, are used along with liquid Freon to clean the connector surfaces. These swabs resemble common swabs, but have lint-free plastic foam tips.

Accessory Kit Devices A2

Introduction

This chapter describes and explains the uses of the components of the HP 54007A Accessory Kit. All precautions apply to the uses covered in this chapter.

7.5 cm Beadless Airline

A 7.5 cm beadless airline has been included in the HP 54007A Accessory Kit for use in discontinuity separation and isolation. This device, although not a perfect termination, can improve and reduce reflections, increase the round-trip time of reflections, or isolate perturbations in the circuit.

The airline is a known 50 Ω load and is a good reference. Due to this fact, the primary uses are as follows:

1. The primary use of the 7.5 cm beadless airline is to separate perturbations. If you place a known load between perturbations you can separate known perturbations from those in the device-under-test and evaluate each individually.

2. The airline can be used as a precision 50 Ω load during reflection calibrations. Place the airline at the reference plane and increase the timebase until the end of the airline is offscreen (to the right). This yields a 50 Ω reference dependent only on the mechanical dimensions of the airline.

3. By placing the airline on the four channel test set, the device-under-test can be separated from the incident edge. This is convenient for viewing data that is close to the incident edge, plus you can see the 50 Ω reference more clearly in relation to the device-under-test.

Connecting the 7.5 cm beadless airline is a very sensitive procedure. More care must be taken than for normal connections. First verify that the center conductor is properly oriented when installed; the male end of the center conductor should be at the end of the outer conductor with the connector nut.

Caution 

Wear a grounded wrist strap and discharge static electricity by grasping the outer shell of the test port briefly before you begin making the connection. When connecting the airline, you are touching exposed center conductors that are connected to the internal circuits of the HP 54120 series.

The airline is small, and the center and outer conductors are almost the same length, so connecting the center conductor at the same time as the outer conductor is difficult. But, it is also difficult to slide the outer conductor over the center conductor without risking damage to the inner surface of the outer conductor. Therefore, check the center conductors to see if they have mated after the outer conductors have been loosely connected. Pressing gently on the end of the center conductor with a plastic rod will usually mate the conductors.

Connect the airline as follows:

1. Retract the connector nut on the airline fully. Put the center conductor into the airline and verify that the female end of the center conductor emerges from the female end of the outer conductor. This end will be connected to the test set.

2. Hold the airline and center conductor, bring both the airline and center conductor to the test port connector. Carefully align and mate the center conductors. Then make a preliminary connection by fastening the test set connector nut finger tight. In handling the center conductor, use lint-free gloves or finger cots.

3. When the preliminary connection has been made, verify that the center conductors have mated by pressing gently on the end of the center conductor with a plastic rod.

4. Connect the termination device to the opposite end of the airline. Carefully align and mate the center conductor of the device with the center conductor of the airline. Then make a preliminary connection of the terminating device and the airline by fastening connector nut finger tight.

Now make the final connections:

5. Start at the test port with the counter-rotation technique (see Figures A4-8 and A4-9) to eliminate air wedges from this connection. After counter-rotation, retighten the connection finger tight and use a torque wrench to make the final connection. Support the airline when making connections to avoid applying lateral or vertical (bending) force.

6. Tighten the connection of the termination device or adapter on the airline with the counter-rotation technique. You will have to hold the airline firmly to prevent loosening the test port connection. After counter-rotation, retighten the connection finger tight and use the 3.5 mm connector torque wrench to make the final connection.

Disconnect the airline by reversing the above procedure.

15 cm Beadless Airline

The 15 cm airline is not included in the HP 54007A Accessory Kit. This device will enhance testing lines and reading reflections by extending the time before they are returned and displayed. The time extension is significant. It will allow you to take measurements without the fear of a known perturbation in the circuit. The 15 cm beadless airline gives greater separation between a known perturbation and perturbations of the device-under-test.

Connection procedures are the same as for the 7.5 cm airline.

The HP 54007A storage box has been designed to accommodate the 15 cm beadless airline.

Model 909D 50 Ω Terminator

The HP 909D is a precision, low-reflection load for terminating 50 Ω coaxial systems in their characteristic impedance. When trying to normalize out gross perturbations the precision 50 Ω becomes more important. The HP 909D is used to improve the quality of precision reflection measurements and normalize the HP 54120 system to precision specifications.

The HP 909D comes with the rugged APC-3.5 connector for measurement repeatability even after hundreds of connections.

The performance is specified to 26.5 GHz. Based on limited tests the expected SWR at 34 GHz is in the range of 1.3, and the HP 909D will operate to 39 GHz before higher mode resonances have any significant effect.

Impedance stability with both time and temperature, a key parameter for precision terminations, is achieved by using tantalum nitride on sapphire thin film technology.

Maintenance

The HP 909D is used for precise measurements so it must be kept in top operating condition. Hewlett-Packard recommends that the connector be inspected periodically and cleaned if necessary. It is also recommended that the HP 909D be verified annually or after 1000 connections.

Specifications

Frequency Range: dc to 26.5 GHz

Impedance: 50 Ω

SWR: 1.02, dc-3 GHz 1.036, 3-6 GHz 1.12, 6-26.5 GHz (At 26.5 GHz the typical SWR is 1.1. Statistically, 90% of the terminators produced will meet this performance).

Power Rating: 2 W ave. @ 20° C derated to 1 W ave. at 75° C 100 W peak (10 μs max. pulse width) @ 20° C

Connector: APC-3.5 male; Opt.. 011, APC-3.5 female.

Dimensions: 23 mm x 4 mm diameter (0.91 in x 0.16 in diameter).

Environment

In a non-operating environment the terminator should be stored in a clean, dry place. The following environmental limitations apply to both storage and shipment (unless stated otherwise in the Data Sheet).

- Temperature: -55° C to +75° C
- Humidity: 95% relative @ +40° C
- Altitude: 15,300 metres (50,000 ft)

The operating environment of the instrument should be within the following limitations (unless stated otherwise in the Data Sheet).

- Temperature: 0° C to +55° C
- Humidity: 95% relative at +40° C
- Altitude: 4500 meters (15,000 ft)

Caution 

Storage or operation of the instrument in an environment other than that specified may cause damage to the instrument and may void the warranty.

Coaxial Attenuators

The HP 33340C coaxial fixed attenuator offers broad frequency coverage, low SWR and small size. The attenuator is available in nominal attenuation values of 3, 6, 10, 20, 30 and 40 dB. It is fully tested to meet specifications at all frequencies and over most of the frequency band. It will typically perform much better than specified.

The HP 33340C attenuator is included in this kit in the 6 dB and 40 dB values.

Applications

One of the main applications is to reduce the power to critical microwave circuits and avoid possible damage. Another application is to "pad" badly matched devices, such as mixers in order to minimize SWR. Use of the HP 33340C will not only protect your instrument, it also increases the input signal range.

Specifications

Frequency range: dc - 26.5 GHz

Attenuation Accuracy:		6 dB	40 dB	
	dc-18.0 GHz	0.6 dB	1.0 dB	
	dc-26.5 GHz	0.6 dB	1.3 dB	
SWR:	6 dB	40 dB		
	dc-8 GHz	1.10	1.10	
	8-12.4 GHz	1.15	1.15	
	12.4-26.5 GHz	1.27	1.25	
Attenuation Range:		6 dB	40 dB	20 dB
		2.0	100	10

Temperature, stability: 0.0002 dB/dB/@C

Maximum input power: 2W ave @ 20° C derated to 1 W ave at 75°C, 100 W peak

Power sensitivity: 0.001 dB/w

Connectors: APC-3.5 (m-f)

Weight: 8.5 g (0.3 oz)

Environmental

- Temperature, non-operating: -55° C to +85° C
- Temperature, operating: -40° C to +75° C
- Altitude, non-operating: 50,000 feet Altitude, operating: 15,000 feet Humidity: cycling 5 days, 40° C at 95% RH with condensation
- Vibration: 7 G's 5-2000 Hz Shock: 500 G's, 1.8 ms in six directions. EMC: radiated interference is within Mil Std. 461 method RE02, VDE 0871 and CISPR Publication 11.

Coaxial Short

The coaxial short is a precision, low-inductance device that will give an accurate representation of frequency information of reflected energy. It can provide a precision reference point for TDNA calibration as a time reference. It can be used to determine a baseline reference (voltage) for absolute ground.

The short is used in calibration of dielectric and velocity constants because it has a precision time offset of 21.17 ps and can be either deducted out of measurements, or more commonly, the offset is 1% and has no bearing on the measurement.

Both male and female shorts have the same electrical length.

Test Port Return Cables

The 17 inch test port return cables are used in performance verifications (see HP 54120 system service manuals.). They are included in the HP 54007A Accessory kit for low loss network measurements. And they are flexible for hard-to-access areas. The lengths are matched so that the reflection path length equals the transmission path length and both measurements can be made in the same timebase setting. The flexible cables are not precision impedance devices.

The cables included in the accessory kit have female-to-female and male-to-female end connectors. The male and female ends of the two cables allow direct connection for calibrating the transmission path. This implies that the device under test should be equipped with male and female connectors. Refer to paragraph in this chapter titled "Adapter (m-m)".

Characteristics

Impedance: 50 Ω

Capacitance: 26 pF/ft (85.3 pF/metre)

Time delay: 1.2 ns/ft (3.9 ns/metre)

Velocity of Propagation: 85% of C

Dielectric Constant: 1.4

Jacket Withstand: 1.0 kV

Dielectric Withstand: 1.0 kV

Center Conductor: 15 AWG solid
Minimum Bend Radius: 25 mm (1 inch)

To prolong the life of these cables, minimize repeated bending to a tight radius. Do not exceed the 25 mm radius specification.

VSWR

2-4 GHz 1.15
4-8 GHz 1.25
8-18 GHz 1.30
18-26.5 GHz 1.35

Insertion Loss

0-4 GHz 0.36 dB
4-8 GHz 0.50 dB
8-12 GHz 0.60 dB
12-16 GHz 0.72 dB
16-18 GHz 0.80 dB
18-26.5 GHz 1.0 dB

Note

VSWR and Insertion loss are typically 10% better than characterized.

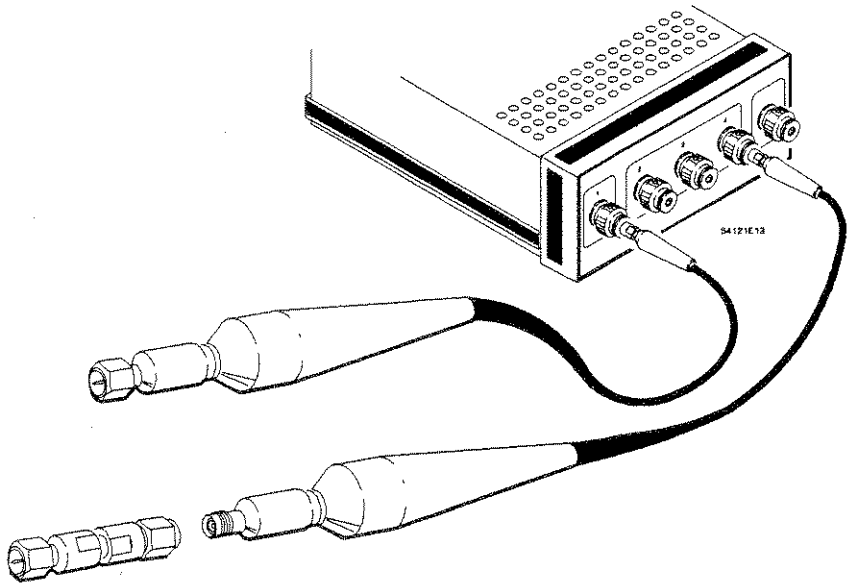


Figure A2-1. Test Port Return Cables

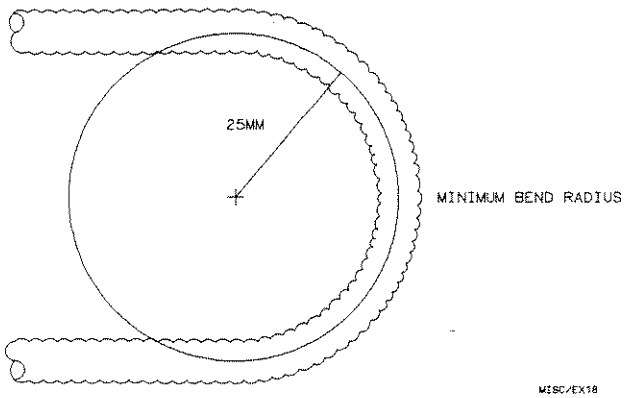


Figure A2-2. Minimum Bend Radius

Adapter (m-m)

The m-m adapter is a precision APC-3.5 device used to change connector sex. Many situations will arise when both ends to be connected are female. Placing a m-m adapter will not change the circuit characteristics other than the electrical length. The electrical length is approximately 137 ps and the mechanical length is 41 mm. These dimensions are approximate and should be verified before any critical measurements are made.

If, when using the test port return cables, the input has two female connections, this adapter can be connected to the device-under-test. This hook-up will add 137 ps to your measurement.

Semi-Rigid L Connectors

The semi-rigid "L" connectors are used to create network connections and access different channels or functions simultaneously. This allows you to view the trigger signal, attenuate the TDR signal, or connect and configure any way you desire.

Power Splitter

This section contains operating and service information for the HP 11667B power splitter. It explains how the operator checks this device and describes the one performance test required to test tracking between the output arms.

Description

The HP 11667B is a two-resistor power splitter used in oscilloscope measurement systems that have one output arm for triggering the HP 54120 system. The power splitter is useful for making attenuated TDR measurements.

Safety Considerations

Do not apply more than +27 dBm RF CW power to the HP 11667B, or the power splitter may be damaged.

Specifications

These are performance standards or limits against which the instrument may be tested.

Frequency Range: dc to 26.5 GHz

Maximum Input Power: +27 dBm (0.5W)

	dc to 18.0 GHz	dc to 26.5 GHz
Input SWR:	1.22	1.29
Equivalent Output SWR: (leveling or ratio measurement)	1.22	1.22
Output Tracking: (between output arms)	0.25 dB	0.40 dB

Connectors: Precision 3.5 mm (f) on all ports

Dimensions: 47 mm X 40 mm X 10 mm (1.85 in x 0.39 in)

Shipping Weight: 0.14 kg (4.94 oz)

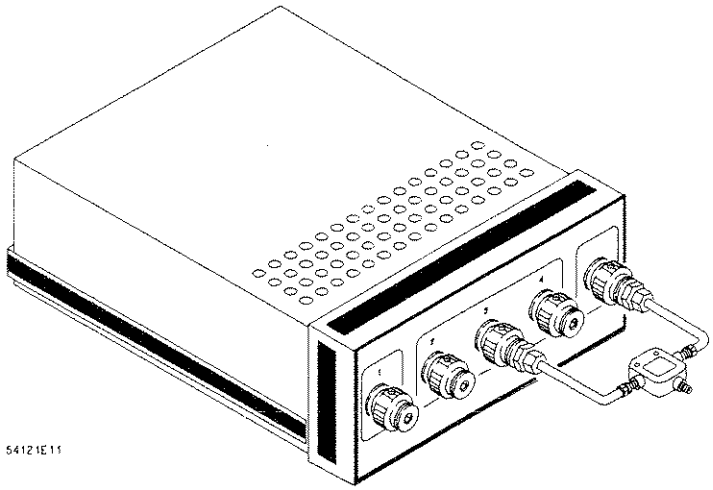


Figure 2A-3. Viewing the Trigger Signal

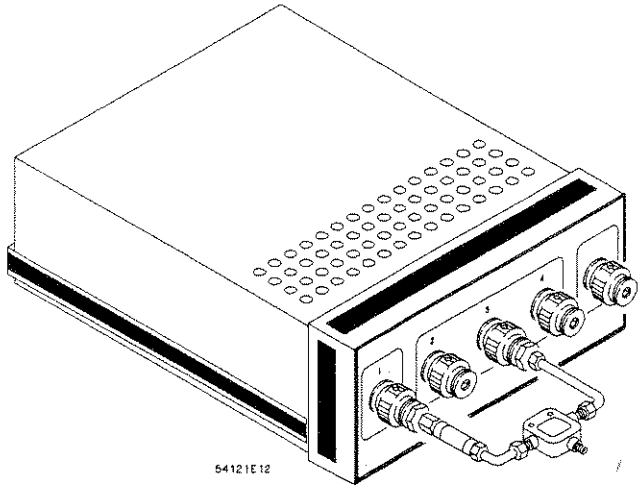


Figure 2A-4. Attenuating the TDR Signal

Supplemental Characteristics

These are not specifications, but typical characteristics included as additional information for the user.

Frequency (GHz)	dc to 18.0	dc to 26.5
Phase Tracking (between output arms)	1.5°	2.5°
Output Tracking	0.25 dB	0.40 dB

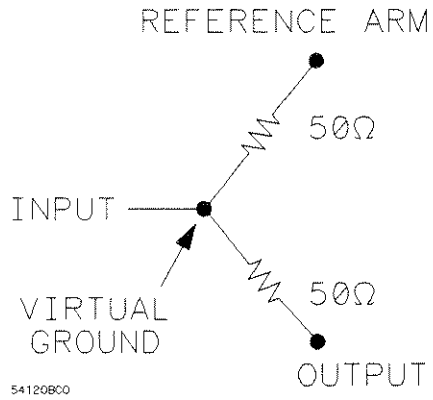


Figure A2-5. HP 11667B Power Splitter Schematic

Connections

Follow all handling precautions discussed in chapter A4 and maintain all device specifications while handling, connecting, or disconnecting the power splitter.

Operating Environment

- Temperature, 0° C to 55° C (32° F to 131° F)
- Humidity, Up to 95% relative
- Altitude, Up to 4,572 metres (15,000 feet)

Storage and Shipment

- Temperature, -40° C to +75° C (-40° F to +167° F)
- Humidity, Up to 95% relative
- Altitude, Up to 7,620 metres (25,000 feet)

Protect the HP 11667B from temperature extremes that could introduce internal condensation.

Features

1. Input port for incoming signal.

2. 3. Output ports used as exit ports. Output signal is 6 dB down in power from input signal. Either port may be used as test or reference port since power is equal in both ports.

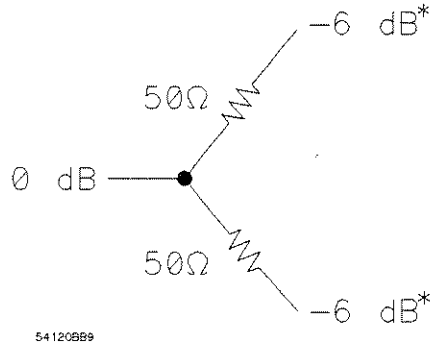


Figure A2-6. HP 11667B Power Splitter Insertion Loss

Making Accurate Measurements A3

Introduction

This chapter acquaints you with the operating conditions and procedures necessary to use the devices properly. Familiarize yourself with this information before trying any measurements.

Hewlett-Packard guarantees that the performance of your calibration devices will equal or exceed the listed specifications. Certain operating procedures must be followed if these specifications are to be met and maintained, due to the precision of the devices and to the performance capabilities of the HP 54120 system.

The performance of the TDNA calibration devices described in Device Specifications are the performance values guaranteed by Hewlett-Packard. Characteristics are typical, or nominal, values.

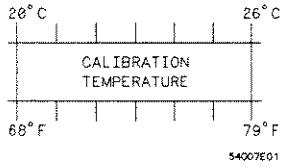
Operating Conditions and Procedures

Temperature, wear of the precision 3.5 mm connectors, and operator skill can all significantly affect the accuracy and repeatability of microwave measurements.

Temperature

Temperature of the calibration devices is critical because the dimensions of the devices (electrical characteristics) change with temperature. Figure A3-1 illustrates the allowable environmental conditions for using the HP 54007A kit. These conditions must be met if accurate measurements are to be obtained.

Note that the operating temperature during calibration and actual device measurements must be 20-26° C (68-79°F). During device measurements, the operating temperature must be within ± 1° C (1.8° F) of the temperature during calibration. Thus, if the calibration was done at 22° C (71.6° F) the operating temperature must be 21-23° C (69.8-73.4° F). If the work area is subject to temperature fluctuations, you might want to record the temperature at which the calibration is made, to assure repeatability and accuracy.



Operating temperature during actual measurements must be within ± 1° C (± 1.8° F) of the calibration temperature.

Storage temperature: Min -40° C (-40° F) Max + 65° C (+ 149° F)

Relative humidity: 20-80% (30° C maximum wet bulb) during operation, 5-95% during storage; non-condensing at all times.

Figure A3-1. Allowable Temperature, Humidity, Pressure

Barometric pressure (expressed as altitude): < 4500 metres (15,000 ft) during operation, < 15,000 during storage.
The temperature of the calibration devices and all connectors must be stable before use. Devices kept with the oscilloscope are usually at a stable temperature and can be used immediately. Devices that have been moved from one location to another should be allowed to reach the same temperature as the oscilloscope.

Heat Source

Your fingers are also a heat source. Normal body temperature is 37° C (98.6° F). You should avoid unnecessary handling of the devices during use. Some devices have a plastic jacket over the connector body to provide thermal insulation during handling. Barometric pressure and relative humidity also affect device performance, although less than temperature. Air exists between the inner and outer conductors of these devices (air-dielectric devices), and the dielectric constant of air depends on pressure and humidity. Refer to Figure A3-2.

Wear

Connector wear will eventually degrade performance. The calibration devices, which are typically used only a few times each day, should have a very long life. However, because the connectors often undergo many connections a day, they wear rapidly. Therefore, it is essential that all connectors on the HP 54120 system be inspected regularly, both visually (with a magnifying glass) and mechanically (with a connector gage), and replaced as necessary. Procedures for visual and mechanical inspection are given in the next section of this manual. For four channel test sets used in high-volume work, it is best to place an adapter on both the input and the output ports. It is easier and cheaper to replace a worn adapter than a worn four channel test set connector.

Skill

Operator skill in making good connections is essential. The mechanical tolerances of the precision 3.5 mm connectors used in the HP 54007A kit are two or three times better than the tolerances in regular 3.5 mm connectors. Slight errors in operator technique that would go unnoticed with regular connectors often appear with precision connectors in the calibration kit. Incorrect operator technique can often result in lack of repeatability. Carefully study and practice the connection procedures that are explained later in this manual until your calibration measurements are consistently repeatable.

Device Specifications

Electrical specifications depend upon several mechanical conditions. A 3.5 mm connector is a precision connector dedicated to very specific tolerances. SMA connectors are not precision mechanical devices. They are not designed for repeated connections and disconnections and are very susceptible to mechanical wear. They are often found, upon assembly, to be out of specification. This makes them potentially destructive to any precision 3.5 mm connectors with which they might be mated.

Caution

Use extreme caution when mating SMA connectors with 3.5 mm precision connectors. Prevent accidental damage due to worn or out-of-specification SMA connectors. Such connectors can destroy a precision 3.5 mm connector, even on the first connection.

Hewlett-Packard recommends that you keep three points clearly in mind when you mate SMA and precision 3.5 mm connectors:

SMA Inspect

1. Before mating an SMA connector (even a new one) with a precision 3.5 mm connector, carefully inspect the SMA connector, both visually and mechanically with a precision connector gauge designed to measure SMA connectors. A male SMA connector pin that is too long can smash or break the delicate fingers on the precision 3.5 mm female connector. Gauging SMA connectors is the most important step you can take to prevent damaging your equipment.

Alignment

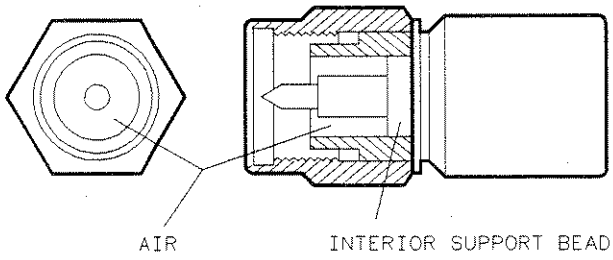
2. Be careful with alignment. Push the two connectors together with the male contact pin precisely concentric with the female. Do not overtighten or rotate either center conductor. Turn only the outer nut of the male connector and use a torque wrench (5 lb.in., 60 N-cm) for the final connection. Note that this torque is less than that when mating precision 3.5 mm connectors with each other. A torque wrench suitable for SMA connectors preset to 5 lb.in. is available (HP part number 8710-1582, CD 0).

   Install an adapter on the four channel test set if many connections and disconnections will be made. Then, if accidental damage does occur, the adapter is all that needs to be replaced. It is easier and cheaper to replace a damaged adapter than an entire four channel test set connector. SMA connectors can then be mated with precision 3.5 mm connectors without difficulty or fear of expensive and time-consuming repairs.

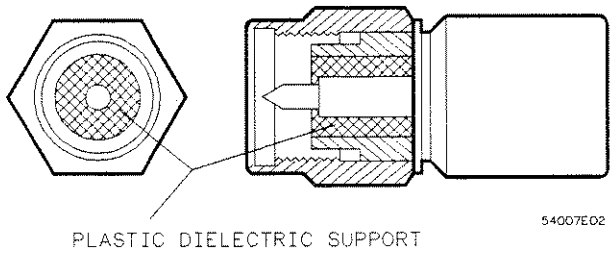
Mismatch

3. Significant structural and dimensional differences exist between these two types of connectors. Precision 3.5 mm connectors, also known as APC-3.5 connectors, are air-dielectric devices. Only air exists between the center and outer conductors. The male or female center conductor is supported by a plastic "bead" within the connector. In SMA connectors, a plastic dielectric supports the entire length of the center conductor. In addition, the diameter of both the center and outer conductors of an SMA differ from that of a precision 3.5 mm connector.

Precision 3.5 mm Connector



SMA Connector



When an SMA connector is mated with a precision 3.5 mm connector, the connection exhibits a continuity mismatch (SWR), typically about 1.10 at 20 GHz. This mismatch is less than when two SMA connectors are mated, but still higher than when precision 3.5 mm connectors are mated. Keep this fact in mind when making measurements on SMA and precision 3.5 mm coupled junctions.

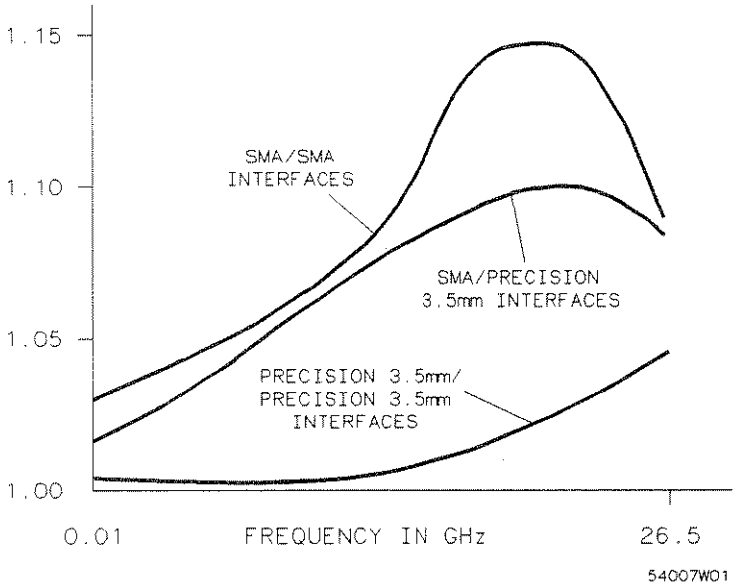


Figure 3A-2. Typical SWR of SMA and APC 3.5 Connectors

Making Good Connections A4

Introduction

This chapter explains the operating procedures which must be followed to obtain an accurate TDNA calibration.

Accuracy requires that 3.5 mm precision connectors be used. However, SMA connectors can be used if special care is taken when mating the two, and all connectors are undamaged and clean. Before each use, the mechanical dimensions of all connectors must be checked with a connector gauge to make sure that the center conductors are positioned correctly. All connections must be made for consistent and repeatable mechanical (and therefore electrical) contact between the connector mating surfaces.

Carefully study and practice all procedures in this chapter until you can successfully perform them repeatedly. Accuracy and repeatability are critical for good microwave measurements. Note that the device connection procedures differ in several important ways from traditional procedures used in the microwave industry. Hewlett-Packard procedures have been developed through careful experimentation.

Handling Precision 3.5 mm Connectors

Precision 3.5 mm connectors must be handled carefully if accurate calibrations and measurements are to be obtained.

- Store the devices in the foam-lined storage case when not in use.
- Avoid bumping or scratching any part of the mating surfaces.
- Be careful to align the center connectors. Check the alignment carefully before tightening the connector nuts.
- Use a torque wrench for all final connections in order to avoid overtightening.
- Support the devices being used in order to avoid vertical or lateral force on any connectors. This precaution is critical when using the airline, 6 cm "L", or cables.

When Disconnecting Devices:

- Do not rock or bend any connections.
- Pull the connector straight out without unscrewing or twisting.

- Before storage, screw the connector nut all the way out to help protect the surfaces, and use the plastic caps provided. These plastic caps can be taken off easily by unscrewing, rather than pulling.

Caution

Do not use a damaged or defective connector. It will damage any good connector to which it is attached. Throw the connector away or have it repaired.

A connector is bad if it fails either the visual or mechanical examinations or when an experienced operator cannot make repeatable connections. The time and expense involved in replacing four channel test set connectors warrants considerable caution when any connector might be less than perfect.

If any doubts exist about a connector, call your Hewlett-Packard representative. HP field offices offer limited professional advice and have access to the factory for information.

Visual Inspection and Cleaning

Always begin a calibration with a careful visual inspection of the connectors, including the test set connectors to make sure they are clean and undamaged.

Caution

Make sure that you and your equipment are grounded before touching any center conductor so you won't cause static electricity and create a potential for electrostatic discharge. When using or cleaning connectors on the test set, be aware that you are touching exposed center connectors that are connected directly to the internal circuits of the oscilloscope. Touching the center conductor, especially with a wiping or brushing motion, can cause an electrostatic discharge (ESD) and severely damage these sensitive circuits.

Visual Inspection

Use an illuminated, 4-power magnifying glass for visual inspection.

1. Before you begin, make sure you and any equipment you are using are grounded to prevent electrostatic discharge.

2. Examine the connectors first for obvious problems, such as deformed threads, contamination, or corrosion.

3. Next concentrate on the mating surfaces of each connector. Look for scratches, rounded shoulders, misalignment, or any other signs of wear or damage.

4. Make sure that the surfaces are clean, free of dust and solvent residues.

Dirt or damage visible with a 4-power magnifying glass can cause degraded electrical performance and possible connector damage. All connectors should be repaired or discarded immediately.

Cleaning

Cleaning the connectors is seldom necessary. Dust or dirt on the connector surfaces can be brushed or wiped away gently with a plastic foam swab or low-pressure, clean, compressed air. Be sure that you and all of your cleaning equipment are grounded to avoid electrostatic discharge.

If necessary, liquid Freon (trichlorotrifluoroethane), HP part number 8500-1914 CD 7, is the only cleaning solvent recommended by Hewlett-Packard for cleaning 3.5 mm connectors. Several types of liquid Freon exist, so make sure that the kind you use contains only trichlorotrifluoroethane. Some other types contain harmful compounds which can damage precision 3.5 mm connectors. Using the solvent in liquid is preferred because the liquid can be applied sparingly and selectively. If spray must be used, spray the cleaning swab only, not the connector. Use a microscope slide, or similar piece of clear glass to check the solvent periodically for contamination. Refer to figure A4-1.

Caution

Do not, under any circumstances, use abrasives (not even pencil eraser) or any solvent other than trichlorotrifluoroethane. Residue can be left behind that can damage the metal connector surfaces and the plastic conductor supports.

When you are satisfied that all the connectors are clean and undamaged, you can proceed to the mechanical inspection of connector dimensions.

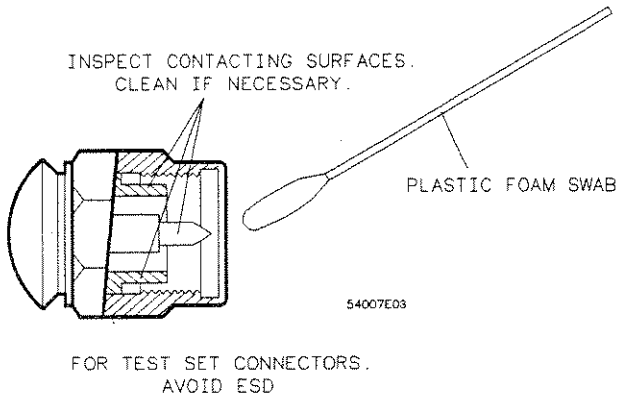


Figure 4A-1. Visual Inspection of APC 3.5 Connectors

Mechanical Inspection

Mechanical inspection of the connectors is the next step. This inspection consists of using the appropriate male or female precision 3.5 mm connector gauge to check the mechanical dimensions of all connectors, including those on the test set. The purpose of doing this is to make sure that perfect mating will occur between the connector surfaces. Perfect mating assures a good electrical match and is very important mechanically to avoid damaging the connectors themselves, especially on the oscilloscope.

Center Conductor

The critical dimension to be measured is the recession of the center conductor. This dimension is shown as MP and FP in Figure A4-2 and A4-3. No protrusion of the center conductor's shoulder is allowable on any connector. The maximum allowable recession of the center conductor shoulder is 0.003 in. (0.08 mm) on all connectors, except those on the four channel test sets.

On the four channel test set connectors, not only is no protrusion allowable, the shoulder of the center conductor must be recessed at least 0.0002 in. (0.005 mm). The maximum allowable recession of the center conductor shoulder on the four channel test set connectors is 0.0021 in. (0.056 mm).

Outer Conductor

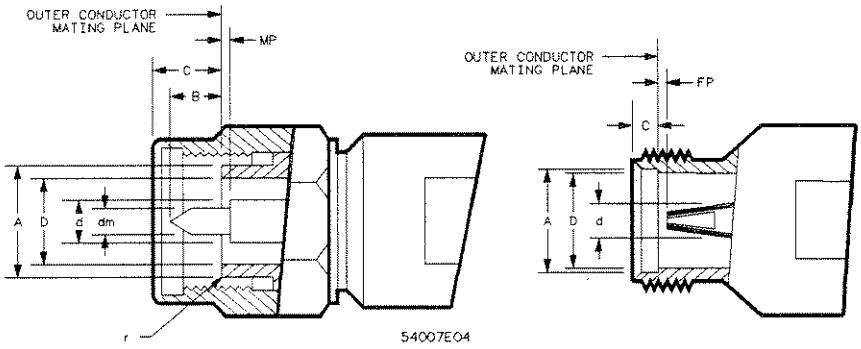
If any contact protrudes beyond the outer conductor mating plane, the contact is out of tolerance and must be replaced. If the center conductor is not recessed at least 0.0002 in. (0.005 mm), it is out of tolerance and must be replaced. In both cases the out-of-tolerance connector will permanently damage any connector attached to it. Destructive electrical interference will also result due to buckling of the female contact fingers. This is often noticeable as a power hole several dB deep occurring at about 22 GHz.

If any contact is recessed too far behind the outer conductor mating plane (0.0021 in. 0.056 mm, except in test sets), poor electrical contact will result, causing high electrical reflections. Careful gauging of all connectors will help prevent this condition.

Before using the connector gauge to measure the connectors, visually inspect the end of the gauge and the calibration block in the same way that you inspected the connectors. Dirty or damaged gauge facings can cause dirty or damaged connectors. Two connector gauges are available from Hewlett-Packard, one for each connector type, male and female. Refer to figure A4-4. A single gauge calibration block is used to zero both gauges; one end protrudes for zeroing the male connector gauge. The part number for both gauges, as well as the calibration block is 85052-80010.

Figures A4-5 to A4-7 show how to use the connector gauges. Zero the gauge with the calibration block. Refer to figure A4-5. It is recommended that you zero both gauges first, then measure each of the terminations and/or adapters that will be used. Then, as the last step, measure the test set connectors.

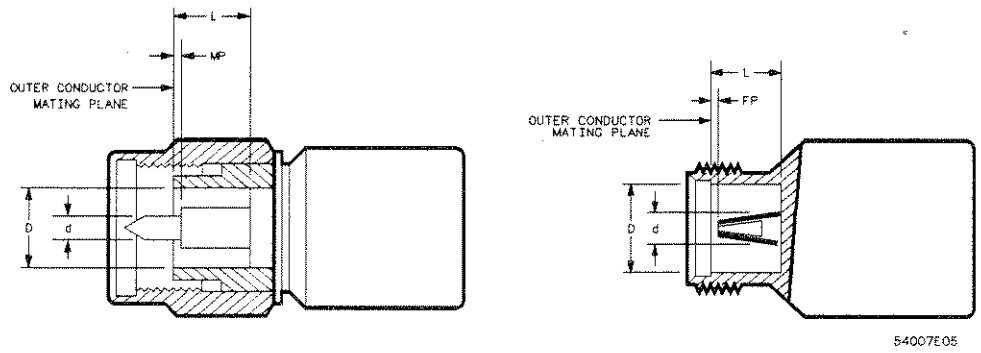
Figures A4-6 and A4-6 show how to measure precision 3.5 mm connectors. Note that a plus (+) reading on the gauge indicates recession of the center conductor and a minus (-) reading indicates protrusion. Since no protrusion of either connector is allowable, readings for connectors within the allowable range will be on the plus (+) scale of the gauge. Also note that the allowable tolerance range for the test set connectors is different from the range for other connectors. Both ranges are shown in Figures A4-6 and A4-7. Before measuring test set connectors, be sure that the power to the test set is off and that you and your equipment are grounded to prevent electrostatic discharge.



D = inside diameter of the outer conductor
d = diameter of male/female center connector
A = outside diameter of outer conductor at the mating plane
r = corner relief for male connector
B = protrusion of the male contact pin tip beyond the outer conductor mating plane
C = recession of the outer conductor mating plane behind outer face of connector
MP = recession of male contact pin shoulder behind outer conductor mating plane
FP = recession of face of female connector behind outer conductor mating plane
Dm = diameter of tip of male contact pin

Male Connectors	Female Connectors	Male Connectors	Female Connectors
D = 0.1378 ± 0.0005 in 3.500 ± 0.013 mm	D = 0.1378 ± 0.0005 in 3.500 ± 0.013 mm	B = 0.085 $^{+0.005}_{-0.015}$ in 2.16 $^{+0.13}_{-0.38}$ mm	N/A
d = 0.0598 ± 0.0003 in 1.519 ± 0.008 mm	d = 0.0598 ± 0.0003 in 1.519 ± 0.008 mm	C = 0.120 ± 0.015 in 3.05 ± 0.38 mm	C = 0.176 ± 0.002 in 1.93 ± 0.05 mm
A = 0.1803 $^{+0.000}_{-0.002}$ in 4.580 $^{+0.00}_{-0.05}$ mm	A = 0.1807 $^{+0.002}_{-0.000}$ in 4.590 $^{+0.05}_{-0.00}$ mm	Mp = 0.000 $^{+0.003}_{-0.000}$ in $^{+0.08}_{-0.00}$ mm	Fp = 0.000 $^{+0.003}_{-0.000}$ in $^{+0.08}_{-0.00}$ mm
r = 0.003 in 0.08 mm	r = 0.003 in 0.08 mm	dm = 0.037 $^{+0.000}_{-0.001}$ in 0.94 $^{+0.00}_{-0.03}$ mm	N/A

Figure A4-2. Mechanical Dimensions of Connector Faces



D = inside diameter of outer conductor = 0.1378 ± 0.0003 in
3.500 ± 0.008 mm

d = diameter of center conductor = 0.0598 ± 0.0002 in
1.519 ± 0.005 mm

MP = recession of center conductor shoulder = 0.000 + 0.000 / -0.003 in
FP 0.00 + 0.00 / -0.08 mm

L = length of outer conductor = 0.197 ± 0.001 in
0.00 ± 0.000 mm

C = concentricity of contact is governed by mating conector: typically, 0.003 FIM (TIR)

Figure 4A-3. Mechanical Dimensions of the Short Circuit

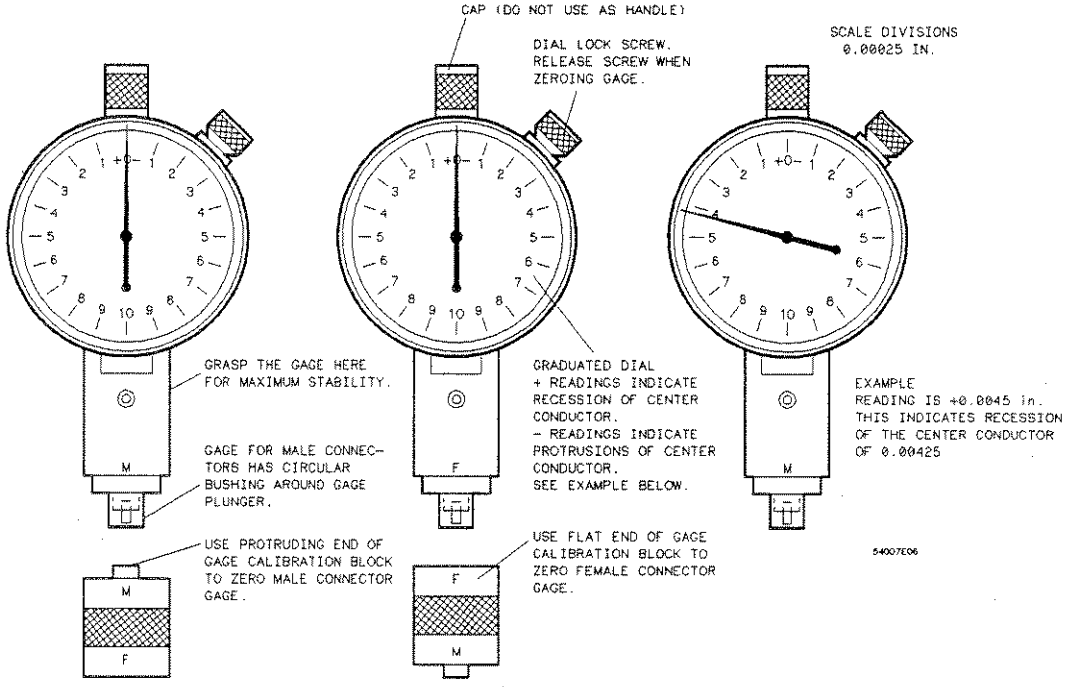


Figure A4-4. Precision 3.5 mm Connector Gages

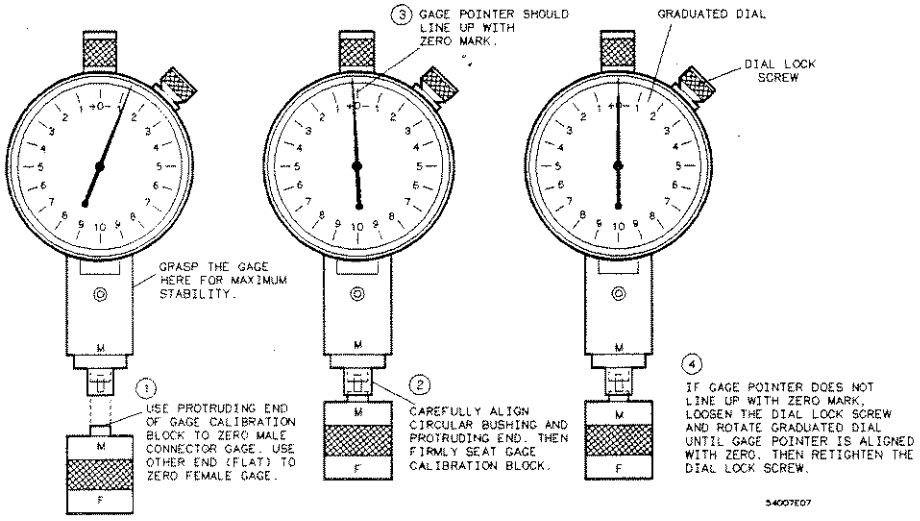


Figure A4-5. Zeroing Precision 3.5 mm Connector Gages

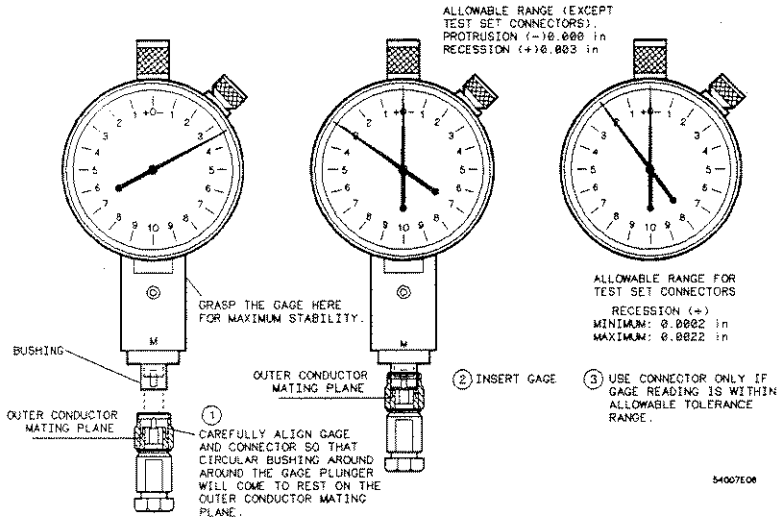


Figure A4-6. Measuring Precision 3.5 mm Male Connectors

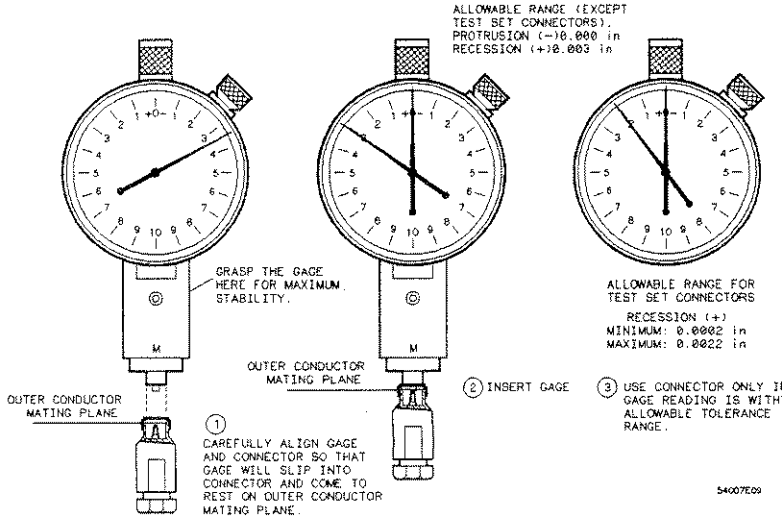


Figure A4-7. Measuring Precision 3.5 mm Female Connectors

Connecting the Devices

Figures A4-8 and A4-9 illustrate the Hewlett-Packard recommended procedures for making connections with the calibration devices. Notice that these recommended procedures differ from traditional procedures used in the microwave industry, especially the counter-rotation technique and procedure for connecting the airline.

The counter-rotation technique, recommended here, involves a slight rotation of the termination or adapter just before the final tightening of the connector nut. This eliminates the very small air wedge between the outer conductors that frequently occurs when the body is held stationary during tightening, as it is in the traditional procedure. The HP 54120 system will detect the reflections caused by such small wedges.

The counter-rotation technique does not harm the connectors. The gold plating on the outer conductor surface will become burnished in time. This is normal, and as long as the surface remains smooth, the connector is still good. After much use the gold plating may eventually wear through and expose the beryllium-copper substratum. This too is normal, and if it is smooth the connector is still good, although the beryllium-copper surface may oxidize if the connector is used infrequently.

If the burnished surface is rough, scratched, rippled, or has other irregularities, too much tightening force is being used. If the roughness is severe, the connector is ruined and should not be used.

Caution

Damage can result if SMA connectors are overtightened to precision 3.5 mm connectors. Use a torque wrench designed for SMA connectors, set to a 5 in lb (60 N/cm). A torque wrench suitable for SMA connectors is available, HP part number 8710-1582.

Counter-Rotation Technique

The recommended Hewlett-Packard counter-rotation technique is for precision 3.5 mm connectors. Before making any connections to the test set, ground yourself with a grounded wrist strap. Also, it is good practice to grasp the outer shell of the test port before you make any connections to the test set in order to discharge any static electricity on your body. This is the most effective single safeguard to prevent ESD damage to your instruments.

Connect 3.5 mm devices by the following procedure. Refer to figures A4-8 and A4-9.

1. If the device has a retractable connector nut, fully retract the nut before mating the connectors. Carefully align the male and female contact pins and slide the connectors straight together until the center and the two outer conductors meet. Be careful not to twist or bend the contact pins. You should feel a slight resistance as the connectors mate.

2. Make the preliminary connection by attaching the connector nut of the male connector to the female. The male connector is held stationary as the female connector is tightened and draws the male pin into the female connector. Refer to figure 4A-8. Any other method used may cause the male pin to damage the female connector. Support the body of the device and turn the connector nut until the mating surfaces make light contact. Do not overtighten. All you want is a connection of the outer conductors with gentle contact at all points of both mating surfaces.

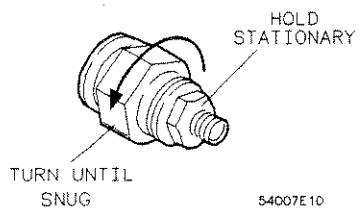


Figure A4-8. Connecting Devices

3. When you are satisfied with this preliminary connection, use the following counter-rotation technique to eliminate air wedges between the mating planes. Refer to figure A4-9. If the calibration device is male, hold the connector nut firmly. Very slowly rotate the body of the device about 10-20° counterclockwise. Note that this slight rotation or backwiping is sufficient. Greater rotation does not improve electrical performance and increases wear on the connector surfaces. If the calibration device is female (the connector nut is on the test set), very slowly rotate both the connector nut and the body of the device clockwise 10-20° (counterclockwise rotation will loosen the connection).

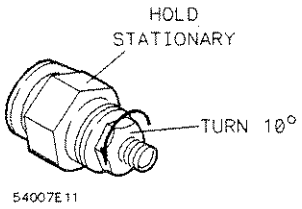


Figure 4A-9. Counter Rotation Technique

Light, smooth frictional resistance felt during the counter-rotation indicates you have made the preliminary connection correctly and that the counter-rotation technique has been successful. Roughness felt during counter-rotation indicates either that the connectors are damaged or that there is roughness in the connector nut/thread contact. Inspect both connectors again before proceeding, to make sure that the roughness is due to roughness in the connector nut interface rather than on the connector mating planes.

4. Tighten the connector nut finger tight, allowing the device to turn with the nut if it tends to do so. A small rotation of the body of the device at this point is acceptable and tends to occur naturally.

5. Use a torque wrench to make the final connection. Use of the torque wrench assures the final connection will be tight enough for optimum electrical performance, but not so tight as to distort or damage the connectors. Refer to pages A1-2.

To disconnect, follow this procedure:

1. Loosen the connector nut on the male connector with the torque wrench. Leave the connection finger tight.

2. While supporting the calibration device, gently unfasten the connectors and pull the calibration device straight out of the test port connector. Do not twist either the center conductor or the outer conductor housing or exert lateral or vertical (bending) force on the connection.

Note that some precision 3.5 mm female connector fingers are very tight and can pull the center pin of their mates out past specifications as they are disconnected. If such a male pin is inserted into a female connector it can cause considerable damage by pushing the female center conductor back too far. Be aware of this possibility and check all connectors before mating them again.