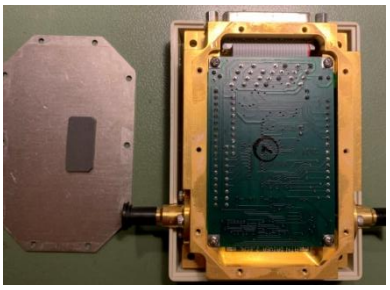
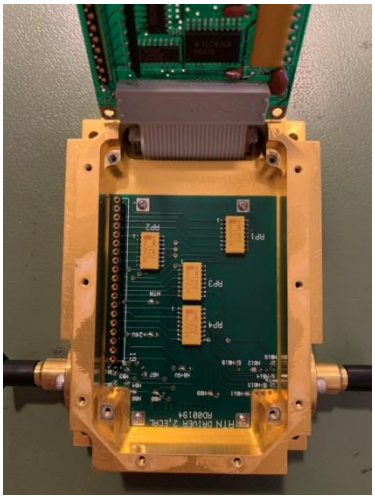
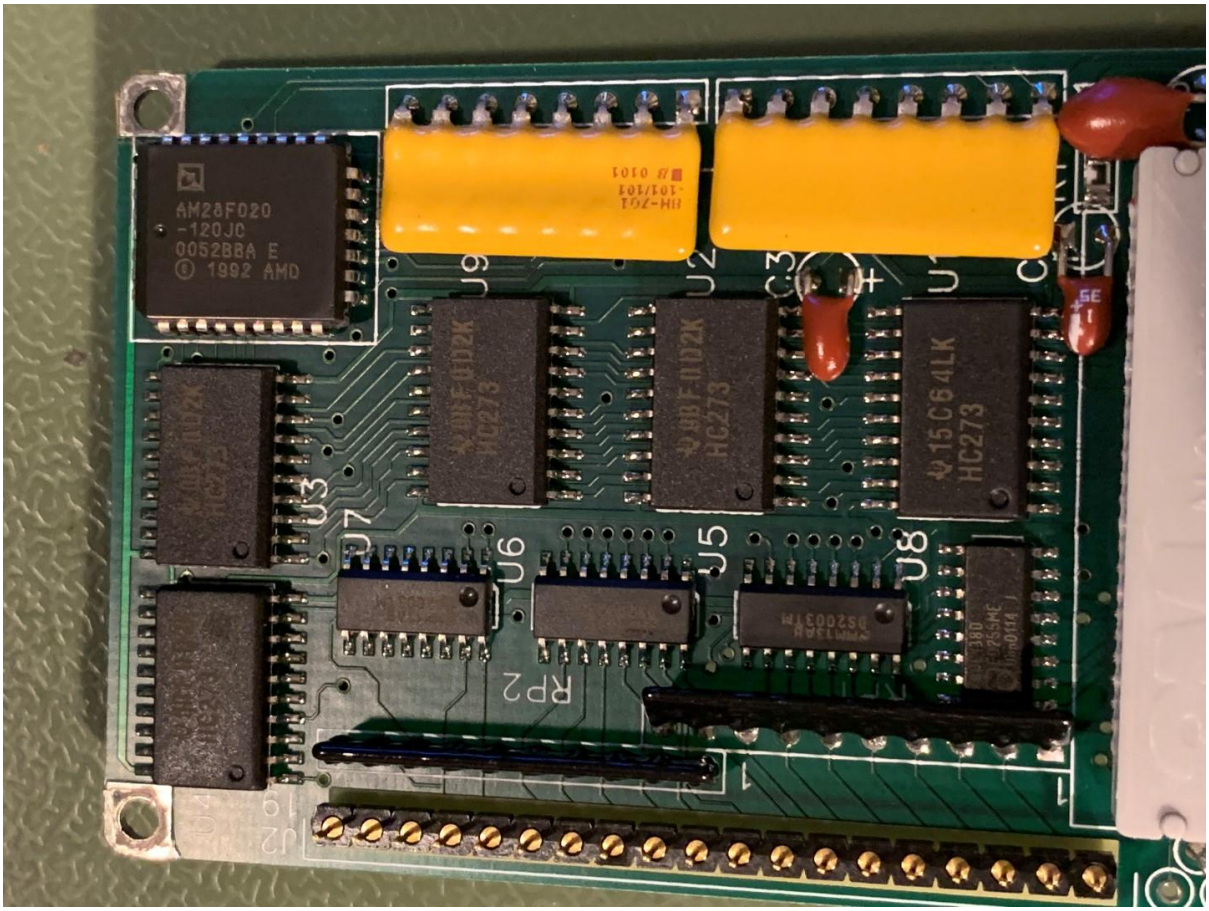
ECal kit 85062-60006







Pin connections DSUB-25

Table. Pinout DSUB-25 on 85062-6006 ECal kit.

Pin	Input/Output (to/from 85062)	Description
1	Power	J2-19, Analog +24V *
14	Power	J2-18, Analog GND***
2	Power	Digital GND***, connected to DSUB-15
15	Power	Digital GND***, connected to DSUB-2
3	Power	VCC +5 V*, U8-6 (Mux E3)
16	Power	J2-17 Analog +5 V*
4	I	Flash pin 1 VPP
17	I	Jumper site 1 (three holes labeled 1, 2, 3 – 2 and 3 connected, 1 not connected)
5	O	Short to DSUB-18 “Detect connect”
18	O	Short to DSUB-5 “Detect connect”
6	I	D-latch-1 MR’ = CLEAR’
19	I	Flash-31 WE’
7	I	Flash-24 OE’, HOLD HIGH when flash is not selected!
20	I	U8-4,5 E1’, E2’, Mux Enable
8	I	U8-3 A2 Mux address
21	I	U8-2 A1 Mux address
9	I	U8-1 A0 Mux address
22	I/O**	D-latch-D7, Flash-D7
10	I/O**	D-latch-D6, Flash-D6
23	I/O**	D-latch-D5, Flash-D5
11	I/O**	D-latch-D4, Flash-D4
24	I/O**	D-latch-D3, Flash-D3
12	I/O**	D-latch-D2, Flash-D2
25	I/O**	D-latch-D1, Flash-D1
13	I/O**	D-latch-D0, Flash-D0

* Note. DSUB 1, 3, 16 are only fed from 85097 controller when DSUB-5 and -18 are connected to each other (max voltage drop 2 V, unloaded voltage drop between these pins is 12 V).

**Note. To protect from driving a pin that may be configured for output, a 10 kΩ resistor can be put in series without affecting function.

***Note. Digital and analog GND should be connected externally through 10 kΩ resistor or similar to control potential, but to prevent current rush.

Chips

U8 – 74HC138 3-8 MUX

U1, U2, U9, U3, U4 – 74HC238 D-latch. All sharing D0-D7 and MR' connected to DSUB-6

U5, U6, U7 DS2003, Darlington drivers ending up in J2. Fed by D-latches.

Flash AM28F020, 8 MBit Flash, 256kx8

U8 MUX connection to other ICs. Chosen address sets corresponding pin LOW when U8 is enabled (otherwise all pins are HIGH)

MUX Address	IC
0	U1 D-Latch (Clock pos edge) -> U5:1-7, U6:1 -> J2:1-8
1	U2 D-Latch (Clock pos edge) -> U6:2-7, U7:1-2 -> J2:9-16
2	U3 D-Latch (Clock pos edge) Flash A0-A7
3	U4 D-Latch (Clock pos edge) Flash A8-A15
4	U9 D-Latch (Clock pos edge) Flash A16-A17 (Q2 – Q7 unused)
5	
6	
7	Flash-22 – CE'

D-Latch

WRITING to D-Latch is done by *selecting* one chip (this clock pin goes low), activate data bus and *deselect* the chip (clock pin goes high). Thus, writing to D-latches occurs when *deselecting* the chip!

Sequence to RESET ALL D-Latches:

DSUB20 HIGH	U8-4,5 E1', E2' (mux disabled, all pins high)
DSUB6 LOW	All D-Latch CLR' activated
DSUB6 HIGH	All D-Latch CLR' deactivated

Sequence to write certain D-Latch:

DSUB6 HIGH	All D-Latch CLR' deactivated
DSUB20 HIGH	U8-4,5 E1', E2' (MUX disabled, all pins high)
DSUB 9/21/8 *ADDRESS*	U8 A0-A2, select MUX pin address
DSUB20 LOW	U8-4,5 E1', E2' (MUX enabled, addressed pin low)
DSUB D-Latch D0-D7	*DATA* set data on pins 22, 10, 23, 11, 24, 12, 25, 13
DSUB20 HIGH	U8-4,5 E1', E2' (MUX disabled, all pins high, *DATA* is clocked into D-Latch)

Flash

Flash CE' is active low and will thus activate when *selected*.
CAUTION: When activated, it MAY OUTPUT VOLTAGE ON DSUB D-Latch D0-D7/Flash D0-D7! Thus use a series 10 kΩ resistor on each line.

Flash: CE' – controls power within the device. Keep low.

Flash: OE' – Output enable if pin is LOW. If pin is high, data pins are three state! Set this pin HIGH when programming D-Latches!

With OE' LOW, Flash will output the data stored in location specified by address stored in U3, U4 and U9

WE' should be held HIGH, but likely not an issue as long as VPP isn't pulled too high...

Pins on J2 (controlling RF circuitry)

Programming pins on J2 1-16. Setting one of the bits in the D-Latch registers HIGH will pull the corresponding J2 pin set (LOW). Voltage on J2 pins are approx 4.5 V when set (LOW) and 21.8 when not set (HIGH). Current consumption on 24 V seems not affected by the pins being HIGH or LOW.

On 5 V, current draw is depending on any bit being high or not. For all bits 0, current draw is 0, any bit set, current draw is approx 340 uA.

Current draw on 24 V

Note that 24 V seems to draw substantial amounts of current. This is related to the internal heater of the ECal kit. By setting current limit to 300 mA, it takes approximately 30 minutes to reach a steady state where current decreases to approximately 80 mA.

Flash content HP85062-60006 ECAL kit

0x0000 – 0x0063 Original info
0x0064 – 0x0113 Serial no, connector info, possible update info

```
00000000: 4850 3835 3036 3043 2045 4341 4c00 85c0  HP85060C ECAL...
00000010: 7c25 e87f 6400 4e6f 7620 3238 2031 3939  |%..d.Nov 28 199
00000020: 3400 ffff ffff ffff ffff ffff ffff ffff  4...............
00000030: ffff ffff ffff ffff ffff ffff ffff ffff  ................
00000040: ffff ffff ffff ffff ffff ffff ffff ffff  ................
00000050: ffff ffff ffff ffff ffff ffff ffff ffff  ................
00000060: ffff ffff 3031 3233 3400 31c0 50e8 8808  ....01234.1.P...
00000070: 3335 4633 3546 204d 5731 00c4 0456 e8fb  35F35F MW1...V..
00000080: 0883 c402 3137 204d 6179 2032 3031 3100  ....17 May 2011.
00000090: 4147 494c 454e 542f 4d54 4100 b8f8 6aeb  AGILENT/MTA...j.
000000a0: 9383 3e94 0600 741e a182 0683 c041 a298  ..>...t......A..
000000b0: 06c6 069b 0600 b804 3031 2e30 3000 00c6  ........01.00...
000000c0: 08eb 29e9 9a00 8dbe 4cff 837e 0000 0000  ..).....L..~....
000000d0: 65cd cd41 0000 00a4 17ae 1842 0001 2c01  e..A.......B..,.
000000e0: 0000 0000 84d7 9741 0080 0100 5595 0000  .......A....U...
000000f0: 3835 3036 322d 3630 3030 3600 0075 03e9  85062-60006..u..
00000100: 39ff c706 0000 0002 3130 3838 00e5 33c7  9.......1088..3.
00000110: 0686 0601 ffff ffff ffff ffff ffff ffff  ................
00000120: ffff ffff ffff ffff ffff ffff ffff ffff  ................
00000130: ffff ffff ffff ffff ffff ffff ffff ffff  ................
00000140: ffff ffff ffff ffff ffff ffff ffff ffff  ................
00000150: ffff ffff ffff ffff ffff ffff ffff ffff  ................
00000160: ffff ffff ffff ffff ffff ffff ffff ffff  ................
00000170: ffff ffff ffff ffff ffff ffff ffff ffff  ................
00000180: ffff ffff ffff ffff ffff ffff ffff ffff  ................
```

0x0190 – 0x1CD Header info for cal files.

Static structure beginning with one frequency list and then datasets of S-parameters. Prior to each set of S-parameters is a list of Short (16 bit) words about how the ECal shall be configured – see below.
Header content:

Frequency: No of entries (Short), start location (Long)

Corr values: No of config words for Ecal (Short), No of entries per set (short), No of sets (short), Start location config (Long), Start location first data set (Long)

```
00000190: 0001 f401 0000 0d00 0001 0d00 f409 0000  ................
000001a0: 0e0a 0000 0d00 0001 0d00 0e72 0000 2872  ...........r..(r
000001b0: 0000 0100 0001 0400 28da 0000 2ada 0000  ........(...*...
000001c0: 0100 0001 0400 2afa 0000 2cfa 0000 ffff  ......*...,.....
000001d0: ffff ffff ffff ffff ffff ffff ffff ffff  ................
000001e0: ffff ffff ffff ffff ffff ffff ffff ffff  ................
```

Frequency.

Frequency data starts at 0x000001F4 and contains 0x0100 entries. Data for frequency is stored in Double format (64 bit) in Hz. In this case, frequencies at 1.0, 1.1, ..., 26.5 GHz

```
000001f0: ffff ffff 0000 0000 65cd cd41 0000 00c0  ........e..A....
00000200: 2a64 d041 0000 0000 a3e1 d141 0000 0040  *d.A.......A...@
```

Corr values.

Following in the header are four areas of datasets (all containing more than one set of S-parameters). Config list contains Short (16 bit) config words to set the ECal to. Data is stored as Real, Imag, Real, Imag,... where each value is stored as float (32 bit)

No config	Set length	No sets	Config start	Set start
0x0D	0x100	0x0D	000009F4	00000A0E
0x0D	0x100	0x0D	0000720E	00007228
0x01	0x100	0x04	0000DA28	0000DA2A
0x01	0x100	0x04	0000FA2A	0000FA2C

Dataset 1 0x09F4

13 config words, 13 datasets. One S-parameter per config.

Config	Setting	Config	Setting
0	8003	7	0083
1	4003	8	0043
2	2003	9	0023
3	1003	10	0013
4	0803	11	000B
5	0403	12	0007
6	0103		

```
000009f0: 17ae 1842 0380 0340 0320 0310 0308 0304  ...B...@. ......
00000a00: 0301 8300 4300 2300 1300 0b00 0700 0078  ....C.#........x
00000a10: d2be 004c 533f 0014 8bbe 0054 613f 0050  ...LS?.....Ta?.P
00000a20: 04be 0030 693f 0000 513c 0026 6b3f 0040  ...0i?..Q<.&k?.@
00000a30: 1b3e 0080 673f 00d0 903e 00ba 5e3f 0074  .>..g?...>..^?.t
00000a40: d03e 00a0 513f 0080 053f 000c 403f 00be  .>..Q?...?..@?..
00000a50: 1f3f 009e 2a3f 0066 363f 00f0 113f 0068  .?..*?.f6?...?.h
```

Dataset 2 0x720E

13 config words, 13 datasets. One S-parameter per config.

Config	Setting	Config	Setting
0	C001	7	C100
1	C002	8	C200
2	C004	9	C400
3	C008	10	C800
4	C010	11	D000
5	C020	12	E000
6	C080		

```
00007200: c93e 0008 d5bd 0088 af3e 00d8 76be 01c0  .>.......>..v...
00007210: 02c0 04c0 08c0 10c0 20c0 80c0 00c1 00c2  ........ .......
00007220: 00c4 00c8 00d0 00e0 0014 d0be 00de 543f
```

Dataset 3 0xDA28

Single config, 4 datasets (all four S-parameters).
DA28: 0x0000

```
0000da20: 00b2 b03e 0058 6ebe 0000 0070 943d 0018  ...>.Xn....p.=..
0000da30: 3fbe 00c0 783c 00be 44be 0078 17bd 003e  ?...x<..D..x...>
```

Dataset 4 0xFA2A

Single config, 4 datasets (all four S-parameters).
FA2A: 0x0200

```
0000fa20: a6bd 00fc 4d3d 00f6 b1bd 0002 000c 9c3e  ....M=.........>
0000fa30: 00bc 533f 0094 fc3e 00b6 3a3f 004c 263f  ..S?...>..:?.L&?
```

Length of the datasets (note: first location is also used for data):
A0E – 720D : 26624, 13*256*2*4 = 26624...
722A – DA27: 26624...
DA2C – FA29: 8192
Finally:
0xFA2B + 0x2000 = 112AB. Data content in flash ends at 0x112AB.

Useful or comments? Please drop me a line at testjarfalla63@gmail.com

/Staffan