

LOW NOISE DIVISION OF 10 MHz OSCILLATORS

APPLICATION NOTE 301-1



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Introduction

As the frequency of a crystal oscillator increases it becomes increasingly difficult to produce high stability resonators. Over a period of about 20 years, the frequency of the state-of-the-art high performance crystal oscillators has increased from 100 kHz to 1 MHz, then to 5 MHz. Currently 10 MHz is the most common frequency available in the highest performance crystal oscillators. Although 10 MHz has become accepted as the standard crystal oscillator frequency, there are still many applications in communications, navigation, and instrumentation which require 5 MHz, 1 MHz or other frequencies. Many times the system designer would like to have a local oscillator or timebase which is not a standard frequency. The choices are either to purchase a special frequency oscillator, often at a significant cost increase, or to design special interface circuitry to take advantage of the standard frequency oscillator. The purpose of this application note is to assist the system designer in designing interface circuitry that will produce required frequencies by division ($\div 2$, $\div 4$, $\div 10$ and others) of a standard 10 MHz oscillator.

The system designer, interested in high stability oscillators, would like an interface to the system which minimally degrades the oscillator performance. In theory, frequency division improves the signal to noise ratio. Practically, interface circuitry can be designed which induces only a small amount of deterioration in performance. This note describes specific circuits which have produced as little as 6 dB to 8 dB of phase noise degradation (at 10 kHz from the carrier) in divide-by-ten and divide-by-two circuits, respectively, when operating on the output of an HP 10811 oscillator. It is a very high stability, ovenized, 10 MHz crystal oscillator which, with a good interface, can provide a highly stable, non-10MHz signal to a system.

The total system might look like Figure 1, with the oscillator and interface circuitry supplying the timebase signal or local oscillator to the designer's main system. The input conditioning modifies the oscillator output so that the divider receives the proper signal levels, then the output conditioning provides amplification to the signal levels needed for the time base or local oscillator requirement.

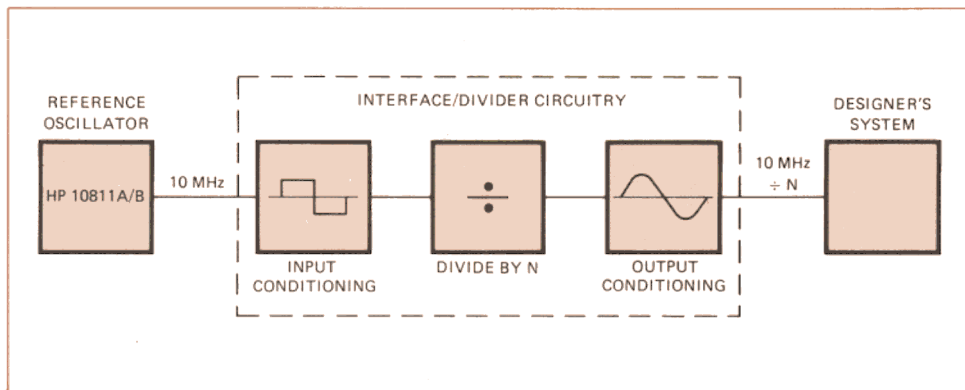


Figure 1

Noise Description

Oscillator noise performance is specified in terms of time domain stability and/or phase noise. Time domain stability and phase noise are the time and frequency domain measurements, respectively, of the same noise. Time domain stability is divided into two different measurements, long term and short term. Long term stability measures the amount of change over a day or more and is usually expressed as an aging rate. The aging rate is crystal dependent and, in good oscillator design, is not affected by the oscillator electronics. Short term stability can be affected by both the electronics and the crystal and includes spurious signals. A noisy transistor can make a major difference in the noise.

Phase noise is usually discussed as random components alone and is comparable to short term time domain stability with no spurious signals. During a phase noise measurement a 60 Hz sideband will show up as a discrete frequency while a time domain stability measurement will

show the 60 Hz sideband as a series of lumps in a graphical plot. Phase noise is normally the accepted measure used to determine the degradation of the oscillator's performance by the interface circuitry.

A measurement system that can be used for understanding very low phase noise measurements is described in the appendix after the sections on input conditioning, frequency dividers, and output conditioning.

Input Conditioning

An input stage should accept the signal from the oscillator and shape it for use by the divider circuit. The designer, therefore, must first decide on the logic family to be used in the divider and then design the input stage accordingly. The HP 10811 oscillator output is a 10 MHz sinewave of 0.5V rms into a 50Ω load. The 10 MHz signal requires DC level shifting (biasing) and squaring before a digital divider can utilize it. The dividers chosen for this application are low power Schottky TTL, requiring a low level of 0.8V and a high level of 2.0V. The most important characteristics of the input conditioning circuit are: noise since it should be as quiet as possible and speed, because sharp transitions help reduce noise.

In some applications, emitter coupled transistors (employed as current switches) have been used to bias and square the signal from an oscillator. The emitter coupled switch prevents saturation of the transistors, thus improving speed and enhancing quiet operation. Another technique described by Baugh¹, is to use a switching diode for the second transistor of an emitter coupled pair. Either circuit can be used as the input stage.

A sample circuit using the diode technique is shown in Figure 2. The circuit degrades the oscillator performance by 3 to 6 dB.* To minimize the degradation it is important to use a well regulated DC power supply to prevent spurious signals. This can be the same +12 VDC supply that powers the oscillator circuitry. Also, while building this stage it is important to keep the path from the emitter through the diode to ground via the shunt capacitor as short as possible. This way, the inductance in the path is minimized so that the high frequency gain of the stage is not degraded. This helps to keep the switching transitions sharp.

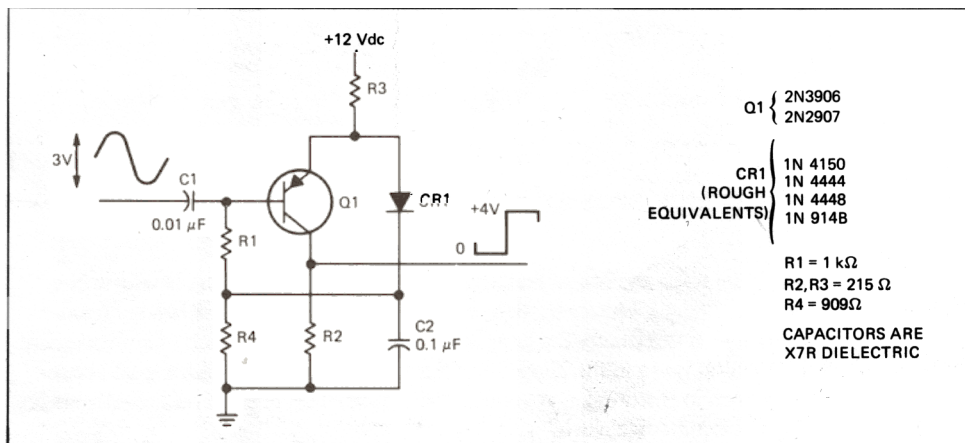


Figure 2

Dividers

The divider circuit takes the squared 10 MHz signal from the input stage, divides by the chosen integer, and provides a quiet squarewave signal. There are several questions the designer needs to consider:

- 1) **Which logic family?**—Low power Schottky is chosen for this application note. Schottky is used because it eliminates saturation, increasing the speed of the device, and

*See appendix for measurement system.

low power is used because it experimentally appears to be the quietest. However, if the designer's system uses another logic family, a trade off in performance is possible. It may be quieter to use the system's logic in the interface circuit rather than using the LS TTL and adding an output stage.

- 2) **Symmetrical or asymmetrical output?**—For this application note, symmetrical output is chosen since it can be easily filtered to provide a sinewave output. Symmetrical signals have a 50% duty cycle (they are ON for 50% of the time) and they contain no even harmonics. The lack of a second harmonic in the signal makes filtering much easier. Asymmetrical output eases the design process for odd integer division but causes a loss of signal due to the <50% ON (or OFF) time. Because of the signal loss, the signal to noise ratio is lower if the output is converted to a sinewave. Therefore, for sinewave output the phase noise may be higher.
- 3) **Which device?**—The choice of a divider IC depends partially on the answers to questions (1) and (2). After that the designer must choose a device that provides the proper division ratio.

There are numerous possibilities for integers, dividers, and devices. Therefore, only two specific examples will be discussed: symmetrical divide-by-two and divide-by-ten. Other circuits can be designed using similar techniques. For an easy symmetrical divide-by-ten the 74LS290, an asynchronous bi-quinary counter, was used (see Figure 3(a)). This device is easily modified for either a symmetrical divide-by-two (Figure 3 (b)) or an asymmetrical divide-by-five. The 74LS290 has four flipflops; three are cascaded together and the fourth can be cascaded onto either end, providing bi-quinary, asymmetrical divide-by-ten and symmetrical divide-by-ten. Cascading additional devices will provide many possibilities for additional division.

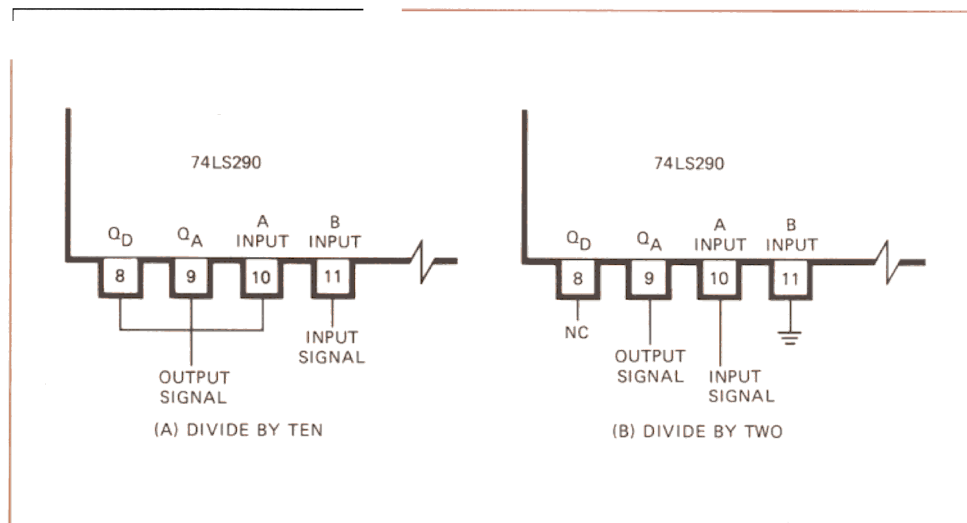


Figure 3

Ideally a divider should improve the phase noise performance in dBc by $20 \log N$ where N is the division integer (2, 4, 10 . . .). However, since the HP 10811 oscillator itself has such low phase noise, improvement is not practically possible. Any deterioration or lack of improvement in the signal must be due to noise in the divider and the buffer stages. Little additional phase noise improvement is seen in the division stage and the combination of input and divider stages looks very similar to the input stage alone.

A subtle trap for the unwary designer is the frequency capability of the divider. Some TTL devices do not function at 10 MHz, so the designer must check the frequency capabilities of every device used. For example: The 74LS290 has a maximum frequency specification of at least 16 MHz for the B input and at least 32 MHz for the A input. For a 20 MHz input signal this device probably could not provide a symmetrical divide-by-ten. However, it is adequate for a 10 MHz signal.

Power for the divider can be furnished by either a regulator circuit from the +12 VDC supply or from a separate +5 VDC supply.

Output

The output stage may or may not be necessary since the output requirement will vary for each application. The system for which the interface circuitry is being designed is going to have a specific timebase or local oscillator need. This may be for a sinewave, one of various logic levels (TTL, ECL, . . .), or something else entirely. Other requirements for the output stage are minimal phase noise degradation and proper amplification to the desired output levels.

Since individual output needs will vary substantially, this application note will address directly only TTL and sinewave outputs. The quietest output will be the TTL from the divider as there will be no additional stages in the interface to add noise. The output of the TTL device functioning as the divider may be applied to any system with TTL requirements; of course, it is necessary to follow fan-out restrictions of the divider.

Additional amplification and signal conditioning will add some amount of noise. A circuit which supplies a sinewave output of 1 Vrms into 50Ω is shown in Figure 4. This circuit adds about 2 dB of noise* to the output. Note that shorting the output of this stage causes the collector of the second transistor to suffer very large voltage swings. If the load impedance isn't matched to the output impedance, filtering problems may occur since the filter does an impedance transformation. A low pass filter is used to produce the sinewave from a squarewave. A capacitor and an inductor, resonant at the desired output frequency, provide additional band pass filtering at the frequency of interest.

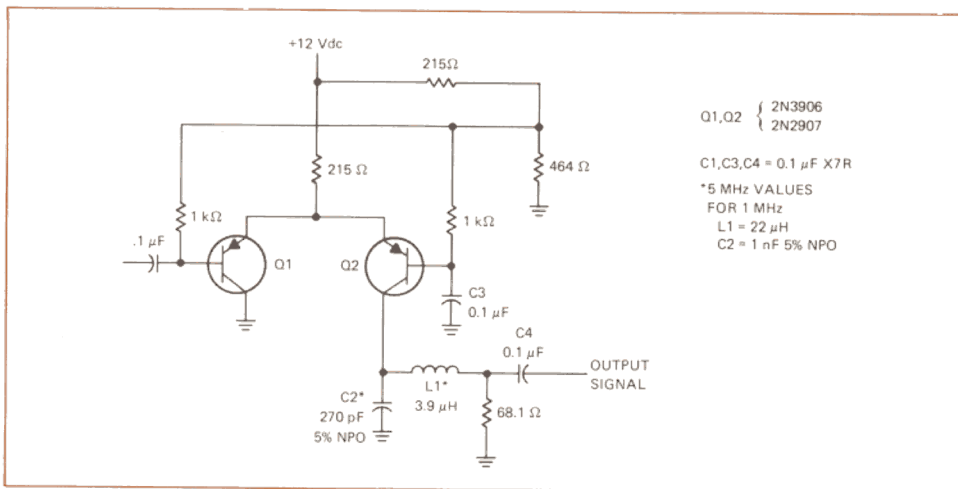


Figure 4

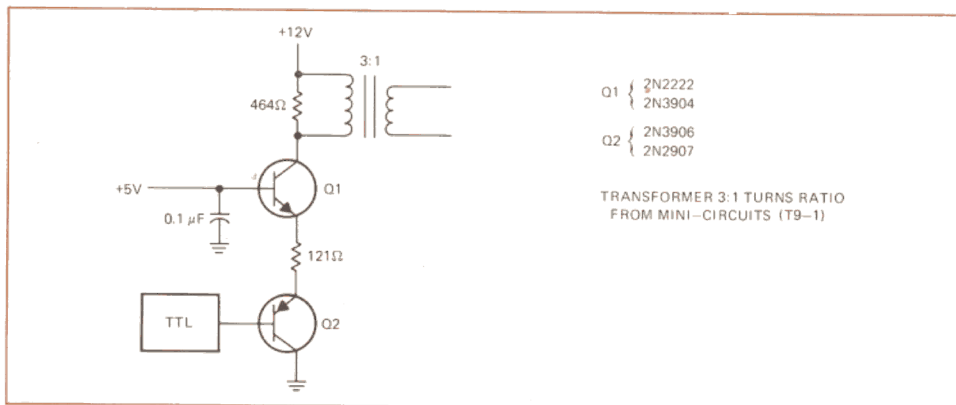


Figure 5

Another possible output stage, shown in Figure 5, provides an amplified squarewave output. The shape of this squarewave depends on transformer parameters, especially its primary magnetizing inductance. If the primary inductance is not high enough, an inordinate amount of

*See appendix for measurement system.

sag or droop will occur in the signal. The transformer also does an impedance transformation on the output. This circuit introduces about the same amount of noise* as the one in Figure 4. but it is isolated better. The amplifiers are similar in function: the one in Figure 5 outputs 1.5V peak to peak squarewave into 50Ω and it uses fewer components. The designer has a trade off of simplicity and squarewave versus sinewave.

Complete circuits are shown in Figure 6. Typical measurements data for each circuit is shown in Table 1. The $\mathcal{L}(f)$ values represent the combined noise of both oscillators or oscillator/ interface combinations. These are worst case $\mathcal{L}(f)$ values. The corrected values can vary from one oscillator being actually at the listed value and the other being at least 6 dB better to both oscillators being 3 dB better than the measured value.

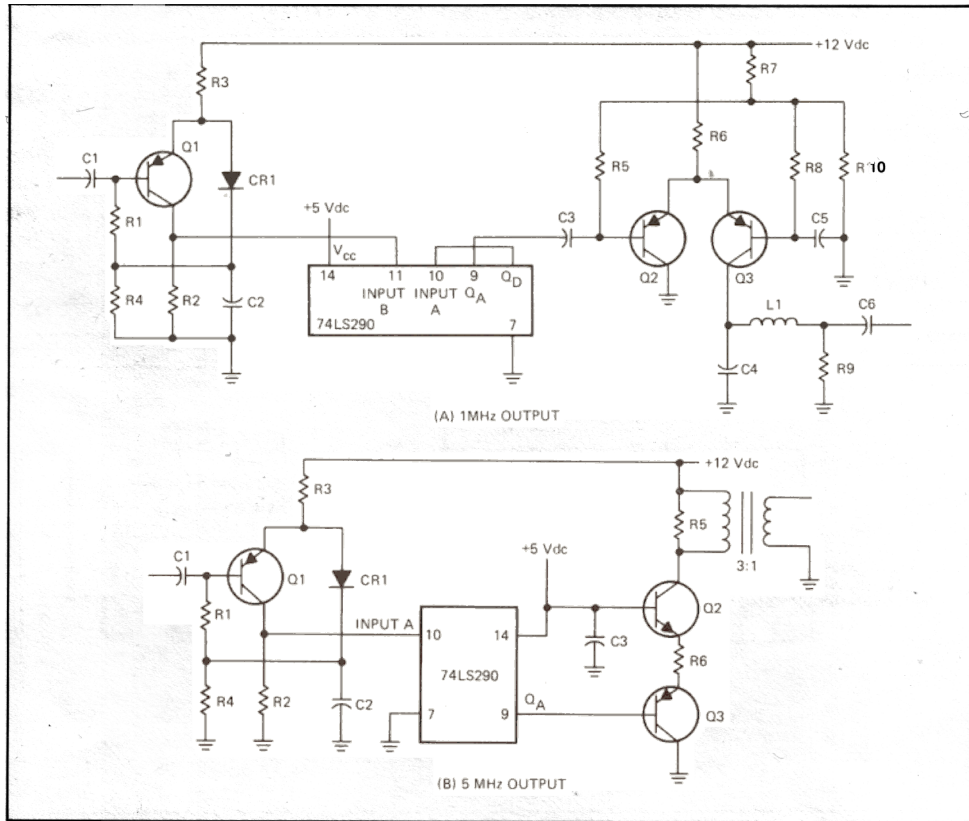


Figure 6

Table 1

What was measured?	Output circuit	frequency (Hz) (offset from carrier)	$\mathcal{L}(f)$ (dB)
10811 vs 10811		10k	-160
		1k	-157
		100	-148
10811 ÷ 2 vs. 10811 ÷ 2	Figure 4	10k	-153
		1k	-152
		100	-147
10811 ÷ 10 vs. 10811 ÷ 10	Figure 4	10k	-154
		1k	-152
		100	-145
10811 ÷ 2 vs. 10811 ÷ 2	Figure 5	10k	-152
		1k	-151
		100	-147

*See appendix for measurement system.

Appendix

Measurement

Measuring low phase noise can be very difficult. This appendix is added to describe the system used, with the intention of giving the reader some understanding of how the measurements were made. It is not intended to provide a cookbook measurement system. For those interested in actually making low phase noise measurements, Fischer's papers on frequency stability³ and frequency domain measurements² should be helpful.

What is phase noise and how is it measured? Phase noise is the amount of phase jitter or variations in zero crossings of a signal. It can also be described as random FM or PM sidebands on the signal. If non-random or discrete frequency sidebands are present, it is more meaningful to specify and discuss the non-random components separately. Phase noise is usually described in one of two ways.

$S_{\phi}(f)$ —the spectral density of phase modulation in a 1 Hz bandwidth¹, or

$\mathcal{L}(f)$ —the single sideband phase noise-to-carrier ratio in a 1 Hz bandwidth which, for high purity signals, is $\sim S_{\phi}(f) - 3$ dB.

Phase noise can be measured by several different techniques,² most of which use spectrum analyzers. When the phase noise is lower than the noise floor of the spectrum analyzer, mixing/filtering techniques must be used. Measurements for this application were made using a double-balanced mixer and a low pass filter for a quadrature mixing technique (see Figure 7). This is a phase locked loop; the null meter and oscilloscope are used to monitor the phase lock.

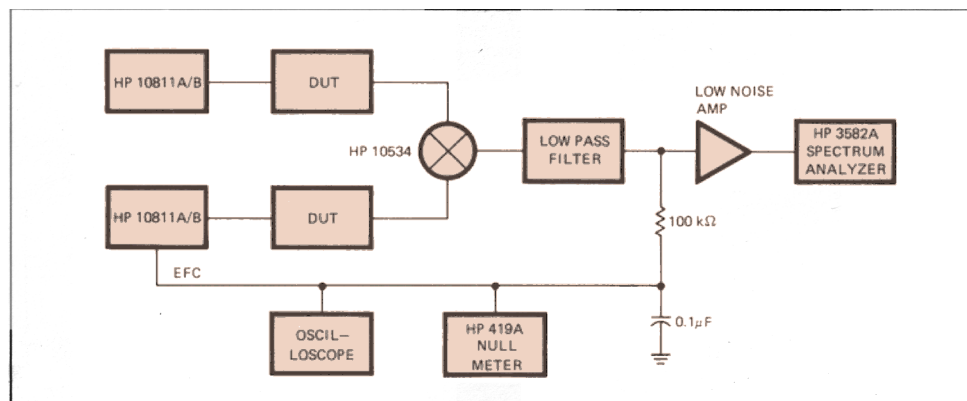


Figure 7

This system mixes two signals in phase quadrature (90° apart) to get the sum and difference frequencies and then filters to pass only the difference frequency. This filtered output is fed back to fine tune one oscillator and to maintain the phase lock. The same signal is amplified and measured with a spectrum analyzer. In this system the spectrum analyzer measures the combined noise of the two signals fed into the mixer. If measuring two identical devices against each other, the measured noise is 3 dB worse than the actual value for each oscillator (the sum of the powers). If there is more than a 6 dB difference in the two signals, the measurement may be considered to represent the worse of the two with less than $\frac{1}{2}$ dB of error.³

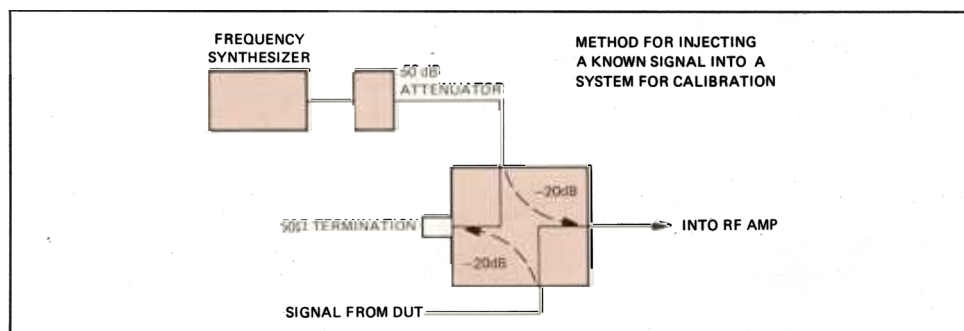


Figure 8

The calibration system (Figure 8) is used to find the correction factor to get $\mathcal{L}(f)$ in dB. The synthesizer's output level is matched to the output level of the device-under-test. The matched signal from the synthesizer is then attenuated by 50 dB and injected through a 20 dB 4-port directional coupler onto the carrier frequency. At this point the signal is 70 dB down (50 dB attenuator + 20 dB coupler) from the carrier. Another 6 dB drop occurs because the system does not respond to AM signals; therefore, the AM signal can be subtracted.

One way to see this is shown in Figure 9. The actual signal is shown in Fig. 9(a) with a single positive sideband. Equivalent, coherent AM and PM signals are shown in Fig 9(c) and 9(d). To cancel the negative sidebands it is a requirement that $|\text{AM signal}| = |\text{PM signal}|$, so each signal supplies half the voltage (Fig. 9(b)).

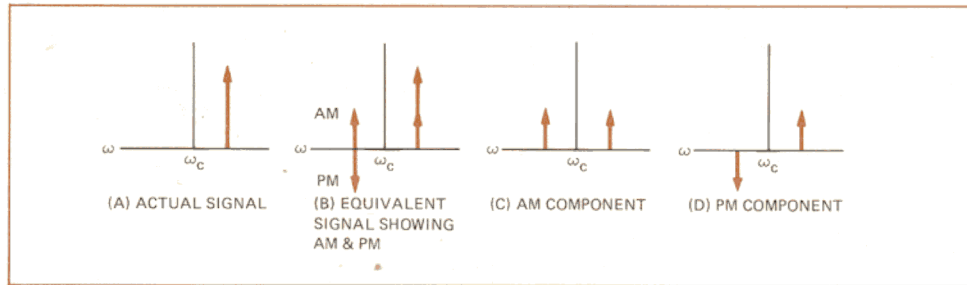


Figure 9

The calibration signal expressed as $\mathcal{L}(f)$, single sideband PM, is now seen to be 76 dB down from the carrier signal (-76 dBc); this large injected signal is easy to locate on the spectrum analyzer. The reading on the analyzer is subtracted from -76 dB to yield the calibration factor found for measurements at that frequency. Typically, phase noise is measured at 1Hz, 10Hz, 100Hz, 1kHz and 10kHz.

Since phase noise is a statistically random process and the calibration signal is discrete (non-random), some confusion may occur when the spectrum analyzer is set up for noise measurements versus for calibration. If the spectrum analyzer has a choice of filter windows, the flattop window should be used for calibration. This provides a wider window, making the measurement of discrete signals easier and more accurate. On the other hand, a Hanning window has a narrower bandwidth which produces a smoother, easier-to-read measurement for noise or other random signals. Correction factors are needed for different filter windows due to the differences in shape. The HP 3582 spectrum analyzer internally corrects for the different filter windows and it is the spectrum analyzer used for the measurements. Since the calibration signal is non-random no averaging or normalization should be used. Phase noise is random therefore, the measurement should be normalized and averaged. The measurement is normalized to a 1 Hz bandwidth ($\div \sqrt{\text{Hz}}$) and is RMS averaged (≥ 32 samples). When using RMS averaging, note that a RMS average will give a result somewhat like a peak detector. A glitch in the system will show up as a high reading and, therefore, that measurement will be inaccurate. More information of stability measurements and phase noise measurement systems are described by Fischer.^{2,3}

References

- (1) Baugh, R.A., "Low Noise Frequency Multiplication," 26th Annual Symposium on Frequency Control, U.S. Army Command, Fort Monmouth, N.J., 1972, pp 50-54. Copies available from Electronic Industries Association, 2001 Eye Street, NW, Washington, D.C. 20006.
- (2) Fischer, Michael C., "Frequency Domain Measurement Systems," 10th Ann. Precise Time and Time Interval Applications and Planning Meeting Proceedings (PTTI); Technical Information & Administrative Support Division, code 250, Goddard Space Flight Center, Greenbelt, MD 20771, 1978, pp 341-377.
- (3) Fischer, Michael C., "Frequency Stability Measurement Procedures," 8th PTTI, 1976, pp 575-617.