LIGHTWAVE CATALOG

Bit Error Ratio and Waveform Analysis

2014

VOLUME III

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Agilent Technologies

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For more than 30 years, Agilent offers high-performance solutions to support you in building the high-speed communication network. Your experience and feedback helped us to continuously improve the product performance and quality, while significantly reducing the cost, especially when it comes to manufacturing optical components.

Your needs and my confidence in our quality let me now offer our products with a 3-year warranty that's standard on all instruments, worldwide. This combination of reliability and coverage brings you three key benefits: increased confidence in instrument uptime, reduced cost of ownership and greater convenience. It's just one more way our solutions help you achieve your business goals. When you choose Agilent, you get greater reliability—standard.

Juergen Beck
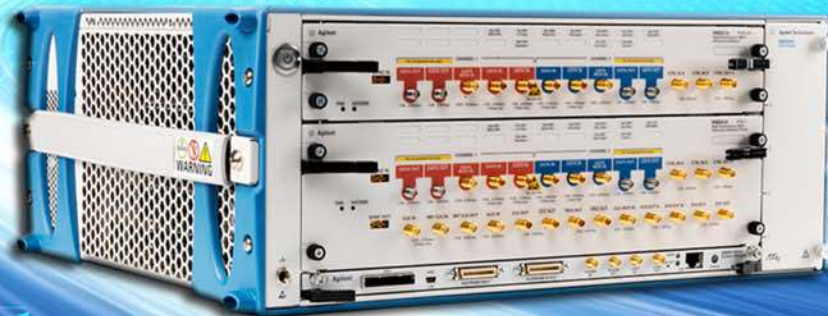Vice President and General Manager
Digital Photonic Test Division

Volume 3: Bit Error Ratio and Waveform Analysis

Introduction

Manufacturers of optical transceivers are faced with increasing challenges to their businesses, particularly how to reduce product cost. Pressures to reduce cost as data rates rise means manufacturing engineering managers and their engineers must be more creative in how to reduce costs before their competitors do. Traditional methods of eliminating tests or trying to make tests run faster may not be feasible, may not yield the intended benefit or may provide results that don't agree well with their customer's measurements. The use of parallel testing promises huge improvements, but more innovation is needed. Read below, how Agilent helps to optimize the manufacturing processes of optical components.
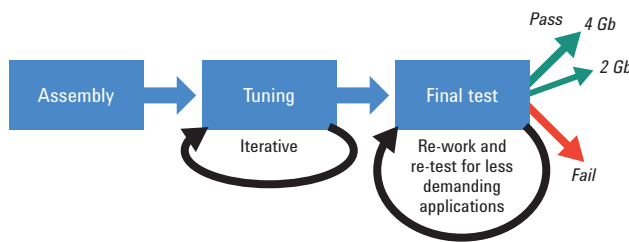
Typical manufacturing flow for simpler and less expensive devices.
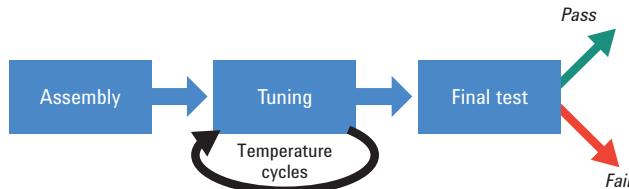
Typical manufacturing flow for more complex devices.

Common transceiver types and manufacturing flows

The number of communications standards and transceiver types has proliferated during the last decade creating more complexity for the typical manufacturing test facility. Mass market and other high volume transceivers typically have fewer tests and less temperature cycling. More complex transceivers at higher data rates have more extensive tuning, temperature cycling and challenges to meet high desired yields.

The ultimate goal of Agilent's approach is to provide a sufficiently accurate answer, very quickly, which is enabled by these recently introduced capabilities:

- DCA with parallel characterization of multiple devices, or characterization of parallel optics, Improved autoscale performance, eye tuning, rapid eye, faster eye mask testing
- Multi-channel BERTs for characterizing multi-channel devices and multi-channel standards (4 x 25 G)
- Great improvements in cost of test are achieved by testing multiple transceivers in parallel, either several single channel transmitters at once or several channels on a multi-channel transmitter
- Multi-port optical attenuator with up to four separate attenuators that are settable in parallel and provide fast settling times, a significant improvement in both multi-device and multi-lane testing
- Newly designed attenuation devices that ensure high modal fidelity in multimode fiber based transceiver testing, a contribution to narrower test margins and thus better yield

Implementing these innovations in your production line can improve by 2X to 10X the number of units tested per station per year, and result in a 2X to 5X improvement in the cost-of-test per transmitter.

Characteristics for common optical communications standards

Standards	Package types	Channel rates, Gb/s	Optical transmitters	Manufacturing test flow
• Fibre Channel to 4X • SONET/SDH to OC-48 • Gigabit Ethernet • Wireless CPRI • Passive optical network	SFP, SFF and PON	0.155 to 6.25	1	Figure 1
• Fibre channel to 16X • 10 G and 40 G Ethernet	SFP+ and XFP	1 to 14	1	Figure 1 or Figure 2
• 10 Gb, 40 Gb and 100 Gb Ethernet • 32G Fibre Channel • SONET OC-192	QSFP and CFP	10 to 29	4, 8, 10, 12	Figure 2

4

The fundamental test for these network elements is the bit error ratio, demonstrating reliable operation in digital data transmission systems and networks. The basic principle is simple: the known transmitted bits are compared with the received bits over a transmission link including the device under test. The bit errors are counted and compared with the total number of bits to give the bit error ratio (BER). The applied test data signal can be degraded with defined stress parameters, like transmission line loss, horizontal and vertical distortion to emulate worst-case operation scenarios at which the device under test has to successfully demonstrate error free data transmission. Obviously, this test is of fundamental importance for receiving network elements, due to the manifold impairments occurring on optical transmission lines. Therefore, many all optical transmission standards define such stressed receiver sensitivity on the basis of a BER measurement. The basic test methods and setups are usually very similar. However, the test conditions, the stress parameters or methods of stress generation vary from standard to standard, depending on the application area, transmission medium, data rate or data protocol.

The basic setup is sketched in the block diagram and consists of the following elemental building blocks:

- The frequency synthesizer: creates sinusoidally jittered clock, Periodic Jitter (PJ)
- The clock output from the clock source will be modulated with the sinusoidal jitter
- The electrical pattern generator creates the defined test pattern at the required rate
- The electrical stress conditioning setup adds various kinds of signal distortion onto the test pattern
- The E/O conditioning setup modifies the electrical stress signal depending on the standard:
  - The electrical-to-optical- converter converts the electrical stressed test signal into the corresponding optical stressed signal (10 GbE, 10 GFC)
  - The tunable E/O source, optical multiplexer and modulated test sources are used to emulate other lanes for higher speed standards (40 GbE, 100 GbE)
  - The optical attenuator emulates the transmission line loss and sets the optical modulation amplitude to the required level
- The optical stressed signal is fed to the optical receiver under test
- The receiver's data output signal is lead to the error detector, which compares the input and output data test patterns, detects errors and calculates the bit error ratio

What is optical stress?

Figure 3 illustrates an optical stressed signal which has to be applied to an optical receiver. While such a signal is applied to the optical input, the bit error ratio at the receiver's output has to be below a certain level (typically 1e-12) to be compliant.

Principle receiver stress test setup

OMA:
Optical Modulation Amplitude, measured in [μW] ("average signal amplitude")

ER:
Extinction Ratio, high-level to low-level, measured in [dB] or [%]

UI:
Unit Interval (one bit period)

LR, SR, ER:
Flavors of 10 Gb Ethernet standard for Long Reach (10 km), Short Reach (300 m), Extended Reach (40 km)

A0:
Vertical eye opening ("innermost eye opening at center of eye") [dBm or μW]

VECP:
Vertical Eye Closure Penalty

$$VECP = 10^x \log (OMA/A0)$$

Figure 3. Definition of the optical parameters

Stress conditioning setup:

Stress conditioning varies depending on the standard and the speed class of the component. But the principle of stress conditioning remains the same:
- Firstly, this block adds different types of jitter, like random jitter, periodic jitter or sinusoidal jitter, to generate defined horizontal closure of the test pattern's eye shape
- Secondly, this block exposes different types of amplitude distortions, like sinusoidal amplitude interference and low-pass filtering, to generate defined vertical closure of the eye-shape

Stress conditioning for 10 GbE and 10 GFC

- 4th Order Bessel Thomson Filter: Creates ISI-induced Vertical Eye Closure (VECP)
- Sinusoidal Amplitude Interferer: Causes Sinusoidal Jitter (SJ) in conjunction with limiter
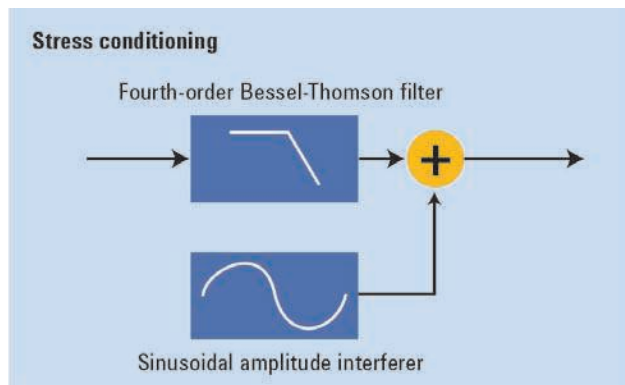
Stress conditioning for 16 GFC

- Coaxial cable: Causes Deterministic Jitter (DJ) in conjunction with limiter
- Limiter: Restores signal edges (fast rise and fall times)
- 4th Order Bessel Thomson Filter: Creates ISI-induced Vertical Eye Closure (VECP)
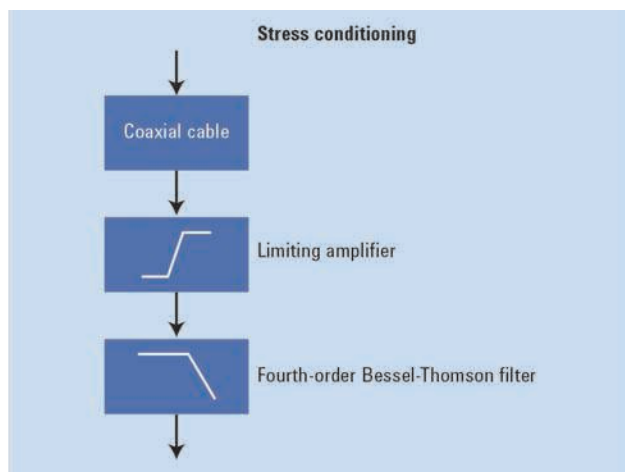
Stress conditioning for 40 GBASE-LR4 and 100 GBASE-LR4, ER4

- Sinusoidal amplitude interferer 1: Causes Sinusoidal Jitter (SJ) in conjunction with limiter
- Gaussian noise generator: Causes Random Jitter (RJ) in conjunction with limiter
- Limiter: Restores signal edges (fast rise and fall times)
- Sinusoidal amplitude interferer 2: Causes additional Vertical Eye Closure (VECP) and Sinusoidial Jitter (SJ)
- Low-pass filter: Creates ISI-induced Vertical Eye Closure (VECP)
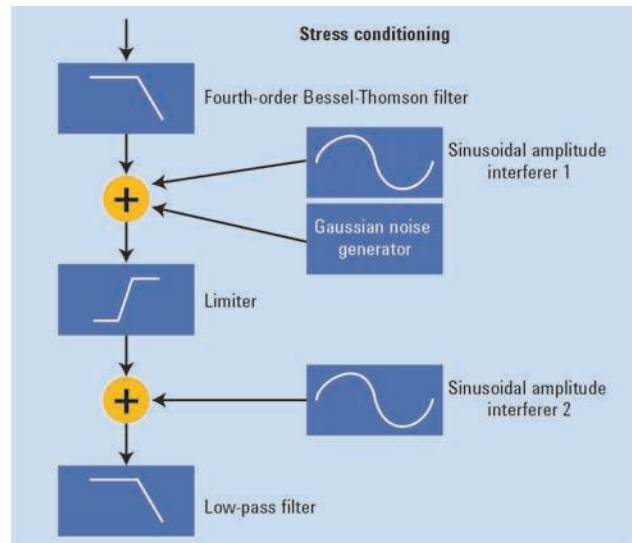
Reference transmitter conditioning setup

This setup varies depending on the speed class and number of lanes. For single lane setups it is just an E/O converter and an optical attenuator. For multi-lane applications it gets more complicated.

WDM conformance testing 40 Gbase, 100 Gbase -LR4, -ER4

E/O conditioning setup
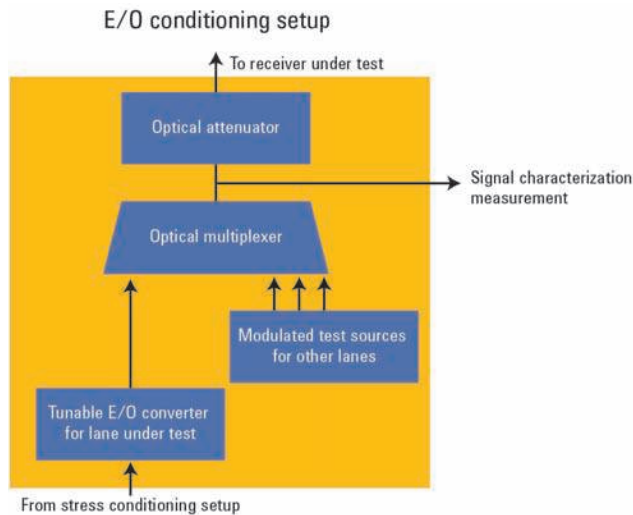
Tunable E/O converter for selecting stressed lane under test:

Modulated with stressed test signal.
OMA set to „stressed receiver sensitivity spec".
 1) Wavelength (I) tuned to corresponding worst-case sensitivity of RXuT
 2) Or fixed wavelength (I) in specified range of RxuT

Modulated test sources for other lanes:

Modulated simultaneously with valid standard pattern.
 3) OMA set to highest „difference in receive power spec".
      Wavelength (I) tuned to corresponding worst-case crosstalk to lane under test.
 4) OMA set to highest „difference in receive power spec" plus increment of loss variation of lane under test, plus increment of isolation variation to lane under test. Fixed wavelength (λ) in specified range of RXuT

Signal characterization measurement

Test signal calibration and verification

Signal characterization measurement
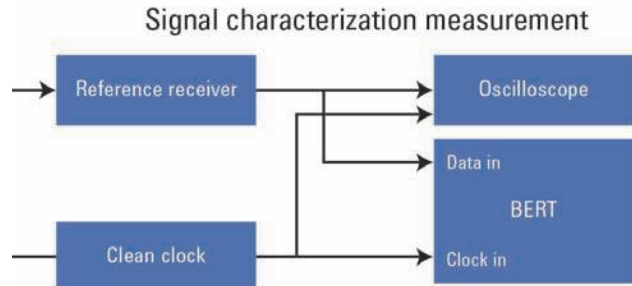
Reference receiver:

Optical to electrical converter with 4th Order Bessel Thomson response and reference frequency ft of:
ft = 7.5 GHz for 8 GFC
ft = 11.0 GHz for 16 GFC
ft = 7.5 GHz for 40 Gbase-LR4

Oscilloscope:

Use clean, un-jittered clock to verify stressed signal.

Optical receiver devices, especially those for data rates in the higher Gbps-range, are commonly exposed to extensive stressed receiver sensitivity tests during their design and qualification phase to verify their performance and to determine their margin against the requirements. The BER is measured under standard compliant stressed conditions at various optical modulation amplitudes (OMA) to BER down to 10^{-12} or lower. In the manufacturing phase, BER tests are performed at a few different OMA points down to only BER of 10^{-9} to reduce test time and cost. Applying this reduced test scheme in series implies that the device manufacturer knows very well the device margins. This leads to the requirements for a test solution with high accuracy and reproducibility regarding the stressed test signal generation. For the optical part of the stressed signal generation, this means maintaining high signal fidelity. This demand may lead especially for multimode fiber devices to some interesting test challenges. This catalog covers the test equipment needed to perform these tests. Get more detail about Agilent's N4917A Optical Receiver Stress Test Solution on page 30.

www.agilent.com/find/n4960a

Figure 1. For 16x Fibre Channel (16 GFC) for transceiver testing.

There are three topologies in this type of network including point-to-point, arbitrated loop, and switched fabric. The connections between devices use transceivers for optimization. For example, in a switched fabric topology, SFP+ (8 GFC and 16 GFC), XFP (10 Gb/s) and SFP (≤ 4 Gb/s) are types of transceivers that connect between the switched fabric and various devices such as storage and computing equipment. Typical patterns used to test transceiver devices include PRBS series, JSPAT, and K28 series which are part of the preloaded library of patterns in the N4960A 32 G BERT.

For 16 GFC applications (14.025 Gb/s), the N4960A can perform BER measurements and can provide a stressed pattern generator signal for receiver tests. 16 GFC devices must be accurately characterized to strict tolerances. The N4960A, used with the N4980A multi-instrument BERT software, can also provide jitter tolerance tests for accurate characterization.

A basic configuration using the 17 Gb/s BERT system is shown above. N4951A-P17 and N4952A-E17 can be loaded with common stress patterns for 16 GFC. You can also custom design your own patterns up to 8 Mb in length and upload them into the N4951A-P17 and N4952A-E17.

Figure 1 shows a typical hardware setup followed by a procedure showing settings for performing a BER test.
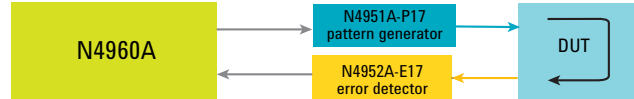
Figure 2. Test setup for 16 GFC.
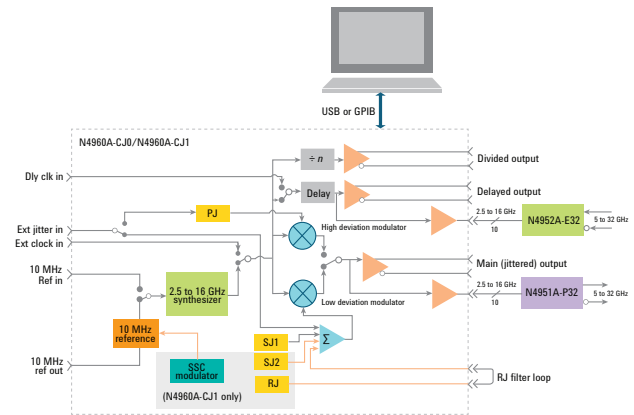
Figure 3. Block diagram (32 Gb/s system).

This example from the optical communication domain is about passive optical networks (PON) based on time division multiple access (TDMA) as used by GPON and BPON.

What is PON?

A passive optical network (PON) – specified by the full service access network (FSAN) vendor consortium – is an access technology for FTTx networks using small inexpensive, passive splitters, instead of optical repeaters. In downstream direction, the signal from an optical line terminal (OLT) is split and sent to optical network units (ONUs). The upstream direction is more challenging for the receiver performance testing, with signals sent from the ONUs to the OLT using TDMA and different power levels due to different distances.

The most critical sub-module in this system is the receiver RX of the optical line terminal (OLT) in the central office which has to deal with the upstream signal bursts arriving from the optical network units (ONU) as depicted in figure 1.
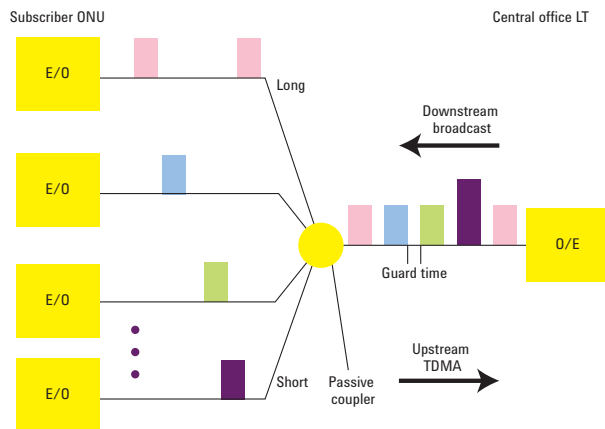
Figure 1. TDMA bursts travelling upstream on a passive optical network.

The spacing between them is very short and the amplitude may be very different, such that the RX in the OLT must settle to the appropriate threshold and synchronize its internal PLL in a very short time.

A test set-up consisting of ParBERT 81250, Agilent's Lightwave Measurement System (LMS) 8163B/8164B and a Digital Communication Analyzer (DCA) 81600D emulating the important portions of a PON is depicted in figure 3. ParBERT's exact timing capability for the two data burst and the related laser control signals is essential for standard compliant testing and characterization of the OLT's RX. The pattern sequencer allows the set-up and generation of the burst-packages with desired content.
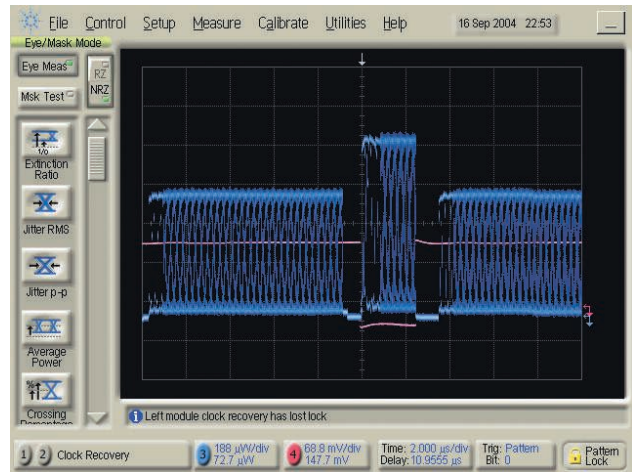
Figure 2. PON requires exact timed data bursts in an upstream test.

The SW controlling ParBERT and the other instruments can be written in a language of your choice. It can run on the same PC that the ParBERT SW resides on. Using e.g. visual Basic or C allows utilization of the Plug & Play libraries provided with ParBERT (and many other instruments), which simplifies programming.
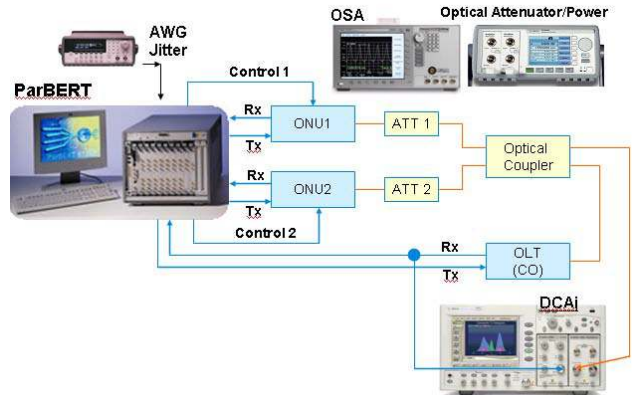
Figure 3. ParBERT based test set-up for characterization of OLTv.

Benefits of Agilent's ParBERT

Test accurately using:
 • Exactly timed signals for data bursts and control signals
 • Adjustable signal delays
 • Controllable preamble states
 • Superior signal quality

Test flexibly using:
 • A modular multi-lane generator and analyzer platform
 • Several generator/analyzer with speed classes up to 13.5 Gb/s

Application overview

For any high-speed communications signal, the channel and basic signal characteristics must be assessed for compliance with standards and interoperability with other devices in the system path. Digital Communications Analyzers (DCA's) based on wide bandwidth sampling oscilloscopes are recognized as the industry standards for accurate analysis of optical waveforms in R&D, device validation and volume transceiver manufacturing. In addition to basic eye-diagram and pulse waveform characterization, DCA's perform advanced jitter analysis and channel impedance characterization.

Transmitter compliance testing and eye-diagram analysis

Viewing the eye-diagram is the most common method to characterize the quality of a high-speed digital transmitter signal. Industry standards such as SONET, SDH, Fibre Channel and Ethernet rely on eye-diagram analysis to confirm transmitter specifications. The eye is examined for mask margin, amplitude, extinction ratio and overall quality. Tests are commonly performed using a well defined reference receiver to provide consistent results both in manufacturing test, incoming inspection, and system level applications. Standards based reference receivers and test procedures are built into the DCA's to provide compliance test capability.

In these standard tests automatic histogram analysis determines signal levels to derive key waveform parameters including but not limited to:

- Extinction ratio: How efficiently laser power is converted to information power
- Optical modulation amplitude (OMA): A measure of modulation power
- Eye height and width: An indication of how open the eye is
- One and zero levels: The logic levels of the eye
- Signal to noise ratio: Signal strength compared to noise
- Duty cycle distortion and crossing percentage: A measure of eye symmetry
- Basic peak-to-peak and RMS jitter: A measure of the timing stability of the signal

For eye mask testing industry defined masks are compared to the transmitter eye-diagram. Pass/Fail is quickly determined. Mask margins can be automatically determined. Eye mask test to industry defined hit ratios (a relatively new concept defined as the allowed number of hits compared to the total number of waveform samples) is also automatically performed. Eye mask tests are almost always performed using a reference receiver. A reference receiver defines the entire measurement system to have a specific low pass frequency response, the most common being a fourth-order Bessel low-pass response with the –3 dB frequency at 75% of the data rate.

For example, a 10 Gb/s reference receiver would have a 7.5 GHz bandwidth. A reference receiver allows the waveform to be viewed closer to what a receiver in an actual communications system would see.
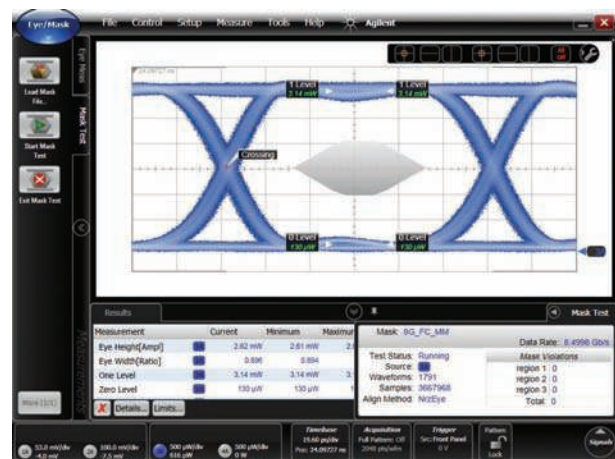
Eye mask tests are performed with a reference receiver based test system
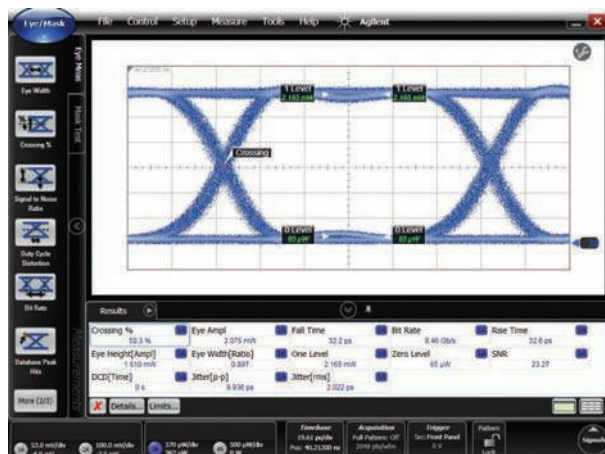
Parameters are automatically derived from the eye-diagram

Waveform measurements

Not all waveform measurements of optical signals are performed with a reference receiver. The filtering can be switched out to provide a wider bandwidth measurement system. The unfiltered properties of the waveform are accurately observed. The transmitter output may be viewed as an unfiltered eye, or as a pulse train depending on how the DCA is triggered. A DCA can be placed in 'pattern lock' mode to view the individual bits of a digital communications signal allowing a simple analysis of the waveform quality including parameters such as rise and fall times, pulsewidth and overshoot. In 'pattern lock' mode a complete single-valued waveform record, up to 2^23 bits long, can be recorded for off-line analysis. Advanced signal processing is available with the 86100D (see pages 31 to 36).
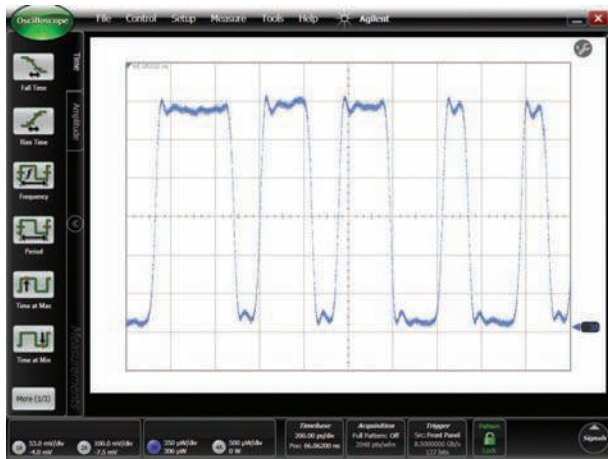
Individual bits can be observed in a 'pattern lock' display

Typically an external timing reference is used to synchronize the oscilloscope to the test signal. In cases where a trigger signal is not available or when required for a standards compliance measurement, clock recovery modules or clock recovery instruments are available to derive a timing reference directly from the waveform to be measured. Clock recovery not only provides a convenient method to synchronize the oscilloscope, it can also control the amount of jitter displayed. Clock recovery effectively creates a high-pass effect in the jitter being observed on the oscilloscope. The clock recovery system loop bandwidth defines the filtering range (see Agilent Product Note 86100-5).

Jitter analysis

Every high-speed communications design faces the issue of jitter. When data are jittered from their expected positions in time, receiver circuits can make mistakes in trying to interpret logic levels and BER is degraded. As data rates increase, jitter problems tend to be magnified. For example, the bit period of a 10 Gb/s signal is only 100 picoseconds. Signal impairments such as attenuation, dispersion and noise can cause the few picoseconds of timing instability to create eye closure that can mean the difference between achieving or failing to reach BER objectives. The problem is further aggravated by the difficulty presented in making accurate measurements of jitter. A variety of measurement approaches exist but there has been frustration within the industry around the complexity of setting up a measurement, getting repeatable results and the inconsistency of different techniques.

The "equivalent time" sampling oscilloscope, with configurations having over 80 GHz of bandwidth and extremely low levels of intrinsic jitter, is the most accurate tool available for jitter measurements at high data rates.

In many communications systems and standards, specifying jitter involves determining how much jitter can be on transmitted signals. Jitter is analyzed from the approach that for a system to operate with very low BER's (one error per trillion bits being common), it must be characterized accurately at corresponding levels of precision. This is facilitated through separating the underlying mechanisms of jitter into classes that represent root causes. Specifically, jitter is broken apart into its random and deterministic components. The deterministic elements are further broken down into a variety of subclasses. With the constituent elements of jitter identified and quantified, the impact of jitter on BER is more clearly understood which then leads to straightforward system budget allocations and subsequent device/component specifications. Breaking jitter into its constituent elements allows a precision determination of the total jitter on a signal, even to extremely low probabilities.

Advanced analysis identifies sources of jitter

Time domain reflectometry and transmission

Most optical devices have high-speed electrical input and output paths. High signal integrity is achieved with well designed signal paths. DCA's can also be configured as time domain reflectometers (TDR) to easily determine the transmission and reflection properties of electrical channels. This information can be presented as a function of time or frequency as S-parameters. Most new circuit designs are differential to improve crosstalk and interference performance. Circuits need to be characterized in single-ended, differential signal and common signal configurations.

The TDR module sends a fast edge along the transmission line, then analyzes the reflected signal and displays voltage or impedance versus distance. This information can also be converted into the frequency domain to display return loss, VSWR or reflection coefficient versus frequency. Any selected portion of the trace can also be assessed for the excess inductance or capacitance, allowing the designer to estimate the amount of required compensation in that region.

Bit Error Ratio Test Solutions

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Bit error ratio test solutions

Agilent offers the broadest choice of BERTs — covering affordable manu-facturing test and high-performance characterization and compliance testing up to 32 Gb/s.

Agilent's bit error ratio test solutions allow the most accurate and efficient design verification, characterization, compliance and manufacturing test of high-speed communication ports for today's ASICs, components, modules and line-cards in the semiconductor, computer, mobile computing, storage and communication industry.

Agilent offers the broadest portfolio with four BERT families that address a variety of speed classes, usability concepts, and flexibility as well as appli-cation specific stimulus and analysis tools. All BERTs provide cost-effective and efficient in-depth insight into critical measurement tasks for today's and next generation devices with gigabit interfaces.

BERTs are used to test and characterize many high-speed digital interfaces:

QPI, FB-DIMM, PCI Express®, SATA,/SAS USB, Thunderbolt, Display-Port, HDMI, MHL, MIPI, UHS-II, Fibre Channel, XAUI/10 Gb Ethernet, CAUI/100 GbE, CEI and other backplanes, XFI/XFP/SFP+/QSPF/CFP modules, OTN, and PON-OLTs, Serdes, DAC, ADC, etc.

Device under Test	Bit rate	Application examples	Typical requirements	Recommended Agilent BERT	
				For R&D characteriza-tion, compliance	For manufacturing
High-speed serial receiver in computer buses and backplanes	< 16 G	QPI, PCI Express, SATA, SAS, USB3, TBT, DP, MIPI D-PHY/ M-PHY, HDMI, MHL, UHS II, SMI	Data rates < 10-16 Gb/s, calibrated jitter, SSC, ISI and S.I., clock recovery, pattern sequencing	J-BERT M8020A*, J-BERT N4903B, ParBERT 81250**	N/A
Backplanes, cables, SERDES, AOC, repeaters	> 10 G – 28 G	100 Gbase-KR4/-CR4, CEI, IB, TBT, CAUI, CAUI 2/4, 10 Gbase-KR	Data rates > 10 Gb/s, de-emphasis, x-talk, PRBS	J-BERT M8020A, M8061A, N4960A, N4965A, J-BERT N4903B, N4877A	N/A
Optical transceivers and sub-components: 0.6 to 44 Gb/s	> 25 G	40 G/100 GbE, 32 G FC, CFP 2/4	Data rates > 16 Gb/s , clean signals, PRBS	N4960A, N4967A J-BERT M8020A/N4903B + M8061A/N4877A	N4960A, N4967A
	10 G	10 G/40 GbE, PON, OTN, 8 G/16 G FC, QSFP, SFP+, QFP	Data rates 3 to 15 Gb/s, PRBS, optical stress & sensitivity, framed bursts	J-BERT M8020A*, J-BERT N4903B, N4917A ParBERT**	N2101B, N4906B-012, N4962A
	< 4 G	1 GbE, XFP, PON, 1 G/2 G/4 G FC	Data rates < 3.5 Gb/s, fast bit synchronization, PRBS or framed bursts	N4906B-003, ParBERT 3.3 G	N5980A, ParBERT

*   Up to 4 lanes
** For multi-lane

Agilent offers the widest choice of serial BERT products for accurate and efficient characterization, compliance and manufacturing test for digital interfaces in computer, video, datacom and telecom applications operating up to 40 Gb/s.

The Agilent M8000 Series is a highly integrated BER test solution for physical layer characterization, validation, and compliance testing. With support for a wide range of data rates and standards, the M8000 Series provides accurate, reliable results that accelerate your insight into the performance margins of high-speed digital devices.
The high-performance J-BERT M8020A is the first product of the M8000 Series.
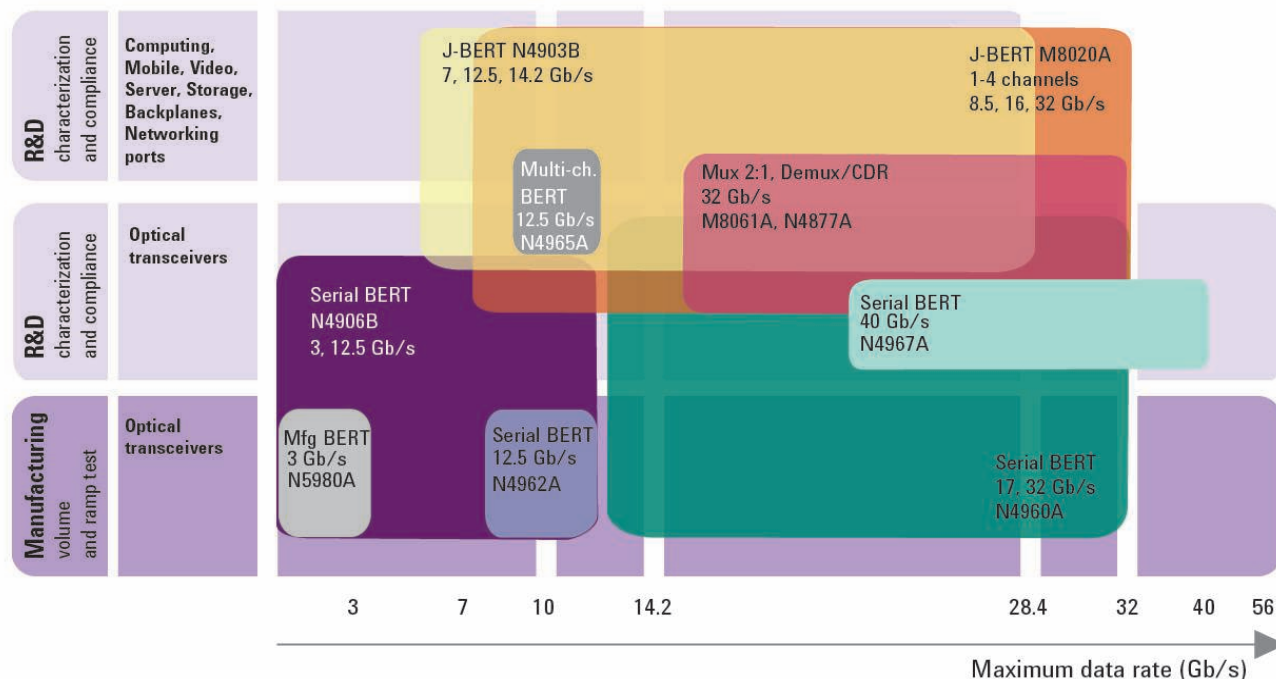
Performance BERTs for characterization and compliance verification in R&D and validation labs up to 40 Gb/s:

The **J-BERT M8020A High-performance BERT** enables fast and accurate receiver characterization of single- and multi-lane devices operating up to 16 or 32 Gb/s.

J-BERT N4903B High-performance Serial BERT – for next generation of forwarded and embedded clock designs such as QPI, PCIe™, DisplayPort, SATA, USB, TBS, UHS-II, FB-DIMM, Fibre Channel, 10 GbE.

The **N4906B Serial BERT** provides excellent signal performance but without jitter injection capabilities for budget sensitive communication device testing. The N4906B Serial BERT is offered in a 3.6 Gb/s and a 12.5 Gb/s version.

The **N4960A Serial BERT 32 and 17 Gb/s**, for testing transceivers in manufacturing and R&D.

The **N4967A Serial BERT System 40 Gb/s**, for characterizing optical transceiver devices in R&D.

The **N4965A Multi-Channel BERT 12.5 Gb/s**, for characterizing multiple lanes.

Manufacturing Serial BERTs for minimizing test cost for optical transceivers up to 12.5 Gb/s:

The **N5980A Manufacturing Serial BERT** up to 3.125 Gb/s enables transceiver test at up to one-sixth of the test cost and the front panel size of comparable BERT solutions.

The **N4962A Serial BERT 12.5 Gb/s**, an economic BERT for transceiver manufacturing test.

In combination with **86100D Infiniium DCA-X and Infiniium 90000-X Series Oscilloscopes** these BERTs are the most comprehensive and accurate jitter tolerance and analysis solution available.

Agilent J-BERT M8020A High-Performance BERT

NEW

- Data rates up to 8.5/ 16 Gb/s for pattern generator and error detector. Extension to 32 Gb/s possible with M8061A multiplexer
- 1 to 4 16 Gb/s BERT channels in a 5-slot AXIe chassis
- Integrated and calibrated jitter injections: RJ, PJ1, PJ2, SJ, BUJ, clk/2, SSC, sinusoidal interference
- 8- tap de-emphasis (positive and negative) up to 20 dB
- Interactive link training for PCI Express
- Built-in clock data recovery and equalization
- In situ calibration
- Modules and options are upgradeable

J-BERT M8020A high-performance BERT with 4 channels

The high-performance Agilent J-BERT M8020A enables fast, accurate receiver characterization of single- and multi-lane devices running up to 16 or 32 Gb/s. With today's highest level of integration, the M8020A streamlines your test setup. In addition, automated in situ calibration of signal conditions ensures accurate and repeatable measurements. And, through interactive link training, it can behave like your DUT's link partner. All in all, the J-BERT M8020A will accelerate insight into your design.

Target applications
R&D and test engineers who characterize, verify compliance of chips, devices, boards and systems with serial I/O ports up to 16 Gb/s and 32 Gb/s. The M8020A can be used to test popular serial bus standards, such as: PCI Express®, USB, MIPI M-PHY, SATA/SAS, DisplayPort, SD UHS-II, Fibre Channel, front-side and memory buses, backplanes, repeaters, active optical cables, Thunderbolt, 10 GbE, 100GbE (optical and electrical), SFP+, CFP2/4 transceivers, CEI.

Specifications
For operating range 32 Gb/s: see M8061A
For operation up to 16 Gb/s:

Pattern generator
- Operating range: 150 MHz to 8.5 GHz (option G08 or C08), 150 MHz to 16.2 GHz (option G16 or C16). For extension to 32.4 Gb/s: use M8061A in addition.
- Data outputs: 1 or 4 for 16 Gb/s (option 0G2 for second channel per M8041/51A module)
- Output amplitude: 50 mV to 1.2 Vpp (single ended)
- Transition time: 15 to 20 ps typical (20-80%)
- De-emphasis: 8 taps positive/ negative (option 0G4)
- Intrinsic jitter: 8 ps pp typical
- Connectors: 3.5 mm (f)
- Supplementary outputs: trigger out, clock out

Pattern
- PRBS: 2^n-1, n = 7,10, 11 15, 23, 23p, 31
- Memory: 4 Gbit per channel
- Sequencer: 3 counted loop levels, 1 infinite loop
- Interactive link training for PCIe

Jitter tolerance test
- Calibrated jitter sources: multi-UI low-frequency jitter up to 5 MHz, high-frequency jitter up to 1 UI @ 500 MHz (RJ, PJ1,PJ2, BUJ, sRJ), clk/2 ±20 ps
- SSC: ±5000 ppm
- ISI: eight ISI traces (see M8048A)
- Interference: built-in common-mode up to 400 mV and differential-mode up to 30% of output amplitude
- Automated jitter tolerance test

Analyzer
- Data inputs; 1 to 4 (option 0A2 for second channel per M8041/51A module)
- Clock recovery: built in, adjustable loop bandwidth up to 20 MHz
- Sensitivity: 50 mV
- CTLE: yes
- Connectors: 3.5 mm (f)

Ordering

J-BERT in 5 –slot AXIe chassis w/ emb. controller	M8020A-BU1
J-BERT in 5 –slot AXIe chassis	M8020A BU2
16 Gb/s BERT 2 ch with clock, 3-slot AXIe module	M8041A*
16 Gb/s BERT 2 ch, 2-slot AXIe module	M8051A
32 Gb/s Multiplexer 2:1 with de-emphasis	M8061A
System software for M8000 Series	M8070A

* available options for M8041A:
8.5/16Gb/s, generator-only, 2nd channel generator/analyzer, de-emphasis, jitter sources, interference sources, reference clock multiplier, SER/FER analysis, link training, CTLE

Agilent M8061A 32 Gb/s Multiplexer 2:1 with De-Emphasis

NEW

- Expands data rate of pattern generator of J-BERT M8020A up to 32.4 Gb/s and J-BERT N4903B up to 28.4 Gb/s
- Adjustable positive and negative de-emphasis for up to 8 taps, optional
- Internal superposition of interference for common-mode and differential mode
- Transparent to jitter generated by J-BERT M8020A or N4903B
- Clock/2 jitter can be added
- Electrical idle
- Control from M8000 Series software as well as from J-BERT N4903B user interface via USB
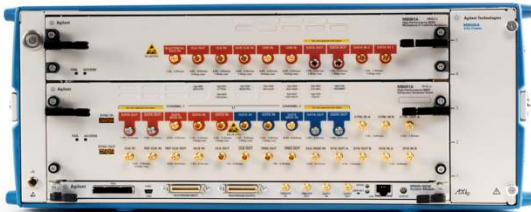
The M8061A multiplexer in a 32 Gb/s BERT setup with J-BERT M8020A.

The M8061A multiplexer can be used to extend the data rate of J-BERT N4903B to 28.4 Gb/s.

R&D and test engineers who need to characterize serial interfaces of up to 32 Gb/s can use the M8061A 2:1 Multiplexer with optional de-emphasis to extend the rate of J-BERT M8020A as well as J-BERT N4903B pattern generator. For the most accurate receiver characterization results, the M8061A provides four calibrated de-emphasis taps, which can be extended to eight taps, built-in superposition of level interference and clock/2 jitter injection. The M8061A is a 2-slot AXIe module that can be controlled via USB from the M8000 Series software as well as from the J-BERT N4903B user interface.

Target applications

R&D and test engineers who characterize, verify compliance of chips, devices, boards and systems with serial I/O ports up 32 Gb/s. Typical receiver test applications include:

- Optical transceivers such as 100GBASE-LR4, -SR4 and -ER4, 32G Fibre Channel
- SERDES and chip-to-chip interfaces such as OIF-CEI -VSR,-SR, -LR
- Backplanes, cables, and repeater such as 100GBASE-KR4, CR4, Infiniband EDR and proprietary active optical cables and interconnects

Specifications

- Operating range of data outputs: 300 Mb/s to 28.4 Gb/s (with N4903B), or 32.4 Gb/s (with M8020A).
- Output amplitude: 50 mV to 1.2 Vpp (single ended)
- De-emphasis: 4 taps (option 004), extended to 8 taps (option 008). Positive/ negative, 20 dB max.
- Transition time: 14 ps typical (20%-80%) for > 25 Gb/s
- Intrinsic jitter: 6 ps pp typical
- Transparent to jitter from N4903B and M8020A
- Auto-alignment of clock/data skew
- Clk/2 jitter ± 20 ps
- Internal superposition of CMI, DMI
- Electrical idle
- Output connectors: 2.4 mm (f)

Ordering

28/32Gb/s Multiplexer 2:1 module, 2-slot AXIe	M8061A-001
De-emphasis, 4 taps	M8061A-004
De-emphasis, extension to 8 taps	M8061A-008
Integrated in 2-slot AXIe chassis with USB	M8061A-BU2
Matched cable kit for connecting with N4903B	M8061A-801

Recommended in addition:

N4877A Clock data recovery with de-multiplexer	N4877A-232

Fast, compact, and affordable BER testing

Testing 16x Fibre Channel (16GFC) transceivers, Infiniband FDR, Infiniband EDR, 100 G Ethernet etc, requires equipment capable of operating up to at least 25 Gb/s, with accurate characterization to strict tolerances. Until now, these systems have been extremely expensive. This often results in multiple designers needing to share the one serial BERT in the lab, delaying their characterization and development schedule.

The Agilent Technologies N4960A serial BERT 32 and 17 Gb/s is an affordable alternative for R&D working at data rates up to 32 Gb/s.

The solution is compact, allowing it to be easily transported throughout the lab and manufacturing. But with its low price, a fraction of competing stressed BERTs, you can afford to put one on each bench.

Figure 1: 16 x Fibre Channel (16 GFC) transceiver testing

Compact architecture

The N4960A serial BERT controller is a platform that forms the basis of the stressed serial BERT. The N4960A serial BERT controller adds the precision timing and control required for the remote pattern generator and error detector heads.

The concept of remote heads, first introduced in the N4965A multi-channel BERT, puts the pattern generation and error detection near the device under test, eliminating long cables which degrade the signal. This is especially important at higher data rates.

Figure 3: N4980A JTOL measurement window

Affordability without compromise

The N4951A/B pattern generator and N4952A error detector remote heads are available in two data rate ranges covering either 4 to 17 Gb/s or
5 to 32 Gb/s with no gaps or missing data rates. They generate and test full rate patterns directly without the need for external multiplexers and delay matching often used in other modular BERT systems.

The signal fidelity in the eye is outstanding, owing to the use of custom-designed and built output amplifiers. Output parameters of amplitude, offset, and termination voltage are user settable.
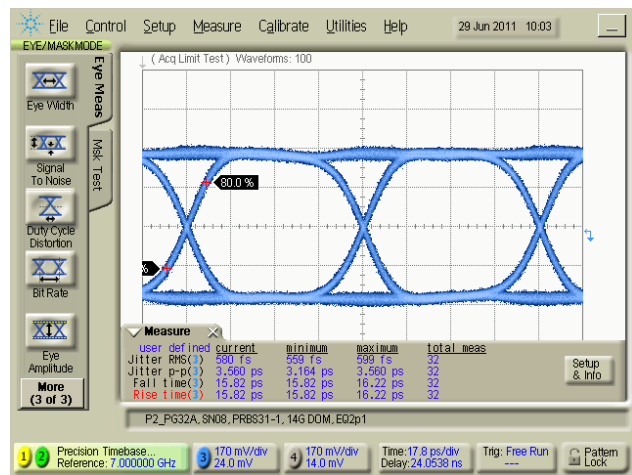
Figure 2: Typical eye at 14 Gb/s

Accurate, repeatable jitter tolerance

The N4960A serial BERT controller contains an accurately calibrated sinusoidal jitter source capable of high deviation at low frequencies, and lower deviation at frequencies up through 200 MHz. A second sinusoidal jitter source, plus random jitter source and spread spectrum clocking can be added with option -CJ1.

Integrated analysis software

Support for both models of the N4960A is included in the N4980A multi-instrument BERT software. The software provides an intuitive user interface. It also provides single or multi-channel BER measurement capability with an unlimited number of channels. Setup is so easy that you'll be testing in seconds.

The optional JTOL measurement package in the N4980A multi-instrument BERT software (Signal Integrity Studio) performs all the set-up and control for single or multi-lane JTOL, and with an intuitive "point and click" template editor.

Agilent N4960A Serial BERT 32 and 17 Gb/s

N4960A Controller Specifications

Standalone clock source and/or Serial BERT controller

Clock output configuration:	Jitter (stressed), Delay, and Divided outputs available. Clock generator Jitter and Delay outputs are shared with Pattern Generator (PG) and Error Detector (ED) heads respectively. The PG/ED data rate is double the frequency of the clock outputs.
Frequency range	1.5 to 16 GHz (1.5 to 8.5 GHz when N4951A-P17, N4951B-H17/D17 or N4952A-E17 is attached)
Outputs	Jitter (stressed), Delay, and Divided
Output configuration (all outputs)	Differential
Clock output amplitude range	300 mV to 1.7 V pp, single ended
Delayed clock delay range	0 to ±1,000 UI
Divided clock divide ratio	÷ 1, 2, 3,..., 99,999,999 integer divider
Jitter clock injection	
- Sinusoidal	SJ1, SJ2 1 – 200 MHz, up to 1UI
- Random RJ	Up to 75 mUI
- Periodic PJ	1 to 17 MHz, up to 100 UI (to 62.5 kHz)

SJ2, RJ requires Option –CJ1. The amplitude of any stress appearing on the front panel jitter clock output will be 1/2 of the value appearing in the N4951A/B pattern generator head. Changing stress amplitudes on the front panel jitter clock output will also change the level appearing on the pattern generator output.

Spread spectrum clock (Option -CJ1)   1 Hz to 50 kHz, 0 to 1.0 %, Triangle, down spread, center spread, or up spread.

Agilent N4951A

Agilent N4952A

Pattern generator head specifications

Data rate range	4 to 17 Gb/s (Options P17/H17/D17)
	5 to 32 Gb/s (Options P32/H32/D32)
Pattern selection	
	PRBS $2^n - 1$, n = 7, 9, 10, 11, 15, 23, 29, 31, 33, 35, 39, 41, 45, 47, 49, 51
	K28.3, K28.5, K28.7, CJPAT, CJTPAT, CRPAT, JSPAT, JTSPAT
	Clock $\div 2, \div 4, \div 8, ..., \div 64$
	User 1 bit to 8 Mb programmable using N4980A Multi-instrument Software
Data output configuration	Differential. May be operated single end with unused output terminated into 50 Ω.
	AC Coupled with internal bias tee
Data output amplitude	adjustable up to 1V pp single ended (option P17/32), 1.5V (option D17/D32), 3V (option H17/H32)
Rise time (20% to 80%)	16 ps typical (Options P17/P32/ D17/ D32), 12 ps typical (Options H17/H32)
De-emphasis	Option D17/D32 has integrated 5-tap de-emphasis
Jitter injection	
Sinusoidal SJ1, SJ2	1 to 200 MHz, up to 1UI
Random RJ	Up to 50 mUI
Periodic PJ	1 to 17 MHz, up to 100UI (to 62.5 kHz)
	SJ2, RJ requires N4960A controller with Option –CJ1

Error detector head specifications

Data rate range	4 to 17 Gb/s (Option E17)
	5 to 32 Gb/s (Option E32)
Pattern selection	
PRBS	$2^n - 1$, n = 7, 9, 10, 11, 15, 23, 29, 31, 33, 35, 39, 41, 45, 47, 49, 51
	K28.3, K28.5, K28.7, CJPAT, CJTPAT, CRPAT, JSPAT, JTSPAT
Clock	$\div 2, \div 4, \div 8, ..., \div 64$
User	1 bit to 8 Mb programmable using N4980A Multi-instrument software
Data output configuration	Differential. May be operated single end with unused output terminated into 50 Ω.
	AC coupled with internal bias tee
Data input range	100 mV to 1 V (p-p) single ended
Data delay range	± 2000 UI
Measurements	Instantaneous and accumulated BER, Error count, Errored 1's and 0's, Data loss, Sync loss. Multi-channel BER, bathtub scan, jitter tolerance testing (with N4980A software)

N4960A controller options

N4960A-CJ0	Standard jitter injection (single tone sinusoidal)
N4960A-CJ1	Expanded jitter injection (two tone sinusoidal, random and SSC)

Remote head options:

- N4951A-P17 pattern generator 17 Gb/s
- N4951A-P32 pattern generator 32 Gb/s
- N4951B-H17 pattern generator high amplitude 17 Gb/s
- N4951B-H32 pattern generator high amplitude 32 Gb/s
- N4951B-D17 pattern generator with 5-tap de-emphasis 17 Gb/s
- N4951B-D32 pattern generator with 5-tap de-emphasis 32 Gb/s
- N4952A-E17 error detector 17 Gb/s
- N4952A-E32 error detector 32 Gb/s

Agilent N4962A and N4963A Serial BERT 12.5G

Applications:
- Optical transceiver production test up to 10 Gb/s
- Communication component incoming inspection
- General device characterization up to 12.5 Gb/s

N4962A Serial BERT features
- Internal clock for 9.85 to 11.35 Gb/s operation
- 0.5 to 12.5 Gb/s operation with external clock
- Low-cost 10G production test solution

N4963A clock synthesizer features
- 0.5 to 13.5 GHz operation
- Jitter injection option
- 6 pairs of differential clock outputs

The Agilent Technologies N4962A Serial BERT 12.5 Gb/s is a small size, high-performance 0.5 to 12.5 Gb/s pseudo-random bit sequence generator and bit error rate tester designed for automated production-line testing, manufacturing and R&D lab use. The internal synthesizer offers performance from 9.85 to 11.35 Gb/s. When used in conjunction with an external clock (e.g., N4963A clock synthesizer 13.5 GHz), operation from 0.5 to 12.5 Gb/s is possible. The BERT and clock synthesizer's compact size and simple user interface making them ideal for use on a production test bench.

Specifications Agilent N4962A	
Data rate range	0.5 to 12.5 Gb/s with external clock
	9.85 to11.35 Gb/s with internal clock
PRBS patterns	$2^n - 1$, n=7, 10, 15, 23, 31
Data output amplitude range	300 to 1800 mVpp (single-ended)
Data output jitter	1.1 ps rms typ at 10 Gb/s
Data output rise/fall time (20 % to 80 %)	18 ps typ
Data input voltage range	0.1 to 2 Vpp (single ended)
Data input phase adjust	0 to 358 °
Data input/output configuration	Differential. AC coupled. May be operated single end without unused inputs/ outputs terminated into 50 Ω.

Specifications Agilent N4963A	
Frequency range	0.5 to 13.5 GHz
Channel 1,2 output amplitude	0.6 to 2.0 V from 0.5 to 7.5 GHz
	0.6 to 1.5 V from 7.5 to 13.5 GHz
Channel 3A, 3B, 4A, 4B output amplitude	0.2 to 0.8 V from 0.5 to 7.5 GHz
	0.2 to 0.6 V from 7.5 to 13.5 GHz
Phase adjust (Channel 1 only)	−180 to +178 °
Clock output configuration	Differential. May be operated single ended with unused output terminated into 50 Ω. Channel 1, 2 DC coupled. Channel 3A, 3B, 4A, 4B AC coupled.
Jitter injection	Sinusoidal 1 Hz to 200 MHz, up to 32 UI

Agilent N4965A Multi-Channel BERT 12.5G

All heads can operate with differential or single ended signal connections. Output parameters in the generator heads and input parameters in the error detector heads can be programmed independently, or ganged together for convenience. Presets for common logic families simplify user set up.

Key features

- Modular architecture supports 1 to 5 pattern generator or error detector heads
- Pattern generators included integrated two or four tap de-emphasis
- Programmable generator output/detector input parameters
- Transparent jitter pass-through
- Unique swept aggressor channel delay for crosstalk characterization
- BER, bathtub and jitter tolerance testing with N4980A
- Remote control through USB or GPIB
- Compact size

The Agilent N4965A multi-channel BERT 12.5 Gb/s is a modular, multi-channel signal integrity test system ideal for characterizing multi-lane serial data channels. By adding remotely mountable heads, each of its 5 channels can be configured as either a pattern generator, or error detector to form a bit error rate tester (BERT). Patterns available include various lengths of hardware generated PRBS, clock patterns, and DC logic 0 and logic 1.

Applications

- Serial data receiver characterization up to 12.5 Gb/s
- Multi-lane device characterization
- Crosstalk characterization

Multi-channel BERT controller (requires external clock signal e.g. N4963A clock synthesizer)	
Data rate range	1.0 to 12.5 Gb/s
Clock delay range (All channels)	0 to ±1000 UI
Delay sweep for crosstalk testing (All channels)	0, 1, 2, 4 UI pp

N4955A pattern generator remote head specifications	
Pattern selection:	
Clock	÷ N, where N = 2,4 (Option –P12), ÷ N, where N = 2, 4, 8, 16, 32, 64 (Option -D12)
Data output amplitude range	0.2 to 2.0 V single ended (Option -P12), 0.6 to 1.2 V single ended (Option -D12)
De-emphasis	2-tap: 1 post cursor, Range 0 to −20 dB (Option –P12)
	4-tap: 1 pre cursor, 2x post cursor (Option –D12)
	Range Pre: 0 to +8dB, post 1: 0 to −10 dB, Post 2: 0 to −8 dB
Data output configuration	Differential. May be operated single end with unused output terminated into 50 Ω. AC Coupled with internal bias tee.

N4956A error detector remote head specifications	
Pattern selection PRBS	$2^n - 1$, n = 7, 10, 15, 23, 31
Data input range	100 mV to 1 V (p-p) single ended
Data delay range	± 1000 UI
Data input configuration	Differential. May be operated single end with unused output terminated into 50 Ω. AC Coupled with internal bias tee
Measurements	Accumulated BER, error count, data loss, sync loss. Multi-channel BER, bathtub scan, jitter tolerance testing (with N4980A software)

N4965A controller options

- N4960A-CTR multi-channel BERT controller

Remote head options:

- N4955A-P12 pattern generator with 2-tap de-emphasis 12.5 Gb/s
- N4955A-D12 pattern generator with 4-tap de-emphasis 12.5 Gb/s
- N4956A-E12 error detector 12.5 Gb/s

Agilent N4967A 40Gb/s BERT System

The N4967A is an affordable and compact modular Serial BERT solution designed for device characterization, research and development testing, and general lab use. The N4967A consists of these main components:

- N4974A PRBS generator 44 Gb/s
- N4968A clock and data demultiplexer 44 Gb/s
- N4965A multi-channel BERT 12.5 Gb/s
- N4980A multi-instrument BERT software

Applications

Characterization of optical transceivers operating up to 44 Gb/s, such as:
- OTU OC-768/STM-256
- 100 Gb Ethernet
- InfiniBand EDR
- 32 G Fibre Channel (32GFC)
- 40 Gb/s backplanes, active optical cables
- CFP

Key features & Specifications

- Internal clock supports 40 Gb/s operation
- External half-rate clock input supports operation from 22 to 44 Gb/s
- True PRBS pattern generation at full data rate
- Supports differential or single ended inputs and outputs
- Fully supported in N4980A software

Agilent N4980A Multi-Instrument BERT Software
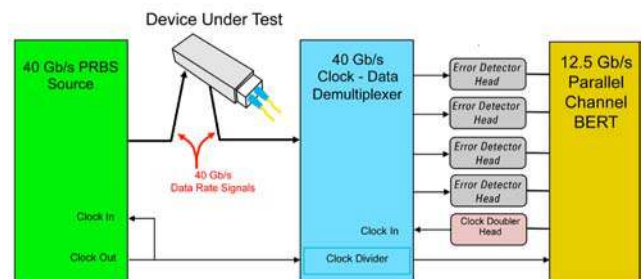
The Agilent N4980A multi-instrument BERT software provides the ability to control multiple instruments through a rich Windows®-based graphical user interface (GUI). Bit error rate measurements are simple to set up with the intuitive control screens. The software is ideal for setting up and performing parallel BER measurements and jitter tolerance testing (N4980A-JTS) in multi-lane and SERDES devices. You can also create your own patterns using the powerful editing tools built into the pattern editor to meet your unique requirements.

Key features & Specifications

- Software is Windows®-based controlling equipment through USB or GPIB
- Simple and fast setup
- Full instrument remote control
- Test single and multi-lane BER with active aggressor signals
- Monitor instantaneous BER over time or measure BER over a specific period
- Fast and efficient parallel jitter tolerance testing (N4980A-JTS)
- View BER-measured BERT scan (often called bathtub curve, a horizontal slice through eye)
- Intuitive pattern editor
- De-emphasis tap weight calculator for easy calculation of required tap settings and programming to supported de-emphasis pattern generators

Applications

- Serial data receiver characterization
- Parallel BER measurements
- N4980A-JTS for jitter tolerance testing
- Optical transceiver/transponder characterization

The N4980A multi-instrument BERT software provides easy-to-use control panels for the following instruments:

- N4965A multi-channel BERT 12.5 Gb/s
- N4962A serial BERT 12.5 Gb/s
- N4963A clock synthesizer 13.5 Gb/s
- N4960A serial BERT 32 and 17 Gb/s

The base software is available free of charge (registration required for download). The N4980A-JTS jitter tolerance measurement package is an option enabled by a software key.

Agilent N4970A PRBS Generator and N4984A Clock Divider Products

The Agilent Technologies N4970A PRBS generator 10 Gb/s is a self-contained 10 Gb/s pseudo random bit sequence (PRBS) generator. The N4970A PRBS generator 10 Gb/s can be configured to use an external clock source allowing operation from 50 Mb/s to 12.5 Gb/s. Five different PRBS pattern lengths and three mark density ratios are available via user selectable jumpers.

Key features & Specifications
- Wide operating range, from 50 Mb/s to 12.5 Gb/s
- Multiple output patterns: $2^n - 1$ where n= 7, 10, 15, 23, 31
- Fixed-frequency internal clock source
- Multiple mark density settings: ½, ¼, ⅛
- Differential outputs

Applications
- SONET/SDH
- 10 Gb/s ethernet
- Production testing

The Agilent Technologies N4984A clock dividers are general purpose test accessories designed for microwave communications and test applications. The inputs and outputs are AC-coupled. The dividers are self-contained and plug into standard AC power sources.

The N4984A-040 clock divider 40 GHz simultaneously provides divide-by-2, divide-by-4, and divide-by-8 outputs. The single-ended input is accessed from the rear via a 2.9 mm connector while the outputs are provided at the front panel via SMA connectors.

The N4984A-020 clock divider 20 GHz provides divide-by-1, divide-by-2, divide-by-4, or divide-by-8 output, set by selectable jumpers on the rear panel. Inputs and outputs are differential.

Key features & Specifications
- Wide frequency range: up to 40 GHz
- High input sensitivity
- Very low jitter
- Fast rise/fall times
- Divide-by- 1/2/4/8 outputs
- AC power supply included
- Size: 3.5" x 4.0" x 1"

Applications
The N4984A dividers can be used to extend the trigger range of high speed sampling oscilloscopes. Precision timebase measurements will benefit from the very low added jitter and fast waveform edges. The N4984A can be used to generate synchronized, high frequency clocks from existing sinusoidal, synthesized sources. The low 1/f phase noise characteristics of the dividers will benefit high frequency phase lock loop designs.

Agilent N4974A and N4975A PRBS Generators

The Agilent Technologies N4974A PRBS generator 44 Gb/s is a self-contained pattern generator capable of operating at either a single fixed-frequency bit rate using the internal oscillator or operating over a wider frequency range when used with an external half-rate clock source. The N4974A PRBS generator 44 Gb/s operates from 22 to 44 Gb/s when used with an external clock or at 39.81312 Gb/s when used with the internal oscillator. The generator is also available with two more internal oscillator choices, operating at either 25.78125 or 28.0 Gb/s.

Key features & Specifications

- 40, 28, or 25 Gb/s data rates with internal fixed frequency clock
- 22 to 44 Gb/s data rates with external clock
- Excellent eye quality — rise/fall time < 8 ps typ
- Patterns $2^n - 1$; n = 7, 15, 31
- 1000 mV differential output
- Ultra low noise trigger for precision time base applications
- Pattern trigger output

Applications

- Ultra-high speed communications components testing
- Stimulus response measurements for 40 Gb/s components
- Backplane signal integrity
- Optical transceiver characterization

The Agilent Technologies N4975A PRBS generator 56 Gb/s is a fully self-contained 56 Gb/s pattern generator. The N4975A is designed to provide an excellent quality "eye" through comprehensive integration of key building blocks into monolithic integrated circuits founded on SiGe technology.

Key features & Specifications

- Operates at 56 Gb/s with internal clock or from 39.8 to 56 Gb/s with external clock source
- Self-contained PRBS generator
- Excellent eye quality, fast rise and fall time
- Built-in quarter-rate clock source (14.0 GHz)
- 1010, 1100, and $2^{15} - 1$ patterns
- 500 to 1000 mV, adjustable differential output
- Quarter and half rate clock outputs
- Pattern trigger output

Applications

- CEI 56G-VSR advanced research
- Characterizing 56 G, 40 G, and 25 G optical transceivers and components
- General high speed serial link characterization

Agilent N4903B J-BERT High-Performance Serial BERT

- Operates from 150 Mb/s to 7, 12.5 or 14.2 Gb/s
- Built-in calibrated and compliant jitter sources for RJ, PJ1, PJ2, SJ, BUJ
- Interference channel with sinusoidal interference and switchable ISI traces
- Automated jitter tolerance, compliance curve and characterization
- Second output channel with independent PRBS and pattern memory
- Built-in tunable CDR
- Half-rate clock with variable duty cycle, sub-rate clock outputs

J-BERT N4903B high-performance serial BERT

Complete receiver jitter tolerance

J-BERT provides built-in and calibrated jitter sources for the most accurate jitter tolerance testing of receivers used in many popular multigigabit serial bus interfaces.

It is used by R&D and test engineers in the semiconductor, computer, and communication industry to characterize new designs and verify standard compliance.

J-BERT supports testing of embedded and forwarded clock architectures for data rates up to 14.2 Gb/s.

Long-term investment

J-BERT is configurable for today's test and budget needs but allows retrofit of all options when test needs change.

Key applications

- Receiver jitter tolerance
- PCI Express, USB3, SATA, SAS, DisplayPort
- Forwarded clock interfaces: QPI
- Fibre Channel
- XFP, SFP, SFP+, 10 GbE, XAUI, 100 GbE (10 x 10 Gb/s)
- Backplanes: CEI, 10 GBASE-KR, 100 GBASE-KR4

Measurement suite

- BER, accumulated, interval; symbol/frame error ratio (Option A02); bit recovery mode (Option A01); pattern capture
- BERT scan, "bathtub" curve including RJ, DJ, TJ separation
- Output level, Q-factor, eye-diagram with BER contour and eye masks
- Fast eye mask, spectral jitter, error location capture, fast TJ

Specifications

Pattern generator

- Operation range: 620 Mb/s[1] to 7 Gb/s (Option C07 or G07), to 12.5 Gb/s (Opt C13 or G13), to 14.2 Gb/s (Opt G13 + D14 or C13 + D14)
- Data outputs: 1 or 2 (Option 002), differential or single-ended
- Output amplitude: 0.1 to 1.8 Vpp
- Jitter: < 9 ps pp
- Transition time: < 25 ps (10 to 90 % and ECL levels)
- Cross point adjust: 20 to 80 %
- Pattern: PRBS $2^n - 1$, n = 7, 10, 11, 15, 23, 31
- Memory: 32 Mbit and pattern sequencing (up to 120 blocks)
- Delay control input: Up to 220 ps for external jitter injection
- [1] 150 Mb/s when using external clock source

Jitter tolerance test

- Built-in, calibrated jitter sources (Option J10): RJ up to 15.7 ps rms @ 1 GHz, PJ1+2 up to 620 ps @ 300 MHz, SJ multiple Uls up to 5 MHz, BUJ up to 220 ps, according CEI
- SSC (Option J11): Triangular and arbitrary modulation, up to 5000 ppm @ 0.1 to 100 kHz
- Interference channel (Option J20): ISI by switchable board traces, sinusoidal interference (vertical eye closure) common and differential mode up to 400 mV @ 3.2 GHz

Error detector

- Ext. Clock: 150 Mb/s to 7 Gb/s (Opt. C07) or 12.5 Gb/s (Opt. C13)
- Data input: 1, differential or single-ended
- Clock recovery: always incl., variable loop bandwidth 0.5 to 12 MHz
- Sensitivity: < 50 mV

Ordering information

- N4903B high-performance serial BERT with several accessories.
- N4903B-C07/C13 BERT with max. data rate 7/12.5 Gb/s
- N4903B-G07/G13 pattern generator w/ max. data rate 7/12.5 Gb/s
- N4903B-D14 data rate extension for pattern generator to 14.2 Gb/s
- N4903B-002 PRBS and pattern on aux data output (2nd output ch)
- N4903B-003 half-rate clock with variable duty cycle
- N4903B-J10 jitter sources (PJ1, PJ2, SJ, RJ, sRJ, BUJ)
- N4903B-J11 SSC, residual SSC
- N4903B-J12 jitter tolerance compliance suite
- N4903B-J20 interference channel
- N4903B-A01 bit recovery mode
- N4903B-A02 SER/FER analysis
- N4903B-UAB upgrade from N4903A

All options are upgradeable

www.agilent.com/find/cdr
www.agilent.com/find/n4876

N4877A, N1075A: Electrical and optical clock recovery solution for BER and waveform analysis

- Continuous, un-banded tuning from 50 Mb/s to 32 Gb/s
- Ultra low residual jitter: < 100 femtoseconds rms
- Golden PLL operation with a tunable loop bandwidth from 30 kHz to 20 MHz for configurable standard compliant test
- PLL BW/jitter transfer and phase noise/jitter spectrum analysis

Both bit-error-ratio-testers (BERTs) and DCA's require a clock signal to synchronize the measurement system to the incoming data stream. When the necessary synchronous clock/trigger is not available, a common solution is to derive a clock from the data being measured. The 83496B clock recovery module for the 86100D and N4877A/N1070A standalone clock recovery instrument provide ideal performance for waveform analysis and BER test.

They can derive a clock from NRZ signals with rates as low as 50 Mb/s, as high as 32 Gb/s, and any rate between, providing the ultimate in flexibility and value. With jitter as low as 100 fs rms, the residual jitter of the output clock is virtually negligible, allowing accurate measurements of very low levels of signal jitter and high margin in jitter tolerance/receiver tests.

- The 83496B operates from 50 Mb/s to 14.2 Gb/s and can be configured for both optical and electrical signals
- The N4877A and N1070A operate from 50 Mb/s to 32 Gb/s and provide clock, auxiliary clock, and demultiplexed data outputs
- The N4877A operates on electrical signals, while the N1070 adds an optical coupler/converter box allowing analysis of both optical and electrical signals

PLL and jitter spectrum analysis

Use 86100CU-400 software to make fast, accurate and repeatable measurements of phase-locked loop (PLL) bandwidth/jitter transfer. With a precision jitter source, the 83496B, N4877, and N1070A can be configured as a jitter receiver to create a PLL stimulus-response test system.

Specifications

- Data rates: 50 Mb/s to 32 Gb/s, continuously tunable
- Tunable loop bandwidth up to 20 MHz
- Optical inputs: MMF to 16 Gb/s, SMF to 32 Gb/s
- Residual jitter as low as 100 fs rms
- Demultiplexed data (outputs can be swapped)
- Recovered clock can be divided by 1, 2, 4
- Input sensitivity: 25 mV differential, 50 Ω

N4876A 28.4 Gb/s multiplexer 2 : 1

- Extends the pattern generator data rate to up to 28.4 Gb/s
- Transparent for timing jitter
- Operation via J-BERT user interface or as stand-alone

Accurate characterization up to 28 Gb/s

The N4876A 28 Gb/s multiplexer allows to extend the pattern generator data rate of the J-BERT N4903B and ParBERT 81250A up to 28.4 Gb/s. Design and test engineers in the semiconductor, communications, storage and computer industry can now accurately characterize the next generation of serial interfaces. N4876A is transparent to jitter, so when using it with the J-BERT N4903B, calibrated RJ and PJ can be generated.
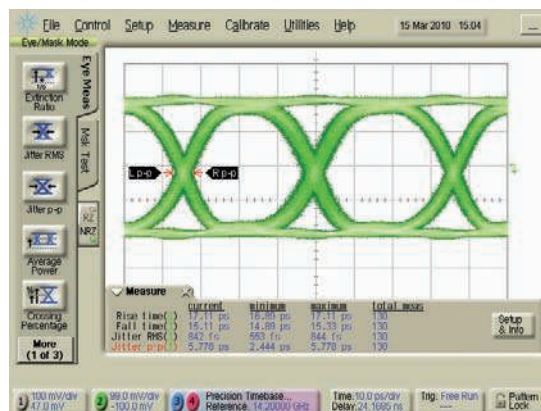
28.4 Gb/s PRBS output signal of multiplexer N4876A

Target applications

- IEEE 802.3 ba 100 GBASE-LR4, -ER4 interfaces operating at data rates of 25.78125 Gb/s, T11 16G or 32G Fibre Channel
- OIF CEI backplanes operating between 19.9 and 28 Gb/s
- Clean generator for transmitter test
- Stressed generator for receiver tolerance testing

Specifications

- Output data rate: 1.25 to 27.0 Gb/s (28.4 Gb/s when using J-BERT N4903B Option D14)
- Output amplitude: 0.05 to 1.800 V in a −2 to +3 V window
- Intrinsic jitter: 1 ps rms typ. for clock pattern
- Transition time: 10 ps typ. (20 to 80%), Crossing point: 20 to 80%
- Clock/2 jitter: 45 to 55% shorter/longer even bits than odd bits
- Output: Differential or single-ended, 50 Ω

ParBERT 81250 Parallel Bit Error Ratio Tester

- Different modules covering a range of data rates from 333 kb/s to 13.5 Gb/s
- Up to 66 synchronous pattern generator and analyzer channels
- Powerful pattern sequencer providing looping and branching on events enabling control of complex tests and devices
- PRBS/PRWS and memory based patterns up to 64 Mb
- Delay control input for jitter generation
- Error detector modules featuring individual CDR
- Measurement suite

The ParBERT 81250 parallel bit error ratio tester provides extremely fast parallel BER testing for high-speed digital communication ports, components, chips or modules. ParBERT is a modular, flexible and scalable platform with comprehensive software and measurement suite suited for many applications in the semiconductor, computer, storage, communications and consumer industry.

Applications
- R&D characterization and compliance testing of single and multi-lane receiver and transmitter ports
- Manufacturing test of multiple devices in parallel MUX, DeMUX testing
- A/D, D/A converter testing
- Multi-lane computer buses: PCI Express, HDMI, MIPI, CPU-frontside buses such as QPI, memory buses such as AMB, SMI
- Communication interfaces: PON ONU/OLT, IEEE 802.3 xx (10 GbE, 40 GbE, 100 GbE) , XAUI, SONET/SDH, SFI-4, SFI-5, CEI backplanes, Fibre Channel

Powerful pattern sequencing
Run complex tests with a variety of test patterns in one shot without stopping the instrument for pattern download is enabled through the powerful ParBERT 81250 pattern sequencer with its up to five nested loop levels and branching on external and internal events or upon programming command.

Configurable with multiple bit rates and channels
Modules for four speed-classes are available for the ParBERT 81250 System that cover data generation and analysis from 333 kb/s up to 13.5 Gb/s. Users can configure the number of analyzer and generator channels independently. Each channel can be programmed with individual level, pattern and timing parameters. Once purchased in a certain configuration ParBERT 81250 can easily be extended to fit future needs protecting investment over a long timeframe.

Real-time analysis of multiple lanes
The ParBERT analyzers can automatically synchronize the incoming data stream. ParBERT offers a comprehensive measurement suite:

- BER measurement (one-/zero errors, accumulated errors...)
- Fast eye mask measurement (mask test with pass/fail)
- DUT output timing measurement (RJ, DJ, TJ, phase margin)
- Spectral decomposition of jitter (spectral jitter analysis)
- DUT output level measurement (high/low level, amplitude, Q-factor)
- Eye opening (3-dimensional eye analysis voltage-time-BER)

Receiver jitter tolerance
The ParBERT generator modules with 13.5/7/3.35 Gb/s data rates offer jitter injection capabilities via the external delay control input. This allows in depth receiver jitter tolerance analysis.
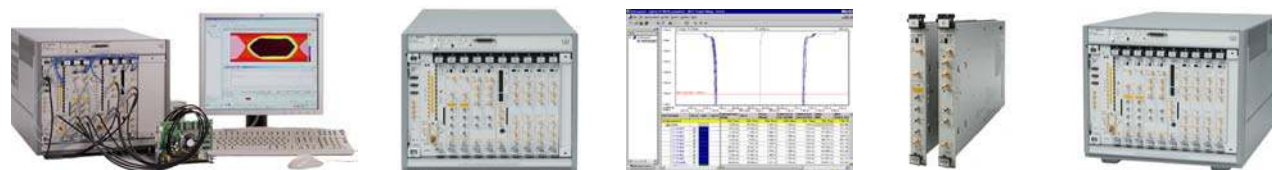
- Standard measurements at rates between 125 Mb/s and 3.125 Gb/s
- Generation of pseudo random bit sequence (PRBS) polynomials and a K28.5 pattern at low voltage differential signal (LVDS) or emitter coupled logic (ECL) levels
- Flexible connections to the device under test via 3.5 mm differential electrical coax connectors and/or standard optical
- SFP module plug-ins
- Optical and electrical error injection once or at selectable bit error ratio (BER)
- Analysis of gated BER with display of the absolute number of errors and selectability of gate time
- Dramatically simplified transceiver measurements that provide just the essential tests via the one page graphical user interface (running on an external Windows XP PC via a USB 2.0 interface)
- Full programmability of all graphical user interface features from another software program

The Agilent N5980A 3.125 Gb/s serial BERT is ideal for manual or automated manufacturing test of electrical and optical devices running at speeds between 125 Mb/s and 3.125 Gb/s. It addresses all common standard speeds via selectable bit rates.

Easy-to-use and cost efficient

The software user interface has one standard or one advanced screen to ensure intuitive use for operators. It makes the instrument easy to use and easy to learn.

Twice the measurement throughput

By using both the electrical and optical (SFP) interfaces concurrently, you can double your measurement throughput (electrical in/optical out and vice versa).

Automation made easy

The remote programmability of the user interface, using SCPI – syntax, makes it simple to integrate the N5980A into other programs.

PRBS, K28.5 pattern or clock generation and integrated clock data recovery

The N5980A can generate standard PRBS polynomials, K28.5 ('Comma') characters and different sub-rate clocks (/2 to /20). It can also inject errors with an adjustable error ratio. The receiver has a clock-data recovery (CDR) built-in and differential inputs (SMA) for signals from 50 mVpp to 2 Vpp amplitude.

Standard (SFP) optical module plug-in

The instrument has a standard SFP – female connector. This enables all different kind of user-selectable optical modules e.g for multimode/single-mode fiber at 850, 1310 and 1550 nm for the test set-up.

Specifications

Data rates
- Fast Ethernet: 125 Mb/s
- OC-3: 155.52 Mb/s, OC-12: 622.08 Mb/s, OC-48: 2.48832 Gb/s
- OC-48 with FEC: 2.66606 Gb/s
- 1 x FC: 1.0625 Gb/s, 2 x FC: 2.125 Gb/s
- 1 x Gb Ethernet: 1.25 Gb/s
- XAUI: 3.125 Gb/s
- Accuracy: ±50 ppm

Pattern generator
Pattern
- PRBS: $2^7 - 1$, $2^{15} - 1$, $2^{23} - 1$, $2^{31} - 1$
- Data pattern: K28.5
- Clock pattern: Data rate divide by n, n = 2, 4, 8, 10, 16, 20
- The pattern can be individually adjusted for pattern generator electrical out and optical out

Error injection
- Fixed electrical and optical error inject
- Fixed error ratios of 1 error in 10^n bits, n = 3, 4, 5, 6, 7, 8, 9
- Single error injection
- Separate error ratios can be adjusted for pattern generator electrical out and optical out

Pattern generator electrical out
A differential electrical output is provided on the front-panel

Output amplitude
ECL: 850 mVpp typ., single-ended/1700 mVpp typ., differential
LVDS: 400 mVpp typ., single-ended/800 mVpp typ., differential
Jitter: 0.05 UI typ. @ OC-12, 0.08 UI typ. @ GbE, 0.15 UI typ. @ OC-48

Pattern generator optical out
- A standard SFP housing is provided
- Minimum number of insertion/deinsertion cycles: 200

Error detector
- A differential electrical input is provided on the front-panel
- Data rate is the same as pattern generator
- Pattern: PRBS: 2^7-1, $2^{15}-1$, $2^{23}-1$, $2^{31}-1$
- Data input: Differential AC coupled
- Max. input amplitude: 1 Vpp, single-ended, 2 Vpp, differential
- Clock data recovery: Internal CDR
- Impedance: 100 Ω nominal, Sensitivity: < 50 mV
- Synchronization: Automatically on level, polarity, phase, bit and pattern

- Excellent price/performance ratio
- Variable bit rates up to 3.6 or 12.5 Gb/s
- < 25 ps transition time
- < 50 mV pp input sensitivity
- Fast eye mask measurement for pass/fail testing (Option 101)
- True differential data generation and analysis capability
- Enhanced measurement suite (Option 101)
- Integrated clock data recovery (Option 102)
- Small form factor saves bench or rack space
- LAN, USB, GPIB for remote control
- Compatibility with existing remote commands, e.g. Agilent 71612, 86130A Series and N4900 Series
- Applications: Manufacturing test, telecom transceivers such as SONET/SDH Fibre Channel, 10GbE, XFP/XFI, PON-OLT's and high-speed serial computer buses

The serial BERT N4906B is a general-purpose bit error ratio tester, designed for testing high-speed digital communication components and systems. It is ideal for cost-effective manufacturing and telecom device testing. It offers a 3.6 or 12.5 Gb/s pattern generator and error detector with excellent price/performance ratio.

Transition times < 25 ps allow precise measurements. The analyzer can be configured with CDR to test clockless interfaces and with true differential inputs to test LVDS and other differential interfaces.

The compact size of the N4906B saves rack space; LAN, USB and GPIB interfaces allow smooth integration into automated test environments. For bench users the N4906B serial BERT offers an intuitive user interface with state-of-the-art Windows-XP based touch-screen.

Deeper insight into the device's performance can be obtained with the enhanced measurement suite. It offers many valuable signal analysis tools, such as BERT scan (so-called bathtub curves) with total jitter and its separation into RJ and DJ, eye contours, spectral jitter decomposition and more.

Specifications

Pattern generator
- Operation range:
  - 9.5 to 12.5 Gb/s (Option 012)
  - 150 Mb/s to 12.5 Gb/s (Option 102)
  - 150 Mb/s to 3.6 Gb/s (Option 003)
- Data output: 1, differential or single-ended
- Output amplitude: 0.10 to 1.8 V in 5 mV steps
- Jitter: 9 ps pp typical
- Transition time: < 25 ps (10 to 90 % and ECL levels)
- Cross point adjust: 20 to 80 %

Pattern
- PRBS $2^n - 1$, n = 7, 10, 11, 15, 23, 31
- User-definable memory: 32 Mbit

Error detector
- Operation range:
  - 9.5 to 12.5 Gb/s (Option 012)
  - 150 Mb/s to 3.6 Gb/s (Option 003)
  - 150 Mb/s to 12.5 Gb/s (Option 102)
- Data input: 1, single-ended or differential (Option 101 or 003)
- Delay adjust: 1.5 ns
- Clock data recovery (Option 102):
- 1.058 to 1.6 Gb/s: Loop bandwidth 1 MHz typ.
- 2.115 to 3.2 Gb/s: Loop bandwidth 2 MHz typ.
- 4.23 to 6.4 Gb/s: Loop bandwidth 4 MHz typ.
- 9.9 to 10.9 Gb/s: Loop bandwidth 8 MHz typ.
- Sensitivity: < 50 mV

Measurements
- BER
- Fast eye mask measurement with pass/fail (Option 101)
- BERT scan with RJ/DJ separation (Option 101)
- Fast total jitter (Option 101)
- Spectral jitter decomposition (Option 101)
- Eye contour (Option 101)
- Output level (Option 101)
- Error location capture (Option 101)

- Calibrated injection of OMA (optical modulation amplitude), ER (extinction ratio), and VECP (vertical eye closure penalty) for accurate results
- Supports multiple standards: 10 Gb Ethernet -LR, -ER, -SR, 8 GFC, 10 GFC
- Automated BER versus OMA measurement saves engineering time
- Reproducible results with Agilent proven and complete accessory kits
- Affordable with one reference transmitter for 1310 and 1550 nm, single-mode
- Reference transmitter for 850 nm, multimode
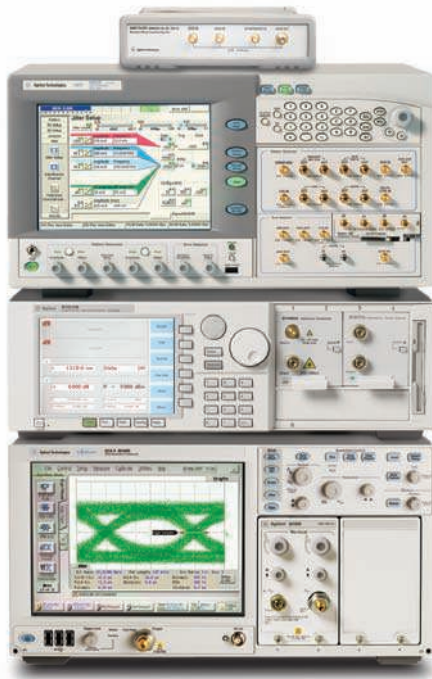
Complete optical receiver stress test solution for robust designs

The Agilent N4917A provides repeatable and calibrated characterization and conformance test results. Design and test engineers can now accurately test optical transceivers and ROSAs up to 14.2 Gb/s.

Complete, calibrated and repeatable stress test of optical receivers

- Optical transceivers and ROSAs (receive optical sub assemblies) up to 14.2 Gb/s
- 10 Gb Ethernet, Fibre Channel
- Compliance test and characterization
- R&D and test of optical storage and communication devices

Calibrated injection of ER, OMA and VECP

The N4917A automation and calibration software controls all instruments and allows the user to enter compliant ER, OMA and VECP.

Automated conformance and charactization tests

Engineers save programming and test time with the automated BER versus OMA measurements.

Reproducible test results

The values of VECP, OMA and ER are calibrated with the 86100C/D Infiniium DCA controlled by the N4917A automation and calibration software. Reproducible test results, even across different test sites are now possible when using the Agilent verified accessory kits including all filters, adapters and cables required.

Affordable solution for 850, 1310 and 1550 nm

The Agilent 81490A reference transmitter supports 850 nm multimode fibers and 1310/1550 nm single-mode fibers, reducing the amount of test equipment needed when testing devices for multiple standards.

Calibration and automation software N4917A

This software controls all instruments required to run the optical receiver stress test. It guides the user through the instrument set-up and calibration procedure with the 86100C/D Infiniium DCA.
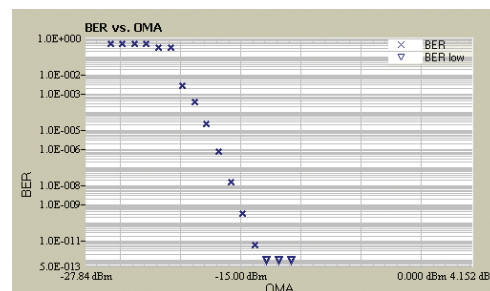
The user interface allows the user to choose between standard compliant stress testing or custom stressed eye values for ER, OMA, sinusoidal interference and sinusoidal jitter. Automated BER versus OMA measurements can be made and displayed as a graphical result screen and documented in a test report.

The N4917A software runs on the J-BERT N4903A/B or on an external Windows XP PC.

Optical receiver stress test solution consists of:

- Calibration and automation software with accessory kits for 10GbE and 8G/10G Fibre Channel N4917A
- Lightwave measurement system frame 8164B with:
  - Reference transmitter:
      81490A-135 for 1310/1550 nm for single-mode fiber
      or
      81490A-E03 for 850 nm, multimode fiber
  - Optical attenuator 81576A or 77-Series
- J-BERT N4903A/B -C13, -J10, -J12, -J20
- Digital communication analyzer 86100C/D with 86105B/C/D

The 86100 series digital communications analyzer is the industry standard for characterizing high-speed transmitter waveforms. Integrated, calibrated optical reference receivers coupled with built-in automated compliance software are the key to accurate measurements.

The 86100D DCA-X has been engineered for unmatched accuracy, insight, and ease-of-use. In addition to providing industry leading signal integrity measurements, the DCA-X provides:

Accurate characterization of optical waveforms

The 86100D is the ideal tool for viewing optical transceiver signals. A variety of plug-in modules are available with built-in optical receivers allowing the highest accuracy in waveform analysis. Industry standard reference receivers provide the correct frequency response to validate compliance to SONET/SDH, Ethernet, Fibre Channel and other specifications. Select from several plug-in modules to get the configuration that best matches your transceiver applications. Built-in test applications provide the following measurements:

- Automatic testing to industry standard eye masks
- Accurate measurement of eye-diagram parameters including extinction ratio, eye-height and width, crossing percentage etc.
- Fast throughput and simultaneous multiple channel testing for extremely low cost-of-test
- Simultaneous parallel mask test for up to 16 channels with up to 64 parametric measurements

Powerful new INSIGHT

- Integrated de-embedding/embedding capability (using 86100D-SIM InfiniiSim-DCA license)
- Advanced signal processing such as filtering, FFT, differentiate and integrate functions
- New measurement capability, including Data Dependent Pulse Width Shrinkage (DDPWS), uncorrelated jitter (UJ), J2, J9 and more…

Improved USABILITY

- Dual user interface:
  - FlexDCA — a new customizable vector-based user interface for scope, eye, and jitter measurements
  - DCA-J "classic" user interface for 100% backwards compatibility
- Customizable user-interface
- Display up to 64 measurements simultaneously
- ONE button setups

Improved PRODUCTIVITY

- Built-in waveform simulator with random/periodic jitter and noise generator
- Live or offline signal analysis (using N1010A FlexDCA remote access software)

NEXT GENERATION platform

- Supports up to 16 channels for testing high density ASIC/FPGA testing and parallel designs. New option 86100D-PTB integrates the precision timebase within the mainframe allowing ultra-low jitter for up to 16 channels.
- Vertical gain and offset controls that can be assigned to all channels and functions
- User-defined multi-purpose button
- User-defined analog control knob
- 3X faster CPU than DCA-J
- 100% backwards compatibility with all DCA modules

Improves margins and helps to differentiate products for a wide range of applications such as:

- Transceiver design and manufacturing
- ASIC / FPGA / IC design and characterization
- Signal integrity measurements on Serial bus designs
- Cables, Printed Circuit Boards (PCB)

Precision measurements on high-speed signals at the touch of one button!

- Scope mode yields the most accurate waveform measurements
- Eye/Mask mode provides fast and accurate compliance testing of transceivers
- TDR/TDT mode for precision impedance measurements with S-parameter capability. TDR edge speed faster than 10 ps with >50 GHz BW.
- Jitter and amplitude mode for comprehensive analysis of signal characteristics

Powerful analysis features provide greater insight

- Integrated de-embedding, embedding, and equalization capability
- Jitter spectrum and phase locked loop (PLL) analysis
- Jitter analysis on long patterns such as PRBS31 (using option 401)
- Custom measurements and analysis using The MathWorks MATLAB software

Lowest cost of test

- Modular platform supports up to 16 parallel channels
- Optimized algorithms designed for manufacturing test
- Modular – buy only what you need today knowing you can upgrade later
- Protect your investment — the 86100D is 100% compatible with all DCA modules

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Scope mode
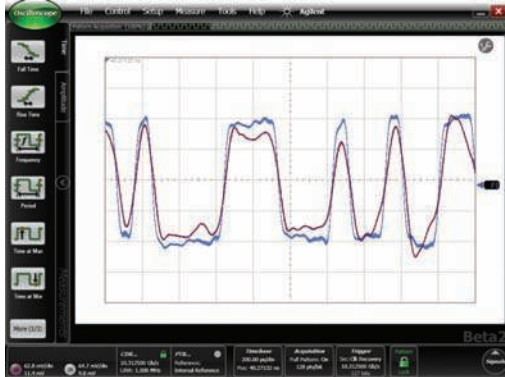
High-fidelity waveform characterization (Purple: raw trace, Blue: de-embedded waveform)

Jitter mode

Precision jitter, amplitude, and frequency analysis capability

Eye/Mask mode
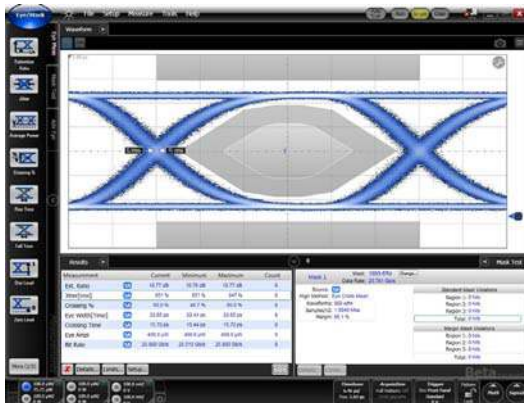
Fast transmitter characterization using eye-diagram analysis and automated mask margin measurements

TDR/TDT mode
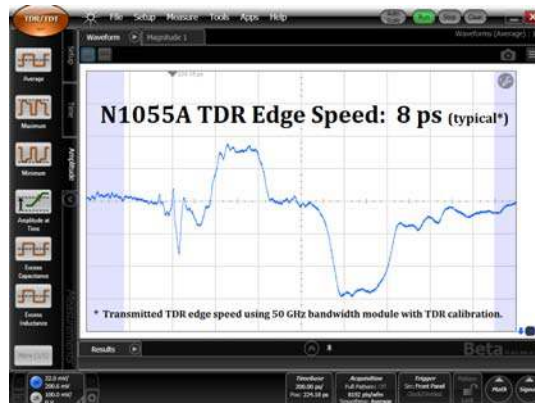
Accurate time domain reflectometry/transmission and S-parameter measurements

Precision measurements, more margin, and more insight

The 86100D DCA-X oscilloscope combines high analog bandwidth, low jitter, and low noise performance to accurately characterize optical and electrical designs from 50 Mb/s to over 80 Gb/s. The mainframe provides the foundation for powerful insight and measurement capability, such as de-embedding of cables and fixtures, that improve margins and allow engineers to see the true performance of their designs.

Modular

The modular system means that the instrument can grow to meet your needs, when you need it. There's no need to purchase capability that you don't need now. The DCA-X supports a wide range of modules for testing optical and electrical designs. Select modules to get the specific bandwidth, filtering, and sensitivity you need. The DCA-X supports all modules in the DCA family and is 100% backwards compatible with the 86100C mainframe.

Software

The DCA-X provides powerful analysis capability that is enabled through licensed software options. Examples include 86100D-200 for fast and accurate jitter analysis, and 86100D-SIM for de-embedding and/or embedding of fixtures and cables.

The 86100D DCA-X features two user interfaces for optimum ease-of-use. It includes the classic DCA interface for complete backwards compatibility with earlier DCA mainframes. It also includes the new FlexDCA interface that provides new measurements and powerful analysis capability in a fully customizable application.

The following measurements are available from the tool bar, as well as the pull down menus. The available measurements depend on the DCA-X operating mode.

Oscilloscope mode

Time

Rise Time, Fall Time, Jitter RMS, Jitter p-p, Period, Frequency, + Pulse Width, − Pulse Width, Duty Cycle, Delta Time, [Tmax, Tmin, Tedge—remote commands only]

Amplitude

Overshoot, Average Power, V amptd, V p-p, V rms, V top, V base, V max, V min, V avg, OMA (Optical Modulation Amplitude)

Eye/Mask mode

NRZ eye measurements

Extinction ratio, Jitter RMS, Jitter p-p, Average Power, Crossing Percentage, Rise Time, Fall Time, One Level, Zero Level, Eye Height, Eye Width, Signal to Noise, Duty Cycle Distortion, Bit Rate, Eye Amplitude

RZ eye measurements

Extinction Ratio, Jitter RMS, Jitter p-p, Average Power, Rise Time, Fall Time, One Level, Zero Level, Eye Height, Eye Amplitude, Opening Factor, Eye Width, Pulse Width, Signal to Noise, Duty Cycle, Bit Rate, Contrast Ratio

Mask test

Open Mask, Start Mask Test, Exit Mask Test, Filter, Mask Test Margins, Mask Margin to a Hit Ratio, Mask Test Scaling, Create NRZ Mask

Advanced measurement options

The 86100D's software options allow advanced analysis.
Options 200, 201, and 300 require mainframe Option ETR.
Option 202 does not require mainframe Option ETR.
Option 401 does not require Options ETR and 200 unless a DDPWS measurement is required.

Option 200 enhanced jitter analysis software

Measurements

Total Jitter (TJ), Random Jitter (RJ), Deterministic Jitter (DJ), Periodic Jitter (PJ), Data Dependent Jitter (DDJ), Duty Cycle Distortion (DCD), Intersymbol Interference (ISI), Sub-Rate Jitter (SRJ), Asynchronous periodic jitter frequencies, Subrate jitter components.

FlexDCA adds the following measurements:

Data Dependent Pulse Width Shrinkage (DDPWS), Uncorrelated Jitter (UJ), J2, J9

Data displays

TJ histogram, RJ/PJ histogram, DDJ histogram, Composite histogram, DDJ versus Bit position, Bathtub curve (log or Q scale)

Option 201 advanced waveform analysis

Measurements

Deep memory pattern waveform, user-defined measurements through MATLAB interface

Data displays

Equalized waveform

Option 202 enhanced impedance and S-parameters

Option 300 amplitude analysis/RIN/Q-factor (requires Option 200)

Measurements

Total Interference (TI), Deterministic Interference (Dual-Dirac model, DI), Random Noise (RN), Periodic Interference (PI), and Inter-symbol Interference (ISI), RIN (dBm or dB/Hz), Q-factor

Data displays

TI histogram, RN/PI histogram, ISI histogram

Option 400 PLL and jitter spectrum measurement software

Jitter spectrum/phase noise measurements

Integrated Jitter: Total Jitter (TJ), Random Jitter (RJ), Deterministic Jitter (DJ); DJ Amplitude/Frequency, Jitter Spectrum Graph, Jitter versus Time Graph, Frequency versus Time Graph, Jitter Histogram, Post Processed Jitter Measurements, Phase Noise Graph dBc/Hz versus frequency

Phase Locked Loop (PLL) measurements

PLL bandwidth, PLL Peaking, Data Rate, Jitter Transfer Function (JTF) Graph, Observed Jitter Transfer (OJTF) Graph, JTF Model.

Option 401 advanced EYE analysis

Jitter measurements

Total Jitter (TJ), Random Jitter (RJ), Deterministic Jitter (DJ), J2 Jitter (J2), J9 Jitter (J9), Data Dependent Pulse Width Shrinkage (DDPWS)*
Requires 86100D-200

Amplitude measurements

Total Interference (TI), Random Noise (RN), Deterministic Interference (DI), Eye Opening

Mask test

Pass/Fail status, hits or hit ratio limits

Option 500 productivity package

Improve the efficiency of eye-diagram testing by 40% or more

Option SIM infiniiSim-DCA
2-port de-embedding and embedding; 4-port de-embedding and embedding; add simulated random jitter and noise

TDR/TDT mode (requires TDR module)
Quick TDR, TDR/TDT setup

Normalize, Response, Rise Time, Fall Time, Δ Time, Minimum Impedance, Maximum Impedance, Average Impedance (Single-ended and Mixed-mode S-parameters with Option 202)

Additional capabilities
Standard functions

Standard functions are available through pull down menus and soft keys, and some functions are also accessible through the front panel knobs

Markers

Two vertical and two horizontal (user selectable)

TDR markers
- Horizontal — Seconds or meter
- Vertical — Volts, ohms or percent reflection
- Propagation — Sielectric constant or velocity

Limit tests
- Acquisition limits
- Limit test "Run Until" Conditions — Off, # of Waveforms, # of samples
- Report action on completion — Save waveform to memory, save screen image

Measurement limit test
- Specify number of failures to stop limit test
- When to fail selected measurement — inside limits

Outside limits, always fail, never fail
- Report action on failure — Save waveform to memory, save screen image, save summary
- Mask limit test
- Specify number of failed mask test samples
- Report action on failure — Save waveform to memory, save screen image, save summary

Configure measurements
Thresholds
- 10%, 50%, 90% or 20%, 50%, 80% or custom

Eye boundaries
- Define boundaries for eye measurments
- Define boundaries for alignment

Format units for
- Duty cycle distortion — Time or percentage
- Extinction/Contrast ratio — Ratio, decibel or percentage
- Eye height — Amplitude or decibel (dB)
- Eye width — Time or ratio
- Average power — Watts or decibels (dBm)

Top base definition
- Automatic or custom

Δ Time definition
- First edge number, edge direction, threshold
- Second edge number, edge direction, threshold

Jitter mode
- Units (time or unit interval, watts, volts, or unit amplitude)
- Signal type (data or clock)
- Measure based on edges (all, rising only, falling only)
- Graph layout (single, split, quad)

Quick measure configuration

When using the classic DCA interface, "Quick Measure" measurements are initiated by pressing the <Multi-Purpose> button on the front panel.
- Four user-selectable measurements for Each Mode, Eye-mask, TDR, etc.
- Default Settings (Eye/Mask mode) Extinction Ratio, Jitter RMS, Average Power, Crossing Percentage
- Default Settings(scope Mode) Rise Time, Fall Time, Period, Vamptd

Histograms

Configure
- Histogram scale (1 to 8 divisions)
- Histogram axis (vertical or horizontal)
- Histogram window (adjustable window via marker knob)

Math measurements — Classic DCA user interface
- Four user-definable functions operator magnify, invert, subtract, versus, min, max
- Source — Channel, function, memory, constant, response (TDR)

Signal processing measurements — FlexDCA
- Math — Add, Subtract, Multiply, Average, Invert, Max, Min, Median
- Signal Processing — Difference (Differentiate), Summation (Integrate), Interpolation (Linear, Sin(x)/x), Filters: 4th Order Bessel, Butterworth, Gaussian
- Option — IRC allows extended operating range and improved frequency response of optical reference receivers
- Transforms — FFT, versus
- Equalizer (Opt 201) — Linear Feed-forward Equalizer (LFE, up to 64 taps)
- Simulation (Option SIM) — De-embedding, embedding, random jitter, random noise

Calibrate

All calibrations
- Module (amplitude)
- Horizontal (time base)
- Extinction ratio, probe, optical channel

Front panel calibration output level
- User selectable –2 V to 2 V

Touch screen configuration/calibration
- Calibration
- Disable/enable touch screen

Upgrade software
- Upgrade mainframe
- Upgrade module

Additional capabilities

Waveform autoscaling

Autoscaling provides quick horizontal and vertical scaling of both pulse and eye-diagram (RZ and NRZ) waveforms.

Gated triggering

Trigger gating port allows easy external control of data acquisition for circulating loop or burst-data experiments. Use TTL compatible signals to control when the instrument does and does not acquire data.

Easier calibrations

Calibrating your instrument has been simplified by placing all the performance level indicators and calibration procedures in a single high-level location. This provides greater confidence in the measurements made and saves time in maintaining equipment.

Stimulus response testing using the Agilent N490X BERTs

Error performance analysis represents an essential part of digital transmission test. The Agilent 86100D and N490X BERT have similar user interfaces and together create a powerful test solution. If stimulus only is needed, the 81133A and 81134A pattern generators work seamlessly with the 86100D.

Transitioning from the Agilent 83480A and 86100A/B/C to the 86100D

While the 86100D has powerful new functionality that its predecessors don't have, it has been designed to maintain compatibility with the Agilent 86100A, 86100B, 86100C and Agilent 83480A digital communications analyzers and Agilent 54750A wide-bandwidth oscilloscope. All modules used in the Agilent 86100A/B/C, 83480A and 54750A can also be used in the 86100D. Since the 86100D includes the classic DCA interface, the remote programming command set for the 86100D designed for the 86100A/B/C will work directly. Some code modifications are required when transitioning from the 83480A and 54750A, but the command set is designed to minimize the level of effort required.

SCPI programming tools for FlexDCA

To facilitate easier and faster remote code development, the FlexDCA user interface includes several SCPI programming tools. The SCPI recorder, for example, records user interaction (via the scope front panel, mouse, or touchscreen) and reports the equivalent SCPI remote-programming command to the user via a Record/Playback pop-up window.

IVI-COM capability

Interchangeable Virtual Instruments (IVI) is a group of new instrument device software specifications created by the IVI Foundation to simplify interchangeability, increase application performance, and reduce the cost of test program development and maintenance through design code reuse. The 86100D IVI-COM drivers are available for download from the Agilent website.

VXII.2 and VXII.3 instrument contro

The 86100D DCA-X provides LAN based instrument control.

The ultimate in accuracy and ease-of-use for analyzing high-speed electrical digital communications signals

Highest accuracy scope featuring:
- Ultra-low jitter < 50 fs (typ.)
- Wide bandwidth
  > 35 GHz (Option LBW)
  > 50 GHz (Option HBW)
- Clock-data delay mitigation ("0 ns" delay)

Easy setup and operation:
- Simple one connection 'triggerless' operation
- Auto setup for serial bus differential signaling including PCI-EXPRESS®, SATA, HDMI, DisplayPort, SFP+, 8 GFC, 10 GbE

PLL characterization / Jitter transfer:
- Flexible operation: Data or clock input/output, 50 Mb/s to 2 Gb/s or 25 MHz to 16 GHz
- Compliant: PCI SIG approved, SONET/SDH

Integrated hardware clock recovery:
- Continuous clock recovery rates:
  - 50 Mb/s to 16 Gb/s (Option 216)
  - 50 Mb/s to 32 Gb/s (Option 232)
- Adjustable loop bandwidth (LBW)/Type-2 transition frequency (Peaking)
  - "Golden PLL" loop bandwidth adjustment 15 KHz to 20 MHz (rate dependent)
  - Peaking 0 to > 2dB (bandwidth dependent)
- Exceeds industry standards for SSC tracking

The Agilent 86108B precision waveform analyzer is a plug-in module used with the 86100C/D DCA Wide-Bandwidth Oscilloscope. An optimum combination ultra-low jitter, low noise, and wide bandwidth makes the 86108B the ideal choice in helping engineers develop and test designs for PCI-EXPRESS®, SATA, SAS, HDMI, DisplayPort, SFP+, Fibre Channel, CEI, Gb Ethernet, and any proprietary rate to 32 Gb/s. The 86108B overcomes conventional test equipment limitations and provides designers with the confidence that the waveform displayed by the oscilloscope is a faithful representation of the true device performance for todays technologies as well a future generations.

New architecture yields precision measurements and easy-to-use operation

The 86108B combines two high-bandwidth channels, an instrumentation-grade clock recovery which features variable loop bandwidth and peaking, and a precision timebase into a single unit.
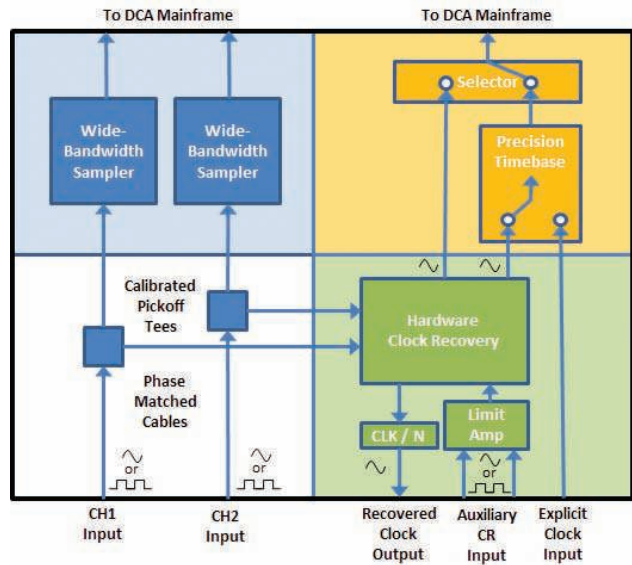
This combination results in the world's most accurate scope measurements available today. With setup similar to a real-time scope, it also provides significant ease-of-use advantages over traditional sampling scopes. The architecture virtually eliminates the trigger-sample delay inherent in most sampling instruments, and permits accurate and compliant measurement of large amounts of periodic jitter (e.g. SSC) without the use of specially matched cables which degrade performance.

PLL bandwidth, jitter transfer and jitter spectrum

The on-board phase detector of the 86108B allows for a precision measurement of phase-locked loop (PLL) bandwidth, sometimes referred to as jitter transfer. An external software application running on a PC controls the jitter source to provide a modulated stimulus to the device under test (DUT). The system is approved by the PCI SIG for PLL bandwidth compliance testing. The fast and flexible measurement can also test SONET/SDH and other PLL designs.

86100 family plug-in module matrix

The 86100 has a family of plug-in modules designed for a broad range of precision optical, electrical, and TDR/TDT measurements. The 86100 can accommodate up to 4 modules for a total of 16 measurement channels.

Module	Option	No. of optical channels	No. of electrical channels	TDR/TDT/S-parameters	Probe power[1]	Wavelength range (nm)	Unfiltered optical bandwidth (GHz)	Electrical bandwidth (GHz)	Fiber input (µm)	Mask test sensitivity (dBm)	155 Mb/s	622 Mb/s	1063 Mb/s	1244/1250 Mb/s	2125 Mb/s	2488/2500 Mb/s	2.666 Gb/s	3.125 Gb/s	4.25 Gb/s	5.00 Gb/s	6.25 Gb/s	8.50 Gb/s	9.953 Gb/s	10.3125 Gb/s	10.51875 Gb/s	10.664 Gb/s	10.709 Gb/s	11.096 Gb/s	11.317 Gb/s	14.025 Gb/s	25.80 Gb/s	27.70 Gb/s	28.025 Gb/s	39.813 Gb/s	41.250 Gb/s	43.018 Gb/s
86105C[6]	100[2]	1	1			750-1650	8.5	20	62.5	-20	•	•	•	•	•	•	•	•	•	•	•	•														
	200	1	1			750-1650	8.5	20	62.5	-16												•	•	•	•	•	•	•	•							
	300[2]	1	1			750-1650	8.5	20	62.5	-16	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•							
86105D[3,6]		1	1			750-1650	20	35	62.5	-12												•	•	•	•	•	•	•	•	•						
	100	1	1			750-1650	20	35	62.5	-12												•	•	•	•	•	•	•	•							
	200	1	1			750-1650	20	35	62.5	-12																				•						
	281	1	1			750-1650	34	50	62.5	-8																				•	•		•			
86115D[3,6]	002	2	0			750-1650	20		62.5	-12												•	•	•	•	•	•	•	•	•						
	102	2	0			750-1650	20		62.5	-12												•	•	•	•	•	•	•	•							
	142	2	0			750-1650	20		62.5	-12																				•						
	004[5]	4	0			750-1650	20		62.5	-11												•	•	•	•	•	•	•	•	•						
	104	4	0			750-1650	20		62.5	-11												•	•	•	•	•	•	•	•							
	144	4	0			750-1650	20		62.5	-11																				•						
	282	2	0			750-1650	34		62.5	-8																				•	•		•			
86116C[3,6]	025	1	1			1300-1620	45	80	9	-10																					•	•				
86116C[3,6]	041	1	1			1300-1620	65	80	9	-5																								•	•	•
54754A		0	2	•	•	N/A		18																												
86108A[3,4]		0	2		•	N/A		32																												
86108B[3,4]	LBW	0	2		•	N/A		35																												
	HBW	0	2		•	N/A		50																												
86112A		0	2			N/A		20																												
	HBW	0	2	•		N/A		30																												
86117A		0	2			N/A		50																												
86118A		0	2			N/A		70																												
N1045A		0	2-4			N/A		60																												
N1055A		0	2-4	•		N/A		50																												

1. Module has receptacle to supply power for external probe.
2. Pick any 4 rates (155 Mb/s to 6.25 Gb/s).
3. This module is not compatible with the 86100A and 86100B Digital Communication Analyzer (DCA) mainframes. If you would like to upgrade older DCA's contact Agilent Technologies and ask for current trade-in deals.
4. The 86108A/B uses all module slots.
5. 4 optical input ports are switched internally to 2 optical-to-electrical (O/E) converter
6. All modules with optical channels can use option -IRC to enhance the effective operating range. Reference receivers can be created at any rate within +/-50% of the hardware capability. IRC also corrects hardware imperfections to yield ideal reference receiver responses.

	120 MHz	165 MHz	330 MHz	330 MHz	400 MHz	660 MHz	3.35 GHz	3.125 Gb/s to 40 Gb/s
Frequency	120 MHz	165 MHz	330 MHz	330 MHz	400 MHz	660 MHz	3.35 GHz	3.125 Gb/s to 40 Gb/s
Mainframe model + interface, resp. 1 or 2 channels	81150A (001/002)	81110A and 81111A	81110A and 81112A	81160A (001/002)	81130A and 81131A	81130A and 81132A	81133A (81134A)	N5980A Serial, 3.125 Gb/s
Number of channels	1 or 2				1 or 2			
Amplitude (Vpp/50 Ω)	50 mV to 10 V	100 mV to 10 V	100 mV to 3.8 V	50 mV to 5 V	100 mV to 3.8 V	100 mV to 2.5 V	50 mV to 2 V	N4962A Serial, 12.5 Gb/s
Transition time (10/90)	2.5 ns to 1000 s	2 ns to 200 s	0.8 ns or 1.6 ns	1 ns to 1000 s	0.8 ns or 1.6 ns	550 ps typ.	< 90 ps	
Differential out	Yes	No	Yes		Yes			
Triggerable	Yes				Limited			
PRBS $(2^n - 1)$	n = 7...31	n = 7...14		n = 7...31	n = 7...15		n = 5...31	
Pattern memory	Arb: 12 kpts, Pat: 16 MBit	16 kBit/Channel		Arb: 256 kpts Pat: 4 MBit	64 kBit/Channel		12 Mbit/ch	N4965A multi-channel, 12.5 Gb/s
Segm. looping	1 inner, 1 outer loop			1 inner, 1 outer loop	1 inner, 1 outer loop			
Jitter injection	Modulation			Modulation			Delay control Input	
LVDS levels	Yes				Yes		Yes, pre-defined	81250A multi-channel 675 Mb/s, 3.35, 7, 13.5 Gb/s
Remote control interface	GP-IB, LAN, USB	GP-IB		GP-IB, LAN, USB	GP-IB		GP-IB, LAN	
Remote programming (Integration info)	SCPI 1992.0, IVI-COM, NI LabView, Matlab, Agilent Waveform Builder Pro	SCPI 1992.0, NI LabView		SCPI 1992.0, IVI-COM, NI LabView, Matlab, Agilent Waveform Builder Pro	SCPI 1992.0		SCPI 1992.0, IVI-COM, NI LabView	N4903B Serial, 7, 12.5 and 14.2 Gb/s
Notes	Pulse-, Pattern-, Function- , Arbitrary-Generator, Noise source #PAT		Complete multi-channel pattern Generator: ParBERT 81250A Series	Pulse-, Pattern-, Function- , Arbitrary-Generator, Noise source #330, #660	Complete multi-channel pattern generator: ParBERT 81250A Series			M8020A, multi-channel, 16 Gb/s, 32 Gb/s
								N4876A, N4877A Mux, Demux/CDR, 28.4 Gb/s
	Internal channel-add			Internal channel-add	Internal channel-add			N4960A Serial, 17 and 32 Gb/s

	Product vs. Measurement parameter	Tunable laser sources (12)	DFB laser sources (17)	Optical power meters (19)	Return loss modules (25)	High-power optical attenuators (26)	Modular optical switches (30)	Polarization controllers (31)	Polarisation solutions (31)	Multi-wavelength meters (33)	Photonic dispersion & Loss analyzer (21)	Lightwave component analyzer (23)	Optical modulation analyzer (27)	Oscilloscope (33)	Reference transmitter & Receiver (34)	Arbitrary waveform generator (36)	Precision source/Measure unit (SMU) (38)	J-BERT N4903B/ M8020A (14)	Serial BERT 32 and 17 Gb/s (16)	Multi-channel BERT 12.5 Gb/s (20)	Serial BERT system 40 Gb/s (21)	ParBERT (27)	Manufacturing serial BERT (28)	Serial BERT (29)	Optical receiver stress test solution (30)	Infiniium DCA-J oscilloscope (31)	Pulse pattern noise generators (38)
		Volume I									Volume II																
Basic optical component test	Insertion loss	✓	✓	✓					✓		✓															✓	
	Return loss				✓																						
	Spectral IL	✓		✓					✓		✓																
	Wavelength									✓		✓															
	EDFA test	✓	✓	✓	✓	✓	✓	✓	✓																		
	Polarization state			✓							✓																
	Chromatic dispersion										✓																
	Polarization dependent loss	✓		✓				✓	✓		✓																
	Polarization extinction ratio								✓																		
	Polarization mode dispersion								✓		✓																
Coherent component test	Electro-optical S-parameter											✓	✓				✓										
	Gain imbalance/IQ offset											✓	✓			✓	✓										
	Channel skew											✓	✓			✓	✓										
	CMRR											✓	✓			✓	✓										
	Quadrature error											✓	✓			✓	✓										
	Magnitude error/Phase error											✓	✓			✓	✓										
Optical transceiver test	Modulation signal															✓					✓					✓	
	Pulse response													✓				✓	✓	✓	✓	✓	✓	✓		✓	✓
	Extinction ratio													✓	✓											✓	✓
	Optical modulation amplitude													✓	✓	✓										✓	✓
	Vertical eye closure penalty														✓	✓										✓	
	Transmitter dispersion penalty																	✓	✓			✓		✓		✓	
	Eye-diagram/Mask													✓		✓		✓				✓		✓		✓	
	Jitter analysis													✓		✓		✓	✓	✓				✓		✓	
	Jitter tolerance													✓	✓	✓		✓	✓	✓				✓			✓
	Bit error ratio													✓	✓			✓	✓	✓	✓	✓	✓	✓		✓	
	Receiver sensitivity														✓	✓		✓	✓	✓	✓	✓	✓	✓			
	Stressed receiver sensitivity														✓	✓		✓	✓	✓					✓	✓	

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Related Literature:

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General Photonic Test 5989-6753EN

Lightwave Catalog Volume 2:
Optical-Electrical / Polarization / Complex Modulation 5989-6754EN

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