Agilent

J-BERT M8020A High-Performance BERT

Preliminary Data Sheet Version 0.5

Master your next designs

Key Features

- *Data rates of up to 8.5 and 16 Gb/s expandable to 32 Gb/s*
- *1- 4 BERT channels in a 5-slot AXIe chassis*
- *Integrated and calibrated jitter injection: RJ, PJ1, PJ2, SJ, BUJ, sinusoidal interference (common-mode and differential-mode), SSC (triangular and arbitrary, residual) and F/2*
- *8 - tap de-emphasis, positive and negative*
- *Interactive link training for PCI Express*
- *Built-in clock recovery and equalization*

Description

The high-performance Agilent J-BERT M8020A enables fast, accurate receiver characterization of single- and multi-lane devices running up to 16 or 32 Gb/s.

With today's highest level of integration, the M8020A streamlines your test setup. In addition, automated in situ calibration of signal conditions ensures accurate and repeatable measurements. And, through interactive link training, it can behave like your DUT's link partner. All in all, the J-BERT M8020A will accelerate insight into your design.

Anticipate ___Accelerate ___Achieve

Agilent Technologies

M8000 Series of BER Test Solutions

Take the Express Lane to Design Verification

Simplified time-efficient testing is essential when you are developing next-generation computer, consumer, or communication devices.

The Agilent M8000 Series is a highly integrated BER test solution for physical layer characterization, validation, and compliance testing.

With support for a wide range of data rates and standards, the M8000 Series provides accurate, reliable results that accelerate your insight into the performance margins of high-speed digital devices.

Shift into high gear with the M8000 Series—and take the design verification express lane.

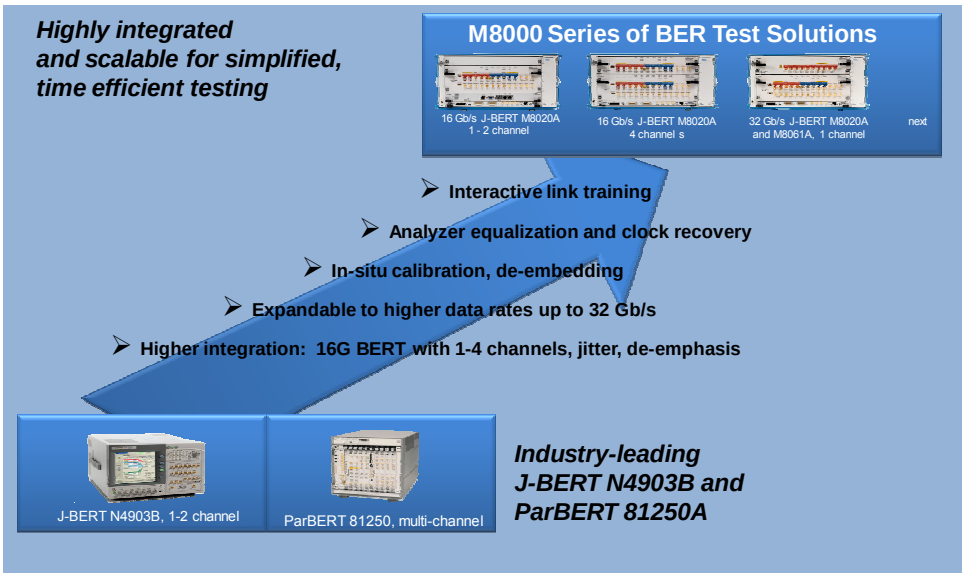


Figure 1. The M8000 Series BER Test Solution is highly integrated and scalable to address the test challenges of the next generation of high-speed digital receiver test.

J-BERT M8020A High-Performance BERT

Enabling fast, accurate receiver characterization of single- and multi-lane devices running up to 16 or 32 Gb/s.

Highest level of integration for streamlined test setups

With J-BERT M8020A all receiver (RX) test capabilities are built in: jitter sources, common- and differential-mode level interference, and de-emphasis to emulate the transmitter (TX) of the device under test (DUT). In addition M8020A provides a built-in reference clock multiplier for synchronization of the BERT pattern generator with the DUT's reference clock which can carry spread spectrum clocking (SSC). On the analyzer side an equalizer to open closed eyes and a clock recovery with adjustable loop bandwidth for the analyzer is built in.

With this high level of integration a receiver test set-up with M8020A is now much easier to connect and more robust. Set up and debug time is shortened, calibration is simpler and the frequency of recalibration is lower, resulting in more efficient use of overall test time.

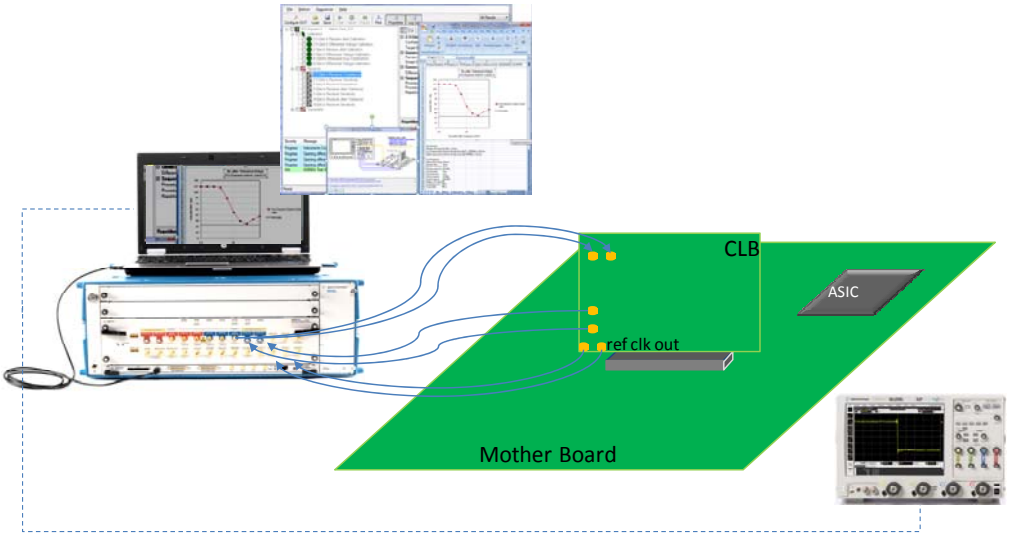


Figure 2: M8020A streamlines complex receiver test setups. The example shows a PCIe 3 (8 GT/s) mother board RX test with J-BERT M8020A connected via a compliance load board (CLB). J-BERT M8020A provides built-in de-emphasis, jitter sources, common-mode and differential mode interference (CMI, DMI), reference clock multiplier, clock recovery and continuous time linear equalizer (CTLE) – everything that is needed is built-in and calibrated.

In-situ calibration for the most accurate and repeatable results

At data rates above 5 Gb/s, the influence of the channel (PC-board , cable, connectors) between TX and RX Is no longer negligible. The reference point for the RX specification moves to the RX input, the test set-up typically has to contain a certain channel characteristic, often an ISI channel, as well. To accurately inject a defined stress condition to the RX in-situ calibration is required: at that same exact point where the receiver under test has to be connected during test, a reference load is connected instead and the generated signal is measured. This allows calibration of the test signal at that point where the specification applies by adjusting the instrument generated stress such as jitter in a way that the target signal with all its ingredients is achieved.

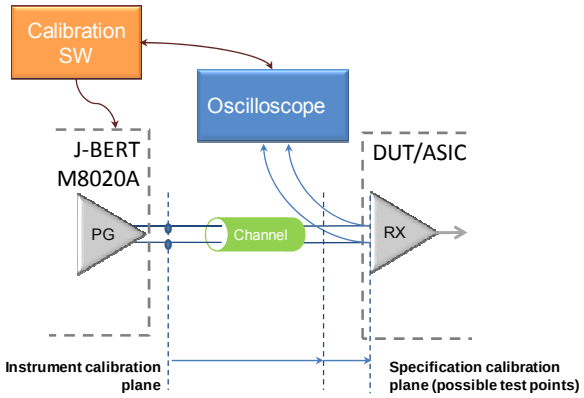


Figure 3. With increasing bit rates the calibration plane for the receiver stress conditions moves closer to the receiver inputs. J-BERT M8020A supports in-situ calibration to achieve higher accuracy of the signal and stress conditions at the relevant definable test point.

Interactive link training to fasten loopback

The ever increasing data rate of computer buses and datacom interfaces results in shrinking margins and the necessity to use equalization techniques in transmitters and receivers to compensate for the lossy channels caused by cheap PC board material or long cables. For the latest industry standards, such as PCI Express 3 or 4, SAS 12G, and backplanes such as 100GBASE-KR4, the link partners are required to optimize the TX de-emphasis and RX-equalization combination. The RX takes the active part during this procedure. In order to do so, the BERT must be capable to understand the low level protocol and to react accordingly, i.e.e. change its TX de-emphasis as requested. J-BERT M8020A can behave like a real link partner with its interactive link training capability, initially PCIe is supported.

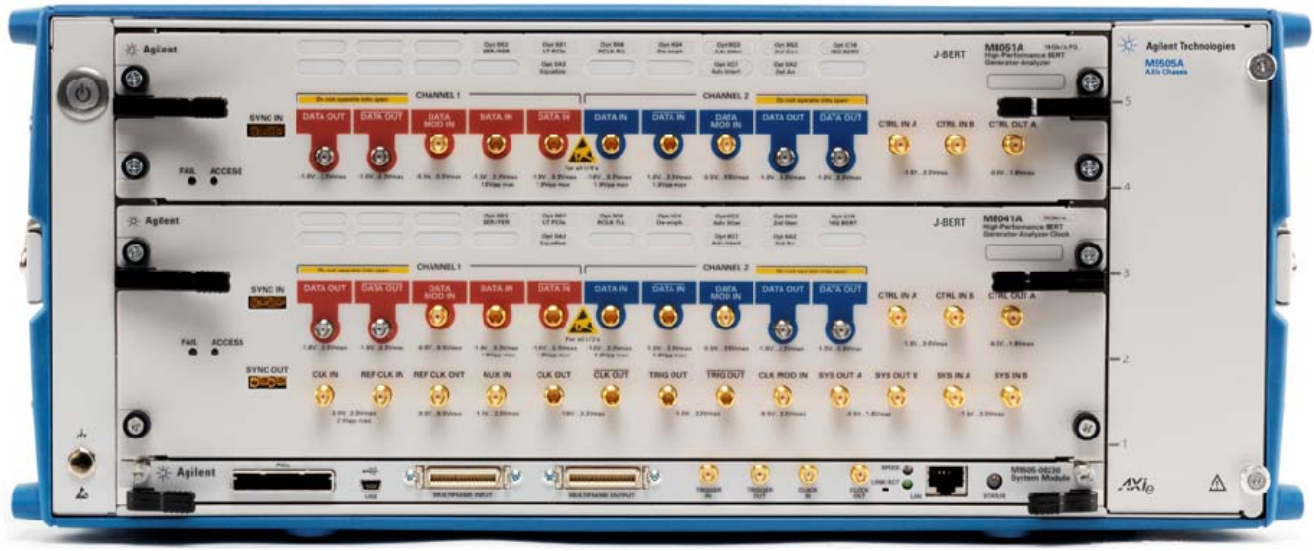


Figure 4. J-BERT M8020A high-performance BERT for accelerated receiver characterization. The configuration shows a 4 channel 16Gb/s BERT in a 5-slot AXIe chasssis consisting of one M8041A modules with two BERT channels and clock synthesizer and one M8051A extender module with two additional BERT channels.

Applications

R&D and test engineers who characterize, verify compliance of chips, devices, boards and systems with serial I/O ports up to 16 Gb/s. The M8020A can be used to test popular serial bus standards, such as PCI Express®, SATA/SAS, DisplayPort, USB Super Speed, MIPI MPHY, SD UHS-II, Fibre Channel, QPI, HyperTransport, memory buses, backplanes, repeaters, active optical cables, Thunderbolt, 10 GbE/SFP+, 100GbE/CFP2.

Receiver characterization and compliance test

Many multi gigabit serial interfaces use transmitter de-emphasis to compensate for electrical signal degradations caused by printed circuit boards or cables between the transmitter and the receiver ports. R&D and test engineers who need to characterize receiver ports under realistic and worst case conditions require a pattern generator that allows to accurately emulate transmitter de-emphasis and the channel with adjustable multi-tap de-emphasis levels. The M8061A can be used in combination with J-BERT N4903B as shown below.

User interface and measurements

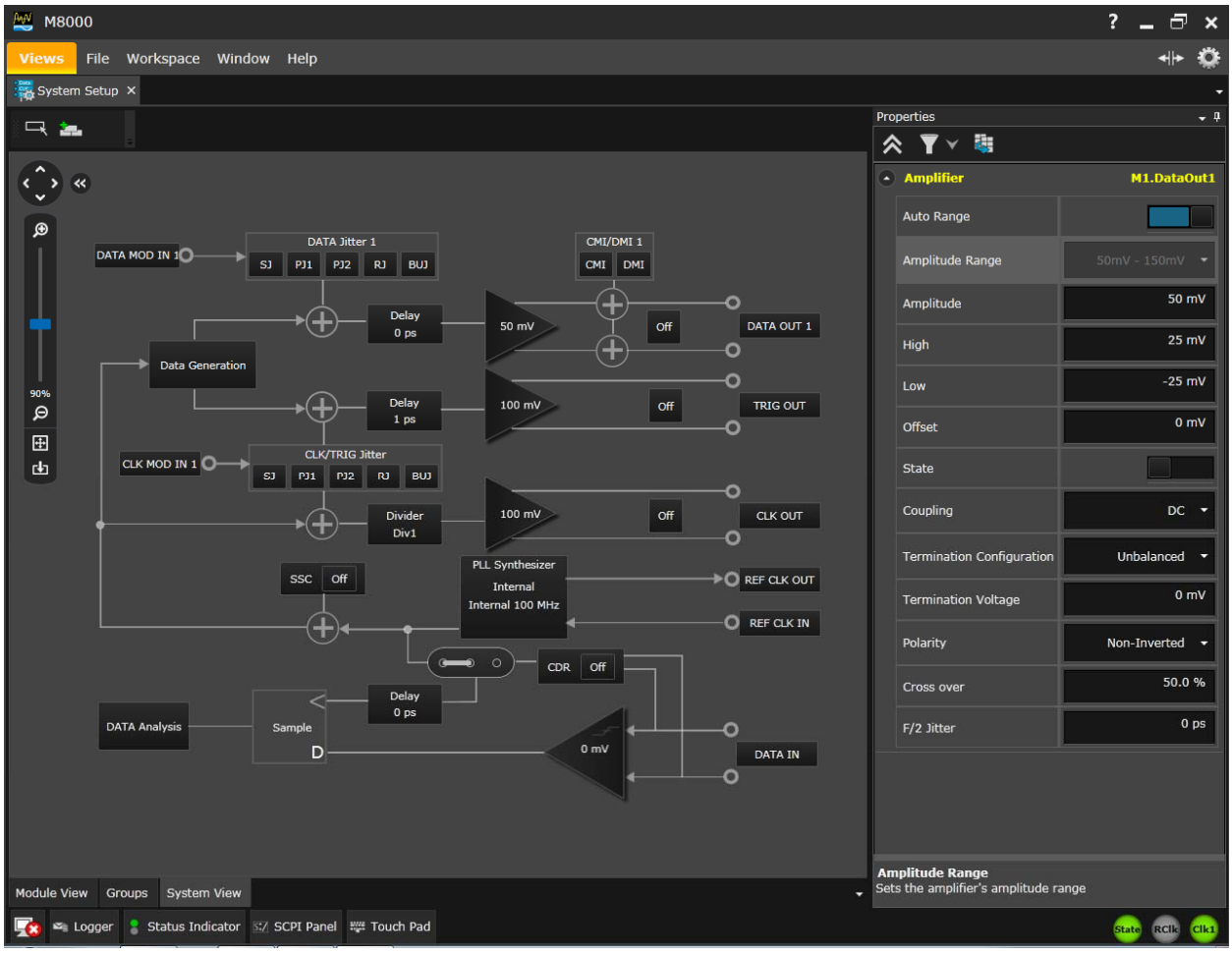


Figure 5: The graphical user interface for J-BERT M8020A offers multiple views that can be defined by the user. This example shows the system view on left side and the pattern generator data output parameter s at the right. P*reliminary GUI screen as of January 2014.*

Accuracy and performance

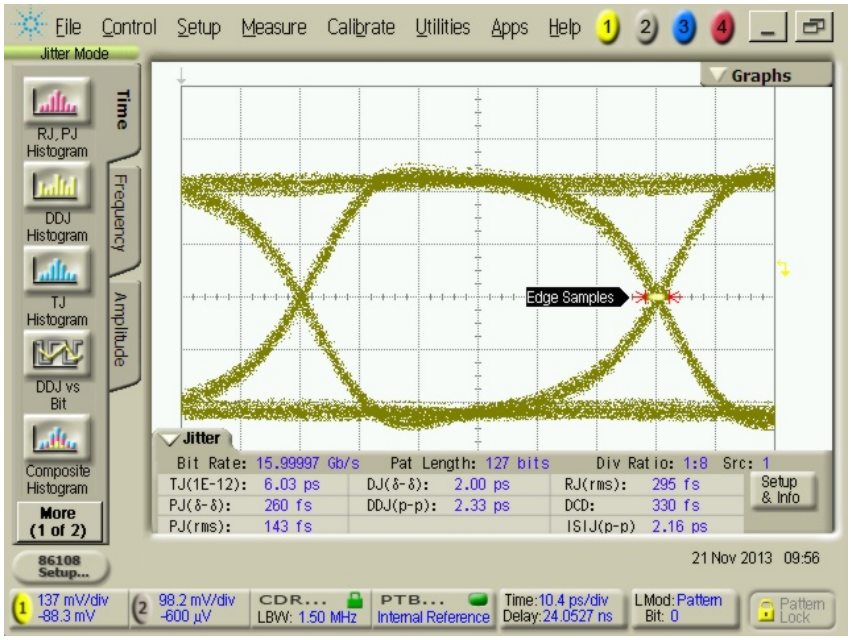


Figure 6. Clean 16.0 Gb/s output signal of J-BERT M8020A with a M8041A 16G BERT module using its internal clock source (preliminary).

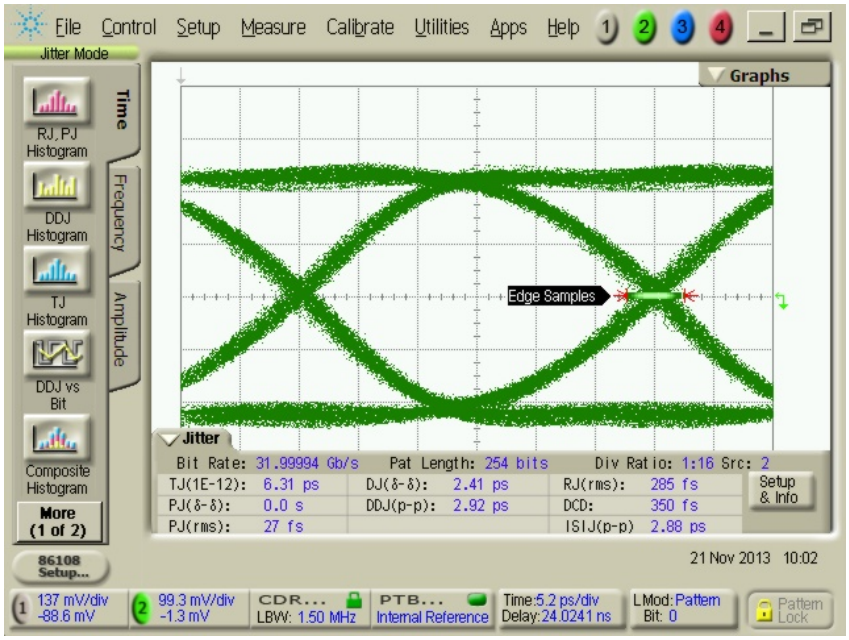


Figure 7: The 32.0 Gb/s output signal shows excellent intrinsic random jitter. This shows the output of the M8061A multiplexer when used with M8041A and its internal clock source (preliminary).

Specifications for M8041A and M8051A

J-BERT High-performance BERT Modules

Figure 8: Front panel view of M8041A module (bottom) and M8051A (top)

Specifications Pattern Generator

Data Output (DATA OUT 1, DATA OUT 2)

Table 1. Data Output characteristics for M8041A and M8051A.

All timing parameters are measured 0.5 V into Ground		M8041A	M8051A
Data rate	150 MHz to 8.50 GHz (opt. G08 or C08), 150 MHz to 16.20 GHz (opt. G16 or C16)	x	x
Frequency accuracy	±15 ppm	x	na
Data format	NRZ	x	x
Channels per module	1 or 2 (second channel requires opt.0G2)	x	x
Amplitude	50 mV to 1.2 Vpp single ended, 100 mV to 2.4 Vpp differential, *1mV resolution; addresses LVDS, CML, low-voltage CMOS, others.* *See table 2 for max. output amplitude*	x	x
Amplitude accuracy	5 % ±5 mV typical (DC)	x	x

Output voltage window		-1 V to +3.0 V	x	x
External termination voltage		-1 V to *+3.0* V. For offset > 1.3 V the termination voltage should be ± 0.5 V of offset	x	x
Transition time	20-80%	15 to 20 ps typical	x	x
Crossing point		adjustable from 30% to 70%	x	x
Total intrinsic jitter[1]		8 ps p-p typical	x	x
Random intrinsic jitter [2]		300 fs rms typical	x	x
Data delay range		0 to 10 ns	x	x
Data delay resolution		100 fs	x	x
Electrical idle transition time		Output transitions from full swing signal to 0 V amplitude and vice versa at constant offset within 4 ns typical. Electrical idle can be controlled from sequencer or external input.	x	x
Termination		50 Ω into GND or external termination voltage. Do not operate into open. Un-used outputs must be terminated into termination voltage.	x	x
Termination modes		Balanced/unbalanced DC/AC coupling	x	x
Connectors		3.5 mm, female	x	x

[1] at 16 Gb/s PRBS 2^{15}-1, BER 10^{-12}, with internal clock

[2] at 16 Gb/s and clock pattern

Table 2. Data output amplitude maximum (single ended) in presence of DMI, CMI, offset voltage > 1.9 V

Offset ≤ 1.9 V	Offset > 1.9 V	CMI	DMI
1.2 Vpp	0.900 Vpp	disabled	disabled
0.9 Vpp	0.675 Vpp	disabled	enabled
0.9 Vpp	0.750 Vpp	enabled	disabled
0.675 Vpp	0.562 Vpp	enabled	enabled
0.8 Vpp	0.666 Vpp	enabled	enabled[1]

[1] for DMI < 12.5% of amplitude

De-emphasis (DATA OUT)

M8020A provides built-in de-emphasis with positive and negative cursors based on a FIR filter.

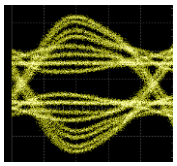
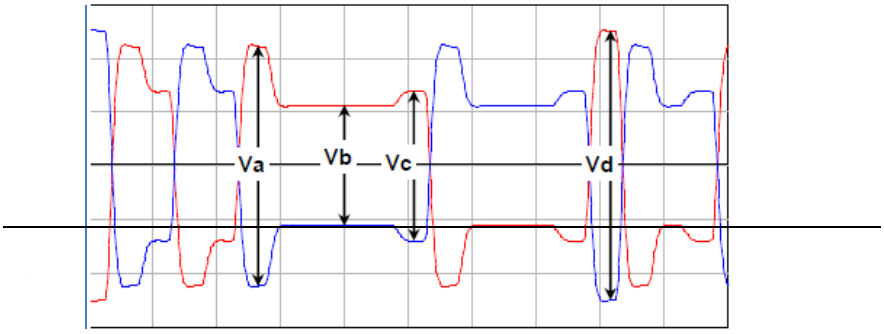


Table 3. Specifications for multi-tap de-emphasis (requires option 0G4)

		M8041A	M8051A
De-emphasis taps	8 (requires opt. 0G4)	opt.0G4	opt. 0G4

	can be adjusted for each channel independently		
Pre-cursor 2	±6.0 dB	opt. 0G4	opt. 0G4
Pre-cursor 1	±12.0 dB	opt. 0G4	opt. 0G4
Post-cursor 1	±20.0 dB	opt. 0G4	opt. 0G4
Post-cursor 2	±12.0 dB	opt. 0G4	opt. 0G4
Post-cursor 3	±12.0 dB	opt. 0G4	opt. 0G4
Post-cursor 4	±6.0 dB	opt. 0G4	opt. 0G4
Post-cursor 5	±6.0 dB	opt. 0G4	opt. 0G4
De-emphasis tap resolution	0.1 dB	opt. 0G4	opt. 0G4
De-emphasis tap accuracy	± 1.0 dB[1]	opt. 0G4	opt. 0G4

[1] sum of all cursors may not exceed Vpp max. The tap accuracy applies for PCIe 3 presets for pre-cursor 1 and post-cursor 1 at 8 Gb/s.



Post-cursor 1 = $20\log_{10}$ Vb/Va
Pre-cursor = $20\log_{10}$ Vc/Vb
Vpp nominal = $20\log_{10}$ Vd

Figure 5. Definition of nominal output amplitude and de-emphasis

Clock Output (CLK OUT)

Table 4. Clock output specifications (M8041A only)

		M8041A	M8051A
Frequency range	150 MHz to 8.50 GHz (opt. G08 or C08), 150 MHz to 16.20 GHz (opt. G16 or C16)	x	no clk
Amplitude	0.1 to 1 V , 5 mV steps	x	

Output voltage window		-1 V to +3 V[1]	x
External termination voltage		-1 V to *+3.0* V	x
Transition times	20-80%	20 ps typical	
Duty cycle		50%, accuracy ± 10%	x
Clock divider		1, 2, 4, 8, 10, 16, 20, 24, 30, 32, 40, 50, 64, 66, 80	x
Intrinsic random jitter		300 fs rms typical at 16.2 GHz	x
SSB phase noise		TBD	
Termination		50 Ω into GND or external termination Voltage. Do not operate into open. Un-used outputs must be terminated into termination voltage.	x
Connectors		3.5 mm, female	x

[1] If V_{term} is other than 0 V the following applies: high level voltage range = V_{term} – 1 V to 3 V and low level voltage range = -1 V to Vterm +1 V.

Reference Clock Input (REF CLK IN)

This input on the M8041A module allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator. Output clocks of 8 to 16 GHz.

Table 5. Reference clock input specifications (M8041A only)

		M8041A	M8051A
Input amplitude	0.2 to 1.4 Vpp	x	no
Input frequency	10 MHz to 16.2 GHz	x	
Interface	Single ended. 50 Ω nominal	x	
Connector	SMA, female	x	

Table 6 Predefined settings for reference clock multiplier (M8041A with option 0G6 only)

Ref clock input	Standard	Target data rate	Multiplier	PLL loop BW	M8041A
100 MHz	*PCIe 4*	*16 Gb/s*	*160*	*TBD*	0G6
100 MHz	PCIe 3	8 Gb/s	80	5 MHz	0G6
100 MHz	PCIe 2	5 Gb/s	50	5 MHz	0G6
100 MHz	PCIe 1	2.5 Gb/s	25	5 MHz	0G6
26 MHz to 52 MHz	SD UHS-II	390 Mb/ to 780 Mb/s	15	2 MHz	0G6

26 MHz to 52 MHz	SD UHS-II	780 MHz to 1.56 Gb/s	30	2 MHz	0G6	n/a
52 MHz to 104 MHz	*SD UHS-II Gen 2*	*1.56 to 3.12 Gb/s*	*30*	*TBD*	0G6	n/a
52 MHz to 104 MHz	*SD UHS-II Gen 2*	*3.12 Gb/s to 6.24 Gb/s*	*30*	*TBD*	0G6	n/a
19.2 MHz	MIPI M-PHY	1.248/ 1.4592/ 2.496/ 2.9184/ 4.992/ 5.8368 Gb/s	TBD	2 MHz	0G6	n/a
26 MHz	MIPI M-PHY	1.248/ 1.456/ 2.496/ 2.912/ 4.992/ 5.824 Gb/s	TBD	2 MHz	0G6	n/a
38.4 MHz	MIPI M-PHY	1.248/ 1.4592/ 2.496/ 2.9184/ 4.992/ 5.8368 Gb/s	TBD	2 MHz	0G6	n/a
52 MHz	MIPI M-PHY	1.248/ 1.456/ 2.496/ 2.912/ 4.992/ 5.824 Gb/s	TBD	2 MHz	0G6	n/a

Supplementary Inputs and Outputs of M8041A and M8051A

Trigger Output (TRG OUT)

Table 7. Trigger output specifications (M8041A only)

		M8041A	M8051A
Amplitude	0.1 to 1 Vpp single ended; 0.2 to 2 Vpp differential	x	no trg
Output voltage window	-1 to 3 V [1]	x	
External termination voltage	-1 to 3 V	x	
Interface	differential, 50 Ω	x	
Connector	3.5 mm, female	x	

[1] If V_{term} is other than 0 V the following applies: high level voltage range = V_{term} – 1 V to 3 V and low level voltage range = -1 V to Vterm +1 V.

Reference clock output (REF CLK OUT)

Outputs a 10 MHz clock, 1 Vpp single ended into 50 Ohm. M8041A only.
Connector: SMA, female.

Clock input (CLK IN)

For future use. For M8041A only

Control Input A and B (CTRL IN A, CTRL IN B)

Functionality of each input can be selected as: sequence trigger, error add input.

Table 8. Control input specifications (M8041A and M8051A)

		M8041A	M8051A
Input voltage	-1 V to +3 V	x	x
Termination voltage	-1 V to +3 V	x	x
Threshold voltage	-1 V to +3 V	x	x
Connector	SMA, female	x	x

Control Output A (CTRL OUT A)

Outputs a pulse in case of an error. SMA connector

Table 9. Control output specifications (M8041A and M8051A)

		M8041A	M8051A
Amplitude [1]	0.1 to 2 V	x	x
Output voltage 1	-0.5 to 1.75 V	x	x
Connector	SMA, female	x	x

[1] when terminated with 50 Ω into GND. Doubles into open.

Synchonization Input and Output (SYNC IN, SYNC OUT)

The Sync Output on M8041A: clock output to synchronize multiple modules to a common clock.
The Sync Input is a clock input on M8051A module to synchronize additional modules to a common clock.
A sync cable is delivered with each M8051A module by default.

System Input A/B and Auxillary Input (AUX IN)

Control inputs to synchronize events for the pattern sequencer.
Auxiliary input: for future use. For M8041A only.

Table 10. System input and auxiliary input specifications (M8041A only)

		M8041A	M8051A
Input voltage	-1 V to +3 V	x	no
Termination voltage	-1 V to +3 V	x	
Threshold voltage	-1 V to +3 V	x	
Connector	SMA, female	x	

System Output A/B (SYS IN A/B and SYS OUT A/B)

Control outputs to synchronize events for the pattern sequencer.

Table 11. System output specifications (M8041A only)

		M8041A	M8051A
Amplitude [1]	0.1 to 2 V	x	no
Output voltage 1	-0.5 to 1.75 V	x	
Connector	SMA, female	x	

[1] when terminated with 50 Ω into GND. Doubles into open.

Jitter Tolerance Test Specifications

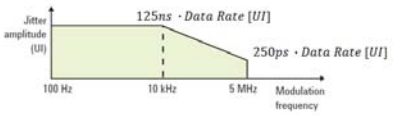
M8020A provides built-in calibrated jitter sources designed to cover receiver test needs for most of the popular multi-gigabit standards such as: PCIe Express, USB, MIPI, SATA, DisplayPort, QPI, Hypertransport, CEI, 10GbE , 100GbE, SFP+, QSFP, CFP2/4, etc.

M8020A provides automated jitter tolerance measurements. A library of pre-defined compliance curves is provided.

Table 12. Specifications for low frequency sinusoidal jitter (requires option 0G3 advanced jitter sources)

			M8041A	M8051A
Low frequency sinusoidal jitter (LF SJ) (generated by IQ modulator)	amplitude range	0 to 1000 UI. For frequencies between 10 kHz and 5 MHz see figure 6 for maximum LF SJ. Formula for fmod > 10 kHz is TBD.	opt. 0G3	opt. 0G3
	frequency	100 Hz to 5 MHz		
	jitter	±2 % ± 1 ps typical		
	amplitude accuracy			
	adjustable	for each data channel independently same SJ for clock and trigger		

Low Frequency Sinusoidal Jitter



Data rate	Max UI at modulation frequency 100 Hz to 10 kHz	Max UI at modulation frequency 5 MHz
8.1 Gb/s to 16.2 Gb/s	1000-2000 UI	2-4 UI
4.05 Gb/s to 8.1 Gb/s	500-1000 UI	1-2 UI
2.025 Gb/s to 4.05 Gb/s	250-500 UI	0.5-1 UI
1.0125 Gb/s to 2.025 Gb/s	125-250 UI	0.25-0.5 UI
506.25 Mb/s to 1.0125 Gb/s	62.5-125 UI	0.125-0.25 UI
253.125 Mb/s to 506.25 Mb/s	31.25-62.5 UI	0.0625-0.125 UI
126.5625 Mb/s to 253.125 Mb/s	15.625-31.25 UI	0.03125-0.0625 UI

Figure 6. Low frequency sinusoidal jitter maximum depends on data rate and modulation frequency.

Table 13. Specifications for high frequency periodic jitter, random jitter, spectrally distributed random jitter, bounded uncorrelated jitter, Clock/2 jitter (requires option 0G3 advanced jitter sources)

			M8041A	M8051A
High frequency jitter (generated by delay line)	range	1 UI p-p for data rates > 1 Gb/s note: this is max sum of RJ, HF-PJ1 and HF-PJ2, spectral RJ, external delay modulation and BUJ.	opt. 0G3	opt. 0G3
High frequency periodic jitter (HF PJ1 and HF PJ2)	range	See HF jitter above [1]	opt. 0G3	opt. 0G3
	frequency	1 kHz to 500 MHz Two tone possible. Sweep.		
	jitter amplitude accuracy	±10% typical		
	adjustable	for each channel independently		
Random jitter (RJ)	range	0 to 72 mUI rms (1 UI p-p max.), [1]	opt. 0G3	opt. 0G3
	jitter amplitude accuracy	± 10% typical		
	filters	high-pass: 10 MHz, low-pass; 100 MHz, 500 MHz		
	adjustable	for each channel independently		
Spectrally distributed RJ according to PCIe 2 (sRJ) [2]	range	0.. 72 mUI rms (1 UIp-p) [1]	opt. 0G3	opt. 0G3
	frequency	LF: 0.01 to 1.5 MHz, HF: 1.5 to 100 MHz		
	jitter amplitude accuracy	±10 % typical		
	adjustable	for each channel independently		

Bounded uncorrelated jitter	range	See HF jitter above[1]	opt. 0G3	opt. 0G3
	PRBS polynomials	TBD		
	Filters	TBD		
	jitter amplitude accuracy	TBD		
	adjustable	for each channel independently		
Clock/2 jitter	range	±20 ps or ±0.1 UI typical (whatever is less). Note: this means that first eye can be up to 20 ps longer or shorter than subsequent eye.	opt. 0G3	opt. 0G3
	adjustable	For each channel independently		

[1] 1 UI is the maximum sum of RJ, HF-PJ1 and HF-PJ2, spectral RJ, external delay modulation and BUJ.

[2] Spectrally distributed jitter is mutually exclusive with RJ.

Table 14. Specifications for Spread Spectrum Clocking (SSC) (requires opt. 0G3: advanced jitter sources)

			M8041A	M8051A
SSC (Spread Spectrum Clock)	range	± 5000 ppm	opt. 0G3	na
	frequency modulation	30 kHz to100 kHz triangular and arbitrary modulation		
	SSC amplitude accuracy	TBD		
	outputs	can be turned on/off independently for CLK OUT, DATA OUT1, DATA OUT 2, TRG OUT		
Residual SSC (@ PCIe2)	range	0 to 100 ps	opt. 0G3	opt. 0G3
	frequency	30 to 33 kHz		
	outputs	can be turned on/off independently for DATA OUT1, DATA OUT2		

Table 15. Specifications for external jitter modulation (DATA MOD IN 1 and 2, CLK MOD IN)

M8041A provides allows individual jitter injection for data 1, data 2 and clock. M8051A for Data 1 and data 2. The Option 0G3 is not needed.

			M8041A	M8051A
External jitter - data modulation input 1 and 2	description	input for delay modulation for each DATA OUT individually.	x	X
	range	up to 1 UI [1], 1 Vpp max		
	frequency	up to 1 GHz		
External jitter - clock modulation input	description	input for delay modulation for the TRG OUT and CLK OUT. Affects both.	x	na
	range	up to 1 UI , 1 Vpp max		
	frequency	up to 1 GHz		
Connectors		SMA, female	x	x

Footnote [1] 1UI is the maximum sum of RJ, HF-PJ1 and HF-PJ2, spectral RJ, external delay modulation and BUJ.

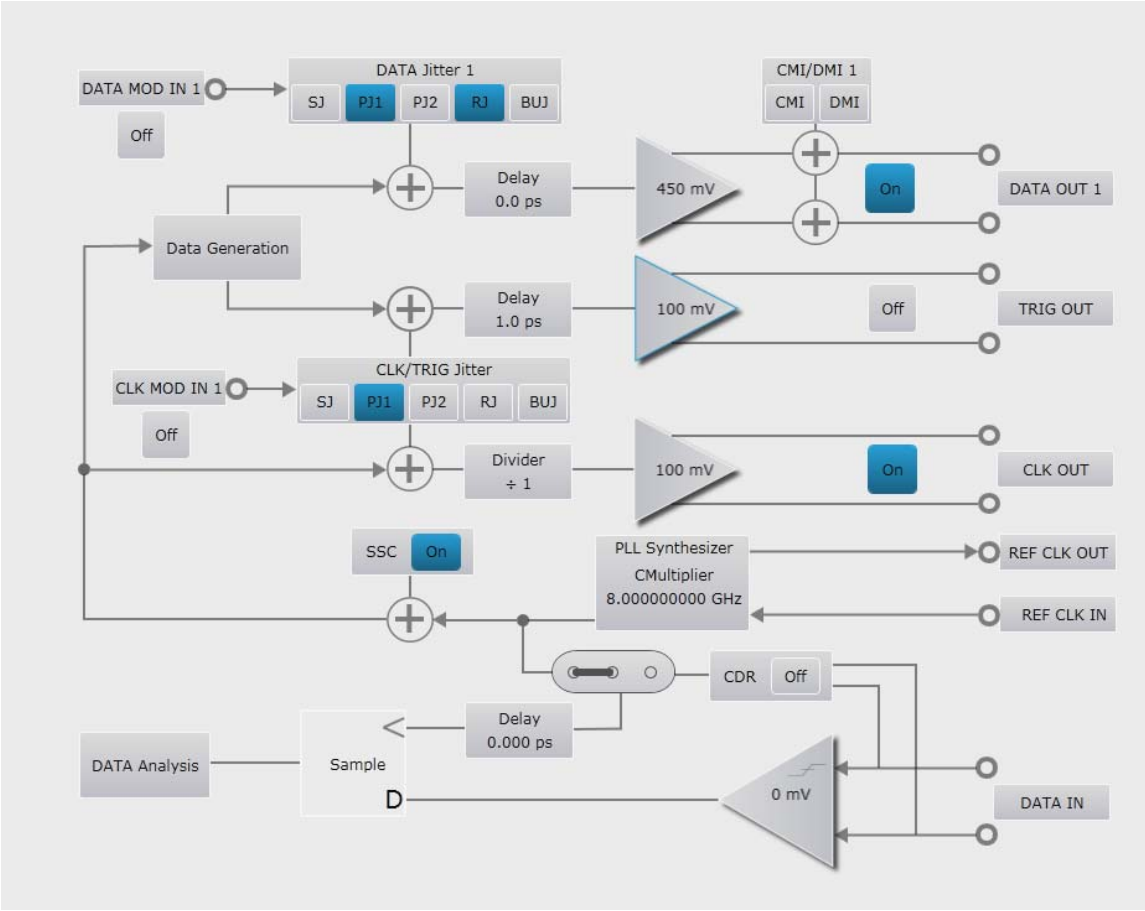


Figure 7. J-BERT M8020A system view for 1 channel, preliminary version.

ISI channels

External ISI channels are available to emulate channel loss. Agilent offers dedicated compliant ISI channels for DisplayPort, PCIe3, and SATA. M8048A is offererd in addition. For detailed specifications see M8048A data sheet.

M8041A-001 ISI Channels provides four short traces:

7.7"(196 mm), 9.4" (240 mm), 11.12 "(282 mm), 12.8"(324 mm)

M8041A.002 ISI Channels p four long traces:

14.8" (366 mm), 16.1" (408 mm), 24.4" (620 mm), 34.4"(874 mm)

Level Interference Injection

Common mode or differential mode level interfernce can be generated internally to test common mode rejection of a receiver and vertical eye closure tolerance.Simultaneous injection of CMI and DMI is possible.

Table 16. Specifications for sinusoidal interference (CMI, DMI) (requires option 0G7)

			M8041A	M8051A
Differential mode interference (DMI)	amplitude[2] amplitude accuracy	max. 30% of output amplitude[1] +-10 mV +-10% typ	opt 0G7	opt 0G7
Common mode interference (CMI)	amplitude[2] amplitude accuracy	up to 400 mV[1] +-10 mV +-10% typ	opt 0G7	opt 0G7
Frequency ranges	LF HF	10 MHz to 1 GHz, sinusoidal only 1 GHz to 6 GHz, sinusoidal only		
Simultaneous injection of CMI and DMI		Yes		

[1]. The maximum output amplitude decreases when CMI or DMI is enabled. See table 2.

[2]: for each channel independently

Pattern, Sequencer and Interactive Link Training

Table 17. Specifications for pattern, sequencer and link training

		M8041A	M8051A
PRBS [1]	2^n-1, n= 7, 10, 11, 15, 23, 23p [3], 31	x	x
PRBS	2^n, n=7,10,11,13,15,23	x	x
Mark density	Mark density: PRBS 1/8...7/8	x	x
Zero substitution	Yes	x	x
Export/import	Patterns from N4900 series can be imported	x	x
Pattern library	yes	x	x
User definable memory	4 Gbit/channel [2] 2 Mbit / channel	x	x
Interactive link training	Link training state machine (LTSSM) for PCIe 2/3 [2].	opt.0S1	na

	Includes speed and de-emphasis negotiation.		
Coding	8B/10B, 128B/130B, 130B/132B, binary	x	x
Vector/sequence granularity	64/80/130/132 bit	x	x
Pattern capture	Yes [2]	C08/C16	C08/C16
Pattern sequencer	3 counted loop levels. 1 infinite loop.	x	x

[1] note: polarity is inverted compared to ParBERT and J-BERT N4903A/B and N49xx models

[2] for availability: contact factory. Free software update (interactive link training requires opt. 0S1).

[3] modified compliance pattern for PCIe3

Analyzer/ Error Detector

Each analyzer channel includes a clock recovery.

For the following functions a separate Module option is required:

- Equalizer CTLE option (option 0A3 for M8041A nad M8051A
- SER/FER analysis (option 0S2 for M8041A only, applies for all analyzers channels in the same clock group): this option provides handling of 8B/10B coded, 128B/130B coded SKPOS. Automatic handling of running disparity changes for 8B/10B coded patterns. Up to 4 filler symbols can be defined. No dead time while filtering filler symbols. Ignores changes of length of 128/130 bit coded Skip Ordered Sets for PCIe. Counters for SER/FER filler symbols.

Table 18. Specifications for analyzer / error detector (Option C08 or C16)

		M8041A	M8051A
Data rate	150 MHz to 8.50 GHz (opt. C08), 150 MHz to 16.20 GHz (opt. C16)	x x	x x
Channels per module	1 or 2 (opt.0A2)	x	x
Data format	NRZ, single ended and differential	x	x
Input sensitivity [1]	*< 50 mV*	x	x
Timing resolution	1 mUI	x	x
Input bandwidth	TBD	x	x
CTLE	Yes	opt.0A3	opt.0A3
Clock data recovery	Yes for each input channel	x	x
Adjustable loop bandwidth	Data rate /10000 to data rate/800 (maximum is 20 MHz)	x	x
Sampling point	Manual and automatic. Finds optimum voltage threshold and delay of the sampling point.	x	x
Decision threshold range	TBD	x	x
Phase margin	TBD	x	x

BER	Accumulated	x	x
Symbol/Frame error rate	8B/10B, 128B/130B coded	opt. 0S2	na
Filtering of filler symbols	Automatic removal of filler symbols. See also description above.	opt. 0S2	na
Interface	Differential: 100Ω, single ended: 50 Ω, DC coupled	x	x
Data input connectors	3.5 mm, female	x	x

[1] *measured with PRBS 2^{31}-1 at 16 Gb/s single ended, target BER 10^{-12}*

Table 19: Available measurements (Option C08 or C16)

		M8041A	M8051A
BERT Scan with RJ, DJ separation	yes	x	x
Accumulated BER	yes	x	x
Jitter tolerance	yes	x	x
Eye contour	yes [1]	x	x
Quick eye diagram	yes [1]	x	x
Output level and Q factor	yes [1]	x	x

[1] for availability: contact factory. Free software update.

User Interface and Remote Control

The M8070A system software for the M8000 Series of BER Test Solutions is required to control M8041A, M8051A and M8061A.

Table 18. User interface and remote control interface

System software	M8070A
Software licensing	Offline version does not require a license. For controlling the hardware you can choose between a transportable, perpetual license (M8070A-0TP) and a network, perpetual license (M8070A-0NP) . The network license is only recommended when using multiple M8020A setups within one company. When ordering M8020A-BU1 the M8070A-0TP license will be pre-installed on the embedded controller.
Controller requirements	**Embedded PC:** Choose M8020A-BU1 for a pre-installed embedded controller M9536A including pre-installation of M8070A software and module licenses. Otherwise: M9536A 1-slot AXIe embedded controller, choose options for Win 7/8, 16 GB RAM, USB **External PC:** USB connection recommended between external PC and AXIe chassis. 8 GB RAM recommended. For PCIe connectivity please refer to list of tested PCs for AXIe Technical Note, pub no. 5990-7632EN
Operating system	MS Windows 7, Windows 8
Controller connectivity	USB 2.0 (mini) recommended, PCIe 2.0/8x (only for highest

with AXIe chassis	data throughput and desktop PC)
Programming language	SCPI. (not compatible with N4900 series and ParBERT 81250A)
Remote control interface	Desktop or Laptop PC: LAN M9536A: LAN
Save/Recall	Yes
Software pre-requisites	MS Win 7 or 8, Agilent IO library rev. 16.3
Software download	See www.agilent.com/find/m8020a for latest version

General Characteristics and Physical Dimensions

Table 19. General characteristics for M8041A and M8051A modules

	M8041A	M8051A
Operating temperature	5 °C to 40 °C (-23 °F to + 104 °F)	
Storage temperature	-40 °C to +70 °C (module) (-65 °F to + 158 °F)	
Operating humidity	15% to 95% relative humidity at 40°C (non-condensing)	
Storage humidity	24% - 90% relative humidity at 65°C (non-condensing)	
Power requirements	350W	250W
Physical dimensions for modules (W x H x D)	3- slot AXIe module: 351 x 92 x 315 mm (13.8 x 3.6 x 12.4 inch)	2-slot AXIe module: 351 x 61 x 315 mm (13.8 x 2.4 x 12.4 inch)
Physical dimensions for M8020A-BU1/-BU2 (W x H x D)	Installed in 5-slot AXIe chassis: 463 x 194 x 446 mm (18.2 x 7.6 x 17.6 inch)	
Weight net	M8041A module: 6.6 kg (14.6 lb) With M8020A-BU1: 24 kg (43.9 lb) With M8020A-BU2: 19.9 kg (53 lb)	M8051A module: 5.0 kg (11.0 lb) In bundle with M8041A and in a 5-slot chassis: 24.9 kg (54.9 lb)
Weight shipping	With M8020A-BU1: 37 kg (82 lb) With M8020A-BU2: 32.5kg (71.7 lb)	
Recommended recalibration period	*1 year*	
Warranty period	3 years return to Agilent	
Warm-up time	30 minutes	
Cooling requirements	Slot airflow direction is from right to left. When operating the M8041A/51A choose a location that provides at least 80 mm of clearance at rear, and at least 30 mm of clearance at each side. See also Start-up guide for M9502A chassis.	
EMC	IEC 61326-1	

Safety	IEC 61010-1
Quality management	ISO 9001, 14001

Supplementary specifications for M8061A Multiplexer 2:1 when used with M8041A for operation up to 32 Gb/s

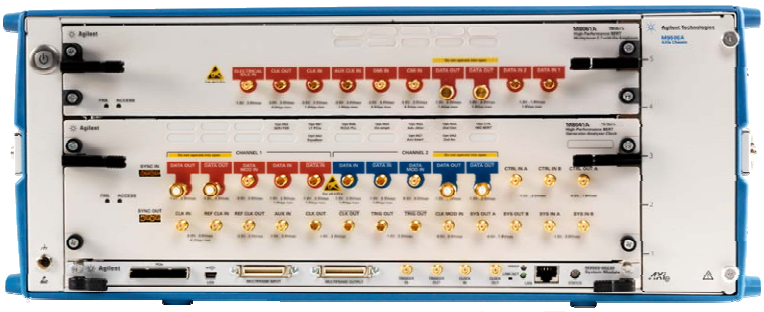


Figure 8: For a 32 Gb/s BERT setup the M8061A multiplexer with de-emphasis option can be used with a two-channel M8041A BERT and the N4877A CDR and de-multiplexer.

The table below lists the supplementary specifications that apply when M8061A is used with M8041A. For all other specifications and features of M8061A please refer to the M8061A datasheet.

Table 20. Supplementary specifications for M8061A multiplexer when used with M8041A

Data rate	300 MHz to 32.4 GHz
Intrinsic random jitter	*350 fs rms typ* (@ 28.4 Gbit/s, clock pattern using M8041A as clock source)
DMI,CMI	External DMI and CMI sources are needed
De-emphasis	4 taps (M8061A opt 004) or 8 taps (M8061A opt 008)
Electrical idle	Use M8061A input; 3.5 mm connector
Error counting	Full-rate sampling. Needs N4877A 32 Gb/s for 1:2 de-multiplexing and clock recovery. Second analyzer channel of M8041A required. No CTLE.
Measurements	For bit rates > 16.2 Gb/s measurements: receiver measurement only: jitter tolerance, accumulated BER (no BERT Scan with RJ/DJ separation)
Software	Requires M8070A
Chassis/connectivity	M8061A module has to be in same chassis as M8041A module. (An external PC is required with just one USB connection to AXIe chassis.)

Specification assumptions

The specifications in this document describe the instruments warranted performance. *Preliminary values are written in italic.* Non-warranted values are described as typical. All specifications are valid in the specified operating temperature range after the warm-up time *and after auto-adjustment. If not otherwise stated all outputs need to be terminated with 50 Ω to GND. All M8041Aand M8051A specifications if not otherwise stated are valid using the recommended cable pair M8041A-801 (2.92 mm, 0.85 m, matched pair).*

Related Agilent literature

Data Sheets:

ISI Channels M8048A Data Sheet	5991-3547EN
M8061A Multiplexer with de-emphasis Data Sheet	5991-2506EN
J-BERT N4903B Data Sheet	5990-3217EN
N4877A and N1075A CDR/Demux Data Sheet	5990-9949EN
M9505A AXIe Chassis 5-slot Data Sheet	5990-6584EN
M8020A Configuration Guide	tbd

Application Notes:

How to pass receiver test according PCI Express CEM specification Application Note	5990-7659EN
Accurate calibration of PCIe 3.0 receiver stress signals Application Note	5990-6599EN
How to test a MIPI M-PHY high-speed receiver Application Note	5991-2848EN
Error Detection up to 28.4Gb/s using under sampling techniques with J-BERT N4903B, Application Note	5990-6239EN

Ordering instructions

Please refer to M8020A configuration guide for ordering details.

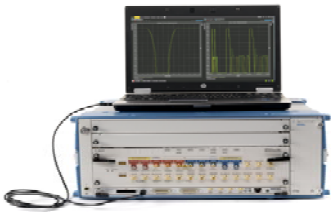
	16 Gb/s High-performance BERT, 1-2 channel with external PC
	with embedded PC
	16 Gb/s High-performance BERT, 3-4 channel (external PC not shown)
	32 Gb/s High-performance BERT, 1 channel (external PC not shown) with N4877A CDR

Figure 9. Overview of possible J-BERT M8020A configurations

Default accessories included with shipment:

M8041A module: eight 50 Ω terminations, commercial calibration report ("UK6"), certificate of calibration, ESD protection kit.
M8051A module: four *50 Ω terminations, clock synchronization cable, commercial calibration report ("UK6"), certificate of calibration*
M8020A-BU1: *M9505A AXIe chassis with embedded controller, USB cable, getting started guide, AXIe filler panel, power cord*
M8020A-BU2: *M9505A AXIe chassis, USB cable, getting started guide, AXIe filler panel, power cord*
M8070A: *CD-ROM with M8070A system software*

Recommended accessories:

Matched cable pair, 2.92 mm (f) to 2.92 mm (f)	M8041A-801
(two pairs are recommended for connecting M8041A with M8061A)	
ISI channels, four short traces	M8048A-001
ISI channels, four long traces	M8048A-002
Short matched cable pair, SMA (f) to SMA (f)	
for cascading M8048A ISI channels	M8048A-801
Four SMA cables, unmatched	15442A
Rack-mount kit for AXIe 5-slot chassis M9505A	TBD

Test automation software with support of M8020A

Test automation software for PCIe receiver test	N5990A-101
Test automation software for USB receiver test	N5990A-102
Test automation software for SATA receiver test	N5990A-103

Warranty, calibration and productivity services:

Extended 5 year warranty Return-to-Agilent	R1280
Calibration services (3 and 5 years)	R1282
Productivity assistance	R1380-M8000

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