Keysight MIMO Receiver Tester

This manual provides documentation for the following instruments:

PXB MIMO Receiver Tester

Notice: This document contains references to Agilent. Please note that Agilent's Test and Measurement business has become Keysight Technologies. For more information, go to www.keysight.com.

Security Features and Document of Volatility

KEYSIGHT TECHNOLOGIES

Notices

Manual Part Number

N5105-90014

Print Date

August 2014

Supersedes: November 2012

Printed in USA

Keysight Technologies Inc.
1400 Fountaingrove Parkway
Santa Rosa, CA 95403

Warranty

The material contained in this document is provided "as is," and is subject to being changed, without notice, in future editions. Further, to the maximum extent permitted by applicable law, Keysight disclaims all warranties, either express or implied, with regard to this manual and any information contained herein, including but not limited to the implied warranties of merchantability and fitness for a particular purpose. Keysight shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein. Should Keysight and the user have a separate written agreement with warranty terms covering the material in this document that conflict with these terms, the warranty terms in the separate agreement shall control.

Technology Licenses

The hardware and/or software described in this document are furnished under a license and may be used or copied only in accordance with the terms of such license.

Restricted Rights Legend

If software is for use in the performance of a US Government prime contract or subcontract, Software is delivered and licensed as "Commercial computer software" as defined in DFAR 252.227-7014 (June 1995), or as a "commercial item" as defined in FAR 2.101(a) or as "Restricted computer software" as defined in FAR 52.227-19 (June 1987) or any equivalent agency regulation or contract clause. Use, duplication or disclosure of Software is subject to Keysight Technologies' standard commercial license terms, and non-DOD Departments and Agencies of the US Government will receive no greater than Restricted Rights as defined in FAR 52.227-19(c)(1-2) (June 1987). US Government users will receive no greater than Limited Rights as defined in FAR 52.227-14 (June 1987) or DFAR 252.227-7015 (b)(2) (November 1995), as applicable in any technical data.

Safety Notices

CAUTION

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING

A **WARNING** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Where to Find the Latest Information

Documentation is updated periodically. For the latest information about these products, including instrument software upgrades, application information, and product information, see the following URLs:

http://www.keysight.com/find/pxb

To receive the latest updates by email, subscribe to Keysight Email Updates:

http://www.keysight.com/find/emailupdates

Information on preventing instrument damage can be found at:

http://www.keysight.com/find/PreventingInstrumentRepair

Is your product software up-to-date?

Periodically, Keysight releases software updates to fix known defects and incorporate product enhancements. To search for software updates for your product, go to the Keysight Technical Support website at:

http://www.keysight.com/find/techsupport

Table of Contents

1 Contacting Keysight Sales and Service Offices

2 Products Covered by this Document
Document Purpose 9

3 Security Terms and Definitions

4 Instrument Memory & Volatility
Non-Volatile Memory 14
Volatile Memory 18

5 Using the Instrument in a Controlled Area
Before Placing the Instrument in a Controlled Area 24
Removing the Instrument from a Controlled Area 24
Returning the Instrument to Keysight for Repair 24
Using or Repairing the Instrument in the Non-controlled Area 25
Returning the Instrument to the Controlled Area 25
After Using the Instrument in a Non-Controlled Area 26
After Repairing the Instrument 26

Appendix A References

1 Contacting Keysight Sales and Service Offices

Assistance with test and measurement needs, and information to help you find a local Keysight office, is available via the internet at, http://www.keysight.com/find/assist. If you do not have internet access, please contact your designated Keysight representative.

NOTE	In any correspondence or telephone conversation, refer to the instrument by its model number and full serial number. With this information, the Keysight representative can determine whether your unit is still within its warranty period.

2 Products Covered by this Document

Product Family Name	Product Name	Model Number	Firmware Revision
X-Series Testers	PXB Baseband Generator and Channel Emulator	N5106A	All

Document Purpose

This document describes instrument memory types and security features. It provides a statement regarding the volatility of all memory types, and specifies the steps required to declassify an instrument through memory clearing, sanitization, or removal.

For additional information, go to:

http://www.keysight.com/find/security

IMPORTANT

Be sure that all information stored by the user in the instrument that needs to be saved is properly backed up before attempting to clear any of the instrument memory. Keysight Technologies cannot be held responsible for any lost files or data resulting from the clearing of memory.

Be sure to read this document entirely before proceeding with any file deletion or memory clearing.

Products Covered by this Document
Document Purpose

3 Security Terms and Definitions

Term	Definition
Clearing	As defined in Section 8-301a of DoD 5220.22-M, "National Industrial Security Program Operating Manual (NISPOM)", clearing is the process of eradicating the data on media before reusing the media so that the data can no longer be retrieved using the standard interfaces on the instrument. Clearing is typically used when the instrument is to remain in an environment with an acceptable level of protection.
Instrument Declassification	A term that refers to procedures that must be undertaken before an instrument can be removed from a secure environment, such as is the case when the instrument is returned for calibration. Declassification procedures include memory sanitization or memory removal, or both. Keysight declassification procedures are designed to meet the requirements specified in DoD 5220.22-M, "National Industrial Security Program Operating Manual (NISPOM)", Chapter 8.
Sanitization	As defined in Section 8-301b of DoD 5220.22-M, "National Industrial Security Program Operating Manual (NISPOM)", sanitization is the process of removing or eradicating stored data so that the data cannot be recovered using any known technology. Instrument sanitization is typically required when an instrument is moved from a secure to a non-secure environment, such as when it is returned to the factory for calibration. Keysight memory sanitization procedures are designed for customers who need to meet the requirements specified by the US Defense Security Service (DSS). These requirements are specified in the "Clearing and Sanitization Matrix" in Section 5.2.5.5.5 of the ISFO Process Manual for the Certification and Accreditation of Classified Systems under the NISPOM.
Secure Erase	Secure Erase is a term that is used to refer to either the clearing or sanitization features of Keysight instruments.

4 Instrument Memory & Volatility

This chapter contains information on the memory components in your instrument.

The tables provide details of the size of each memory component, its type, how it is used, its location, volatility, and the sanitization procedure.

The following tables describe each memory type used in the instrument:

- "Non-Volatile Memory" on page 14
- "Volatile Memory" on page 18

Non-Volatile Memory

This section contains information on the types of non-volatile memory available in your instrument. It explains the size of memory, how it is used, its location, and the sanitization procedure.

Table 4-1 Summary of PXB Non-Volatile Memory

Memory Component, Type and Size	Writable During Normal Operation?	Data Retained When Powered Off?	Purpose/Contents	Data Input Method	Location in Instrument and Remarks	Sanitization Procedure
Board ID Memory (EEPROM) 256 Kb	No	Yes	Header EEPROM used to identify assembly and revision	Programmed before board assembly	N5105-63002 Interconnect Board (U300) N5105-80004	None
License Storage Memory (EEPROM) 512 Kb	No	Yes	Contains instrument serial number and license keys for instrument applications	Programmed before board assembly, when new licenses are installed, or by factory/service center calibration software	N5105-63003 Midplane Board (U32) N5105-80016	None
Control Logic Memory (CPLD) 32 macrocells	No	Yes	Contains configuration information for PCI Express switches and master/slave functionality	Programmed before board assembly or by factory/service center calibration software	N5105-63003 Midplane Board (U50) N5105-80011	None
PCIe SW1 Int Config Memory (EEPROM) 256 Kb	No	Yes	Contains configuration information for PCI Express switch 1 when using internal host	Programmed before board assembly. May be reprogrammed with switch manufacturer software	N5105-63003 Midplane Board (U57) N5105-80013	None
PCIe SW1 Ext Config Memory (EEPROM) 256 Kb	No	Yes	Contains configuration information for PCI Express switch 1 when using external host	Programmed before board assembly. May be reprogrammed with switch manufacturer software	N5105-63003 Midplane Board (U33) N5105-80002	None
PCIe SW2 Int Config Memory (EEPROM) 256 Kb	No	Yes	Contains configuration information for PCI Express switch 2 when using internal host	Programmed before board assembly. May be reprogrammed with switch manufacturer software	N5105-63003 Midplane Board (U34) N5105-80003	None
IO Expander (EEPROM) 64 bytes	Yes	Yes	Contains configuration for master versus slave operation	Programmed via user interface	N5105-63003 Midplane Board (U49)	None
(FLASH) 8 Mb	No	Yes	Contains configuration information for PCI Express FPGA	Programmed before board assembly. Field upgrade by service only	N5105-63204 Baseband Board (U52) N5105-80005 Contains no user data	None

Table 4-1 Summary of PXB Non-Volatile Memory

Memory Component, Type and Size	Writable During Normal Operation?	Data Retained When Powered Off?	Purpose/Contents	Data Input Method	Location in Instrument and Remarks	Sanitization Procedure
(FLASH) 8 Mb	No	Yes	Contains configuration information for PCI Express FPGA	Programmed before board assembly. Field upgrade by service only	N5105-63204 Baseband Board (U53) N5105-80006 Contains no user data	None
Board ID Memory (EEPROM) 256 Kb	No	Yes	Header EEPROM used to identify assembly and revision	Programmed before board assembly	N5105-63005 DRAM Board (U301) Contains no user data	None
EEPOT (EEMEM) 14 bytes	No	Yes	Stores optimum varactor bias for 100 MHz crystal oscillator	Programmed during board test and by service center	N5105-63006 Clock Board (U202) Contains no user data	None
(EEPROM) 256 Kb	No	Yes	Header EEPROM used to identify assembly and revision	Programmed prior to assembly	N5105-63006 Clock Board (U601) N5105-80015 Contains no user data	None
FLASH 4 Mb	No	Yes	Contains programming information for FPGA1 on Clock Board	Programmed prior to assembly. May be reprogrammed in the field by firmware upgrades	N5105-63006 Clock Board (U1219) N5105-80001 Contains no user data	None
CPLD XC9572XL 72 macrocells	No	Yes	Contains fixed digital logic associated with front-panel keyboard operation	Programmed prior to assembly. May be reprogrammed by the service center	N5105-63008 Front Panel Assy (U24) W1312-80018 Contains no user data	None
PIC mController PIC18LF445 24 KB FLASH 256 bytes EEPROM	No	Yes	Contains program code for front-panel microcontroller. Transmits key presses to system processor	Programmed prior to assembly. May be reprogrammed during a firmware upgrade	N5105-63008 Front Panel Assy (U17) W1312-80015 Contains no user data	None

Table 4-1 Summary of PXB Non-Volatile Memory

Memory Component, Type and Size	Writable During Normal Operation?	Data Retained When Powered Off?	Purpose/Contents	Data Input Method	Location in Instrument and Remarks	Sanitization Procedure
Display ID (EEPROM) 2 Kb	No	Yes	Extended display identification data is a standard data format that contains basic information about a monitor and its capabilities, including vendor information, maximum image size, color characteristics, factory preset timings, frequency range limits, and character strings for the monitor name and serial number	Programmed prior to assembly	N5105-63008 Front Panel Assy (U26) E6601-87009 Contains no user data	None
EEPROM 256 Kb	No	Yes	Header EEPROM used to identify assembly and revision	Programmed prior to assembly	N5105-63009 IO Board (U5) N5105-80008 Contains no user data	None
EEPROM	Yes	Yes	Contains configuration information for touchscreen performance and calibration	Programmed prior to assembly and is reprogrammed by touchscreen application	N5105-60018 Touchscreen Controller Contains no user data	None
Main Memory (Hard Disk Drive *or* Solid-State Drive) 160 GB	Yes	Yes	Contains operating system, instrument software, factory calibration data, recovery image, user instrument states, user data files, user trace data and any user-installed software	Programmed before assembly, by factory/ service center calibration software, or by software upgrade installation. Also via instrument software operations and by user	W1312-60057 Hardware platform processor Contains user data	None
CPU BIOS (CMOS NVRAM) 256 bytes	No	Yes	Contains default BIOS settings to use when booting the hardware platform processor	Programmed by factory and settings can be toggled by user	W1312-60057 Hardware platform processor battery backed-up to maintain calendar time. Contains no user data	None
Flash 14 Kbytes	No	Yes	Contains operating code for power supply mainframe	Programmed by Astec	Astec Power Supply Mainframe Contains no user data	None
Flash 14 Kbytes	No	Yes	Contains operating code for +12 Vdc power supply module	Programmed by Astec	Astec Power Supply +12 Vdc Module Contains no user data	None

Table 4-1 Summary of PXB Non-Volatile Memory

Memory Component, Type and Size	Writable During Normal Operation?	Data Retained When Powered Off?	Purpose/Contents	Data Input Method	Location in Instrument and Remarks	Sanitization Procedure
Flash 14 Kbytes	No	Yes	Contains operating code for +12 Vdc standby power supply module	Programmed by Astec	Astec Power Supply +12 Vdc Standby Module Contains no user data	None
Flash 14 Kbytes	No	Yes	Contains operating code for +5 Vdc and +16.5 Vdc power supply module	Programmed by Astec	Astec Power Supply +16.5 Vdc/ +5.1 Vdc Module Contains no user data	None
Flash 14 Kbytes	No	Yes	Contains operating code for +3.3 Vdc power supply module	Programmed by Astec	Astec Power Supply +3.3 Vdc Module Contains no user data	None

Volatile Memory

The PXB baseband generator and channel emulator also contains volatile memories. The volatile memories are not battery backed-up. They do not retain any information when AC power is removed.

Removing power from this memory meets the memory sanitization requirements specified in the “Clearing and Sanitization Matrix” in Section 5.2.5.5.5 of the ISFO Process Manual for the Certification and Accreditation of Classified Systems under the NISPOM.

Table 4-2 Summary of PXB Volatile Memory

Memory Component, Type and Size	Writable During Normal Operation?	Data Retained When Powered Off?	Purpose/Contents	Data Input Method	Location in Instrument and Remarks	Sanitization Procedure
FPGA XC4VFX60 56,880 cells 4,176 Kb RAM	Yes	No	Channel 1 switch matrix for data routing	Written to during application program execution	N5105-60002 Interconnect Board (U1) Contains no user data	Turn off instrument power
FPGA XC4VFX60 56,880 cells 4,176 Kb RAM	Yes	No	Channel 2 switch matrix for data routing	Written to during application program execution	N5105-60002 Interconnect Board (U2) Contains no user data	Turn off instrument power
USB Controller (RAM) 16 KB	Yes	No	Microcontroller for the Interconnect Board. Software communicates with this controller through USB interface	Written to during application program execution	N5105-60002 Interconnect Board (U302) Contains no user data	Turn off instrument power
DSP ADSP-TS201S (DRAM) 24 Mb	Yes	No	Computation data storage	Written to during application program execution	N5105-60104 Baseband Board (U35) Contains no user data	Turn off instrument power
DSP ADSP-TS201S (DRAM) 24 Mb	Yes	No	Computation data storage	Written to during application program execution	N5105-60104 Baseband Board (U36) Contains no user data	Turn off instrument power
Baseband signal processing ASIC control registers 192 bytes	Yes	No	Computation coefficient storage	Written to during application program execution	N5105-60104 Baseband Board (U37) Contains no user data	Turn off instrument power
Baseband signal processing ASIC control registers 192 bytes	Yes	No	Computation coefficient storage	Written to during application program execution	N5105-60104 Baseband Board (U38) Contains no user data	Turn off instrument power
SRAM 18 Mb	Yes	No	Computation data storage	Written to during application program execution	N5105-60104 Baseband Board (U54) Contains no user data	Turn off instrument power
SRAM 18 Mb	Yes	No	Computation data storage	Written to during application program execution	N5105-60104 Baseband Board (U55) Contains no user data	Turn off instrument power

Table 4-2 Summary of PXB Volatile Memory

Memory Component, Type and Size	Writable During Normal Operation?	Data Retained When Powered Off?	Purpose/Contents	Data Input Method	Location in Instrument and Remarks	Sanitization Procedure
SRAM 18 Mb	Yes	No	Computation data storage	Written to during application program execution	N5105-60104 Baseband Board (U56) Contains no user data	Turn off instrument power
(SRAM) 18 Mb	Yes	No	Computation data storage	Written to during application program execution	N5105-60104 Baseband Board (U57) Contains no user data	Turn off instrument power
(SRAM) 18 Mb	Yes	No	Computation data storage	Written to during application program execution	N5105-60104 Baseband Board (U58) Contains no user data	Turn off instrument power
(SRAM) 18 Mb	Yes	No	Computation data storage	Written to during application program execution	N5105-60104 Baseband Board (U59) Contains no user data	Turn off instrument power
(DRAM) 128 Mb	Yes	No	Computation data storage	Written to during application program execution	N5105-60104 Baseband Board (U60) Contains no user data	Turn off instrument power
(DRAM) 128 Mb	Yes	No	Computation data storage	Written to during application program execution	N5105-60104 Baseband Board (U61) Contains no user data	Turn off instrument power
FPGA XC3S1200 19,512 cells RAM 136 Kb distributed 504 Kb block	Yes	No	Logic function configuration data	Written to during application program execution	N5105-60104 Baseband Board (U68) Contains no user data	Turn off instrument power
FPGA XC4VSX55 55,296 cells 5,760 Kb RAM	Yes	No	Logic function configuration data	Written to during application program execution	N5105-60104 Baseband Board (U69) Contains no user data	Turn off instrument power
FPGA XC4VFX60 56,880 cells 4,176 Kb RAM	Yes	No	Logic function configuration data	Written to during application program execution	N5105-60104 Baseband Board (U79) Contains no user data	Turn off instrument power
FPGA XC4VSX55 55,296 cells 5,760 Kb RAM	Yes	No	Logic function configuration data	Written to during application program execution	N5105-60104 Baseband Board (U99) Contains no user data	Turn off instrument power
FPGA XC4VLX25 24,192 cells 1,296 Kb RAM	Yes	No	Data routing and memory controller	Written to during application program execution	DRAM Board (U1) Part of N5105-60104 Baseband Board Contains no user data	Turn off instrument power

Table 4-2 Summary of PXB Volatile Memory

Memory Component, Type and Size	Writable During Normal Operation?	Data Retained When Powered Off?	Purpose/Contents	Data Input Method	Location in Instrument and Remarks	Sanitization Procedure
(SRAM) 18 Mb	Yes	No	User waveform sequencing	Written to during application program execution	DRAM Board (U300) Part of N5105-60104 Baseband Board Contains no user data	Turn off instrument power
(DRAM) 1 Gb	Yes	No	User waveform storage	Written to during application program execution	DRAM Board Part of N5105-60104 Baseband Board Contains user signal data	Turn off instrument power
(DRAM) 1 Gb	Yes	No	User waveform storage	Written to during application program execution	DRAM Board Part of N5105-60104 Baseband Board Contains user signal data	Turn off instrument power
(DRAM) 1 Gb	Yes	No	User waveform storage	Written to during application program execution	DRAM Board Part of N5105-60104 Baseband Board Contains user signal data	Turn off instrument power
(DRAM) 1 Gb	Yes	No	User waveform storage	Written to during application program execution	DRAM Board Part of N5105-60104 Baseband Board Contains user signal data	Turn off instrument power
FPGA XC3S500 10,476 cells RAM 73 Kb distributed 360 Kb block	Yes	No	Controls the main phase lock loop for the system, and controls clock routing functionality of the PXB	Written to during application program execution	N5105-60006 Clock Board (U400) Contains no user data	Turn off instrument power
USB Controller (RAM) 16 KB	Yes	No	Microcontroller for the Clock Board. Software communicates with this controller through USB interface	Written to during application program execution	N5105-60006 Clock Board (U600) Contains no user data	Turn off instrument power
FPGA XC3S400 8,064 cells 360 Kb RAM	Yes	No	Controls trigger and marker functionality	Written to during application program execution	N5105-60006 Clock Board (U1000) Contains no user data	Turn off instrument power
PIC mController PIC18LF445 2 KB SRAM	Yes	No	Temporary storage used by front panel keyboard controller	Written to by normal keyboard use. Not accessible by user	N5105-60008 Front Panel Assy (U17) Contains no user data	Turn off instrument power

Table 4-2 Summary of PXB Volatile Memory

Memory Component, Type and Size	Writable During Normal Operation?	Data Retained When Powered Off?	Purpose/Contents	Data Input Method	Location in Instrument and Remarks	Sanitization Procedure
USB Controller (RAM) 16 KB	Yes	No	Microcontroller for the IO Board. Software communicates with this controller through USB interface	Written to during application program execution	N5105-60009 IO Board (U16) Contains no user data	Turn off instrument power
Baseband signal processing ASIC control registers 192 bytes	Yes	No	Registers which dictate Channel 1 baseband signal processing ASIC configuration	Written to during application program execution	N5105-60009 IO Board (U15) Contains no user data	Turn off instrument power
FPGA XC4VLX25 24,192 cells 1,296 Kb RAM	Yes	No	Controls IO functionality for Channel 1. Sets up the digital bus interface ports, communicates with the baseband signal processing ASIC, and controls analog output	Written to during application program execution	N5105-60009 IO Board (U13) Contains no user data	Turn off instrument power
Baseband signal processing ASIC control registers 192 bytes	Yes	No	Registers which dictate Channel 2 baseband signal processing ASIC configuration	Written to during application program execution	N5105-60009 IO Board (U18) Contains no user data	Turn off instrument power
FPGA XC4VLX25 24,192 cells 1,296 Kb RAM	Yes	No	Controls the IO functionality for Channel 2. Sets up the digital bus interface ports, communicates with the baseband signal processing ASIC, and controls analog output	Written to during application program execution	N5105-60009 IO Board (U17) Contains no user data	Turn off instrument power
(DRAM) 4 Gb	Yes	No	Main dynamic RAM memory for Intel processor. Contains working copies of operating system, instrument firmware personalities, calibration data, and measurement data	Written to by firmware operations and by the user	W1312-60057 Hardware platform processor. Contains user data. This memory is not battery backed-up or connected to standby power	Turn off instrument power

5 Using the Instrument in a Controlled Area

The only non-volatile user memory storage location in the instrument is the A14 Hard Drive Assembly. The remainder of the user-accessible memory storage is in volatile memory, which is deleted/erased when power is removed from the instrument.

The instrument does not have an erasure and sanitization procedure for the A14 Hard Drive Assembly.

When an instrument is used within a controlled area and the need arises to remove it from that controlled area, the security strategy is to remove the A14 Hard Drive Assembly from the instrument and leave the removed hard drive in the controlled area.

This chapter contains procedures to maintain security when placing the instrument in a controlled area, removing it from that area and then returning it to the controlled area:

- "Before Placing the Instrument in a Controlled Area" on page 24
- "Removing the Instrument from a Controlled Area" on page 24
- "Returning the Instrument to the Controlled Area" on page 25

Before Placing the Instrument in a Controlled Area

Before moving the instrument into a controlled area, ensure that the latest firmware revision is installed. Refer to the instrument firmware upgrade guide for complete instructions. This document is available at:

http://www.keysight.com/find/upgradeassistant

This is the same web page from which you can download the latest firmware revision.

Removing the Instrument from a Controlled Area

If you need to remove the instrument from a controlled area, you will need to remove the A14 hard drive assembly to prevent sensitive information from leaving the controlled area.

Use the following procedure while the instrument is located inside the controlled area:

Step	Action	Notes
1	Remove the A13 CPU Assembly	Refer to the PXB Guided Service and Support documentation for instructions. The most current version is available at the Technical Support tab of: http://www.keysight.com/find/pxb
2	Remove the A14 Hard Drive Assembly from the CPU Assembly.	
3	Annotate removed Hard Drive Assembly	On the hard drive assembly, mark the instrument model number, the serial number, and that it is for the controlled area. Store the hard drive assembly in the controlled area until the instrument is returned to this area.
4	Reinstall the A13 CPU Assembly in the instrument	The CPU Assembly is re-installed **without** the Hard Drive Assembly

At this point, the instrument may be removed from the controlled area.

Returning the Instrument to Keysight for Repair

The instrument can now be sent to the Keysight service center for repair, without the A14 Hard Drive Assembly installed.

IMPORTANT Be sure to note on the documents being shipped with the instrument to the Keysight repair center that the A14 Hard Drive has been removed to protect your sensitive information.

- If the instrument is under warranty, the A14 Hard Drive will be replaced without charge.
- If the instrument is out of warranty, the A14 Hard Drive will be replaced and you will be billed for this new assembly as part of the repair.

NOTE In both cases, the instrument will be returned with the A14 Hard Drive Assembly that was installed by Keysight repair personnel. After receiving the instrument back from the repair facility, follow the procedure described in "Returning the Instrument to the Controlled Area" on page 25 before placing it back in a controlled area.

Using or Repairing the Instrument in the Non-controlled Area

After the instrument has left the controlled area, to use or repair it in a non-controlled area, you will need a backup imaged hard drive to install into the CPU Assembly.

Step	Action
1	Before installing the backup hard drive, mark on it the instrument model number and serial number. It may also be good to mark that it is for the non-controlled area.
2	Remove the CPU Assembly from the instrument.
3	Install the hard drive into the CPU Assembly.
4	Reinstall the CPU Assembly into the instrument.

Returning the Instrument to the Controlled Area

This section provides detailed steps required to return your instrument to a controlled area after it was repaired or used outside the controlled area. Follow the applicable procedure listed below:

- If you removed the instrument from the controlled area to use it in a non-controlled area, refer to "After Using the Instrument in a Non-Controlled Area" on page 26.
- If you removed the instrument from the controlled area to send it for repair, refer to "After Repairing the Instrument" on page 26.

NOTE For instructions on installing and removing the A13 CPU and the A14 Hard Drive Assemblies, refer to the PXB Guided Service and Support documentation, which is available by selecting the Technical Support tab at:

http://www.keysight.com/find/pxb

After Using the Instrument in a Non-Controlled Area

Step	Action
1	While the instrument is still in the non-controlled area, remove the A13 CPU Assembly.
2	Remove the A14 Hard Drive Assembly from the CPU assembly.
3	If the Hard Drive Assembly is **not** labeled, mark the instrument model number and serial number and that the hard drive is designated for use in the non-controlled area. Store the hard drive assembly in an ESD-safe storage container in the non-controlled area.
4	Reinstall the A13 CPU Assembly (without the hard drive assembly) into instrument.
5	Move the instrument to the controlled area.
6	Once in the controlled area, remove the A13 CPU Assembly from the instrument again.
7	Install the original A14 Hard Drive Assembly into the A13 CPU Assembly. (This is the Hard Drive Assembly for this instrument serial number that was removed from the instrument and stored in your controlled area, before the instrument was removed from the controlled area.)
8	Reinstall the CPU Assembly, with the hard drive, into the instrument. The instrument is now ready for use in the controlled area.

After Repairing the Instrument

While the instrument is still in the non-controlled area, read the repair documentation to identify the cause of repair, because this determines the procedure that you should follow at this point.

- If the repair documentation indicates that the A14 Hard Drive Assembly **was** the cause of the repair, you need only move the instrument into the controlled area. The instrument is now ready for use.
- If the repair documentation indicates that the A14 Hard Drive Assembly was **not** the cause of the repair, the hard drive returned with the instrument should be removed from it and kept in the non-controlled area, for use outside the controlled area, as follows:

Step	Action
1	Remove the A13 CPU Assembly from the instrument.
2	Remove the A14 Hard Drive Assembly from the CPU Assembly.
3	On the Hard Drive Assembly that you just removed, mark the instrument model number and serial number, and that it is for use in the non-controlled area. Store the hard drive assembly in an ESD-safe storage container in the non-controlled area.
4	Reinstall the A13 CPU Assembly (without the hard drive assembly) into the instrument.
5	Move the instrument to the controlled area.
6	Once the instrument is back in the controlled area, remove the A13 CPU Assembly again.
7	Install the original A14 Hard Drive Assembly into the A13 CPU Assembly. (This is the Hard Drive Assembly for this instrument serial number that was removed from the instrument and stored in your controlled area, before the instrument was removed from the controlled area.)
8	Reinstall the CPU Assembly, with the hard drive, into the instrument. The instrument is now ready for use in the controlled area.

A: References

1. **DoD 5220.22-M, "National Industrial Security Program Operating Manual (NISPOM)"**
United States Department of Defense. Revised February 28, 2006.
May be downloaded in Acrobat (PDF) format from:
http://www.dss.mil/isp/fac_clear/download_nispom.html

2. **ISFO Process Manual for the Certification and Accreditation of Classified Systems under the NISPOM**
Defense Security Service.
DSS-cleared industries may request a copy of this document via email, by following the instructions at:
http://www.dss.mil/isp/odaa/request.html

References