Excerpt Edition

This PDF is an excerpt from Chapter 1
of the Parametric Measurement Handbook.

The Parametric Measurement Handbook

Third Edition
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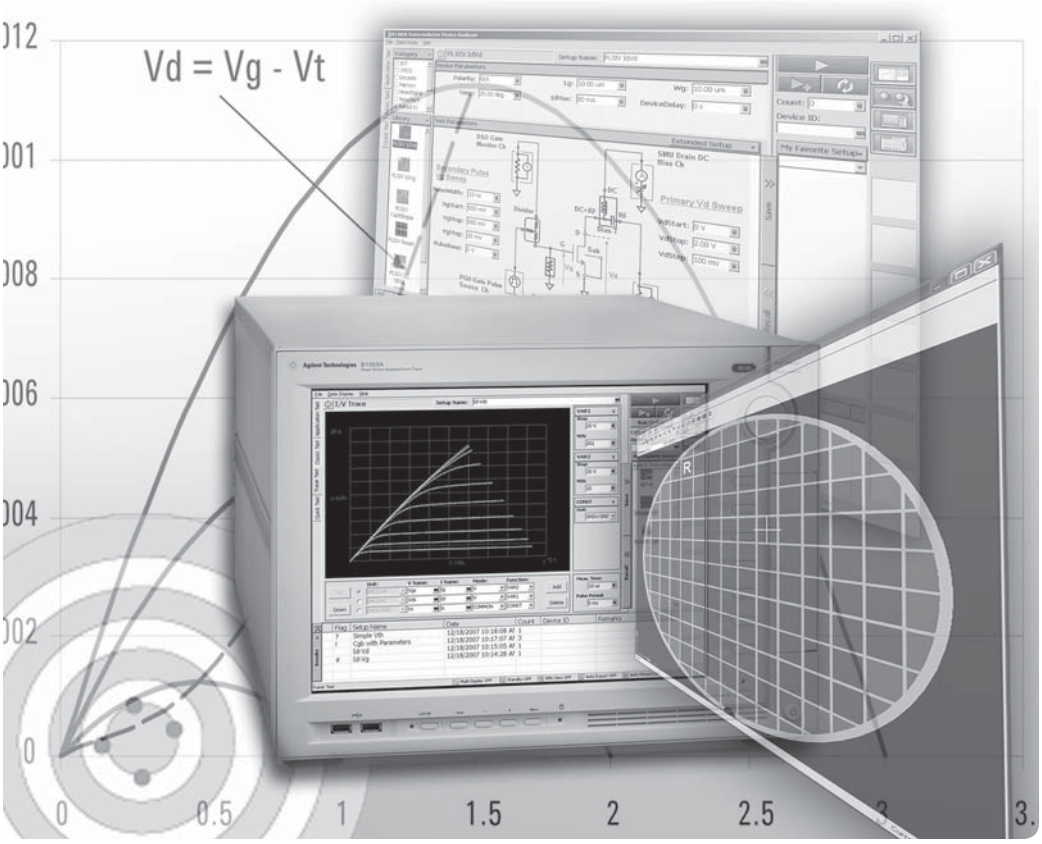


Agilent Technologies

Chapter 1: Parametric Test Basics

"The central activity of engineering, as distinguished from science, is the design of new devices, processes and systems." — Myron Tribus

What is parametric test?

The question as to what constitutes parametric test is an interesting one and is possibly open to some debate. Nevertheless, in general parametric test involves the electrical testing and characterization of four main types of semiconductor devices: resistors, diodes, transistors, and capacitors. This is not to say that parametric test never involves the testing of other device types; however, the vast majority of parametric test structures can be classified into one of these categories or considered to be a combination of these categories.

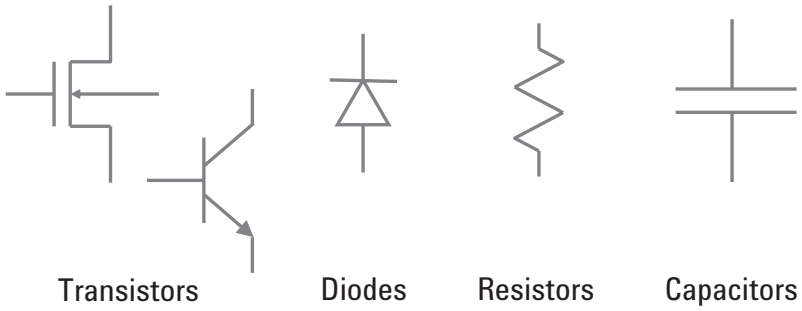


Figure 1.1. Parametric test involves the testing of these four basic device types.

The vast majority of parametric testing involves either current versus voltage (IV) or capacitance versus voltage (CV) measurements.

To many people parametric test means "DC" testing, but this is not an accurate description. Of course, it can take source/monitor units (SMUs) anywhere from milliseconds to seconds to make a measurement, which is certainly "slow" by the standards of functional testers (which typically perform measurements in the nanosecond or picosecond range). However, in recent years the need to perform extremely fast parametric measurements (1 µs spot measurements with data sampling rates in the nanosecond range) has greatly increased. This has required the creation of new measurement module types (such as the waveform generator/fast measurement unit or WGFMU) to meet this need. Extremely fast IV and pulsed IV measurements will continue to take on increased importance in the future, as transistor lithographies continue to shrink and more exotic materials are incorporated into semiconductor processes.

One major subcategory of parametric test is reliability testing. Reliability testing relies heavily upon the well-known Arrhenius equation that expresses the rate constant (k) of a chemical reaction as follows:

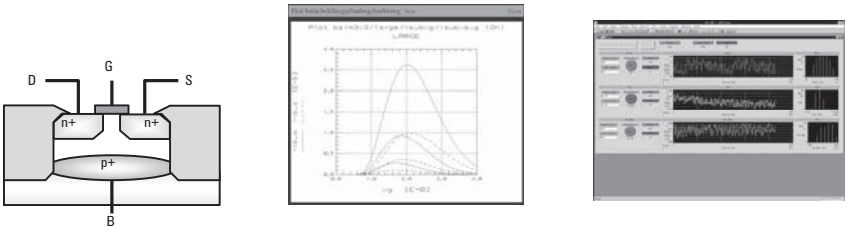
$$k = Ae^{-\frac{E_a}{RT}}$$

Where: A is the pre-exponential factor
Ea is the activation energy
R is the ideal gas constant
T is the temperature in degrees Kelvin

In reliability testing devices are typically stressed by the application of large currents and/or voltages (larger than that experienced by the devices under normal operation) to lower the value of the activation energy and thereby increase the rate of the failure mechanism. Temperature is also often increased to achieve this same purpose. Once the failure mechanism occurs then the expected failure rate under normal operating conditions can be extrapolated using a variety of mathematical and statistical techniques.

Why is parametric test performed?

The purpose of parametric test is to determine the characteristics of a semiconductor manufacturing process. Broadly speaking, parametric test covers three main areas: process development, process modeling, and process production.



Process development | Device modeling | Process control

Figure 1.2. Parametric test focuses in three main areas: process development, device modeling, and process control.

The first two of these areas are performed in a laboratory, R&D or pre-production environment, while the last one is obviously performed in a manufacturing environment. The parametric equipment used in these disparate environments obviously has different requirements, with benchtop instruments being used for process development and process modeling and high-throughput testers being used for process production.

Figure 1.3. A production parametric tester is designed to optimize throughput

It is important to understand that parametric test is almost never performed on final products. Instead it is performed on special structures that are designed to yield information about the process itself. Parametric test is also generally performed directly on semiconductor wafers. In production test the parametric test structures are sometimes located in the scribe lanes or "streets" of the wafer to minimize the wafer area taken up by these devices. However, for process development and reliability testing entire wafers of nothing but parametric test structures are often fabricated.

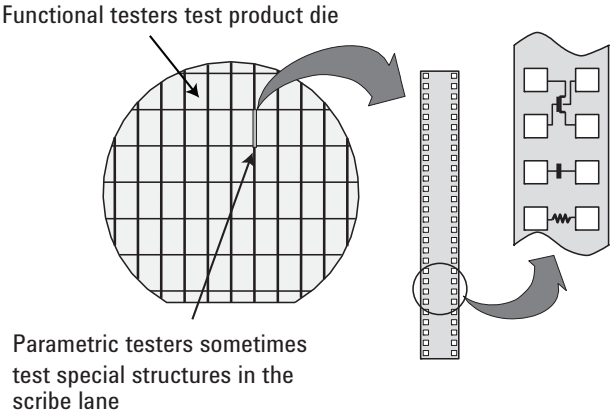


Figure 1.4. To conserve valuable wafer area, parametric test structures are sometimes placed in the wafer's scribe lines (or "streets").

Where is parametric test done?

In production, parametric test is typically performed on the wafers after they have completed the wafer fabrication process (i.e. after passivation has been applied) but before electrical sort (E-sort) on the functional product dice.

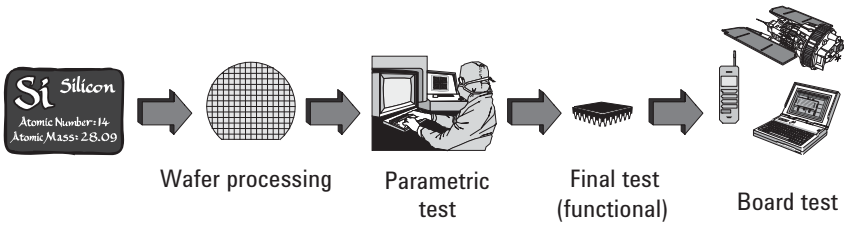


Figure 1.5. Parametric test performed after wafer fabrication is complete but before functional product verification.

Each wafer from every lot is tested and the data is stored into a database. Obviously, the amount of data is quite massive, and various software tools are employed to manipulate the data into a variety of different formats. One popular format is the wafer map, where a scalar quantity is plotted across a wafer using different colors for different ranges of the data value.

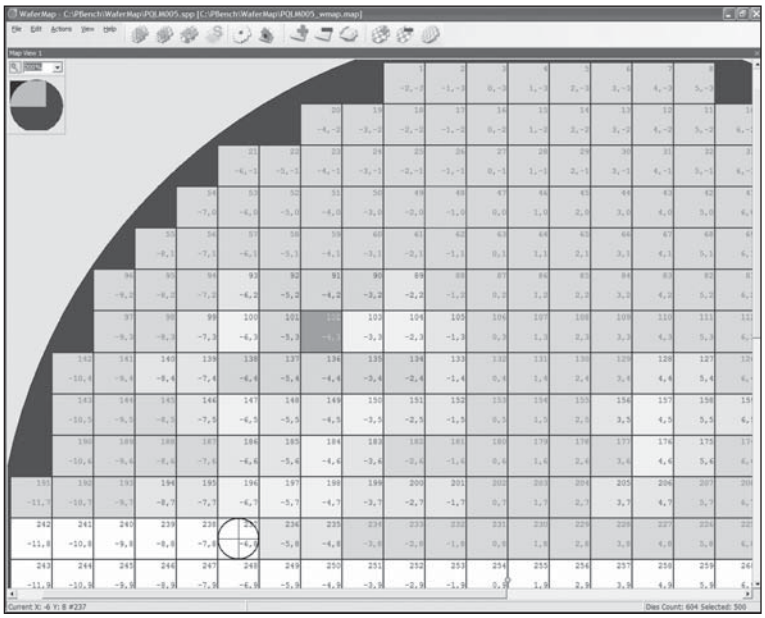


Figure 1.6. Wafer map example.

For advanced processes, conventional test structures placed in the scribe lines or even drop-in test die placed around the wafer may not be sufficient to adequately characterize the process. Advanced processes typically require much more testing due to their innate complexity, and it is sometimes difficult to fit all of the necessary test structures into the available area. Unfortunately, the tips of the probe card have physical limitations on how small they can be made and still maintain reasonable probe card lifetimes, which in-turn creates physical limits on the minimum size of the probe pads. This means that the pads cannot physically scale down as devices scale down with each new process generation.

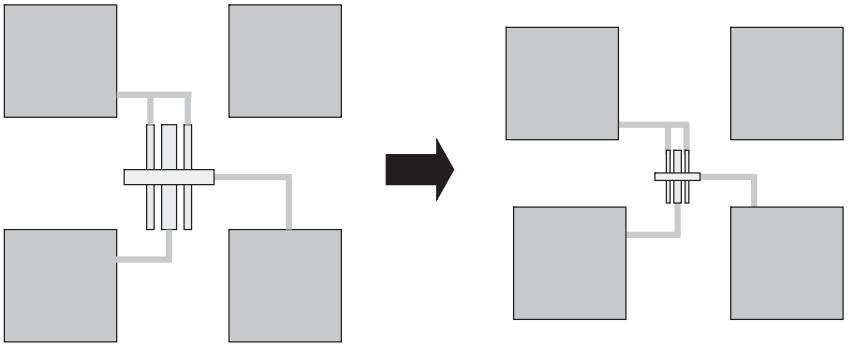


Figure 1.7. Pad size cannot scale with design rule changes, which limits the number of conventional test structures that can be placed on a wafer.

One solution to this issue is to use arrays, since an array allows test devices to share pads and thereby improve the test device to pad ratio. An example of this scheme is shown below.

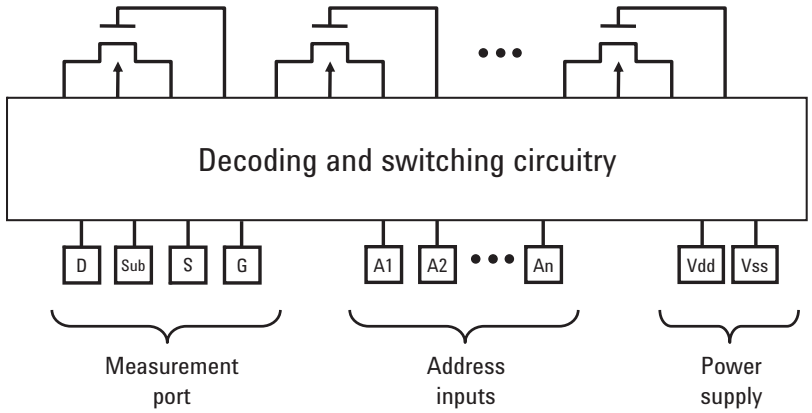


Figure 1.8. An example of an addressable array scheme used for production parametric test.

Addressable arrays can offer significant throughput improvement over conventional test device arrangements, although achieving substantial test time reduction requires a complete re-engineering of all of the parametric test processes.

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If you want to have more information, visit the following URL. You can get the complete "Parametric Measurement Handbook". This total guide contains many valuable information to measure your semiconductor devices accurately, also includes many hints to solve many measurement challenges. Now, English, Japanese, Traditional Chinese, and Simplified Chinese versions are available.

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