Advanced Design System 2014_01 Hotfix Release Notes

Hotfix Release Notes

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Table of Contents

Table of Contents **3**

Chapter 1 – ads_2014_01_hf3 Release Notes **5**

1.1 Version 5

1.2 Platform Support 5

1.3 Issues Addressed 5

1.3.1 Artwork 5

1.3.2 Circuit Simulation 5

1.3.3 DesignGuide 6

1.3.4 Dynamic Link 6

1.3.5 FEM Simulation 6

1.3.6 Momentum Simulation 6

1.3.7 Design Rule Check (DRC) 6

1.3.8 Layout versus Schematic 6

1.3.9 Installation 7

1.3.10 Instrument Links 7

1.3.11 Layout 7

1.3.12 Platform 8

Chapter 2 – ads_2014_01_hf2 Release Notes **9**

2.1 Version 9

2.2 Platform Support 9

2.3 Issues Addressed 9

2.3.1 ADFI 9

2.3.2 Circuit Simulation 9

2.3.3 EM Simulation 10

2.3.4 Design Rule Check 10

2.3.5 Layout versus Schematic 10

2.3.6 Instrument Links 11

2.3.7 Platform 11

2.4 Improvements (if any) 11

Chapter 3 – ads_2014_01_hf1 Release Notes 12
3.1 Version 12
3.2 Platform Support 12
3.3 Issues Addressed 12
3.3.1 ADFI 12
3.3.2 AEL 12
3.3.3 Artwork Translators 12
3.3.4 Circuit Simulation 12
3.3.5 Circuit Simulation - Electrothermal 13
3.3.6 Data Display 13
3.3.7 EM Simulation 13
3.3.8 Examples 13
3.3.9 Layout versus Schematic 14
3.3.10 PCB 14
3.3.11 Platform 14
3.3.12 Verilog-A 14
3.4 Improvements (if any) 15
3.4.1 AEL 15
3.4.2 Data Display 15

Chapter 1 – ads_2014_01_hf3 Release Notes

Release 27 August 2014

1.1 Version

410.hf3

1.2 Platform Support

- **Supported Platforms**: Windows and Linux only

1.3 Issues Addressed

This hotfix addresses various issues related to Artwork, Circuit Simulation, EM, DRC, LVS, IC Design Flow, Instrument Links, Installation, and Platform.

1.3.1 Artwork

- 95819: GDSII export/re-import works on fixed artwork.
- 98681: Top level GDSII import does not displays error with blank cell in ADS2014.01.

1.3.2 Circuit Simulation

- 98490: DC bias annotation issue is fixed even if the current probe is activated.
- 91099: Floorplanner: Improved error handling of missing heat and default layer on initial ghost draw.
- 94784: bsource can be probed error for bsource1 i=i(bsource2) and bsource2 r=exp(v(n3,0)).
- 97708: spectre nport in subckt works in ADS subcricuit (inside define/end, i.e., subcircuit header/footer in ads syntax).
- 88849: Floorplanner: Allows heat sources to be placed into a subcell.

1.3.3 DesignGuide

- 98674: DDR4 DesignGuide is supported.

1.3.4 Dynamic Link

- 95752: Fixed the RFIC DynamicLink higher load average problem.
- 97016: Fixed the issue with eesofg2p process that becomes idle consuming CPU.
- 97075: ADS Dynamic Link node probing only works for top level Cadence schematic
- 97927: Fixed the Cadence design variable g1=pcomplex(a1, b1) issue that gets split up by Dynamic Link.

1.3.5 FEM Simulation

- 95100: Sheet ports properties are now picked up in 3D component flow.
- 96114: Fixed the 3D Viewer crash when using the EM Circuit Excitation flow with FEM-based EM Model.

1.3.6 Momentum Simulation

- 13980, 97232, 97580: Fixed a memory allocation issue that led to a segmentation violation for very large designs.
- 29774, 38292, 85341, 96139: Fixed an error in the direct compressed matrix load where some coupling contributions were ignored in specific circumstances (typically involving TML calibration cells).
- 92939: Correct material properties (instead of perfect conductor) are applied for the vertical cells at thick conductor ports.

1.3.7 Design Rule Check (DRC)

- 92611: Removed the limitation of running Assura DRC through ADS-Assura link.
    - 99251: (Duplicate) Fixed the DRC Layer map definition problem.

1.3.8 Layout versus Schematic

- 99006: Fixed the LVS Incorrect Nodal/Parameter Mismatch by wrong component treat.

- 98357: Fixed the Desktop LVS UI issue that adds a new wire on the original wire in layout on drc_err_layer.
- 99554: Fixed the LVS syntax issues that changes for new device replace function.
- 99565: Device callback max seg length is returning correct length.
- 93114: Fixed the unrecognized Pin connection on Device Recognition LVS.
- 93440: Fixed the LVS incorrect Parameter Mismatch issue.
- 95442: Fixed the pin count mismatch errors for terms associated with area pins.
- 95451: Fixed the Device Recognition: Performance issue when Check Parameter Mismatches is enabled.
- 95454: List component and net mappings alphabetically by first and second column of data.
- 95676 Device Recognition LVS uses instance names to resolve ambiguity.
- 96076: LVS Components with Pin Nets uses instance names to resolve ambiguity.
- 97706: Similar hierarchy does not display sub elements for some designs
- 97909: Instance name mapping is supported when the device key shape cuts the instance bounding box.
- 94643: Provides ability to group similar devices as one family.

1.3.9 Installation

- 94865: Supported Patch OpenSSL Libraries to avoid Customer corporate security issues with ADS due to Heartbleed bug.
    - 96117: (Duplicate) IT identified vulnerabilities for the “heart bleed” bug in ADS2014.01.

1.3.10 Instrument Links

- 98329: Fixed the Connection Manager crash when in Command Expert mode and Instrument IP address is set to "localhost".
- 97331: Fixed the defect of CM_ESG_E4438C_Sink in ADS2014.01 hf2 on OS=Linux.

1.3.11 Layout

- 95217: Fixed two issues for OA customer Via.

- 93273: Lock component now cannot be moved.

1.3.12 Platform

- 96073: (IC Interoperability) Miltiplier now works fine when used with pPar.

Chapter 2 – ads_2014_01_hf2 Release Notes

Release 24 June 2014

2.1 Version

410.hf2

2.2 Platform Support

- **Supported Platforms**: Windows and Linux only

2.3 Issues Addressed

This hotfix addresses various issues related to ADFI, Circuit Simulation, FEM, DRC, LVS, IC Design Flow, Instrument Links, and Platform.

2.3.1 ADFI

- 25298: Improved export of Cadence Package Designer and SiP designs
- 83802: Wildcard now working as expected when browsing for nets in ADFI window in Allegro.
- 89978: Pin text height and symbol size can be updated from Adfi Tools menu.
- 90641: The transfer of manufacturing film masks is now supported
- 90642: Enhanced component selection filters
- 92402: Fixed csv import of ebond instances in Bondwire Utilitiy Kit version 0.12.

2.3.2 Circuit Simulation

- 93207: mint spectralnoise calculations seem off for correlated noise.
- 95220: Changed the model latency scan range from 100 to 200.
- 95684: STMicroelectronics changed the OP definitions for the UTSOI2.

- 92756: Added support for HSPICE BSIM level 72 and binning on L.
- 92591: Fixed ADS vs HSPICE results for W-element.
- 91627: Fixed simulation errors with workspace that uses a Hspice netlist.
- 92303: Fixed problem with IBIS 5.1 parser.
- 92962: Added support of 4-terminal PSP 103.2 model with self heating.
- 92966: Added support of MOSVAR 1.2.
- 93295: ADS vs Spectre: NFmin and RN difference.
- 92907: Fixed crash while tuning in a test lab.

2.3.3 EM Simulation

- 93092: 2 port FEM simulation result with TML cal port and None cal port shows the wrong phase. This issue is fixed.
- 93699: Initial Target Mesh size setting is now pass to FEM simulation.
- 94701: Fixed a scale factor issue in 2D plots of power related far field quantities like Gain, Directivity, Radiation Intensity and Effective Area (Momemtum).

2.3.4 Design Rule Check

- 93154: The ADS-Assura DRC link no longer exits if the LayerMap file does not contain layer numbers for the DRC error layers.
- 92611: The ADS-Assura DRC link now displays results in the viewer.

2.3.5 Layout versus Schematic

- 92433: Ignore ADS simulation components like sprobe, iprobe.
- 93439: Improvements to component mapping.
- 88977: List all components and physical nets including those that have not been mapped.
- 92349: Specify tolerance of calculated parameter as a percentage.
- 81847: Recognize deactivated components in schematic.

- 93818: Recognize deactivated subcircuits in schematic.

2.3.6 Instrument Links

- 95107: AutoScaling now works well with setting DownloadMode=write_to_datafile in CM_ESG_E4438C_Sink.
- 90717: Added ael function to set the setup type in emSetup. Need to set EM Cosimulation for ADFI imports with components that only have circuit simulation capabilities.
- 94081: Added ael functions to get and set emsetup setuptype.

2.3.7 Platform

- 85831: The version of OA has been upgraded to prevent a corrupted string table.
    - 91084 (*Duplicate*): The version of OA has been upgraded to prevent a corrupted string table.
    - 92580 (*Duplicate*): The version of OA has been upgraded to prevent a corrupted string table.
    - 94678 (*Duplicate*): The version of OA has been upgraded to prevent a corrupted string table.
    - 95029 (*Duplicate*): The version of OA has been upgraded to prevent a corrupted string table.
    - 95363 (*Duplicate*): The version of OA has been upgraded to prevent a corrupted string table.
- 92157: Fixed error message when de_set_item_parameters() is called for SnP.
- 92334: Version Control: Copy Cell results in error if destination cell is managed and NOT checked out.
- 92337: Version Control: Move Cell results in error if destination cell is managed and NOT checked out.
- 92338: Version Control: ADS doesn't abort delete when SOS reports an error during deletion.

2.4 Improvements (if any)

Chapter 3 – ads_2014_01_hf1 Release Notes

Release 1 May 2014

3.1 Version

410.hf1

3.2 Platform Support

- **Supported Platforms**: Windows and Linux only

3.3 Issues Addressed

This hotfix addresses various issues related to ADFI, AEL, Artwork Translators, Circuit Simulation, Data Display, EM Simulation, Examples, IC Design Flow, PCB, Platform, and Verilog-A.

3.3.1 ADFI

- 89770: Fixed the ADFI import of traces with consecutive arced segments with same radius but different chord lengths.

3.3.2 AEL

- 89482: write_hdf5() exports an extra folder called "Top" during write operation. This issue has been fixed.

3.3.3 Artwork Translators

- 91613: Fixed crash when ADS runs in no window (-nw) mode.

3.3.4 Circuit Simulation

- 89778: Added 128B/132B encoding options.

3.3.5 Circuit Simulation - Electrothermal

- 88641: Write electrothermal temperatures and powers to the dataset for Transient.
- 89458: Added the ability to reuse `.ptval` file on Windows.
- 90455: Improved the power dissipation (Pdiss) calculation for passive components.
- 91099: Improved error handling of missing heat layer and default layer when drawing the initial ghost image in the Floorplanner.
- 91371: Improved the simulation of large heat sources. Added an option to use the center (peak) temperature instead of the volume average temperature.
- 91450: Added an option to not automatically open the thermal viewer after the electrothermal simulation is complete.

3.3.6 Data Display

- 88714: Added the ability to handle a `.adx` file that is created by merging a group of other `.adx` files (ParameterizedAdxFile) in "reference" mode.

3.3.7 EM Simulation

- 88782: The EM Model no longer supports a non-grounded reference node. Transient simulations with an EM Model impose this restriction, which is always enforced now by the EM Model view netlisting.
- 90777: The EBOND shape lookup no longer displays shapes that are not within the scope of the simulation.
- 91181: An FEM simulation runs properly now with an instance of an EBOND bondwire in a symmetry plane.
- 91335: Fix for the FEM-based EM Model S-parameter data interpolation. The interpolation could be wrong when the imaginary part of the S-parameter changes sign.
- 92025: Fix for opening the 3D visualization environment from an EM Model when data files are very large (proj.msf > 2GB).

3.3.8 Examples

- 92786: Updated the EM examples available under `$HPEESOF_DIR\examples\Training\EM`.

3.3.9 Layout versus Schematic

- 90050: Fixed LVS component highlighting and alignment issue.
- 92739: Changed the Net mappings highlighting color.
- 87014: Add a check box to disable physical/nodal warnings.
- 90217: Do not show physical/nodal mismatches for Device Recognition LVS.
    - 90433 (*Duplicate*): Physical highlight calculation results in delay in running LVS.

3.3.10 PCB

- 91472: Changed the ADS Board Link root keyword from <AgilentBoardLink> to <ABLRoot>. Import will accept both old and new root keyword whereas export only accepts the new keyword.

3.3.11 Platform

- 91278: Fixed crash when ADS runs in no window (-nw) mode.
- 92006: Using copy/paste or swapping CDF instances will now retain parameter values.

3.3.12 Verilog-A

- 89418: Using current port access operator I(<p>) in hierarchical Verilog-A code causes connectivity error.
- 89744: "vams auto_encrypt" utility not working on Windows and unable to read encrypted Verilog-A on Windows.
- 90547: Verilog-AMS shuts down the digital simulator during pseudotran.
- 90965: Verilog-A model parameters that could be varied in tune mode in 2013.01 are no longer variable.
- 91888: Verilog-A outvars available in 2013.06 are no longer in the dataset.

3.4 Improvements (if any)

3.4.1 AEL

- 89481: The data exported using the write_hdf5() is now written as 32 floats in HDF5 file.

3.4.2 Data Display

- 88851: Improved the representation of VTB swept data in DDS.