Agilent TS-8989 PXI Functional Test System

Diagnostics User's Guide

Agilent Technologies

Notices

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Any adjustment, maintenance, or repair of this product must be performed by qualified personnel. Contact your customer engineer through your local Agilent Service Center.

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You can find information about technical and professional services, product support, and equipment repair and service on the web: http://www.agilent.com/

Double-click the link to **Test & Measurement**. Select your country from the drop-down menus. The web page that appears next has contact information specific for your country.

Agilent by phone

If you do not have access to the Internet, call one of the numbers in the "Contact us" section at the end of this manual.

2
Safety and Regulatory Information

Safety Summary

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Agilent Technologies, Inc. assumes no liability for the customer's failure to comply with these requirements.

Safety Notices

CAUTION

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WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

General Safety Considerations

This product is provided with a protective earth terminal. The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

WARNING

- **DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE. Do not operate the product in the presence of flammable gases or flames.**
- **DO NOT REMOVE RACK PANELS OR INSTRUMENT COVERS. Operating personnel must not remove any rack panels or instrument covers. Component replacement and internal adjustments must be made only by qualified service personnel. Products that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by a qualified service personnel.**
- **The protection provided by the TS-8989 system may be impaired if the system is used in a manner not specified by Agilent.**

Environmental Conditions

The TS-8989 Automotive Electronics PXI Functional Test System is designed for indoor use only. Table 2-1 shows the general environmental requirements.

Table 2-1 General environmental requirements

Environment condition	Requirement
Maximum altitude	2000 meters
Operating temperature	5 °C to 40 °C
Relative humidity	The test system is designed to operate in the range from 5% to 80% relative humidity (non-condensing)

CAUTION This product is designed for use in Installation Category II and Pollution Degree 2, per IEC 61010-1 and 664 respectively.

Before Applying Power

Verify that the product is set to match the available line voltage and that all safety precautions are taken. Note the external markings of the instruments described in "Safety Symbols and Regulatory Markings".

Ground the System

Agilent chassis' are provided with a grounding-type power plug. The instrument chassis and cover must be connected to an electrical ground to minimize shock hazard. The ground pin must be firmly connected to an electrical ground (safety ground) terminal at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Fuses

Use only fuses with the required rated current, voltage, and specified type (fast acting). Do not use repaired fuses or short-circuited fuse holders. Doing so could cause a shock or fire hazard.

WARNING **To avoid electrical hazards, all system internal fuses must be replaced by trained and qualified personnel.**

Operator Safety Information

WARNING **Module connectors and test signal cables connected to them cannot be operator-accessible.**

Cables and connectors are considered inaccessible if a tool (such as a screwdriver, wrench, or socket) or a key (for equipment in a locked cabinet) is required to gain access to a conductive surface connected to any cable conductor (High, Low, or Guard).

WARNING **Do not touch the exposed connector pins or remove connected cables while the system is powered ON (see Figure 2-1).**

Figure 2-1 Examples of exposed connectors

Safety Symbols and Regulatory Markings

Symbols and markings on the system, in manuals, and on instruments alert you to potential risks, provide information about conditions, and comply with international regulations. Table 2-2 defines the symbols and markings you may find in a manual or on an instrument.

Table 2-2 Safety symbols and regulatory markings

Symbol	Description
Safety symbol	
	Warning: risk of electrical shock.
	Warning: hot surface.
	Caution: refer to accompanying documents.
	Laser radiation symbol: marked on products that have a laser output.
	Alternating current.
	Both direct and alternating current.
	3-phase alternating current.
	Earth (ground) terminal.
	Protective earth (ground) terminal.

Table 2-2 Safety symbols and regulatory markings (continued)

Symbol	Description
	Frame or chassis terminal.
	Terminal is at earth potential. Used for measurement and control circuits designed to be operated with one terminal at earth potential.
	Terminal for a neutral conductor on permanently installed equipment.
	Terminal for a line conductor on permanently installed equipment.
	Standby (supply); units with this symbol are not completely disconnected from the AC mains when this switch is turned off. To completely disconnect the unit from the AC mains, either disconnect the power cord, or have a qualified electrician install an external switch.
Regulatory marking	
	The CE mark is a registered trademark of the European Community. If it is accompanied by a year, it indicates the year the design was proven.
	The CSA mark is a registered trademark of the Canadian Standards Association.
	The C-tick mark is a registered trademark of the Spectrum Management Agency of Australia. This signifies compliance with the Australian EMC Framework regulations under the terms of the Radio Communications Act of 1992.
ISM - 1A	This text indicates that the instrument is an Industrial Scientific and Medical Group 1 Class A product (CISPER 11, Clause 4).

Declaration of Conformity

The Declaration of Conformity (DoC) for this instrument is available on the Agilent website. You can search the DoC by its product model or description at the web address below.

http://regulations.corporate.agilent.com/DoC/search.htm

NOTE If you are unable to search for the respective DoC, contact your local Agilent representative.

Electrostatic Discharge (ESD) Precautions

Static electricity is destructive to your production process and the TS-8989. Careless handling and poor site planning can cause system reliability problems and reduce your product yield. The system may not be as easily damaged as the modules you will be testing, but good anti-static planning will help ensure high reliability.

The ESD symbol below indicates areas where ESD caution must be exercised. This is to prevent damage to instruments and/or test disruption.

Caution: static sensitive

Electrostatic discharge in this area may cause equipment damage and/or test disruption.

While not an exhaustive list of anti-static precautions, Table 2-3 provides suggestions to consider as you plan your system area.

Table 2-3 Suggested anti-static solutions for site planning

Precaution	Suggested solution
Anti-static flooring	Plan to use an anti-static floor covering or mats.
Grounding straps	Plan for foot straps in conjunction with anti-static flooring and wrist straps for system operators.

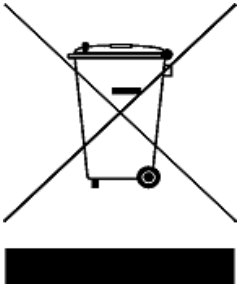
End of Life: Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC

This instrument complies with the WEEE Directive (2002/96/EC) marking requirement. This affixed product label indicates that you must not discard this electrical or electronic product in domestic household waste.

Product Category:

With reference to the equipment types in the WEEE directive Annex 1, this instrument is classified as a "Monitoring and Control Instrument" product.

The affixed product label is as shown below.



Do not dispose in domestic household waste.

To return this unwanted instrument, contact your nearest Agilent Service Center, or visit

www.agilent.com/environment/product

for more information.

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3
Running Diagnostics

This chapter describes the overview of the diagnostic testplans, the DGN testplan, and the CEDGN testplan. It also teaches you to use the diagnostics test fixtures to verify the operation of the system equipment.

NOTE Diagnostic testing is intended to verify basic connectivity and instrument functionality. It does not provide a full functional test of instrumentation and specifications.

Overview of Diagnostics Testplans

Standard diagnostic testplans are shipped with each system. There are two different testplans to test the system, from functionality to internal connections, to connections on the Test System Interface.

The first testplan, called the DGN, is used to verify both the core system instrument operation and internal test paths. No hardware is required to run this testplan. It verifies about 50% of the system functionality.

The second testplan, the “Customer Engineer Diagnostics” testplan or simply CEDGN, is used to complete the test coverage. This test requires external hardware, which is packaged as a CEDGN kit, because it verifies the internal connections out to the Test System Interface.

The tests are executed in the Agilent TestExec SL software and the TS-8989 system programming environment using both standard and specialized test actions. The testplans only cover standard instruments in the system. If there is a special case where non-standard equipment are incorporated into the system, tests for these equipment would have to be added.

Standard instruments and the system.ust file

Before running the DGN or CEDGN testplans, instruments in the system have to be added to the *system.ust* file. Testplans can access and control instruments only if they have been added into the *system.ust* file.

Standard instruments in the TS-8989 are included in the DGN and CEDGN testplans. A ✔ (tick) next to an instrument shows that it is included in the DGN or CEDGN testplan.

Table 3-1 List of standard instruments in the TS-8989 system

P/N	Description	DGN	CEDGN
E6198B	21-Slot Switch/Load Unit	✔	✔
E8792A	32 Measurement Channels and 16 Instrument Channels Matrix Card	✔	✔
E8793A	32-Pin Matrix Card	✔	✔
E8782A	40 Measurement Channels and 24 Instrument Channels Matrix Card	✔	✔
E8783A	64-Pin Matrix Card	✔	✔
E6175A	8-Channel Load Card		✔
E6176A	16-Channel Load Card		✔
E6177A	24-Channel Load Card		✔
E6178B	8-Channel Load Card		✔
U7177A	24-Channel Load Card with Current Sense		✔
U7178A	8-Channel Heavy Duty Load Card		✔
U7179A	16-Channel High Current Load Card		✔
N9377A	16-Channel Dual-Load Load Card		✔
N9378A	24-Channel Low Resistance Load Card		✔
N9379A	48-Channel High-Density Load Card		✔
M9182A	DMM	✔	✔
M9183A	DMM	✔	✔
M9186A	V/I Source	✔	✔
M9185A	8-Channel/16-Channel DAC	✔	✔
M9216A	32-Channel HV-DAQ	✔	✔
M9187A	32-Channel PXI DIO	✔	✔
AD1750	32-Channel PCI DIO	✔	✔
Softing CAN	2 Channel CAN	✔	✔

Configuring the system.ust file in the System Configuration Editor

1 Start the System Configuration Editor by clicking this icon on your desktop:

2 Click on the *detected on system* button. The screen will show instruments detected on the system. Any instrument in Table 3-1 which is in your system should be detected.

3 Double-click on the instrument name to add it to the *system.ust* file. It is recommended that you add instruments in the following order:

i the SLU,

ii the first pin matrix card in the SLU, and

iii other instruments in any order.

NOTE At least 1 SLU, 1 Pin Matrix, and 1 DMM must be in the system and in the *.ust* file for the DGN and CEDGN testplans to run.

4 Once the instruments have been added, click **Save** or **Save As** if you would like to change the name of your *.ust* file.

NOTE Ensure that you have added all the standard instruments you would like to test. The DGN and CEDGN testplans will only test instruments in the *.ust* file.

Configuring and Running the DGN Testplan

1 Start the Agilent TestExec SL (version 7.1 or greater) by clicking this icon on your desktop:

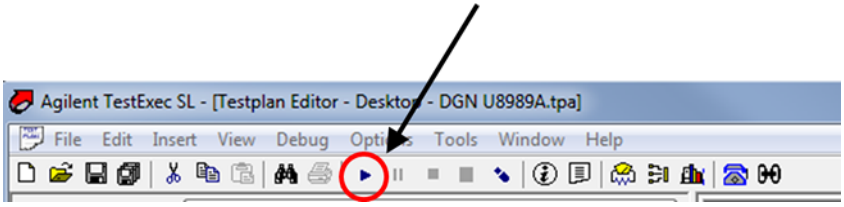
2 Load the *DGN U8989A.tpa* testplan into the TestExec SL. The testplans are located in this directory:

```
C:\Program Files\Agilent\TS-5000 System
Software\testplan\dgn
```

or

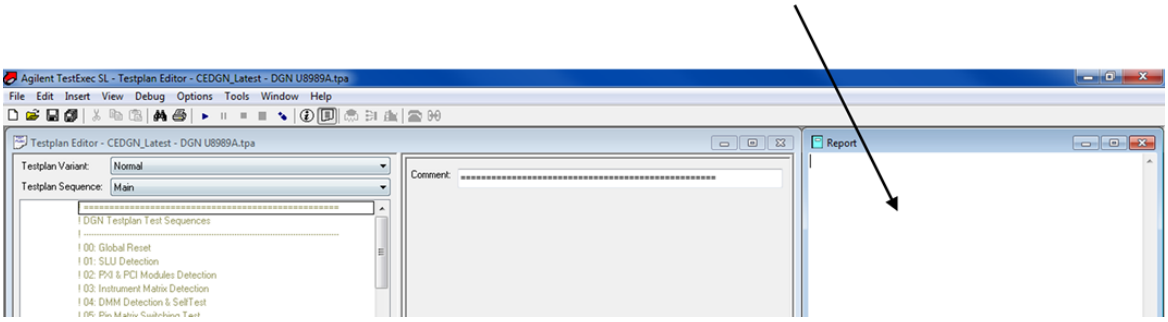
```
C:\Program Files (x86)\Agilent\TS-5000
System Software\testplan\dgn
```

3 Press the play button (shown by the arrow in the figure below) to run the testplan.



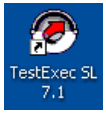
4 During certain sequences, message boxes will pop up with instructions on putting on fixtures or taking them out. Follow these instructions carefully to avoid any test errors.

5 The test report will be printed in the report window (shown by the arrow in the figure below).



Configuring and Running the CEDGN Testplan

1 Start the Agilent TestExec SL (version 7.1 or greater) by clicking this icon on your desktop:



2 Load the *CEDGN U8989A.tpa* testplan into the TestExec SL. The testplans are located in this directory:

```
C:\Program Files (x86)\Agilent\TS-5000
System Software\Service\U8989A\Testplans
```

or

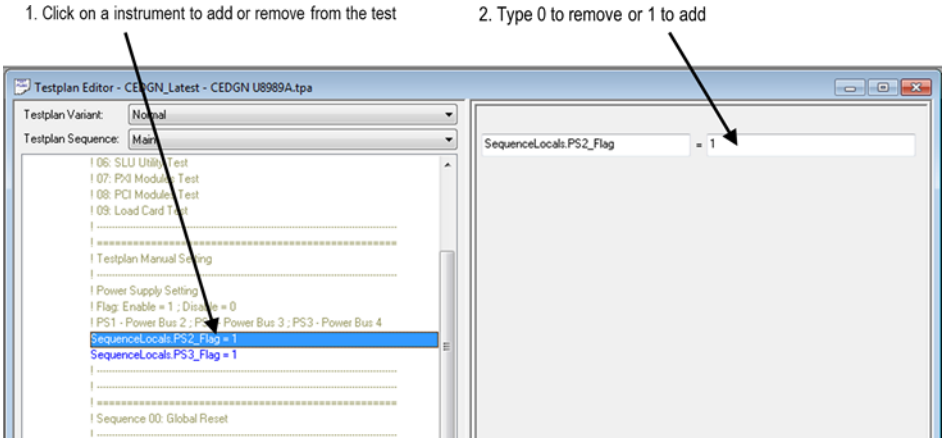
```
C:\Program Files (x86)\Agilent\TS-5000
System Software\Service\U8989A\Testplans
```

3 The CEDGN testplan will perform the test according to the settings set in the system topology file.

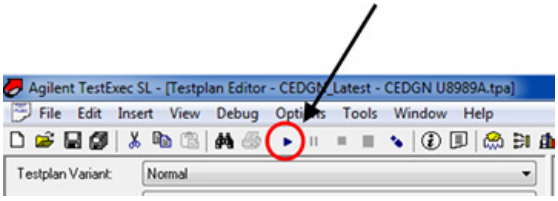
However, the DUT power supply needs to be configured in the CEDGN testplan as shown in Figure 3-1.

Place a *1* next to instruments you want to test and a *0* next to the instruments you do not want to test (or instruments that are not in your system).

Figure 3-1 Configure DUT power supply in the CEDGN testplan



4 Press the play button (shown by the arrow in the figure below) to run the testplan.



The testplan will run tests on each instrument configured in the system topology file and also the instruments specified in step 3. The results of the tests are displayed.

5 Follow the instructions appearing on the display throughout the test.

Installing the Diagnostic Test Fixtures

Specific diagnostic test fixtures are required to be connected to the Test System Interface based on the messages prompted while running the CEDGN testplan. The DGN testplan only requires external fixture connections for the Pin Matrix Card tests, whereas the CEDGN testplan would most likely require more types of fixtures. The number of fixtures required would depend on the instruments installed in the system.

Figure 3-2 shows the U8989-61625 CEDGN Test Fixture connected to the Pin Matrix's slot (1-4 and 6-9). This fixture connection is used to test the connectivity and Pin Matrix functionality. This fixture is the only one required for DGN tests.

Figure 3-2 Installing the U8989-61625 CEDGN Test Fixture

Figure 3-3 shows a U8989-61620 CEDGN Test Fixture connected to the SLU Utility slot with a U8989-61625 CEDGN Pin Matrix Cable connected to Slot 21.

This fixture connection is used to test the SLU Utility functionality.

Figure 3-3 Installing the SLU Utility U8989-61620 CEDGN Test Fixture with a U8989-61625 CEDGN Pin Matrix Cable

Figure 3-4 shows a U8989-61621 CEDGN Test Fixture connected to the Load Card Slot with a U8989-61625 CEDGN Pin Matrix Cable connected to Slot 21.

This fixture connection is used to test the SLU Load Card (24-/16-/8-Channel) functionality.

Figure 3-4 Installing the Load Card U8989-61 1 CEDGN Test Fixture with a U8989-61625CEDGN Pin Matrix Cable

Figure 3-5 shows a U8989-61621 CEDGN Test Fixture connected to the SLU Utility Slot with a U8989-61625 CEDGN Pin Matrix Cable connected to Slot 21.

This fixture connection is used to test the Load Card ISense functionality.

Figure 3-5 Installing the Load Card ISense U8989-61621 CEDGN Test Fixtures with a U8989-61625 CEDGN Pin Matrix Cable

Figure 3-6 shows a U8989-61624 CEDGN Test Fixture connected to the Heavy Duty Load Card with a U8989-61625 CEDGN Pin Matrix Cable connected to Slot 21.

This fixture connection is used to test the Heavy Duty Load Card functionality.

Figure 3-6 Installing the Heavy Duty Load Card U8989-61624 CEDGN Test Fixture with a U8989-61625 CEDGN Pin Matrix Cable

Figure 3-7 shows a U8989-61622 CEDGN Test Fixture connected to the 48-Channel Load Card with a U8989-61625 CEDGN Pin Matrix Cable connected to Slot 21.

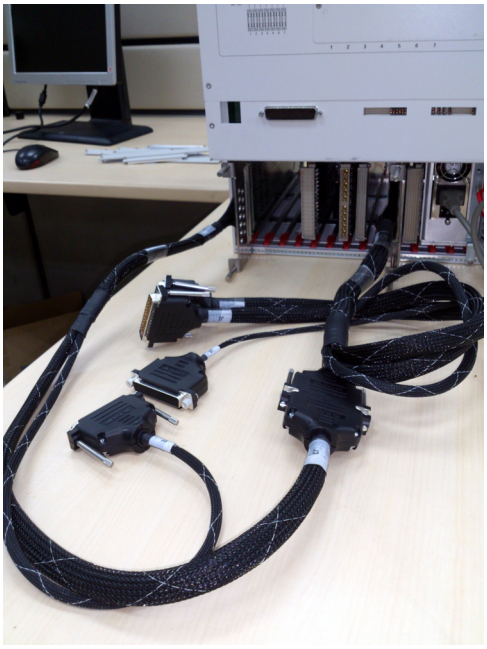
This fixture connection is used to test the 48-Channel Load Card functionality.

Figure 3-7 Installing the 48-Channel Load Card U8989-61622 CEDGN Test Fixture with a U8989-61625 CEDGN in Matrix Cable

Figure 3-8 shows a U8989-61623 CEDGN Test Fixture connected to the Instrument Routing Card with a U8989-61625 CEDGN Pin Matrix Cable connected to Slot 21.

This fixture connection is used to test the PXI/PCI Modules functionality.

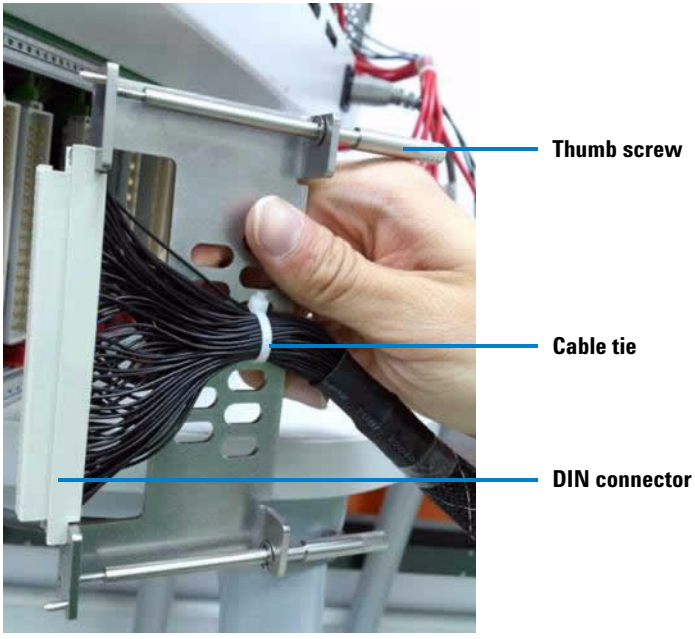
Figure 3-8 Installing the Instrument Routing Card U8989-61623 CEDGN Test Fixture with a U8989-61625 CEDGN Pin Matrix Cable



Installing the CEDGN fixture kit bracket

The CEDGN fixture kit bracket is used to secure the DIN connector onto the SLU. It utilizes a thumb screw mechanism to mount the DIN connector onto the SLU. The holes on the mounting plate helps secure the the cables on the the fixture kit bracket with the help of cable ties (see Figure 3-9).

Figure 3-9 Overview of the CEDGN Fixture Kit Bracket

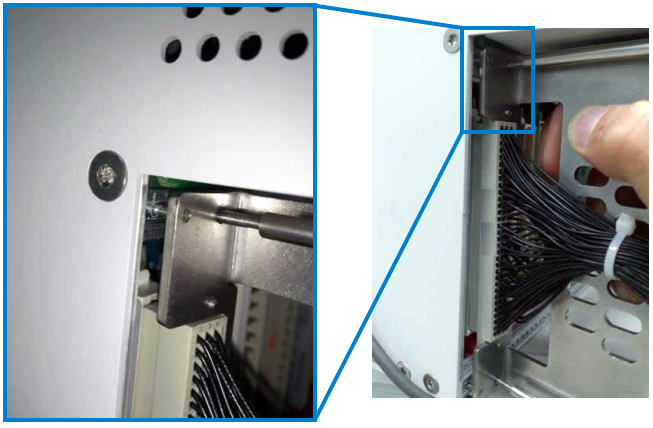


1 Before connecting the fixture kit bracket, ensure that the C-Clip is in contact with the back of the mounting plate, as shown in Figure 3-10.

Figure 3-10 CEDGN Fixture Kit Bracket Installation Step 1

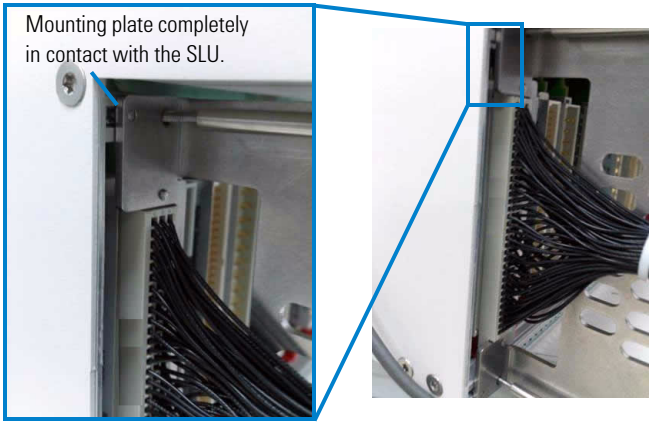
2 When connecting the fixture kit bracket to the SLU, ensure that the guiding pin is on the screw hole of the SLU.

Figure 3-11 CEDGN Fixture Kit Bracket Installation Step 2



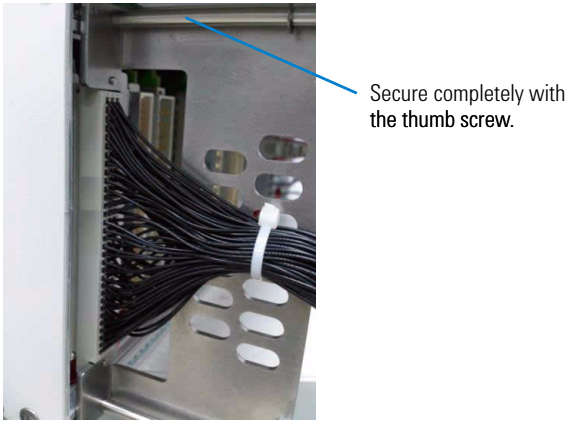
3 Connect the fixture kit bracket completely and ensure that there is no big gap between the SLU and the mounting plate, as shown in Figure 3-12.

Figure 3-12 CEDGN Fixture Kit Bracket Installation Step 3



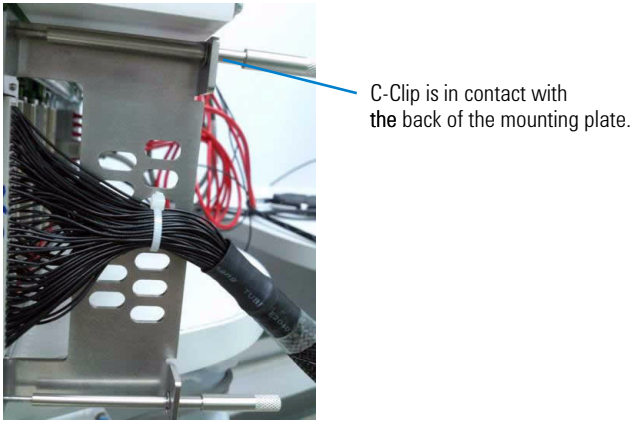
4 Secure the fixture kit bracket onto the SLU by tightening the thumb screw.

Figure 3-13 CEDGN Fixture Kit Bracket Installation Step 4



5 When removing the fixture kit bracket from the SLU, make sure to unscrew the bracket using the thumb screw *completely* until the the C-Clip is in contact with the back of the mounting plate, as shown in Figure 3-14.

Figure 3-14 CEDGN Fixture Kit Bracket Installation Step 5



6 Pull the fixture kit bracket away from the SLU by pulling the mounting plate, not the fixture cable.

Figure 3-15 CEDGN Fixture Kit Bracket Installation Step 6

Resolving Test Failures

Test failures can be caused by improper switch settings on the Diagnostic Test Fixture, improperly specifying the system equipment, or by an actual test system instrument failure.

Before troubleshooting the system equipment, verify that the test fixture switches are properly set and that the test system instrumentation was properly specified. If the problem seems to be the system equipment, swap the instrument and/or the cable between the instrument and the Test System Interface.

Chapter 4 contains detailed descriptions of each test that may help in isolating equipment problems to a particular component.

4
Diagnostic Testing Details

DGN Testplan Description and Flow

The DGN testplan comprises basic tests to verify the system internal connections and the basic functions of the instruments.

Sequence 00: Global Reset

This section include IPC information queries, instrument initializations, and reset. This section also clears the parameter in the symbol tables.

Sequence 01: SLU Detection

This section first checks the presence of the SLU in the system topology file. The SLU must be detected to continue the test. Otherwise, the testplan will stop. This section will list down all the cards present in the SLU from slot 11 to slot 21.

Sequence 02: PXI and PCI Modules Detection

This section first checks the presence of the PXI and PCI modules in the system topology file and lists down the present modules. This section will also display the modules serial number.

Sequence 03: Instrument Matrix Detection

This section detects the presence of the Instrument Matrix in the system topology file. The Instrument Matrix must be present in the SLU on slot 21 to continue the test. Otherwise, the testplan will stop.

Sequence 04: DMM Detection and Test

This section detects the presence of a DMM in the system topology file. At least one DMM must be present in the system to continue the test. Otherwise, the testplan will stop.

Upon successful detection, the testplan will set the detected DMM(s) to run the self-test sequentially.

Sequence 05: Pin Matrix Switching Test

This section will detect and test all the pin matrix cards present in the system topology file, and it comprises four tests: Instrument Matrix DMM Mux Test, Instrument Matrix DAC Relay Test, Pin Matrix Non-Fixture Test, and Pin Matrix Fixture Test.

- "Instrument Matrix DMM Mux Test" on page 39
- "Instrument Matrix DAC Relay Test" on page 42
- "Pin Matrix Non-Fixture Test" on page 43
- "Pin Matrix Fixture Test" on page 46

Instrument Matrix DMM Mux Test

Instrument Matrix Inst1 and Inst2 Pin Test	Connect/Disconnect *matrix1:Inst1*|*matrix1:ABus1* and *matrix1:Inst2*|*matrix1:ABus1*, and measure the path resistance. See Figure 4-1 on page 40. Repeat test for ABus2, ABus3, ABus4, and UUTCommon.
ABUS Short Test	Connect and measure the path resistance between *matrix1:Inst1*|*ABus1* and *matrix1:Inst2*|*ABus2*. See Figure 4-2 on page 41. There should not be any connection between the two ABUS. Repeat the test for ABus3 and ABus 4.

Instrument Matrix Inst3 and Inst4 Pin Test

Connect/Disconnect *matrix1:Inst1|matrix1:ABus1*, *matrix1:Inst2|matrix1:ABus2*, *matrix1:Inst3|matrix1:ABus1* and *matrix1:Inst3|matrix1:ABus2*, and measure the path resistance. See Figure 4-3 on page 41. Repeat the test for ABus3, ABus4, and UUTCommon for both Inst3 and Inst4 Pin.

Figure 4-1 Instrument Matrix Inst1 and Inst2 Pin Test

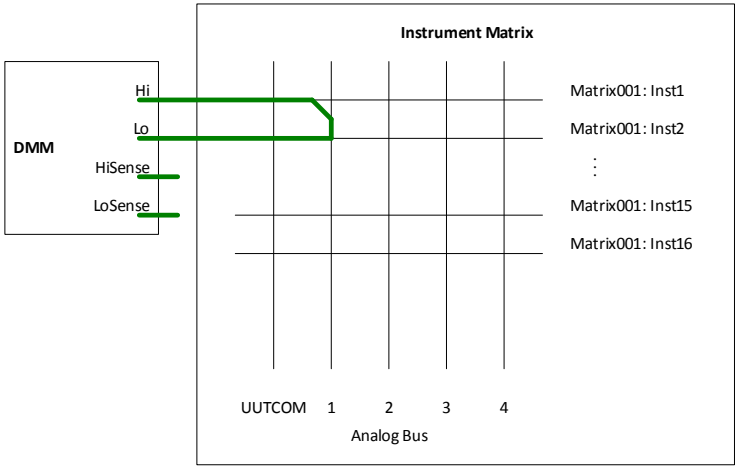


Figure 4-2 ABUS Short Test

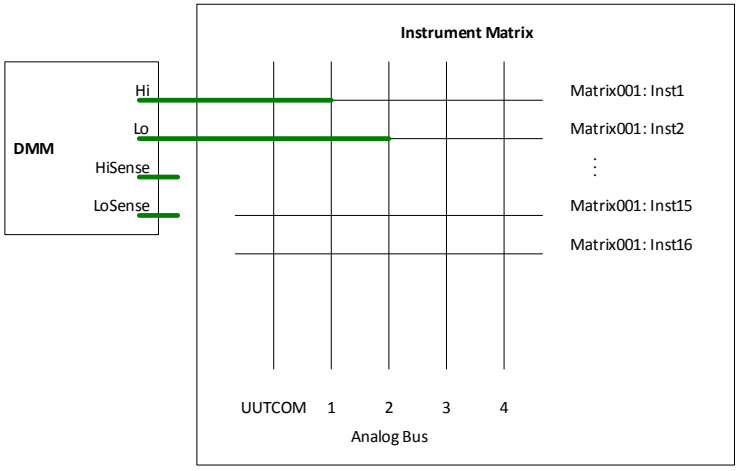
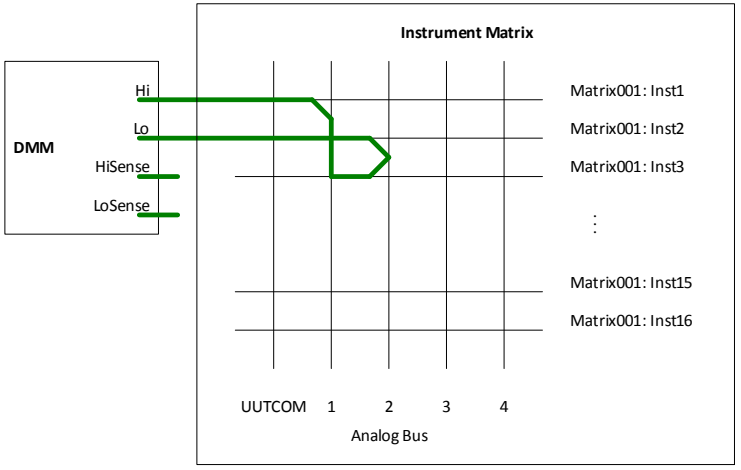


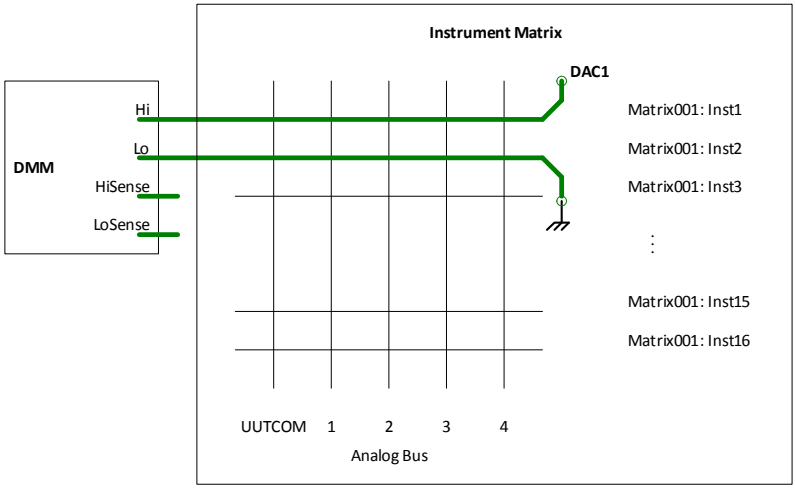
Figure 4-3 Instrument Matrix Inst3 and Inst4 Pin Test



Instrument Matrix DAC Relay Test

Connect/Disconnect the DAC1 relay; output the DAC to 16 V and measure the voltage level. See Figure 4-4. Repeat for the DAC2 relay.

Figure 4-4 Instrument Matrix DAC Relay Test



Pin Matrix Non-Fixture Test

Instrument Rows Open/Short Test	Connect/Disconnect *DMM_Hi*|*ABus1*|*Matrix001:Inst5* and *DMM_Lo*|*ABus2*|*Matrix001:Inst5*, and measure the path resistance. See Figure 4-5 on page 43. Repeat the test for instrument rows 6 to 40. This test starts from instrument row 5 because instrument rows 1 to 4 are allocated for DMM Hi, Lo, ISrc Hi, and ISrc Lo.
Measurement Rows Open/Short Test	Connect/Disconnect *DMM_Hi*|*ABus1*|*Matrix001:RowX* and *DMM_Lo*|*ABus2*|*Matrix001:RowX*, and measure the path resistance. See Figure 4-6 on page 44. Repeat the test for the remaining Row Relays.
Bypass Relays Test	Open/Close the Pin Matrix Bypass relays, and measure the path resistance. See Figure 4-7 on page 45. The protection resistor values are 200 Ohms.

Figure 4-5 Instrument Rows Open/Short Test

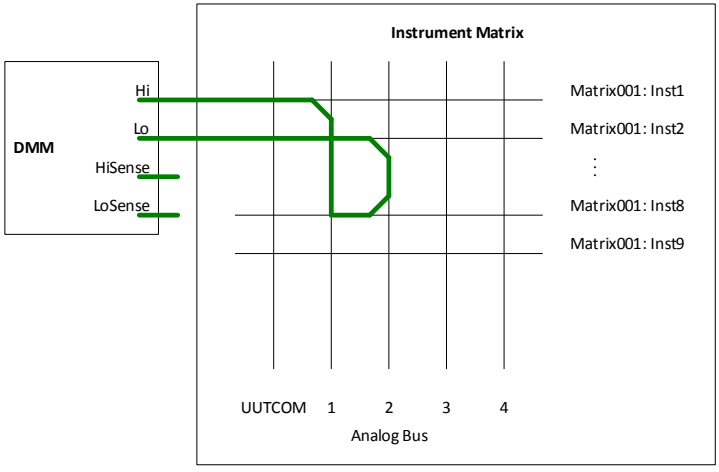


Figure 4-6 Measurement Rows Open/Short Test

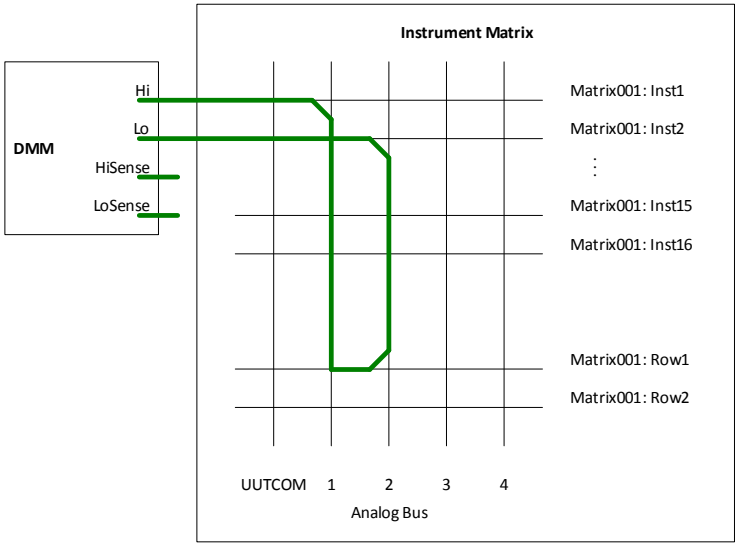
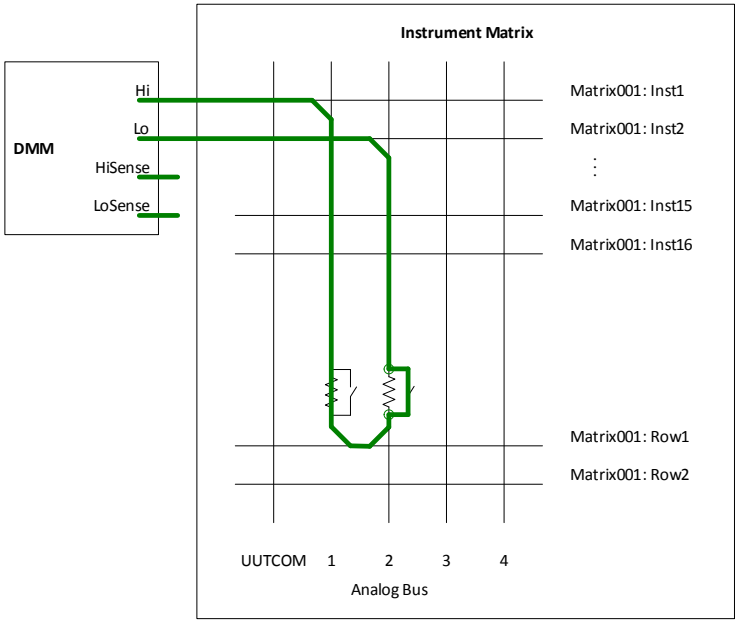


Figure 4-7 Bypass Relays Test



Pin Matrix Fixture Test

This section requires the external fixture and loopback cable to test the relays open/short between pin matrix ROW and AUX. Figure 4-8 and Figure 4-9 illustrates the internal and external connections for this test.

There are two types of loopback cable, U8989-61625 for the E879xA pin matrix and U8989-61619 for the E878xA pin matrix.

Using the loopback cable, pin matrix Row1 will be shorted to Row2, Row3 to Row 4, and so on. The DMM should measure SHORT when the internal switching is done. See Figure 4-8.

For the AUX test, the loopback cable connects AUX1 via the UUTCOM, similarly for AUX2, AUX3 and so on. The DMM should measure SHORT when the internal switching is done. See Figure 4-9.

Figure 4-8 Pin Matrix Fixture Test (Row Pin)

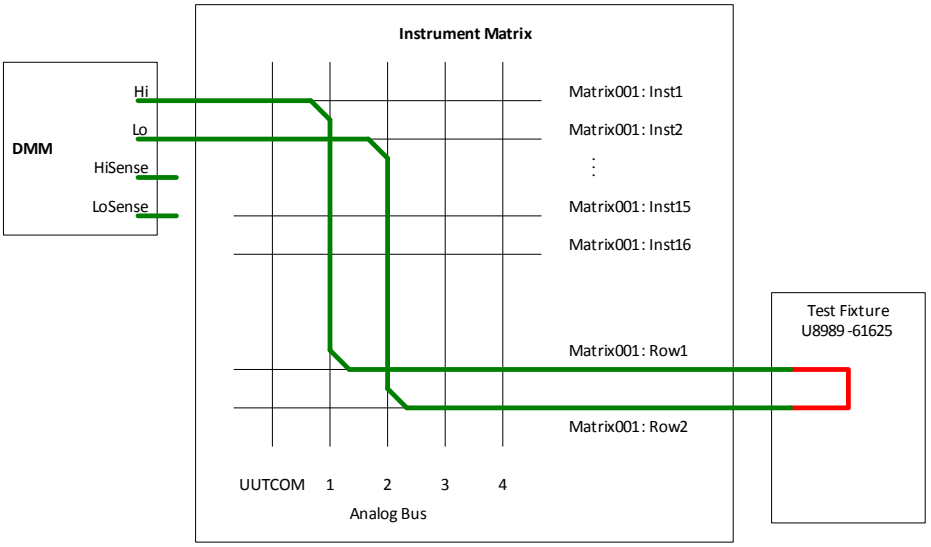
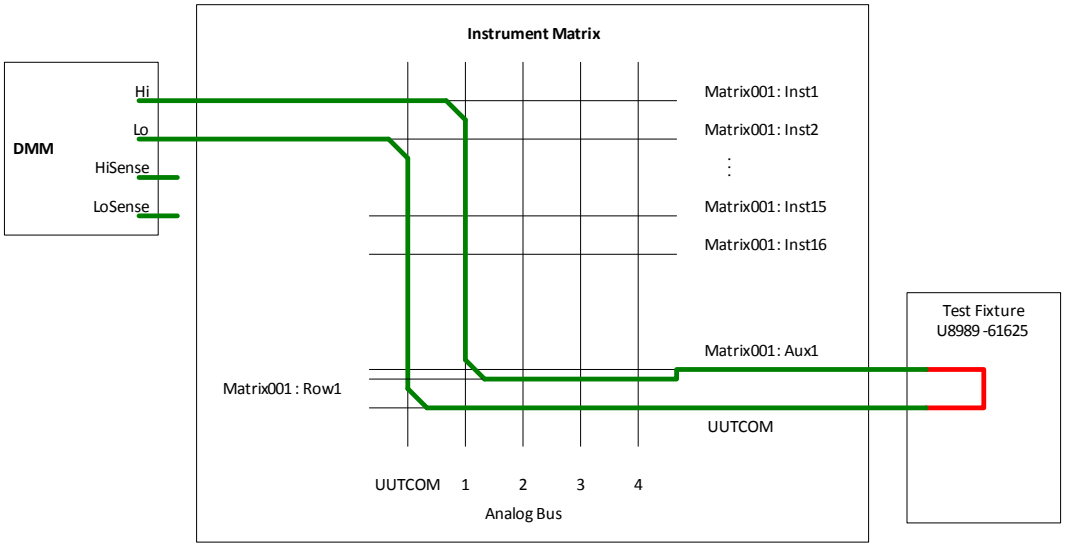


Figure 4-9 Pin Matrix Fixture Test (Aux Pin)



CEDGN Testplan Description and Flow

Sequence 00: Global Reset

This sequence includes IPC information queries, instrument initializations, and reset. This sequence also clears the parameter in the symbol tables.

Sequence 01: SLU Detection

This sequence first checks the presence of the SLU in the system topology file. The SLU must be detected to continue the test. Otherwise, the testplan will stop. This sequence will list down all the cards present in the SLU from slot 11 to slot 21.

Sequence 02: PXI & PCI Modules Detection

This sequence first checks the presence of the PXI and PCI modules in the system topology file and list down the present modules.

Sequence 03: Instrument Matrix Detection

This sequence detects the presence of the Instrument Matrix in the system topology file. The Instrument Matrix must be present in the SLU on slot 21 to continue the test. Otherwise, the testplan will stop.

Sequence 04: DMM Detection & Test

This sequence detects the presence of a DMM in the system topology file. At least one DMM must be present in the system to continue the test. Otherwise, the testplan will stop.

Upon successful detection, the testplan will set the detected DMMs to run the self-test sequentially.

Sequence 05: Pin Matrix Switching Test

This sequence will detect and test all the pin matrix cards present in the system topology file. It requires the external fixture and loopback cable to test the relays open/short between pin matrix ROW and AUX. Figure 4-8 and Figure 4-9 illustrates the internal and external connections for this test.

There are two types of loopback cable, U8989-61625 for E879xA pin matrix and U8989-61619 for E878xA pin matrix.

Using the loopback cable, pin matrix Row1 will be shorted to Row2, Row3 to Row 4, and so on. The DMM should measure SHORT when the internal switching is done. See Figure 4-8.

For the AUX test, the loopback cable connects AUX1 via the UUTCOM, similarly for AUX2, AUX3 and so on. The DMM should measure SHORT when the internal switching is done. See Figure 4-9.

Sequence 06: SLU Utility Test

This sequence verifies the connectivity of the SLU Fixture ID, Digital IO, Power Bus Sense, ISense, System Ground Pin, Inst DAC, and VDC Supply (+12 V and –12 V).

Sequence 07: PXI Modules Test

This test sequence will detect all the PXI modules present in the system topology. A test will be performed on the detected PXI modules.

- "DAC M9185A Test" on page 50
- "VI M9168A Test" on page 52
- "DIO M9187A Test" on page 54
- "DAQ M9216A Test" on page 57
- "AD1750 Test" on page 58
- "Softing CAN Test" on page 59

DAC M9185A Test

This test verifies the physical connection between the M9185A DAC and the instrument routing card.

Figure 4-10 illustrates the internal switching connection to test DAC Channel 1. Each DAC channel is set to output voltage +16 V) and a DMM will measure the respective channel under test. Note that the DAC sense lines are not connected at this stage. The same test is repeated with the DAC sense lines connected, see Figure 4-11.

Finally, the DAC trigger function is checked with the SLU DAC1 as the trigger source. The DAC output should only be present upon trigger from the SLU DAC1. See Figure 4-12.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61623 cable.

Figure 4-10 DAC Output Port Test

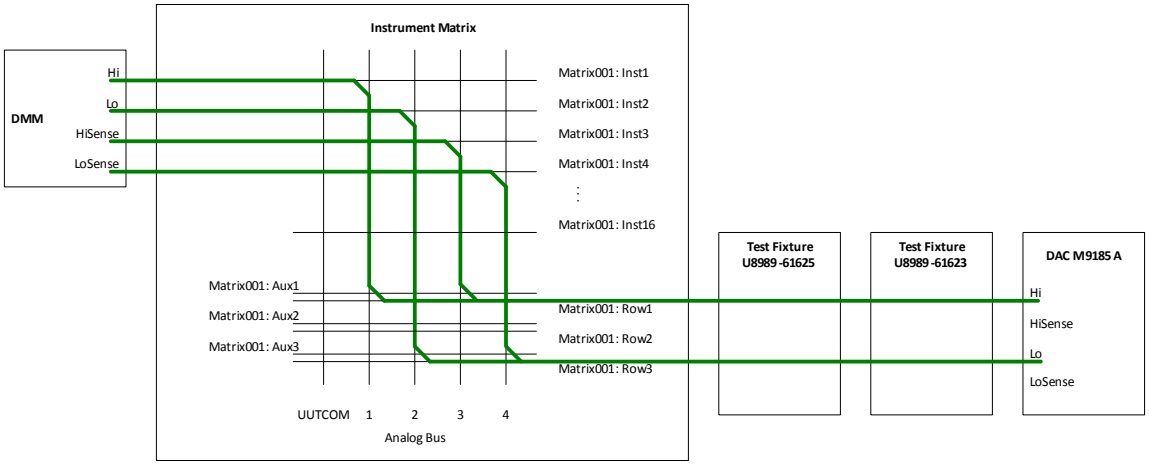


Figure 4-11 DAC Output Sense Port Test

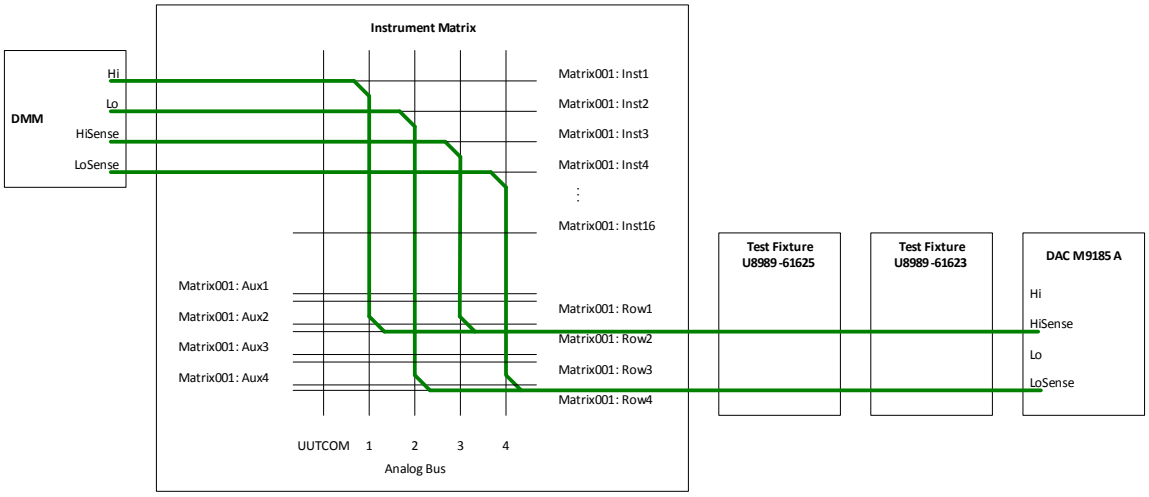
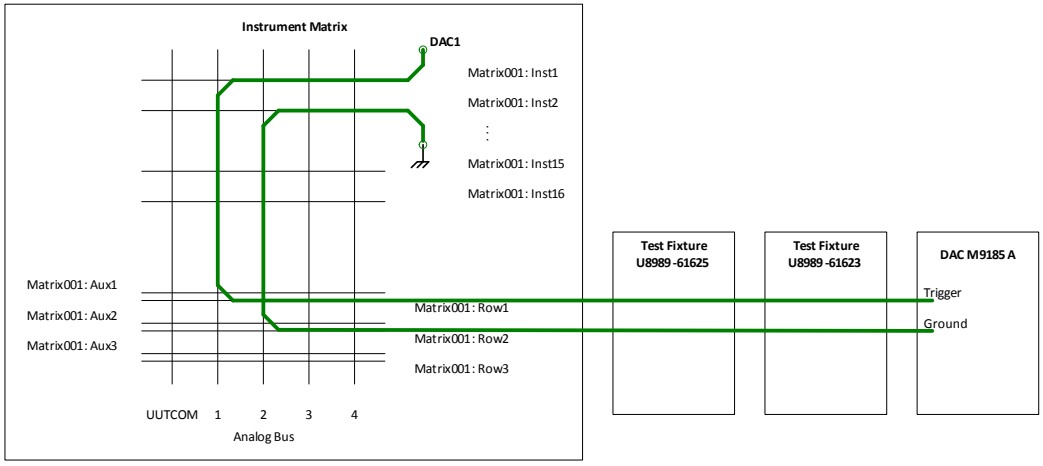


Figure 4-12 DAC Trigger Port Test



VI M9168A Test

This test verifies the physical connection between the M9186A V/I Source and the instrument matrix.

Table 4-1 shows the output value of the V/I source-under-test in voltage or current mode, low or high range. Figure 4-13 illustrates the internal switching connection for the DMM to measure the voltage and current output from the V/I source-under-test. Figure 4-14 shows the connection of the V/I Interlock through pin matrix.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61623 cable.

Table 4-1 V/I source output value

V/I source under test	Output 1	Output 2
Low Voltage:		
0 Ω path	–16 V	16 V
10 Ω path	–16 V	16 V
100 Ω Path	–16 V	16 V
1 kΩ Path	–16 V	16 V
10 kΩ Path	–16 V	16 V
High Voltage:		
0 Ω Path	–10 V	100 V
100 Ω Path	–10 V	100 V
Low Current	–0.02 A	0.02 A
High Current	–0.2 A	0.2 A

Figure 4-13 DMM Internal Switching Connection Test

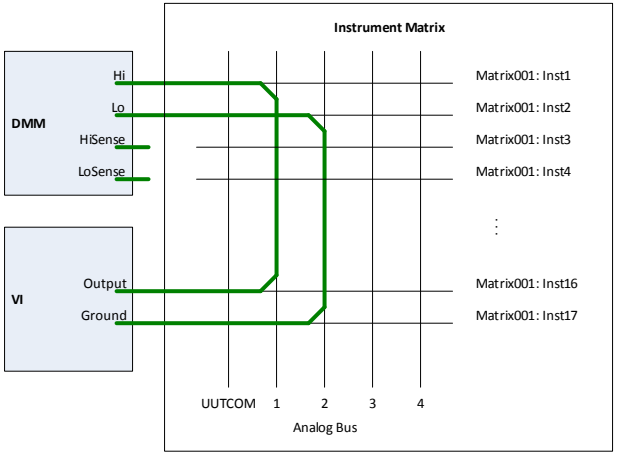
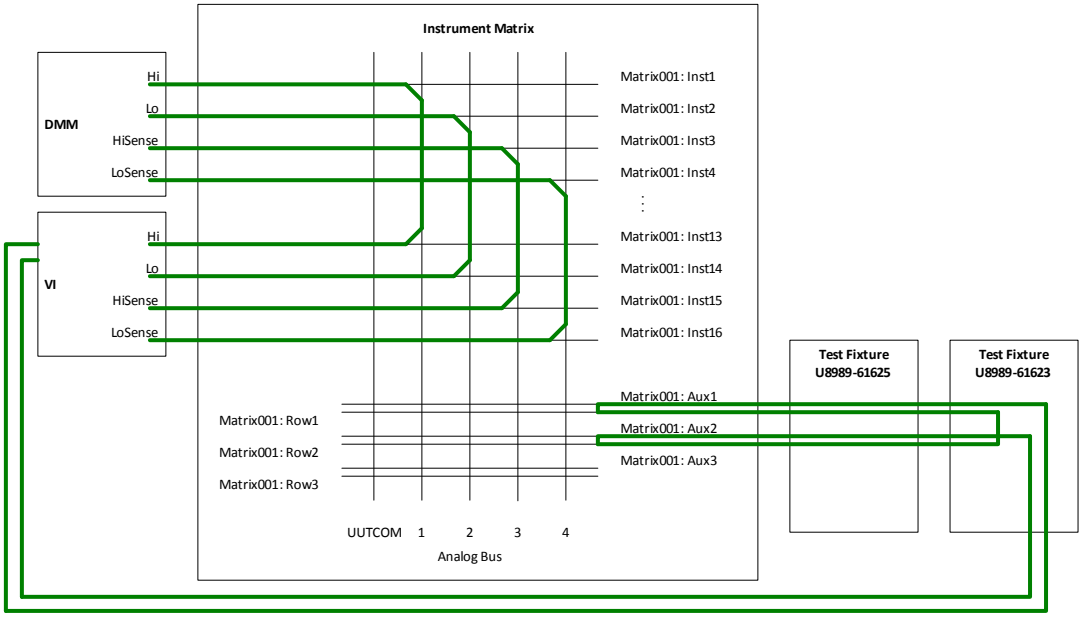


Figure 4-14 VI Voltage and Current Test - VI Interlock Connection



DIO M9187A Test

This test verifies the physical connection between the M9187A DIO and the instrument routing card.

This test requires voltage input from the SLU DAC to the DIO Vext to power up the Digital Output Signal.

Figure 4-15 illustrates the internal switching connection of pin matrix AUX to short the Digital Input and Digital Output of the M9187A. The test will conduct by writing data to the specified output ports and reading back the data from the specified input ports.

Figure 4-16 illustrates the internal switching connection to test the Gnd Pin of the M9187A. The DMM will measure each Gnd Pin through the pin matrix and fixtures to ensure that the Gnd Pin connections are connected.

Figure 4-17 illustrates the internal switching connection to test the Vext Pin of the M9187A. The DMM will measure each Vext Pin through the pin matrix and fixtures to ensure that the Vext Pin connections are connected.

This test requires pin a matrix fixture (U8989-61625 or U8989-61619) and a U8989-61623 cable.

Figure 4-15 DIO DI DO Test

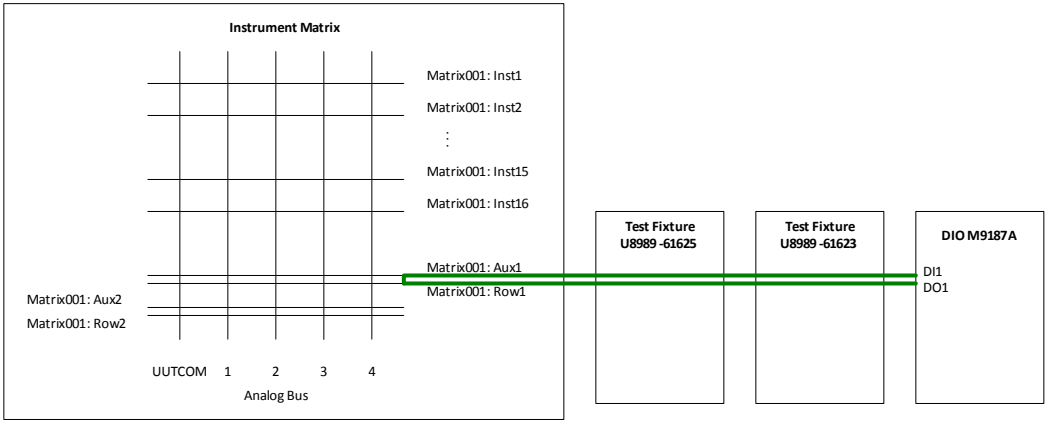


Figure 4-16 DIO GND Test

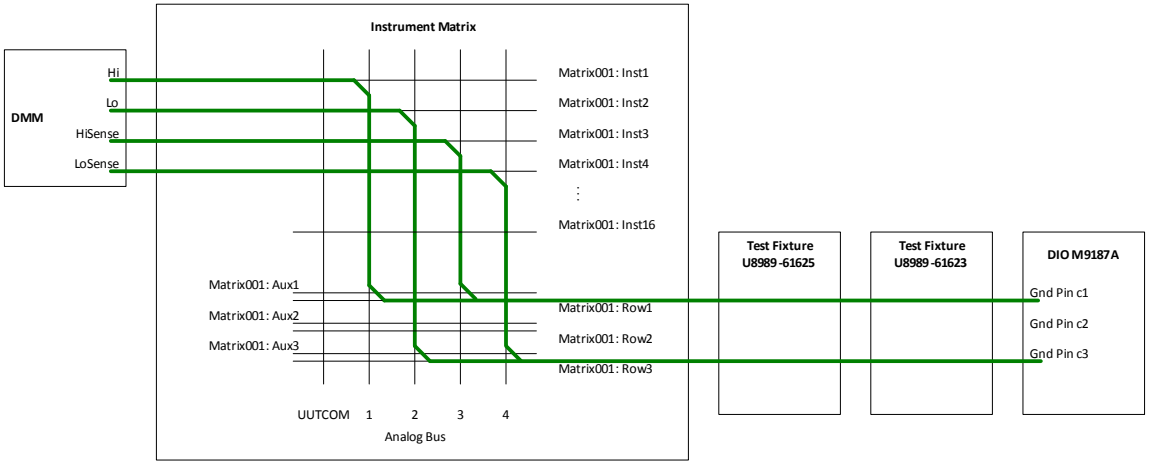
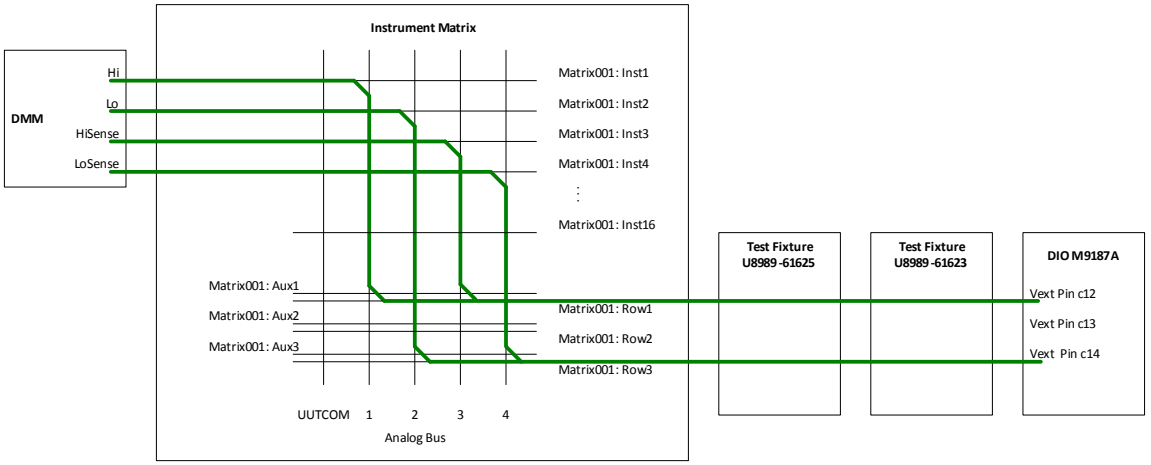


Figure 4-17 DIO Vex Test



DAQ M9216A Test

This test verifies the physical connection between the M9216A HV-DAQ and the system ICA.

SLU DAC1 is set to output voltage and the HV-DAQ will measure the voltage. Figure 4-18 illustrates the internal and external switching connections to test the basic functions of the HV-DAQ.

The CEDGN test kit provides the loopback between the HV-DAQ and its respective AUX, see Figure 4-19.

Both tests require a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61623 cable.

Figure 4-18 DAQ Input Port Test

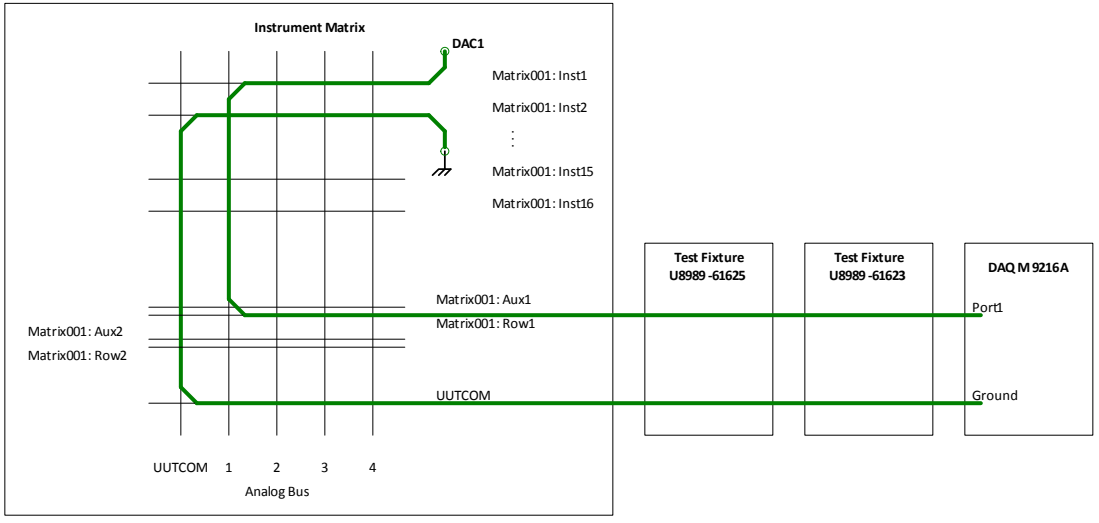
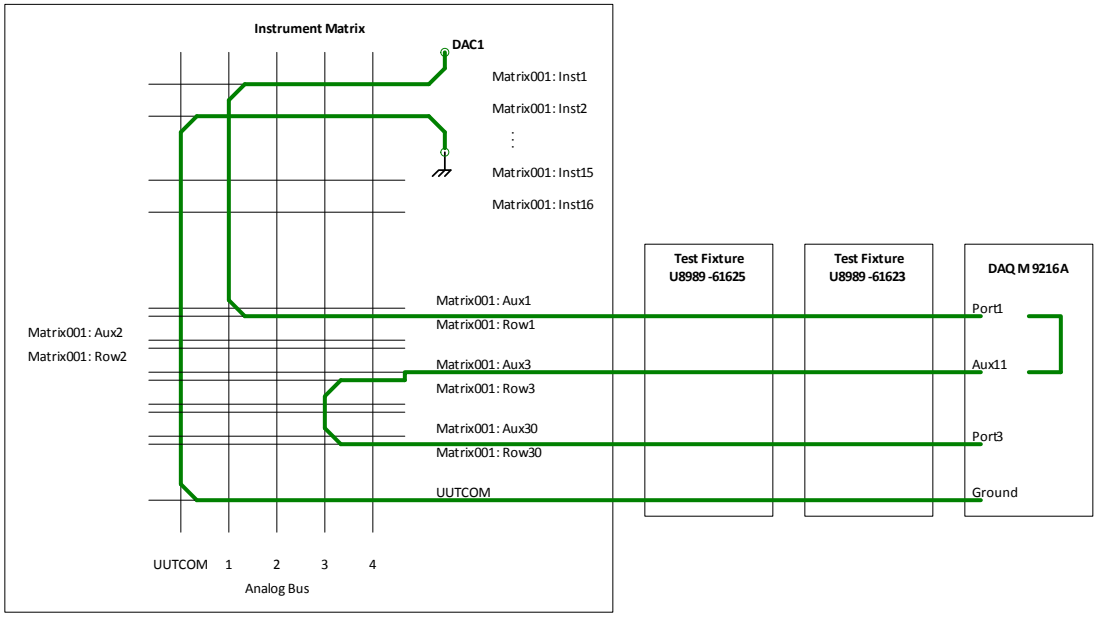


Figure 4-19 DAQ Aux Port Test



Sequence 08: PCI Modules Test

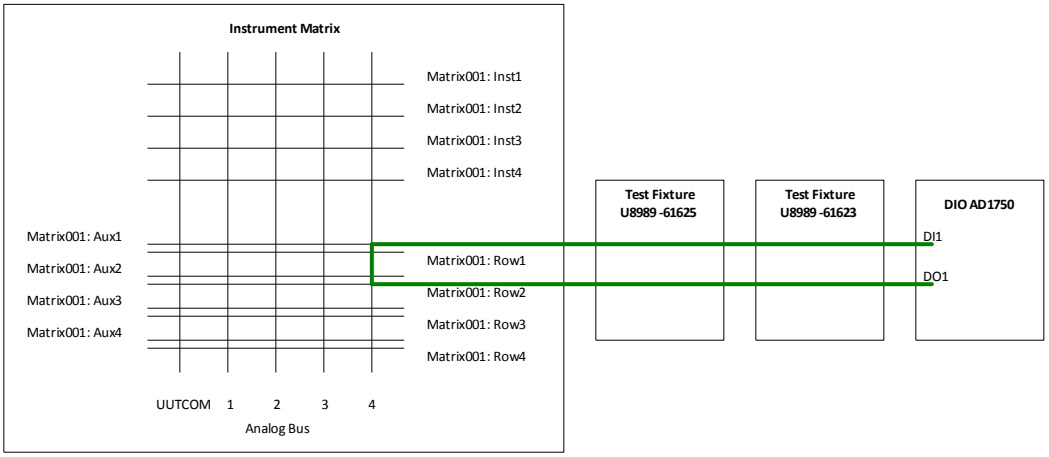
AD1750 Test

This test verifies the physical connection between the PCI 1750 DIO card and the instrument routing card by writing digital data to the specified output ports, and reading back the data from the specified input ports.

Figure 4-20 illustrates the internal switching connection of pin matrix AUX and Row to short the Digital Input and Digital Output of the AD1750.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61623 cable.

Figure 4-20 AD1750 Test



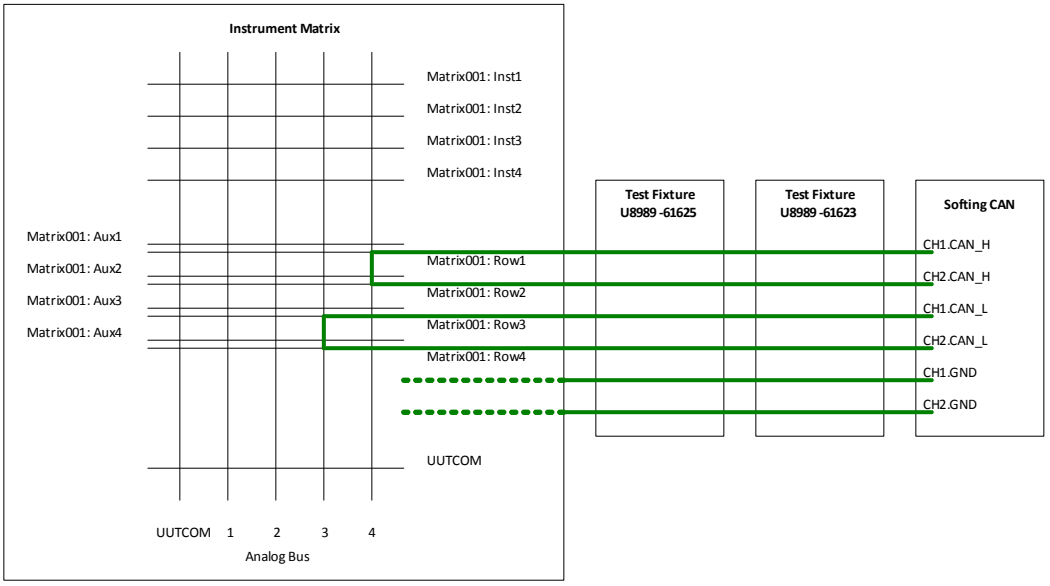
Softing CAN Test

This test verifies the physical connections between the Softing CAN card and the instrument routing card through a loopback test. Specific data bytes are sent and read back from the serial port under test.

Figure 4-21 illustrates the internal switching connection of pin matrix AUX to short Channel 1 and Channel 2 of Softing CAN.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61623 cable.

Figure 4-21 Softing CAN Test



Sequence 09: Load Card Test

E6175A Load Card Test

This test verifies the physical connections between the E6175A Load Card, power supply, and system ICA.

This test consists of an unpowered load card test, a powered load card test, and a current sense test.

Load relay switches are tested in the unpowered load card test. In this test, an external mount load with an effective load resistance of 28.86 Ω (E2240-67012) is mounted on the E6175A J1 connector. Use a DMM to measure the resistance path between channel 1 and channel 2, similarly between channel 3 and channel 4, and so on until channel 7 and channel 8. Figure 4-22 illustrates the resistance measurement path for the E6175A unpowered load card test.

The powered load card test requires the a DUT power supply. If no DUT power supply is present, this test will be skipped. The DUT power supply is set to output +5 V (current limit at 0.1 A) and the DMM will measure the voltage via the load card channels, NC, and NO. Figure 4-23 illustrates the measurement path for the E6175A powered load card test.

Figure 4-24 illustrates the internal and external switching connections to test the E6175A current sense. This test measures the resistance of the current sense path via the SLU backplane.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61621 cable.

Figure 4-22 E6175A Unpowered Load Card Test

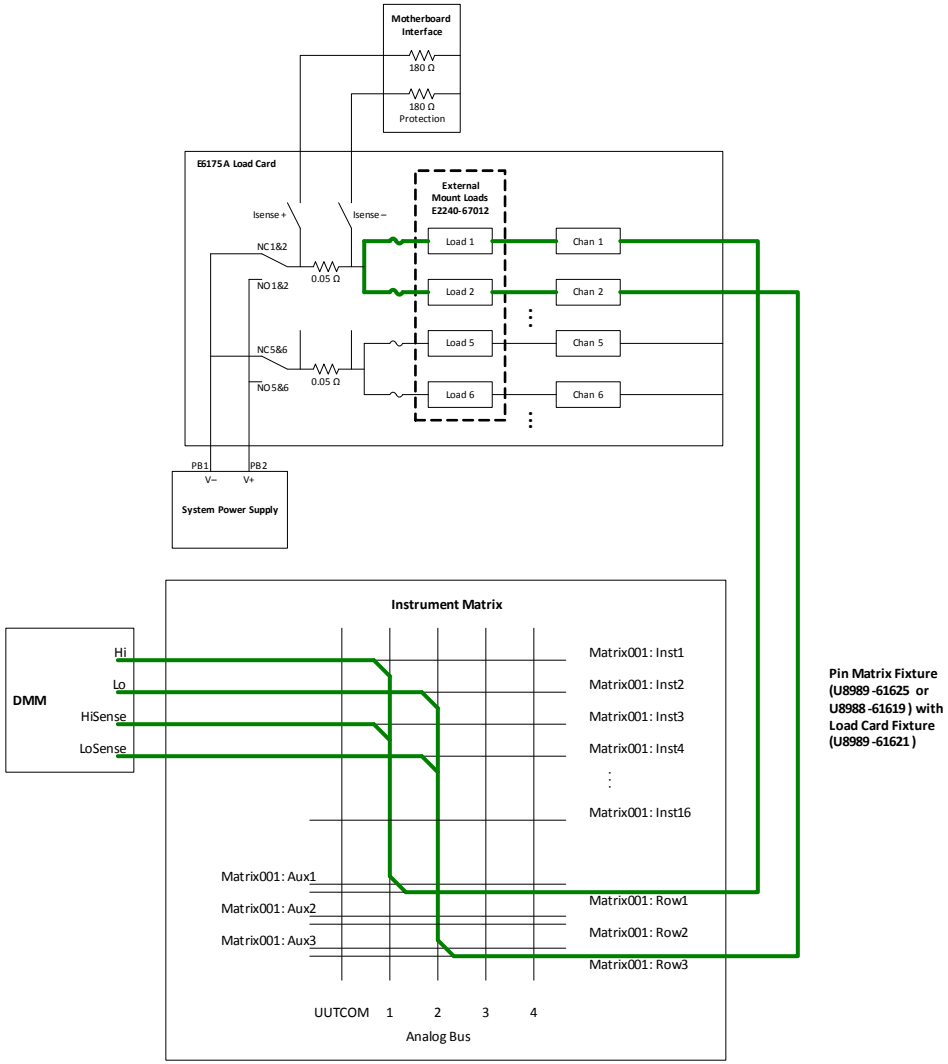


Figure 4-23 E6175A Powered Load Card Test

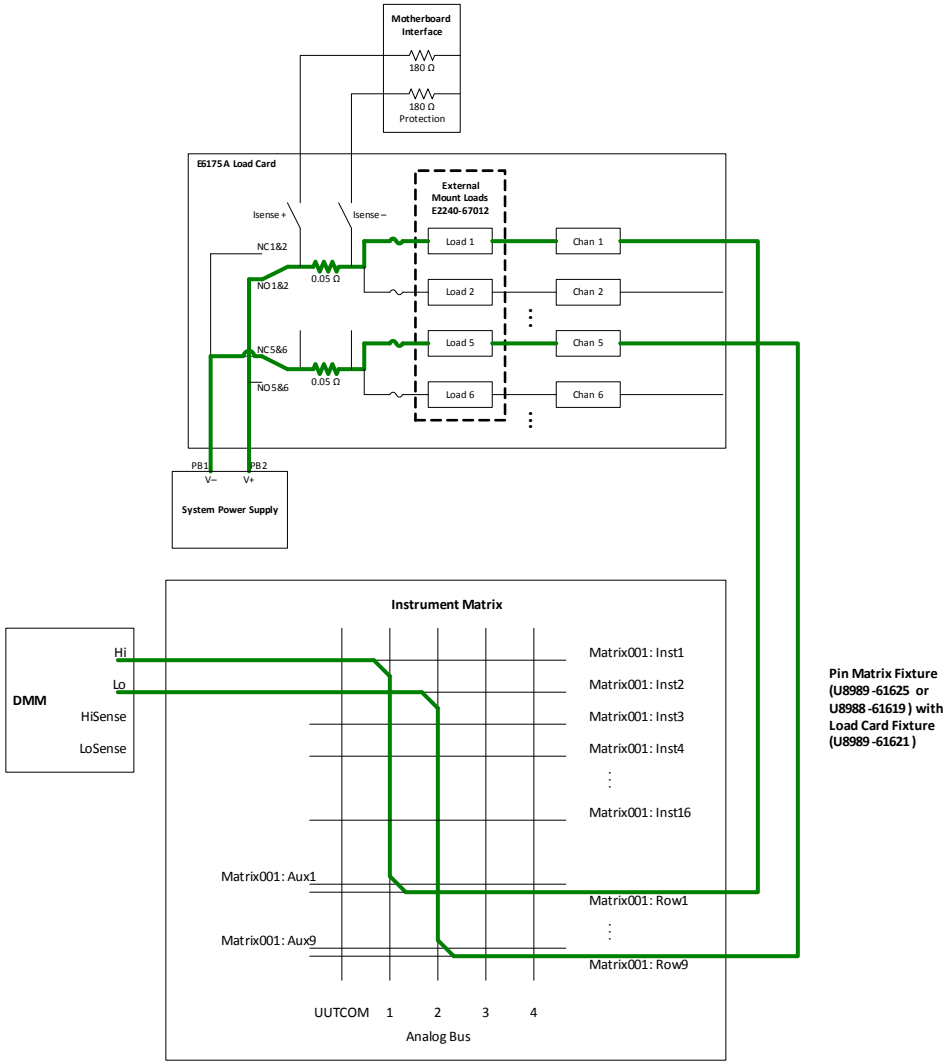
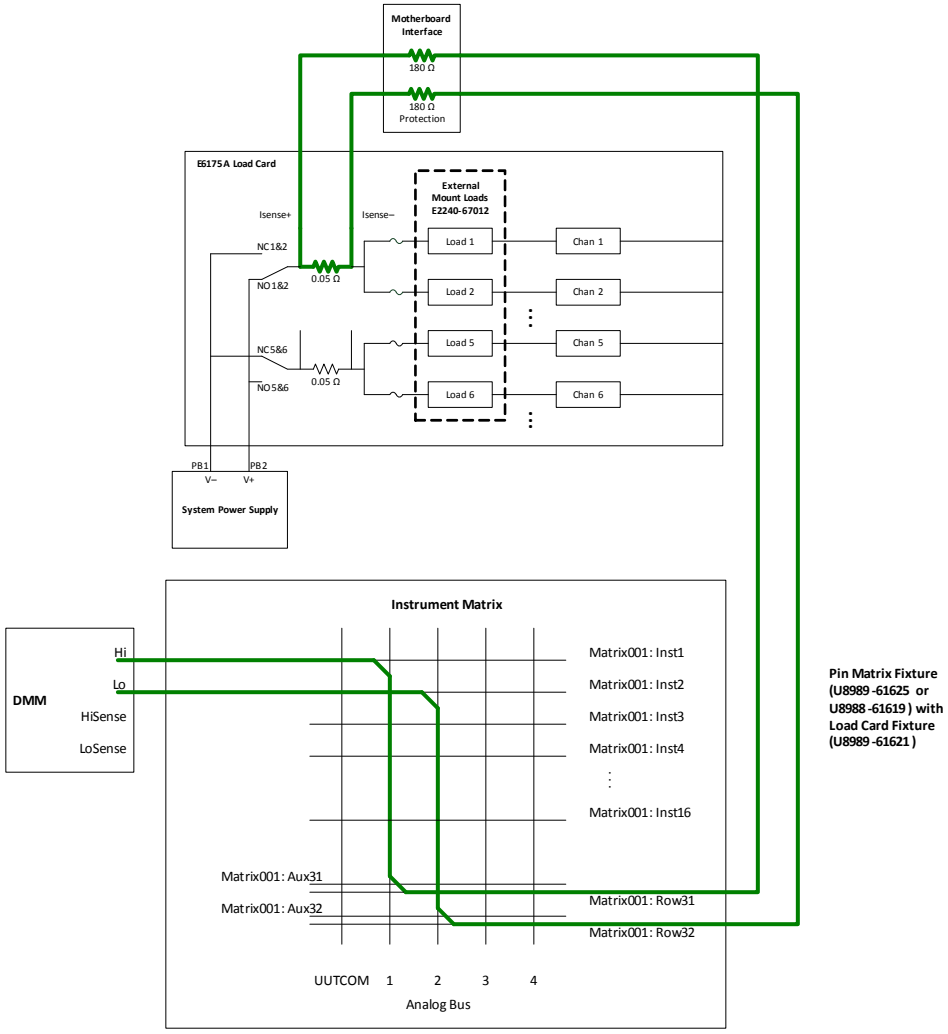


Figure 4-24 E6175A Current Sense Test



E6176A Load Card Test

This test sequence verifies the physical connection between the E6176A Load Card, power supply, and system ICA.

This test consists of an unpowered load card test, a powered load card test, and a current sense test.

Load relay switches are tested in the unpowered load card test. In this test, an external mount load with an effective load resistance of 28.86 Ω (E2240-67012) is mounted on the E6176A J1 and J2 connector. Use a DMM to measure the resistance path between channel 1 and channel 9 via the load card channels, NC and NO, similarly for channel 2 and channel 10, and so on until channel 8 and channel 16. Figure 4-25 illustrates the resistance measurement path for the E6176A unpowered load card test.

The powered load card test requires a DUT power supply. If no DUT power supply is present, this test will be skipped. The DUT power supply is set to output +5 V (current limit at 0.1 A) and the DMM will measure the voltage via the load card channels, NC and NO. Figure 4-26 illustrates the measurement path for the E6176A powered load card test.

Figure 4-27 illustrates the internal and external switching connections to test the E6176A current sense. This test measures the resistance of the current sense path via the SLU backplane.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61621 cable.

Figure 4-25 E6176A Unpowered Load Card Test

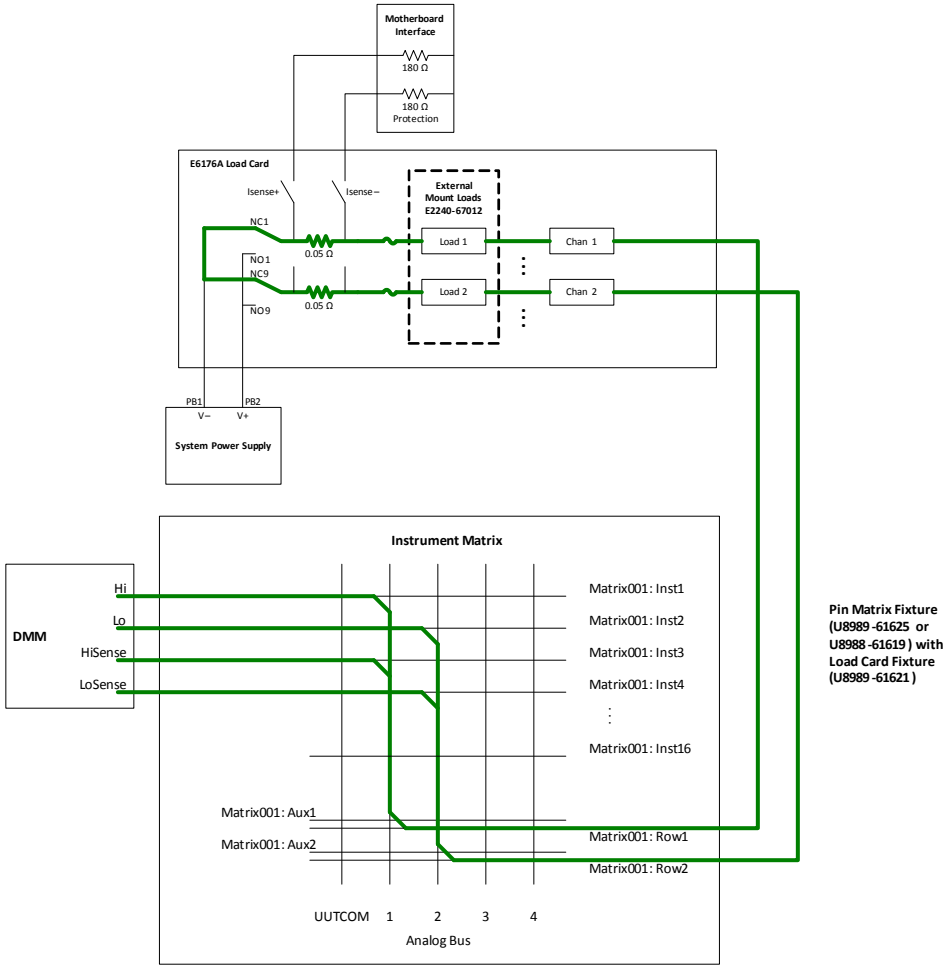


Figure 4-26 E6176A Powered Load Card Test

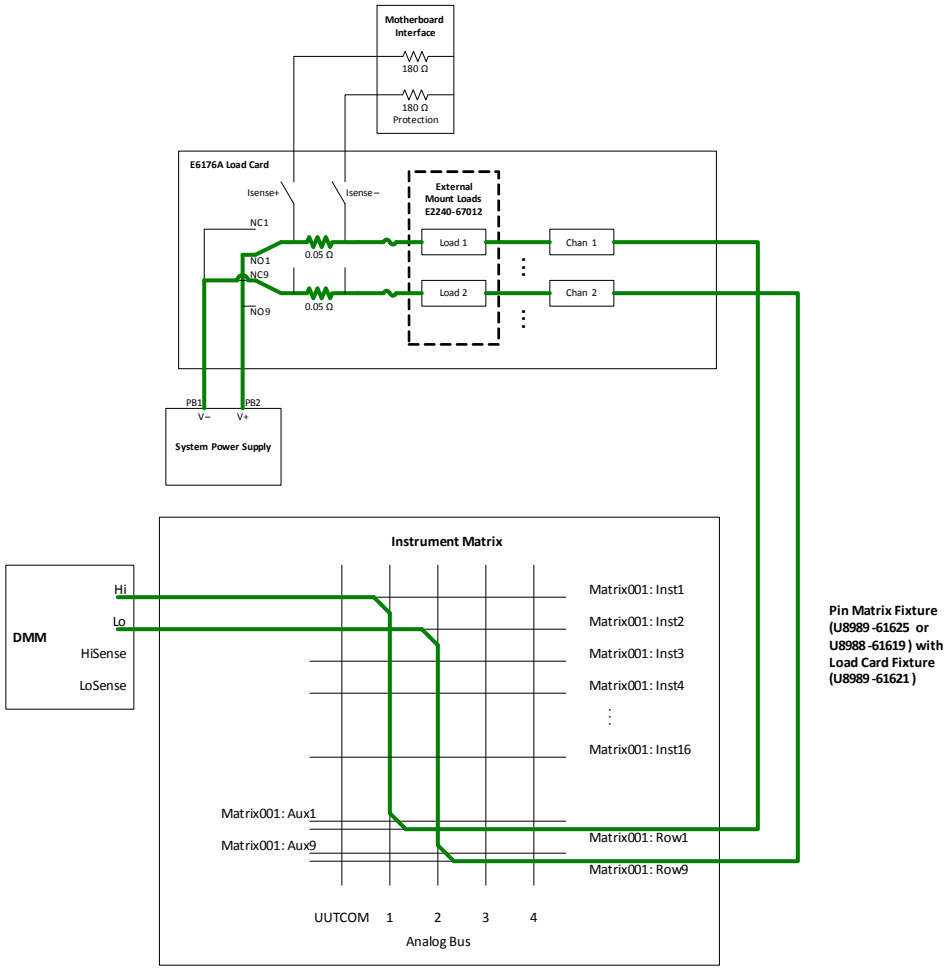
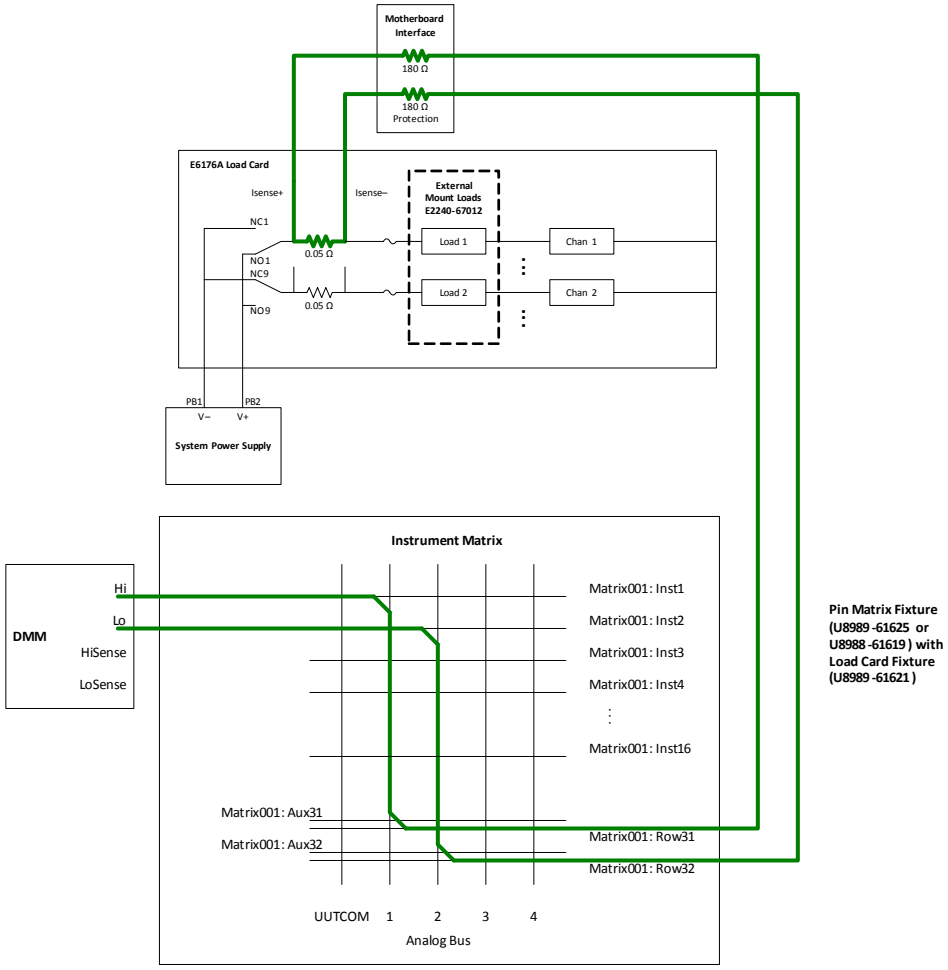


Figure 4-27 E6176A Current Sense Test



E6177A Load Card Test

This test verifies the physical connection between the E6177A Load Card, power supply, and system ICA.

This test consists of an unpowered load card test and a powered load card test.

The load relay switches are tested in the unpowered load card test. In this test, an external mount load with an effective load resistance of 86.6 Ω (E2240-67012) is mounted on the E6177A J1 connector. Use a DMM to measure the resistance path between channel 1 and common 1 (or channel power 1), similarly for between channel 2 and common 2, and so on until between channel 24 and common 24. Figure 4-28 illustrates the resistance measurement path for the E6177A unpowered load card test.

The powered load card test requires a DUT power supply. If no DUT power supply is present, this test will be skipped. The DUT power supply is set to output +5 V (current limit at 0.1 A) and the DMM will measure the voltage via the load card channels, NC and NO. Figure 4-29 illustrates the measurement path for the E6177A powered load card test.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61621 cable.

Figure 4-28 E6177A Unpowered Load Card Test

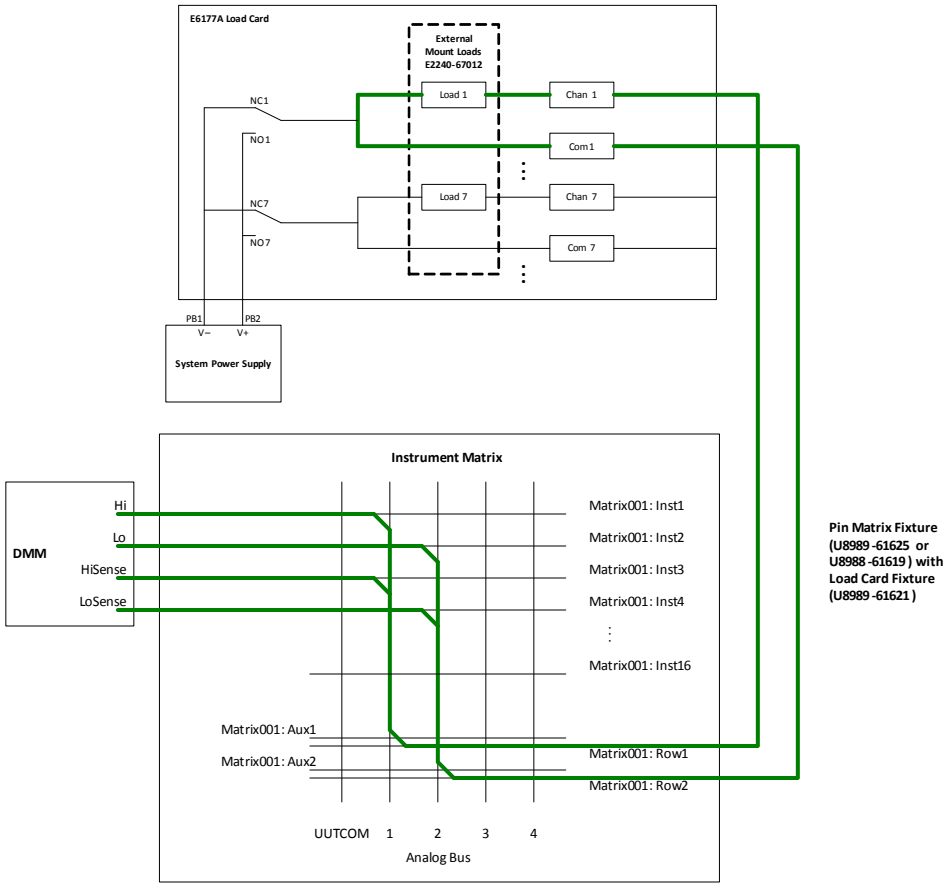
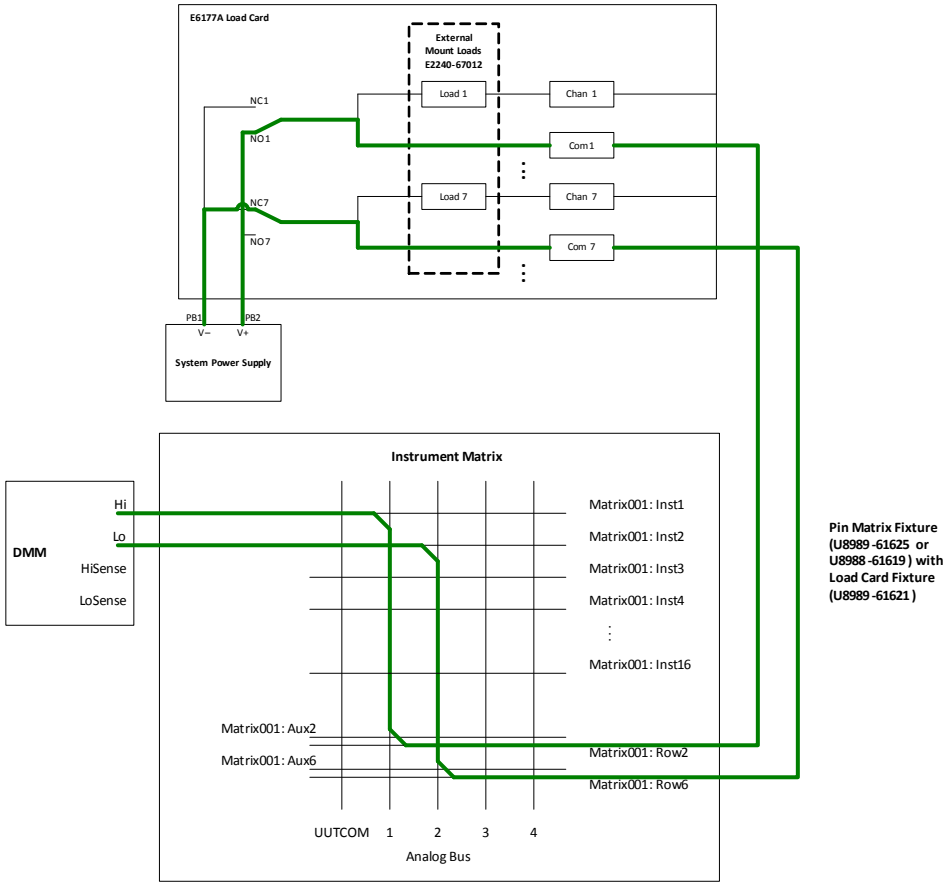


Figure 4-29 E6177A Powered Load Card Test



U7177A Load Card test

This test verifies the physical connection between the U7177A Load Card, power supply, and system ICA.

This test consists of an unpowered load card test, a powered load card test, and a current sense test.

The load relay switches are tested in the unpowered load card test. In this test, an external mount load with an effective load resistance of 86.6 Ω (E2240-67012) is mounted on the U7177A J1 connector. Use a DMM to measure the resistance path between channel 1 and common 1, similarly between channel 2 and common 2, and so on until between channel 24 and common 24. Figure 4-30 illustrates the resistance measurement path for the U7177A unpowered load card test.

The powered load card test requires a DUT power supply. If no DUT power supply is present, this test will be skipped. The DUT power supply is set to output +5 V (current limit at 0.1 A) and the DMM will measure the voltage via the load card channels, NC and NO. Figure 4-31 illustrates the measurement path for the U7177A powered load card test.

Figure 4-32 illustrates the internal and external switching connections to test the U7177A current sense. This test measures the resistance of the current sense path via the SLU backplane.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61621 cable.

Figure 4-30 U7177A Unpowered Load Card Test

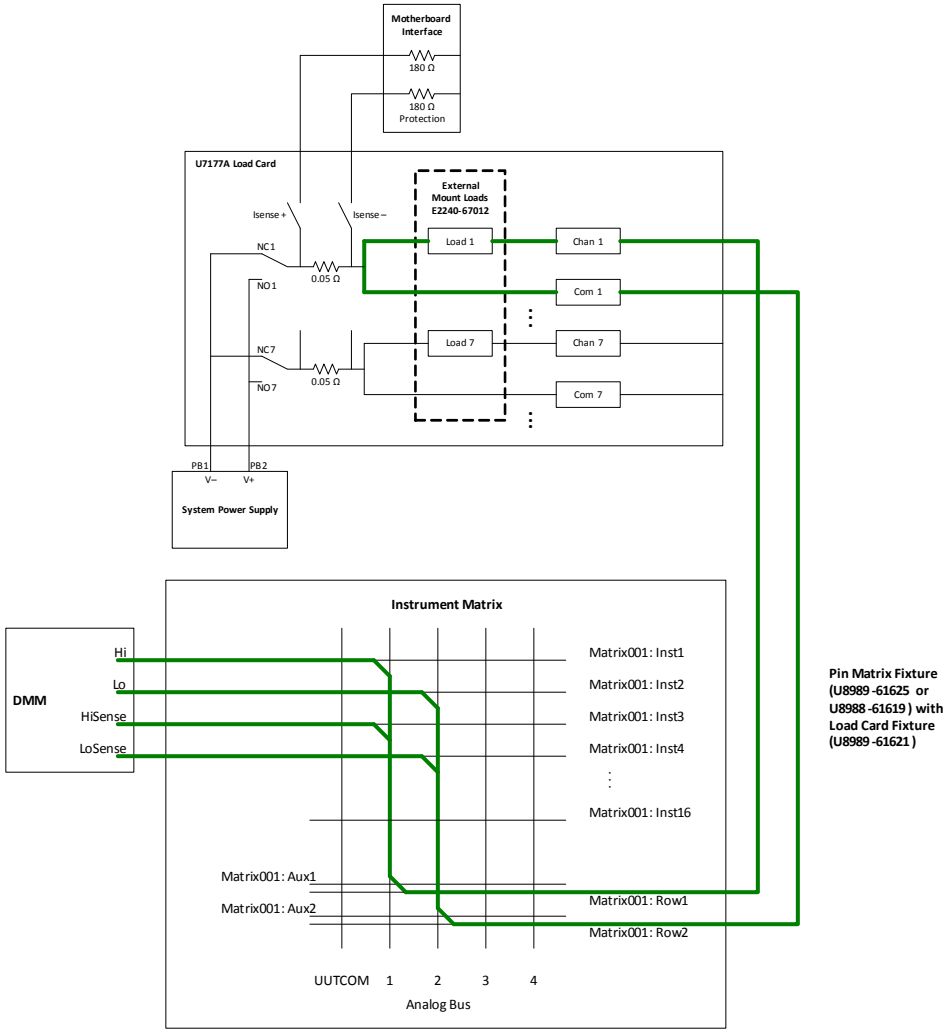


Figure 4-31 U7177A Powered Load Card Test

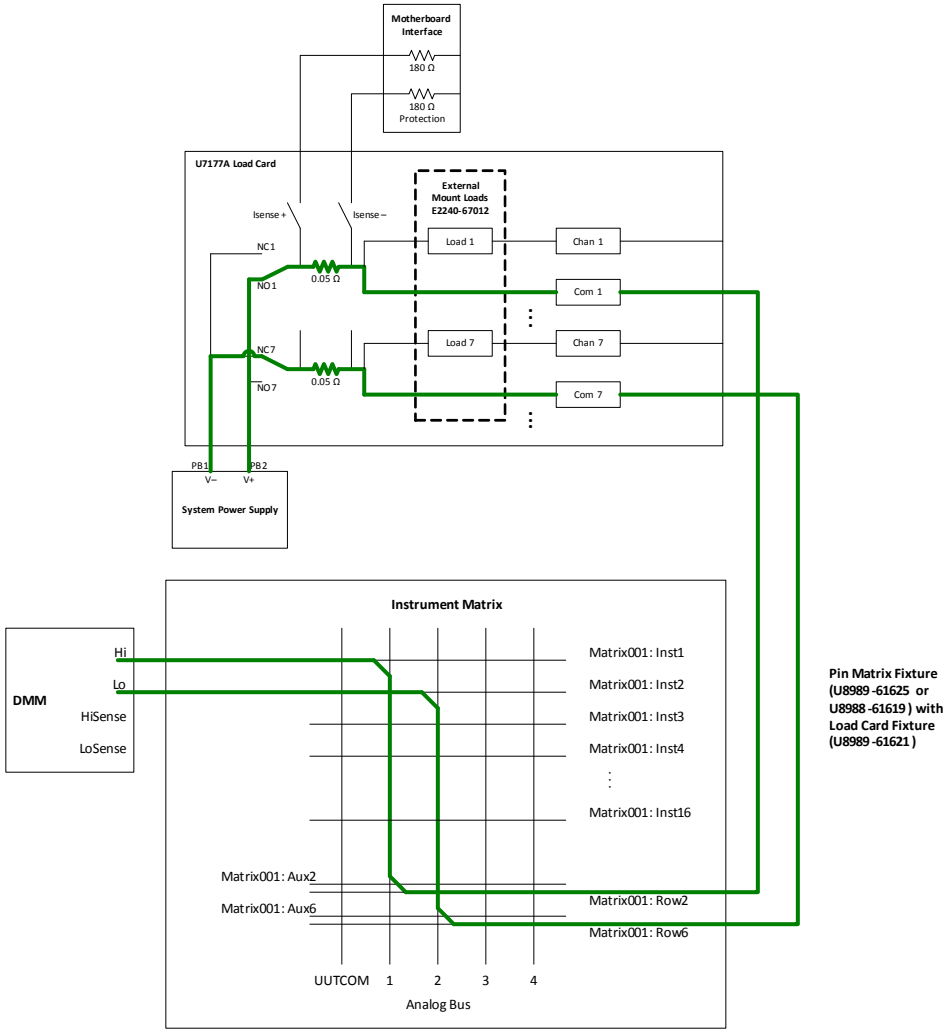
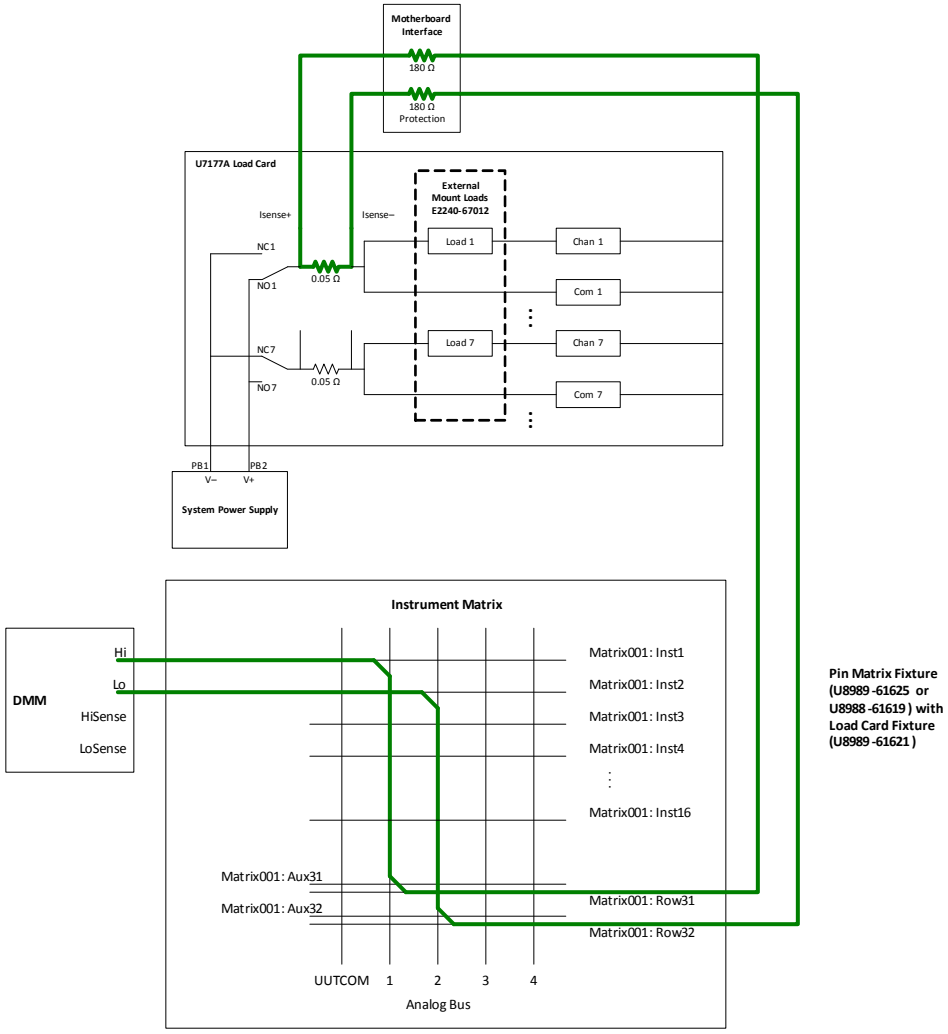


Figure 4-32 U7177A Current Sense Test



N9377A Load Card Test

This test verifies the physical connection between the N9377A Load Card, power supply, and system ICA.

This test consists of an unpowered load card test, a powered load card test, and a current sense test.

The load relay switches are tested in the unpowered load card test. In this test, the external mount load, E2240-67012 is mounted on the N9377A, J1 and J2 connector. The effective load resistance on load X.1 is 28.86 Ω and on load X.2 is short (0 Ω). X represents the channel number from 1 to 16. Use a DMM to measure the resistance path between channel 1 and channel 9 via load1.1 and NC. The expected reading is 60.6588 Ω. Next, measure the short (0 Ω) between channel 1 and channel via load1.2 and NO. This test is repeated until channel 8 and channel 16. Figure 4-33 illustrates the resistance measurement path for the N9377A unpowered load card test.

The powered load card test requires a DUT power supply. If no DUT power supply is present, this test will be skipped. The DUT power supply is set to output +5 V (current limit at 0.1 A) and the DMM will measure the voltage via the load card channels, NC and NO. Figure 4-34 illustrates the measurement path for the N9377A powered load card test.

Figure 4-35 illustrates the internal and external switching connections to test the N9377A current sense. This test measures the resistance of the current sense path via the SLU backplane.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61621 cable.

Figure 4-33 N9377A Unpowered Load Card Test

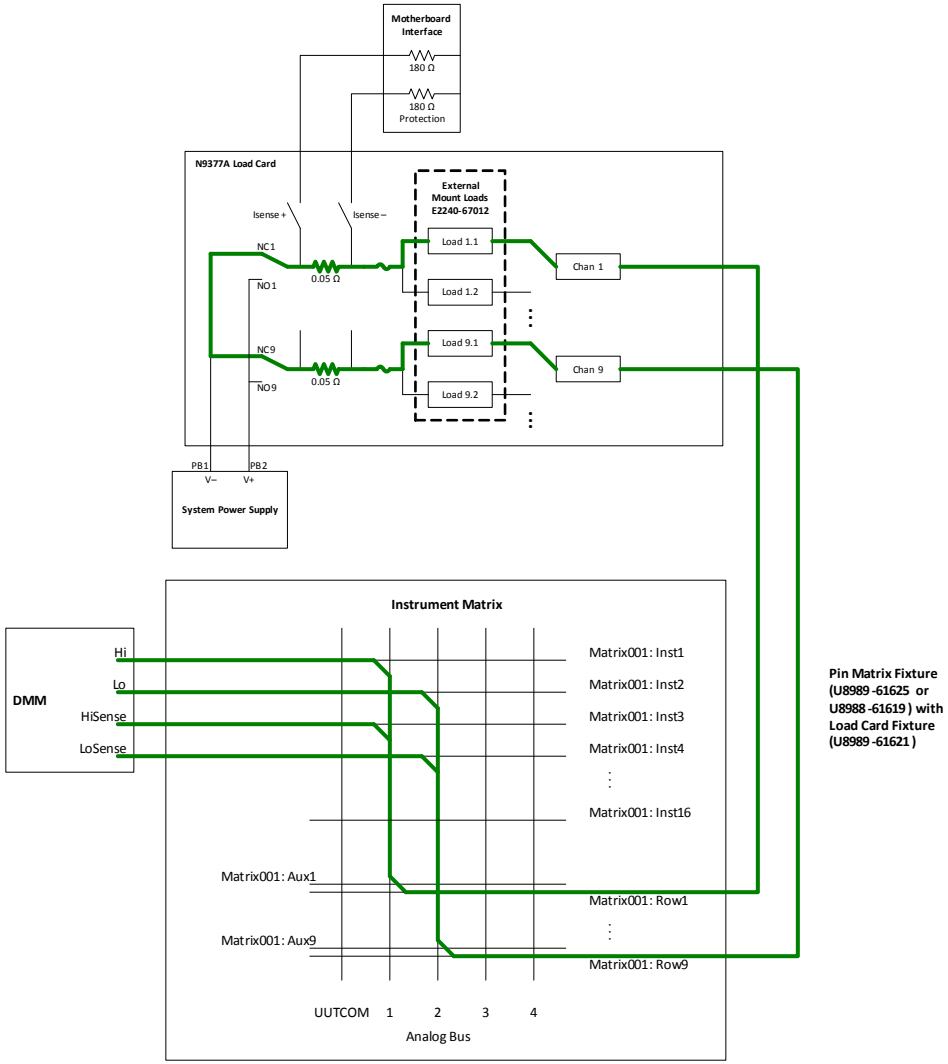


Figure 4-34 N9377A Powered Load Card Test

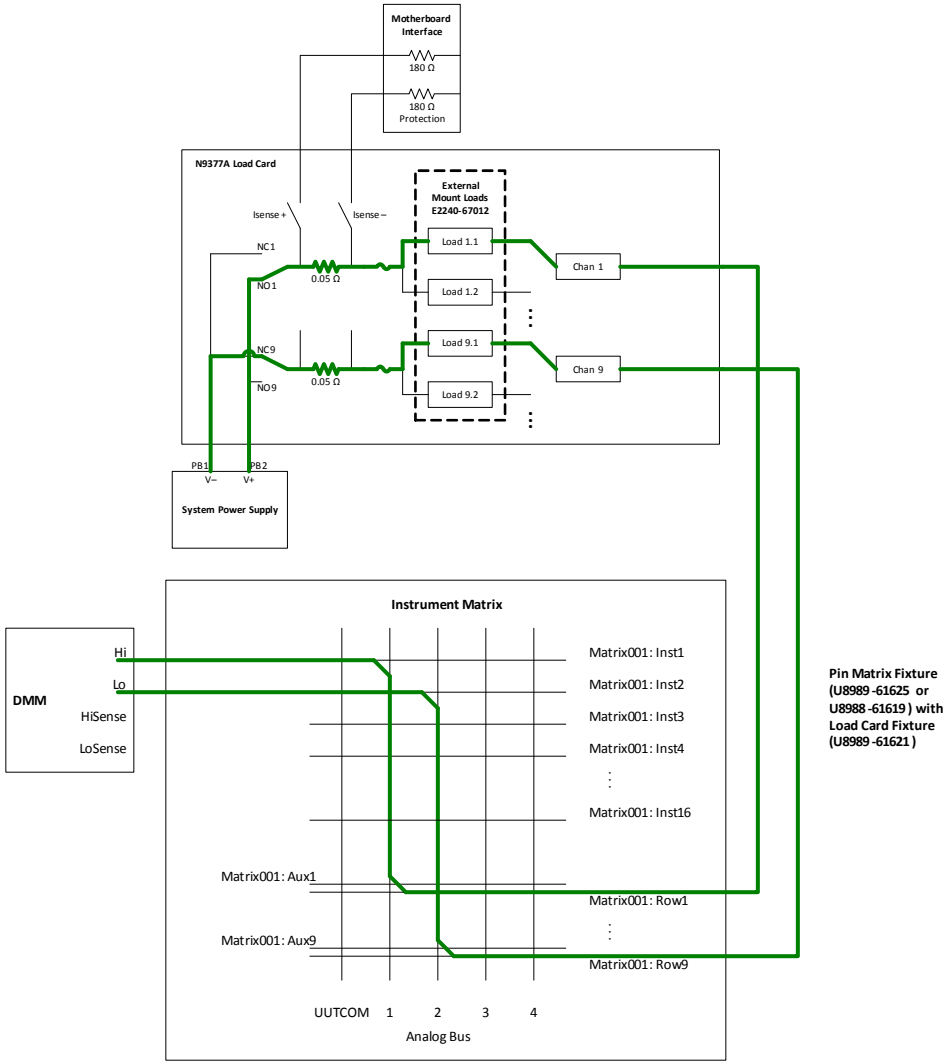
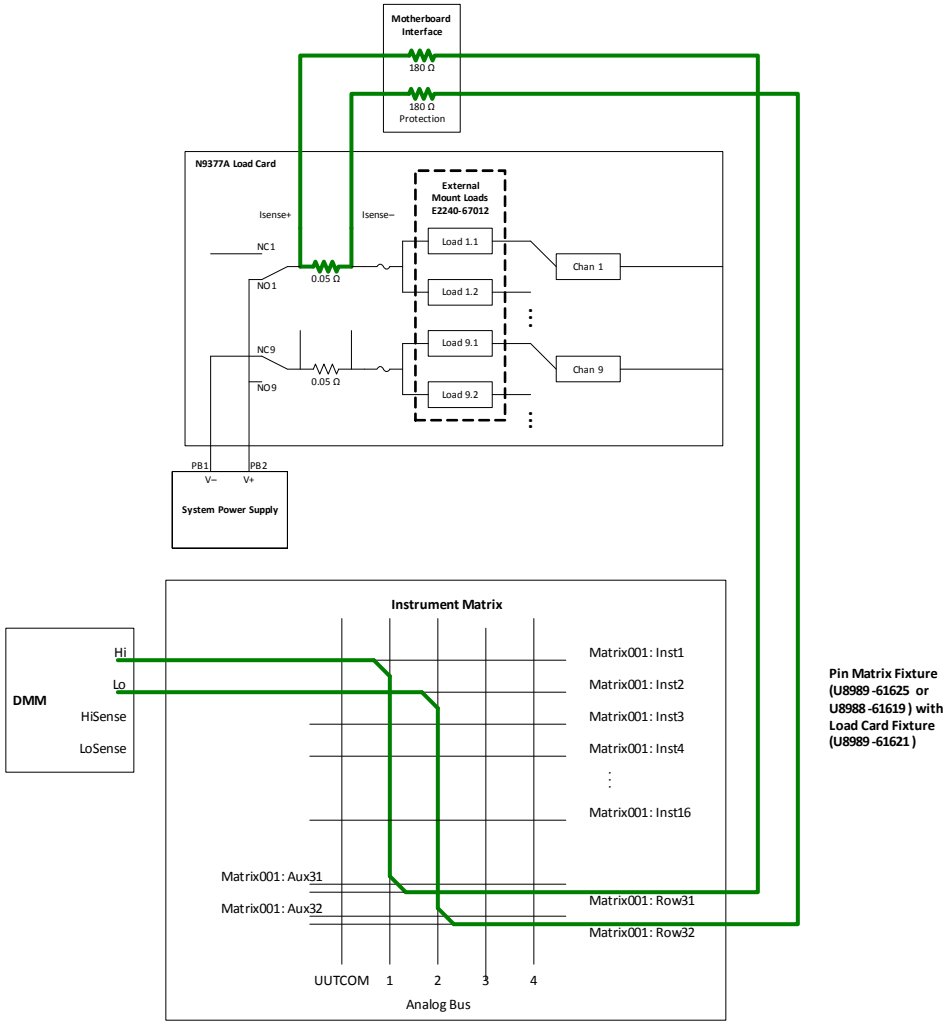


Figure 4-35 N9377A Current Sense Test



N9378A Load Card Test

This test verifies the physical connections between the N9378A Load Card, power supply, and system ICA.

This test consists of an unpowered load card test and a powered load card test.

The load relay switches are tested in the unpowered load card test. In this test, an external mount load with an effective load resistance of 820 Ω (E6170-66520) is mounted on the N9378A. Use a DMM to measure the resistance path between channel 1 and Pwr 1 via Load1.1. This test is repeated until channel 24 with loadX.1, loadX.2, loadX.3 and loadX.4. X represents the channel number from 1 to 24.

Figure 4-36 illustrates the resistance measurement path for the N9378A unpowered load card test.

The powered load card test requires a DUT power supply. If no DUT power supply is present, this test will be skipped. There are four power groups for this test, Pwr 1-6, Pwr 7-12, Pwr 13-18, and Pwr 19-24. The DUT power supply is set to output +5 V (current limit at 0.1 A) and the DMM will measure the voltage via the load card power groups, NC and NO. For example, Pwr 1-6 connects to NC, while Pwr 7-12 connects to NO and the DMM measures the voltage. The test then repeats with Pwr 1-6 connected to NO and Pwr 7-12 connected to NC. This sequence is repeated until all load channels are tested. Figure 4-37 illustrates the measurement path for the N9378A powered load card test.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61621 cable.

Figure 4-36 N9378A Unpowered Load Card Test

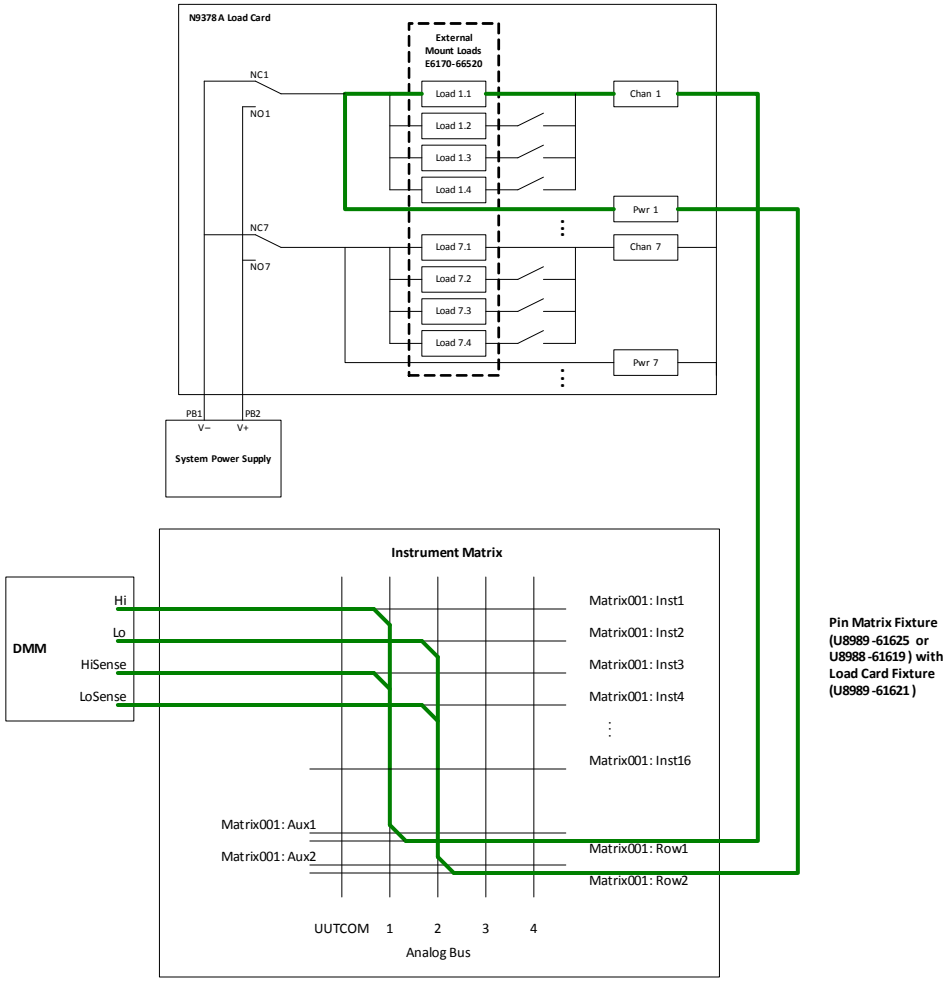
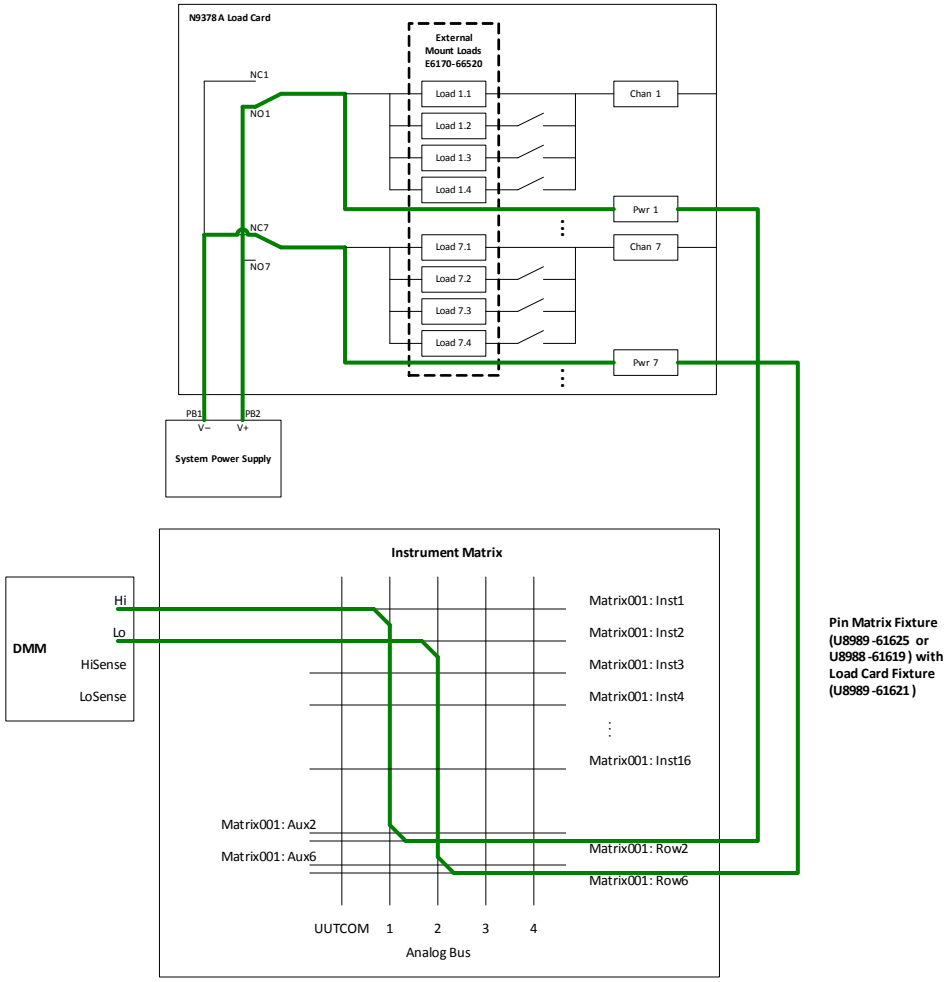


Figure 4-37 N9378A Powered Load Card Test



U7179A Load Card Test

This test verifies the physical connections between the U7179A Load Card, power supply, and system ICA.

This test consists of an unpowered load card test, a powered load card test, and a current sense test.

The load relay switches are tested in the unpowered load card test. In this test, an external mount load with an effective load resistance of 28.86 Ω (E2240-67012) is mounted on the U7179A, J1 and J2 connector. Use a DMM to measure the resistance path between channel 1 and channel 9 via NC and NO, similarly for channel 2 and channel 10, and so on until channel 8 and channel 16. Figure 4-38 illustrates the resistance measurement path for the U7179A unpowered load card test.

The powered load card test requires a DUT power supply. If no DUT power supply is present, this test will be skipped. The DUT power supply is set to output +5 V (current limit at 0.1 A) and the DMM will measure the voltage via the load card channels, NC and NO. Figure 4-39 illustrates the measurement path for the U7179A powered load card test.

Figure 4-40 illustrates the internal and external switching connections to test the U7179A current sense. This test measures the resistance of the current sense path via the SLU backplane.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61621 cable.

Figure 4-38 U7179A Unpowered Load Card Test

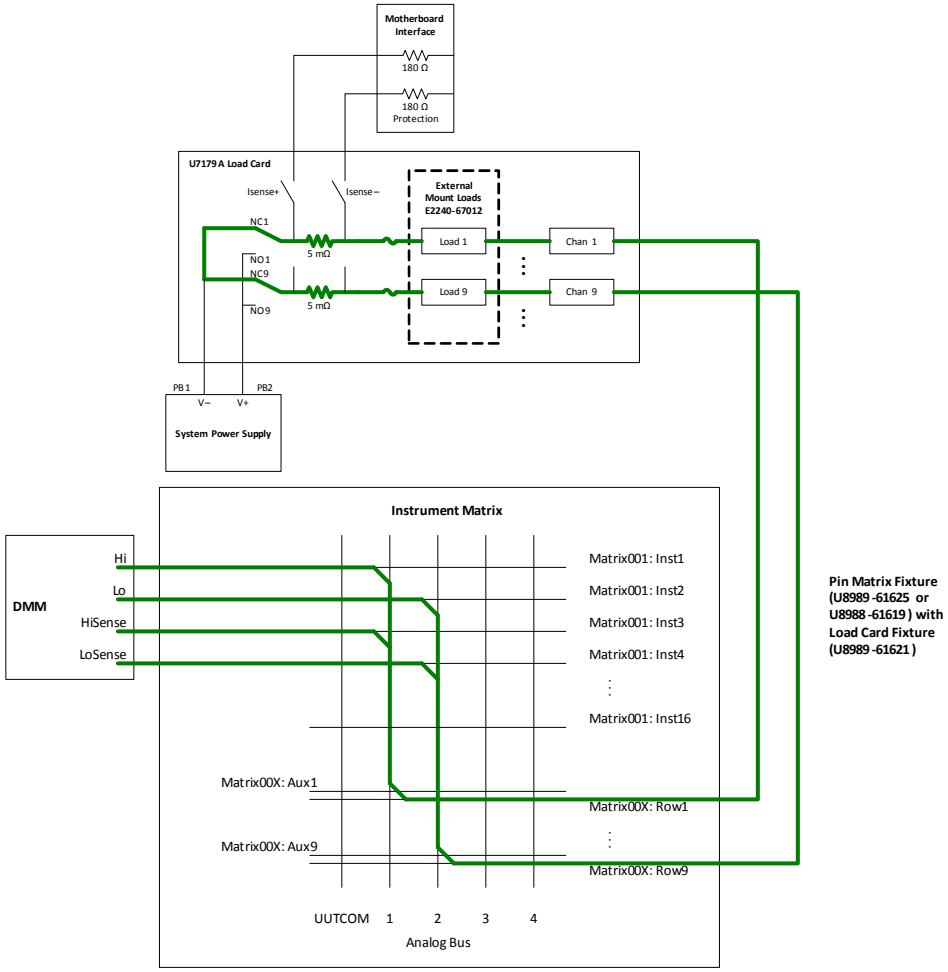


Figure 4-39 U7179A Powered Load Card Test

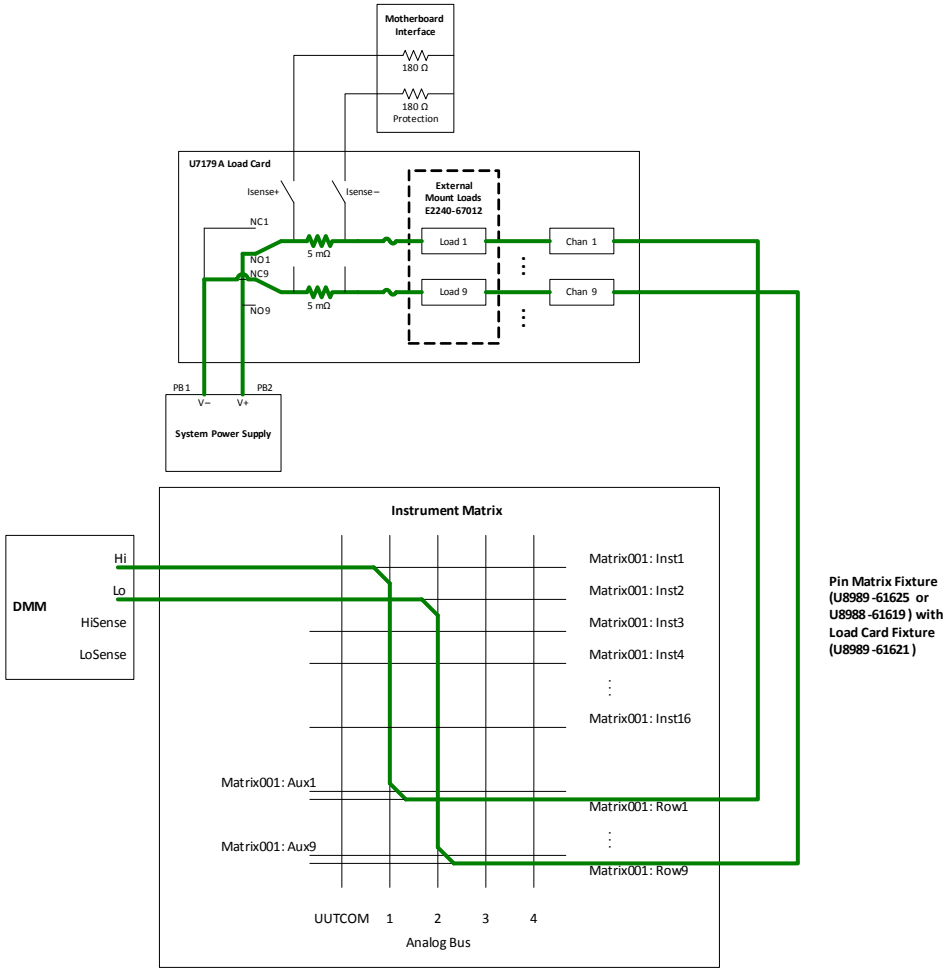
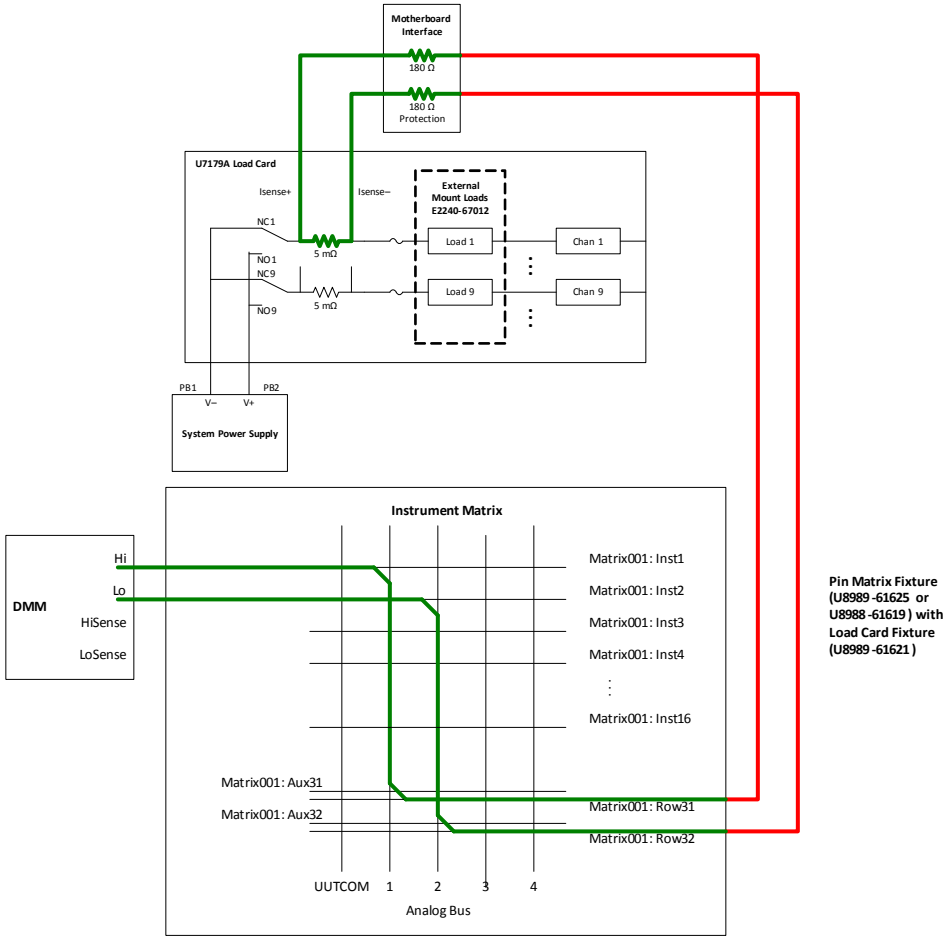


Figure 4-40 U7179A Current Sense Test



N9379A Load Card Test

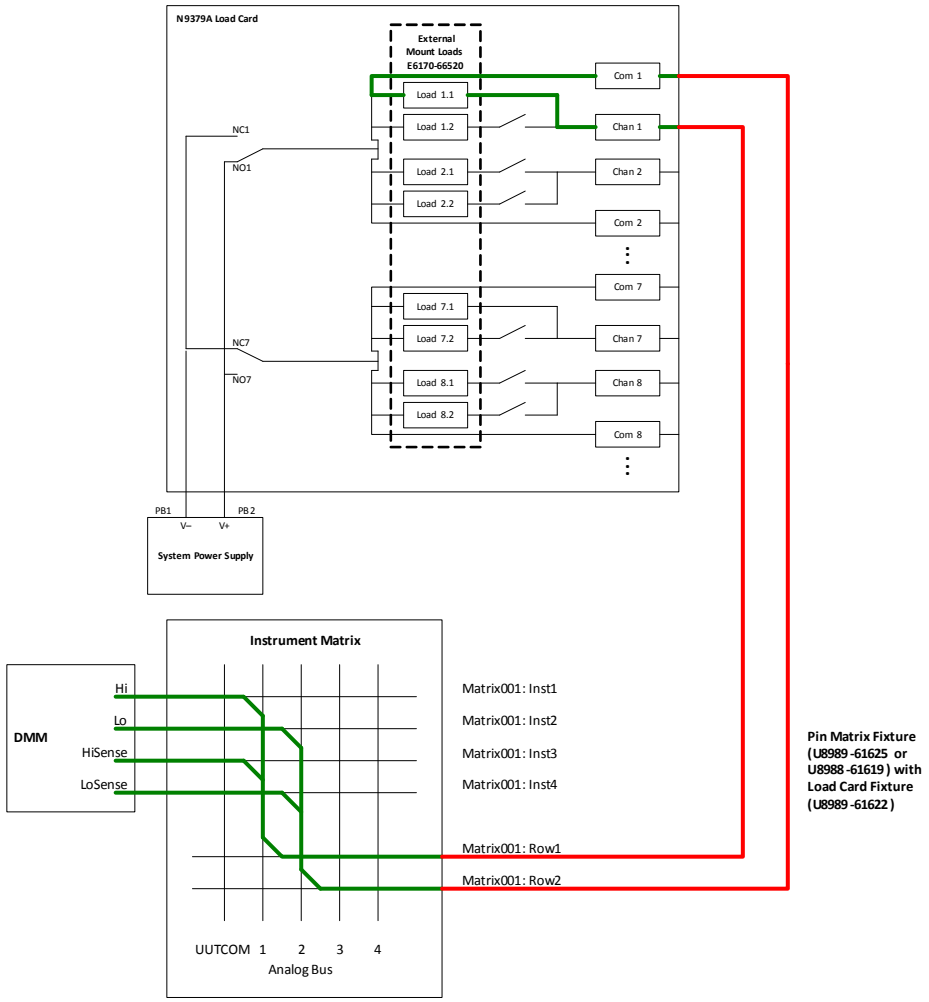
This test verifies the physical connections between the N9379A Load Card, power supply, and system ICA.

This test sequence consists of an unpowered load card test, and a powered load card test.

The load relay switches are tested in the unpowered load card test. In this test, an external mount load with an effective load resistance of 820 Ω (E6170-66520) is mounted on the N9379A. Use a DMM to measure the resistance path between channel X and com X via loadX.1 follow by loadX.2. X represents the channel number from 1 to 48. Figure 4-41 illustrates the resistance measurement path for the N9379A unpowered load card test.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61622 cable.

Figure 4-41 N9379A Unpowered Load Card Test



E6178B Load Card Test

This test verifies the E6178B Load Card.

This test consists of an unpowered load card test and a current sense test.

The load relay switches are tested in the unpowered load card test. In this test, a loopback cable, E6170-61619 is installed from the E6178B J1 connector to J3 connector. Use a DMM to measure the resistance (100 Ω) path between Channel 1 and Channel 2 until Channel 8. Figure 4-42 illustrates the resistance measurement path for the E6178B unpowered load card test. The 100 Ohm resistor is connected from the fixture U8989-61624 cable.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61624 cable.

Figure 4-43 illustrates the internal and external switching connections to test the E6178B current sense. This test measures the resistance of the current sense path via the SLU backplane.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61621 cable.

Figure 4-42 E6178B Unpowered Load Card Test

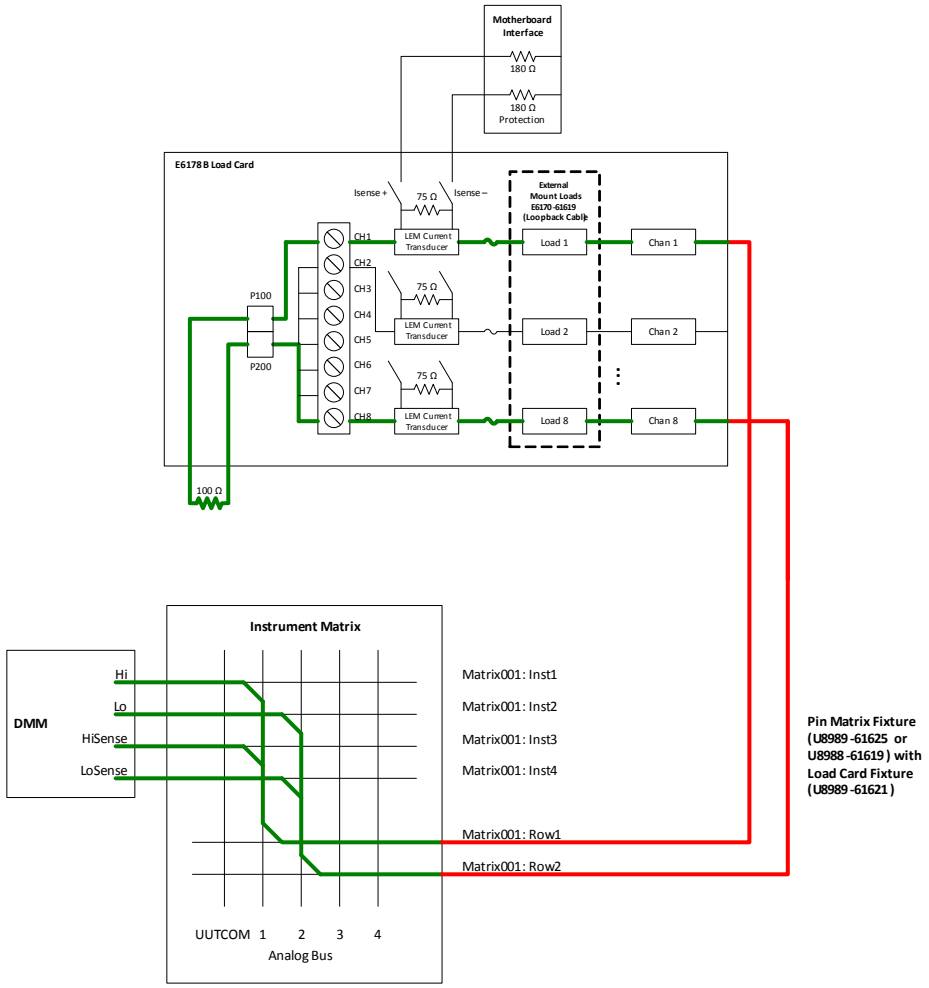
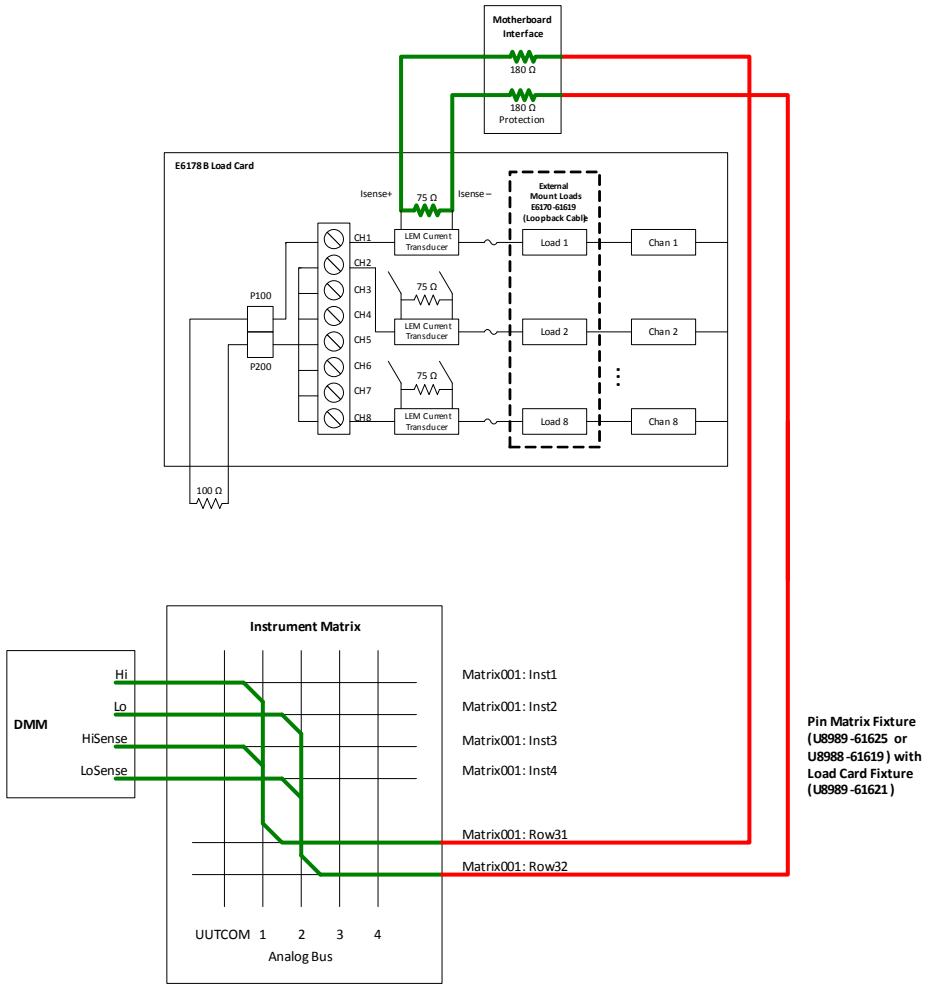


Figure 4-43 E6178B Current Sense Test



U7178A Load Card Test

This test verifies the U7178A Load Card.

This test consists of an unpowered load card test and a current sense test.

The load relay switches are tested in the unpowered load card test. In this test, a loopback cable, E6170-61619 is installed from the J1 connector to J3 connector of the U7178A. Use a DMM to measure the resistance (100 Ω) path between Channel 1 and Channel 2 until Channel 8. Figure 4-44 illustrates the resistance measurement path for the U7178A unpowered load card test. The 100 Ohm resistor is connected from the fixture U8989-61624 cable.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61624 cable.

Figure 4-45 illustrates the internal and external switching connections to test the U7178A current sense. This test measures the resistance of the current sense path via the SLU backplane.

This test requires a pin matrix fixture (U8989-61625 or U8989-61619) and a U8989-61621 cable.

Figure 4-44 U7178A Unpowered Load Card Test

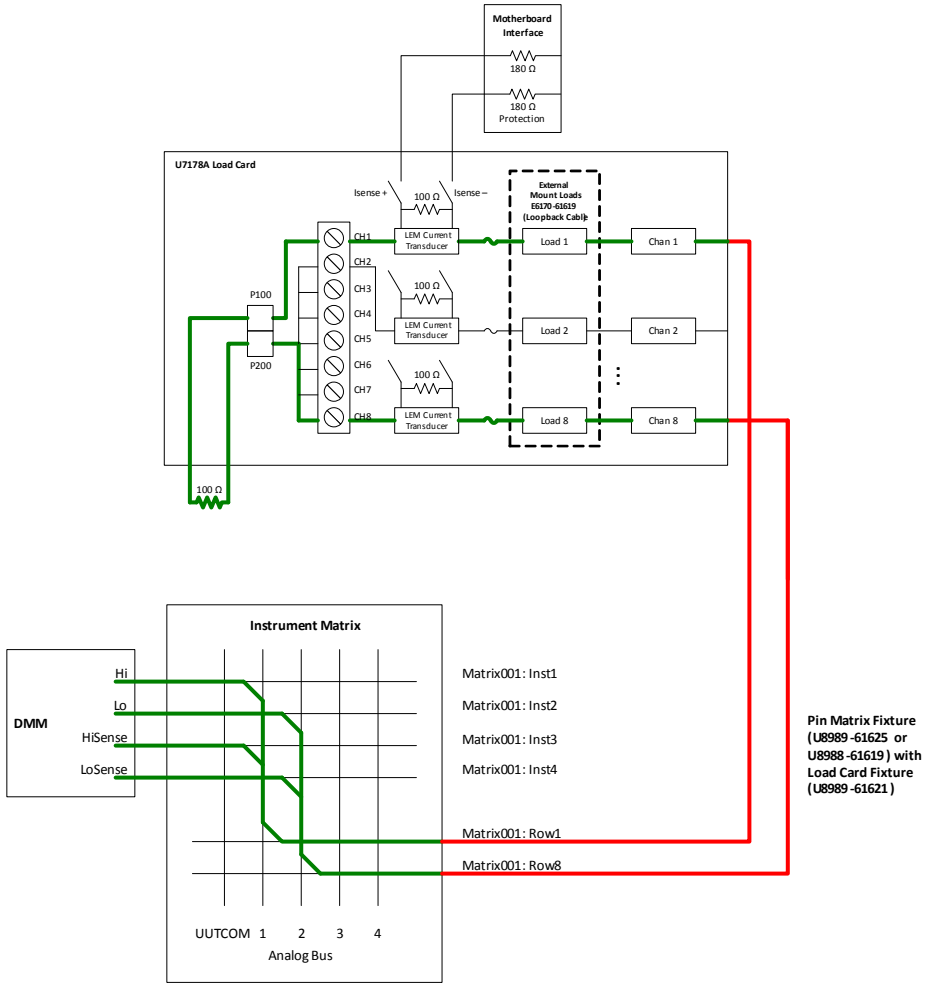
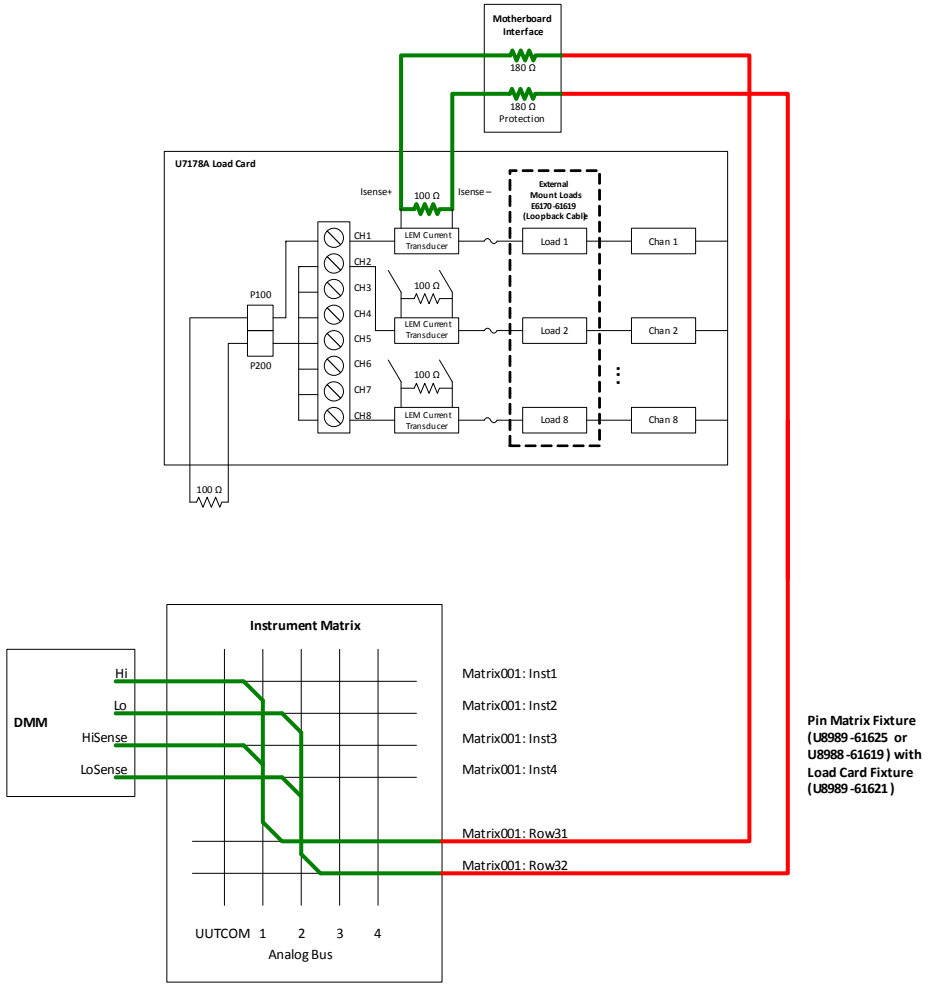


Figure 4-45 U7178A Current Sense Test



5
Diagnostic Test Fixture Details

U8989-61625 E8792A/E8793A Pin Matrix Cable

Figure 5-1 U8989-61625 E8792A/E8793A Pin Matrix Cable

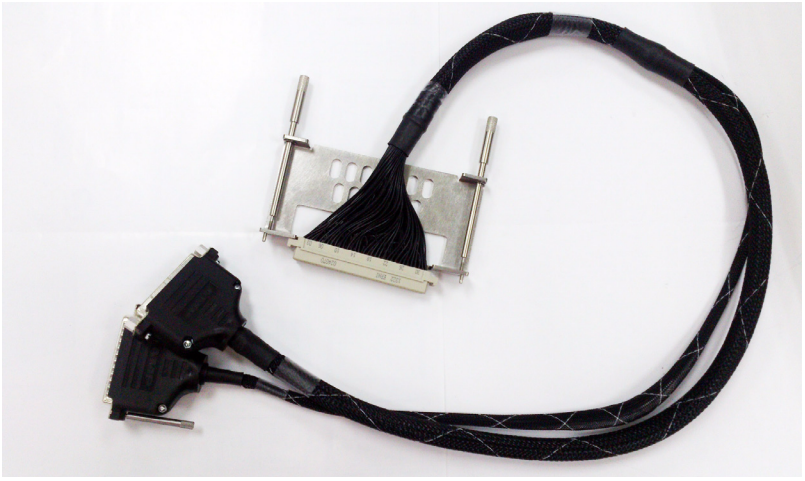


Figure 5-2 U8989-61625 E8792A/E8793A Pin Matrix Cable Schematic

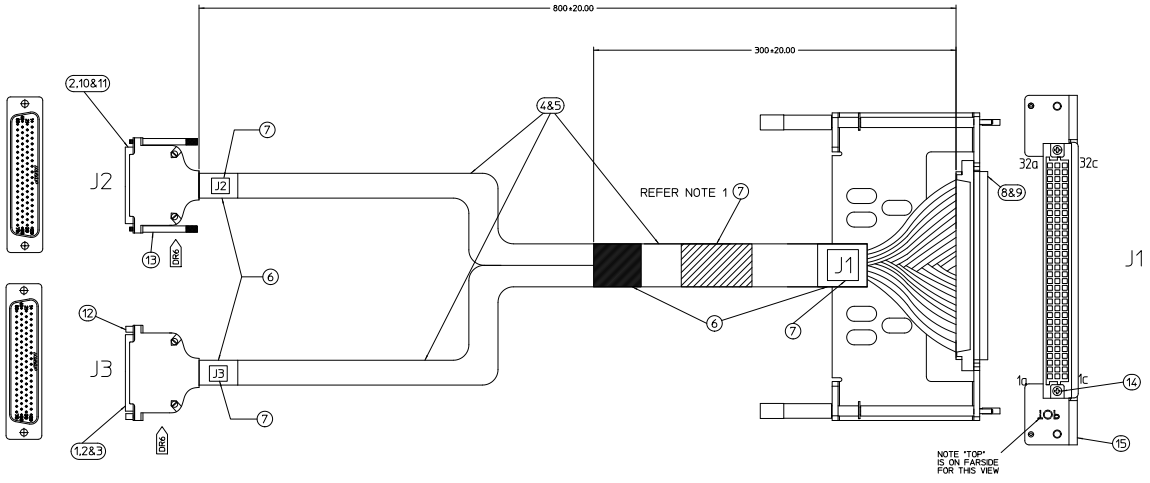


Table 5-1 U8989-61625 Cable Pinout

J1			
Connect to E8792A/E8793A P2 Connector			
Row	c	b	a
1	J1_c1	J1_b1	J1_a1
2	J1_c2	J1_b2	J1_a2
3	J1_c3	J1_b3	J1_a3
4	J1_c4	J1_b4	J1_a4
5	J1_c5	J1_b5	J1_a5
6	J1_c6	J1_b6	J1_a6
7	J1_c7	J1_b7	J1_a7
8	J1_c8	J1_b8	J1_a8
9	J1_c9	J1_b9	J1_a9
10	J1_c10	J1_b10	J1_a10
11	J1_c11	J1_b11	J1_a11
12	J1_c12	J1_b12	J1_a12
13	J1_c13	J1_b13	J1_a13
14	J1_c14	J1_b14	J1_a14
15	J1_c15	J1_b15	J1_a15
16	J1_c16	J1_b16	J1_a16
17	J1_c17	J1_b17	J1_a17
18	J1_c18	J1_b18	J1_a18
19	J1_c19	J1_b19	J1_a19
20	J1_c20	J1_b20	J1_a20
21	J1_c21	J1_b21	J1_a21
22	J1_c22	J1_b22	J1_a22
23	J1_c23	J1_b23	J1_a23
24	J1_c24	J1_b24	J1_a24
25	J1_c25	J1_b25	J1_a25
26	J1_c26	J1_b26	J1_a26
27	J1_c27	J1_b27	J1_a27
28	J1_c28	J1_b28	J1_a28
29	J1_c29	J1_b29	J1_a29
30	J1_c30	J1_b30	J1_a30
31	J1_c31	J1_b31	J1_a31
32	J1_c32	J1_b32	J1_a32

J2							
Connect to the Other Test Cable							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	J1_a1	21	J1_a21	40	J1_b1	60	J1_b21
2	J1_a2	22	J1_a22	41	J1_b2	61	J1_b22
3	J1_a3	23	J1_a23	42	J1_b3	62	J1_b23
4	J1_a4	24	J1_a24	43	J1_b4	63	J1_b24
5	J1_a5	25	J1_a25	44	J1_b5	64	J1_b25
6	J1_a6	26	J1_a26	45	J1_b6	65	J1_b26
7	J1_a7	27	J1_a27	46	J1_b7	66	J1_b27
8	J1_a8	28	J1_a28	47	J1_b8	67	J1_b28
9	J1_a9	29	J1_a29	48	J1_b9	68	J1_b29
10	J1_a10	30	J1_a30	49	J1_b10	69	J1_b30
11	J1_a11	31	J1_a31	50	J1_b11	70	J1_b31
12	J1_a12	32	J1_a32	51	J1_b12	71	J1_b32
13	J1_a13	33	J1_c1	52	J1_b13	72	J1_c8
14	J1_a14	34	J1_c2	53	J1_b14	73	J1_c9
15	J1_a15	35	J1_c3	54	J1_b15	74	J1_c10
16	J1_a16	36	J1_c4	55	J1_b16	75	J1_c11
17	J1_a17	37	J1_c5	56	J1_b17	76	J1_c12
18	J1_a18	38	J1_c6	57	J1_b18	77	J1_c13
19	J1_a19	39	J1_c7	58	J1_b19	78	J1_c14
20	J1_a20			59	J1_b20		

J3							
Connect to Pin Matrix Cable - J2 Connector							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	Jumper	21	Jumper	40	J3_33	60	J1_c21
2		22		41	J3_34	61	J1_c22
3	Jumper	23	Jumper	42	J3_35	62	J1_c23
4		24		43	J3_36	63	J1_c24
5	Jumper	25	Jumper	44	J3_37	64	J1_c25
6		26		45	J3_38	65	J1_c26
7	Jumper	27	Jumper	46	J3_39	66	J1_c27
8		28		47	J3_72	67	J1_c28
9	Jumper	29	Jumper	48	J3_73	68	J1_c29
10		30		49	J3_74	69	J1_c30
11	Jumper	31	Jumper	50	J3_75	70	J1_c31
12		32		51	J3_76	71	J1_c32
13	Jumper	33	J3_33	52	J3_77	72	J3_72
14		34	J3_34	53	J3_78	73	J3_73
15	Jumper	35	J3_35	54	J1_c15	74	J3_74
16		36	J3_36	55	J1_c16	75	J3_75
17	Jumper	37	J3_37	56	J1_c17	76	J3_76
18		38	J3_38	57	J1_c18	77	J3_77
19	Jumper	39	J3_39	58	J1_c19	78	J3_78
20				59	J1_c20		

U8989-61619 E8782A/E8783A Pin Matrix Cable

Figure 5-3 U8989-61619 E8782A/E8783A Pin Matrix Cable

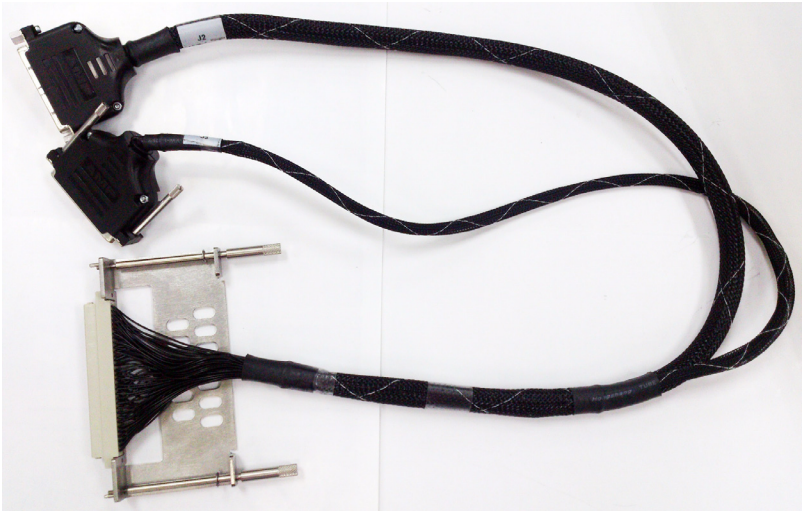


Figure 5-4 U8989-61619 E8782A/E8783A Pin Matrix Cable Schematic

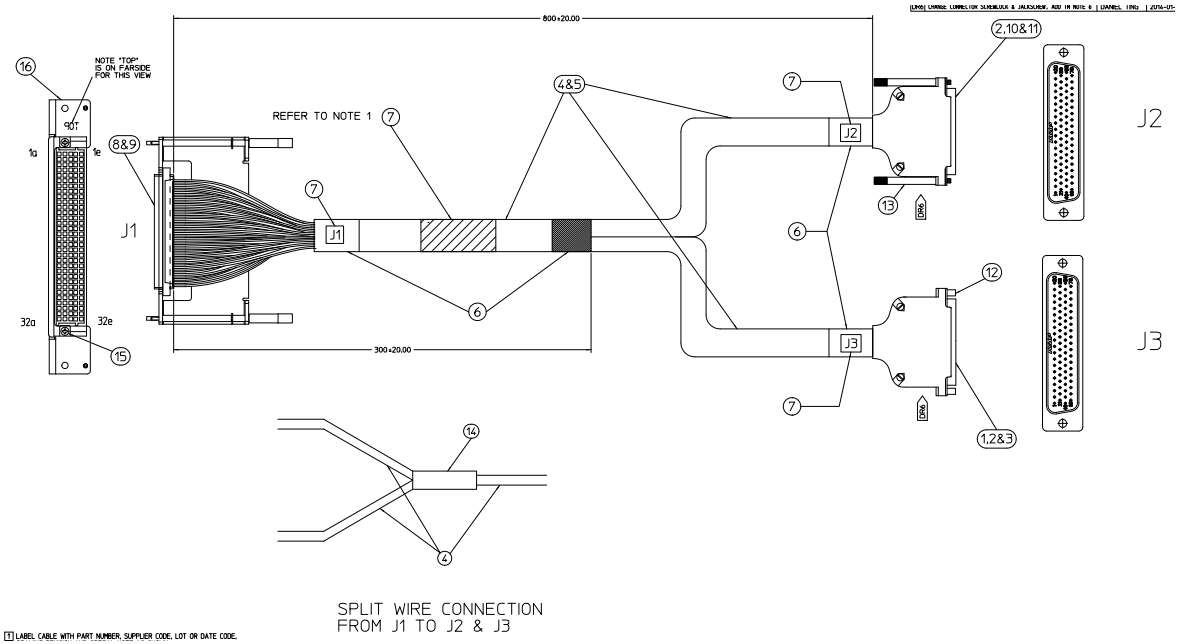


Table 5-2 U8989-61619 Cable Pinout

J1[1][2]							
Connect to E8782A/E8783A P2 Connector							
Row	e	d		c	b		a
1	J1_e1	J1_d1	Jumper	J1_c1	J1_b1	Jump to J1_a1	J1_a1
2	J1_e2	J1_d2		J1_c2	J1_b2	Jump to J1_a2	J1_a2
3	J1_e3	J1_d3	Jumper	J1_c3	J1_b3	Jump to J1_a3	J1_a3
4	J1_e4	J1_d4		J1_c4	J1_b4	Jump to J1_a4	J1_a4
5	J1_e5	J1_d5	Jumper	J1_c5	J1_b5	Jump to J1_a5	J1_a5
6	J1_e6	J1_d6		J1_c6	J1_b6	Jump to J1_a6	J1_a6
7	J1_e7	J1_d7	Jumper	J1_c7	J1_b7	Jump to J1_a7	J1_a7
8	J1_e8	J1_d8		J1_c8	J1_b8	Jump to J1_a8	J1_a8
9	J1_e9	J1_d9	Jumper	J1_c9	J1_b9	Jump to J1_a9	J1_a9
10	J1_e10	J1_d10		J1_c10	J1_b10	Jump to J1_a10	J1_a10
11	J1_e11	J1_d11	Jumper	J1_c11	J1_b11	Jump to J1_a11	J1_a11
12	J1_e12	J1_d12		J1_c12	J1_b12	Jump to J1_a12	J1_a12
13	J1_e13	J1_d13	Jumper	J1_c13	J1_b13	Jump to J1_a13	J1_a13
14	J1_e14	J1_d14		J1_c14	J1_b14	Jump to J1_a14	J1_a14
15	J1_e15	J1_d15	Jumper	J1_c15	J1_b15	Jump to J1_a15	J1_a15
16	J1_e16	J1_d16		J1_c16	J1_b16	Jump to J1_a16	J1_a16
17	J1_e17	J1_d17	Jumper	J1_c17	J1_b17	Jump to J1_a17	J1_a17
18	J1_e18	J1_d18		J1_c18	J1_b18	Jump to J1_a18	J1_a18
19	J1_e19	J1_d19	Jumper	J1_c19	J1_b19	Jump to J1_a19	J1_a19
20	J1_e20	J1_d20		J1_c20	J1_b20	Jump to J1_a20	J1_a20
21	J1_e21	J1_d21	Jumper	J1_c21	J1_b21	Jump to J1_a21	J1_a21
22	J1_e22	J1_d22		J1_c22	J1_b22	Jump to J1_a22	J1_a22
23	J1_e23	J1_d23	Jumper	J1_c23	J1_b23	Jump to J1_a23	J1_a23
24	J1_e24	J1_d24		J1_c24	J1_b24	Jump to J1_a24	J1_a24
25	J1_e25	J1_d25	Jumper	J1_c25	J1_b25	Jump to J1_a25	J1_a25
26	J1_e26	J1_d26		J1_c26	J1_b26	Jump to J1_a26	J1_a26
27	J1_e27	J1_d27	Jumper	J1_c27	J1_b27	Jump to J1_a27	J1_a27
28	J1_e28	J1_d28		J1_c28	J1_b28	Jump to J1_a28	J1_a28
29	J1_e29	J1_d29	Jumper	J1_c29	J1_b29	Jump to J1_a29	J1_a29
30	J1_e30	J1_d30		J1_c30	J1_b30	Jump to J1_a30	J1_a30
31	J1_e31	J1_d31	Jumper	J1_c31	J1_b31	Jump to J1_a31	J1_a31
32	J1_e32	J1_d32		J1_c32	J1_b32	Jump to J1_a32	J1_a32

[1] The pinout shown above is for the E8783A only.

[2] The E8782A pinout comprises Row 1 to Row 40 and Aux 1 to Aux 40 only.

J2							
Connect to other test cable							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	J1_e1	21	J1_e21	40	J1_c1	60	J1_c21
2	J1_e2	22	J1_e22	41	J1_c2	61	J1_c22
3	J1_e3	23	J1_e23	42	J1_c3	62	J1_c23
4	J1_e4	24	J1_e24	43	J1_c4	63	J1_c24
5	J1_e5	25	J1_e25	44	J1_c5	64	J1_c25
6	J1_e6	26	J1_e26	45	J1_c6	65	J1_c26
7	J1_e7	27	J1_e27	46	J1_c7	66	J1_c27
8	J1_e8	28	J1_e28	47	J1_c8	67	J1_c28
9	J1_e9	29	J1_e29	48	J1_c9	68	J1_c29
10	J1_e10	30	J1_e30	49	J1_c10	69	J1_c30
11	J1_e11	31	J1_e31	50	J1_c11	70	J1_c31
12	J1_e12	32	J1_e32	51	J1_c12	71	J1_c32
13	J1_e13	33	J1_a1	52	J1_c13	72	J1_a8
14	J1_e14	34	J1_a2	53	J1_c14	73	J1_a9
15	J1_e15	35	J1_a3	54	J1_c15	74	J1_a10
16	J1_e16	36	J1_a4	55	J1_c16	75	J1_a11
17	J1_e17	37	J1_a5	56	J1_c17	76	J1_a12
18	J1_e18	38	J1_a6	57	J1_c18	77	J1_a13
19	J1_e19	39	J1_a7	58	J1_c19	78	J1_a14
20	J1_e20			59	J1_c20		

J3							
Connect to Pin Matrix Cable - J2 Connector							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	Jumper	21	Jumper	40	J3_33	60	J1_a21
2		22		41	J3_34	61	J1_a22
3	Jumper	23	Jumper	42	J3_35	62	J1_a23
4		24		43	J3_36	63	J1_a24
5	Jumper	25	Jumper	44	J3_37	64	J1_a25
6		26		45	J3_38	65	J1_a26
7	Jumper	27	Jumper	46	J3_39	66	J1_a27
8		28		47	J3_72	67	J1_a28
9	Jumper	29	Jumper	48	J3_73	68	J1_a29
10		30		49	J3_74	69	J1_a30
11	Jumper	31	Jumper	50	J3_75	70	J1_a31
12		32		51	J3_76	71	J1_a32
13	Jumper	33	J3_33	52	J3_77	72	J3_72
14		34	J3_34	53	J3_78	73	J3_73
15	Jumper	35	J3_35	54	J1_a15	74	J3_74
16		36	J3_36	55	J1_a16	75	J3_75
17	Jumper	37	J3_37	56	J1_a17	76	J3_76
18		38	J3_38	57	J1_a18	77	J3_77
19	Jumper	39	J3_39	58	J1_a19	78	J3_78
20				59	J1_a20		

U8989-61620 SLU Utility Cable

Figure 5-5 U8989-61620 SLU Utility Cable

Figure 5-6 U8989-61620 SLU Utility Cable Schematic

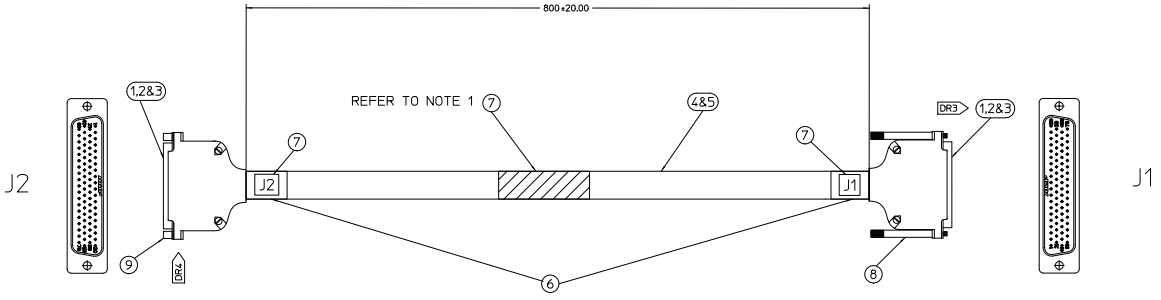


Table 5-3 U8989-61620 Cable Pinout

J1									
Connect to SLU Utility									
Pin	Connect to		Pin	Connect to	Pin	Connect to		Pin	Connect to
1	J1_1		21	J1_21	40	J1_40		60	J1_60
2	J1_2	Jump to J1_22	22	J1_22	41	J1_41	Jump to J1_61	61	J1_61
3	J1_3	Jump to J1_23	23	J1_23	42	J1_42	Jump to J1_62	62	J1_62
4	J1_4	Jump to J1_24	24	J1_24	43	J1_43	Jump to J1_63	63	J1_63
5	J1_5	Jump to J1_25	25	J1_25	44	J1_44	Jump to J1_64	64	J1_64
6	J1_6	Jump to J1_26	26	J1_26	45	J1_45	Jump to J1_65	65	J1_65
7	J1_7	Jump to J1_27	27	J1_27	46	J1_46	Jump to J1_66	66	J1_66
8	J1_8	Jump to J1_28	28	J1_28	47	J1_47	Jump to J1_67	67	J1_67
9	J1_9	Jump to J1_29	29	J1_29	48	J1_48	Jump to J1_68	68	J1_68
10	J1_10		30	J1_30	49	J1_49		69	J1_69
11	J1_11		31	J1_31	50	J1_50		70	J1_70
12	J1_12		32	J1_32	51	J1_51		71	J1_71
13	J1_13		33	J1_33	52	J1_52		72	J1_72
14	J1_14		34	J1_34	53	J1_53		73	J1_73
15	N/C		35	N/C	54	N/C		74	J1_74
16	J1_16		36	J1_36	55	N/C		75	J1_75
17	J1_17		37	J1_37	56	N/C		76	N/C
18	N/C		38	N/C	57	N/C		77	N/C
19	N/C		39	N/C	58	N/C		78	N/C
20	N/C				59	N/C			

J2							
Connect to Pin Matrix Test Kit - J2 Connector							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	J1_16	21	J1_21	40	N/C	60	N/C
2	J1_36	22	J1_40	41	N/C	61	N/C
3	J1_70	23	J1_60	42	N/C	62	N/C
4	J1_71	24	J1_10	43	N/C	63	N/C
5	J1_72	25	J1_30	44	N/C	64	N/C
6	J1_73	26	J1_49	45	N/C	65	N/C
7	J1_74	27	J1_69	46	N/C	66	N/C
8	J1_50	28	J1_17	47	N/C	67	N/C
9	J1_51	29	J1_37	48	N/C	68	N/C
10	J1_52	30	J1_75	49	N/C	69	N/C
11	J1_53	31	N/C	50	N/C	70	N/C
12	J1_11	32	N/C	51	N/C	71	N/C
13	J1_12	33	N/C	52	N/C	72	N/C
14	J1_13	34	N/C	53	N/C	73	N/C
15	J1_14	35	N/C	54	N/C	74	N/C
16	J1_31	36	N/C	55	N/C	75	N/C
17	J1_32	37	N/C	56	N/C	76	N/C
18	J1_33	38	N/C	57	N/C	77	N/C
19	J1_34	39	N/C	58	N/C	78	N/C
20	J1_1			59	N/C		

U8989-61621 24/16/8 Channel Load Card Cable

Figure 5-7 U8989-61621 24/16/8 Channel Load Card Cable

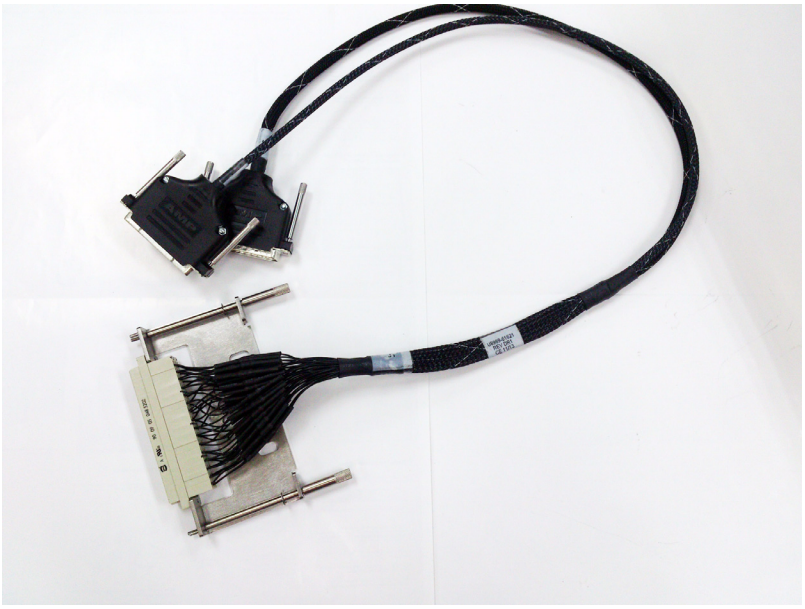


Figure 5-8 U8989-61621 24/16/8 Channel Load Card Cable Schematic

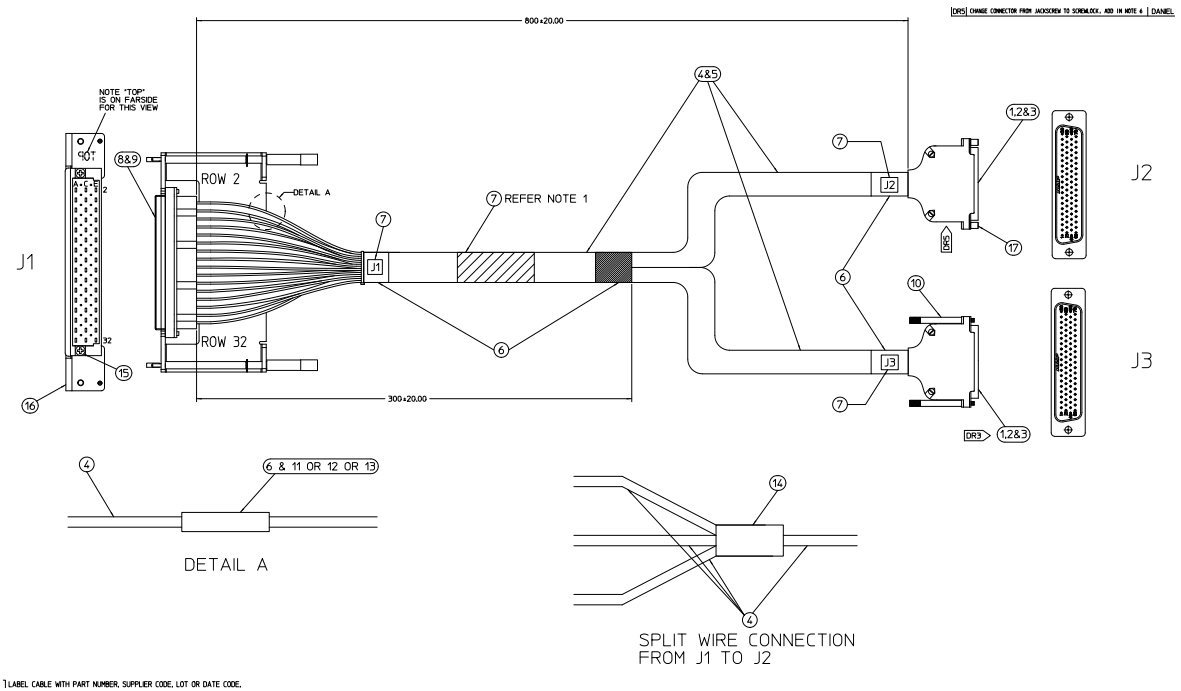


Table 5-4 U8989-61621 Cable Pinout

J1						
Connect to 24/6/8 Channel Load Card						
Row	e		c		a	
2	J1_e2	Add 75 Ohm R	J1_c2	Add 82 Ohm R	J1_a2	Add 91 Ohm R
4	J1_e4	Add 75 Ohm R	J1_c4	Add 82 Ohm R	J1_a4	Add 91 Ohm R
6	J1_e6	Add 75 Ohm R	J1_c6	Add 82 Ohm R	J1_a6	Add 91 Ohm R
8	J1_e8	Add 75 Ohm R	J1_c8	Add 82 Ohm R	J1_a8	Add 91 Ohm R
10	J1_e10	Add 75 Ohm R	J1_c10	Add 82 Ohm R	J1_a10	Add 91 Ohm R
12	J1_e12	Add 75 Ohm R	J1_c12	Add 82 Ohm R	J1_a12	Add 91 Ohm R
14	J1_e14	Add 75 Ohm R	J1_c14	Add 82 Ohm R	J1_a14	Add 91 Ohm R
16	J1_e16	Add 75 Ohm R	J1_c16	Add 82 Ohm R	J1_a16	Add 91 Ohm R
18	J1_e18	Add 75 Ohm R	J1_c18	Add 82 Ohm R	J1_a18	Add 91 Ohm R
20	J1_e20	Add 75 Ohm R	J1_c20	Add 82 Ohm R	J1_a20	Add 91 Ohm R
22	J1_e22	Add 75 Ohm R	J1_c22	Add 82 Ohm R	J1_a22	Add 91 Ohm R
24	J1_e24	Add 75 Ohm R	J1_c24	Add 82 Ohm R	J1_a24	Add 91 Ohm R
26	J1_e26	Add 75 Ohm R	J1_c26	Add 82 Ohm R	J1_a26	Add 91 Ohm R
28	J1_e28	Add 75 Ohm R	J1_c28	Add 82 Ohm R	J1_a28	Add 91 Ohm R
30	J1_e30	Add 75 Ohm R	J1_c30	Add 82 Ohm R	J1_a30	Add 91 Ohm R
32	J1_e32	Add 75 Ohm R	J1_c32	Add 82 Ohm R	J1_a32	Add 91 Ohm R

J2								
Connect to Pin Matrix Test Kit - J2 Connector								
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	J1_e2, J1_c2, J1_a2	21	N/C	40	N/C	60	N/C
2	J1_e4, J1_c4, J1_a4	22	N/C	41	N/C	61	N/C
3	J1_e6, J1_c6, J1_a6	23	N/C	42	N/C	62	N/C
4	J1_e8, J1_c8, J1_a8	24	N/C	43	N/C	63	N/C
5	J1_e10, J1_c10, J1_a10	25	N/C	44	N/C	64	N/C
6	J1_e12, J1_c12, J1_a12	26	N/C	45	N/C	65	N/C
7	J1_e14, J1_c14, J1_a14	27	N/C	46	N/C	66	N/C
8	J1_e16, J1_c16, J1_a16	28	N/C	47	N/C	67	N/C
9	J1_e18, J1_c18, J1_a18	29	N/C	48	N/C	68	N/C
10	J1_e20, J1_c20, J1_a20	30	N/C	49	N/C	69	N/C
11	J1_e22, J1_c22, J1_a22	31	J3_11	50	N/C	70	N/C
12	J1_e24, J1_c24, J1_a24	32	J3_31	51	N/C	71	N/C
13	J1_e26, J1_c26, J1_a26	33	N/C	52	N/C	72	N/C
14	J1_e28, J1_c28, J1_a28	34	N/C	53	N/C	73	N/C
15	J1_e30, J1_c30, J1_a30	35	N/C	54	N/C	74	N/C
16	J1_e32, J1_c32, J1_a32	36	N/C	55	N/C	75	N/C
17	N/C	37	N/C	56	N/C	76	N/C
18	N/C	38	N/C	57	N/C	77	N/C
19	N/C	39	N/C	58	N/C	78	N/C
20	N/C			59	N/C		

J3							
Connect to SLU Utility							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	N/C	21	N/C	40	N/C	60	N/C
2	N/C	22	N/C	41	N/C	61	N/C
3	N/C	23	N/C	42	N/C	62	N/C
4	N/C	24	N/C	43	N/C	63	N/C
5	N/C	25	N/C	44	N/C	64	N/C
6	N/C	26	N/C	45	N/C	65	N/C
7	N/C	27	N/C	46	N/C	66	N/C
8	N/C	28	N/C	47	N/C	67	N/C
9	N/C	29	N/C	48	N/C	68	N/C
10	N/C	30	N/C	49	N/C	69	N/C
11	J3_11	31	J3_31	50	N/C	70	N/C
12	N/C	32	N/C	51	N/C	71	N/C
13	N/C	33	N/C	52	N/C	72	N/C
14	N/C	34	N/C	53	N/C	73	N/C
15	N/C	35	N/C	54	N/C	74	N/C
16	N/C	36	N/C	55	N/C	75	N/C
17	N/C	37	N/C	56	N/C	76	N/C
18	N/C	38	N/C	57	N/C	77	N/C
19	N/C	39	N/C	58	N/C	78	N/C
20	N/C			59	N/C		

U8989-61622 48 Channel Load Card Cable

Figure 5-9 U8989-61622 48 Channel Load Card Cable

Figure 5-10 U8989-61622 48 Channel Load Card Cable Schematic

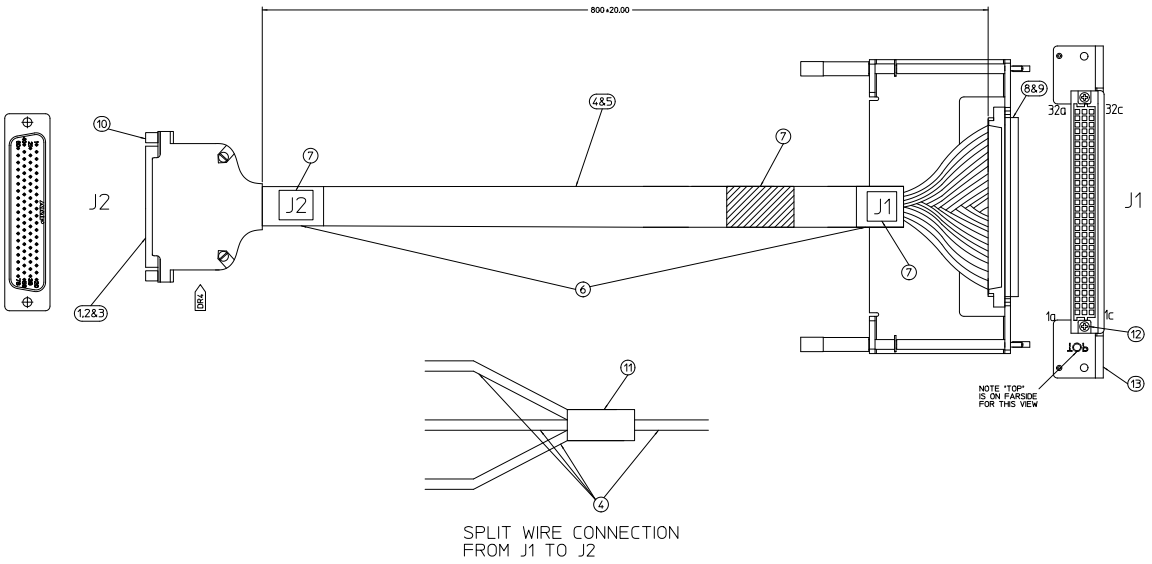


Table 5-5 U8989-61622 Cable Pinout

J1			
Connect to 48 Channel Load Card			
Row	c	b	a
1	J1_c1	J1_b1	J1_a1
2	J1_c2	J1_b2	J1_a2
3	J1_c3	J1_b3	J1_a3
4	J1_c4	J1_b4	J1_a4
5	J1_c5	J1_b5	J1_a5
6	J1_c6	J1_b6	J1_a6
7	J1_c7	J1_b7	J1_a7
8	J1_c8	J1_b8	J1_a8
9	J1_c9	J1_b9	J1_a9
10	J1_c10	J1_b10	J1_a10
11	J1_c11	J1_b11	J1_a11
12	J1_c12	J1_b12	J1_a12
13	J1_c13	J1_b13	J1_a13
14	J1_c14	J1_b14	J1_a14
15	J1_c15	J1_b15	J1_a15
16	J1_c16	J1_b16	J1_a16
17	J1_c17	J1_b17	J1_a17
18	J1_c18	J1_b18	J1_a18
19	J1_c19	J1_b19	J1_a19
20	J1_c20	J1_b20	J1_a20
21	J1_c21	J1_b21	J1_a21
22	J1_c22	J1_b22	J1_a22
23	J1_c23	J1_b23	J1_a23
24	J1_c24	J1_b24	J1_a24
25	J1_c25	J1_b25	J1_a25
26	J1_c26	J1_b26	J1_a26
27	J1_c27	J1_b27	J1_a27
28	J1_c28	J1_b28	J1_a28
29	J1_c29	J1_b29	J1_a29
30	J1_c30	J1_b30	J1_a30
31	J1_c31	J1_b31	J1_a31
32	J1_c32	J1_b32	J1_a32

J2							
Connect to Pin Matrix Test Kit - J2 Connector							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	J1_c1, J1_b1, J1_a1	21	J1_c21, J1_b21, J1_a21	40	N/C	60	N/C
2	J1_c2, J1_b2, J1_a2	22	J1_c22, J1_b22, J1_a22	41	N/C	61	N/C
3	J1_c3, J1_b3, J1_a3	23	J1_c23, J1_b23, J1_a23	42	N/C	62	N/C
4	J1_c4, J1_b4, J1_a4	24	J1_c24, J1_b24, J1_a24	43	N/C	63	N/C
5	J1_c5, J1_b5, J1_a5	25	J1_c25, J1_b25, J1_a25	44	N/C	64	N/C
6	J1_c6, J1_b6, J1_a6	26	J1_c26, J1_b26, J1_a26	45	N/C	65	N/C
7	J1_c7, J1_b7, J1_a7	27	J1_c27, J1_b27, J1_a27	46	N/C	66	N/C
8	J1_c8, J1_b8, J1_a8	28	J1_c28, J1_b28, J1_a28	47	N/C	67	N/C
9	J1_c9, J1_b9, J1_a9	29	J1_c29, J1_b29, J1_a29	48	N/C	68	N/C
10	J1_c10, J1_b10, J1_a10	30	J1_c30, J1_b30, J1_a30	49	N/C	69	N/C
11	J1_c11, J1_b11, J1_a11	31	J1_c31, J1_b31, J1_a31	50	N/C	70	N/C
12	J1_c12, J1_b12, J1_a12	32	J1_c32, J1_b32, J1_a32	51	N/C	71	N/C
13	J1_c13, J1_b13, J1_a13	33	N/C	52	N/C	72	N/C
14	J1_c14, J1_b14, J1_a14	34	N/C	53	N/C	73	N/C
15	J1_c15, J1_b15, J1_a15	35	N/C	54	N/C	74	N/C
16	J1_c16, J1_b16, J1_a16	36	N/C	55	N/C	75	N/C
17	J1_c17, J1_b17, J1_a17	37	N/C	56	N/C	76	N/C
18	J1_c18, J1_b18, J1_a18	38	N/C	57	N/C	77	N/C
19	J1_c19, J1_b19, J1_a19	39	N/C	58	N/C	78	N/C
20	J1_c20, J1_b20, J1_a20			59	N/C		

U8989-61623 Universal Instrument Routing Card Cable

Figure 5-11 U8989-61623 Universal Instrument Routing Card Cable

Figure 5-12 U8989-61623 Universal Instrument Routing Card Cable Schematic

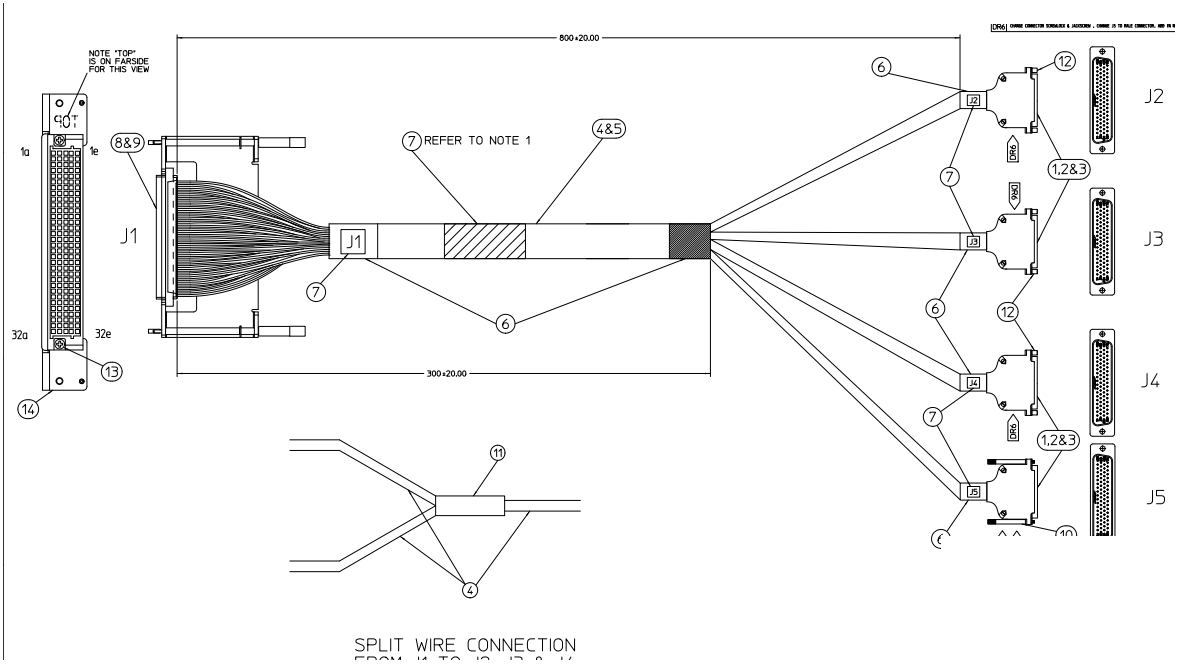


Table 5-6 U8989-61623 Cable Pinout

J1					
Connect to Instrument Routing Card					
Row	e	d	c	b	a
1	J1_e1	J1_d1	J1_c1	J1_b1	J1_a1
2	J1_e2	J1_d2	J1_c2	J1_b2	J1_a2
3	J1_e3	J1_d3	J1_c3	J1_b3	J1_a3
4	J1_e4	J1_d4	J1_c4	J1_b4	J1_a4
5	J1_e5	J1_d5	J1_c5	J1_b5	J1_a5
6	J1_e6	J1_d6	J1_c6	J1_b6	J1_a6
7	J1_e7	J1_d7	J1_c7	J1_b7	J1_a7
8	J1_e8	J1_d8	J1_c8	J1_b8	J1_a8
9	J1_e9	J1_d9	J1_c9	J1_b9	J1_a9
10	J1_e10	J1_d10	J1_c10	J1_b10	J1_a10
11	J1_e11	J1_d11	J1_c11	J1_b11	J1_a11
12	J1_e12	J1_d12	J1_c12	J1_b12	J1_a12
13	J1_e13	J1_d13	J1_c13	J1_b13	J1_a13
14	J1_e14	J1_d14	J1_c14	J1_b14	J1_a14
15	J1_e15	J1_d15	J1_c15	J1_b15	J1_a15
16	J1_e16	J1_d16	J1_c16	J1_b16	J1_a16
17	J1_e17	J1_d17	J1_c17	J1_b17	J1_a17
18	J1_e18	J1_d18	J1_c18	J1_b18	J1_a18
19	J1_e19	J1_d19	J1_c19	J1_b19	J1_a19
20	J1_e20	J1_d20	J1_c20	J1_b20	J1_a20
21	J1_e21	J1_d21	J1_c21	J1_b21	J1_a21
22	J1_e22	J1_d22	J1_c22	J1_b22	J1_a22
23	J1_e23	J1_d23	J1_c23	J1_b23	J1_a23
24	J1_e24	J1_d24	J1_c24	J1_b24	J1_a24
25	J1_e25	J1_d25	J1_c25	J1_b25	J1_a25
26	J1_e26	J1_d26	J1_c26	J1_b26	J1_a26
27	J1_e27	J1_d27	J1_c27	J1_b27	J1_a27
28	J1_e28	J1_d28	J1_c28	J1_b28	J1_a28
29	J1_e29	J1_d29	J1_c29	J1_b29	J1_a29
30	J1_e30	J1_d30	J1_c30	J1_b30	J1_a30
31	J1_e31	J1_d31	J1_c31	J1_b31	J1_a31
32	J1_e32	J1_d32	J1_c32	J1_b32	J1_a32

J2							
Connect to Pin Matrix Test Kit - J2 Connector							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	J1_e1	21	J1_e21	40	J1_d1	60	J1_d21
2	J1_e2	22	J1_e22	41	J1_d2	61	J1_d22
3	J1_e3	23	J1_e23	42	J1_d3	62	J1_d23
4	J1_e4	24	J1_e24	43	J1_d4	63	J1_d24
5	J1_e5	25	J1_e25	44	J1_d5	64	J1_d25
6	J1_e6	26	J1_e26	45	J1_d6	65	J1_d26
7	J1_e7	27	J1_e27	46	J1_d7	66	J1_d27
8	J1_e8	28	J1_e28	47	J1_d8	67	J1_d28
9	J1_e9	29	J1_e29	48	J1_d9	68	J1_d29
10	J1_e10	30	J1_e30	49	J1_d10	69	J1_d30
11	J1_e11	31	J1_e31	50	J1_d11	70	J1_d31
12	J1_e12	32	J1_e32	51	J1_d12	71	J1_d32
13	J1_e13	33	J1_c1	52	J1_d13	72	J1_c6
14	J1_e14	34	J1_c2	53	J1_d14	73	J1_c7
15	J1_e15	35	J1_c3	54	J1_d15	74	J1_c8
16	J1_e16	36	J1_c4	55	J1_d16	75	J1_c9
17	J1_e17	37	J1_c5	56	J1_d17	76	J1_c10
18	J1_e18	38	N/C	57	J1_d18	77	N/C
19	J1_e19	39	N/C	58	J1_d19	78	N/C
20	J1_e20			59	J1_d20		

J3							
Connect to Pin Matrix Test Kit - J2 Connector							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	J1_a1	21	J1_a21	40	J1_b1	60	J1_b21
2	J1_a2	22	J1_a22	41	J1_b2	61	J1_b22
3	J1_a3	23	J1_a23	42	J1_b3	62	J1_b23
4	J1_a4	24	J1_a24	43	J1_b4	63	J1_b24
5	J1_a5	25	J1_a25	44	J1_b5	64	J1_b25
6	J1_a6	26	J1_a26	45	J1_b6	65	J1_b26
7	J1_a7	27	J1_a27	46	J1_b7	66	J1_b27
8	J1_a8	28	J1_a28	47	J1_b8	67	J1_b28
9	J1_a9	29	J1_a29	48	J1_b9	68	J1_b29
10	J1_a10	30	J1_a30	49	J1_b10	69	J1_b30
11	J1_a11	31	J1_a31	50	J1_b11	70	J1_b31
12	J1_a12	32	J1_a32	51	J1_b12	71	J1_b32
13	J1_a13	33	J1_c23	52	J1_b13	72	J1_c28
14	J1_a14	34	J1_c24	53	J1_b14	73	J1_c29
15	J1_a15	35	J1_c25	54	J1_b15	74	J1_c30
16	J1_a16	36	J1_c26	55	J1_b16	75	J1_c31
17	J1_a17	37	J1_c27	56	J1_b17	76	J1_c32
18	J1_a18	38	N/C	57	J1_b18	77	N/C
19	J1_a19	39	N/C	58	J1_b19	78	N/C
20	J1_a20			59	J1_b20		

J2							
Connect to Pin Matrix Test Kit - J2 Connector							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	J1_e1	21	J1_e21	40	J1_d1	60	J1_d21
2	J1_e2	22	J1_e22	41	J1_d2	61	J1_d22
3	J1_e3	23	J1_e23	42	J1_d3	62	J1_d23
4	J1_e4	24	J1_e24	43	J1_d4	63	J1_d24
5	J1_e5	25	J1_e25	44	J1_d5	64	J1_d25
6	J1_e6	26	J1_e26	45	J1_d6	65	J1_d26
7	J1_e7	27	J1_e27	46	J1_d7	66	J1_d27
8	J1_e8	28	J1_e28	47	J1_d8	67	J1_d28
9	J1_e9	29	J1_e29	48	J1_d9	68	J1_d29
10	J1_e10	30	J1_e30	49	J1_d10	69	J1_d30
11	J1_e11	31	J1_e31	50	J1_d11	70	J1_d31
12	J1_e12	32	J1_e32	51	J1_d12	71	J1_d32
13	J1_e13	33	J1_c1	52	J1_d13	72	J1_c6
14	J1_e14	34	J1_c2	53	J1_d14	73	J1_c7
15	J1_e15	35	J1_c3	54	J1_d15	74	J1_c8
16	J1_e16	36	J1_c4	55	J1_d16	75	J1_c9
17	J1_e17	37	J1_c5	56	J1_d17	76	J1_c10
18	J1_e18	38	N/C	57	J1_d18	77	N/C
19	J1_e19	39	N/C	58	J1_d19	78	N/C
20	J1_e20			59	J1_d20		

J3							
Connect to Pin Matrix Test Kit - J2 Connector							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	J1_a1	21	J1_a21	40	J1_b1	60	J1_b21
2	J1_a2	22	J1_a22	41	J1_b2	61	J1_b22
3	J1_a3	23	J1_a23	42	J1_b3	62	J1_b23
4	J1_a4	24	J1_a24	43	J1_b4	63	J1_b24
5	J1_a5	25	J1_a25	44	J1_b5	64	J1_b25
6	J1_a6	26	J1_a26	45	J1_b6	65	J1_b26
7	J1_a7	27	J1_a27	46	J1_b7	66	J1_b27
8	J1_a8	28	J1_a28	47	J1_b8	67	J1_b28
9	J1_a9	29	J1_a29	48	J1_b9	68	J1_b29
10	J1_a10	30	J1_a30	49	J1_b10	69	J1_b30
11	J1_a11	31	J1_a31	50	J1_b11	70	J1_b31
12	J1_a12	32	J1_a32	51	J1_b12	71	J1_b32
13	J1_a13	33	J1_c23	52	J1_b13	72	J1_c28
14	J1_a14	34	J1_c24	53	J1_b14	73	J1_c29
15	J1_a15	35	J1_c25	54	J1_b15	74	J1_c30
16	J1_a16	36	J1_c26	55	J1_b16	75	J1_c31
17	J1_a17	37	J1_c27	56	J1_b17	76	J1_c32
18	J1_a18	38	N/C	57	J1_b18	77	N/C
19	J1_a19	39	N/C	58	J1_b19	78	N/C
20	J1_a20			59	J1_b20		

J4							
Connect to Pin Matrix Test Kit - J2 Connector							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	J1_c11	21	J1_d4	40	N/C	60	N/C
2	J1_c12	22	J1_c1	41	N/C	61	N/C
3	J1_c13	23	J1_a1	42	Jumper	62	N/C
4	J1_c14	24	J1_a2	43		63	N/C
5	J1_c15	25	J1_a3	44	N/C	64	N/C
6	J1_c16	26	J1_a4	45	N/C	65	N/C
7	J1_c17	27	J1_a5	46	N/C	66	N/C
8	J1_c18	28	J1_b1	47	N/C	67	N/C
9	J1_c19	29	J1_b2	48	Jumper	68	N/C
10	J1_c20	30	J1_b3	49		69	N/C
11	J1_c21	31	J1_b4	50	N/C	70	N/C
12	J1_c22	32	J1_c32	51	N/C	71	N/C
13	J1_e1	33	N/C	52	N/C	72	N/C
14	J1_e2	34	N/C	53	N/C	73	N/C
15	J1_e3	35	N/C	54	N/C	74	N/C
16	J1_e4	36	N/C	55	N/C	75	N/C
17	J1_e5	37	N/C	56	N/C	76	N/C
18	J1_d1	38	N/C	57	N/C	77	N/C
19	J1_d2	39	N/C	58	N/C	78	N/C
20	J1_d3			59	N/C		

J5							
Connect to SLU Utility							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	N/C	21	N/C	40	N/C	60	N/C
2	N/C	22	N/C	41	N/C	61	N/C
3	N/C	23	N/C	42	N/C	62	N/C
4	N/C	24	N/C	43	N/C	63	N/C
5	N/C	25	N/C	44	N/C	64	N/C
6	N/C	26	N/C	45	N/C	65	N/C
7	N/C	27	N/C	46	N/C	66	N/C
8	N/C	28	N/C	47	N/C	67	N/C
9	N/C	29	N/C	48	N/C	68	N/C
10	N/C	30	N/C	49	N/C	69	N/C
11	N/C	31	N/C	50	N/C	70	N/C
12	N/C	32	N/C	51	N/C	71	N/C
13	N/C	33	N/C	52	N/C	72	N/C
14	N/C	34	N/C	53	N/C	73	N/C
15	N/C	35	N/C	54	N/C	74	N/C
16	J1_c12	36	J1_c18	55	N/C	75	N/C
17	J1_c1	37	J1_c32	56	N/C	76	N/C
18	N/C	38	N/C	57	N/C	77	N/C
19	N/C	39	N/C	58	N/C	78	N/C
20	N/C			59	N/C		

U8989-61624 Heavy Duty Load Card Cable

Figure 5-13 U8989-61624 Heavy Duty Load Card Cable

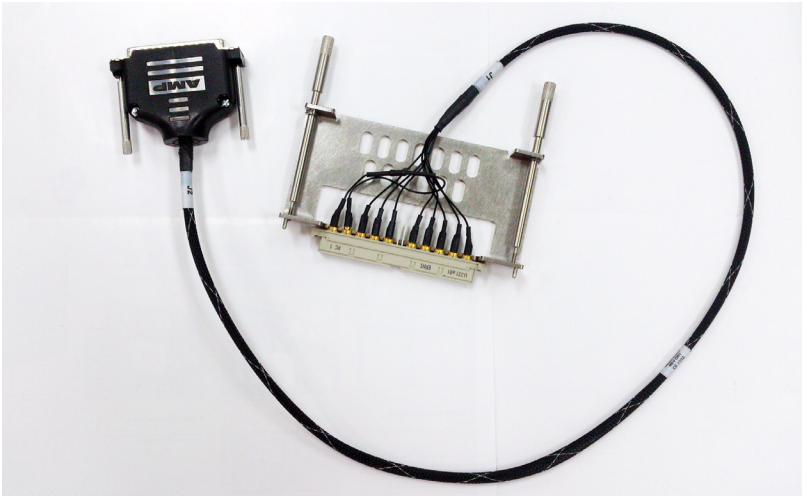


Figure 5-14 U8989-61624 Heavy Duty Load Card Cable Schematic

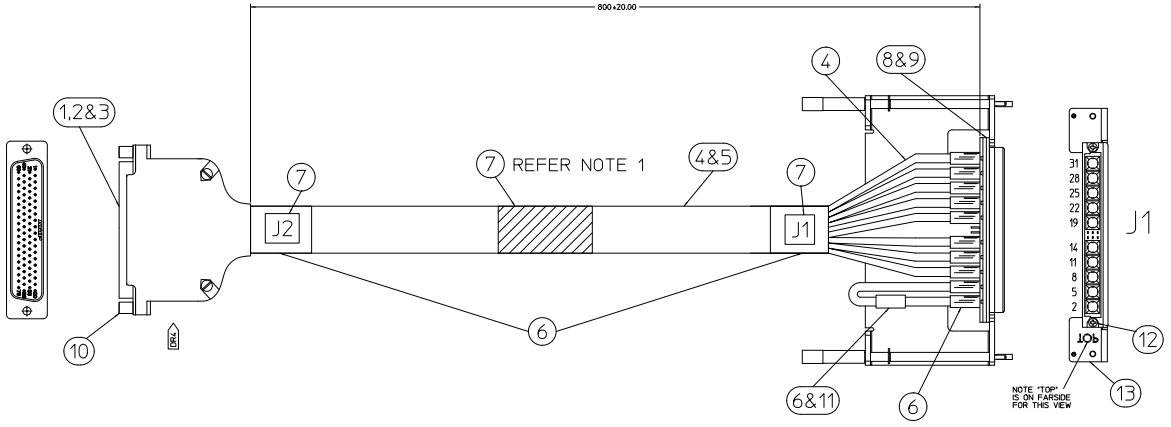


Table 5-7 U8989-61624 Cable Pinout

J1		
Connect to Heavy Duty Load Card		
Row	b	a
2	J1_b2	Add 100 Ohm R
5	J1_b5	Jump to J1_b2
8	J1_b8	
11	J1_b11	
14	J1_b14	
19	J1_b19	
22	J1_b22	
25	J1_b25	
28	J1_b28	
31	J1_b31	

J2							
Connect to Pin Matrix Test Kit - J2 Connector							
Pin	Connect to	Pin	Connect to	Pin	Connect to	Pin	Connect to
1	J1_b8	21	N/C	40	N/C	60	N/C
2	J1_b11	22	N/C	41	N/C	61	N/C
3	J1_b14	23	N/C	42	N/C	62	N/C
4	J1_b19	24	N/C	43	N/C	63	N/C
5	J1_b22	25	N/C	44	N/C	64	N/C
6	J1_b25	26	N/C	45	N/C	65	N/C
7	J1_b28	27	N/C	46	N/C	66	N/C
8	J1_b31	28	N/C	47	N/C	67	N/C
9	N/C	29	N/C	48	N/C	68	N/C
10	N/C	30	N/C	49	N/C	69	N/C
11	N/C	31	N/C	50	N/C	70	N/C
12	N/C	32	N/C	51	N/C	71	N/C
13	N/C	33	N/C	52	N/C	72	N/C
14	N/C	34	N/C	53	N/C	73	N/C
15	N/C	35	N/C	54	N/C	74	N/C
16	N/C	36	N/C	55	N/C	75	N/C
17	N/C	37	N/C	56	N/C	76	N/C
18	N/C	38	N/C	57	N/C	77	N/C
19	N/C	39	N/C	58	N/C	78	N/C
20	N/C			59	N/C		

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