Keysight W3630-Series DDR3 DRAM BGA Probes

Installation Guide

KEYSIGHT TECHNOLOGIES

Notices

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Contents

Keysight W3630-Series DDR3 DRAM BGA Probes

Installation Guide

1 Introduction

Updated versions of this manual may be available. Go to www.keysight.com and search for W3631A.
This document provides installation information for the following Keysight products:

- W3631A DDR3 x16 BGA address/control/data probe
- W3633A DDR3 x4/x8 BGA address/control/data probe
- W3636A DDR3 x16 non-stacked DRAM96 ball BGA probe
- E5845A adapter cable for W3631A and W3636A probes
- E5847A adapter cable for W3633A probe
- W3635B DDR3 oscilloscope probe adapter

KEYSIGHT TECHNOLOGIES

DDR3 DRAM BGA Probe Description

The DDR3 DRAM BGA probes enable logic analyzer state and timing measurements of DRAM buses, including the DQ, DQS, and clock signals of x4, x8 and x16 DRAMs using the JEDEC standard common DDR3 DRAM footprints.

The probe interposes between the DRAM being probed and the PC board where the DRAM would normally be soldered. The probe is designed to be soldered to the PCB footprint for the DRAM The DRAM being probed is then soldered to the top side of the probe.

Each DRAM signal in the common footprint (including those defined for x4, x8 and x16 DRAMs) passes directly from the bottom side of the probe to the top side of the probe. Buried probe resistors placed at the DRAM balls connect the probed signals to the rigid flex to mate with an Keysight cable adapter (ZIF probe).

Oscilloscope Probing

The W3630-series probes, when used with the W3635B adapter, are also compatible with the Keysight InfiniiMax oscilloscope probes. This allows scope probing of the DRAM signals with an Infiniium 9000- or 90000-Series oscilloscope, giving you a DDR3 testing solution covering the clock characterization, electrical and timing parameters of the JEDEC specification.

Fixture Technical Feature Summary

- Probing of DDR3 x4, x8 and x16 DRAMs in BGA packages using one of the JEDEC standard common BGA footprints.
- Logic analyzer (using E5845A/47A single ended ZIF probe) and oscilloscope (W3635B adapter and InfiniiMax socketed probe head) connection to RAS, CAS, WE, DQ, DQS, DQS#, and CK/CK# signals.
- Differential CLK signal.
- Interposer design probes signals between DRAM BGA balls and DIMM.
- Use of separate single ended probes for connection to the logic analyzer optimizes use of analyzer channels by allowing assignment of analyzer channels to 8 or 16 bits on each DRAM.
- Gold plating of the DRAM footprint on the top side of the probe is compatible with leaded and no-lead DRAM balls.

Equipment Required

You will need:

- Keysight U4154A, 16900-series, or 16850-series logic analysis system.
- Keysight B4621B DDR2/3 decoder software.
- (optional) Keysight B4622B DDR2/3 protocol compliance and analysis tool.
- An appropriate number of Keysight U4154A, 16850B, 16960A, or 16962A logic analyzer cards connected together as a module.
- One or more W3630-series BGA probes
- One or more E5840-series adapter cables
- (optional) One or more W3635B oscilloscope adapters and E2678A socketed probe heads for use with the 90000A series oscilloscopes and one of the following licenses:
  - N5465A-001 InfiniiSim Waveform Transformation Toolset Basic license for use with W3635B transfer function file (.tf2)

    or:
  - N5465A-002 InfiniiSim Waveform Transformation Toolset Advanced license for use with S parameter files for W3631/3A BGA probes and W3635B scope adapter.
- (optional) MSO 9000A Series oscilloscope with E5383A single-ended flying leads with 40 pin cable connector for use with W3635B oscilloscope adapter board.

Mechanical Considerations

Probe Dimensions and Keep Out Volume

The following 8s show the KOV of the Keysight logic analyzer cable adapters when connected to the BGA probe.

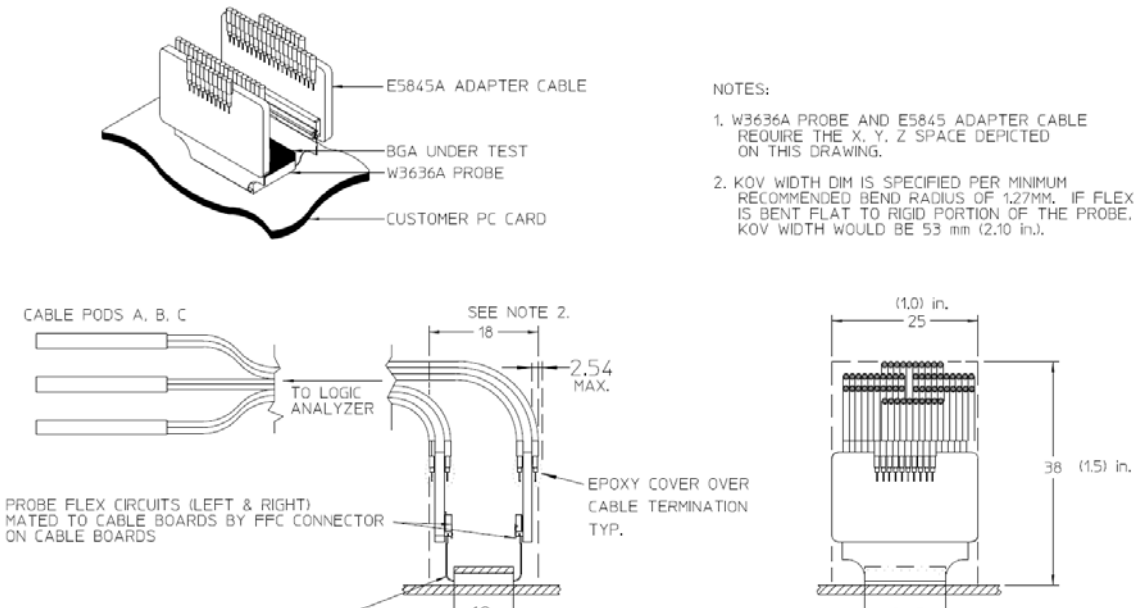


Figure 1 Keep Out Volume for W3631A with E5845A (same as W2631B with E5384A)

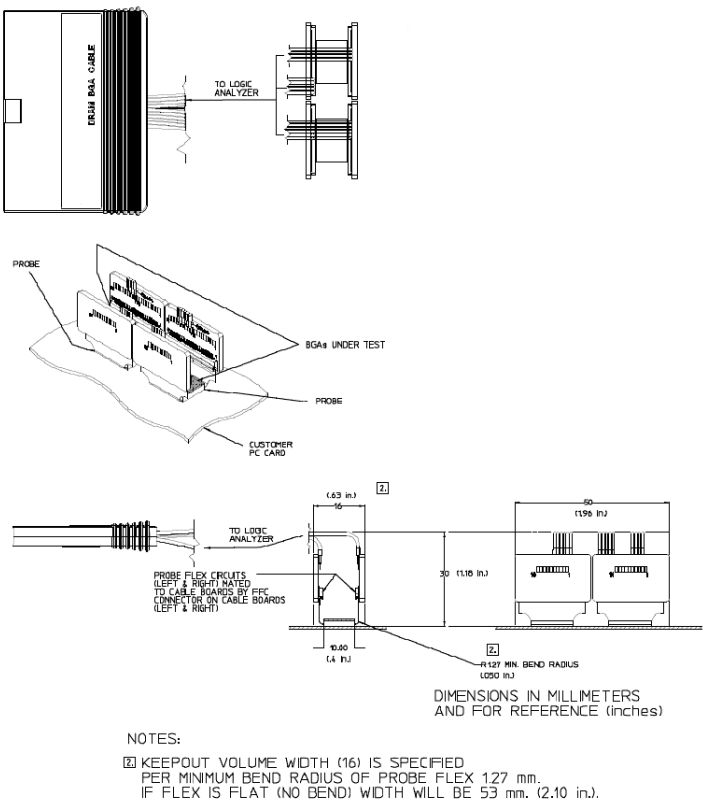


Figure 2 KOV of W3633A with E5847A, (same as W2633B, W2634A and E5827A)

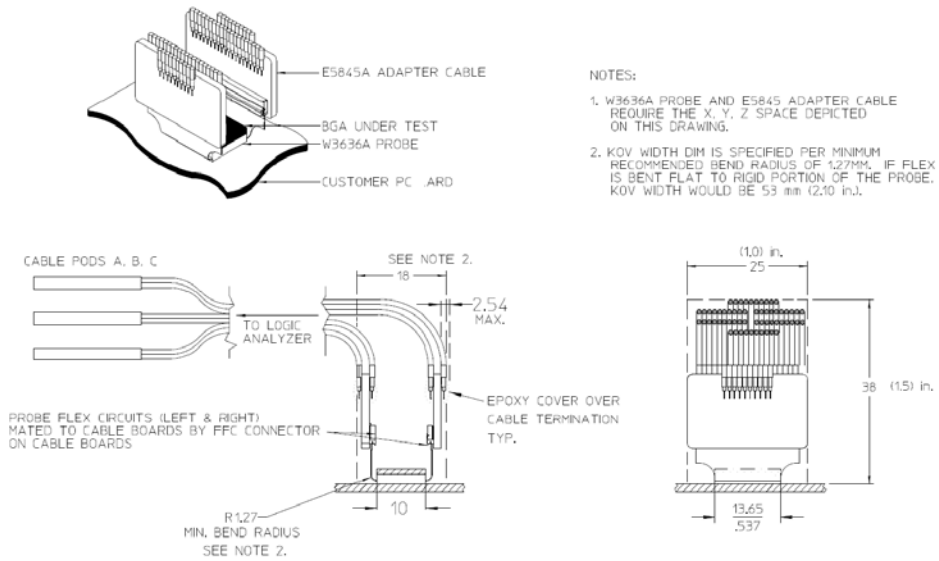


Figure 3 KOV of W3636A with E5845A

The following figures show the dimensions of the BGA probes.

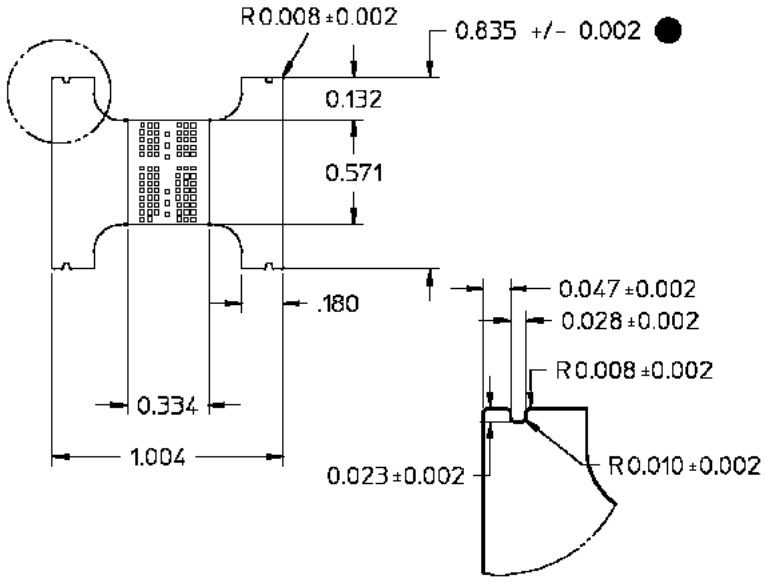


Figure 4 W3631A probe dimensions

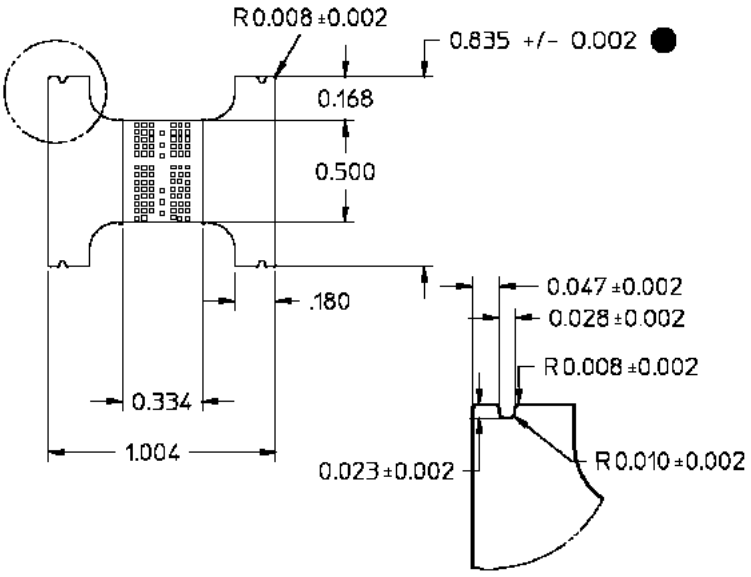


Figure 5 W3633A probe dimensions

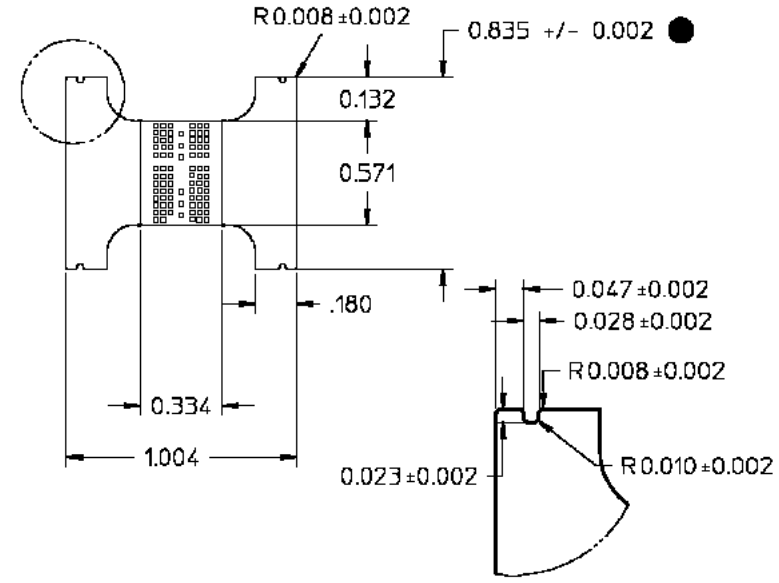


Figure 6 W3636A probe dimensions

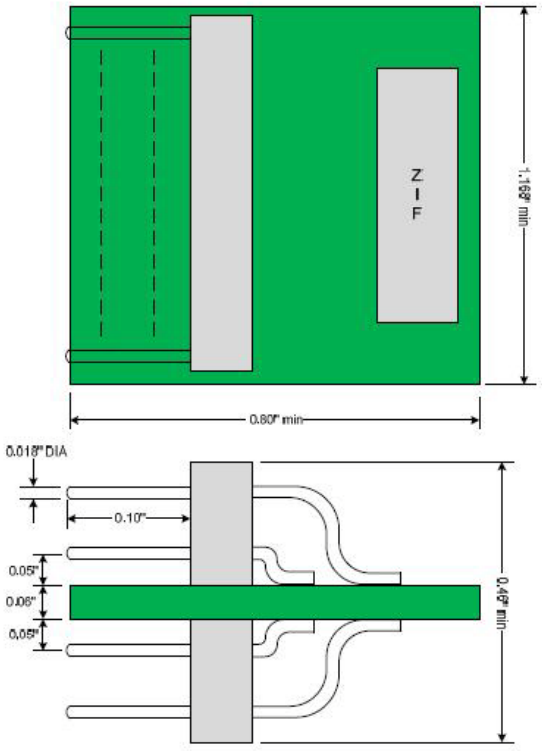


Figure 7 W3635B Probe Adapter Dimensions

Board and Wings Thickness

- Board thickness - 0.072 inches (+/-10% for maximum variation)
- Thickness above the wing (Layer 1-4) - 0.0298
- Thickness below the wing (Layer 7-9) - 0.0192

DDR2 Probes

Keysight offers equivalent probes for DDR2 memory:

- W2631B DDR2 x16 command and data probe
- W2632A DDR2 x16 BGA data probe
- W2633B DDR2 x8 BGA command and data probe
- W2634A DDR2 x8 BGA data probe
- E5384A adapter cable adapter for 8x16 DRAM BGA
- E5826A adapter cable for 2x16 DRAM BGA
- E5827A adapter cable for 2x8 DRAM BGA

The probes can be distinguished by the color of the printed circuit board: DDR2 probes are green and DDR3 probes are red.

2 Installing the Probe

Soldering the Probe

The BGA probes need to be attached to the DRAM PCB footprint on the design to be probed, and the desired DRAM is soldered to the top side of the probe. This attachment may occur in any order (i.e. first solder the probe to the DUT, and then solder the DRAM to the probe, or first solder the DRAM to the probe, and then solder the DRAM+probe assembly to the DUT). The probe is designed to tolerate lead-free soldering temperature profiles. However, it is always recommended to apply the minimum temperature required and the minimum number of heating/cooling cycles to reduce risk of any damage to the probe.

The probe is supplied without solder balls. Depending on the exact attachment order, either leaded or lead-free solder may be preferred to attach the probe to the DUT. The design of the probe supports either choice.

The flexible “wings” on the probe may need to be bent upwards before soldering to avoid mechanical contact with components adjacent to the probe on the DUT. This will also ensure reliable connection when connect to the logic analyzer cable adapters.

If the in-house expertise to attach the BGA probe and DRAM cannot be found, there are contract manufacturers with this expertise who may be willing to perform the attachment for a fee. More information on BGA soldering and rework techniques that may be useful in attaching the probe may be found at: "http://www.circuitrework.com/guides/9-0.shtml".

Recommended soldering guidelines:

1 Maximum temperature that the BGA probe can withstand is 260C.

2 Bake out boards and or components to eliminate moisture entrapment in the boards and components. Normally back for 24 hours at 125C or to the component or board specification.

Connecting to the Logic Analyzer

CAUTION **Use ESD precautions.** Electrostatic discharge can damage components on your board or in the probes. Use a grounded wrist strap and other ESD control measures as appropriate.

The adapter cables (sometimes called probes) are used with the BGA probes to connect the probe to the logic analyzer. The adapter cables plug into the 90-pin logic analyzer pod cable.

NOTE Please ensure that the wings on the BGA probe are properly latched to the ZIF connectors on the adapter cables. The ZIF connectors can withstand up to 50 cycles of insertions. Please handle the probe with care.

Table 1 Logic Analyzer Channel Mapping for the E5845A Probe Cable (when used with the W3636A probe)

Data Pod / Pod A		Control Pod / Pod B		Address Pod / Pod C	
LA Channel	Signal Name	LA Channel	Signal Name	LA Channel	Signal Name
0	DQL0	0	BA1	0	-
1	DQL1	1	A10/AP	1	A14
2	DQL2	2	DML	2	A13
3	DQL3	3	-	3	A12/BC#
4	DQL4	4	RESET#	4	A11
5	DQL5	5	BA0	5	A15
6	DQL6	6	BA2	6	A9
7	DQL7	7	WE#	7	A8
8	DQU0	8	CS0#	8	A7
9	DQU1	9	CAS#	9	A6
10	DQU2	10	ODT0	10	A5
11	DQU3	11	RAS#	11	A4
12	DQU4	12	DQSL	12	A3
13	DQU5	13	-	13	A2
14	DQU6	14	-	14	A1
15	DQU7	15	-	15	A0
Clock_P	DQSU	Clock_P	CK	Clock_P	CKE0
Clock_N	DQSU#	Clock_N	CK#	Clock_N	-

Table 2 Logic Analyzer Channel Mapping for the E5845A Probe Cable (when used with the W3631A probe)

Data Pod / Pod A		Control Pod / Pod B		Address Pod / Pod C	
LA Channel	Signal Name	LA Channel	Signal Name	LA Channel	Signal Name
0	DQL0	0	BA1	0	-
1	DQL1	1	A10/AP	1	A14
2	DQL2	2	DML	2	A13
3	DQL3	3	-	3	A12/BC#
4	DQL4	4	RESET#	4	A11
5	DQL5	5	BA0	5	A15
6	DQL6	6	BA2	6	A9
7	DQL7	7	WE#	7	A8
8	DQU0	8	CS0#	8	A7
9	DQU1	9	CAS#	9	A6
10	DQU2	10	ODT0	10	A5
11	DQU3	11	RAS#	11	A4
12	DQU4	12	DQSL	12	A3
13	DQU5	13	-	13	A2
14	DQU6	14	-	14	A1
15	DQU7	15	-	15	A0
Clock_P	DQSU	Clock_P	CK	Clock_P	CKE0
Clock_N	DQSU#	Clock_N	CK#	Clock_N	-

Table 3 Logic Analyzer Channel Mapping for the E5847A Probe Cable (when used with the W3633A probe)

Data Pod / Pod A		Control Pod / Pod B		Address Pod / Pod C	
LA Channel	Signal Name	LA Channel	Signal Name	LA Channel	Signal Name
0	DQ0	0	BA1	0	A15
1	DQ1	1	-	1	A14
2	DQ2	2	CKE1	2	A13
3	DQ3	3	-	3	A12/BC#
4	DQ4	4	RESET#	4	A11
5	DQ5	5	BA0	5	A10/AP
6	DQ6	6	BA2	6	A9
7	DQ7	7	CS1#	7	A8
8	DM	8	CS0#	8	A7
9	-	9	WE#	9	A6
10	-	10	ODT0	10	A5
11	-	11	CAS#	11	A4
12	-	12	ODT1	12	A3
13	-	13	RAS#	13	A2
14	-	14	-	14	A1
15	-	15	-	15	A0
Clock_P	DQS	Clock_P	CK	Clock_P	CKE0
Clock_N	DQS#	Clock_N	CK#	Clock_N	-

Table 4 Signals not probed by the logic analyzer

Probe	Signal Name
W3633A	CS2#
	CS3#
	VREFCA
	VREFDQ
	ZQ3..ZQ0

Probe	Signal Name
W3631A	BA2
	A15
	CS2#
	CS3#
	VREFCA
	VREFDQ
	ZQ3, ZQ2, ZQ1, ZQ0
	DMU
	DQSL, DQSL#
W3636A	
	VDD
	VDDQ
	CKE1
	CS1#, CS2#, CS3#
	ODT1
	VREFCA, VREFDQ
	ZQ3, ZQ2, ZQ1, ZQ0
	DQSL#
	DMU

NOTE

Refer to page 33 for a list of signals for each probe that are accessible to a probe with an oscilloscope via provided test points.

For multi DR3 x16 stacked (DDP) DRAM 2G or deeper, a combination of W3631A and W3636A interposer probes may be used to gain access to all CMD/ADD signals on the DDR3 channel.

Scope Connection to the W3630 Series Probe

The DDR3 BGA probes may be used with the E2678A socketed probe head.

Most signals may be probed using the W3635B oscilloscope probe adapter, which has a ZIF connector for attachment to the BGA probes.

A few additional signals may be probed by soldering the scope probe directly to a test point on the BGA probe.

The solder-in probe makes a 2 GHz bandwidth connection with the test point on the adapter or BGA probe.

Using the W3631A, W3633A, or W3636A BGA Probe and W3635B Oscilloscope Adapter with InfiniiSim

Before you begin this procedure, download the .zip file containing the transfer function file and the S-parameter file from the Keysight web site at:

http://www.keysight.com/find/w3631a-w3635b-files

Step 1: For use with this W3631/3A and W3635B configuration, connect the E2678A socketed probe head to the pin header on the W3635B.

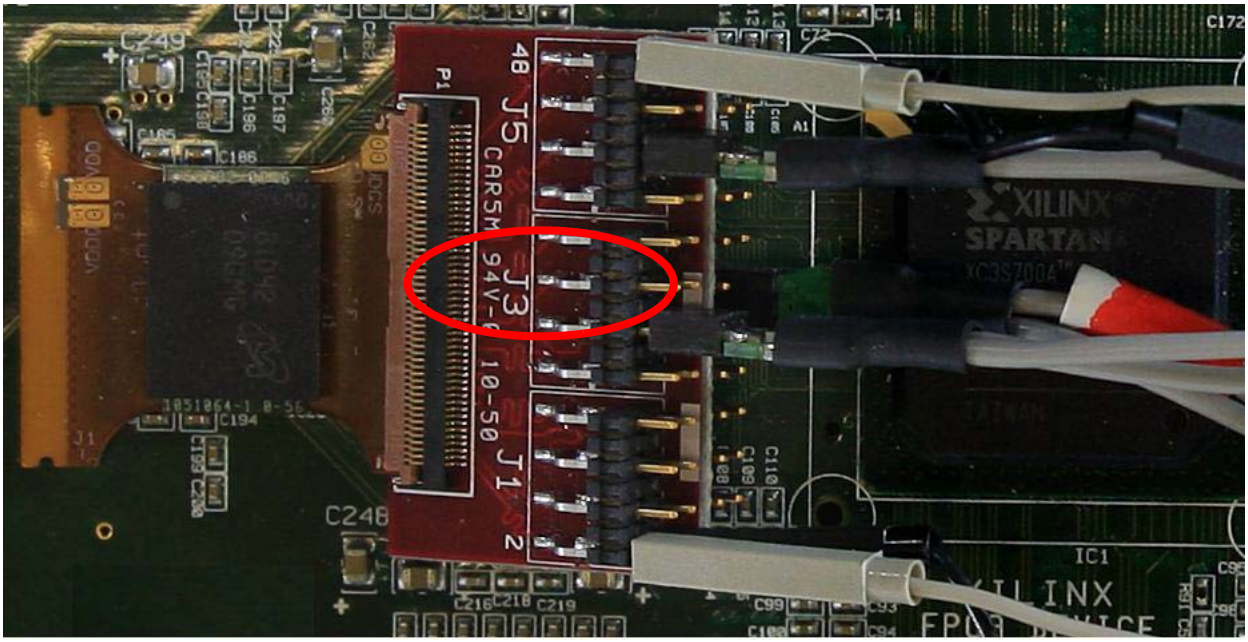
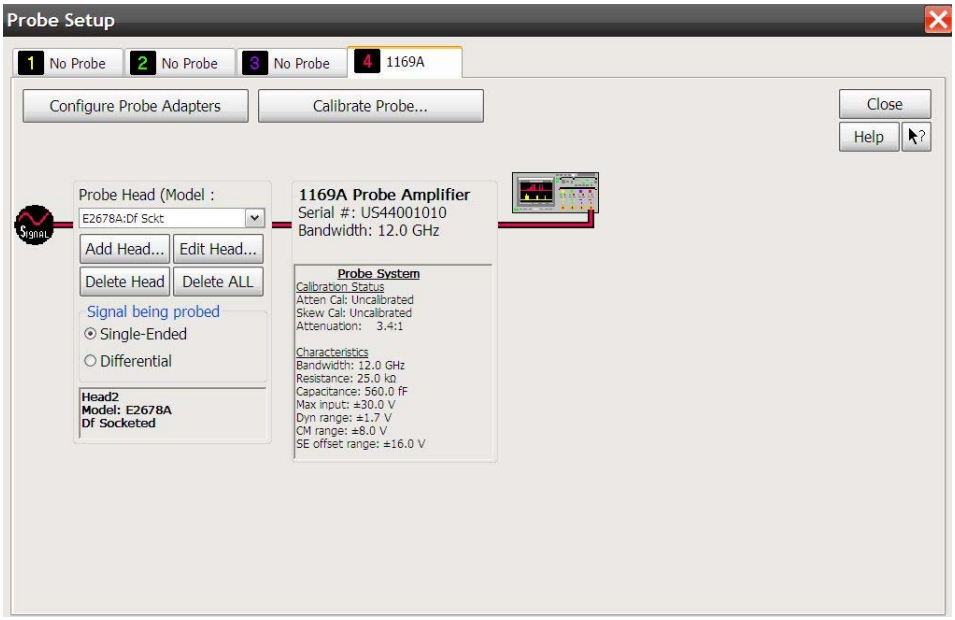


Figure 8 E2678A socketed probe head connected to the W3635B adapter board to provide connection to the oscilloscope

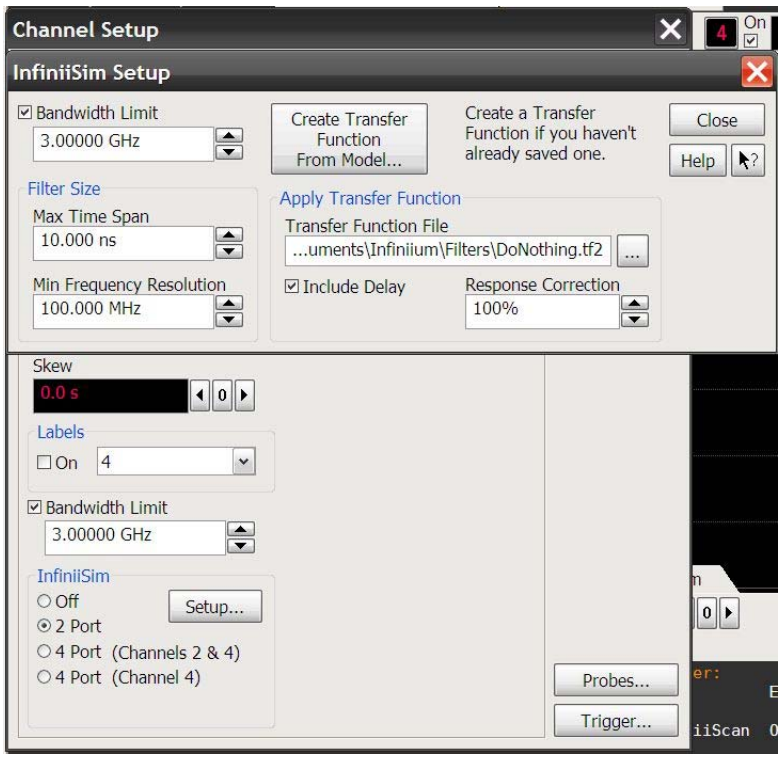
Connect the probe amp to the desired channel, and then select the E2678A probe head and whether the signal being probe is single-ended or differential:



Step 2: Apply W3635B transfer function file

This step requires N5465-001 InfiniiSim Waveform Transformation Toolset Basic license.

Go to the channel menu and turn InfiniiSim on to 2 Port. Set the BW limit appropriately; 3 GHz should be enough for these DDR 3 applications with ~ 150 pS 20-80% transition times.



Under Apply Transfer Function menu, navigate to the location of W3635B.tf2 file and click Close.

OR

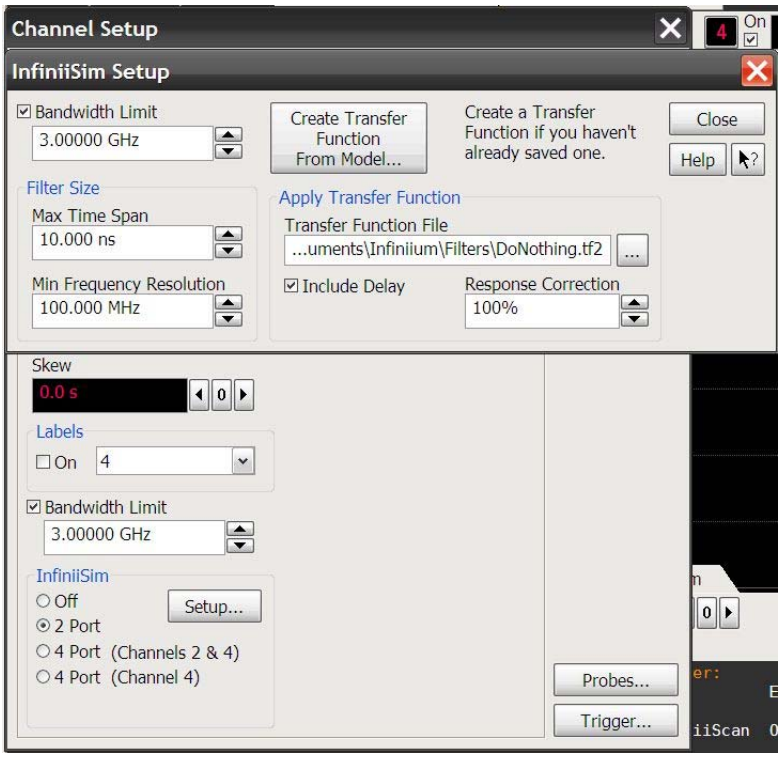
Step 2: **Build a transfer function file with S parameter files of W3631/3A BGA probe with W3635B scope adapter and E2678A socketed probe head**

This step requires N5465A-002 InfiniiSim Waveform Transformation Toolset Advanced license.

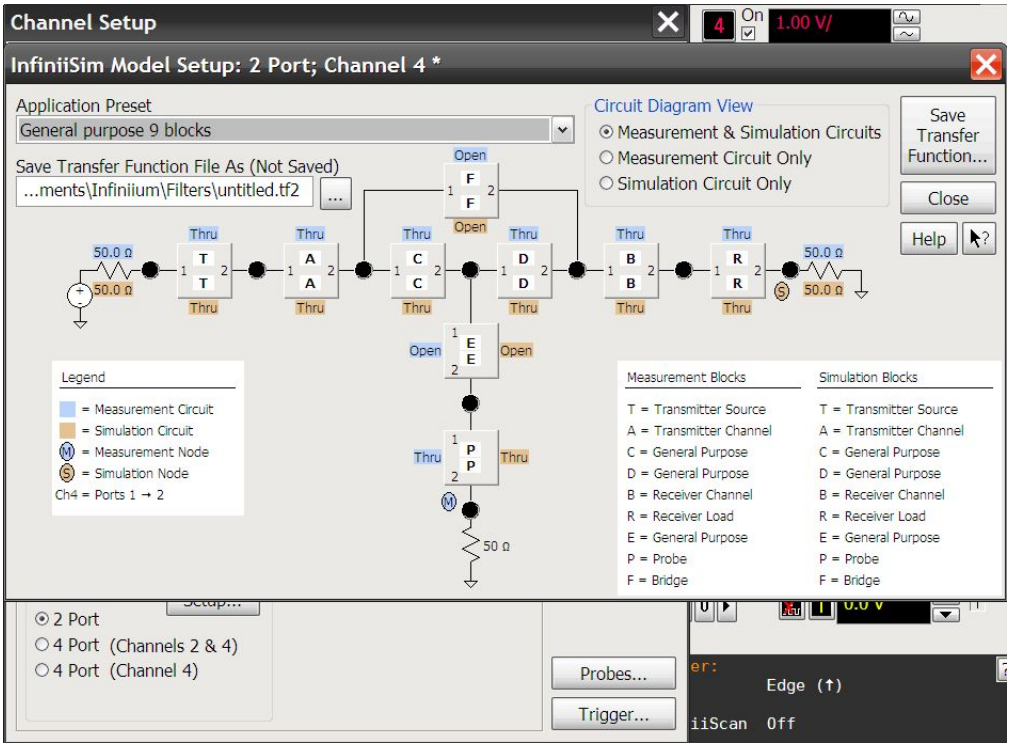
Go to the channel menu and turn InfiniiSim on to 2 Port. Set the BW limit appropriately; 3 GHz should be enough for these DDR 3 applications with ~ 150 pS 20-80% transition times.

Select the “Setup” button and this menu will appear.

Step 3: **Select the "Setup" button and this menu will appear**

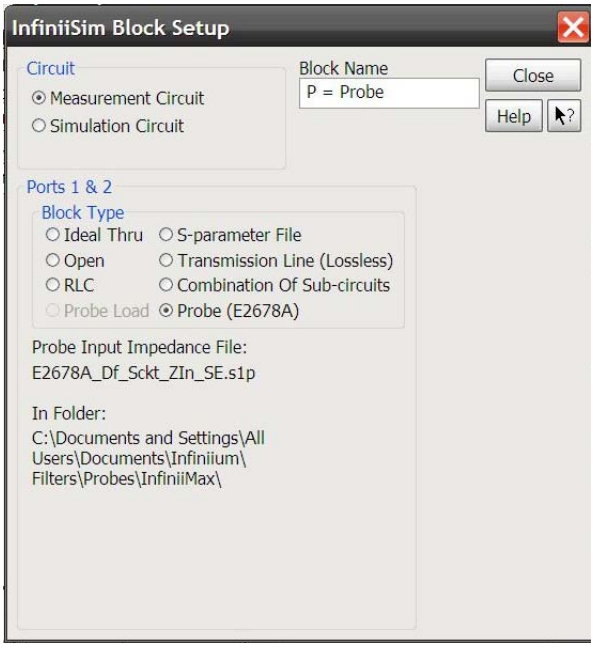


Step 4: Select the “Create Transfer Function From Model” button and then set Application Preset to “General Purpose 9 Blocks”



Step 5: Select block “P” and then set “Block Type” for E2678A

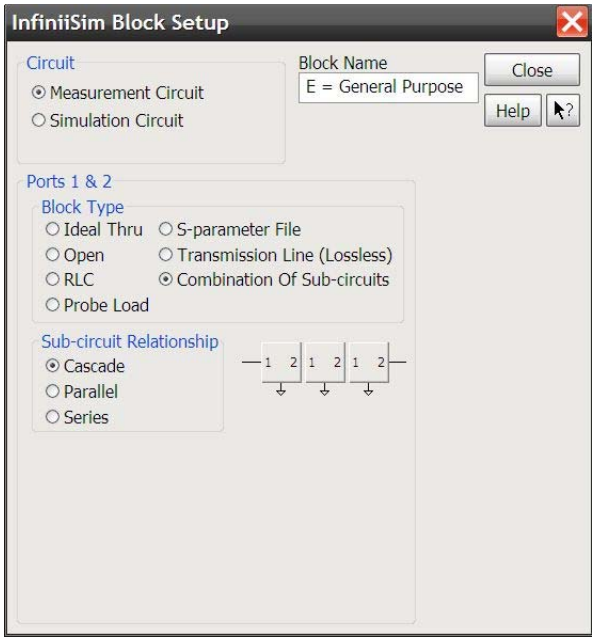
Do this for both the measurement circuit and the simulation circuit. Close this window.



Step 6: **Select block “E” and then set “Block Type” to “Combination OF Sub-circuits”**

“Sub-circuit Relationship” should be set to “Cascade”.

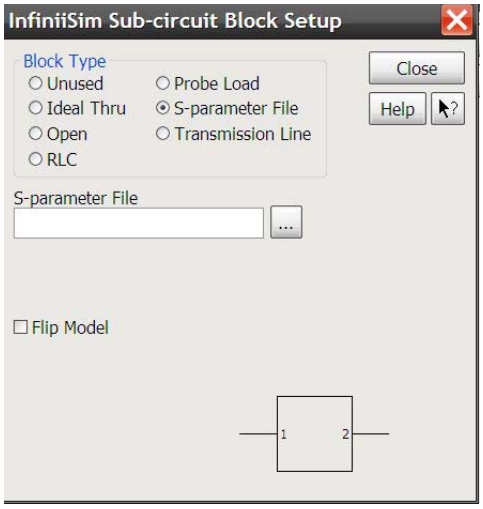
Do this for both the measurement circuit and the simulation circuit. Close this window.



Step 7: **Select the right most sub-block and set for “S-parameter file”**

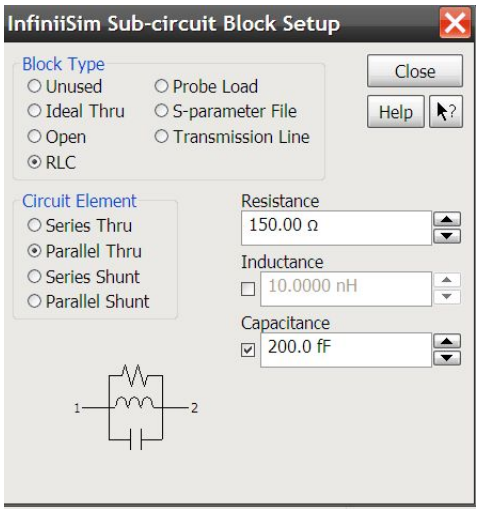
Navigate the file selector to the “W3631A_W3635B_PostResMod.s2p” file supplied in this zip package. Do this for both the measurement circuit and the simulation circuit. Close this window.

NOTE The same file W3631A_W3635B_PostResMod.s2p can be used for W3633A DDR3 x8 BGA probe.



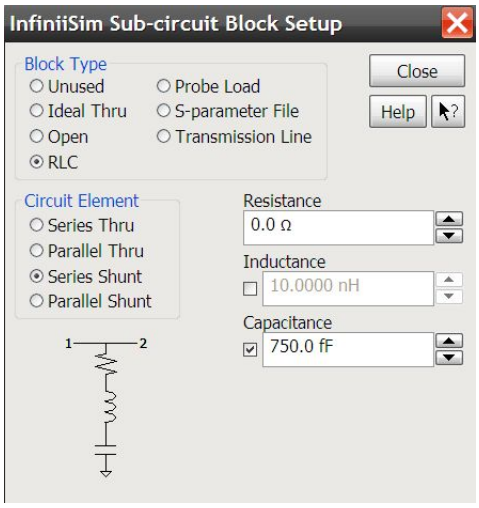
Step 8: **Select the middle sub-block and set for “RLC” block type with “Parallel Thru” circuit element**

Set the resistor to 150ohms nominal (or to the measured value for a particular W3631A) and the capacitance to 200fF. Do this for both the measurement circuit and the simulation circuit. Close this window.



Step 9: **Select the left most sub-block and set for “RLC” block type and “Series Shunt” circuit element**

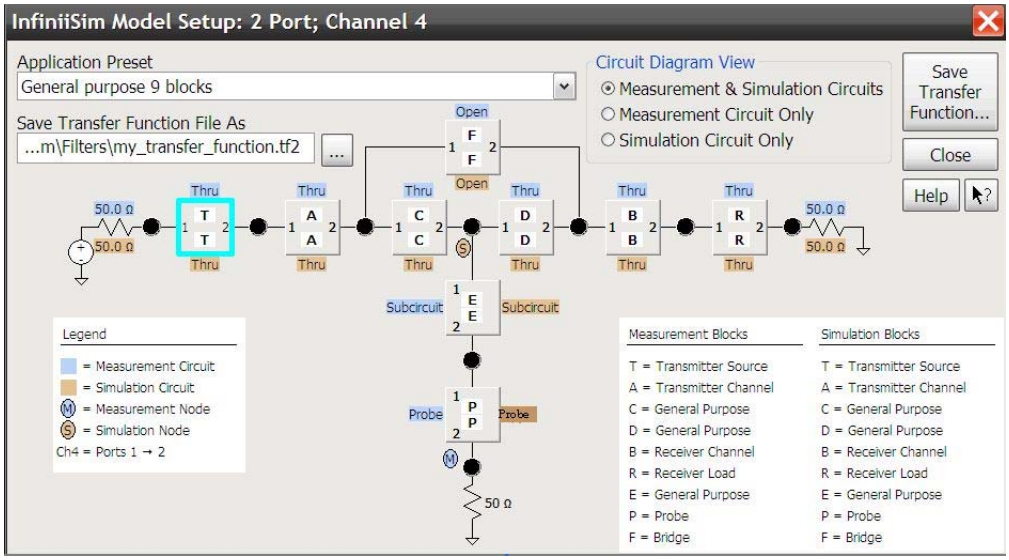
Set the resistance to zero and the capacitance to 750 fF. Do this for both the measurement circuit and the simulation circuit. Close this window.



Step 10: **Display should be back at this screen**

Things to do:

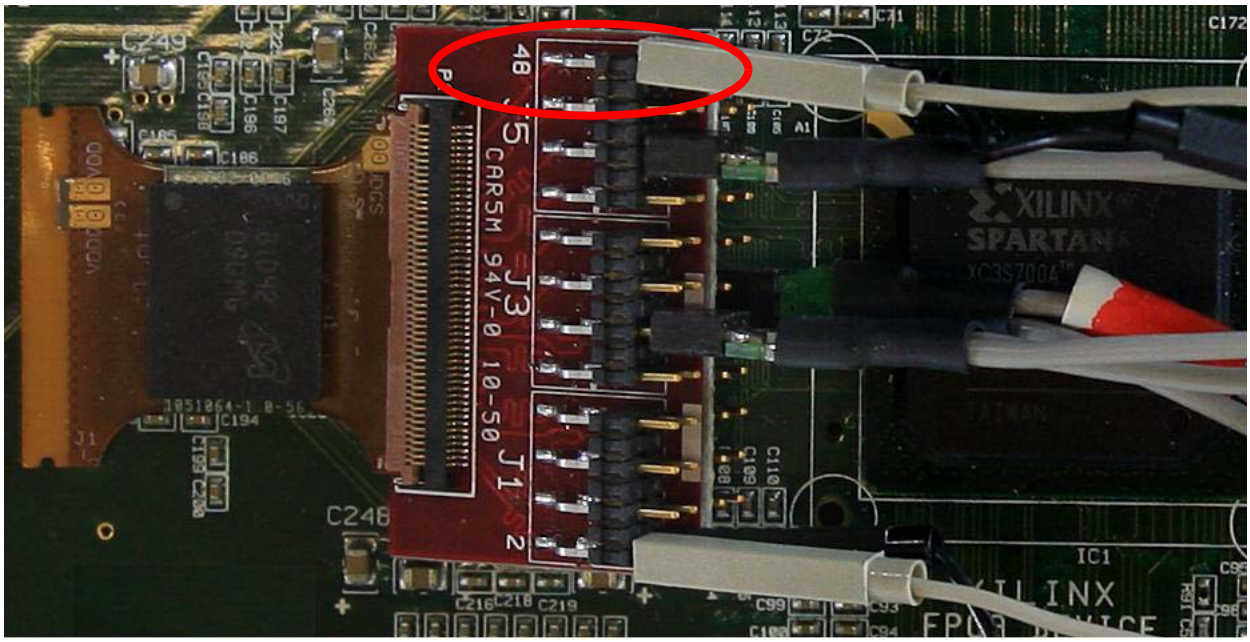
- Make sure measurement node “M” and simulation node “S” are positioned as shown.
- Enter a file name you want to store this transfer function (and setup) to. In this screen this is “my_transfer_function.tf2”. Press the “Save Transfer Function...” button. If everything is right you'll get “transfer function successfully created” message.


InfiniiSim Model Setup: 2 Port; Channel 4
Application Preset
General purpose 9 blocks
Save Transfer Function File As
...m\Filters\my_transfer_function.tf2
...
Circuit Diagram View
Measurement & Simulation Circuits
Measurement Circuit Only
Simulation Circuit Only
Save Transfer Function...
Close
Help
Open
Thru
Subcircuit
Probe
50.0 Ω
50 Ω
Legend
= Measurement Circuit
= Simulation Circuit
= Measurement Node
= Simulation Node
Ch4 = Ports 1 → 2
Measurement Blocks
T = Transmitter Source
A = Transmitter Channel
C = General Purpose
D = General Purpose
B = Receiver Channel
R = Receiver Load
E = General Purpose
P = Probe
F = Bridge
Simulation Blocks
T = Transmitter Source
A = Transmitter Channel
C = General Purpose
D = General Purpose
B = Receiver Channel
R = Receiver Load
E = General Purpose
P = Probe
F = Bridge

Using the W3631A, W3633A, or W3636A BGA Probe and W3635B Oscilloscope Adapter with 9000A Series MSO Oscilloscopes

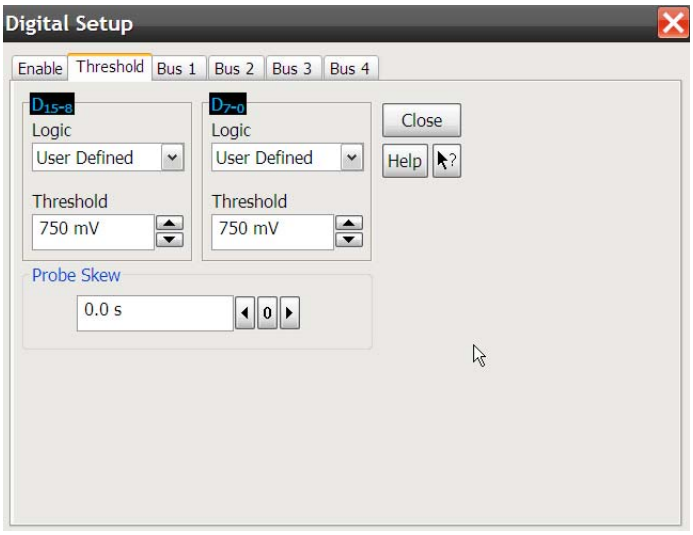
For use with this W3631/3A/6A and W3635B configuration, connect E5383A single-ended flying leads with 40-pin cable connector from the digital output of MSO oscilloscope to the pin header on the W3635B.

E5383A single-ended flying leads with 40-pin cable connector



E5383A single-ended flying leads connected to the W3635B adapter board to provide connection to the digital channels on MSO oscilloscope

On the menu for “Digital Setup”, select User Defined logic and input the threshold voltage to use DDR3 Vref 750mV.



Signals Probed By the W3635B Adapter

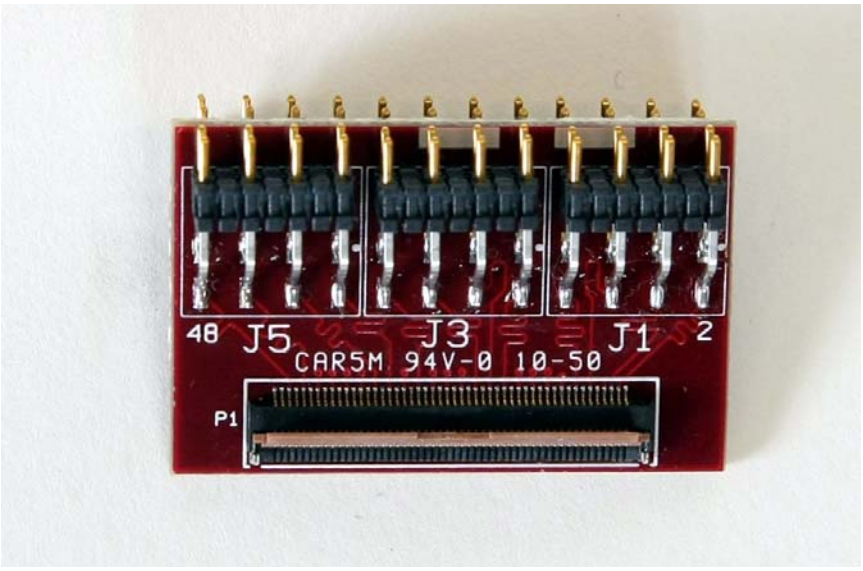


Figure 9 Top view of the W3635B

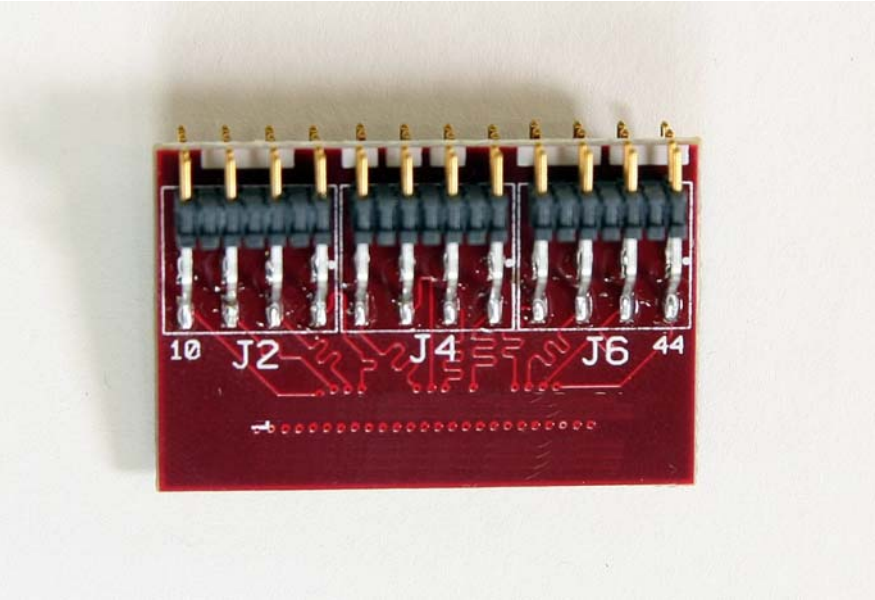


Figure 10 Bottom view of the W3635B

Table 5 W3635B pin out for W3631A x16 DDR3 BGA probe

	LEFT WING (W3631A)						RIGHT WING (W3631A)					
J2	DQL0	GND		GND	DQU7	J1	DQU4	GND		GND	DQSU#	J5
	DQL2	GND		GND	DQU5		DQU6	GND		GND	DQSU	
	DQL6	GND		GND	DQU1		DML	GND		GND	DQU2	J6
	DQL4	GND		GND	DQU3		DQL1	GND		GND	DQU0	
	CAS#	GND		GND	ODT1		DQL7	GND		GND	DQL3	
	CS0#	GND		GND	RAS#		CKE1	GND		GND	DQL5	
J4	CS1#	GND		GND	ODTO	J3	CKE0	GND		GND	CK	J3
	BA0	GND		GND	WE#		A10	GND		GND	CK#	J4
	A5	GND		GND	A3		A6	GND		GND	A12	
	A2	GND		GND	A0		A11	GND		GND	BA1	
J6	A7	GND		GND	RESET#	J5	A8	GND		GND	A4	J1
	A9	GND		GND	A13		A14	GND		GND	A1	J2

Table 6 W3635B pin out for W3633A x8 DDR3 BGA probe

LEFT WING (W3633A)						RIGHT WING (W3633A)					
	DQ6	GND		GND	DQ0		NC	GND		GND	NC	
	DQ4	GND		GND	DQ2		NC	GND		GND	NC	
J2	NC	GND		GND	DQS	J1	DQ1	GND		GND	NC	J6
	RAS#	GND		GND	DQS#		DQ3	GND		GND	DM	
	WE#	GND		GND	ODT1		DQ5	GND		GND	DQ7	
	CS0#	GND		GND	CAS#		CKE0	GND		GND	CK	
J4	CS1#	GND		GND	ODTO	J3	A10	GND		GND	CK#	J4
	BA0	GND		GND	BA2		A15	GND		GND	CKE1	
	A5	GND		GND	A0		A6	GND		GND	A12	
	A2	GND		GND	A3		A11	GND		GND	BA1	
J6	A7	GND		GND	RESET#	J5	A8	GND		GND	A4	J2
	A9	GND		GND	A13		A14	GND		GND	A1	

Table 7 W3635B pin out for W3636A DDR3 x16 non-stacked BGA probe

LEFT WING (W3636A)						RIGHT WING (W3636A)					
	DQL0	GND		GND	DQU7		DQU4	GND		GND	DQSU#	
	DQL2	GND		GND	DQU5		DQU6	GND		GND	DQSU	
J2	DQL6	GND		GND	DQU1	J1	DML	GND		GND	DQU2	J6
	DQL4	GND		GND	DQU3		DQL1	GND		GND	DQU0	
	CAS#	GND		GND	DQSL		DQL7	GND		GND	DQL3	
	CS0#	GND		GND	RAS#		A10	GND		GND	DQL5	
J4	WE#	GND		GND	ODTO	J3	CKE0	GND		GND	CK	J4
	BA0	GND		GND	BA2		A15	GND		GND	CK#	
	A5	GND		GND	A3		A6	GND		GND	A12	
	A2	GND		GND	A0		A11	GND		GND	BA1	
J6	A7	GND		GND	RESET#	J5	A8	GND		GND	A4	J2
	A9	GND		GND	A13		A14	GND		GND	A1	

Signals Probed Directly on the BGA Probes

Test points are provided on the BGA probes for some of the signals which are not probed by the logic analyzer and which are not available through the W3635B adapter. The signal names are silkscreened by the test points.

W3631A and W3633A:

- CS2#, CS3#
- VREFCA, VREFDQ
- VDD, VDDQ

W3636A:

- VREFCA, VREFDQ
- VDD, VDDQ

3 Setting Up the Logic Analysis System

The mapping of specific signals to logic analyzer channels depends on:

- Which DRAMs in a system are probed
- Which probe you are using
- How the single ended logic analyzer cable adapters are arranged when connecting to the BGA probe

Because of these dependencies, there is no single logic analyzer configuration file setup, and no configuration file is supplied with the probes. The logic analyzer Buses/Signals setup dialog will allow you to assign descriptive labels to each analyzer channel that associate each channel with the particular DRAM and DRAM signal being probed.

To save a configuration file

After you set up the logic analyzer, it is strongly recommended that you save the configuration.

To save your work, select **File>Save As...** and save the configuration as an ALA format file.

ALA format configuration files are more complete and efficient than XML format configuration files. See the logic analyzer Online help for more information on these formats.

4 Characteristics, Regulatory, and Safety Information

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Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics.

Table 8 Environmental Characteristics (Operating)

Environmental Characteristics	Values
Temperature	20° to 40° C (+68° to +104° F)
Altitude	4,600 m (15,000 ft)
Humidity	Up to 50% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board. For indoor use only.

Table 9 Inputs and Outputs

Inputs and Outputs	Values
To interposer	Memory bus signals from target system
From interposer	High-density connectors for Keysight logic analyzer cards in an Keysight 16900-series or U4154A logic analysis system and for an oscilloscope

Regulatory Notices

WEEE Compliance

Safety Symbol	Description
	This product complies with the WEEE Directive (2002/96/EC) marking requirements. The affixed label indicates that you must not discard this electrical/electronic product in domestic household waste. *Product Category: With reference to the equipment types in the WEEE Directive Annex I, this product is classed as a "Monitoring and Control Instrumentation" product.* **Do not dispose in domestic household waste. To return unwanted products, contact your local Keysight office, or see** "www.keysight.com" for more information.

China RoHS

W3631A, W3633A, W3635B, W3636A, E5845A, and E5847A

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