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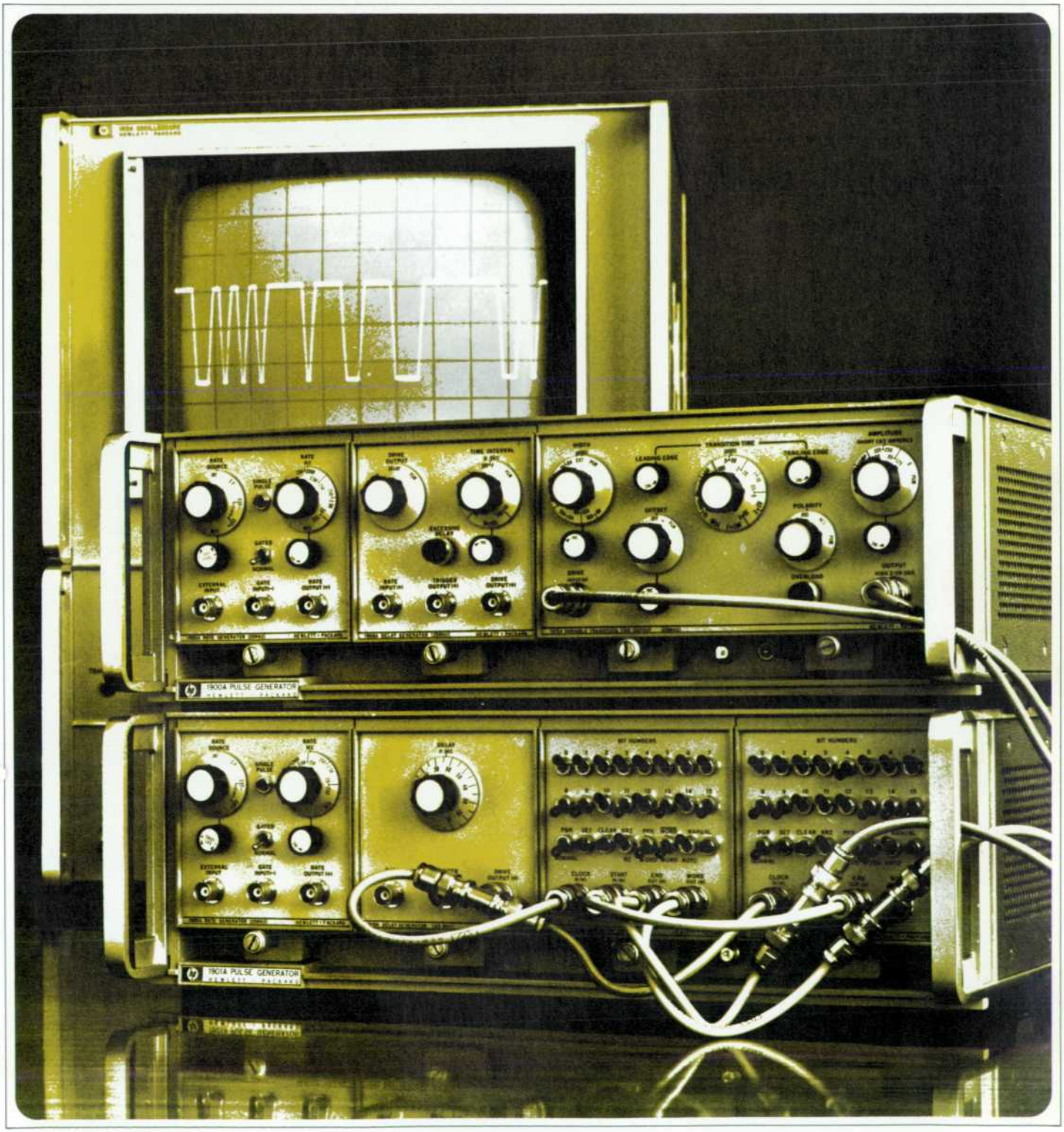

APRIL 1969

A New Programmable, Building-Block Pulse and Digital System

A pulse generator system consisting of a series of plug-ins that can be combined to provide a wide variety of digital test signals. Variable rise and fall time pulses and digital words in a number of formats are among its capabilities.

By Gordon K. Blanz and Ronald L. Knauber

PULSE AND DIGITAL TESTING requires compatibility with state-of-the-art developments and components and techniques. There is a need for a variety of pulse generation, timing and shaping methods for easier digital systems design, for remote operation of digital equipment, and at the same time a need to reduce the effects of electrical radiation. To meet these needs the HP Model 1900 Pulse System, Fig. 1 was developed as a versatile plug-in system. At present it consists of two mainframes and seven plug-ins. Others are planned. It was designed to be electronically programmable as an option, and special care was taken to reduce radiation.

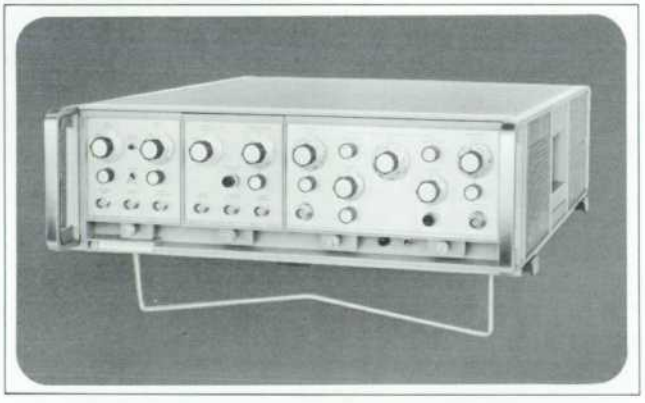

Fig. 1. *Four of the building blocks of the Model 1900 Pulse System are shown here. They are the Model 1900A Mainframe, the Model 1905A Rate Generator, the Model 1908A Delay Generator and the Model 1915A Variable Transition Time Output.*

The two mainframes, the key to the system flexibility, are the Models 1900A and 1901A. The Model 1901A omits two high voltage variable power supplies included in the Model 1900A.

The mainframes are five-inch high cabinets with four compartments designed to accept any combination of ¼-module and ½-module plug-ins (except two Model 1915A's). The Model 1900A has six supplies which provide a total of 300 watts. Any supply is available to any plug-in via connectors on a motherboard. There are two 10-volt unregulated supplies, two 25-volt fixed, regulated supplies and two 20-to-70 volt variable regulated supplies. To minimize use of power, the variable supplies were designed with switching regulators, Fig. 2. This circuit is easily programmed to supply large currents at variable voltages.

To reduce electromagnetic radiation in the system environment, several techniques are used, Fig. 3. A line filter is used as well as two inner and two outer top and bottom covers. There are gaskets between plug-ins and mainframes, and beads between ¼-module plug-ins. Also die castings are used for plug-in front panels.

Plug-ins

Plug-ins initially available include the Model 1905A Rate Generator, Model 1908A Delay Generator, Model 1910A Delay Generator, Model 1915A Variable Transition Time Output, Model 1917A Variable Transition Time Output, Model 1920A 350 ps Transition Time

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Output and the Model 1925A Word Generator. The Model 1905A has an internal clock rate of 25 Hz to 25 MHz in six decade ranges with a 10:1 continuous vernier. It supplies a positive clock pulse of less than 10 ns pulse width. In the external mode it can be driven from dc to 25 MHz with a 0.5 volt peak-to-peak positive signal with selectable trigger level and slope. By overdriving, it will provide a 50 MHz clock rate for the Model 1925A. The Model 1905A has a gating feature in which the clock pulses are synchronous with the gating signal. Programming allows remote control, computer interfacing, and phase/frequency locked loops.

The Model 1908A Delay Generator provides trigger pulses and drive pulses (each similar to the Model 1905A rate output pulse) which are used for the system timing signals. The Model 1908A can be operated in any of the following modes: drive pulse delay, drive pulse advance, double pulse and programmed. The time interval varies in six ranges from 15 ns to 10 ms with a 10:1 continuous vernier. The double pulse mode can be used to provide a 50 MHz pulse train.

The Model 1910A Delay Generator provides trigger and drive pulses up to a repetition rate of 125 MHz. The delay between trigger and drive pulses is available in twenty ranges from 5 ns to 100 ns in 5 ns increments. The Model 1910A has low jitter and can be used to obtain delays greater than a period at high repetition rates.

Varying Transition Time

Transition times variable from 7 ns to 1 ms with a 100:1 vernier can be obtained with the Model 1915A Variable Transition Time Output. Variable transition time is especially useful for testing of magnetic memory devices and MOS integrated circuits. See page 5. The leading edge and trailing edge transition times are determined by a capacitance-current source circuit, Fig. 4. A synchronous switch alternately connects a charging current source and a discharging current source to the selected capacitance C to determine the rise and fall time of the pulse. With no signal at the base of Q1, Q1 and Q4 are off, Q2 and Q3 are on and trailing edge constant current I_T linearly charges C to the baseline voltage determined by V_C. Leading edge constant current I_L flows through Q2. A negative signal at the base of Q1 turns on Q1 and Q4, turns off Q2 and Q3, and I_L linearly discharges C through Q4 to clamp CR3. A positive signal at the base of Q1 reverses the procedure and returns the output to its quiescent level. Assuming a fixed voltage V_C, the time rate of change of the transition time output voltage is:

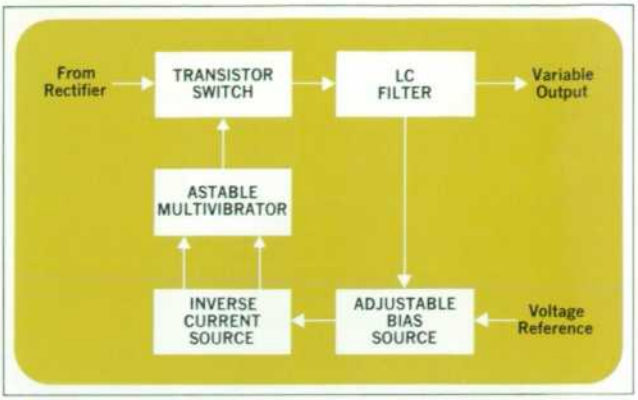

Fig. 2. *The voltage reference from a plug-in changes the inverse current source through the adjustable bias. The current controls the duty cycle of the astable multivibrator which in turn controls the operation of the transistor switch. When the switch is closed, the LC filter charges from the rectifier. When it is open, the LC filter discharges. The voltage at the output of the LC filter is variable from 20 to 70 volts. Since power is dissipated only during the switching interval and not during the open and closed interval, power in the transistor switch (the high-current path) is reduced.*

$$\frac{dv}{dt} = \frac{I}{C} = \text{constant since the charging currents are constant.}$$

(v = peak-to-peak output voltage, t = time required for peak-to-peak voltage change, I = I_L or I_T, C = selected capacitance.) I_L and I_T can be changed by a ratio of 100:1.

Variable rise and fall time pulse generators can be classified as either constant transition time or constant slope as a function of amplitude change. Unlike the constant slope instruments, the Model 1915A provides the highly useful constant transition time.

If the output pulse amplitude is to change without changing the pulse width, the rise time or the fall time, then both leading and trailing edge transition time cur-

Cover: *Two Model 1925A Word Generators are cascaded to produce a 32-bit word in a nonreturn-to-zero format shown on the face of a Model 143A Oscilloscope.*

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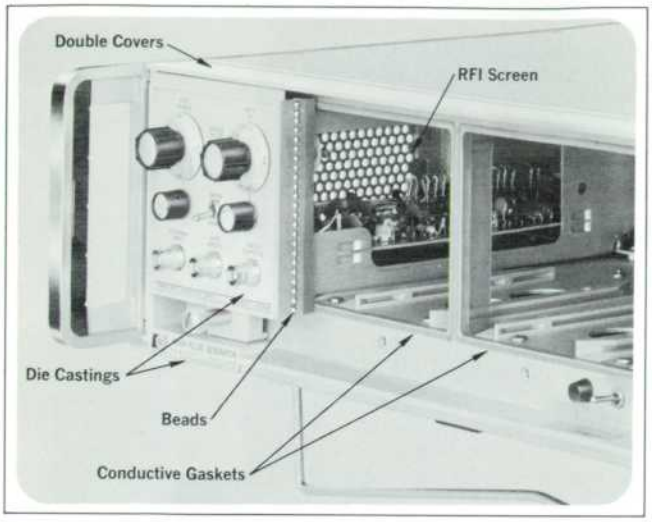


Fig. 3. *Reducing RFI is accomplished by this combination of techniques.*

rents must be modified, as well as the output current, in accordance with any change in amplitude. This is accomplished by the amplitude vernier circuitry (see Fig. 5). As the amplitude is changed by the front panel amplitude vernier control, the pulse baseline clamp voltage in the transition time circuit is changed. This results in a change in waveform 1 amplitude V_A. Simultaneously, the leading and trailing edge currents which charge and discharge capacitor C are changed by the amplitude vernier circuit to keep the transition times constant. From the basic transition equation given previously:

$$\frac{dv}{dt} = \frac{I}{C},\ dt = \frac{C}{I}\Delta v.\ But\ I = k\ \Delta v.$$

$$So\ dt = \frac{c\Delta v}{k\Delta v} = \frac{C}{k} = constant$$

$$(k = front\ panel\ amplitude\ vernier\ setting)$$

The amplitude vernier circuit also changes the current in the output current source I_0 so the voltage across resistor R, V_B, is proportional to the pulse amplitude. In Fig. 5 on waveform 2, $V_B = I_0R$.

The Model 1915A can provide 50 mA to 1 ampere output current (or 50 volts maximum into 50 ohms) in four ranges at a repetition rate from dc to 25 MHz. This current is provided by five current sources which supply four output differential amplifiers. A simplified positive output amplifier and representative waveforms are shown in Fig. 5. During the quiescent state Q7 is on and Q14 is off. When a positive pulse (waveform 2 for the positive output amplifier) is applied to the base of Q7, the sequence of turning on Q14 and turning off Q7 is started. At about the 10% level of maximum amplitude of the positive transition, Q14 turns on and conducts more heavily as the amplitude increases. At about the 90% level Q7 turns off completely, clipping the top 10% of the pulse. As the negative transition of waveform 2 starts, Q7 is fully off and Q14 is fully on. At about 90% of maximum amplitude Q7 turns on. As the negative transition falls toward the baseline, Q7 current increases and Q14 current decreases. When the 10% level is again reached, Q14 turns off, clipping the bottom 10% of the pulse. This 'window' framed by the clipping levels and represented by voltage V_B in Fig. 5, can be adjusted by changing the base voltage of Q14. Its purpose is to maintain a clean output pulse. However, it causes a small corner shift as amplitude is changed.

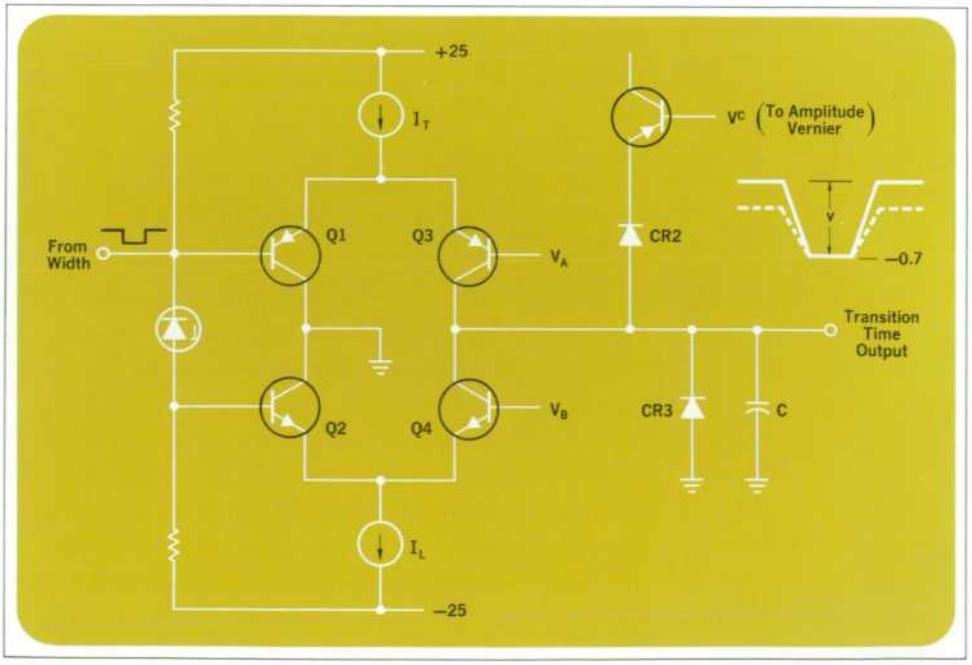


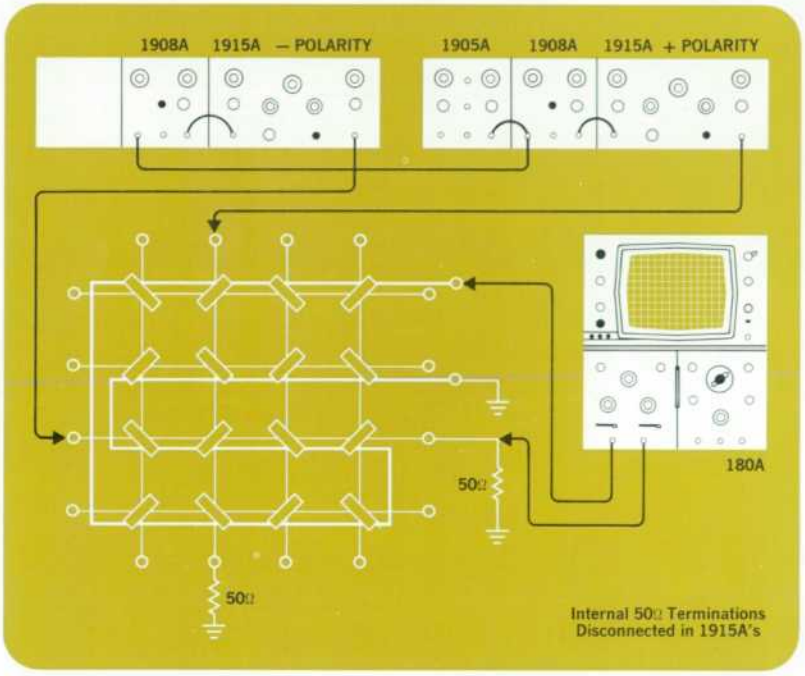
Fig. 4. *Linear leading edge and trailing edge transition times are produced by discharging capacitor C with constant current I_L and by charging the capacitor with constant current I_T.*

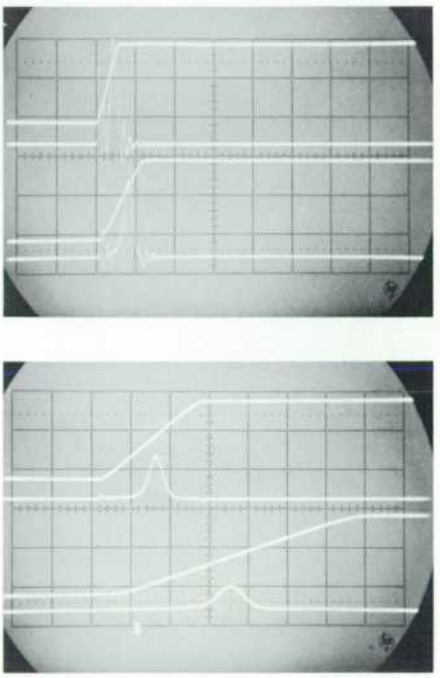
Why Use Variable Rise and Fall?

A variable rise and fall pulse generator is an extremely valuable tool in electronic circuit design. It can be used to determine the effect of the speed of an input driving pulse on a circuit output. For example, magnetic memory devices are generally tested with pulses with linear rise and fall times ranging from 10 to 700 ns. Drive currents up to 800 mA are needed. Testing of cores in a magnetic core plane is another application of a variable rise and fall pulse system.

A typical setup (below) is used to test the output of the sense winding of a core.

In these scope photos, the upper waveform is the drive signal (500 mA/cm) and the lower waveform is the sense output (200 mV/cm). The horizontal calibration is 500 ns/cm. Note that as the input drive risetime increases, output amplitude increases, output delay decreases and reflections appear and increase in amplitude.





To prevent excessive power dissipation in the output amplifier at low output levels, the high voltage variable supply level is controlled by a sample and hold circuit, the peak detector, which samples the peak output voltage and stores it on a capacitor (see Fig. 5). This peak voltage controls the reference voltage input to the variable supply in the mainframe. It maintains the variable supply (and thus the output base supply referenced to it) at minimum for outputs less than 10 volts. Above 10 volts, both supplies change one volt for every one volt change in the output. These supply changes keep the output amplifier about five volts from saturation, which reduces its power dissipation.

The Model 1915A has unique overload protection circuits for both positive and negative output stages. The instantaneous power in the output stage is monitored. If excessive dissipation occurs, the output is disabled. At the same time an overload light on the front panel is lighted. It stays on until the overload is eliminated by reducing the output amplifier dissipation with the front panel controls.

Negative Overload Protection

The currents in current sources 2 and 4, Fig. 6, are proportional to the currents in output current sources 1 and 3. Since V_2 is at the same voltage as V_B, the current in Q30A, I_1, is proportional to Q14 emitter current and the current in Q29A, I_2, is proportional to Q14 base-collector voltage. Q29A, Q29B and Q30A are matched transistors connected as diodes. The collector current of Q30B, derived from basic diode voltage-current relationships in the I_1I_2 multiplier circuit, is proportional to the product of I_1 and I_2. Therefore, the output voltage of

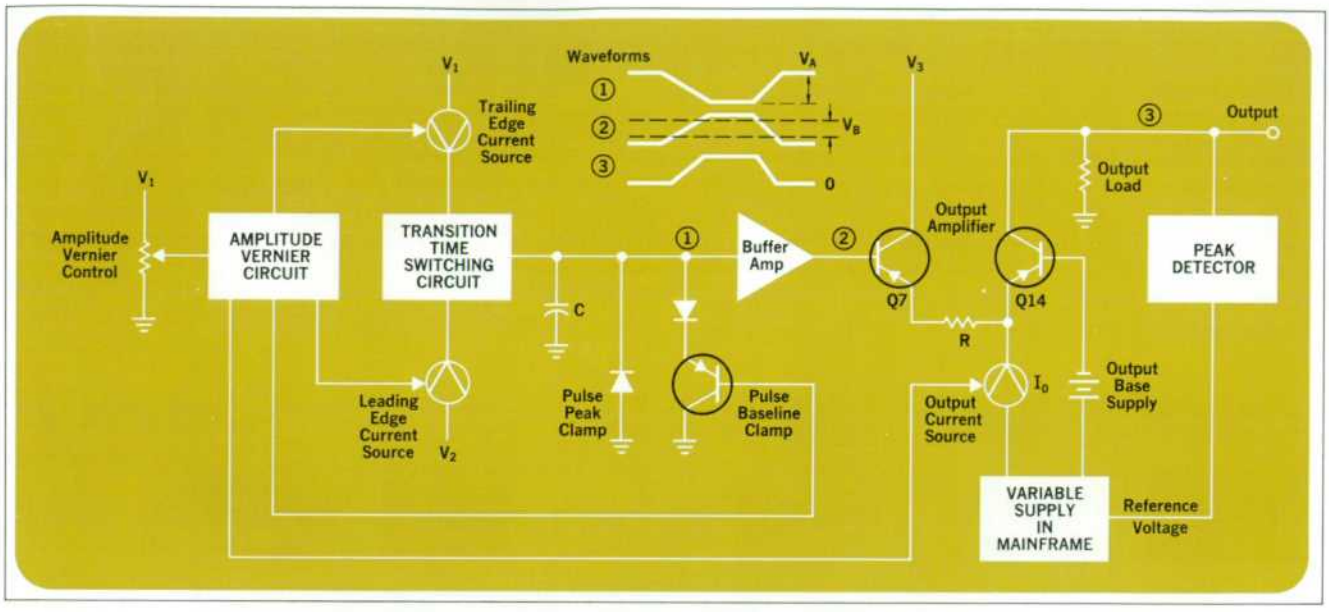


Fig. 5. *This amplitude vernier circuit maintains constant leading and trailing edge transition times as output amplitude is changed.*

emitter follower Q31 will be proportional to the instantaneous power in Q14. Due to the 3 ns response time of the diode multiplier, a small capacitor C1 was included to prevent very short overload signals from energizing the disable driver. During a longer overload, the negative disable driver (a Schmitt trigger circuit) switches, disabling the output current sources and energizing the overload light. As I_1 and I_2 are reduced, the circuit returns to its quiescent state. The cycle repeats as long as the overload continues. The repetition rate of the circuit is determined by the time rate of discharge of C2 through Q31 and the severity of the overload. It varies from 5 kHz to 30 kHz (see Fig. 7).

Varying Pulse Widths

Internal pulse widths from 10 ns to 40 ms with a con-

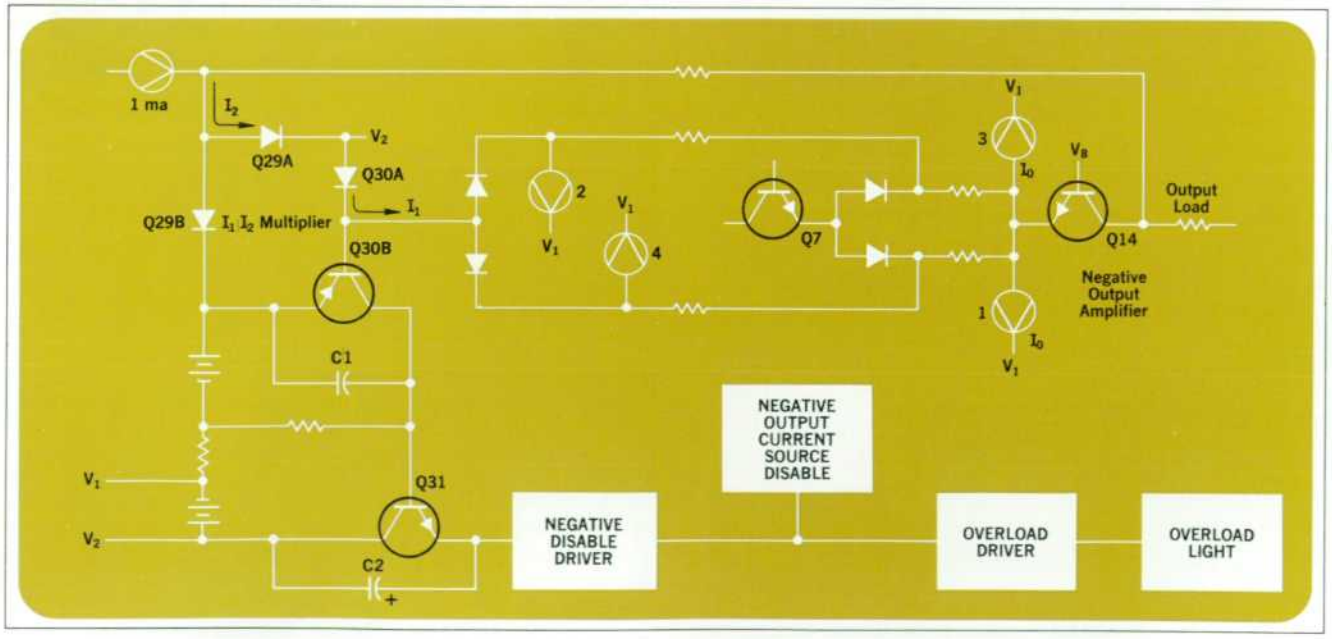


Fig. 6. *Two currents, one proportional to output amplifier current and one proportional to output amplifier base-collector voltage are multiplied in a diode multiplier circuit. This product represents the instantaneous output amplifier power. A voltage proportional to the power disables the output when the power exceeds a predetermined level.*

tinuous 10:1 vernier are supplied by the Model 1915A. Duty cycles up to 90% can be obtained with internal width operation. The Model 1915A also provides an external width setting which converts the width circuit to a pulse amplifier. The external width mode allows the Model 1915A to accept a variable width pulse train, and to shape and amplify the pulses but retain the initial widths. In this mode 100% duty cycles are possible. Also three of the four basic logic formats can be used with the external width mode: return-to-zero, non-return-to-zero and bi-phase. Only bi-polar logic cannot be used. The external width mode is extremely useful in conjunction with the HP Model 1925A Word Generator (see page 8).

To fill the needs of bipolar transistor and IC testing and general purpose work, a low-power output plug-in was designed. This Model 1917A Variable Transition Time Output is a low-power, low-cost version of the Model 1915A with many of the same features. Width capabilities are identical. Transition times available are 7 ns to 500 μs in five ranges with a 50:1 vernier. Five amplitude settings span a range from 0.2 to 10 volts into an external 50 ohm load. A maximum of 100 mA offset (or 2.5 volts into an external 50 ohms) in both polarities is provided.

A fast 350 ps, fixed rise and fall time is available in the Model 1920A 350 ps Transition Time Output. It provides an output amplitude of 0.5 to 5 volts in three ranges, continuously adjustable, at repetition rates to 25 MHz. Pulse width is 0 to 10μs in four ranges, also continuously adjustable. Outputs are available in either positive or negative polarity with offsets up to 2 volts into 50 ohms.

The Model 1925A is a serial digital word generator (see accompanying article) which provides variable word length at clock rates from dc to 50 MHz. It has a pseudo-random bit sequence, and programming that is compatible with integrated circuits.

Designed for Programming

Programming is an integral part of the pulse system design. The circuits are designed so that the programming response times are as short as possible. With few exceptions, response times are between 3 and 30 μs. Circuit functions are designed with electronic controllability in mind, that is, with the application of a voltage or a current, not by a mechanical method. For example, in the Model 1915A, the output current sources are turned on and off by applying a voltage to transistor bases. This allows easy programming of the output current and avoids wasteful dissipation (as much as 50 watts) in a mechanical attenuator. Also, the set of range capacitors are linearly charged and discharged in the rate, delay, width and transition time range circuits, Fig. 8.

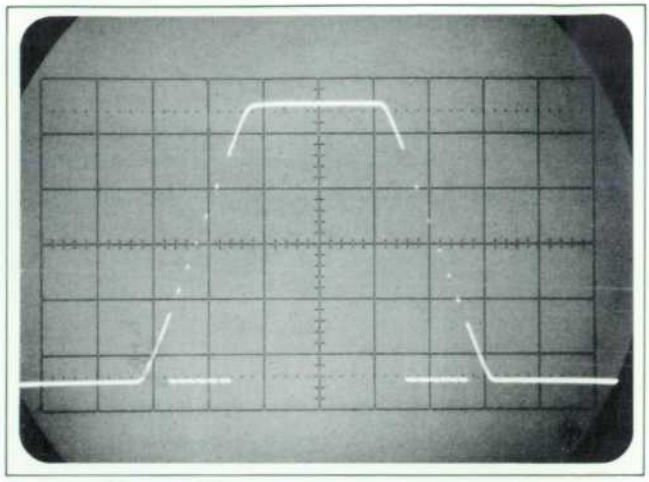


Fig. 7. *How the overload protection circuit disables output current during excessive power dissipation in the output amplifier. This output waveform is 50 volts into 50 ohms with a rise and fall time of 1 ms.*

At the present time the two mainframes can be wired with a program cable assembly used to connect the plug-ins to the rear panel. Four rear panel connectors, one for each ¼-module plug-in compartment, provide the interface between the Model 1900 system and an external programming system. The required programming circuitry is provided by plug-in boards or other boards which can be installed at the factory or in the field.

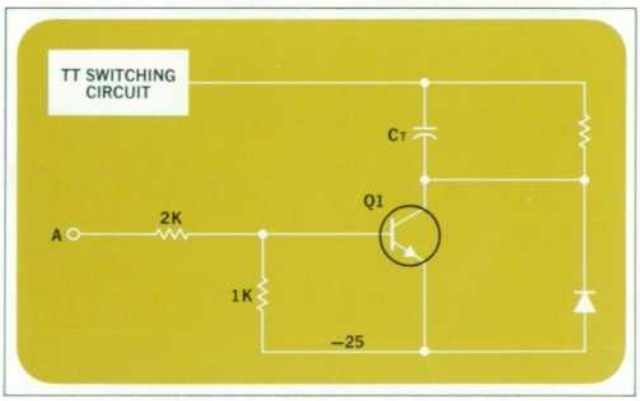


Fig. 8. *The transition time range capacitor CT can be energized mechanically or electronically with the circuit shown here. When point A is grounded, 12 mA passes into the base of Q1 causing it to saturate. Thus CT is connected to the −25 V supply. Then capacitor CT will charge and discharge in accordance with the transition time switching circuit. During saturation, both the forward and reverse beta characteristics of the transistor Q1 are important, since current will flow in both directions through the transistor.*

Gordon Blanz (right) has a degree of BEE from the University of Minnesota (1960) and a degree of MSEE from the University of Colorado (1968). He joined Hewlett-Packard in Palo Alto in 1960 as a development engineer and worked on the design of the HP Model 140A Oscilloscope. He later transferred to Colorado Springs in the high-frequency design group and was responsible for the design of the Model 1755A Dual Trace Amplifier. He is presently part of the Model 1900 System design group.

Among his hobbies, Gordon plays tennis and climbs mountains. He has climbed 37 of 53 Colorado peaks over 14,000 feet. Gordon is a member of Eta Kappa Nu.

Ron Knauber (left) attended the University of Nebraska where he received his BSEE in 1961. He was project leader on the initial design phase of the Model 1900 Pulse System. Prior to joining Hewlett-Packard in 1965, Ron worked on flight control systems.

Ron is an accomplished pianist, and like many of his associates at HP, is a mountain climber and enjoys hunting. He is a member of Eta Kappa Nu and Pi Mu Epsilon.

The range and the 'not-continuously-adjustable' functions are digitally programmed by a contact closure to ground that also is a 10 mA current sink. An open circuit deactivates a program line. A continuously adjustable function requires an analog program current of 0 to 10 mA.

Acknowledgments

The major contributors to the Model 1900 System circuit design were Gordon K. Blanz, Dee Broadhead, James D. Dolan, Edward S. Donn, Ronald L. Knauber, Stanley R. Lang, Robert L. Morrell, Jeffrey H. Smith and James M. Umphrey. Early project work was done by Larry Nevin and Ronald J. Huppi. The product design was done by Albert C. Knack, Spencer M. Ure and Norman L. O'Neal. Technical support was contributed by Paul P. Ficek, Charles T. Small and E. Yates Keiter. We would especially like to acknowledge the valuable work done on 1900 system multilayer printed circuit boards, both by Paulette Metcalf and Sheila McCullough for the printed circuit artwork and by Charles Canfield's processing shop for providing many prototype and production boards. Blair H. Harrison's encouragement and ideas are also greatly appreciated.

Generating Words for Digital Testing

By Eddie Donn

DIGITAL EQUIPMENT TESTING requires a wide variety of special test signals. The most practical way to meet these varied requirements is with the programmable plug-in system used in the HP Model 1900 Pulse System. A key element of this system, the HP Model 1925A Word Generator, Fig. 1, is capable of generating a variable length, serial digital word at clock rates up to 50 MHz, in several operating modes. Front-panel switching on the plug-in permits selection of: return-to-zero (RZ) or non-return-to-zero (NRZ) format, Fig. 2(a), complementary output, Fig. 2(b), command or automatic word recycling, and electronic programming. In addition a long pseudo-random sequence (32,767 bits) is provided for testing communcations channels and LSI memories. The internal registers may be set or cleared from the front panel to establish reference levels and sequences.

Interface

The Word Generator will interface with all other plug-ins in the 1900 system. It accepts clock signals from the Rate Generator (HP Model 1905) or the Delay Generator (HP Model 1908A), and it can supply compatible

trigger pulses to the Output Stages (Models 1915 or 1917).

Most pulse generators accept only return-to-zero (RZ) trigger inputs because they operate only upon the leading edge of the trigger pulse. A special trigger input on the 1900 output stages, External Width, assures compatibility with all data formats of the Word Generator. In this mode the output stage is operated as a pulse amplifier (the pulse width is determined by the incoming signal). This special mode is essential when NRZ digital waveforms or any form of the biphase formats is used. The usual Internal Width mode on the Output Stage will accommodate RZ formats (the pulse width is determined by the output stage).

Logic power supplies in the Model 1900A mainframe are capable of driving two Word Generators; power supplies in the Model 1901 mainframe are capable of driving four Word Generators. Both positive and negative voltages are available for powering either saturated or emitter-coupled types of logic.

Fig. 1. *Characters are generated by setting the appropriate toggle switches on the front panel of this HP Model 1925A Word Generator plug-in. Complement, pseudo-random noise, and RZ and NRZ formats can be selected.*

Logic

Emitter-coupled integrated circuit logic is used in the Word Generator. Emitter-coupled, non-saturated circuits are quite at home in the Model 1900 system, since that is basically the technique used in most of the pulse generator circuits.

The digital word is generated by first loading it in parallel into an open-ended shift register at the end of each word, Fig. 3. This is essential for rapid reprogramming of the word. The parallel data can be set by the front panel switches or brought in from the electronic programming inputs. The word is then shifted out of the register in synchronism with the clock input. The shift register output is operated upon to produce the desired format: non-return-to-zero or return-to-zero, normal or complemented. A transmission line driver then delivers the word to its destination.

WORD recycling is accomplished by a flip-flop which keeps track of the WORD state. When the WORD state is false the instrument loads the shift register with incom-

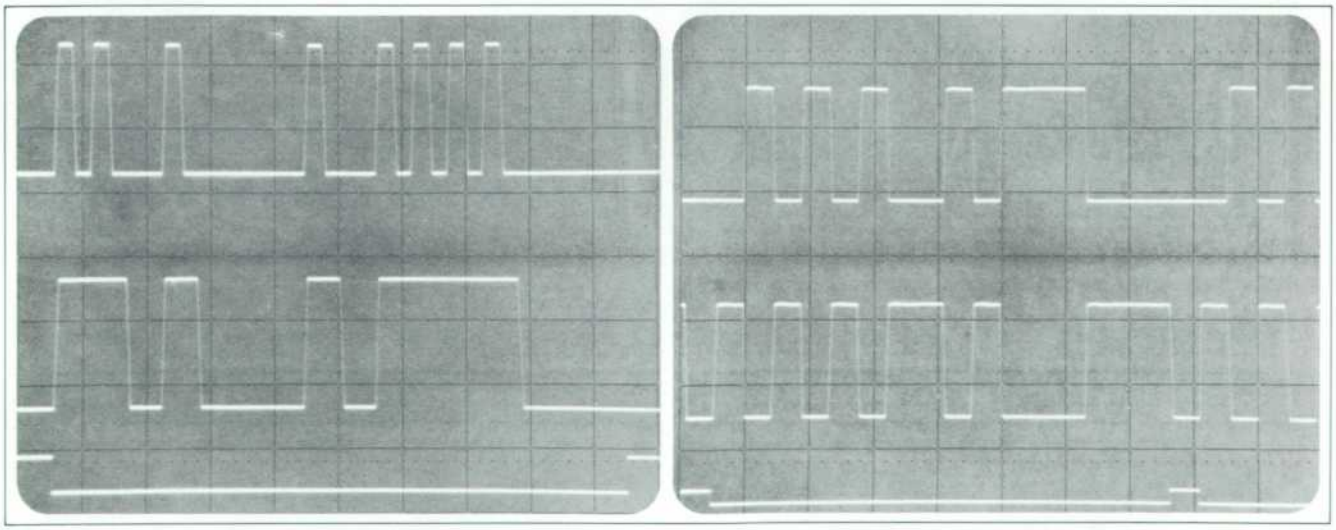


Fig. 2. *Oscilloscope traces (left) show a return-to-zero (top trace) and nonreturn-to-zero format (middle trace) with END pulses on the bottom trace. At (right), the top trace is a normal output signal while its complement is the middle trace. The WORD output is forced to zero at the END signal (bottom trace).*

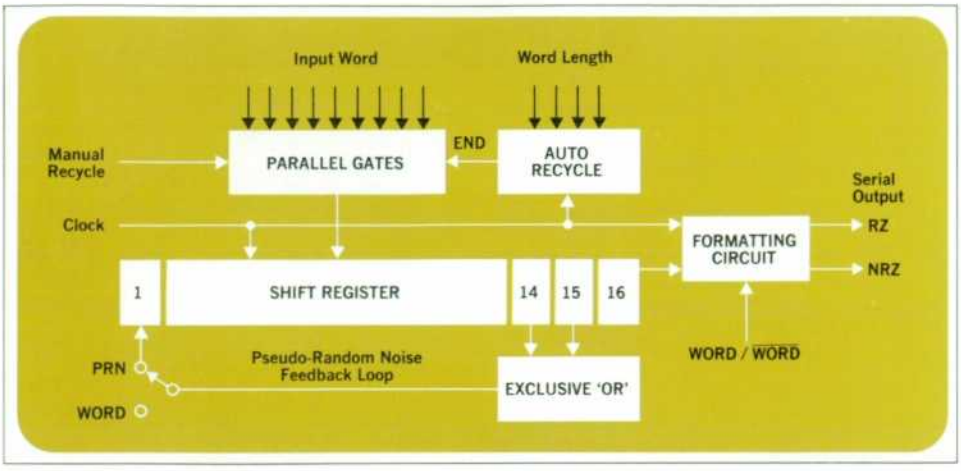


Fig. 3. *For rapid programming, the input word to the Model 1925A Word Generator is loaded in parallel into the shift register. The word is then shifted out in sync with the clock. Pseudo-random noise sequences are generated by a digital feedback technique.*

ing data and presets a counter according to the desired word length. In the AUTO recycle mode, this occurs for one period of the clock. In the MANUAL recycle mode the WORD state remains false until the receipt of a START signal or a command from the MANUAL push-button, Fig. 4. The END output is the logical complement of the WORD state. It goes true between words in the AUTO recycle mode. This information may be used for scope sync or to command a new word from an electronic programmer.

Variable Word Length

Word length is determined by a variable modulus counter. Words shorter than 16 are generated by reducing the modulus of the counter which controls the word state, Fig. 5. This is accomplished by four switches inside the Model 1925A which are set in the 17's complement of the desired word length — 0001 for 16, 1000 for 9, etc. Unused data switches are simply set to zero.

Long Words

Words longer than 16 bits, Fig. 6, are generated by either continually programming new sequences with the parallel inputs or by stacking the word generators. Stacking is accomplished by connecting the END of the one generator to the START of the next. The loop is completed by connecting the END of the last generator to the START of the first.

Pseudo Random Noise

In the pseudo-random-noise (PRN) mode, the WORD state is forced true, hence END is inoperative. In this mode a digital feedback circuit is enabled such that the input to the first register is equal to the Exclusive-Or of

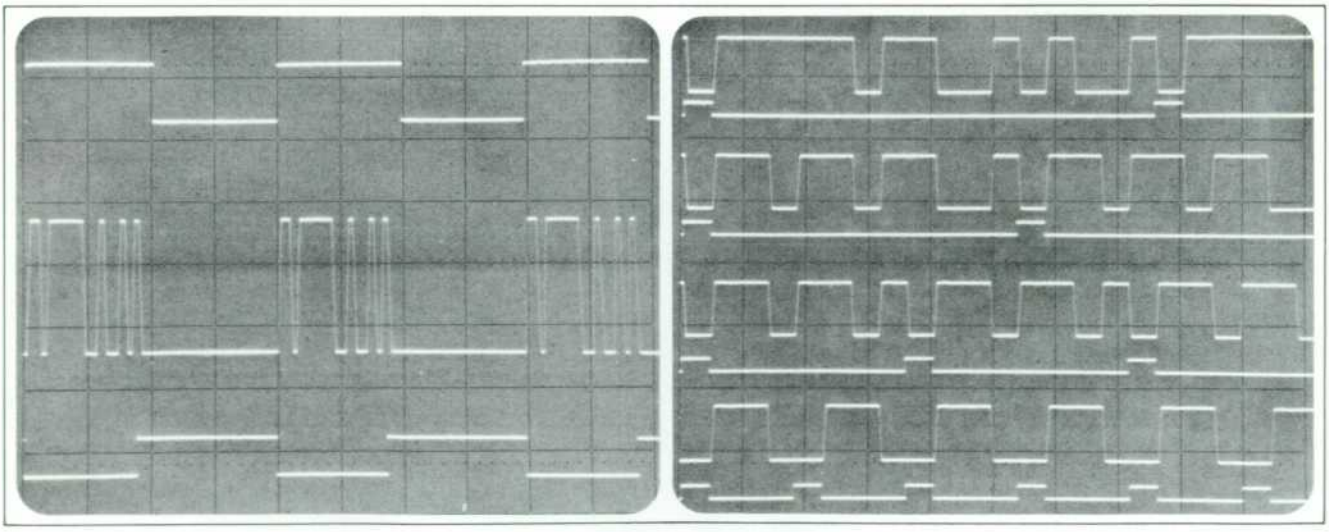


Fig. 4. *(left) Synchronous gating of a word from an external source is possible by providing a signal (top trace) to both the Rate Generator GATE input and the Word Generator START input. The resulting word (middle trace) and the END pulses (bottom trace) are shown.* **Fig. 5.** *(right) Word lengths from 2 to 16 bits may be constructed. Shown from top to bottom are word lengths of 16, 11, 7 and 3 bits.*

the contents of the 14th and 15th cells in the register. This results in a maximal length linear shift register sequence of 2^{15}-1 or 32,767 bits. Other sequences can be provided. The sequence starts with the current contents of the shift register. This will be the same as the data input if the machine is in the MANUAL mode. The sequence will continuously recycle.

The sequence has the following randomness properties: ones and zeros occur equally often; after a run of ones and zeros there is a 50% chance the run will end with the next bit; and it is not possible to predict an entire sequence from any partial sequence. The runs of ones and zeros are useful for investigating duty cycle problems. In this sequence there are 4096 runs of length one, 2048 runs of length two, 1024 runs of length three, etc., 1 run of 14 zeros, and 1 run of 15 ones.

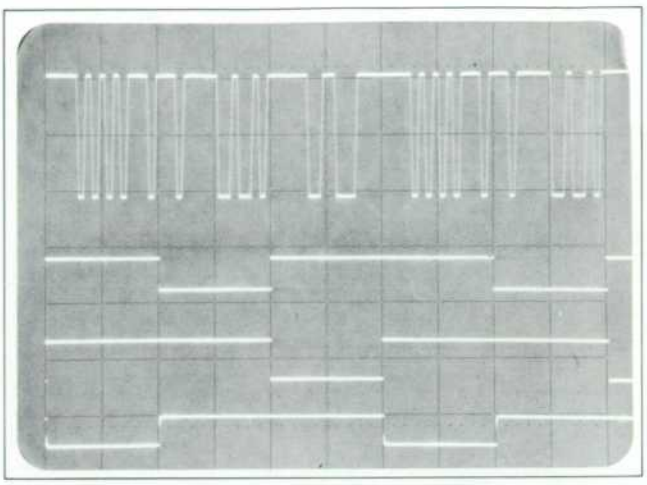


Fig. 6. *Long words are constructed by ganging word generators together. The top trace shows a 48-bit word. Below are END pulses from the first, second and third word generators.*

Construction

Logic is on three multilayer printed circuit boards separated into logical functions. The shift register flip-flops and their loading gates are located on one board to minimize the transmission of high frequency signals to other parts of the instrument. The other two circuit boards contain the control circuitry for the various modes of operation. Two additional multilayer PC boards contain interconnections and programming circuitry. Multilayer PC boards allow better transmission of the high speed ECL (emitter-coupled logic) signals and reduce the need for elaborate wire harnesses.

The plug-in boards permit fast trouble-shooting with high packaging density. The problem of rigidity is solved by anchoring the boards with a sheet metal top cover. This also provides good airflow and increases RFI shielding.

Programming

Programming is accomplished by an interface network which transforms contact-closure or TTL type inputs (0 to +4 V) to MECL levels (−0.7 to −1.5 V). The front panel switches are disabled by gates during programmed operation. When they are enabled, the front panel switches override any information on the programming lines.

When fast programming is desired, the electronic inputs should be provided via transmission lines (twisted pairs are most economical). The programming source should be matched to the impedance of the transmission line by a series resistor if it is a voltage source (approximately 100 ohms for twisted PVC wire).

Two methods of programming may be used. The fastest is to reprogram at the start of each word. This allows the maximum possible time for the programming lines to settle to their new values. Alternately, the programmed data may be strobed into the word generator during END. The data gates to the internal memory are open during END and the memory will latch on the strobed data bits. The time constant of the interface network is about 0.1 μs, so END must have a duration of at least 0.2 μs. The need for buffer storage of the parallel programming data is eliminated.

Circuits

CLOCK and START inputs are terminated in 50 ohms and designed to receive 1 volt or 20 mA signals. The width of the CLOCK signal is important; the word generator is designed to receive the output of the 1905A or 1906A Rate Generators. The rate generators, however, are designed to receive external signals with arbitrary waveforms. The leading edge of the START input is differentiated internally, so it may be of any width between 10 ns and the period of the word cycle.

WORD and END outputs are from current source line drivers. The complementary MECL outputs are used to drive two pairs of emitter-coupled differential amplifiers. The result is a fast, clean signal suitable for triggering. The propagation delay between the incoming CLOCK and the WORD and END outputs is less than 20 ns.

Since the outputs of the Word Generator are intended to drive 50 ohm trigger inputs of the 1900 system, they

Eddie Donn

Ed Donn graduated from the University of Florida with a BSEE in 1962. After graduating he worked on missile guidance, anti-submarine warfare, satellite communications, and ground support systems. Since joining HP in 1966 he has worked on the pulse shaping circuits in the 1915 Variable Rise and Fall Output Stage and product planning for the 1900 series digital plug-ins.

Ed enjoys motorcycling, mountain and rock climbing. He has climbed 19 of Colorado's 14,000-foot peaks and led several local roped climbs.

are unterminated. To drive unterminated or ac terminated loads (such as some scope trigger inputs), END and WORD may be terminated at the plug-in or at the load, whichever is appropriate.

Similar to other 1900 System plug-ins, the electronic inputs and outputs of the Word Generator may be switched to the front panel or to the mainframe connector. Complicated configurations are thus patched together inside the mainframe rather than by cables on the front panel. Any one or all of the inputs and outputs may be connected in this manner.

Noise induced problems are eliminated by adequate grounding and power supply filters. Ground loops are eliminated with balun transformers. For accurate phase control, all clock signals are transmitted to the logic boards via coaxial transmission lines.

Noise between plug-ins is reduced by having separate power supply regulators in each digital plug-in. This also provides better voltage regulation and very fast current limiting in case of a malfunction.

Applications

Several features of the word generator may be illustrated by a typical application which requires a return-to-zero format with 11 bits of data of width t_1, and a sync bit of width t_2, Fig. 7(a). The equipment needed includes a rate generator and two word generators. One of the following combinations of output stages may be used: A 1901A low power mainframe with two 1920A's for fast risetime applications, or a 1900A with two 1915A plug-ins modified for two positive, two negative, or positive and negative outputs. The rate generator provides the clock for both word generators. Word generator #1 provides timing for the data (which could be programmed), and word generator #2 provides timing for the sync. Similarly, output stage #1 provides the data outputs of width t_1 and output stage #2 provides the sync output of width t_2. The two output stages are summed together for the desired output. Both word generators are set for a word length of 12 bits (11 data bits plus 1 sync bit).

Using a similar configuration it is possible to generate bipolar outputs, Fig. 7(b). In that case output #1 would generate the positive pulses and output #2 would generate the negative pulses of the bipolar pulse train. Using Model 1915A or the Model 1917A plug-ins, the pulse widths, rise and fall times, amplitude, current offset and polarity can be independently controlled and programmed.

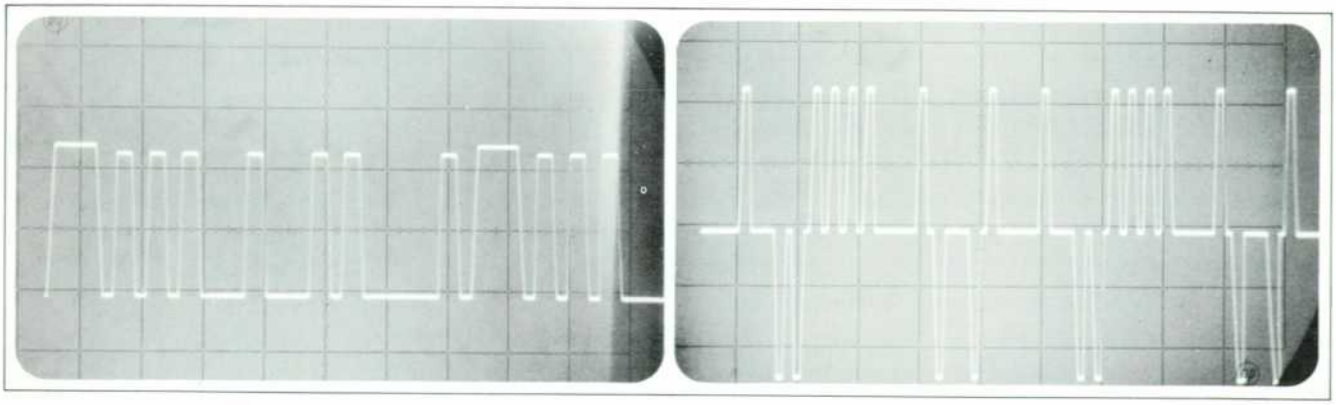


Fig. 7. *Two word generators and two output stages are used to generate this word (left) consisting of one wide sync bit and 11 narrow data bits. Bipolar words (right) can be generated with the same combination.*

Acknowledgments

Much of the convenience and economy of the Word Generator — both to the user and in production — is the result of innovations contributed by Al Knack (product design) and Chuck Small (electronic technician). Rodger Earley contributed many ideas which helped speed the transfer from breadboard to production.

Bibliography

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2. Solomon W. Golomb, 'Shift Register Sequences,' Holden-Day, San Francisco 1967.
3. George C. Anderson, Brian W. Finnie and Gordon T. Roberts, 'Pseudo-Random and Random Test Signals,' **Hewlett-Packard Journal,** Sept. 1967.

SPECIFICATIONS

HP Model 1900

Pulse System

The HP Model 1900 Pulse System is all solid-state with plug-in capability and can be assembled in a variety of combinations. All major functions can be programmed with an added option.

Model 1900A Mainframe

PLUG-INS:
Mainframe accepts any 1900 series quarter-size or half-size plug-ins. Plug-ins may be interchanged in any manner within the mainframe.

INTERCONNECTION BETWEEN PLUG-INS
Either external (with BNC cables) or internally selectable with switches in the plug-ins.

GENERAL
DIMENSIONS: 16¾ in. wide, 5¼ in. high, 21⅛ in. deep overall (425 x 133 x 543 mm).
POWER: 115 or 230 volts ±10% 50 to 60 Hz, 300 watts max.
PRICE: HP Model 1900A, **$750.00.**

Model 1901A Mainframe

PLUG-INS:
Mainframe accepts low power 1900 series quarter-size or half-size plug-ins. Plug-ins may be interchanged in any manner within the mainframe.

INTERCONNECTIONS BETWEEN PLUG-INS:
Either external (with BNC cables) or internally, selectable with switches in the plug-ins.

GENERAL
DIMENSIONS: 16¾ in. wide, 5¼ in. high, 21⅛ in. deep overall (425 x 133 x 543 mm).
POWER: 115 or 230 volts ±10%, 50 to 60 Hz, 250 watts max.
PRICE: HP Model 1901A, **$450.00.**

Model 1905A Rate Generator

INTERNAL
REPETITION RATE: 25 Hz to 25 MHz in 6 decade ranges. 10:1 vernier allows continuous adjustment on any range.
PERIOD JITTER: <0.1% of selected period.

EXTERNAL INPUT
REPETITION RATE: 0 to 25 MHz.
INPUT IMPEDANCE: 50 Ω, dc-coupled.
SENSITIVITY: 0.5 volts peak-to-peak.
LEVEL: Continuously variable over ±3 volt range.
SLOPE: + or −, selectable.
DELAY: Approx. 10 ns between trigger input and rate output.

SYNCHRONOUS GATING
SENSITIVITY: −2 volts or more required to gate pulse train on.
INPUT IMPEDANCE: 50 Ω, dc-coupled.
DELAY: Approx. 27 ns between gate input and first rate output.

MANUAL OPERATION: Pushbutton for single pulse.

RATE OUTPUT
AMPLITUDE: >1 volt into 25 Ω (drives two 1900 series plug-ins).
RISETIME: <5 ns.
WIDTH: <10 ns.

GENERAL
PRICE: HP Model 1905A, **$200.00.**

Model 1908A Delay Generator

FUNCTIONS (DRIVE OUTPUT SWITCH)
DELAY: Drive output delayed with respect to trigger output.
ADVANCE: Trigger output delayed with respect to drive output.
DOUBLE PULSE: Generated from drive output connector. Spacing determined by time interval setting.

TIME INTERVAL
RANGE: 15 ns to 10 ms in 6 ranges. 10:1 vernier allows continuous adjustment on any range.
JITTER: <0.1% of selected time interval.
EXCESSIVE DELAY INDICATOR: Light comes on when selected time interval exceeds pulse period.

RATE INPUT
REPETITION RATE: 0 to 25 MHz.
INPUT IMPEDANCE: 50 Ω, dc-coupled.
SENSITIVITY: >+1 volt peak.
WIDTH: Portion of input trigger above 0.8 volts must be <7 ns.

TRIGGER AND DRIVE OUTPUTS
AMPLITUDE: >+1 volt into 25 Ω (drives two 1900 series plug-ins).
WIDTH: <10 ns.
RISETIME: <5 ns.
MINIMUM DELAY AFTER RATE INPUT: Trigger output occurs in approx. 14 ns in drive output delay mode; approx. 29 ns in drive output delay mode; approx. 14 ns in drive output advance mode.

GENERAL
PRICE: HP Model 1908A, **$200.00.**

Model 1910A Delay Generator

TIME INTERVAL
RANGE: 5 ns to 100 ns, 5 ns steps.
JITTER: <10 ps.

RATE INPUT
REPETITION RATE: 0 to 125 MHz.
INPUT IMPEDANCE: 50 Ω, dc-coupled.
SENSITIVITY: >+1 volt peak.
CONNECTION: Rate input may be connected internally or externally from other plug-ins, selected by internal switch.

TRIGGER AND DRIVE OUTPUTS
AMPLITUDE: >+1 volt into 25 ohms (drives two 1900 series plug-ins).
BASE WIDTH: <8 ns.
RISETIME: <3 ns.
MINIMUM DELAY AFTER RATE INPUT: ≃ 5 ns.

GENERAL
PRICE: HP Model 1910A, **$150.00.**

Model 1915A Variable Transition Time Output

OUTPUT
SOURCE IMPEDANCE
50 Ω or high Z; self contained 50 Ω termination may be connected or disconnected.
HIGH Z OUTPUT: Approx 5 k ohms shunted by 45 pF.
50 Ω OUTPUT: Approx 50 Ω shunted by 45 pF.
AMPLITUDE (SHORT CIRCUIT CURRENT)
50 milliamperes to 1 ampere in 4 ranges; 2.5:1 vernier allows continuous adjustment on any range. Voltage into external 50 Ω is ±2.5 V to ±50 V with high Z source; ±1.25 V to ±25 V with 50 Ω source. Maximum amplitude (including offset) is ±50 V.
PULSE TOP VARIATIONS
WITH 50 Ω SOURCE AND 50 Ω LOAD: ±5% for transition times 7 ns to 10 ns; ±2% for transition times >10 ns.
WITH HIGH Z SOURCE AND 50 Ω LOAD: ±5% for all transition times.
POLARITY: + or −, selectable.
DUTY CYCLE: 0 to >90% internal width mode; 0 to 100% external width mode.
BASELINE OFFSET: ±60 milliamperes. Maximum offset into external 50 Ω is ±1.5 volts with 50 Ω source; ±3 volts with high Z source.
TRANSITION TIMES: 7 ns (10 ns with high Z source) to 1 ms in 11 ranges (1,2,5 sequence); two 100:1 verniers allow independent control of rise and fall times.

WIDTH
INTERNAL
RANGES: 10 ns to 40 ms in 7 decade ranges (except for first range which is 10 to 40 ns); 10:1 vernier allows continuous adjustment on any range.
WIDTH JITTER: <0.5% of selected pulse width.
EXTERNAL
Provides pulse amplifier operation; output pulse width determined by width of drive input.

DRIVE INPUT
REPETITION RATE: 0 to 25 MHz.
INPUT IMPEDANCE: 50 Ω, dc-coupled.
SENSITIVITY: >+1 volt peak.

GENERAL
PRICE: HP Model 1915A, **$1600.00.**

Model 1917A Variable Transition Time Output

OUTPUT PULSE
SOURCE IMPEDANCE: Approx 50 ohms shunted by 45 pF amplitude (volts into 50 ohms) 0.2 to 10 volts; 2.5:1 vernier allows continuous adjustment on any range.
PULSE TOP VARIATIONS: ±5% for transition times >7 ns.
POLARITY: + or −, selectable.
DUTY CYCLE: 0 to >90% internal width mode.
0 to 100% external width mode.
BASELINE OFFSET: ±2.5 volts into external 50 ohms.
TRANSITION TIMES: 7 ns to 500 μs in 5 ranges; two 50:1 verniers allow independent control of rise and fall times.
WIDTH
INTERNAL
RANGES: 10 ns to 40 ms in 7 decade ranges (except for first range which is 10 to 40 ns); 10:1 vernier allows continuous adjustment on any range.
EXTERNAL
Provides pulse amplifier operation, output pulse width determined by width of drive input.
DRIVE INPUT
REPETITION RATE: 0 to 25 MHz.
INPUT IMPEDANCE: 50 ohms, dc coupled.
SENSITIVITY: >+1 volt peak.

GENERAL
PRICE: HP Model 1917A, **$525.00.**

Model 1920A 350 ps Transition Time Output

OUTPUT PULSE
SOURCE IMPEDANCE: Approx 50 ohms.
AMPLITUDE: 0.5 to 5 volts in three ranges; 2.5:1 vernier allows continuous adjustment on any range.
TRANSITION TIME: Rise and fall times <350 ps at max amplitude.
PULSE TOP VARIATIONS: <8% at max amplitude.
POLARITY: + or −, selectable.
BASELINE OFFSET: Max offset into external 50 ohms is ±2 volts.
WIDTH: 0 to 10 ns in four ranges, 10:1 vernier allows continuous adjustment on any range.
DRIVE INPUT
REPETITION RATE: 0 to 25 MHz.
INPUT IMPEDANCE: 50 ohms, dc-coupled.
SENSITIVITY: >+1 volt peak.

GENERAL
PRICE: HP Model 1920A, **$1750.00.**

Model 1925A Word Generator

WORD GENERATION
WORD LENGTH: 2 to 16 bits, set by internal switches, not programmable.
WORD CONTENT: Set by front panel switches or rear panel programming. Loaded into shift register between each word cycle during END.
WORD FORMAT:
NRZ/RZ, selectable from front panel or programmed. RZ pulse width less than clock period/2. WORD or WORD selectable from front panel switch.
WORD CYCLING: Automatic (continuous with one clock period delay between words), external start command, or manual push button.
MANUAL/AUTO: Selectable from front panel switch or programmed. In AUTO mode, word continuously recycles with one clock period delay between words. In program mode, content of each word corresponds to the previous parallel word input that existed >200 ns before and during END. In manual mode, a word starts after receiving an external start signal or pressing MANUAL push button and stops after 16 clock pulses.
END OUT: Available from front panel BNC corresponding to end-of-word.
SET: Serially loads ones into shift register. Output word bits are all ones after 16 clock pulses.
CLEAR: Resets shift register in parallel. Output word bits are all zero.
PSEUDO-RANDOM NOISE: Provides a linear shift register sequence of 32,767 bits. The sequence starts with the last 16 bit word in the shift register.
PROGRAMMING: All data bits, NRZ/RZ, PRN/WORD, and MAN/AUTO.

INTERFACE
CLOCK INPUT: (1905A or 1906A)
REPETITION RATE: 0 to 25 MHz
AMPLITUDE: >0.9 volts, <4 volts
WIDTH: >4 ns, <18 ns at +0.6 volts
INPUT IMPEDANCE: 50 ohms dc-coupled
START INPUT
PERIOD: Word length +15 ns
AMPLITUDE: >0.9 volts, <4 volts
WIDTH: >5 ns
INPUT IMPEDANCE: 50 ohms dc-coupled
PROGRAMMING INPUTS
TRUE: Contact closure, saturated DTL, or voltage source (TTL) <+0.2 V.
FALSE: Open, off DTL or voltage source (TTL) >2.5 V, <4.0 V.
WORD AND END OUTPUT:
TRUE: 40 ±10 ma current source or 2.0 ±0.5 V into 50 ohms.
FALSE: <1 ma.
RISE AND FALL TIMES: <4 ns (10% to 90%).
PERTURBATIONS: <15%.
SOURCE IMPEDANCE: Unterminated current source.

GENERAL
PRICE: HP Model 1925A, **$850.00.**

MANUFACTURING DIVISION: COLORADO SPRINGS DIVISION
1900 Garden of the Gods Road
Colorado Springs, Colorado 80907

Frequency-Domain Oscilloscope Now Measures to 1250 MHz

With this new RF plug-in, HP's absolutely calibrated RF spectrum analyzer can display any part of the frequency range from 500 kHz to 1250 MHz — or the whole range at once.

By Siegfried Linkwitz

DESIGNERS OF BROADCAST, COMMUNICATIONS, NAVIGATION, and other electronic equipment operating in the frequency range from 500 kHz to 1250 MHz can now make absolutely calibrated frequency-domain measurements with a spectrum analyzer as easily as they have always made lower-frequency time-domain measurements with an oscilloscope. The instrument that makes this possible consists of a Display Section (Model 140S, 141S, or 143S), a plug-in IF section (Model 8552A), and a plug-in RF section, the new 0.5 to 1250 MHz Model 8554L (Fig. 1). Although it's a spectrum analyzer, this instrument has many of the qualities that have made the oscilloscope such a universal instrument. It has absolute calibration on both horizontal and vertical axes, it's easy to operate, it gives unambiguous spurious-free displays, and it has high stability and sensitivity. Because it has these qualities, it is beginning to acquire the name *frequency-domain oscilloscope.**

The new Model 8554L is the second spectrum analyzer RF Section to be designed for the same display sections. The display sections, the IF plug-in, and the first RF plug-in, a 1 kHz to 110 MHz instrument, were described in these pages in August 1968.[1],[2] Also described at that time were many of the frequency-domain measurements that the new spectrum analyzer can make. They include such traditional spectrum-analyzer measurements as spectrum surveillance and EMI testing, measuring pulse spectra, and checking multichannel communications systems. More important, however, are the measurements the new analyzer can make in general RF circuit design. For example, it can measure the flatness, harmonic content, and spectral purity of oscillators; it can measure AM and FM modulation indexes; it can measure gain, frequency response, harmonic and inter-

Fig. 1. *A new plug-in RF section makes this a 0.5-to-1250-MHz spectrum analyzer — or frequency-domain oscilloscope, if you prefer. It has absolute amplitude calibration, automatic phase lock, and simple controls. Its frequency response is flat within ±1 dB from 1 to 1000 MHz. It has a 60 dB spurious free display range, −120 dBm maximum sensitivity, and scan widths from 20 kHz to 1250 MHz. Variable-persistence and large-screen displays are optional.*

* See page 16 for more about frequency-domain oscilloscopes.

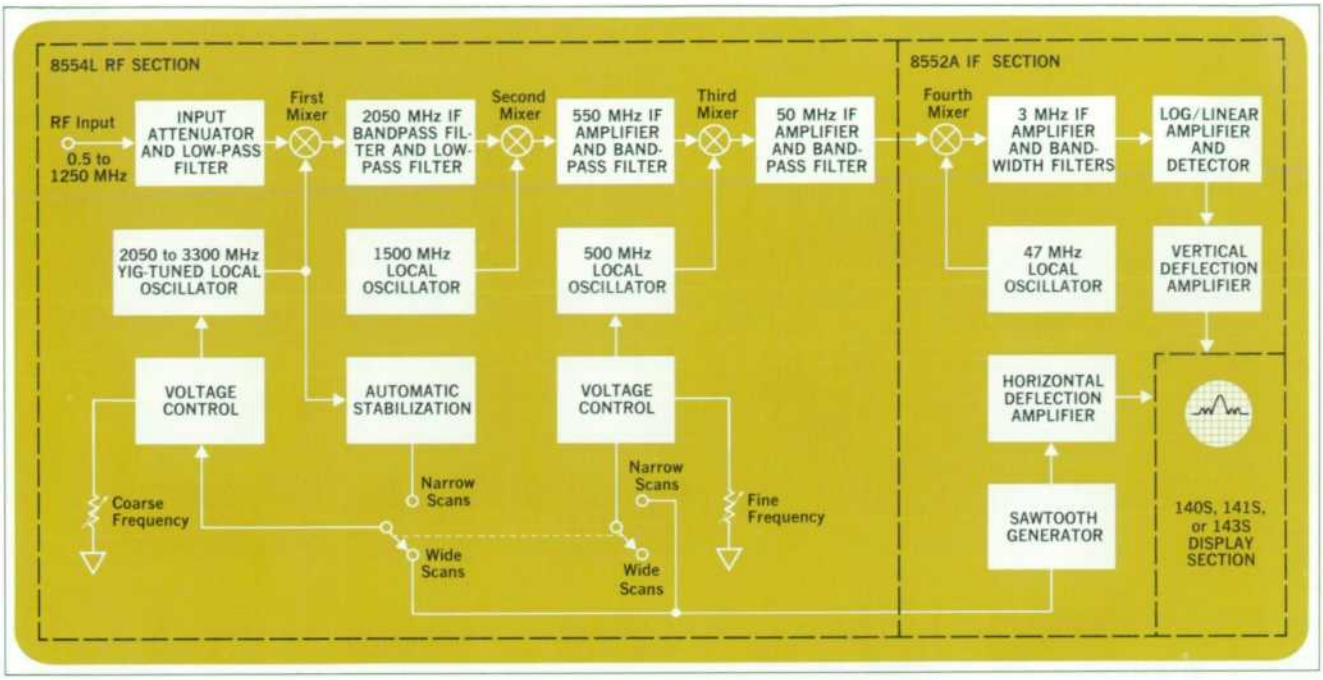


Fig. 2. *A quadruple conversion process, plus low-pass input and IF filters, keep spurious responses off the display. For wide scan widths the YIG-tuned first LO is swept. For narrow scan widths the third LO is swept and the first LO is phase-locked to a stable reference to reduce residual FM to less than 300 Hz.*

modulation distortion, and parasitic oscillations in amplifiers; it can measure mixer conversion loss and local-oscillator suppression in balanced mixers. The new RF section extends all these measurements to 1250 MHz. A few examples of its use are described on page 18.

Analytical Capabilities

One of the new spectrum analyzer's most powerful capabilities is its scanning versatility. It can display the full spectrum from 0 to 1250 MHz, or any part of it. When set for the 1250-MHz scan, a marker pip appears on the display at the frequency to which the analyzer is tuned. The pip points downwards to distinguish it from a signal. When the analyzer is switched to any of its ten narrower scan widths, the scan is symmetrical about the marker frequency. The narrowest scan width is 20 kHz, and the widest symmetrical scan width is 1000 MHz. Alternatively, scanning can be halted and the analyzer can be operated as a sensitive manually tuned receiver with variable bandwidth.

The analyzer's amplitude scale is absolutely calibrated in dBm and μV. Hence the analyzer doesn't merely display a spectrum; it accurately measures the components of the spectrum. Input signals can be as small as -120 dBm (0.3 μV) or as large as $+10$ dBm (0.8 V). Frequency response is flat within ± 1 dB from 1 MHz to 1000 MHz, and most amplitude measurements can be made to within ± 1.5 dB or better.

Residual responses and harmonic mixing responses are kept off the display by microcircuit filters. This makes it easy to identify signals and to read their frequencies directly on the analyzer's scales. The distortion-free and spurious-free display range is greater than 60 dB.

The analyzer has seven calibrated bandwidths ranging from 300 Hz to 300 kHz. The narrowest bandwidths give high resolution for analyzing signals close together in frequency, and the wider bandwidths allow fast scanning of wide frequency ranges. If the operator selects a bandwidth too narrow for the scan rate, a red light warns him that the display is uncalibrated.

To provide the stability needed to make its narrow bandwidths and narrow scan widths useful the analyzer has a phase-lock system that automatically stabilizes the first local oscillator when a narrow scan width is selected. The phase-lock system reduces residual FM to less than 300 Hz peak-to-peak. The operator doesn't have to manipulate any controls to achieve phase lock.

Advanced technology was needed to get many of the new RF plug-in's capabilities into such a small package. Most noteworthy are its YIG-tuned solid-state first local

oscillator, its microcircuit filters, and the microcircuit sampler in its phase-lock loop.

What's Inside

The new spectrum analyzer is essentially an electronically tuned superheterodyne receiver. The amplitude of the received signal is displayed on the CRT as vertical deflection. The frequency of the receiver is changed in synchronism with the horizontal movement of the electron beam across the CRT. The result is a display of amplitude vs frequency, that is, a display of the spectrum.

The block diagram, Fig. 2, illustrates the operation in detail. The low-pass filter at the analyzer input has a frequency response which is flat to 1300 MHz, down 3 dB at 1500 MHz, and down 70 dB at 2050 MHz. Following the filter, the input mixer and the YIG-tuned solid-state first local oscillator convert the incoming signal to 2050 MHz, the first intermediate frequency. Even signals as low as 500 kHz are transformed to this high frequency. The high first IF and the low-pass input filter eliminate image responses which might otherwise occur for input frequencies from 4000 to 5300 MHz. This is a major

The Meaning of 'Frequency-Domain Oscilloscope'

Excerpts from an informal talk by **Roderick Carlson** of Hewlett-Packard's Microwave Division

"'Frequency-domain oscilloscope' is a term that we at Hewlett-Packard have adopted to describe a certain type of spectrum analyzer. As a name, it's not important; in fact, 'spectrum analyzer' is a much more accurate name than 'oscilloscope'. What is important is the concept behind the name — a new way of thinking *about spectrum analyzers and a new way of* using *them.*

"To deserve the name 'frequency-domain oscilloscope', a spectrum analyzer has to be fully calibrated, like an oscilloscope, and just as easy to use as an oscilloscope. There are now two spectrum analyzers that have evolved this far; they are the 110 MHz instrument described in the August 1968 HP Journal (Model 8552A/8553L), and the new 0.5 to 1250 MHz unit described in the accompanying article (Model 8554L/8552A).

"These fully calibrated, easy-to-use instruments have an area of application that is, quite literally, immense. This application area is general circuit design *— the same area in which the oscilloscope finds most of its applications. The spectrum analyzer is a basic measuring tool for designing oscillators, amplifiers, mixers, modulators, filters and so on. Like a scope or a dc voltmeter, it's a general-purpose, constant-use tool — not a special purpose instrument, but one that has a broad range of uses."*

Usefulness Found by Experience

"We recognized the broad usefulness of the spectrum analyzer through experience in our own laboratories with our microwave spectrum analyzer (Model 851B/8551B). In our laboratories we do much the same kind of circuit design that everyone else does. Our microwave spectrum analyzer was conceived with the classical spectrum-analyzer applications in mind. These are such things as looking at the spectra of radar pulses or looking at the signals in microwave carrier systems. This analyzer was also designed for some new applications, such as spectrum surveillance and radio-frequency-interference measurement. However, as soon as the analyzer was put to use in our laboratories, it became apparent that it was an excellent general-purpose tool for observing the everyday signals we were working with. In fact, it was better than an oscilloscope for most of our purposes. Now we have several of these analyzers and they are in constant use. We wonder how we ever got along without them. To lose them would be like losing one of our senses, like going deaf or going blind.

"Now, oscilloscopes and spectrum analyzers aren't rivals. They complement each other. Each has its own place: the oscilloscope is the instrument for working in the time domain, and the spectrum analyzer is the instrument for working in the frequency domain. When we call a spectrum analyzer a frequency-domain oscilloscope we mean that the spectrum analyzer is exactly analogous to the oscilloscope, but is for the frequency domain, and that the spectrum analyzer has the same general usefulness as the oscilloscope."

Characteristics of FDO's

"Our new spectrum analyzers are designed to be well suited to general circuit-design work, and so are true frequency-domain oscilloscopes. They have several characteristics that other spectrum analyzers don't have. One is absolute amplitude calibration, which allows you to measure signal levels accurately with the spectrum analyzer. Some day all spectrum analyzers will have absolute amplitude calibration—users are going to demand it. Imagine how far you would get with an oscilloscope these days if it didn't have vertical calibration.

"Another characteristic of these frequency-domain oscilloscopes is an easy-to-interpret, unambiguous display. This comes from an input filter which allows the analyzer to have only a single response, thereby avoiding the confusion of images and multiple responses due to harmonic mixing.

"A third characteristic of the new analyzers is a phase-lock system that operates almost automatically, so the operator doesn't even realize that the local oscillator has been stabilized by phase-locking. This is something that in the past has required some skill and a bit of hope on the part of the operator.

"Finally, the new spectrum analyzers are much smaller in size and lower in cost than are many older analyzers."

Frequency-Domain Measurements

"Very few of the frequency-domain measurements that can be made with the spectrum analyzer are new. Nearly all are very familiar. They just haven't been made with spectrum analyzers in the past. What engineers need to realize now is that the spectrum analyzer has evolved to a point where it is the most convenient and accurate instrument available for making these measurements. In many cases, with a fully calibrated spectrum analyzer on his bench a design engineer doesn't need an RF voltmeter, or a power meter, or a wave analyzer, or a distortion meter, or a swept-frequency indicator. What's more, he can make much more eye-opening measurements with his spectrum analyzer than he can with a collection of these other instruments."

factor in keeping the display free of spurious signals.

To get narrow analyzing bandwidths, it is necessary to convert to a lower intermediate frequency. This is done in 3 steps, to avoid undesired image responses. A 1500 MHz fixed-frequency transistor oscillator and a second mixer convert the 2050 MHz first IF signal to a 550 MHz signal, the second IF. The signal has so far undergone two conversions and is now amplified for the first time in a 550 MHz amplifier.

After further mixing with a 500 MHz third-local-oscillator signal, followed by amplification of the resulting 50 MHz IF signal and mixing with a 47 MHz fourth-local-oscillator signal, the final 3 MHz IF is obtained. It is at this last frequency that the bandwidth is narrowed to seven calibrated bandwidths between 300 kHz and 300 Hz, one of which is selected by the user. Finally, the 3 MHz signal is amplified by a logarithmic amplifier which has a dynamic range of 70 dB, and the amplifier output is detected to produce the video signal which is applied to the vertical deflection circuits of the CRT.

The horizontal deflection of the electron beam of the CRT is controlled by a sawtooth generator. The same sawtooth generator causes the analyzer's frequency to scan, centered on the value set by the coarse frequency tuning control and indicated on the slide-rule dial on the front panel. For scan widths of 1250 MHz to 5 MHz, the first local oscillator is swept. For narrower scan widths, the sawtooth voltage is removed from the first LO and applied to the third LO. The bandwidth of the IF stages preceding the third mixer is sufficiently wide to allow for the maximum tuning range of the third LO. When the third LO is being swept, the first LO is automatically phase-lock stabilized to a constant reference frequency, and acts strictly as an up-converter. Narrow-band frequency tuning and scanning are accomplished with the third LO. Stepping the scanning operation between the first LO and the third LO gives in one instrument the advantages of both very wide scans and very stable narrow-band scans.

YIG-Tuned Solid-State First LO

The YIG-tuned solid-state first local oscillator made it possible to get the new RF plug-in into the required small package. This oscillator is not only smaller, but also far superior in frequency stability and tuning linearity to previously used backward-wave-tube oscillators. The tuning element is a highly polished 0.035 inch diameter sphere of Yttrium-Iron-Garnet, a ferrite material. Its electrical equivalent is a parallel tuned circuit of low loss. The resonance frequency of the YIG is a linear function

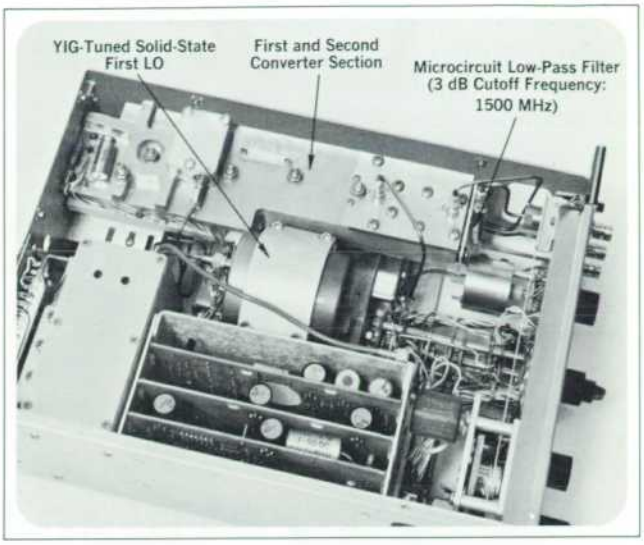


Fig. 3. *Four hybrid microcircuits are used in the new RF plug-in. One is the YIG-tuned transistor first local oscillator, two are low-pass filters (one is hidden under the first and second converter section), and the fourth is a sampler in the phase-lock system (see Fig. 5).*

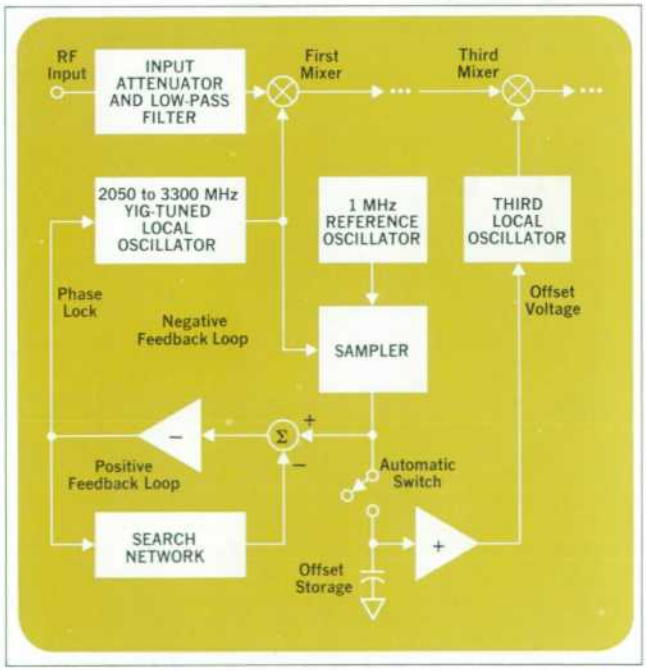


Fig. 4. *When the analyzer is switched to stabilized operation and the phase-lock system is unlocked, the positive feedback loop oscillates at a rate of about 5 Hz, tuning the YIG oscillator until its frequency is equal to a harmonic of 1 MHz. Then, with the sampler acting as a phase detector, the negative feedback loop takes over to keep the YIG oscillator phase-locked to the reference oscillator. The offset voltage to the third LO keeps the display from shifting when phase-lock occurs.*

of the strength of the magnetic field applied to it.

The YIG sphere is mounted between the pole pieces of an electromagnet and the magnet current controls the first LO frequency, to the degree with which the magnetic field follows this current. By careful selection of the magnet material, excellent tuning linearity and small hysteresis were obtained over the range from 2000 to 3300 MHz. The oscillator's center frequency is always within 10 MHz of the front-panel dial setting, and the frequency error between any two points on the display is less than 10% of the indicated separation.

A loop around the YIG sphere forms the RF coupling to a single-transistor oscillator. The oscillator is followed by two stages of power amplification, which act as a buffer against variations in the load on the oscillator, which could otherwise pull the frequency.

The magnet/YIG combination has high tuning sensitivity (20 kHz/μA), so an extremely low-noise-current power supply had to be designed for the magnet. Careful magnetic shielding against extraneous fields was also required to maintain spectral purity, since the frequency depends on magnetic field strength. In the final design, residual FM is less than 10 kHz peak to peak without phase-lock stabilization.

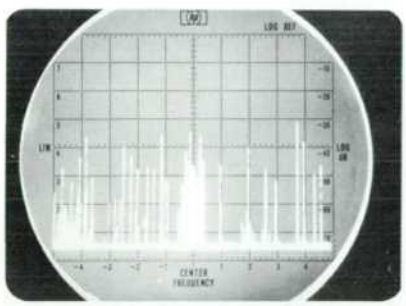
Beyond Traditional Spectrum Analyzer Uses

Absolute calibration, ease of use, freedom from spurious responses, and automatic stabilization—characteristics that qualify the new 1250 MHz Spectrum Analyzer as a frequency-domain oscilloscope — obviously give it substantially greater analytical capabilities than older spectrum analyzers in the same applications. But a frequency-domain oscilloscope isn't limited to such traditional areas as radar, communications, and EMI measurements. It's a general-purpose design tool, useful for measurements on oscillators, modulators, mixers, amplifiers, and filters. Shown here are a few measurements made with the new analyzer.

Three main-frame Display Sections will accept the 1250 MHz Model 8554L RF Section. Model 140S is the basic mainframe; it has a 5 inch internal-graticule CRT with a normal-persistence P11 phosphor. Model 141S has the additional advantages of variable persistence and storage; these features are useful for measuring intermittent signals, for comparing signals before and after adjustments, and for making high-resolution measurements at low sweep speeds where flicker might otherwise be a problem. The third main-frame, Model 143S, has a large 8 by 10 inch display, useful in production areas or classrooms.

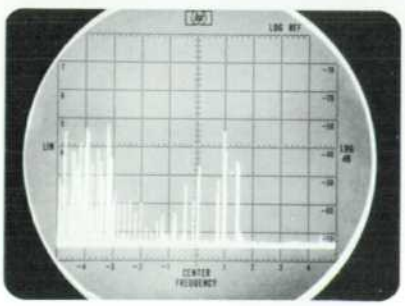
1. SPECTRUM SURVEILLANCE

Signal spectrum observed at Palo Alto, California with a single-turn 16" x 24" loop antenna
Vertical scale (amplitude): Logarithmic, −20 dBm to −90 dBm, 10 dB/division, reference −20 dBm.

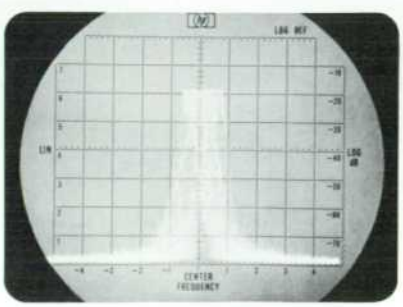


0 to 200 MHz Band at 20 MHz/division
Note FM band at center screen, TV Channels 2, 4, 5, 7, and 9 all clearly visible

2. MEASURING RESIDUAL FM



0 to 1000 MHz Band at 100 MHz/division
In addition to FM and VHF-TV channels, note UHF Channel 36 at 600 MHz, and other signals.

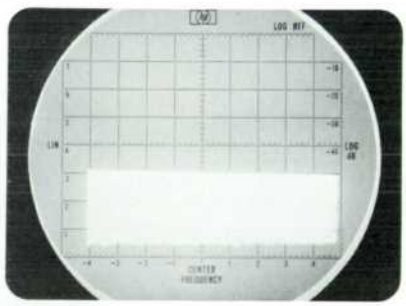


Center frequency = 300 MHz
Horizontal scale (frequency) = 20 kHz/division, thus FM deviation = 30 kHz.

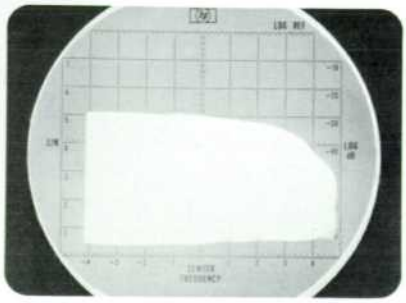
3. NETWORK CHARACTERIZATION

Measuring Gain and Frequency Response of an Amplifier

Horizontal scale (frequency): 0–1000 MHz, 100 MHz/division.
Vertical scale (amplitude): Logarithmic, +10 dBm to −60 dBm, 10 dB/division, reference +10 dBm.



Swept Source Directly Into Analyzer



Amplifier Output
Gain = 20 dB, −3 dB point = 700 MHz

Thin-film microcircuit technology, computer-aided design, and the ability to accurately characterize microwave devices by scattering parameters were key factors in the development of the YIG oscillator circuitry. The oscillator and amplifier are small enough that they can be mounted together with the YIG sphere in the 0.10 inch gap between the pole pieces of the driving magnet. The entire oscillator, including magnets, is in a package just 2 inches high and 2.5 inches in diameter (Fig. 3).

Microcircuit Filters

The input low-pass filter, which helps establish the 60 dB spurious-response-free display range of the new RF plug-in, and the low-pass filter in the first IF, which rejects undesired mixing products, were designed using thin-film circuit elements. These filters operate in the microwave region and exhibit excellent attenuation characteristics in their stop bands, a result of the small physical size of the filter elements in relation to the wavelength at which they are used. Because of their size, individual capacitors and inductors in the filter can be characterized as discrete rather than distributed elements. A computerized synthesis procedure determines the actual dimensions and the layout for the plating masks. Element losses are taken into account so filters with sharp cutoffs in their attenuation characteristics can be realized.

Both filters are thirteen-element, thirteen-pole Tschebyscheff low-pass filters. The input filter has a 3 dB cutoff frequency of 1500 MHz and has more than 70 dB rejection in its stop band from 2050 MHz through 12 GHz. It is 2 inches long and 0.25 inch in diameter. The filter in the first IF has a cutoff frequency of 5.0 GHz and has 70 dB rejection through 20 GHz. Its dimensions are 0.7 by 0.1 by 0.04 inch.

Sampling Phase-Lock System

The resolution which can be obtained in any spectrum analyzer is limited by the bandwidths and shape factors of the IF filters and by the stability of the local oscillators which are used to frequency-translate the input signal. In practice the limitation is set by oscillator stability, which in turn determines the narrowest usable filter bandwidths.

One way to improve the stability of an oscillator is to phase-lock it to a stable reference frequency. This approach has been widely used in spectrum analyzers, but it has always required some effort from the operator in setting up the instrument. In the new RF plug-in, phase-locking of the first local oscillator (YIG) occurs automatically for narrow scan widths and does not require operator intervention.

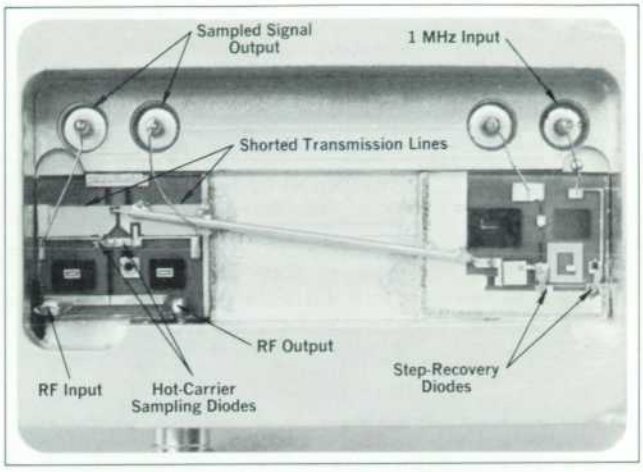


Fig. 5. *This balanced, two-diode hybrid-microcircuit sampler acts as a phase detector in the automatic phase-lock system of the Model 8554L RF Section. The reference signal, a 1 MHz square wave, drives the two step-recovery-diode stages to produce voltage steps with very fast risetimes. The balanced configuration of shorted transmission lines then differentiates this waveform and the resulting narrow pulses switch the two hot carrier diodes on and off to sample the voltage from the YIG oscillator.*

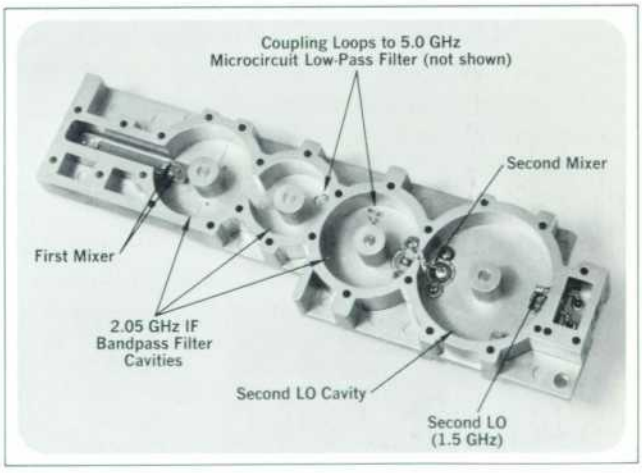


Fig. 6. *To get flat frequency response in the first mixer, the two hot carrier mixer diodes (it's a balanced mixer) are mounted so their packages and leads are part of the mixer operation and don't contribute parasitic effects. The two diodes are inductively coupled to the stripline from the first LO and to the first IF filter cavity. A similar technique is used in the second mixer.*

The phase-lock system is shown in Fig. 4. An important part of the system is a balanced, two-diode microcircuit sampler which produces a voltage proportional to the phase difference between the YIG oscillator output signal and the reference oscillator output signal. Fig. 5 is a photograph of the sampler.

SPECIFICATIONS

HP Model 8554L/8552A
Spectrum Analyzer

FREQUENCY
FREQUENCY RANGE: 500 kHz–1250 MHz
SCAN WIDTH: (on 10 division CRT horizontal axis)
Per Division: 15 calibrated scan widths from 100 MHz/div to 2 kHz/div in 1, 2, 5 sequence.
Preset: 0–1250 MHz
Zero: Analyzer is fixed-tuned receiver.
FREQUENCY ACCURACY:
Center Frequency Accuracy: The dial indicates the display center frequency within 10 MHz.
Scan Linearity: Frequency error between two points on the display is less than 10% of the indicated separation.
RESOLUTION:
IF Bandwidth: Bandwidths of 0.3 to 300 kHz provided in a 1, 3 sequence
IF Bandwidth Accuracy: Individual bandwidths' 3 dB points calibrated to ±20% (10 kHz bandwidth ±5%).
IF Bandwidth Selectivity: 60 dB/3 dB bandwidth ratio <20:1 for IF bandwidths from 1 kHz to 300 kHz, 60 dB/3 dB bandwidth ratio <25:1 for 300 Hz IF bandwidth.

STABILITY:
Residual FM:
Stabilized: <300 Hz peak-to-peak.
Unstabilized: <10 kHz peak-to-peak.
Noise Sidebands: More than 60 dB below CW signal, 20 kHz or more away from signal, for 1 kHz bandwidth.

AMPLITUDE
ABSOLUTE AMPLITUDE CALIBRATION RANGE:
LOG: From −120 to +10 dBm, 10 dB/div on a 70 dB display.
LIN: From 0.1 μV/div to 100 mV/div in a 1, 2 sequence on an 8 division display.
DYNAMIC RANGE:
Average Noise Level: < −102 dBm with 10 kHz IF bandwidth.
Spurious Responses: For −40 dBm signal level to the input mixer*, image responses, out of band mixing responses, harmonic and intermodulation distortion are all more than 60 dB below the input signal level.
Residual Responses: < −100 dBm.

* Signal level to input mixers = signal level at input − input RF attenuation.

AMPLITUDE ACCURACY:	LOG	LINEAR
Frequency Response (Flatness):		
(1 MHz to 1.0 GHz)	±1 dB	±12%
(500 kHz to 1.25 GHz)	±2 dB	
Switching between Bandwidths: (At 20°C)	±0.5 dB	±5.8%
Amplitude Display:	±0.25 dB/dB but not more than ±1.5 dB over the full 70 dB display range.	±2.8% of full 8 div deflection

Calibrator Output: Amplitude −30 dBm, ±0.3 dB
Frequency 30 MHz, ±0.3 MHz

INPUT SPECIFICATIONS:
Input Impedance: 50 Ω nominal. Reflection coefficient <0.30 (Return loss >10.5 dB).
Maximum Input Level: Peak or average power +13 dBm (1.4 Vac peak, ±50 Vdc).

SCAN TIME SPECIFICATIONS:
Scan Time: 16 internal scan rates from 0.1 ms/div to 10 s/div in a 1, 2, 5 sequence.
Scan Time Accuracy:
0.1 ms/div to 20 ms/div ±10%
50 ms/div to 10 s/div ±20%

PRICES:

Model 8554L RF Section	$3300.00
Model 8552A IF Section	$1900.00
Model 140S Display Section	$ 725.00
Model 141S Display Section	$1525.00

MANUFACTURING DIVISION: HP MICROWAVE DIVISION
1501 Page Mill Road
Palo Alto, California 94304

First and Second Converters

In an absolutely calibrated spectrum analyzer, the frequency response of the input mixer is very important. The responses of the other mixers, amplifiers, and filters in the signal path have an effect only at fixed frequencies or over very narrow bandwidths. The input mixer, however, is broadband, so its response largely determines the instrument's accuracy. The input mixer in the new RF plug-in is a balanced mixer mounted inside the coaxial cavity of the 2050 MHz first IF bandpass filter. Two standard hot carrier diodes in glass packages mounted on a printed circuit board are inductively coupled to the IF cavity and to a balanced stripline which carries the first-local-oscillator signal (Fig. 6). Thus the diode packages and their leads are used as part of the mixer operation to avoid parasitic effects.

A similar technique is used for the second mixer, which uses a single hot carrier diode. The diode is mounted in the wall between the IF filter cavity and the second LO cavity. It couples to the second LO cavity with one lead and to the IF filter cavity with its other lead.

Acknowledgments

Merely to list all those who worked with me on the design of the Model 8554L RF Section doesn't do justice to their efforts and dedication. However, even a list of those who contributed their talents at various stages of the project would be quite long. It would include *Harley L. Halverson,* who was project leader during the early phases, *Richard C. Keiter* and *James C. Harmon,* who designed the first and second converters, *John J. Dupre,* who designed the YIG oscillator, *Fendall G. Winston,* who designed the sampler and phase-lock system, *William Swift* and *Melvin D. Humpherys,* who designed the third converter, *John E. Nidecker* and *Fred H. Meyers,* who did the product design, and many others, particularly *Roderick Carlson,* who guided the project through several critical phases.

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[1]. Brian D. Unter, 'Fully Calibrated Frequency-Domain Measurements,' **Hewlett-Packard Journal,** August 1968.
[2]. Thomas L. Grisell, Irving H. Hawley, Jr., Brian D. Unter, and Paul G. Winninghoff, 'Design of a Third-Generation RF Spectrum Analyzer,' **Hewlett-Packard Journal,** August 1968.

Siegfried Linkwitz

Curiosity about the possible course of human development, which he shares with many other contemporary scientists and engineers, has caused Siegfried Linkwitz to give much of his leisure time to social and psychological studies. One aspect of this activity has been to lead encounter groups concerned with human potential.

Siegfried attended the Technische Hochschule in Darmstadt, Germany, where he received his Diplom Ingenieur in 1961. He joined Hewlett-Packard in the same year and worked on the design of several instruments and systems before becoming project manager for the 8554L. A member of IEEE, Siegfried has taken some graduate courses at Stanford and holds one patent.

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