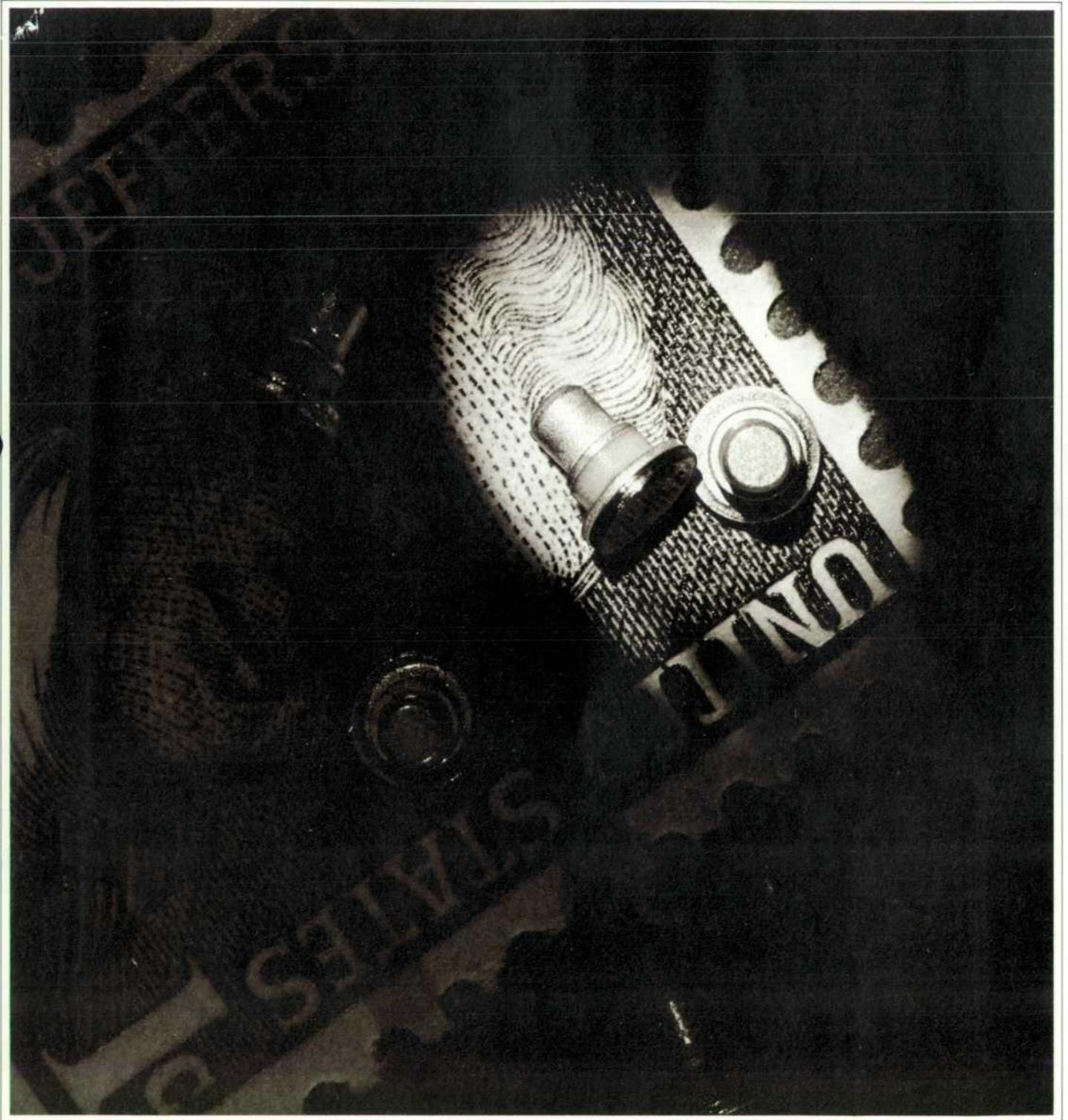# HEWLETT-PACKARD JOURNAL

MAY 1970

Design and Application of Silicon IMPATT Diodes

DC power is converted directly into microwave energy by an IMPATT diode. In X-band, these devices generate higher CW power than any other present-day, solid-state microwave source, clearing the way for new cost-sensitive microwave designs.

By A. M. Cowley

MICROWAVE POWER GENERATION has been the last major holdout against the solid-state revolution. The smaller size, longer life, and lower power consumption of solid-state circuits could make a host of startling developments possible but, just as vacuum tube designers reached a frequency ceiling with grid-controlled vacuum tubes, solid-state designers are faced with an apparent limit to the capabilities of transistors. Yet, just as vacuum-tube designers succeeded in generating microwave power using new concepts in electron beam control, solid-state designers are now generating microwaves by taking advantage of certain ways charge carriers behave in semiconductors.

One technique for solid-state generation of microwave energy was suggested a dozen years ago by W. T. Read of the Bell Telephone Laboratories.[1] Read proposed that the finite delay between an applied voltage and the current generated by avalanche breakdown in a specially-designed PN junction device, plus the transit delay as the charge carriers travel through the diode,[2] could amount to a total delay of 180° at microwave frequencies. Such a mechanism would thus contribute power to an external circuit.

Practical realization of a "Read" diode, however, was not achieved until seven years later[3] despite the fact that Read presented a complete and basically correct analysis of the device. The problem was largely thermal: how to remove the heat generated in the device. Since microwave applications require very small devices for practical impedance levels, and since operation in avalanche breakdown at the required current densities means extremely high power densities — as much as 10^8 *watts per cubic centimeter* —, a method had to be found to extract large quantities of heat efficiently to prevent destructively high temperatures.

A successful thermal design was achieved by inverting a mesa-type PN junction diode and bonding the top of the mesa with heat and pressure directly to a gold-plated copper heat sink, as shown in Fig. 1 (solder wouldn't do here because of its thermal resistance). When all the variables in the thermal-compression bonding process are at the optimum, thermal resistances low enough to permit continuous microwave oscillations are obtained.

Cover: *Scarcely an eighth of an inch long, IMPATT diodes generate more than one-half watt of microwave power in X band (8–12.4 GHz) when imbedded in a resonant circuit supplied with dc power. The article beginning on this page explains the why's and wherefore's of these mighty Lilliputians.*
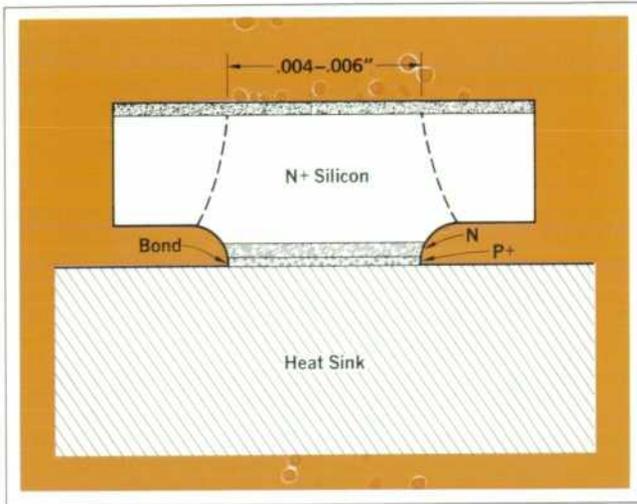
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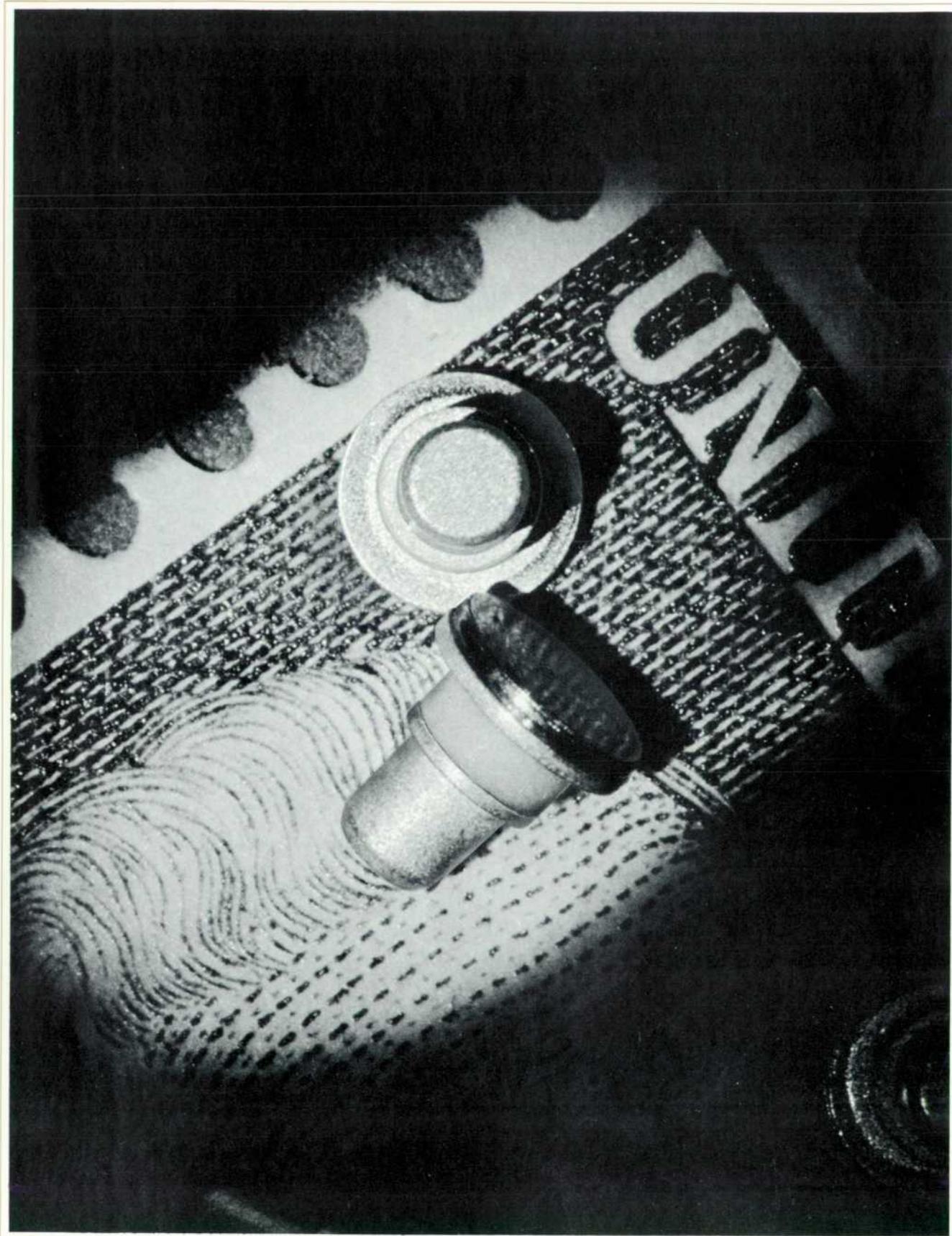
Fig. 1. *IMPATT diode formed on silicon substrate and thermal-compression bonded to metal heat sink. Dotted lines show shape, mechanically more stable but harder to handle, obtained by etching from both sides of wafer. Dimensions apply to X-band diodes.*

Thermal-compression bonding, though, takes more time than conventional techniques (e.g., soldering) and it requires extreme care to produce an adequate and reproducible bond. In a search for a less expensive and more consistent means of constructing an adequate thermal path, members of the development team at the HP Associates Division of Hewlett-Packard developed a means of electroplating a heat sink on the junction side of a wafer, and then etching mesa diodes directly on the heat sink,[4] as shown in Fig. 2.* Because the integral heat sink diffuses the diode heat over a relatively wide area, the individual diodes can then be soldered into a package or circuit by conventional techniques.

Thermal resistances typically between 14 and 17°C/W are obtained in Hewlett-Packard's X-band diodes made this way. Power output for the two types of HP diodes are shown in Fig. 3. A typical diode can generate 700 mW at 10 GHz with 6.5% efficiency at a junction temperature of about 200°C. One watt output can be obtained at a junction temperature of 250 to 260°C. Since burnout does not occur until a junction temperature of 350°C is reached, there is a large margin for safety (until extensive reliability studies are completed, however, conservative operation at junction temperatures below 200°C is recommended).

The new HP diodes, in common with most avalanche diodes intended for microwave oscillators, use a simple PN junction in a three-layer P+NN+ structure rather than

* This method was proposed independently by Bernd Hoefflinger (see reference [5]).

the special four-layer N+PIP+ structure proposed by Read. The three-layer structure has all the microwave oscillation properties of the four-layer structure but is easier to make. Both of these devices are called IMPATT diodes, an acronym derived from IMPact ionization and Avalanche Transit Time.

Among the important benefits added by the integral heat-sink construction technique are a reduction in fabrication costs and a significant improvement in uniformity from diode to diode. Also, since the PN junction is at the wide base of the mesa, rather than at the narrow top, the slope of the mesa sides reduces the electric field at the junction periphery, lowering the chances of premature edge breakdown. Furthermore, the diodes can be passivated by conventional dielectric deposition techniques while still in wafer form.

HP IMPATT diodes made with integral heat sinks are currently priced at $150 each in sample quantities, as compared to the $200–$300 price range of earlier IMPATT's. There is every reason to believe that the price will go down substantially as both demand and production rates for these diodes grow.

Hence, the era of solid-state microwave systems is upon us. IMPATT diodes, presently the highest power solid-state source of CW microwave power in X-band, are already being designed into airborne Doppler navigation radars, point-to-point microwave communications links, and airborne phased array radars. Besides making
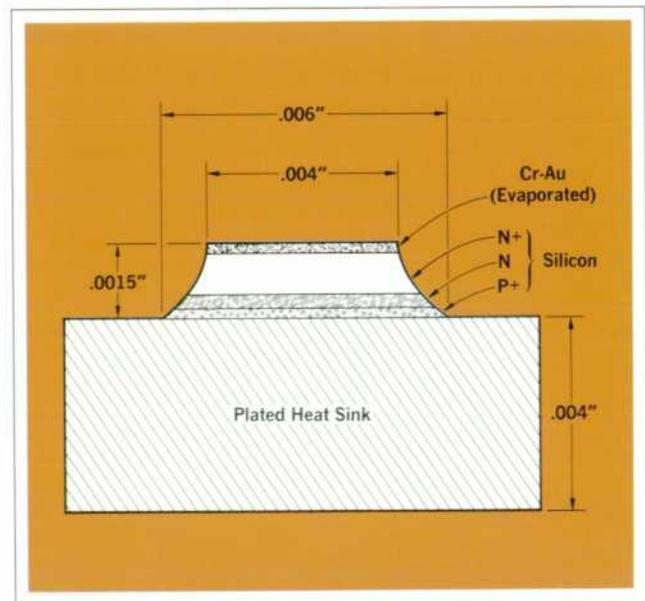

Fig. 2. *Integral heat sink serves as wafer substrate during manufacture of new HP IMPATT diodes. Chips can be soldered into circuit or package without seriously degrading thermal properties.*
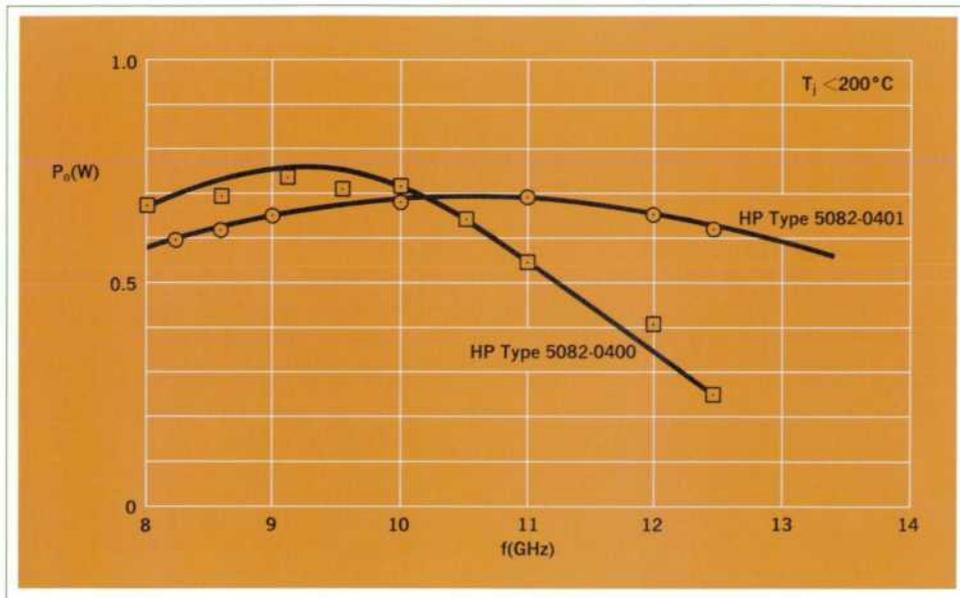
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Fig. 3. *Typical performance of HP IMPATT diodes in X-band. Two types are currently offered.*

possible some rather complex microwave systems, the IMPATT diodes will also contribute to low-cost, compact systems like radar transponders, navigation beacons, collision avoidance systems, disposable ECM jammers, fuses, automobile radar braking systems, and intrusion alarms.

Theory

To provide insight into IMPATT diode performance in preference to exact quantitative design theory, several simplifying assumptions are made in the description of diode operation presented in this section. The basic theory was well described by Read in his original paper[1] and more recently Sze[6] and deLoach[7] have reviewed the theory in the light of experimental results.

A diagram representing a three-layer P^+NN^+ diode is shown in Fig. 4. The diode is represented as biased into reverse breakdown, which gives rise to a positively charged depletion layer that has a triangular field distribution, the field maximum being at the PN junction. Breakdown occurs when the electric field is so high that an electron or hole entering the depletion region has a significant probability of ionizing a hole-electron pair. If, on the average, each carrier in the depletion region produces just *one* new hole-electron pair, a sustained avalanche can exist, in much the same way an electrical discharge occurs in a gas. The diode can thus support any dc current with essentially a constant voltage V_{bd}, the breakdown voltage.

The probability of ionization is a strongly *increasing*

function of the electric field. For this reason, charge generation in a diode biased into breakdown tends to be localized near the P^+N junction, i.e., in the region of highest electric field. In an abrupt silicon P^+N junction, this region, known as the avalanche zone (W_a in the diagram), is about 25% of the total depletion layer width. The remainder of the depletion layer is the drift zone, shown as W_d.

When the diode is operating, charge is generated throughout the avalanche zone. Under the influence of the high electric field, the charge drifts to the N^+ end of the depletion region at constant velocity. It is characteristic of this mechanism that the charge velocity is independent of electric field levels above $2 \times 10^4 V/cm$; under typical IMPATT operating conditions, the field is higher than this over most of the depletion region. The resulting charge velocity, known as the saturated velocity, v_{sat}, is about $10^7 cm/s$ for electrons in silicon.

Since diode operation involves the time delay in the avalanche process, we need to consider how charge builds up in response to an applied voltage. From analysis of charge build-up in a thin avalanche zone in a diode biased with a dc voltage just equal to the breakdown voltage V_{bd}, and with a sinusoidal microwave voltage superimposed, Read arrived at an approximation that shows a sharp pulse occurring just as the total diode voltage drops below the breakdown level, as shown in Fig. 5. The charge pulse occurs in the avalanche region and as the charge moves across the drift zone, it generates a rectangular current waveform in the external circuit. The
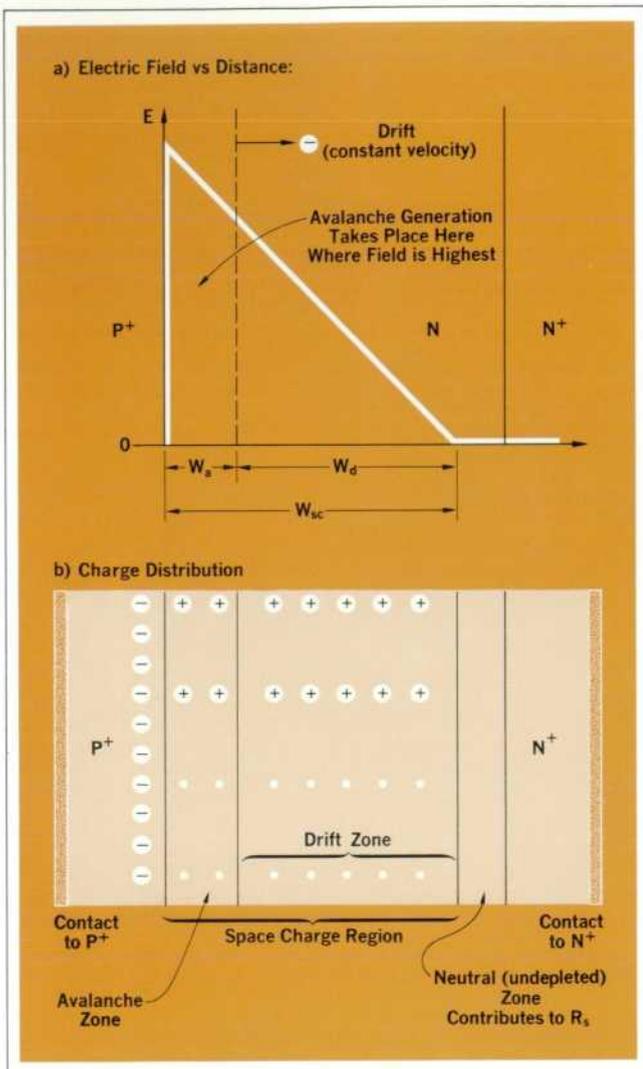
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a) Electric Field vs Distance:

b) Charge Distribution

Fig. 4. *Representation of diode with abrupt P⁺NN⁺ junction reverse-biased in avalanche breakdown. Avalanche is generated in W_A region where electric field is highest. Charge carriers move at constant velocity through drift region W_d. W_{sc} is total space charge region.*

quency, as explained above. In practice, this is done by careful control of the resistivity and consequently the breakdown voltage of the N-type layer. The N-type region, however, should not be much thicker than required to support the depletion layer at breakdown, since "undepleted" material contributes to series resistance.

When epitaxial wafer requirements are met, the remaining parameter to be controlled is junction area, since it determines the operating or depletion capacitance, C_d, of the diode. Depletion capacitance is related to junction area, A, and depletion layer thickness, W_{sc}, by:

$$C_d = \frac{A}{W_{sc}} \, pF$$

where A is in cm² and W_{sc} is in cm.

If W_{sc} were 4×10^{-4}cm (4.0 μm) and A were 2×10^{-4}cm², C_d would be 0.5 pF. In principle, maximum power output is increased as junction area A is made larger, but diode reactance is reduced. Convenience of circuit design usually dictates a capacitance that gives a reactance around 20 to 30 ohms at the operating frequency.
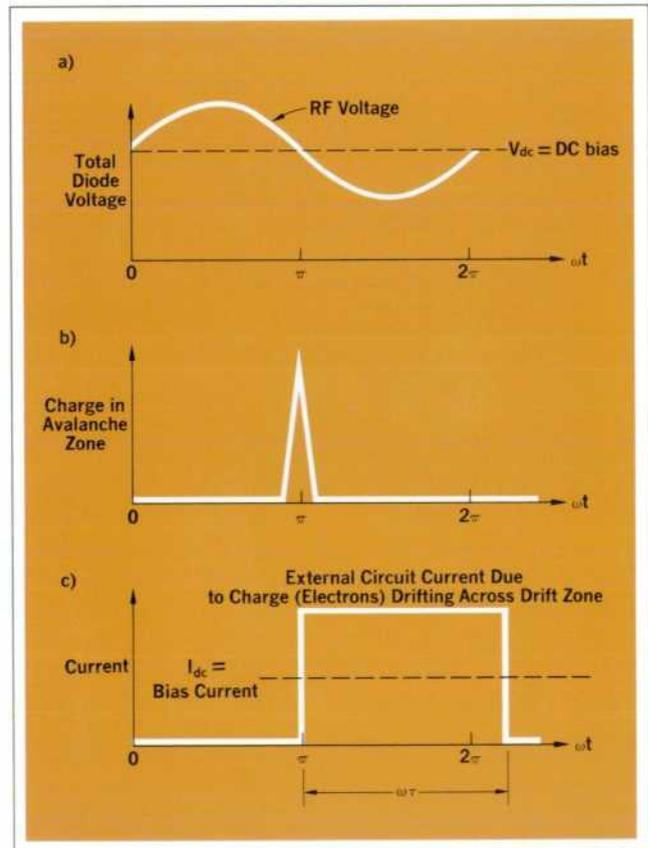

Fig. 5. *Charge builds up in avalanche zone just as microwave voltage falls below breakdown level. Movement of charge across drift zone causes rectangular current waveform in external circuit.*

duration of the external current waveform is determined by the time τ required by the charge to move across the drift zone, and is equal to W_d/v_{sat}. If τ equals one-half the ac period, the fundamental Fourier component of the current waveform will be 180° out of phase with the diode voltage. The diode thus delivers ac power to the external circuit or, looking at it from another viewpoint, the diode has *negative resistance* at this frequency.

Diode Design

Fabrication of IMPATT diodes at Hewlett-Packard is described step-by-step in the box on page 8. The wafer is designed so that transit time across the drift region is roughly one-half a period of the desired oscillation fre-
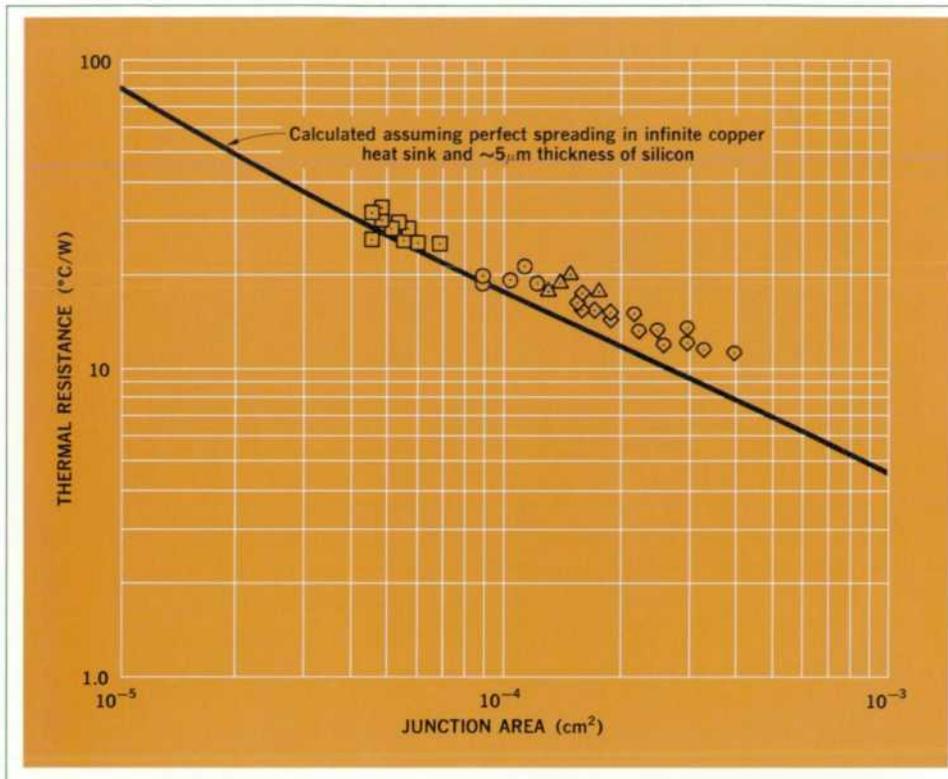
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Fig. 6. *Thermal resistance of HP IMPATT diode vs. junction area. Smaller diodes are closer to ideal than larger ones.*

Thermal resistance of Hewlett-Packard IMPATT diodes was measured using the dc incremental avalanche resistance technique, a variation of a method originally proposed by Haitz[8]. Some typical results are shown in Fig. 6. The solid line represents the ideal — the *best* one can do with a silicon mesa bonded to a copper heat sink. It was calculated from the assumption that the thermal resistance consists of perfect thermal spreading resistance working into a semi-infinite copper heat sink, plus the contribution to thermal resistance of the silicon itself.

The diodes with small junction areas come very close to the ideal. The larger area diodes do not come as close because the solder interface with the package assumes greater importance. For the Hewlett-Packard X-band diodes, which have junction areas around 2×10^{-4} cm², the average measured values of thermal resistance are about 15°C/W, as compared to a calculated value of 12°C/W. More detailed calculations that take into account the solder interface are within a few percent of the measured values.

Silicon vs. GaAs

Use of gallium arsenide (GaAs) for IMPATT's has some potential advantages, among them increased efficiency (23% theoretical maximum vs. 15% for Si[4]), and reduced noise. These advantages are offset somewhat by the significantly greater cost of GaAs, and the relatively
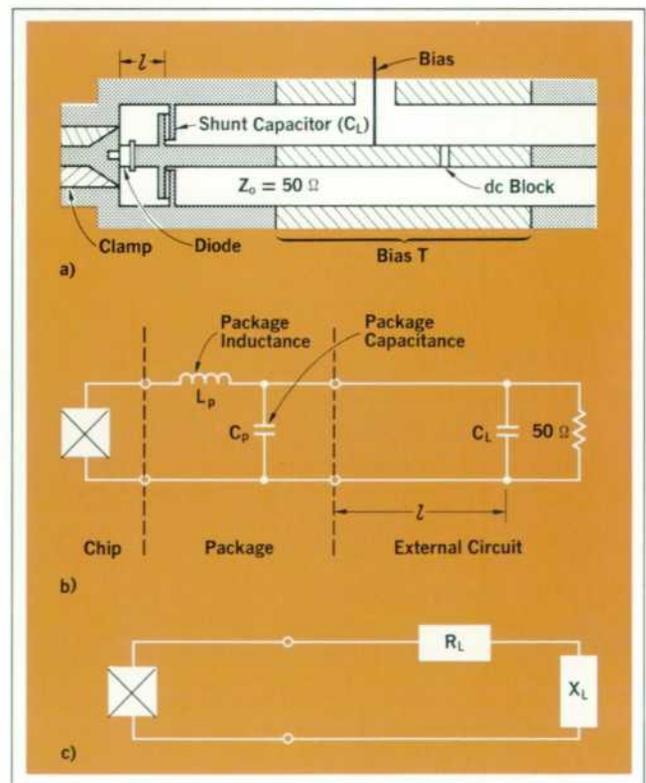

Fig. 7. *Coaxial oscillator circuit designed for IMPATT diode operation in X-band. Adjusting value of shunt capacitor tunes circuit.*
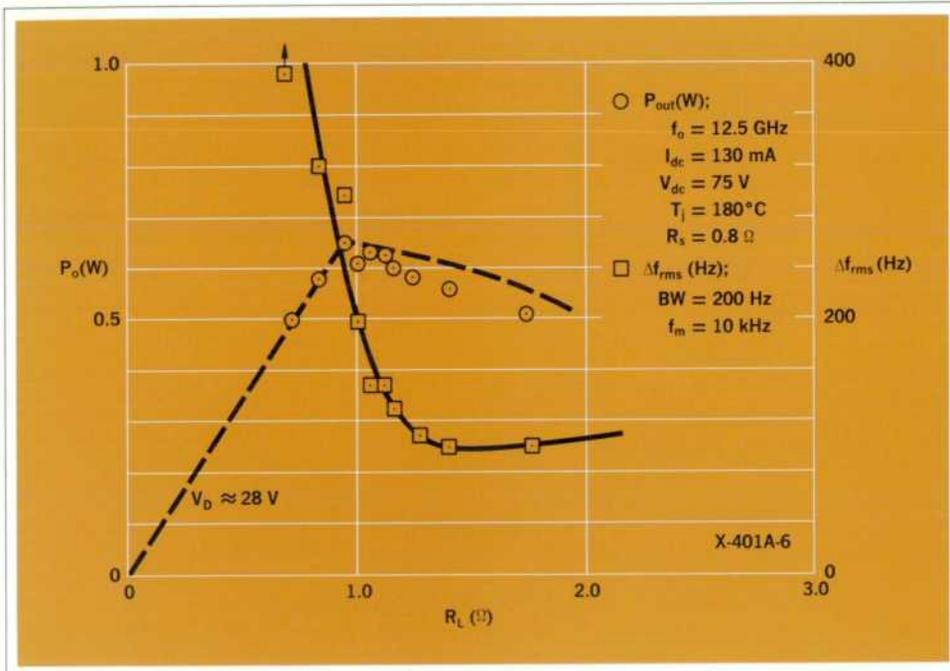
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Fig. 8. *Power output and noise vs. load resistance for two types of IMPATT diodes (f_m is spacing of measured 200-Hz band from oscillator center frequency).*

primitive state of GaAs material and device technology compared to that of Si. It is likely that GaAs IMPATT diodes will find their place in those high-performance applications where greater cost can be tolerated; silicon devices are destined to be inexpensive, and hence will appeal to designers of low-cost, high-volume products.

Making Cool-Running IMPATT Diodes

A. Construction starts with highly-doped N⁺ silicon wafer of low resistivity ($\approx 0.01\ \Omega$ cm). On this, first an N layer ($\rho = 0.5 - 1.0\ \Omega$ cm) and then a P⁺ layer ($\rho = 0.003\ \Omega$ cm) are grown epitaxially. Double epitaxial construction achieves abrupt junction and closely controlled layer widths.

B. Wafer is metallized on junction (P⁺N) side by thin-film techniques. Copper or gold is then electroplated on metallic film to thickness of 0.003 to 0.004 inch.

C. Wafer's other side (N⁺) is thinned mechanically and chemically to reduce wafer thickness to 0.001 to 0.002 inch. This side is then metallized.

D. Standard photoresist techniques are used to etch metal into circular pads and to etch silicon mesas (mesa diameter: 0.006 inch).

E. Wafer is cut apart. Relatively large metal substrate left with each mesa is soldered to copper stud of Hewlett-Packard style 41 microwave package. Gold strap or wire is thermal-compression bonded to top of mesa and to top edge of package. Package interior is then filled with inert gas and, finally, Kovar or steel cap is welded to top, forming hermetic seal.
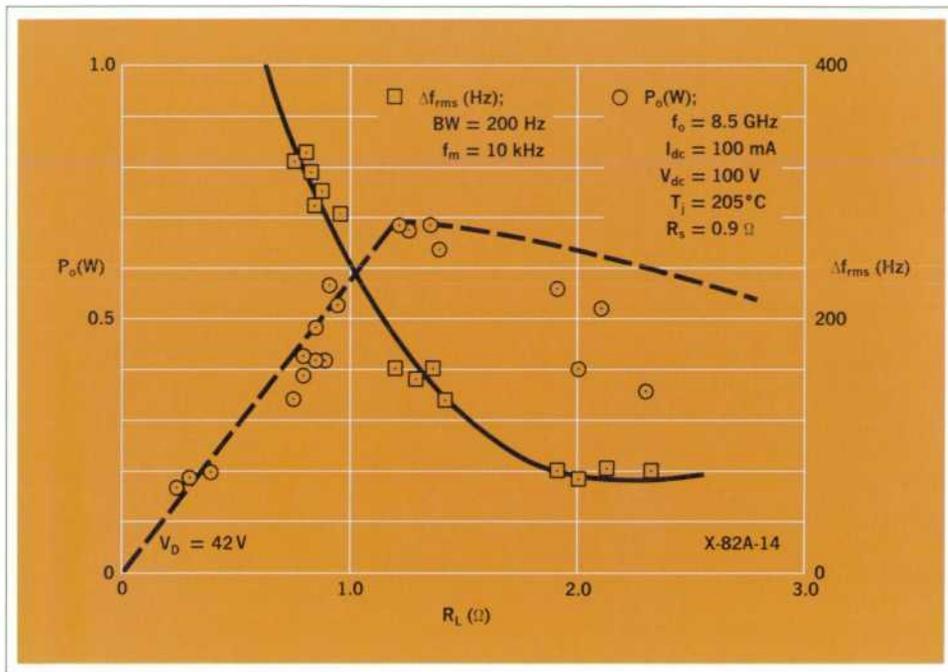

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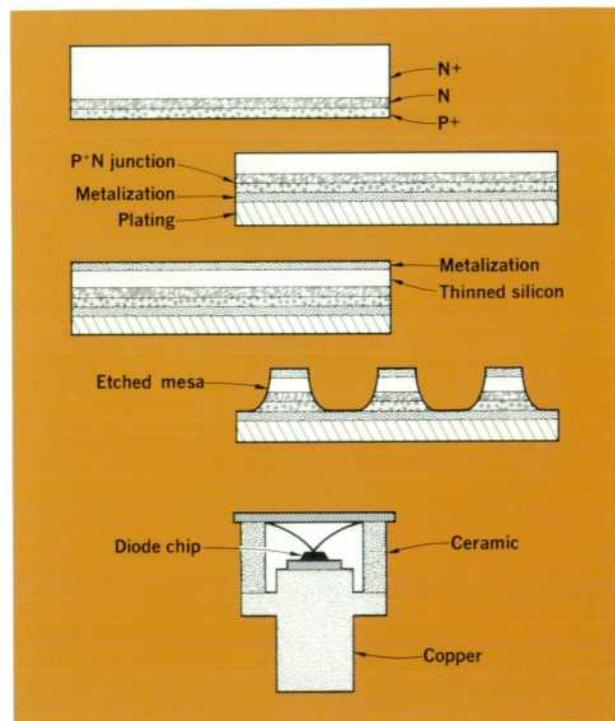
Fig. 8b.

Oscillator Circuit

The oscillator circuit used to obtain results reported here is shown in Fig. 7. It is simply a length of 7 mm coaxial line with the diode mounted at the end in a clamp for good heat sinking. Inductive loading is provided by the diode package inductance and by the length (1) of line between the shorted end and the shunt radial capacitor C_L. This circuit also transforms the 50Ω line impedance to an impedance of 1 to 3 ohms as seen by the diode. The circuit is tuned by inserting appropriate dielectric shims between the two parts of capacitor C_L. To load an X-band diode properly, the value of C_L lies typically between 1 and 3 pF.

The equivalent circuit shown in Fig. 7b is transformed into an equivalent series-load circuit in Fig. 7c. The values of R_L and X_L in Fig. 7c were calculated and have also been measured with the Hewlett-Packard Model 8542A Automatic Network Analyzer. It was found that R_L and X_L could be calculated within 10% of the measured values.

Power output and noise as a function of R_L are plotted for two diodes in Fig. 8. These show behavior typical of all diodes tested: as R_L is reduced from a relative high value, say 3 ohms, the power increases slowly until "saturation," a self-limiting effect, takes place. Saturation occurs when the peak value of the applied ac waveform, V_D sin ωt, reaches a value equal to one-half the diode breakdown voltage, V_{bd}. The power then drops *linearly* as a function of a further drop in R_L. This linear dependence

corresponds to constant ac voltage across the diode.

The behavior shown in Fig. 8 is qualitatively explained by a simple modification of Read's basic large-signal theory[9].

RF power output as a function of bias current is shown with R_L as a parameter in Fig. 9. Here, it is seen how small values of R_L lead to saturation at relatively low values of I_{dc} and power output. The output power level at which saturation occurs becomes higher as R_L is increased up to a particular level. Note in Fig. 9 that in each case, the diode voltage at saturation is about the same: ½ V_{bd}. It should be emphasized that this is *not* a thermal effect — it is purely electrical. (The diode used for the data in Fig. 9 is typical of some of the better diodes obtained during our development program: for $R_L = 2.2\Omega$, 0.8W was obtained at a junction temperature of 195°C with 10W input; for $R_L = 2.6\Omega$, 1.0W was obtained at $T_j = 240$°C and 12.7W input).

Noise

When voltage saturation occurs or is imminent, the RF spectrum becomes noisy, and under certain conditions bias current oscillations can occur. This situation is shown in the frequency spectra illustrated in Fig. 10. Here, a low value of R_L was chosen so that saturation would occur at a relatively low power, 0.4 watt. The photos show that as the bias current is increased beyond the saturation level, the spectrum degrades rapidly.
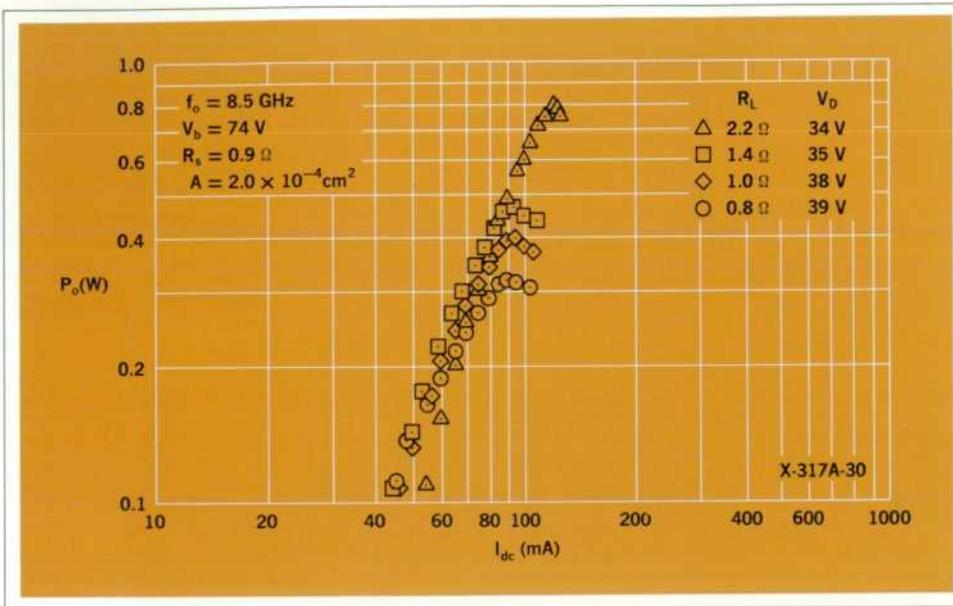
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Fig. 9. *Typical power output as a function of bias current with load resistance as a parameter.*

Power limits when $V_D = \dfrac{1}{2} V_{bd}$.

Measuring IMPATT Diode Thermal Resistance

Thermal resistance measurements made during this study relied on the fact that the breakdown voltage V_{bd} of silicon PN junctions is almost an exact linear function of temperature. For example, the abrupt P-N junctions in HP IMPATT diodes have a breakdown voltage vs. temperature characteristic $\partial V_{bd}/\partial T \approx 1.17 V_{bd}$ mV/°C. If V_{bd} were 70 volts at 25°C, V_{bd} would thus increase 82 mV for each degree of temperature rise in the junction.

With reference to the diagram, the junction voltage V_{dc} can be considered as having three components: $V_{bd}(T_o)$, $\dfrac{\partial V_{bd}}{\partial T} \Delta T$, and $I_{dc}R_{sc}$. $V_{bd}(T_o)$ is the room-temperature breakdown voltage, $\dfrac{\partial V_{bd}}{\partial T} \Delta T$ is the increment in V_{bd} caused by junction heating, and $I_{dc}R_{sc}$ is the voltage drop in the junction space charge resistance, R_{sc}.

R_{sc}, a purely electronic effect, can be measured by straightforward pulse techniques. With R_{sc} known, determination of the thermal resistance θ is simply a matter of accurately measuring the junction voltage and current. Derivation of θ from these quantities is as follows:

$$\Delta T = T - T_o = \theta \, V_{dc} I_{dc}$$

$$V_{dc} = V_{bd}(T_o) + \frac{\partial V_{bd}}{\partial T}(T - T_o) + I_{dc}R_{sc}$$

$$\theta = \frac{V_{dc} - V_{bd}(T_o) - I_{dc}R_{sc}}{\dfrac{\partial V_{bd}}{\partial T} V_{dc} I_{dc}}$$

This method is fast, reliable, and accurate. It has a further advantage in that θ is determined under actual operating conditions.
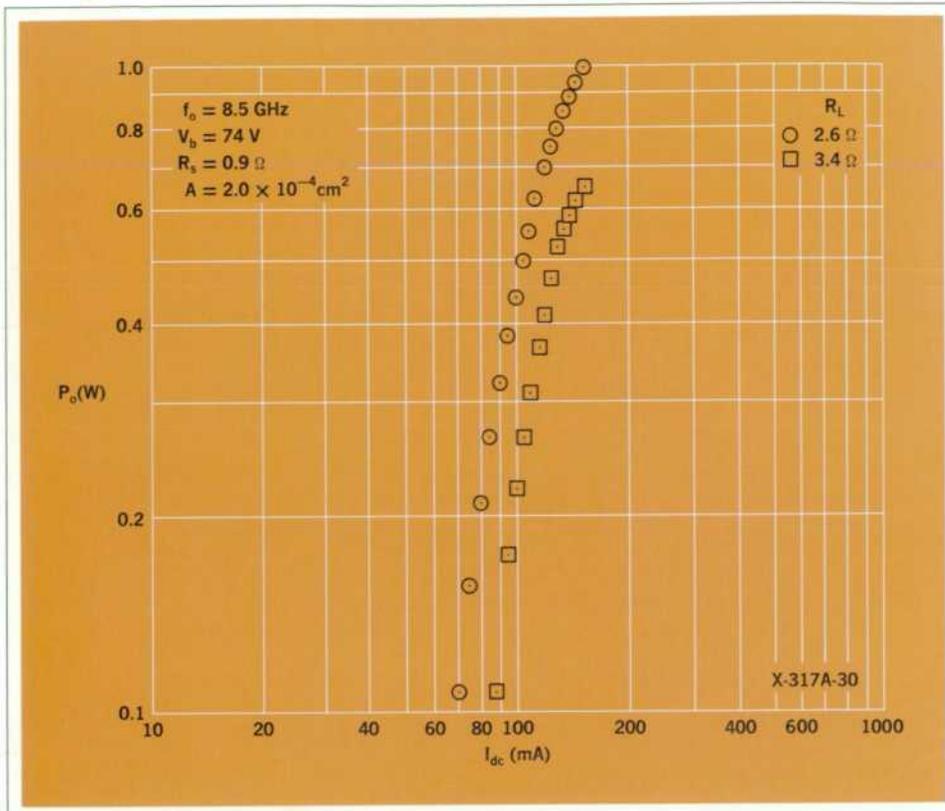

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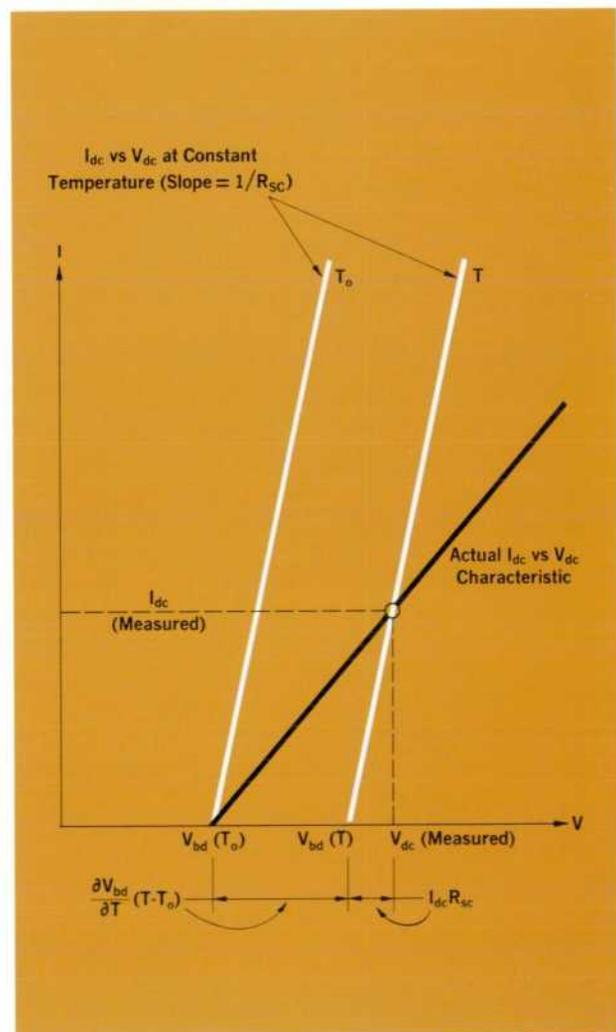
Fig. 9b.

In Fig. 10d, a resonant circuit had been connected from the bias port to ground. With the oscillator operating above the saturated power level the bias circuit oscillated, introducing AM and FM modulation on the RF output, as shown by the sidebands in the frequency spectrum.

The noisy behavior accompanying power saturation appears to be characteristic of IMPATT diode operation. For quiet operation, then, an IMPATT diode should be operated well below the saturation level, i.e., with R_L somewhat larger than the value that obtains maximum power. Values of FM and AM noise measured in diodes operated this way are plotted in Fig. 11. In view of the circuit Q's employed, these are respectable noise performances. At the time of writing there has been no concerted effort to characterize FM noise in circuits with higher Q. Isolated measurements, however, in cavities with Q's on the order of 100 to 200 at 350 mW power levels, have shown FM less than 7 Hz (rms) in a 100-Hz bandwidth in X-band. This figure is competitive with reflex klystrons and better than that of BWO's found in typical laboratory signal generators.

Modulation

Amplitude modulation of IMPATT diodes can be achieved by directly modulating the diode's bias current. This method also produces some frequency modulation simultaneously. Frequency modulation can also be achieved with YIG or varactor circuits, or by modulating the frequency of an external injection-phase-locking signal. This technique is especially suitable when an injection-locking scheme is already included for frequency stabilization. A typical application is in microwave telecommunication systems where an injection-locked IMPATT oscillator serves as the transmitter.

Conclusions

The IMPATT diode has been shown to be a practical source of CW microwave power in X-band. The fundamentals of IMPATT circuit design are well understood in terms of simple large-signal equivalent circuits. New manufacturing techniques produce diodes reliably at reasonable cost, pointing the way to large-scale use of these devices in microwave systems design. Future plans at the HP Associates Division of Hewlett-Packard include development of diodes for operation at frequencies both above and below X-band, from C band through K_u band, and further applications work focused on those areas which appear especially suitable for IMPATT diodes.

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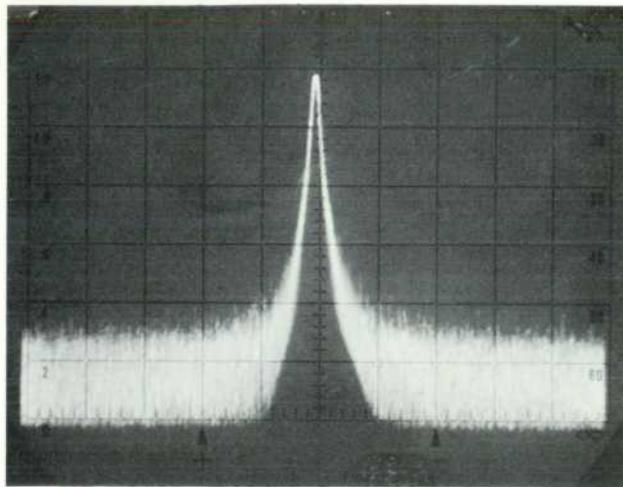
a I_{dc} = 55 mA; P_o = 176 mW
     f_o = 8.2 GHz
     R_L = 1.0 Ω
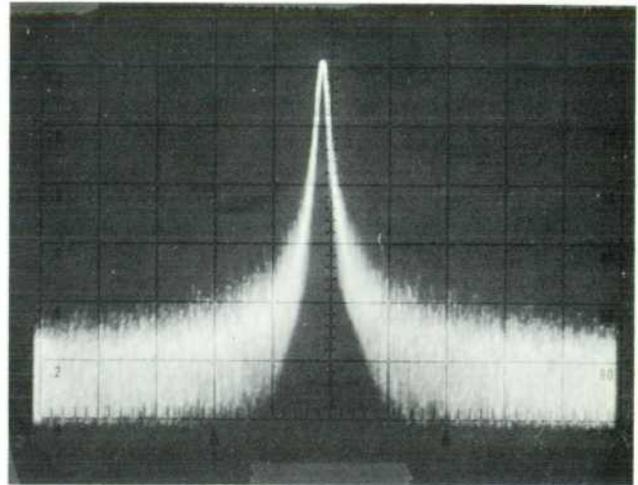
b I_{dc} = 90 mA; P_o = 395 mW
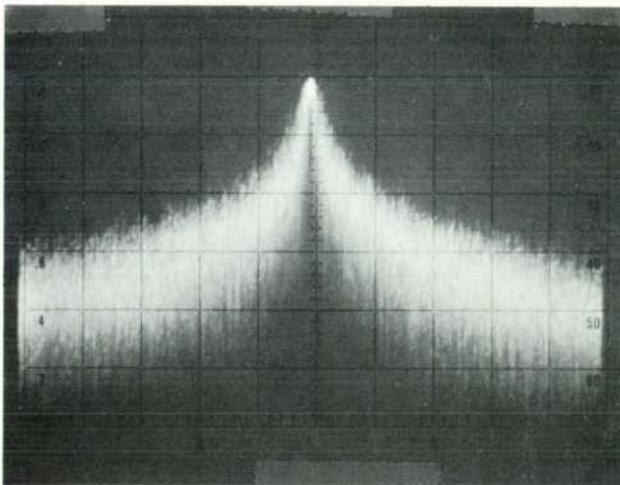
c I_{dc} = 95 mA; P_o = 400 mW
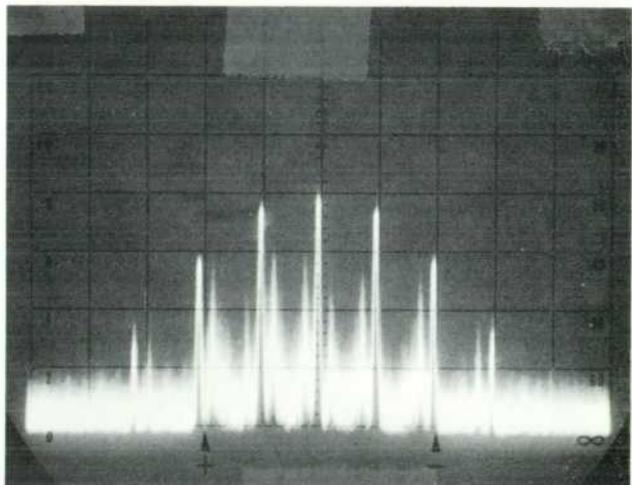
d   I = 90 mA;
     (RESONANT BIAS CIRCUIT)

Fig. 10. *Spectra of IMPATT diode oscillator operated at 8.2 GHz with 1.0 Ω load. Vertical scale is 10 dB/cm. Horizontal scale is 1 MHz/cm in a, b, and c; 30 MHz in d.*

SPECIFICATIONS
HP MODELS 5082-0400 (8–10 GHz) and
5082-0401 (10–12.4 GHz)
Silicon X-Band IMPATT Diodes

SUGGESTED MAXIMUM RATINGS:

Parameter	Symbol	5082-0400/0401
Storage Temperature	T_{STG}	150°C
Junction Operating Temperature (Note 1)	T_J	200°C
Power Dissipation (Note 2)	P_{DISS}	$\dfrac{200 - T_{CASE}}{\theta_{JC}}$

ELECTRICAL SPECIFICATIONS AT T_A = 25°C:

Parameter	Symbol	5082-0400 Min.	5082-0400 Typ.	5082-0400 Max.	5082-0401 Min.	5082-0401 Typ.	5082-0401 Max.	Units	Note
CW Output Power	P_o	0.5	0.7	—	0.50	0.60	—	W	3
Efficiency	η	5	6.5	—	5	6	—	%	4
Thermal Resistance	θ_{JC}	—	15.0	16.0	—	16.0	17.0	°C/W	5

TYPICAL PARAMETERS AT T_A = 25°C:

Parameter	Symbol	5082-0400	5082-0401	Units	Note
Breakdown Voltage (I = 10 μA)	V_{BR}	78	65	V	—
Chip Capacitance at Zero Bias	C_{jo}	5.5	5.0	pF	6
Package Capacitance	C_p	0.33	0.33	pF	—
Package Inductance	L_p	0.60	0.60	nH	7

NOTES:

1. Diode burnout occurs for $T_J \simeq 350$°C. Operation at $T_J < 200$°C thus allows a large margin for safety, ensuring long-term reliable operation and stability of diode parameters.

2. $P_{DISS} = P_{in} - P_o$

3. Output power is measured in a nominally fixed-tuned mount like that shown in figure 7 The frequency of oscillation varies slightly from diode to diode, due to slight variations in junction capacitance and package inductance. For the 5082-0400, the frequency is approximately 10 GHz; for the 5082-0401, it is approximately 12.4 GHz. Maximum DC input power (P_{in}) for this measurement is 11.0 W for 5082-0400 and 10.0 W for 5082-0401.

4. $\eta = P_o/P_{in}$

5. Thermal resistance is measured under DC conditions with the diode in reverse bias, using the temperature dependence of the breakdown voltage as a temperature sensor. This method ensures that the thermal resistance is determined as it occurs in actual operation.

6. Measured at 1.0 MHz.

7. Measured in X-band in 0.276" O.D. coaxial transmission line. Diode biased to V = V_{BR}.

PRICE:
1– 9	$150.00
10– 99	$125.00
100–249	$100.00
250–499	$ 85.00
500–999	$ 70.00
≥1000	$ 60.00

MANUFACTURING DIVISION: HP ASSOCIATES
620 Page Mill Road
Palo Alto, California 94304

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A. M. Cowley

Mike Cowley earned BSEE and MSEE degrees at Notre Dame (1959 and 1961) and a PhD in electrical engineering at Stanford in 1965. Along the way he taught electrical engineering at the University of California at Santa Barbara and worked as a consultant in physical electronics. He joined HP in 1965, where he has been concerned with Schottky-barrier diode technology and with microwave oscillators using avalanche effects in silicon and the Gunn effect in gallium arsenide. Mike is presently manager of the Applied Research Section of the HP Associates R and D Laboratory. He is a member of the IEEE, Tau Beta Pi, Sigma Xi, and the American Physical Society.

Staunch members of the Sierra Club, Mike and his wife enjoy backpacking in the high Sierras with their two sons, aged 1 and 2½ years, usually with the help of a not-too-stubborn burro.

Measuring Capacitance Automatically

*Completely automatic multifrequency
bridge measures capacitance from
0.001 pF to 1.2 μF, conductance
and dissipation factor.*

**By Hitoshi Noguchi, Takeo Shimizu
and Koichi Maeda**

VALUES OF CAPACITANCE USED IN CIRCUIT DESIGN range from less than 1 pF to 1 F. To measure capacitance and loss factor over this wide range, designers most often use the frequencies 120 Hz, 1 kHz or 1 MHz to drive a capacitance bridge.

Large capacitors (greater than $1 \mu F$) and electrolytics are usually measured at the lowest frequency. Capacitors less than 1 μF down to several hundred pF are measured at 1 kHz, and capacitors less than about 1000 pF are commonly measured at 1 MHz. Most capacitance bridges use a single frequency—either 1 kHz or 1 MHz —for capacitance and loss measurements.

Efficiency in capacitor measurement can be improved with automatic methods of measurement. Measurements at several frequencies rather than a single frequency also allow complete evaluation of frequency sensitive devices. The new HP Model 4270A Automatic Capacitance Bridge, Fig. 1, automatically measures capacitance and loss at four frequencies between 1 kHz and 1 MHz. It measures capacitance from 0.001 pF to 1.2 μF in six automatically selectable ranges. The loss component is measured as either parallel conductance or dissipation factor. The loss (G) can be measured down to 0.1 nanomhos. The instrument has an internal, continuously variable dc bias supply to 200 volts to measure parameters of such devices as varactor diodes.

Balancing the Bridge

A bridge measurement, obviously, is valid only when the bridge is balanced. Various types of bridges are balanced in different ways. The best bridge design balances quickly with relatively simple operation. Ideally, the null detector should control bridge operation during balancing.

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Fig. 1. *The new HP Model 4270A Automatic Capacitance Bridge can measure grounded cables and input capacitance of amplifiers with the LOW terminal grounded. In L-GROUND operation, the instrument still retains the guarded feature.*

In the Model 4270A, the output of the phase detector is integrated. Detector sensitivity is a function of the ingration time interval. When the bridge is far off null, the integrating time is short (1 millisecond) for rapid approach to the null. But detector sensitivity is lowered. As the null is approached, integrating time is automatically increased to about 20 milliseconds, and detector sensitivity is increased. Thus the bridge is balanced in the fastest possible time.

The traditional, manually-operated bridge uses a very sensitive null detector. The detector, however, shows only the magnitude of the unbalanced voltage or current, but does not indicate the direction necessary to achieve balance. Satisfactory control of the bridge depends largely upon the operator's experience.

AC bridges often use phase detectors as null detectors. It is a characteristic of ac bridges that the bridge output waveform inverts as the bridge output passes through the null.[1] Thus, the phase detector can provide information about the direction of balance. In the Model 4270A, this information through logic circuits, directly controls the balancing operation.

Basic Operation

The Model 4270A Bridge is balanced by adjusting attenuators in the C and D,G arms (Fig. 2). Digital signals operate transistor switches in each attenuator, Fig. 3. When the proper value of attenuation is reached, the currents i_X, i_C, and i_D or i_G equal zero and the bridge is balanced. (The capacitance and loss displays indirectly
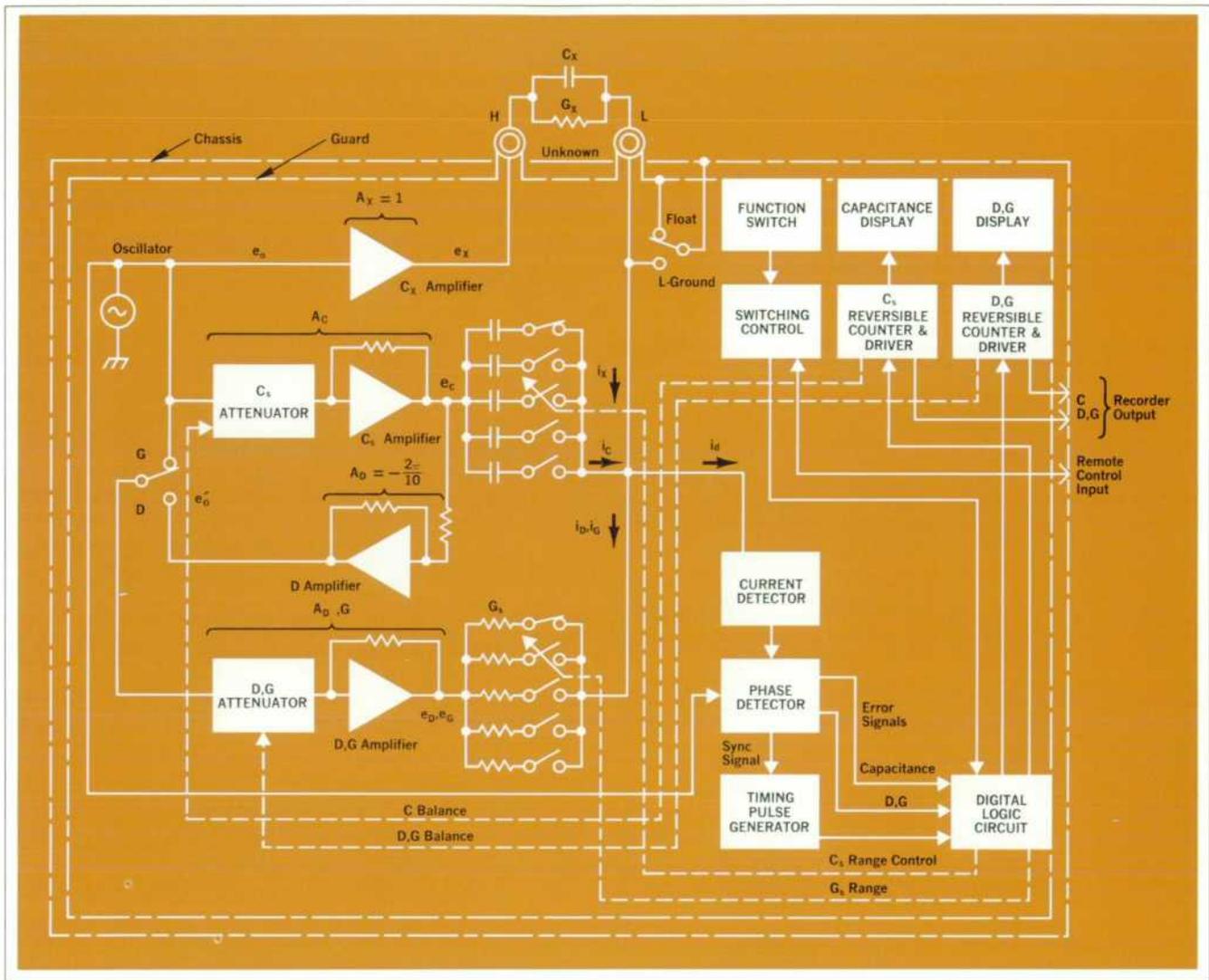
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Fig. 2. *Digital logic circuits control range and balance functions of the capacitance bridge.*

indicate attenuator resistance values.) During balancing, the phase detector output, through the logic circuitry, operates the reversible counter and driver in the direction necessary to achieve balance.

Balance Equations

Null detector current i_d is the sum of current i_x through the unknown, current i_C through the C measurement arm, and current i_D or i_G through the D, G measurement arm. From the block diagram, Fig. 2,

$$i_x = (G_x + j\omega C_x)e_x = (G_x + j\omega C_x)A_x e_o.$$

Since the gain A_x of operational amplifier C_x has been selected to be 1, then
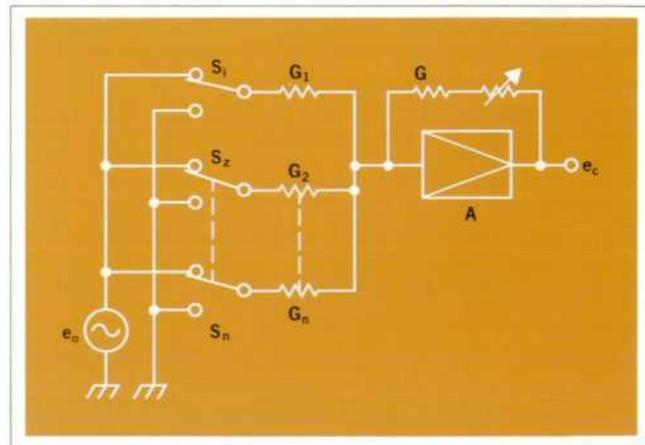
$$i_x = (G_x + j\omega C_x)e_o \qquad (1)$$

Fig. 3. *Transistor switches in the attenuator (S1, etc.) ground resistances to keep noise low.*

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Logic Circuits

The logic circuits are the control circuits that balance the bridge. They switch the standards and digitally select values of attenuation so that balance is reached and maintained. When a measurement is started, the gates that operate the C_s and G_s relays (through the range selector) are opened in the "Auto Range" mode. The "parameter change" circuit switches to C.

The signal from the phase detector is integrated as described in the text. From the integrators, the signal goes to comparators that determine its polarity and compare its level with a reference voltage. Polarity is an indication of which direction the signal is off null; level is an indication of how close the signal is to the null.

Two gate controls, one for C and one for D,G are actuated by the comparator output. The gate controlling the C_s and G_s relays is closed, and the gate to operate the first C dis-

play digit through the reversible counter is opened. Whether the counter runs forward or reverse depends upon the polarity of the comparator output. Digital signals from the counter change the attenuators and operate the display once during each integrating interval. When the integrator output polarity changes (which means that the signal is off null in the other direction) the gate to the next digit is opened, and the counter reverses. Attenuators are operated, and each digit actuated in sequence by repeating this process.

If the integrator output drops below the reference level while sequencing through the C display, or when the last C digit is reached and integrator output polarity changes, the "parameter change" circuit switches to D,G. Each D,G digit is then actuated in sequence by repeating the same process. If the integrator output drops below the reference level while sequencing through the D,G display, the null circuit stops the measurement. Otherwise the measurement stops after the last digit has been actuated.

Similarily
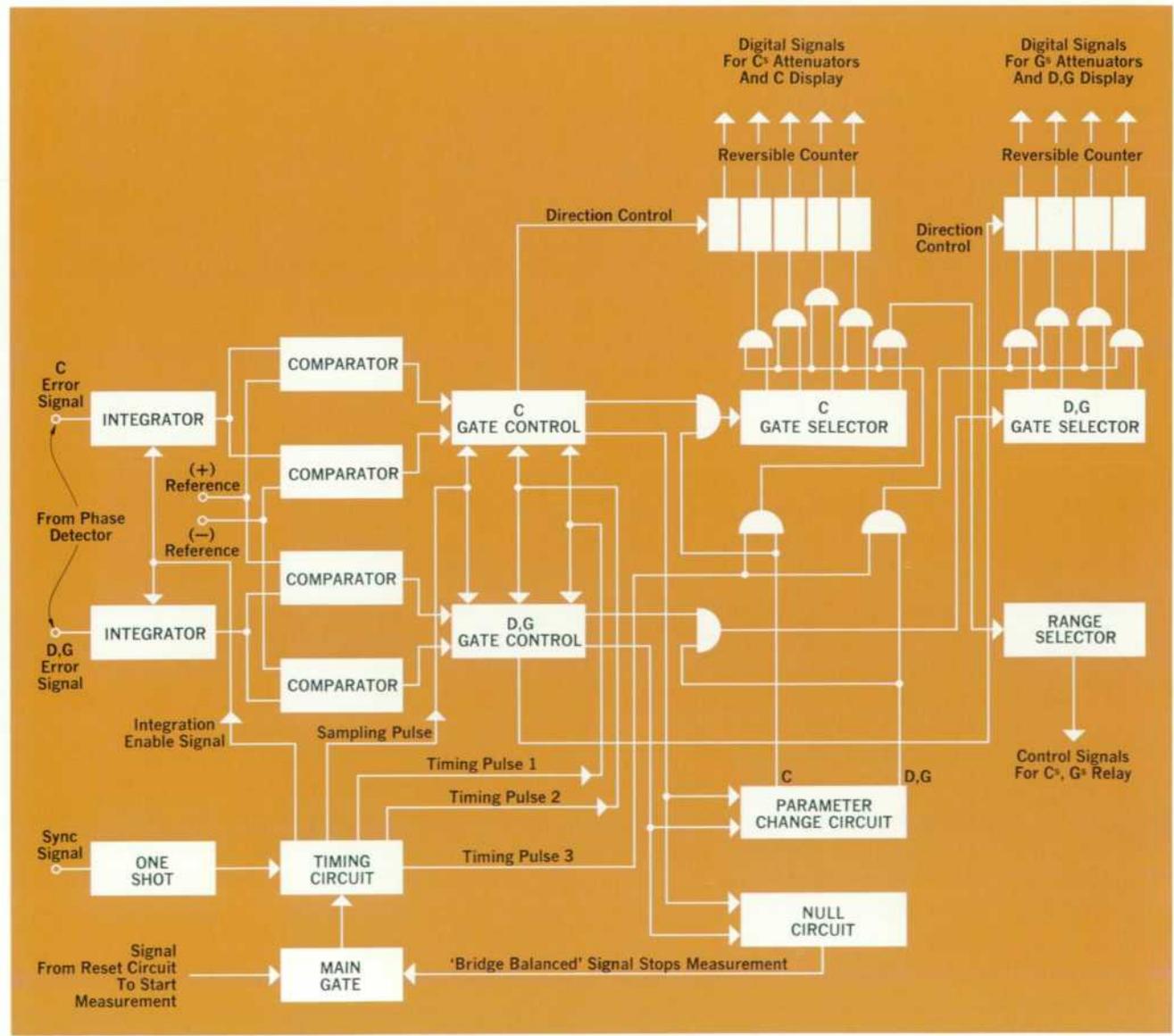
$$i_C = j\omega C_s e_C = j\omega C_s A_C e_o \qquad (2)$$
$$i_G = G_s e_G = G_s A_{D,G} e_o$$

At bridge balance, $i_d = 0$. Then $i_d = i_x + i_C + i_G = 0$.

Thus
$$C_X = -A_C C_s$$
$$G_X = -A_{D,G} G_s$$

To measure dissipation factor D, the slide switch on the front panel is moved to D. Substituting source voltage e'_o (see Fig. 2) for source voltage e_o,

$$i_D = G_s e_D = G_s A_{D,G} e'_o = G_s A_{D,G} A_D e_C \qquad (3)$$

Since $i_d = i_x + i_C + i_D = 0$, from equations (1), (2) and (3),

$$D_X = \frac{G_X}{\omega C_X} = \frac{-G_s A_{D,G} A_D A_C}{-\omega C_s A_C} = \frac{G_s}{\omega C_s} \cdot A_D A_{D,G}$$

In the Model 4270A, $\frac{G_s}{\omega C_s}$ is selected to be $\frac{10}{2\pi}$ and $A_D = \frac{-2\pi}{10}$.

Thus,
$$D_X = -A_{D,G} \qquad (4)$$

At balance then, $C_X = -A_C C_s$, $G_X = -A_{D,G} G_s$ and $D_X = -A_{D,G}$.

As mentioned previously, the front panel readouts are an interpretation of attenuator settings, which set the gains A_C and $A_{D,G}$ in the above equations.

Three-terminal measurements reduce errors introduced by stray capacitance. In a conventional ac bridge, a transformer isolates the source voltage so that three-terminal measurements are possible. But transformers have limited frequency range. Therefore, another scheme was used in the Model 4270A to cover the 1 kHz to 1 MHz frequency range with only *one* bridge network.

In the Model 4270A, each measurement arm consists of a resistance attenuator and an operational amplifier. All of the amplifiers have identical frequency and phase characteristics. All use low-impedance elements to reduce effects of stray capacitance at high frequencies.

All components in the resistance attenuator are likewise low-impedance elements. The resistance attenuators are a form of digital-to-analog converter. Digital signals actuate the switching transistor, adding or removing resistances, and producing an analog output voltage.

Switching transistors are in series with the standard resistors in the attenuator. It is possible to compensate for any deviation in each resistor by adjusting the base current of its switching transistor. Switching is so arranged that unused resistances are grounded. The output
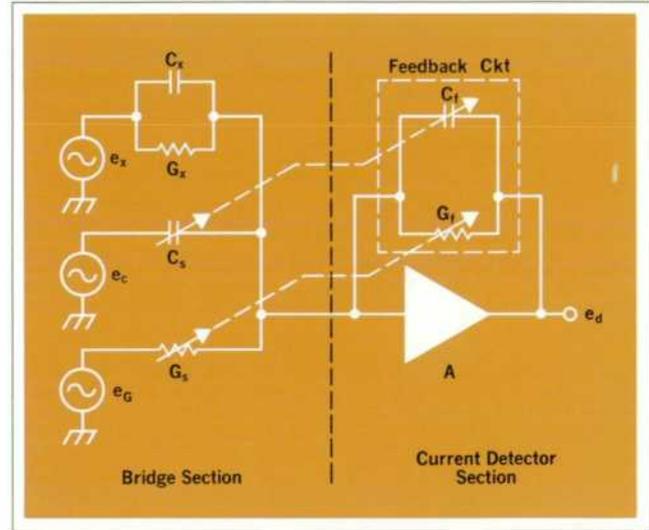

Fig. 4. *Feedback admittance in the current detector is adjusted automatically to maintain constant bridge sensitivity over the operating range.*

resistance is thus kept constant, regardless of the attenuator setting.

Stray capacitances can cause differences in the time constant between the attenuator resistors. This appears as error in measuring dissipation factor or conductance especially at 1MHz. In the Model 4270A, the attenuators are shielded, and the highest value resistors have adjustments so that time constant differences can be kept below 100 picoseconds.

Current Detector

When using the guarded three-terminal method of measurement, terminal-to-ground capacitance will decrease the sensitivity of a voltage sensitive null detector. With a phase sensitive null detector, this capacitance causes phase shift which also reduces the detection capability. A solution to this problem, used in the Model 4270A, is the current sensitive detector and preamplifier with low input impedance.

The detector has a feedback circuit, Fig. 4, consisting of an adjustable capacitor and resistor. Values of the feedback capacitance and resistance are adjusted to (1) maintain constant detector sensitivity, (2) maintain a constant phase relationship between the bridge driving voltage e_o and the detector voltage e_d, and (3) maintain a low input impedance to the detector preamplifier. This assures stable bridge operation and reduces problems associated with phase detection.

Because the input impedance to the detector preamplifier is low, the voltage at that point is low. Thus the effect of stray capacitance is negligible. Also, the low input

SPECIFICATIONS

HP Model 4270A

AUTOMATIC CAPACITANCE BRIDGE

MEASURING CIRCUIT:

FLOAT: Guarded terminals of unknown are floated from ground.

L-GROUND: One side of unknown terminals is grounded, guard is retained.

PARAMETERS MEASURED: Capacitance, equivalent parallel conductance and dissipation factor.

MEASURING FREQUENCY: 1 kHz, 10 kHz, 100 kHz and 1 MHz, ±1%.

AVAILABLE FULL SCALE RANGES:

CAPACITANCE				CONDUCTANCE	DISSIPATION FACTOR
1 kHz	10 kHz	100 kHz	1 MHz		
180.00pF	18.000pF			999.9n	
1800.0pF	180.00pF	18.000pF		9.999µ	
18.000nF	1800.0pF	180.00pF	18.000pF	99.99µ	0.9999
180.00nF	18.000nF	1800.0pF	180.00pF	999.9µ	
1.2000µF	180.00nF	18.000nF	1200.0pF	9.999m	

REPEATABILITY: ±2 digits at NORMAL TEST VOLTAGE, ±8 digits at LOW TEST VOLTAGE.

RANGE MODE:

AUTO: Range selection and balance performed automatically.

HOLD: Range is held on fixed position determined by previous AUTO and can be selected manually by stepping RANGE STEP. Balance begins with fourth digit from right.

TRACK: Range held on fixed position, balance begins with last digit.

BALANCING TIME: Typically 0.5 s.

MEASURING RATE: Measurement cycle equals balance time plus display time. Balance time typically 0.5 s. Display times selected by MEAS RATE are 70 ms, 2 s, 5 s, and MANUAL.

RESET: Bridge is reset and new balance operation started automatically (at MEASURING RATE), or manually by RESET pushbutton, or remotely by contact closure. If the unknown changes value during the balance operation, or other changes shift the unknown outside of the balance range, the bridge resets to rebalance after 2 seconds.

TEST VOLTAGE ACROSS UNKNOWN:

NORMAL: 500 mV rms constant, at capacitance units displayed in pF or nF, 100 mV rms constant at µF.

LOW: 100 mV rms constant at pF or nF. 20 mV rms constant at µF. Other test voltages are available.

ACCURACY:

CAPACITANCE, CONDUCTANCE AND DISSIPATION FACTOR:

STANDARD CAPACITANCE:

FULL SCALE RANGE	STANDARD CAPACITANCE
18.00pF	10pF
180.00pF	100pF
1800.0pF and 1200.0pF	1nF
18.000nF	10nF
180.00nF	100nF
1.2000µF	100nF

DC BIAS: INTERNAL or EXTERNAL to ±200 V, in HOLD and TRACK mode.

INTERNAL BIAS at FLOAT measurement:

VOLTAGE: 0 to 20 V dc; 0 to 200 V dc; continuously variable on front panel, monitored on rear panel.

DIAL ACCURACY: ±5% of full scale.

SOURCE RESISTANCE: 100 kΩ.

POLARITY: LOW unknown terminal (−), HIGH unknown terminal (+) in FLOAT position of MEAS CKT control.

REMOTE: Programmable by resistor with 250 Ω/V rate at 20 V range, 25 Ω/V rate at 200 V range.

REMOTE ACCURACY: ±2% of full scale.

INTERNAL BIAS at L-GROUND: An additional connection using a blocking capacitor and a coaxial cable is necessary for INTERNAL source.

DATA OUTPUTS: (If unknown in FLOAT)

CODE: Positive 4 line BCD (1-2-4-8), 13 columns consisting of decimal location, overrange, units, 5 digits of capacitance and 4 digits of conductance or dissipation factor.

'1' LEVEL: +5 V, open circuit, source impedance 7.5 kΩ at all data except at 10^4 digit of C data and OVER-RANGE. +4V, open circuit, source impedance 7.5 kΩ at 10^4 digit of C data and OVER-RANGE.

'0' LEVEL: Ground.

PRINT COMMAND: DC coupled, print level +5 V, print holdoff level 0V.

INPUTS:

TRIGGER HOLD OFF LEVEL: Level must be between −10 V and −15 V.

REMOTE PROGRAMMING: Eight front-panel functions can be remotely controlled by external contact closure to ground with impedance less than 400 Ω. Programmable functions are RESET, FREQUENCY, RANGE MODE, TEST VOLTAGE, LOSS MEASUREMENT, RANGE STEP, DC BIAS RANGE, BIAS VERNIER.

OPERATING TEMPERATURE: 0°C to 50°C.

POWER REQUIREMENTS: 115 or 230 V ac ±10%, 50 to 60 Hz, approx. 110 W.

WEIGHT: 34 lb (15.5 kg).

PRICE: $4825.00.

MANUFACTURING DIVISION: YOKOGAWA-HEWLETT-PACKARD LTD.
9-1, Takakura-cho
Hachioju-shi
Tokyo, Japan

NOTE: Cs = internal standard capacitor. Cx = capacitance measured. Dx = dissipation factor measured.

FREQUENCY: ±1%.

			1 kHz 1 µF RANGE	1 kHz except 1 µF RANGE	10 kHz	100 kHz	1 MHz
CAPACITANCE	TEST VTG NORMAL	D <0.1	±(0.1% + 1 digit + 0.01 pF)			±(0.3% + 1 digit + 0.01 pF)	±(1% + 1 digit + 0.01 pF)
		0.1 ≤ D <1	±(0.2% + 1 digit + 0.01 pF)			±(0.5% + 1 digit + 0.01 pF)	±(2% + 1 digit + 0.02 pF)
	TEST VTG LOW	D <0.1	±(0.3% + 6 digits)	±(0.2% + 6 digits + 0.01 pF)		±(0.4% + 6 digits + 0.01 pF)	±(1.1% + 6 digits + 0.01 pF)
		0.1 ≤ D <1	±(0.6% + 6 digits)	±(0.4% + 6 digits + 0.01 pF)		±(0.8% + 6 digits + 0.01 pF)	±(2.2% + 6 digits + 0.01 pF)
	If DC BIAS used add:	FLOAT	− 3.2 Dx · Cs (µF) × (100 ±10)%				
		L − GND	unspecified (depends on C & D of blocking capacitor used)				
CONDUCTANCE	TEST VTG: NORMAL		±(1% + 10 digits)				±(3% + 10 digits)
	TEST VTG: LOW		±(1.2% + 15 digits)	±(1.1% + 15 digits)			±(3.1% + 15 digits)
	If DC BIAS used add:	FLOAT	+ [3.2 Cs (µF)]² × (100 ±20)%				
		L − GND	unspecified				
DISSIPATION FACTOR	TEST VTG: NORMAL		±[1% + (10 + Cs/Cx) digits]				±[3% + (10 + Cs/Cx) digits]
	TEST VTG: LOW		±[(1.4 + 0.06 Cs/Cx)% + (10 + 5 Cs/Cx) digits]	±[(1.2 + 0.06 Cs/Cx)% + (10 + 5 Cs/Cx) digits]			±[(3.2 + 0.06 Cs/Cx)% + (10 + 5 Cs/Cx) digits]
	If DC BIAS used add:	FLOAT	+ [[3.2 Cs (µF)]² + 3.2 Dx · Cs (µF) × (100 ±20)%]				
		L − GND	unspecified				

impedance nearly eliminates noise induced by electrostatic coupling, mainly power line noise. Capacitance introduced by connecting cables may be balanced out with an available option.

Applications

For development of new components, circuits or systems, the Model 4270A can be operated as an independent lab-type instrument. It can be used to measure discrete capacitor values, cable capacitance and loss, input and output capacity, strays, junction capacitance and other non-linear capacitances. Other areas using the instrument alone include quality assurance, production or incoming inspection.

The HP Model 4270A has been designed for use with other instruments, computers or in systems. Data outputs (measured value, multiplier and units) are available in BCD form. Signals for remote programming are supplied to the bridge through a rear-panel connector. All major functions can be controlled individually. Thus, the Model 4270A finds application in quality control, reliability analysis, and statistical analysis of products. Users are able to make comparison checks, environmental classification, sorting and inspection. In-process testing of integrated circuits is another important application.

There are also applications where capacitance itself is not the main parameter being measured, but capacitance is monitored to derive other information. For example, in process control, dielectric or capacitance variation may be monitored. Changes in capacity or loss indicate changes in other physical parameters.

Acknowledgments

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Reference

[1]. K. Yoshimoto, 'A New Universal Impedance Bridge', **Hewlett-Packard Journal**, Sept. 1966.

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Hitoshi Noguchi obtained a BSEE degree from Akita University in 1961. He then joined Yokogawa Electric Works as an R and D engineer, working on the development of signal generators. Hitoshi joined Yokogawa Hewlett-Packard in 1964, working on the design of the Model 4260A Universal Bridge, and then on the design of the Model 4270A as the project leader.

Takeo Shimizu

Takeo Shimizu received his BSEE degree from Fukui University in 1961, and joined Yokogawa Electric Works as an R and D engineer, working on the development of a dc potentiometer, dc bridge, and mechanical strain measurement. Takeo joined YHP as a senior field engineer in 1964. In 1966 he transferred to the R and D section and developed logic section circuitry for the HP Model 4270A.

Koichi Maeda

Koichi Maeda received his BSEE from Waseda University, Tokyo, in 1963. After a year of working at Yokogawa Electric Works as an R & D engineer, he joined YHP in 1964. At YHP he worked on oscillator development, specifically on the design of the Model 4204A Digital Oscillator. He designed the bridge section circuitry for 4270A.