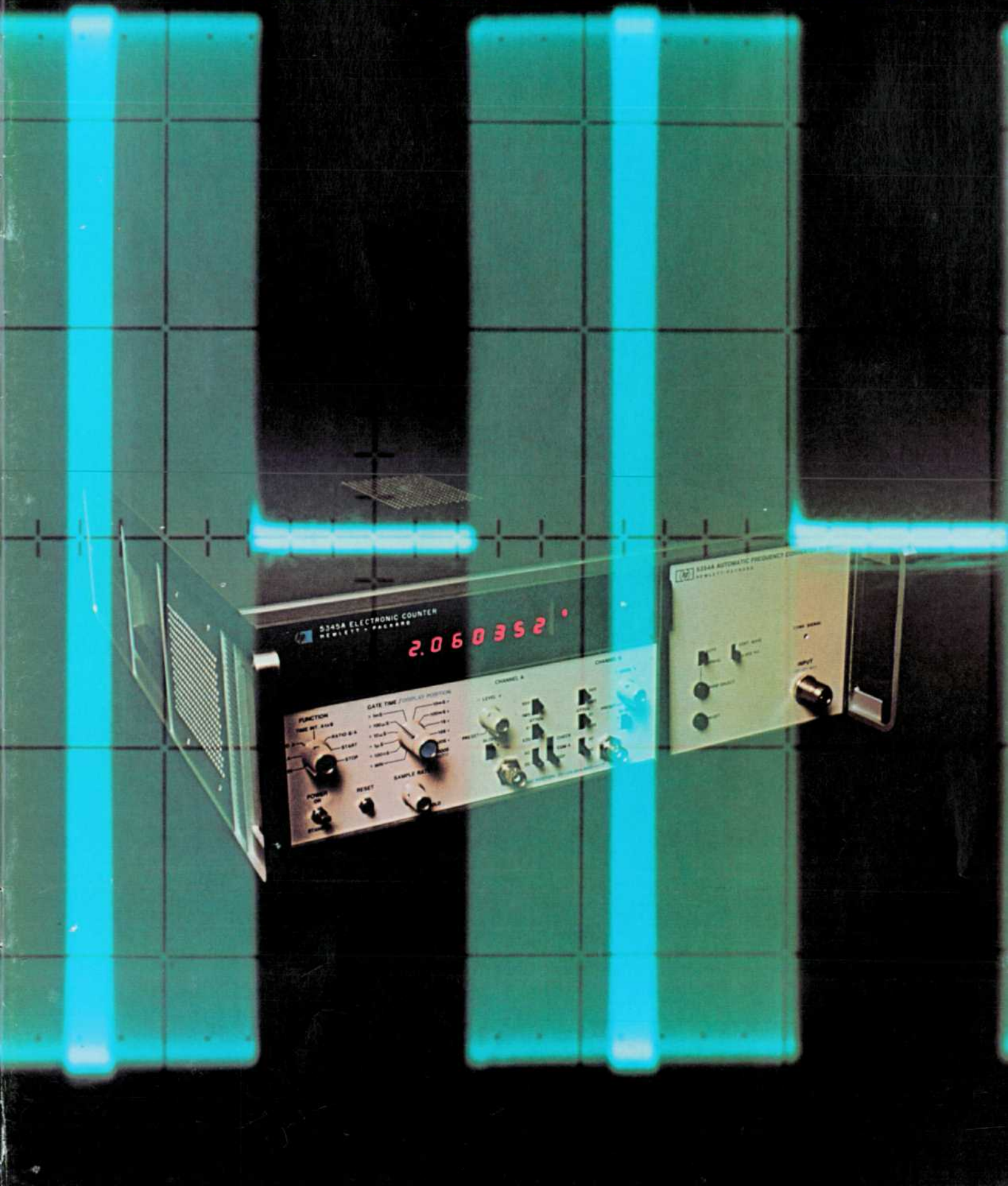
JUNE 1974

HEWLETT-PACKARD JOURNAL



A New Generation in Frequency and Time Measurements

This new general-purpose electronic counter refines the art of frequency and time measurements to an impressive degree by the application of advanced technology.

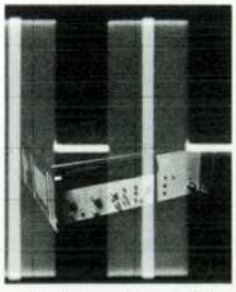
by James L. Sorden

THE MODERN HISTORY of measuring time and frequency with general-purpose electronic instrumentation dates from the vacuum-tube counters of the early-1950's. As technology moved from vacuum tubes to transistors, better input amplifiers and digital circuits were designed and the frequency limits of electronic counters advanced from 10 MHz to 50 MHz. Integrated circuits of the late 1960's brought the cost of electronic counters down but left performance relatively unchanged. A significant jump in the performance of general-purpose machines for the measurement of time and time-related quantities awaited the development of wideband digital logic circuits and high-sensitivity dc-coupled input amplifiers.

In the story of the new Model 5345A Electronic Counter (Fig. 1), development of these critical circuits fills the largest chapter. However, the story doesn't end there. At least four major technical contributions have gone into this radically new general-purpose plug-in counter:

- High-sensitivity dc amplifiers provide state-of-the-art front-end signal conditioning for frequency and pulse measurements.
- 500-MHz E^2L logic greatly improves resolution for time interval measurements.
- ROM-controlled reciprocal frequency measurements provide constant high resolution independent of frequency.
- White noise modulation of the time base clock yields consistent picosecond-resolution time interval average measurements.

Model 5345A can measure any frequency from 50 μHz to 500 MHz. Above 1 Hz it gives nine-digit resolution in a one-second measurement. It resolves one-shot time intervals to two nanoseconds, and measures the frequencies of RF pulses as brief as 50 nanoseconds. With its improved time interval averaging, it can resolve repetitive time intervals to one picosecond. Frequency averaging, a technique new with the 5345A, substantially improves precision in measurements of the frequencies of pulsed microwave signals.



Cover: *Model 5345A Electronic Counter advances the art of pulsed RF frequency measurements with frequency averaging, a new technique that improves resolution even for very short gate times. By controlling the position of the gate (intensified section of bursts in cover photo) one can measure the frequency profile within a burst.*

In this Issue:

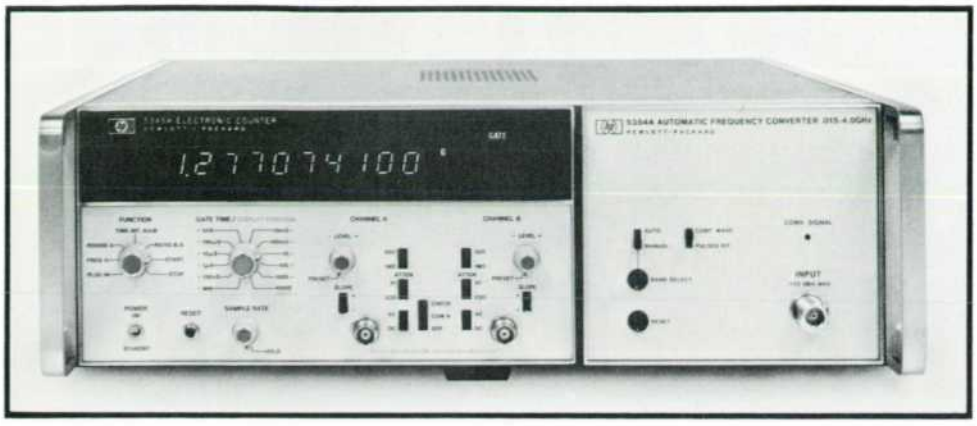


Fig. 1. *Model 5345A Electronic Counter is a new general-purpose plug-in instrument for frequency and time measurements. It has an 11-digit display, 10-mV sensitivity, and 500-MHz direct count capability. The plug-in shown, Model 5354A, extends the frequency measurement range to 4 GHz.*

The new counter has two input amplifier channels. Each has 10-mV sensitivity from dc to 500 MHz, is dc-coupled, and has switchable input impedance: 1 megohm/30 pF or 50 ohms. The 5345A is the first high-frequency counter that uses standard oscilloscope probes, either 10:1 compensating high-impedance types or 50-ohm probes.

A new family of high-performance plug-ins is under design, and two are already available. However, virtually all of the existing plug-ins for the 5345A's predecessor, the widely-used Model 5245L, function in the 5345A with improved speed and resolution.

One of the two new plug-ins is the first automatic heterodyne converter that can measure pulsed microwave signals as well as CW signals (see article, page 19). The second new plug-in adds a third 10-mV 500-MHz input channel, which is especially useful in analyzing data communications circuits (see article, page 16).

Full digital output and remote programming input are available for the new counter, which is compatible with the HP interface bus (see article, page 22).

Frequency Measurements

To make a frequency measurement, the 5345A first makes a period measurement, then inverts the period to get frequency, which it displays. Nominal gate times are set with a front-panel switch, and these determine resolution. Fig. 2 compares the resolution of the new counter with that of conventional direct counters. The key to the new counter's high-frequency capability and high resolution in brief measuring periods is its 500-MHz clock coupled with the reciprocal technique.

Time Interval and T.I. Average Measurements

Time interval measurements are made by the 5345A mainframe. To resolve single time interval measurements meaningfully to two nanoseconds it is not enough to have a clock period of two nanoseconds (500 MHz). It is also necessary to open and close the measuring gate at subnanosecond speeds. A new family of 500-MHz monolithic IC's were designed specifically for the 5345A and are manufactured by HP.

Time interval averaging is not new with the 5345A. What is new is that for the first time, picosecond-resolution time interval measurements can be made with no harmonic problems. It can be shown that averaging reduces the ±1 count (±2 ns) quantization error to an rms value of $1/\sqrt{n}$ count, where n is the number of samples averaged. However, for true averaging, the counter's gating signal must maintain a uniform phase distribution around the counter's clock period. Measurements made when the distribution is not uniform will lead to an "average" value that is biased away from the true value no matter how many intervals are averaged. This occurs whenever the repetition rate of the in-

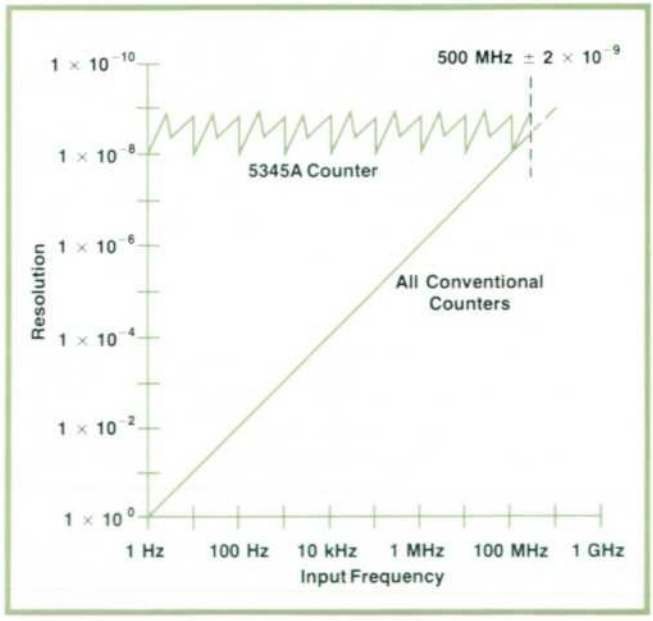


Fig. 2. *Model 5345A is a reciprocal-taking counter. This diagram compares its resolution with that of conventional direct frequency counters for a one-second measurement.*

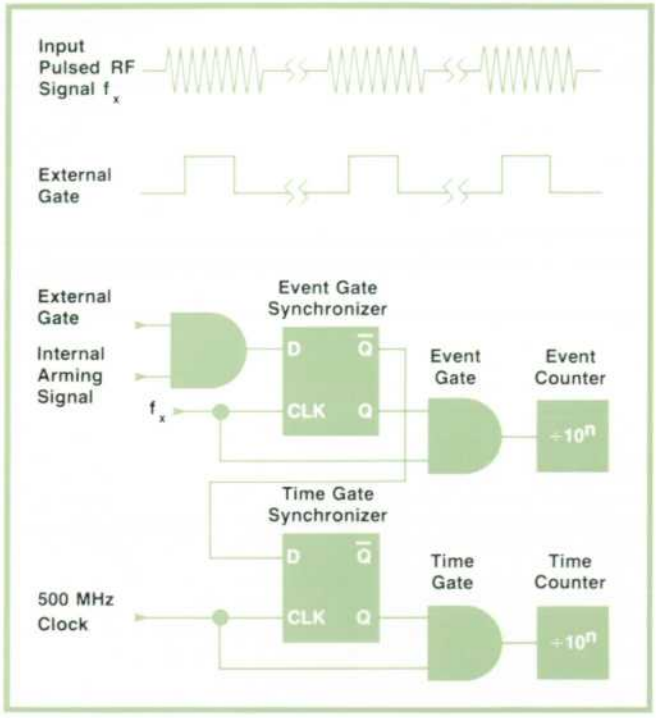


Fig. 3. *Synchronizers track RF bursts in frequency-average measurements, a technique new with the 5345A. Benefit is improved resolution over single measurements.*

coming signal has any harmonic or submultiple relationship to the counter's clock frequency.

The 5345A is the first counter to recognize this problem and to guarantee truly useful averaged measurements under all circumstances. This is achieved by deliberately adding jitter to the 500-MHz clock by modulating it with white noise (see article, page 12). Jitter of slightly greater than one period at 500 MHz is generated by modulating the time base clock with band-limited Gaussian noise.

Pulsed RF and Frequency Averaging

Because it needs only a brief measurement period, the 5345A is well suited for frequency measurements of pulsed RF signals. Gate openings as brief as 50 nanoseconds may be selected (one microsecond is usually the minimum found in electronic counters). To make a single-shot carrier frequency measurement of an RF burst, all that is necessary is to select a gate time narrower than the burst. The counter will trigger on the leading edge of the burst and measure for the selected time.

With external gating, the counter can measure the frequency profile within a burst. Or, to improve resolution for very narrow pulses, it can average frequency measurements over many pulses. This capability, new with this instrument, produces resolution never before attainable.

In frequency-average measurements, synchronizers (Fig. 3) track the RF bursts in such a manner that the averaged sum appears in the event counter and time counter. The pulsed bursts are clocked through the event gate flip-flop synchronously with an externally applied gate pulse. The event gate flip-flop output is then used to synchronize the time counter such that with a zero-biased jittered 500-MHz time base clock, the averaging will increase the resolution of a single shot measurement from ± 1 count to an rms value of approximately $1/\sqrt{n}$ count, where n is the number of pulsed RF bursts averaged. This improvement is qualified by the pulsed RF gate pulse width and the noise bandwidth of the jittered clock. Accuracy also improves, the amount of improvement depending mainly on how precisely the system has been calibrated.

The jittering is absolutely mandatory. Without it, it is not possible to assure either unique samples or a zero-biased answer. Fig. 4 gives theoretical (colored line) and typical (black line) improvements of pulsed RF measurement resolution. The curve flattening in the log-log resolution improvement plot occurs because of the band-limited nature of the Gaussian noise used to jitter the time base clock.

Counter Architecture

Fig. 5 is the 5345A's block diagram. System architecture is designed to support a wide variety of measurement capabilities, present and future.

The arithmetic processor performs fifteen-digit addition, subtraction, multiplication, and division. It also does display formatting on mainframe measurements and sum-of-products calculations on plug-in measurements. The T²L design operates at a clock rate of 2 MHz. 4096 bits of read-only-memory

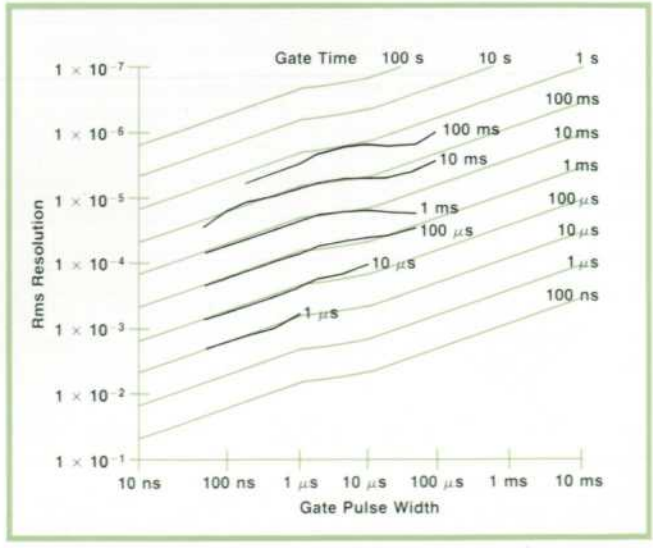


Fig. 4. *Resolution in pulsed RF measurements as a function of external gate width. Colored lines show theoretical resolution. Black lines show typical resolution.*

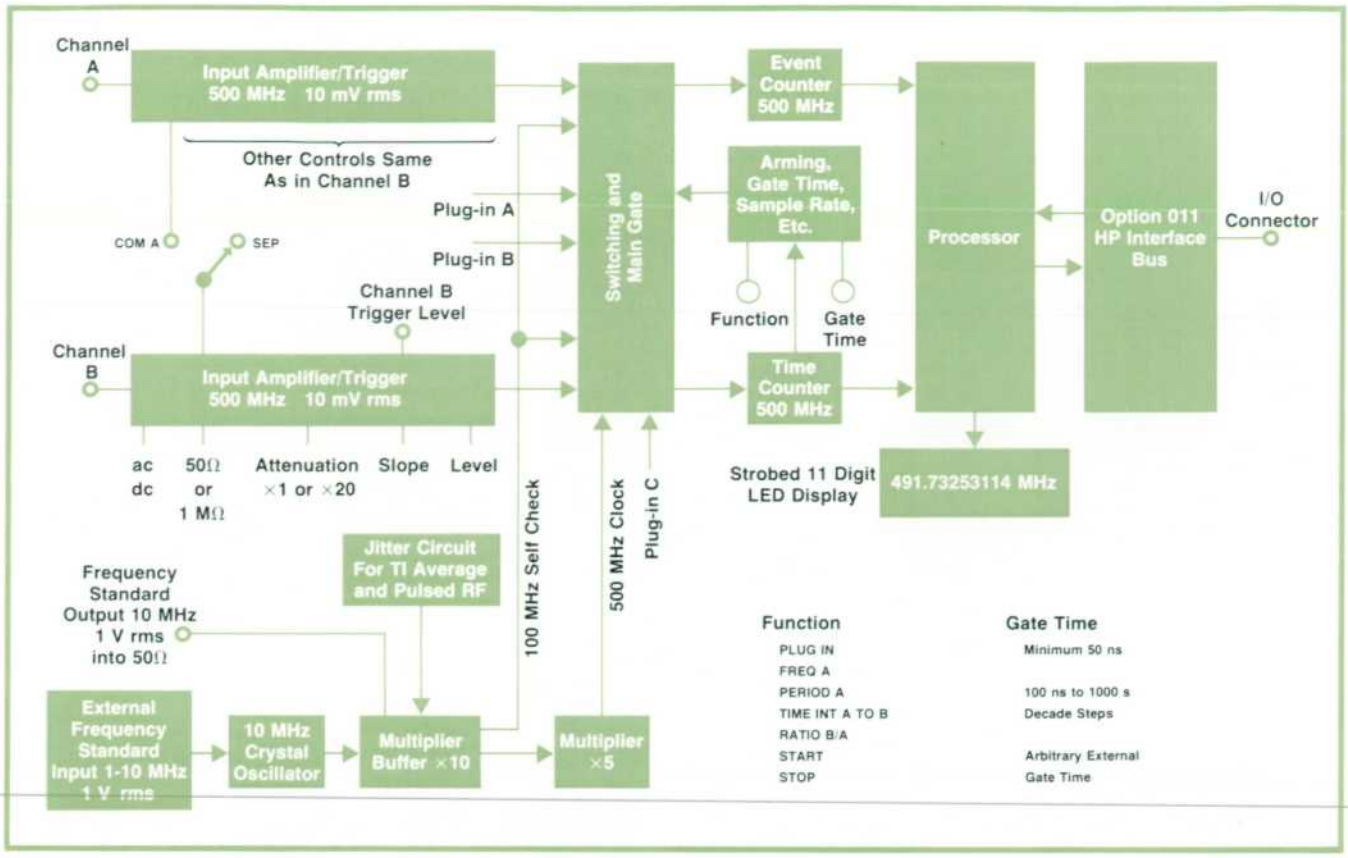


Fig. 5. *Model 5345A Counter's ROM-controlled processor performs various computation and control functions. For averaged measurements, jitter is added to the time base clock to eliminate coherence errors.*

are organized into 128 32-bit instructions. 62 qualifiers are used in the algorithmic state machine design (see article, page 9). Data storage and manipulation in this three-register machine are provided by three 16×4-bit T^2L RAMs.

Instruction inputs for the various arithmetic routines and subroutines come from front-panel or remote-control function definition, plug-in arithmetic requirements, output formatting instructions, and input data (contents of the event counter and time counter). For a frequency measurement, the event counter totalizes the number of cycles for a given unit of time defined by the time counter ±2 ns. Both event and time counters consist of $\div 10^{13}$ scaling registers. The highest-speed element is a 500-MHz Hewlett-Packard E^2L binary followed by an E^2L decade, the next quinary (25 MHz) is commercial Schottky T^2L and the last $\div 10^{11}$ dividers consist of HP PMOS $\div 10^5$ and $\div 10^6$ LSI divider chips.

Input Amplifier and Attenuator Design

The 5345A's 10-mV, 500-MHz input amplifier is a three-stage integrated-circuit design. Fig. 6 is its circuit diagram. The 500-MHz bandwidth is a result of three factors: the use of a fast IC technology that had previously been used only for digital circuits, the somewhat unusual circuit configuration, and frequency compensation of the circuit *on the IC wafer.*

The first stage is a series-shunt feedback pair, its low frequency gain proportional to $(R_{E1} + R_{F1})/R_{E1}$. Capacitor C_{E1} shapes the response at high frequencies.

The second stage is a dc level shifter and low-output-impedance emitter-follower impedance converter. Its purpose is to minimize loading of the first stage. The dc level shift is accomplished by using the emitter-base reverse breakdown voltage of a transistor, with the collector open to reduce offsets caused by leakage currents.

The third stage is a compensated cascode amplifier that reduces the Miller effect for large load resistors. Third stage gain is determined by resistor R_{E2} and capacitor C_{E2}.

An unusual aspect of this amplifier is the compensation of the overall response by adjusting C_{E1} and C_{E2} at the second metal layer. The second metal layer is used to interconnect small MOS capacitors to obtain a total capacitor value that will compensate for wafer-to-wafer processing variations. The choice of capacitor values is governed by measurements of

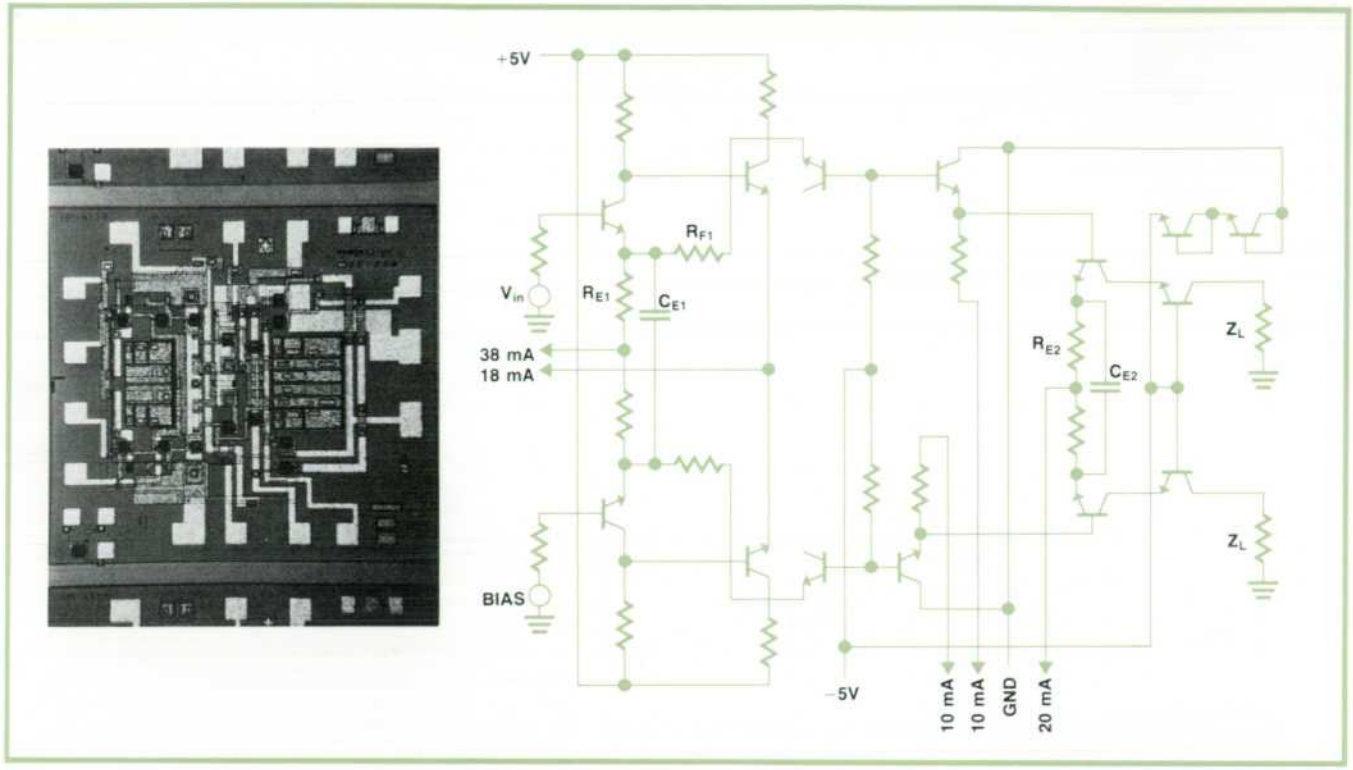


Fig. 6. *Dc-to-500-MHz input amplifier is one of the major design contributions in the 5345A.*

the characteristics of a test transistor and a test resistor on the IC wafer.

A photomicrograph of the integrated circuit is shown in Fig. 6. The MOS capacitors are visible as large rectangular metal areas. Also visible in the photomicrograph are several metal strips used in each capacitor, and the test transistor in the lower right-hand corner of the chip. The input resistance of the amplifier is greater than 10 kΩ and the equivalent input capacitance is less than 1 pF.[1]

This monolithic IC amplifier is incorporated into the input amplifier and attenuator design shown in Fig. 7. To meet the requirements of low-frequency, high-impedance measurements, the attenuator is constructed with high-impedance components. Frequency compensation in the attenuator extends its useful frequency response to beyond 500 MHz. The attenuator impedance is changed to 50Ω by a switched, compensated 50Ω termination.

To facilitate risetime or pulse width measurements, in which start and stop events occur on the same signal line, the two input amplifiers may be paralleled. In this mode, good termination is assured by a 50Ω power splitter.

High-Speed Logic

The key to making high-resolution single-shot time interval and/or fast bit-rate measurements on computer or communications digital data is the development of a family of digital logic of compatible speed. Currently, several manufacturers have some form of IC binary capable of toggling at rates in excess of 500 MHz. The problem that had to be solved to make a higher-performance counter possible was to develop logic circuits with enough gain and bandwidth to match the performance of the prescaling binaries.

5345A logic circuits are of E^2L (emitter-emitter logic) type.[2] E^2L differs from ECL (emitter-coupled logic) in that the E^2L output is an open collector whose logic swing is approximately 0V and −0.8V into an external 50Ω load, whereas ECL circuits have emitter-follower outputs and logic swings of approximately −0.8V to −1.6V. By means of a combination of techniques, including an unusual circuit configuration, useful frequency response of a typical E^2L gate has been extended to greater than 650 MHz. E^2L circuit outputs are compatible with 50Ω microstrip interconnect techniques, which are mandatory at the 500 megabit/second rates. Fig. 8 shows the 500-MHz logic circuit on a multilayer printed-circuit board using microstrip interconnect techniques.

Time Base

The accuracy of any counter depends ultimately on the stability of the time base. The standard time base for the 5345A Electronic Counter is a state-of-the-art 10-MHz oven-stabilized oscillator. The 10 MHz is multiplied to 500 MHz for clock purposes. Aging rate is under 5 parts in 10^{10} per day, and short-

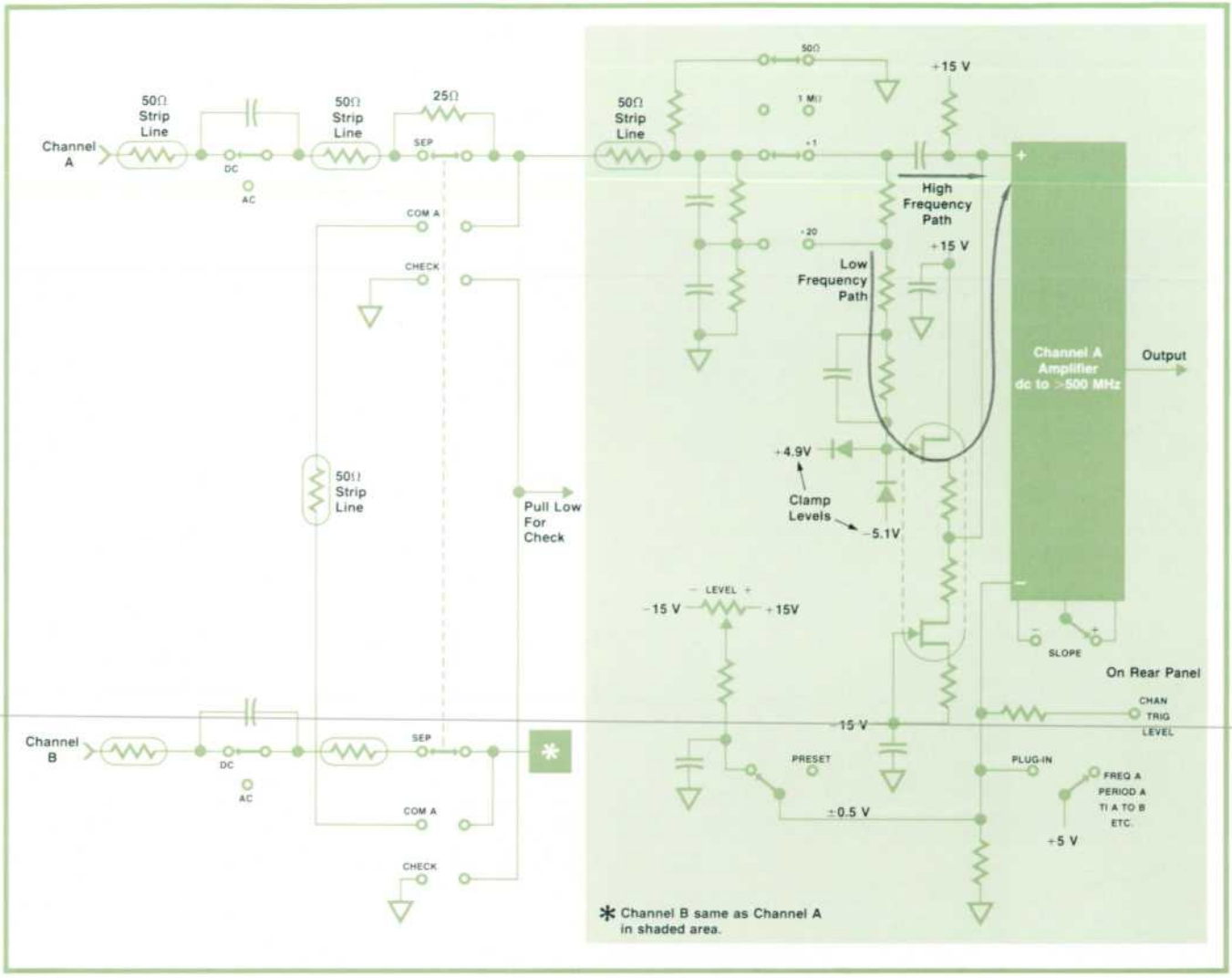


Fig. 7. *Input amplifier and attenuator. Input impedance is switchable, 1MΩ/30 pF or 50Ω.*

term stability is better than one part in 10^{11} for a 1-second average. This is the most stable standard-equipment oscillator in present-day commercial instrumentation.

Acknowledgments

The author is indebted to Merrill Brooksby, Dexter Hartke, John Dukes, and Darwin Throne for their leadership and encouragement throughout the years of development.

In addition to the several engineers who have authored other articles appearing in this journal, a special word of thanks must go to Steve Upshinsky for his design of the input amplifier and to Jose Furlan for his pioneer work on 500 MHz E^2L gates. John Gliever's RF design with associated noise modulation scheme made true time interval averaging possible. The product design by Keith Leslie afforded the electronic designers great latitude.

Successful production has been assured by the efforts of Tom Coates, who designed most of the production testing techniques, and Phil Deaver, whose production engineering effort has been outstanding. Holly Cole and Dick Holmes have assured us of a fine marketing and service program. Finally, a personal word of thanks to Dan Lansdon, whose early encouragement made it possible for me to enjoy the many opportunities at Hewlett-Packard.

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2. M. Brooksby, et. al., Fast Logic Extends Range of High-Frequency Counters", Electronics, Vol. 43, pp. 62-67, Dec. 7, 1970.
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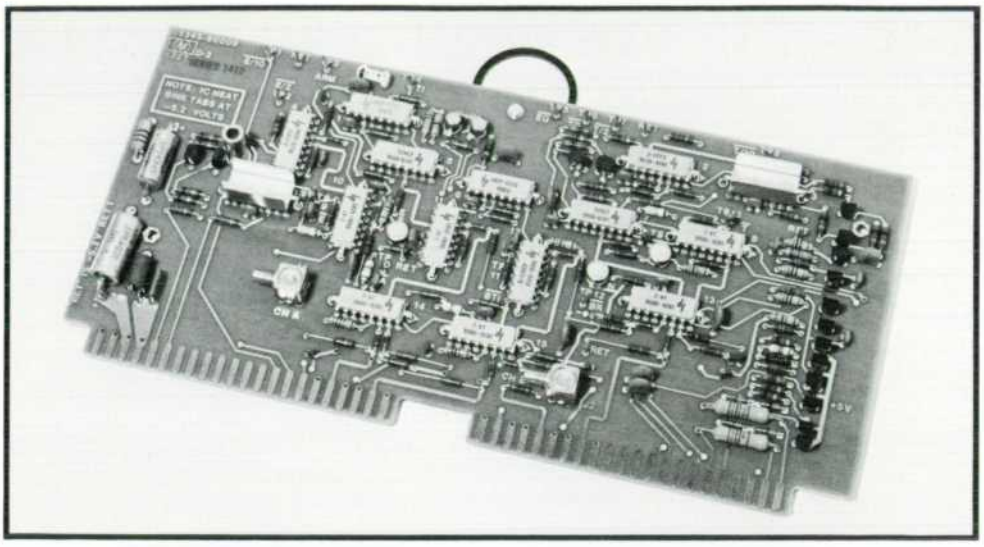


Fig. 8. *5345A main gate, a 500-MHz logic system. Multilayer printed-circuit boards and microstrip techniques contribute to the wide bandwidth.*

CONDENSED SPECIFICATIONS

HP Model 5345A Electronic Counter

Frequency, Frequency Average, Period, Period Average

Both frequency and period are measured by measuring the total elapsed time T, for an integral number of cycles, N, of the input waveform. Computation, involving the quantities of N and T, provides direct readout of either frequency or period.

RANGE: 50 μHz to 500 MHz; 2 nsec to 20,000 seconds.

MEASUREMENT TIME: Consists of GATE TIME plus the time required to reach the next STOP trigger level. When in MIN the GATE TIME is less than 50 nanoseconds. Decade GATE TIME ranges from 100 nsec to 1000 sec.

ACCURACY: Resolution is nine digits per second of measurement time. With DISPLAY POSITION switch in AUTO the least significant digit error is ±1 count if the most significant digit is 1 through 4, and ±2 counts if the most significant digit is 5 through 9. Accuracy is ±LSD counts ± time base accuracy ± trigger error.

Time Interval, Time Interval Average

RANGE: 10 nsec to 20,000 sec.

MINIMUM TIME BETWEEN TRIGGER POINTS: 10 nsec.

TRIGGER PULSE WIDTH: 1 nsec minimum width input at minimum voltage input.

ACCURACY:

TIME INTERVAL: ± trigger error ± 2 ns ± time base accuracy.

TIME INTERVAL AVERAGING: ±(trigger error ± 2 ns)/$\sqrt{\text{intervals averaged}}$ ± 7 nsec ± time base accuracy.

Not affected by harmonics of clock frequency.

RESOLUTION:

TIME INTERVAL: 2 nsec.

TIME INTERVAL AVERAGE: ±(2 ns)/$\sqrt{\text{intervals averaged}}$ ± 2 ps.

Ratio B/A

RANGE: Both channels accept dc to 500 MHz.

ACCURACY: ± L.S.D. ± trigger error.

MEASUREMENT TIME: Measurement time is equal to the GATE TIME selected times 500 MHz/frequency of channel B input.

Start/Stop

RANGE: Both inputs may have repetition rates from dc to 500 MHz.

MODES: A, A+B, and A−B is determined by a rear panel switch.

RESOLUTION: Not affected by GATE TIME setting. Resolution is one count up to eleven digits.

ACCURACY: Coincident pulses may be applied to both inputs. One count is required to initiate each input.

Scaling

RANGE: dc to 500 MHz.

OUTPUT: Output frequency equals input frequency divided by scaling factor. Rear panel BNC supplies 80% duty cycle TTL compatible pulses.

Input Channels A and B

RANGE: 0 to 500 MHz dc coupled 50Ω and 1 MΩ; 4 MHz to 500 MHz ac coupled, 50Ω; 200 Hz to 500 MHz ac coupled, 1 MΩ.

IMPEDANCE: Selectable: 1 MΩ shunted by less than 30 pF or 50Ω (nominal).

SENSITIVITY: X1, 10 mV rms sine wave and 30 mV peak-to-peak pulse. X20, 200 mV rms sine wave and 600 mV peak-to-peak pulse.

DYNAMIC RANGE: 30 dB.

TRIGGER LEVEL: Continuously adjustable to more than cover the DYNAMIC RANGE (±0.5V dc times the attenuator setting). Adjustment is noninear with more settability in the more sensitive region.

PRESET: Centers trigger level about dc at 25°C.

DRIFT: ±10 mV dc max., 0°C to 55°C.

OUTPUT: Rear panel BNC connectors bring out CHAN A TRIG LEVEL and CHAN B TRIG LEVEL for convenient DVM monitoring. Accurate to ±15 mV.

SLOPE: Independent selection of positive or negative slope.

Common Input

In this mode the signal is applied to channel A through a power splitter which equalizes impedances and delays to the input amplifiers. Channel B input is disabled. Both input impedance switches should be in the same position. All specifications are the same as for separate operation with the following differences.

RANGE: ac coupled 50Ω, 4 MHz to 500 MHz; ac coupled 1 MΩ, 300 Hz to 500 MHz.

IMPEDANCE: 50Ω remains 50Ω; 1 MΩ becomes 500 kΩ shunted by 60 pF.

SENSITIVITY:

50Ω: X1, 20 mV rms sine wave and 60 mV peak-to-peak pulse.
X20, 400 mV rms sine wave and 1.2V peak-to-peak pulse.

1 MΩ: No change.

TRIGGER LEVEL: Continuously adjustable over the range of ±1V dc in 50Ω and ±0.5V dc in 1 MΩ multiplied by the attenuator setting.

General

SAMPLE RATE: Continuously variable from <0.1 sec to >5 sec with front panel control. In HOLD position the last reading is maintained until the counter is manually reset or an EXTERNAL ARM signal is applied. Number of readings per second will generally be limited by the output device, i.e., 5050B Printer or 9820A Calculator. In COMPUTER DUMP mode the counter can take up to several thousand readings per second.

EXTERNAL ARM INPUT: Counter can be armed by a −1.0V signal applied to the rear panel 50Ω input. The signal should be applied for more than 50 nsec. Minimum time between EXT ARM and acceptance of start pulse is <1 μsec.

EXTERNAL GATE INPUT: Same conditions as for EXT ARM. Minimum time between EXT GATE and acceptance of start pulse is <20 nsec.

GATE OUTPUT: >1 volt into 50Ω.

TIME BASE: Standard High Stability Time Base. Crystal Frequency, 10 MHz (10544A).

STABILITY

Aging Rate:	$<5 \times 10^{-10}$ per day
Short Term:	$<1 \times 10^{-11}$ for 1 sec average

For oscillator off time less than 24 hrs.

SELF TEST: A 100 MHz signal is internally applied for testing all functions. Pushing RESET illuminates all segments of display digits. Seven internal diagnostic switches are provided for verifying the operation of the input amplifiers, digital front end, processor and plug-ins.

EXTERNAL FREQUENCY STANDARD INPUT: Input voltage >1.0V rms into 1 kΩ required from source of 1, 2, 2.5, 5, or 10 MHz. $\pm 5.0 \times 10^{-6}$. Input can be sine or square wave.

FREQUENCY STANDARD OUTPUT: >1V rms into 50Ω at 10.0 MHz sine wave.

OPTION 001: Room Temperature Time Base.

OPTION 002: Same as 5345A but with no input amplifiers. Signal must be applied through plug-in.

OPTION 010: Digital output only. HP Interface Bus format, ASCII talk only. Useful with 59301A ASCII-to-Parallel Converter and 5050B or 5055A Digital Printers.

OPTION 011: Digital Input/Output. Full compatibility with HP Interface (ASCII) Bus. Provides digital output as well as input for control over all functions except input amplifier. Allows counter to operate with all ASCII Programmable Modules (see 59300 series) and Controllers such as card readers, calculators, and 2100 series computers.

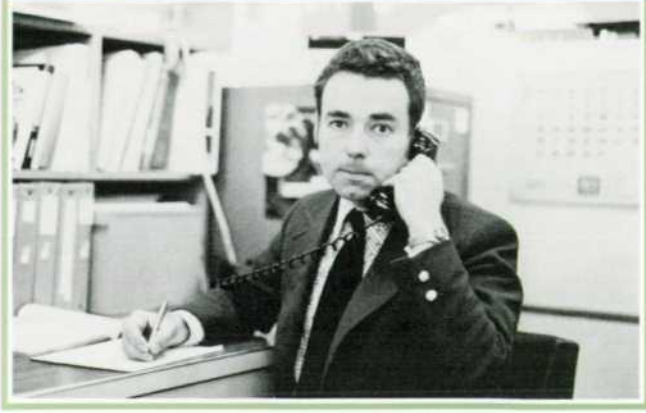
Accessories Available

10593A: 5345A TO 9820A INTERFACE KIT: Includes ASCII I/O card and PCII ROM, 10631B, 10631C, documentation and 5345A Self Test Software Package. To be used with 5345A Option 011 and 9820A Calculator.

10590A PLUG-IN ADAPTER: Increases usefulness of 5345A by providing interface to 5245L plug-ins. In all cases the plug-ins operate in a similar manner as they do in the 5245L.

PRICE IN U.S.A.: 5345A, $3450.

MANUFACTURING DIVISION: SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050 U.S.A.



James L. Sorden

Jim Sorden is project manager for the 5345A Electronic Counter. He first joined HP in 1962 after receiving his BSEE degree from the University of Wisconsin. After a while the promise of greener pastures lured him elsewhere, but by October, 1964 he was back to stay. Jim's responsibilities at HP have been heavily concentrated in digital circuit and systems design and high-frequency integrated-circuit design. Earlier he served as project leader for a multichannel analyzer system. An amateur winemaker who also enjoys gardening, sailing, and skiing, Jim is a native of the state of Wisconsin. He and his wife and two small children live in Saratoga, California.

The 5345A Processor: An Example of State Machine Design

by Ronald E. Felsenstein

THE 5345A PROCESSOR is an example of state machine design.[1] The first step in the design of such a machine is to draw a flow diagram showing all processor functions. Fig. 1 is a section of a typical flow diagram.

The rectangular boxes in the flow diagram represent states. The machine spends sufficient time within a state to execute all the commands that are active. A command might be something very simple, such as resetting a flip-flop or incrementing a counter. A more sophisticated example, one used in the 5345A processor, is a subtraction involving two serial strings of 16 binary-coded-decimal (BCD) digits. Subtraction takes a combination of commands. Two commands gate 16 clock pulses to shift the data through a BCD adder/subtractor, one command puts the BCD adder/subtractor in "subtract" mode, and several commands route data so the resulting difference is fed back to one of the subtracting storage elements while the contents of the other storage element remain unaltered.

Once sufficient time has elapsed for all of the commands to have been executed, one of two new sets of commands will be executed. Which new set is executed depends on the status of a qualifier.

An example of a 5345A qualifier is the status of a carry flip-flop that determines whether the result of a subtraction is positive or negative. Some qualifiers require considerable hardware for generation. For example, the display is made more readable by an automatic display formatting algorithm (AUTO), which gives the displayed digits an annunciator multiplier computed so the decimal point is within the first three positions to the right of the most significant digit. The position of the most significant digit varies according to the number of digits of resolution (in AUTO, the least significant digit is always right justified within the display). The generation of the qualifier that determines whether the AUTO criterion has been met requires a subtractor that outputs the difference between a counter containing the decimal point code and a four-bit latch storing in binary form the number of digits of resolution. The output of the subtractor is then further examined with combinational logic to determine whether it ranges between -1 and -3. If the difference is between -1 and -3, the AUTO criterion has been met. This qualifier is further complicated by having to recognize three special cases where the AUTO criterion of decimal point positioning cannot be met.

Each state box within the flow diagram is coded to distinguish it from any other state box. These codes are represented in Fig. 1 by the encircled letters. Thus if state (X) occurs at time T, then (Y) or (Z) will occur at time T+1. The process is continuously repeated as the flow diagram is sequentially executed.

ROM Addressing

When the number of states and commands is large, as it is in the 5354A, it makes sense to use read-only memories (ROMs) to store the flow-diagram program. A block diagram of the first scheme that was consid-

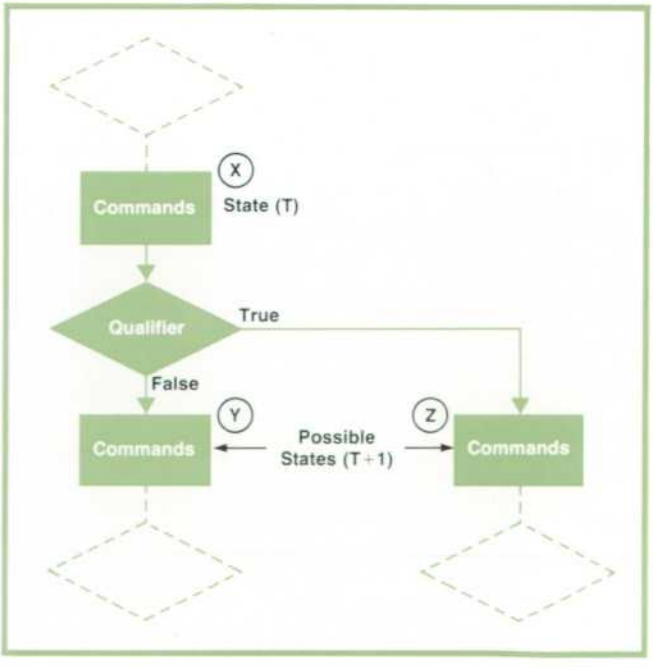


Fig. 1. *A segment of the flow diagram of a state machine. As the commands of the present state are completed, a qualifier is tested to determine which of two possible states will be the next state of the machine.*

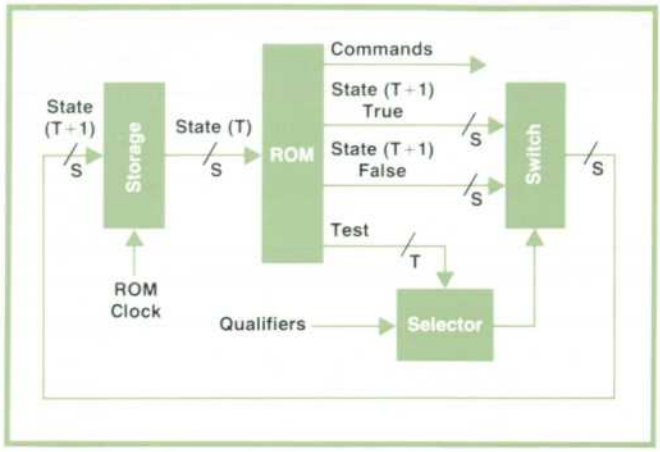


Fig. 2. *State-qualifier-pair ROM address structure, a typical way to implement a state machine.*

ered for the 5345A, a state-qualifier-pair ROM address structure,[1] is shown in Fig. 2. The storage circuit contains the code (X) at state time T. There are S bits in the state code; these become the inputs or addresses to the ROM. For every address presented, the ROM has been programmed to produce four output fields. The COMMANDS field activates all the lines needed to satisfy the requirements of a flow-diagram state-box description.

The STATE (T+1) TRUE field contains the S-bit code representing the state at time T+1 if the qualifier following state (X) is true; for Fig. 1 this would be the code representing state (Z). Similarly, the STATE (T+1) FALSE field contains S bits and represents the qualifier-false address or the (Y) code in Fig. 1.

The TEST field addresses a selector (multiplexer) to select the qualifier required by the flow diagram. The test field requires T bits such that $2^T \geq Q$, where Q is the number of unique qualifiers in the flow diagram description.

The qualifier selected then controls the switch so the STATE (T+1) TRUE code is supplied to the storage circuit if the qualifier is true, and the STATE (T+1) FALSE code is supplied if the qualifier is false. Upon completion of state (X), the ROM CLOCK signal initiates the new state, which will be either (Y) or (Z). This cycle repeats for every state box in the flow diagram until the flow diagram is completed.

The hardware disadvantage of the state-qualifier-pair ROM address structure is that many ROM outputs are used just for stepping through the flow diagram. Furthermore, at a given state time, the S-bit field that does not get selected by the qualifier-controlled switch serves no useful purpose. It is unlikely that any of the STATE (T+1) TRUE or STATE (T+1) FALSE bits could also serve as command lines.

In the 5345A, the state-qualifier-pair ROM address structure would have used 20 ROM outputs. The address structure that was finally used is a modification requiring only six ROM outputs (see Fig. 3).

The reduction of ROM outputs was achieved by coding the STATE (T+1) TRUE and STATE (T+1) FALSE codes so they differ in only one bit. That bit is established directly by the selected qualifier. This means that for STATE (T+1) addressing, only S−1 ROM outputs are required.

The final reduction was achieved by eliminating the TEST field entirely. This was possible because of the large number of unique qualifiers that the 5345A flow diagram definition required. Had a separate TEST field been used, the number of TEST bits would be S−1; thus it made sense to address the selector with the S−1 bits directly.

Command Generation

When the definition of the 5345A was complete, the S field was seven bits long and the COMMAND field was 39 bits long. The only circuits that were commercially available in both ROM and PROM* versions had 1024 bits arranged with an eight-bit input address and four-bit output (256×4 organization). To convert to a seven-bit input, eight-bit output circuit (128×8 organization), the ROM is given two addresses at every state time and the ROM outputs during the first address are stored (see Fig. 4).

A new state code is presented to the ROM every time a ROM CLOCK pulse occurs and MSB (the most significant bit of the ROM address) is high. After the ROM outputs reach steady state, a WORD DOUBLING CLOCK pulse causes them to be stored and the MSB=1 outputs to be generated. Then MSB goes low, offering a new address to the ROM and causing a new set of ROM outputs, called MSB=0 outputs, to be generated.

*The PROM (Programmable Read-Only Memory) saves time and money in the design stage. PROMs are also useful for implementing customers' special requirements.

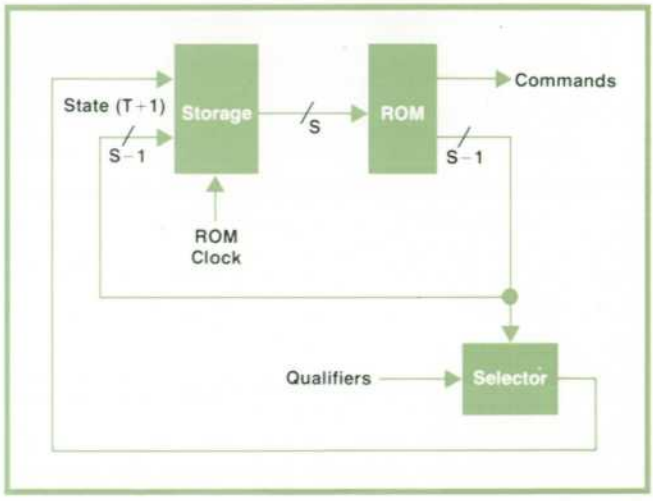


Fig. 3. *5345A ROM address structure reduces ROM output requirements.*

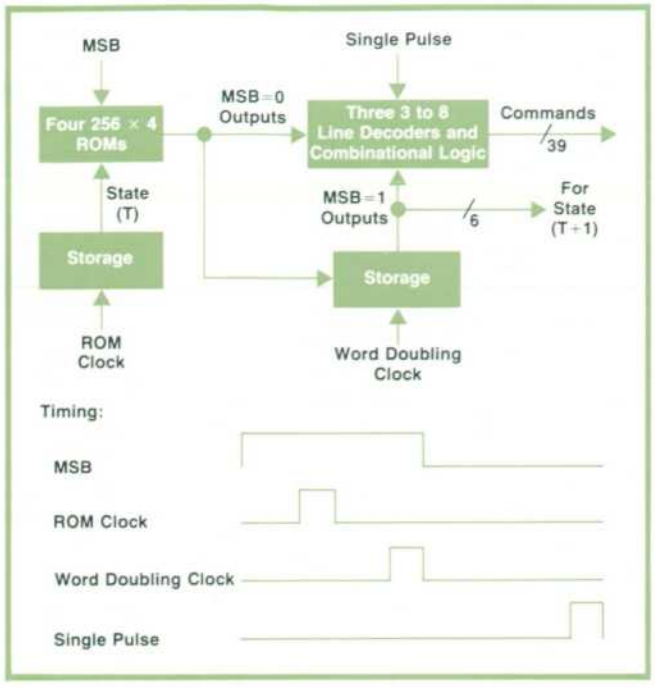


Fig. 4. *5345A command generation scheme.*

Because the MSB=1 outputs are stored, they have no transients, but the MSB=0 outputs cannot be relied upon while MSB is high. To take care of the MSB=0 output transients, a signal called SINGLE PULSE is generated after the MSB=0 outputs achieve steady state. The MSB=0 outputs are gated with SINGLE PULSE so the hardware looks at these outputs only when their information is correct.

Even after doubling the number of ROM outputs, if all the 39 commands had been derived directly from the ROM in addition to the S−1 or six bits for the STATE (T+1) field, the processor would have required 6K of ROM. This would have increased the price and power consumption of the processor.

With the aid of a "bit packing" computer program developed at HP Laboratories, the amount of ROM was reduced to 4K. The first step in the bit packing procedure was to feed the program with a complete listing of the STATE (T) and STATE (T+1) codes, and the status of each command bit (active, inactive, or don't care). The program then reduced the number of ROM outputs required by finding sets of mutually exclusive commands that could be derived from a decoder, and commands that could be generated by simple logic-gate combinations of other commands, STATE (T), and/or STATE (T+1) bits.

Originally, there were 45 ROM outputs: 39 commands and six STATE (T+1) lines. After bit packing only 29 outputs were required. On four 1K ROMs with 128×8 organization, three ROM outputs remain free for possible future use.

Hardware

As the flow diagram of a state machine is developed, hardware requirements become apparent: storage elements, flip-flops, counters, and so on. During definition of the 5345A, flow diagram and hardware development went hand in hand, each affecting the minimization of the other.

The processor was built with TTL circuits. To handle 15-digit binary-coded-decimal arithmetic, there are three 16-by-4-bit random-access memories and a BCD adder/subtractor. Two six-bit counters are used to store decimal point information. Latches store the multiplier for the annunciators, the sign, and the overflow light of the display. Additional counters, latches, and flip-flops are used for special purposes such as counting and storing the number of digits of resolution.

Acknowledgments

Credit for design contributions is due Jim Sorden, Bob Livengood, and Tommy Thomason. Special thanks go to Gerry Alonzo for his help in "packing ROM bits" with the computer program, and Chuck McWilliams for his idea that made our ROM simulator possible. Finally, I would like to thank Tom Coates for making the processor boards computer testable.

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Ronald E. Felsenstein

Ron Felsenstein received his BS degree in electrical engineering from Massachusetts Institute of Technology in 1969 and joined HP the same year. Designer of the digital processor for the 5345A counter, he has now been named production engineer for lasers and logic test instruments. Ron was born in Montevideo, Uruguay. He and his wife recently returned there for a visit during a two-month tour of Uruguay, Mexico, and six other countries in Central and South America. At home in Santa Clara, California, Ron is currently busy rebuilding a 1961 Mercedes-Benz, but he also enjoys camping, tennis, hiking, and skiing.

Time Interval Averaging: Theory, Problems, and Solutions

by David C. Chu

TIME INTERVAL AVERAGING is an easy and economical way to increase resolution in measuring repetitive time intervals. The idea is quite simple: the same interval is measured repeatedly and, given some degree of independence between measurements, the ±1 count quantization error in each measurement is statistically reduced if the average measurement value is used to estimate the interval.

There are many pitfalls in making measurements this way. My purpose here is to point these out and describe the approaches used in the 5345A to solve these problems.

The Folly of Direct Gating

In one all too obvious implementation of time interval averaging, the time interval repeatedly enables a gate through which the clock pulses are passed and counted. Unfortunately, when the gate turns on and off, partial clock pulses are generated and fed to the counting circuits. The average value obtained this way is as much a function of the response of the counter to partial pulses as it is to the width of the interval. Because this response is difficult to characterize reliably and even harder to control accurately, one can attach no meaningful significance to the average value so obtained. In general, for averaging over a large number of measurements, a biased value, which can differ significantly from the true time interval value, will be approached. The difference can be expressed as:

$$\text{partial pulse bias} = T_0\frac{d}{100}(1 - 2r) \qquad (1)$$

where T_0 is the clock period, d is the duty cycle of the clock in percent, and r is the fraction of the full clock pulse below which the counter does not respond. The parameter r, which is always between 0 and 1, cannot be controlled precisely.

The use of a synchronizer in HP averaging counters eliminates the partial pulse problem by reducing the effective duty cycle (d) to zero.[1] The decades are fed full-width pulses under all conditions. The remainder of this article assumes the use of synchronizers.

Non-Averaging Because of Coherence

Another fundamental problem of time interval averaging occurs when the time intervals are repeated at a rate coherent with the clock frequency. For example, if the rate is a submultiple of the clock frequency, the occurrence of the time interval relative to the clock phase is the same for each measurement. Hence, all the measurements read exactly the same and no statistical averaging takes place. In this case, the quantizing error for a million measurements is no different from that for a single measurement.

Coherence, unfortunately, is not limited to submultiples. There are other rates at which only partial averaging takes place. For example, rates given by $f_0/(Q+\frac{1}{2})$, where f_0 is the clock frequency and Q is a positive integer, give rise to two alternating discrete clock phases separated by $T_0/2$. Averaging over a large number of measurements is no better than averaging over two successive measurements.

In general, we can partition the coherent rates into classes. A "class-M" rate results in the time interval's occurring at M discrete phases of the clock. If one is interested in gaining resolution improvement by, say, a factor of 100 over the clock period, a class-M rate where M is under 100 would be unacceptable. A class-M rate is given by:

$$f_R(M) = \frac{f_0}{Q + \frac{L}{M}} \qquad M = 1,2,3... \qquad (2)$$

where $f_R(M)$ is a class-M rate, Q, L, and M are non-negative integers, and $L \leq M$. Furthermore, L and M are co-prime, that is, they have no common factors. For M = 1, the class of submultiples is generated.

These rates are very numerous. In fact, there is an infinite number of rates for each class.

Coherence Bandwidth

If one is interested in gaining resolution by a factor of N, how far must the time interval rate depart from one of the coherent rates f_R to assure proper averaging? Straightforward analysis of the phase of the intervals at these frequencies shows that for a

class-M rate f_R, a departure of $\pm\Delta f_R$ from f_R can result in almost perfect averaging by the factor N, where Δf_R is given by:

$$\Delta f_R = \frac{f_R^2}{f_0 MN} \quad (3)$$

The coherence bandwidth is $2\Delta f_R$.

In terms of fractional frequency stability $\Delta f_R/f_R$, the stability that would cause the non-averaging effect is:

$$\frac{\Delta f_R}{f_R} = \frac{f_R}{f_0 MN} \quad (4)$$

Conversely, any stability worse than this destroys the coherence and allows the reduction of measurement quantization error by statistics.

The coherence bandwidth is large for high rates and low M, and non-averaging can often be observed without instrumentation. Submultiples (M=1), for example, give rise to measurements always equal to or close to whole clock periods, an easily discernible effect. Partial averaging is more subtle, and the experimenter is often led to accept a result which does not give an adequate interpolation factor.

Time Base Random Phase Modulation

Coherence between the time interval pulse train and the time base clock pulse train can be destroyed by introducing random phase modulation to either or both of the trains, allowing meaningful time interval averaging measurements to be made without regard to the time-interval rate. In the HP 5345A Counter, phase modulation is deliberately introduced into the clock pulse train when making time interval average and pulsed RF measurements. The modulation is random Gaussian noise band-limited to approximately 3 kHz.

The bias errors caused by the non-averaging effect are functions of many parameters, including the time interval rate, the fractional part of the time interval (obtained by subtracting all whole clock periods from the time interval), and the interval-to-clock phase relationship. However, the *worst case* bias error, E_B, can be expressed simply as a function of σ, the rms value of the phase modulation:

$$E_B = T_0\left[\sum_{n=-\infty}^{\infty}\int_{n-1/4}^{n+1/4}\frac{1}{\sqrt{2\pi}\sigma}\exp\left\{\frac{x^2}{2\sigma^2}\right\}dx - 1/2\right] \quad (5)$$

where E_B is the non-averaging bias error and σ is the rms value of the phase modulation in units of 2π radians or periods of the time base clock.

Fig. 1 shows a plot of bias error E_B versus σ in radians, assuming a 2-ns clock period, and a time interval given by $2(Q+\frac{1}{2})$ ns. The bias error decreases rapidly with increasing phase modulation. This indicates that the phase modulation should be large. However, as will be shown, another type of error demands just the opposite.

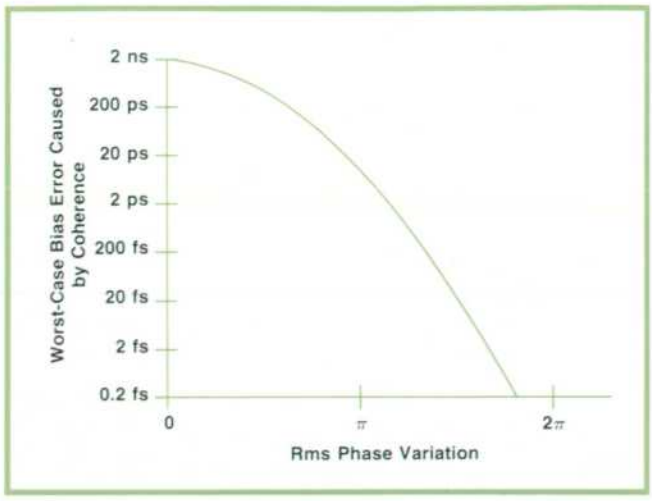

Fig. 1. *Coherence bias error in time interval averaging is reduced by increasing random phase modulation of the counter time base.*

Modulation Bandwidth

There are also two opposing requirements on the phase modulation bandwidth. With a large bandwidth, time intervals can arrive rapidly and still maintain relative independence between measurements. On the other hand, for very large modulation bandwidths and relatively long time intervals, there may be only limited correlation between the time base at the start edge and at the stop edge, and the measurement accuracy may be degraded by time base short-term instability.

Quantitatively, the relationship is as follows. For a given time interval τ seconds, modulation bandwidth f_c (Hz), and rms phase modulation σ (cycles), the rms error caused by time base uncertainty in a single measurement is given by E_{TB}, where

$$\text{rms value of } E_{TB} = T_0\sigma\left[2\left(1 - e^{-2\pi f_c|\tau|}\right)\right]^{1/2} \quad (6)$$

seconds. For a given time interval, this error is smaller for a smaller modulation bandwidth. Thus a small modulation bandwidth is desirable.

With averaging, this error is reduced by the factor $1\sqrt{N}$, where N is the number of *independent* measurements. Not all measurements averaged are independent if the time interval rate exceeds approximately twice the modulation bandwidth. In this latter respect, a large bandwidth is desirable because it makes full use of all measurements made at higher rates.

Notice that E_{TB} increases linearly with σ, the rms phase modulation, in contrast with the coherence error, which decreases with σ.

Normal ±1 Count Quantization Error

Even if the time interval rate is incoherent and time base uncertainty error is negligible (such as when measuring short time intervals), an error is expected in time interval average measurements because of the normal ±1 count quantization error in each measurement.* For a given time interval $\tau = T_0 (Q+F)$, where Q is an integer and F a proper fraction, this quantization error can take on only two fixed values, FT_0 and $(F-1)T_0$, with probabilities $(1-F)$ and F respectively. The mean of this distribution is zero, and the standard deviation (rms value) is $T_0[F(1-F)]^{1/2}$. The worst case occurs when F is 1/2, with the corresponding worst case rms quantization error of $T_0/2$. With proper averaging over N independent measurements, this rms error is reduced by the familiar factor $1/\sqrt{N}$.

Measurement Error Summary

Three types of errors in time interval averaging have been discussed. They are non-averaging bias error, time base short-term uncertainty error, and normal quantization error.

The first error is caused by coherence and can be as large as one whole clock count. It is independent of the number of measurements averaged. This error can be reduced to a negligible level according to Fig. 1 by randomly phase modulating the time base clock. In the 5345A Counter, random phase modulation of 0.8 cycle rms minimum allows meaningful time interval average measurements without regard to the time interval rate.

The second error is a result of time base uncertainty caused by the random phase modulation introduced. For measuring time intervals less than 7 μs with the 5345A, this time base error is completely dominated by the quantization error, and is therefore negligible. For measuring time intervals much larger than 7 μs, the measurement deviation is increased by a factor of approximately 2.7 above that due to the normal ±1 count quantization error. This increase can be nullified by averaging more intervals.

The third type of error is a result of quantization to whole numbers in the counting process and is a function of many parameters. The worst case occurs when the time interval has a value half way between whole clock counts, giving an rms error $T_0/2$. Like time base uncertainty error, quantization error is reduced if averaged over N independent measurements by the factor $1/\sqrt{N}$.

There are other errors in time interval measurements, caused primarily by non-ideal circuit components. Examples are start-stop channel mismatch, trigger error, and plain old thermal noise. These errors are important, but have been excluded from this discussion, which is limited to those errors that are unique to the time interval averaging process.

*"±1 count" is actually a misnomer when synchronizers are used, because they make it impossible to have an error exactly equal to one count.

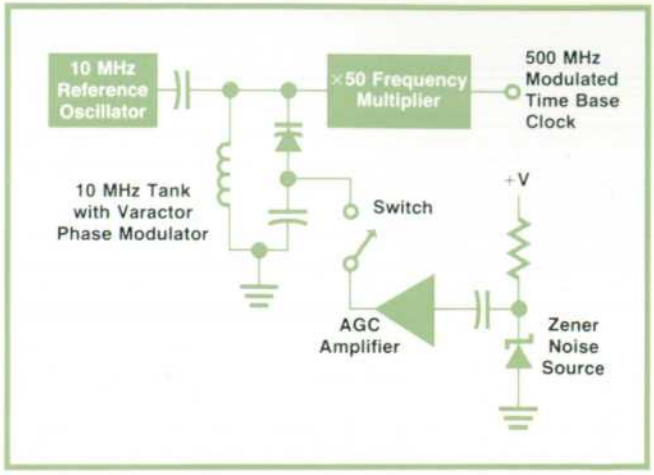

Fig. 2. *Implementation of time-base-clock random phase modulation in the HP 5345A. The switch is closed only for time interval average and pulsed RF measurements.*

In the 5345A Counter, the phase modulating signal is derived from noise generated by a zener diode. The noise is amplified and filtered before being used to modulate the phase of the clock at 10 MHz with an rms value of approximately 7°. The frequency multiplier chain effectively increases this value by a factor of 50 to about 350°. The noise voltage level is accurately controlled at all times by a feedback loop. A block diagram of the implementation scheme is shown in Fig. 2.

FM versus PM

There are two fundamental reasons why phase

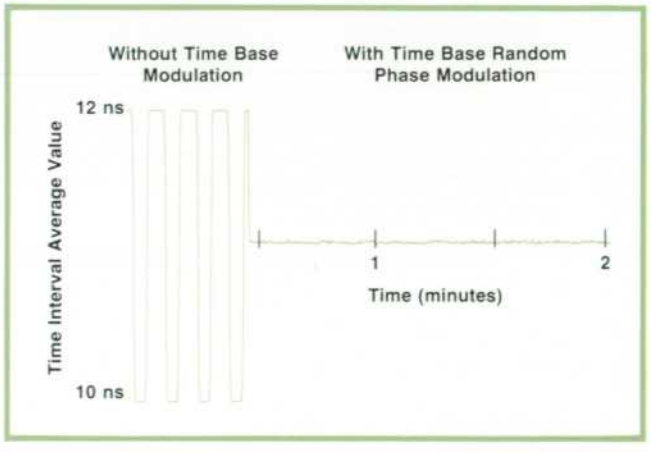

Fig. 3. *Effectiveness of time base random phase modulation is demonstrated by this time record of the counter reading during a time interval average measurement. Time intervals arrive at a rate of 50 MHz + 0.1 Hz, which is nearly coherent with the 5345A clock frequency of 500 MHz. Without modulation, the reading is either 10 ns or 12 ns. Modulation results in a true reading of approximately 11 ns.*

modulation (PM) of the clock is superior to frequency modulation (FM) for time interval averaging. First of all, it is the phase variations that destroy the coherence. Of course, phase variations are also generated by FM, but they decrease at 6 dB/octave as the modulating frequency is increased. Therefore, to obtain sizeable and rapid phase variations, relatively large FM signals must be used.

A more fundamental reason is that with FM, the mean value of the modulating function must be *absolutely zero* or errors will accumulate as the time base drifts. Zero mean modulation is difficult to obtain with nonlinear modulation circuits. With phase modulation, this zero mean value is not a necessity, because any constant phase offset is effectively cancelled by the start/stop process.

An Experiment

A simple experiment was performed to illustrate the effectiveness of phase modulation of the clock. Time intervals arriving at a rate nearly coherent with the 5345A clock frequency were measured with and without modulation. Fig. 3 shows the result.

Acknowledgments

The author received many useful comments from conversations with Art Muto, Jim Sorden and Ken Jochim, all of whom had been doing pioneering work in time interval averaging for some time. The elegant implementation of the phase modulation is a result of the ingenuity and expertise of John Gliever and John Dukes.

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APPENDIX

Time Interval Estimation in the Presence of Quantization Error

For measuring short intervals by time interval averaging, only ±1 count quantization error is present. An interesting problem is to determine the statistics of estimating the true time interval from the reading obtained from averaging N independent measurements. The usual rule-of-thumb estimate gives this uncertainty as $T_0/\sqrt{N}$ where T_0 is the clock period. A more formal analysis shows that the actual rms uncertainty of the estimate is not so simply stated. In fact, the actual probability density function of the interval can be computed given the counter reading after averaging N independent measurements. The results can be summarized as follows.

An unknown time interval τ is measured N independent times with a clock period of T_0. The average value of the measurements is $\bar{\tau} = T_0(P+K/N)$ where P and K are integers and $0 \leq K < N$. What is the probability density function of $e = (\tau - \bar{\tau})$ given P, K, and N? Assuming no *a priori* knowledge of τ, maximum likelihood estimation may be used, and the result is as follows:

Case I: K = 1,2,3,...,N−1. The probability density function P(x), that is, the probability density of $(\tau - \bar{\tau})$ taking on value x, is

$$P(x) = \frac{N+1}{T_0}\binom{N}{K}\left(1 - \frac{K}{N} - \frac{x}{T_0}\right)^{N-K}\left(\frac{x}{T_0} + \frac{K}{N}\right)^{K} \quad (1)$$

for $-KT_0/N \leq x < (1-K/N)T_0$

$= 0$ otherwise

The mean of this distribution is $\frac{T_0(N-2K)}{N(N+2)}$ and the standard deviation is σ_τ, where

$$\sigma_\tau = \frac{T_0}{N+2}\left[\frac{(N-K+1)(K+1)}{N+3}\right]^{1/2} \quad (2)$$

Case II: K = 0. The probability density function P(x) for this case is

$$P(x) = \frac{N+1}{2T_0}\left(1 - \frac{x}{T_0}\right)^{N} \quad \text{for} \quad 0 \leq x \leq T_0 \quad (3a)$$

and

$$P(x) = \frac{N+1}{2T_0}\left(1 + \frac{x}{T_0}\right)^{N} \quad \text{for} \quad -T_0 \leq x \leq 0 \quad (3b)$$

The standard deviation of this function is σ_τ, where

$$\sigma_\tau = \left[\frac{2}{(N+2)(N+3)}\right]^{1/2} T_0 \quad (4)$$

These results show that the rms uncertainty in estimating the time interval by the average measurement value is a function of K as well as of N. The parameter K, always an integer, can be obtained directly from the measurement: K/N is the fractional part of the normalized measurement value $(\bar{\tau}/T_0)$. For large N, which is typical for most time interval average measurements, the rms uncertainty of equation 2 is reduced to

$$\sigma_\tau = T_0\left[\frac{\left(1 - \frac{K}{N}\right)\left(\frac{K}{N}\right)}{N}\right]^{1/2} \quad (5)$$

For a given N, the largest σ_τ, representing the worst case estimation uncertainty occurs when K/N is one-half. The corresponding rms uncertainty is $T_0/2\sqrt{N}$. The uncertainty becomes less when K/N approaches either 0 or 1. The rule-of-thumb estimate of $T_0/\sqrt{N}$, therefore, represents twice the worst case rms uncertainty for large N. One can further use the knowledge of the fractional part of the measurement value to increase confidence in estimating the time interval.

David C. Chu

Dave Chu holds BS, MS, and PhD degrees in electrical engineering, the BS from the University of California at Berkeley in 1961 and the MS and PhD from Stanford University in 1962 and 1973. At HP since 1962 (except for a 1967-69 leave of absence to teach physics and mathematics at Cuttington College in Liberia), Dave has contributed to the design of many of HP's top-of-the-line counters. A member of IEEE and the Optical Society of America, he's an expert on computer holography and inventor of the ROACH, a single transparency with controlled complex transmittance. He's authored many papers and patent applications in the fields of optics, information theory, statistics, and electronics. Dave was born in Hong Kong. He's married, has two children, and lives in a "shack"—which he's currently remodeling—on five acres of land in rural Woodside, California. He's active in his church and political party, and confesses to being addicted to Balkan and Israeli folkdancing.

Third Input Channel Increases Counter Versatility

by Arthur S. Muto

MODEL 5353A CHANNEL C PLUG-IN contributes several new and useful measurement capabilities to the 5345A Electronic Counter. It was conceived primarily as a solution for many measurement problems in the new and expanding field of high-speed digital measurements, but it is useful for many other applications as well.

The channel C plug-in, Fig. 1, adds a third, 10-millivolt-rms-sensitivity, dc-to-500-megahertz input channel to the two channels of the mainframe.

Three of the measurement modes of the channel C plug-in, namely FREQ C, PERIOD C, and RATIO C/A, duplicate functions found in the mainframe. As a consequence, frequency or period measurements can be made on two different signals in a systems or production environment without having to disconnect coaxial cables or reset trigger levels. One signal can be measured with the mainframe's channel A and the other with the plug-in's channel C. Similarly, the plug-in can be used to make a multiplexed ratio measurement with channel A by selecting either the mainframe's RATIO B/A function or the plug-in's RATIO C/A function.

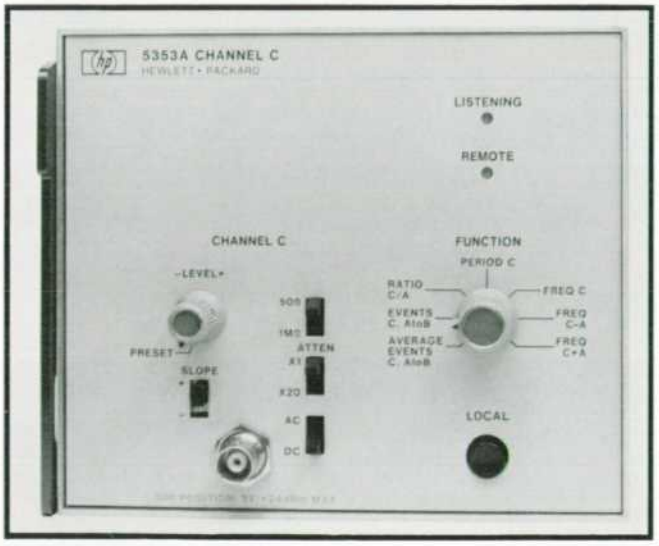


Fig. 1. *Model 5353A Channel C Plug-in adds a third 10-mV-sensitivity, 500-MHz input channel to the two 5345A mainframe channels.*

A fourth function of the channel C plug-in permits automatic sum and difference frequency measurements to be executed by selecting FREQ C+A, or FREQ C−A. A direct application of this measurement is in determining a receiver input frequency by separately measuring the local oscillator frequency (LO) and the intermediate frequency (IF) and performing the sum or difference (LO ± IF) calculation. By connecting the LO to channel C and the IF to channel A, automatic LO±IF measurements can be performed.

A nulling technique for making frequency adjustments is another application of FREQ C−A. With a standard frequency source connected to channel A, the frequency of the channel C signal can be adjusted until the counter displays zero. The frequency of the channel C input signal is then equal to the frequency of the standard source.

Events Mode

Still another measurement mode of the 5353A Channel C Plug-In is called EVENTS C,A to B. In this mode, channel C events—pulses as narrow as one nanosecond in width—are totalized during a precise time interval defined by a start-pulse edge in channel A and a stop-pulse edge in channel B. The polarity of the pulse edge is determined by the user's selection of positive and/or negative trigger slopes (Fig. 2).

In the digital communications field, this EVENTS measurement is especially useful in measuring data within a specific burst inside a frame of TDMA (Time-Division-Multiple-Access) formatted data. By adding a pulse generator having variable width and delay capabilities and using the COMMON A input feature of the mainframe, any 10 nanosecond or wider portion of the burst can be isolated for bit pattern characterization. This ability to isolate bits is also useful in troubleshooting digital systems, whenever searching for specific or even random bits may be required.

To achieve greater resolution on repetitive signals, automatic averaging of the number of channel C events over several time intervals can be accomplished by selecting the AVERAGE EVENTS C, A to B function. Since the events measurement is basically

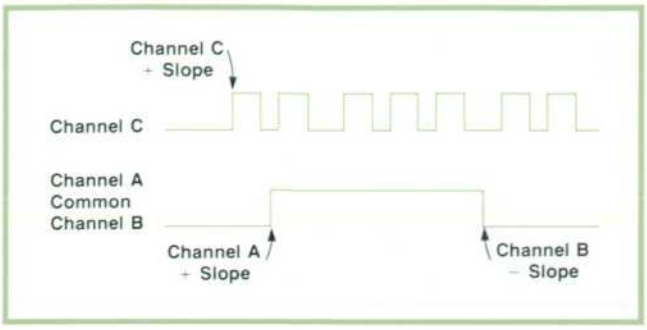


Fig. 2. *EVENTS C, A to B mode is especially useful in digital communications. In this example the counter display would read "4."*

a normalized time-interval measurement, events averaging is analogous to time-interval averaging, excluding the time base jittering as described in David Chu's article in this issue.

All seven 5353A functions are programmable via the optional HP interface bus system. The lamps on the front-panel indicate when the plug-in is listening for bus programming instructions (LISTENING lamp) and when the plug-in is under remote control (REMOTE lamp). The front-panel LOCAL reset pushbutton switch returns the function selection from bus control to the front-panel FUNCTION switch. Bus programming can disable the LOCAL reset switch when desired.

Plug-In Interface

The block diagram of the 5353A Channel C Plug-In is shown in Fig. 3. Also included in the same figure is a simplified block diagram of the 5345A Counter showing the interface between the mainframe instrument and all plug-ins, not only the 5353A.

The channel C plug-in uses two of the four RF lines available to plug-ins. Three of these four lines, the PI Channel A, PI Channel B, and PI Channel C lines, represent full-bandwidth, dc-coupled, E^2L channels paralleling the two mainframe input channels, A and B, and the internal 500-MHz clock, respectively. The fourth RF line is a buffered 10-MHz frequency standard output from the mainframe.

The three PI channels, coupled with the corresponding three channels in the mainframe, afford enormous measurement flexibility to the mainframe/plug-in combination. Through the control interface shown in Fig. 3, the mainframe recognizes which mainframe and/or plug-in RF channels to enable for a given measurement. The plug-in has access to the full measurement capabilities of the mainframe; every mainframe measurement can be controlled by the plug-in through the control interface.

Upon completion of any measurement, the arithmetic processor in the mainframe algebraically combines the contents stored in the BCD counters to create a meaningful result. Through the processor interface shown in Fig. 3, the plug-in can command the processor to scale the result before displaying it.

The general form of equation that the processor is capable of executing is

$$\pm (K \pm XN) \qquad (1)$$

where X is the measurement result and K and N are values supplied by the plug-in when scaling is desired. Arithmetic expressions of the general form

$$\pm (K \pm PI/N) \qquad (2)$$

in which numerical values for K, N and PI are supplied by the plug-in, can also be evaluated by the processor. The algorithm that adds K and the algorithm that multiplies by N will be bypassed if values for K or N are not supplied.

Solutions to more complex arithmetic equations can be calculated by multiple executions of equations 1 and 2 before displaying the final result. Each result calculated by equation 1 or 2 is returned to the plug-in and can subsequently be returned to the mainframe as a plug-in variable in later processing cycles. As a consequence, extremely complex arithmetic processing of measurement results is available to the plug-in.

Plug-In Operation

The digital control logic of the channel C plug-in relays to the mainframe the function selected by the function switch or the optional HP interface bus. In the case of the FREQ C–A function, for instance, the mainframe is commanded to perform a frequency measurement of PI Channel A, which is the plug-in channel C input signal directed to PI Channel A by the high-speed digital logic, after digitization by the input amplifier and trigger circuit. The measurement is a standard frequency measurement using the mainframe 500-MHz clock, and the measurement result is returned directly to the FREQ C±A digital logic for storage in the plug-in without additional processing. As soon as this transmission is completed a second machine cycle is initiated by the digital control logic, commanding the mainframe to perform a frequency measurement of the channel A analog input signal. During the processing of this second frequency measurement, the frequency of the channel

Correction

In our last issue (May 1974) the result for I_D in Fig. 4 on page 10 should be 6.278 mA. Also, the second "user action" in the second column on page 13 should be "CHS following EEX," the third "user action" should be "Multiple CHS," and the third "desired result" should be "Complement mantissa sign, or exponent sign if EEX has been pressed."

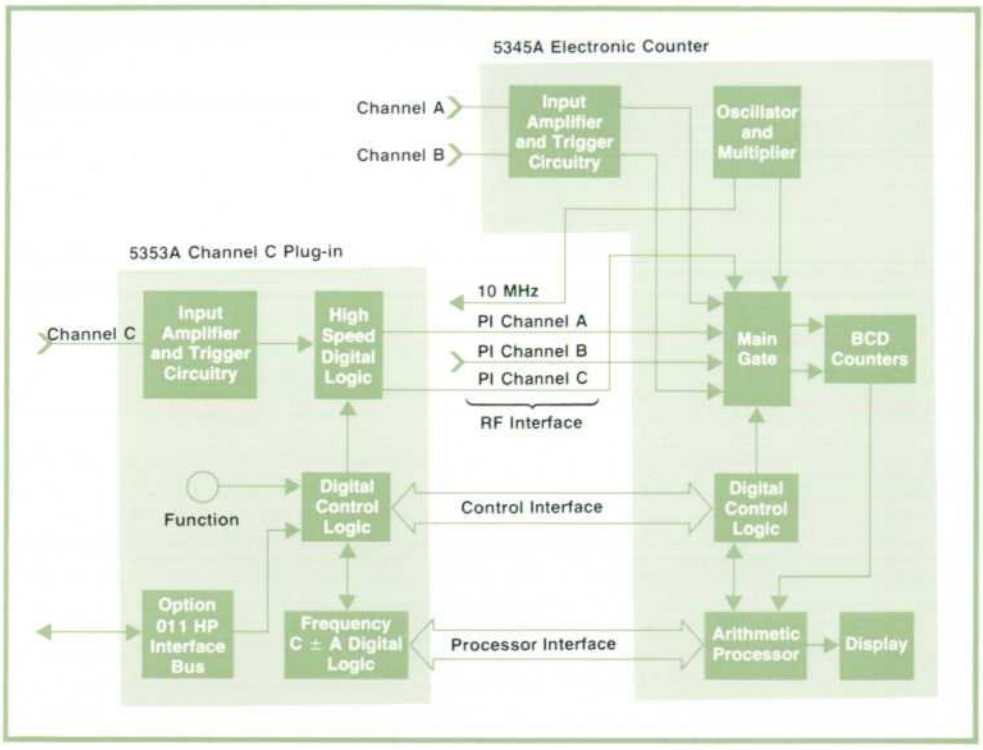


Fig. 3. *Block diagram of the 5353A plug-in and the 5345A plug-in interface. The plug-in controls mainframe measurements and processing of measured data.*

C input signal is returned to the mainframe as K in equation 1. The result is then displayed as the positive or negative difference in frequency between the channel A and channel C input signals.

The other 5353A functions follow similar steps but require only a single machine cycle to generate a display.

Acknowledgments

My associates in the design of the 5353A Channel C Plug-In were Bryce Jeppsen (T^2L digital logic and HP interface bus option), Keith Leslie (mechanical design), and Steve Upshinsky (high-frequency amplifier and trigger). The early design efforts of Ron Felsenstein and Hans Trosch are gratefully acknowledged.

SPECIFICATIONS
HP Model 5353A Channel C Plug-In

MODES OF OPERATION: Frequency C, Period C, Ratio C/A, Events C between A and B, Average Events C between A and B, C−A, C+A.
RANGE:
DC COUPLED: 0 to 500 MHz
AC COUPLED: 10 MHz to 500 MHz
IMPEDANCE: 50Ω (nominal), or 1 MΩ shunted by less than 30 pF.
SENSITIVITY: Variable to 10 mV rms sine wave and 30 mV peak-to-peak pulse. Attenuator settings are X1 and X20.
DYNAMIC RANGE: 30 dB
TRIGGER LEVEL: Continuously adjustable over dynamic range.
PRESET: Centers trigger level about dc at 25°C.
DRIFT: ±10 mV dc max, 0°C to 55°C.
OUTPUT: Rear panel BNC connectors bring out TRIGGER LEVEL for convenient DVM monitoring. Accuracy is ±15 mV.
MAXIMUM INPUT: Same as Channel A and B, separate input.
OPTION 011: Digital Input. Full compatibility with HP Interface (ASCII) Bus. Provides for digital control over all functions excluding amplifier.
PRICE IN U.S.A.: $850.
MANUFACTURING DIVISION: SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050 U.S.A.

Arthur S. Muto

Art Muto designed the high-speed gating circuits for the 5345A Counter and was project leader for the 5353A Channel C Plug-In. A graduate of the University of California at Berkeley, he received his BSEE degree in 1967 and his MSEE in 1969. He joined HP part-time in 1969 and full-time in 1970. Art is a native Californian, born in Sacramento and raised in San Francisco. He and his wife and daughter now live in Saratoga, California. His favorite leisure time pursuits are listening to classical and rock music, playing table tennis, and camping and hiking with his family.

A Completely Automatic 4-GHz Heterodyne Frequency Converter

by Ali Bologlu

A FREQUENCY CONVERTER translates an unknown high-frequency signal downward in frequency by mixing it with a precisely known signal of slightly lower frequency. This heterodyne process yields a difference frequency within the basic range of the counter. Then the counter reading and the known frequency of the mixing signal are added to give the unknown.

A new plug-in for the HP 5345A Electronic Counter completely automates the heterodyne frequency converter technique for both CW and pulsed RF input signals. The 5354A Automatic Converter (see Fig. 1) extends the basic frequency measurement range of the counter to 4 GHz.

A simplified block diagram is shown in Fig. 2. The converter sends signals in the 5-to-525-MHz range directly to the mainframe. Input signals between 510 MHz and 4 GHz are translated by nine crystal-controlled frequencies to an intermediate frequency between 10 and 525 MHz, and are then sent to the mainframe for measurement. The frequency measured by the mainframe (IF) is then added to the crystal-controlled frequency used in the translation process (LO), and the result is displayed. The table below lists the LO and intermediate frequencies for various input frequencies.

Input Frequency (MHz)	LO Frequency (MHz)	IF to Counter (MHz)
15-525	—	Direct
510-775	500	10-275
760-1025	750	10-275
1010-1525	1000	10-525
1510-2025	1500	10-525
2010-2525	2000	10-525
2510-3025	2500	10-525
3010-3525	3000	10-525
3510-4025	3500	10-525

Operating Modes

The converter has both automatic and manual modes of operation, selectable by a front-panel switch. In the automatic mode, the converter automatically steps through nine frequency bands repetitively until a signal within the converter range is detected. The time required for acquisition is 160 microseconds worst case. In the manual mode, the converter remains in one of the frequency range bands until the BAND SELECT or RESET switch is pressed. Each time the BAND SELECT switch is pressed, the next higher frequency band is selected. Pushing RESET returns the converter to the zero band.

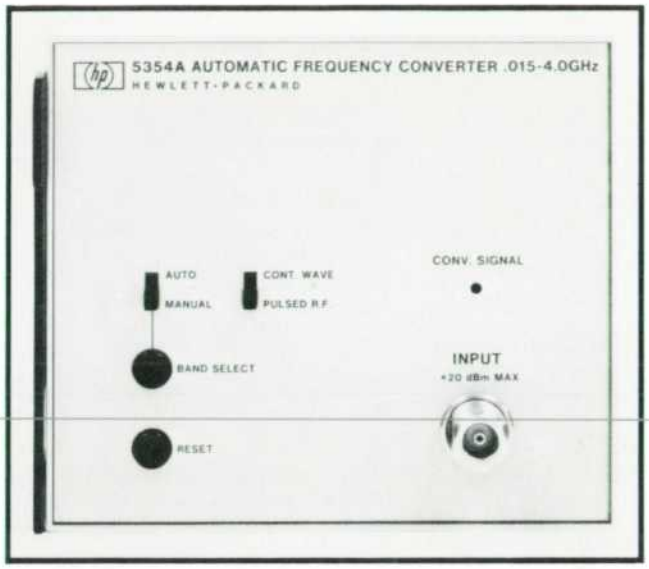


Fig. 1. *Model 5354A Automatic Converter extends the frequency measurement range of the 5354A Electronic Counter to 4 GHz. Operation can be manual or completely automatic, even for pulsed RF signals.*

In the manual mode, if there is no signal or the signal level is inadequate, the mainframe will display the LO frequency. In both modes, manual and automatic, the CONV signal light comes on when the counter is making a correct measurement. One can operate the converter in the automatic mode until a signal is acquired and then switch to manual. In this case, the manual mode retains the band information and will be ready to make a measurement in that particular band within 20 microseconds.

In the automatic mode the converter assumes that the first signal of sufficient amplitude to be detected is the correct one. When many frequencies in differ-

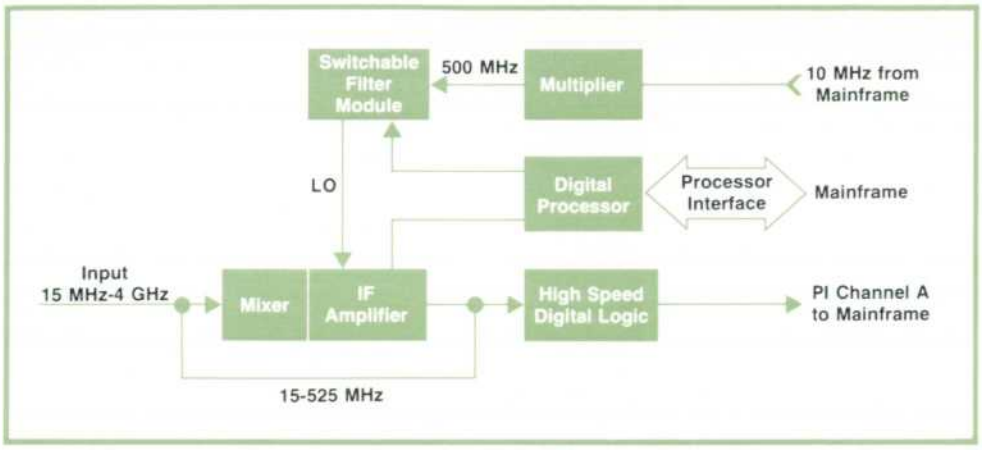


Fig. 2. *The 5354A automatic converter heterodynes high-frequency input signals with one of nine crystal-controlled frequencies to derive an intermediate frequency within the range of the 5345A.*

ent bands are present simultaneously the user may switch to the appropriate bands manually to count the higher frequencies.

The rapid acquisition in the automatic mode and the flexible switching capability in the manual mode are possible because of the switching filter assembly shown in Fig. 3.

CW Performance

The 5354A Automatic Converter is very tolerant of signals that have various kinds of modulation. It can tolerate large frequency deviations—up to ±250 MHz—at band centers. At band edges it is limited to deviations of about ±10 MHz. These tolerances are sufficient for communications applications, in which carrier frequencies need to be measured under operating conditions.

Specified sensitivity in the CW mode is −10 dBm.

Pulsed RF Performance

The most unusual feature of the converter is its ability to measure pulsed frequencies automatically. Pulsed signals whose modulation width is greater than 250 nanoseconds can be acquired automatically in one second.

For narrower pulse widths the manual mode may be used—the minimum RF pulse width is 50 ns. Converter sensitivity is greater in the manual mode; signals of −20 dBm (typical) may be counted. Furthermore, the mainframe gate and plug-in signal detectors are pre-armed in the manual mode, so actual measurement times may be as short as 2 ns. The 5354A's pulsed RF capability together with the mainframe's averaging capability allows meaningful high-resolution frequency measurements on narrow pulses. Displaying the auxiliary output of the plug-in on an oscilloscope simultaneously with an external gating signal shows exactly which portion of the RF pulse is being measured. By sliding the gate pulse along the down-converted RF signal, frequency profile measurements may be made.

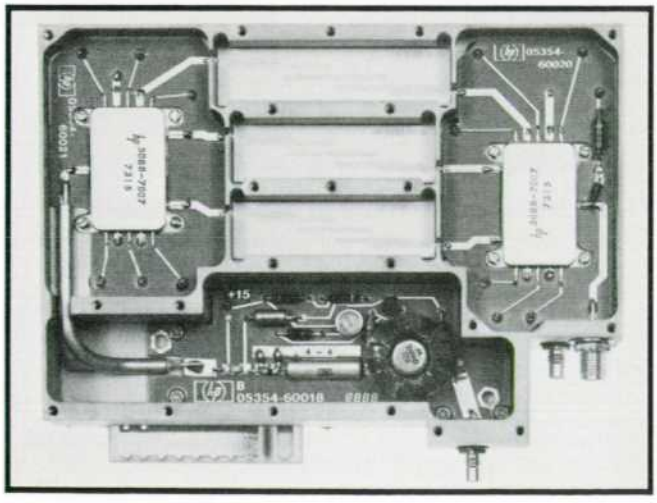


Fig. 3. *Switching filter assembly permits rapid acquisition of input signals. 160 μs is worst case in automatic mode.*

Special Features

Besides the RF circuits necessary to process microwave signals, the converter also contains digital processing circuits. These have two main functions. One is control of the interface to the mainframe and the other is the algorithms for automatic operation of the converter. For rapid troubleshooting, a self-test feature has been incorporated. This is enabled by putting an internal switch in the test position with the mainframe in self-check mode. With the plug-in in manual mode, the mainframe will display the LO frequency plus 100 MHz. When the 3.5 GHz LO is selected, the CONV signal light comes on. This routine checks the plug-in/mainframe interface. When the plug-in is placed in the automatic mode, the mainframe will immediately display 3.6 GHz with the CONV light on, thereby checking the automatic acquisition routine.

Options and Rear-Panel Controls

A buffered version of the down-converted IF signal is available at the rear-panel AUX OUT connector for such applications as viewing the down-converted

microwave signal on an oscilloscope. Another rear-panel control, the NORM/-L.S. slide switch, controls the mainframe processing of the converter output signals. In the normal position, the mainframe is instructed to add the frequency of the converter local-oscillator signal to the frequency of the converter IF signal and display the result. In the manual mode the -L.S. position may be used, causing the IF to be subtracted from the LO signal frequency. One application for this control is the measurement of pulsed signals having narrow pulse widths, when the resulting converter IF signal is a low frequency. By switching to the lower sideband (-L.S.), one can increase the number of zero crossings per unit time, and therefore the accuracy of the measurement.

When the mainframe is under remote control of the HP interface bus, option 011 for the converter gives the plug-in its own address and allows all of its functions to be remotely programmed.

An optional LO±IF ON-OFF switch controls the addition or subtraction capability of the converter. With this option, input signals of microwave receivers can be monitored. The receiver IF signal is applied to the mainframe channel A input and the receiver local oscillator to the converter input. The LO±IF ON/OFF switch is set to ON. The +IF/-IF switch is set to +IF if the receiver local-oscillator frequency is known to be below the received signal frequency, or to -IF if the local-oscillator frequency is above the received frequency.

LO Details

Crystal-controlled mixing frequencies are generated from a 500-MHz signal derived from the 10-MHz time base. The 500-MHz signal drives a spectrum-generator diode whose output goes to a PIN single-pole six-throw switch. Each output of this switch is connected to a band-pass filter whose center frequency is tuned to a harmonic of 500 MHz which, in turn, is connected to a single-pole six-throw switch. The output of this switch is connected to the input mixer module. The PIN switches, filters, and spectrum-generator modules are hybrids, all contained in one assembly (Fig. 3). It is this unique structure that makes the extremely fast acquisition of input signals possible.

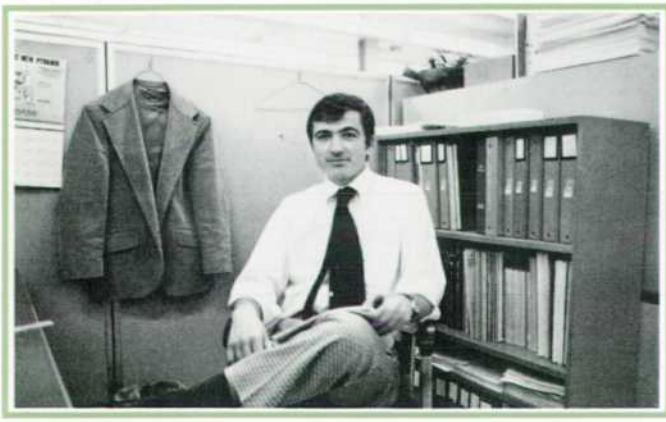
Acknowledgments

Special credit is due Hans Trosch and Al Barber for their design efforts. Larry Jackson initiated the product design, which was completed by Roland Krevitt. Thanks are also due Dick Harris for production support and Holly Cole for market introduction.

SPECIFICATIONS

HP Model 5354A Automatic Frequency Converter

RANGE: 15 MHz to 4 GHz
SENSITIVITY: -10 dBm (70 mV rms) to +20 dBm (2.2V rms)
INPUT SIGNAL CAPABILITY: CW signals. Pulsed microwave signals. Signals with very high FM content.
RF PULSE WIDTH: Determined by counter GATE TIME setting.
FM SENSITIVITY: Maximum deviation at band edges ±10 MHz. Maximum deviation at band center: ±250 MHz above 1 GHz and below 500 MHz, ±125 MHz between 500 MHz and 1 GHz.
OPERATING MODES: Automatic and manual.
AUTOMATIC: Measures lowest frequency signal of sufficient amplitude to trigger counter.
MANUAL: Measures signal within selected band. Signals of sufficient amplitude between 15 MHz and 525 MHz will also be counted.
ACQUISITION TIME:
AUTOMATIC MODE: cont. wave <160 μ sec, pulsed RF <1 sec.
MANUAL MODE: When proper band has been selected: cont. wave <5 μsec, pulsed RF <20 nsec.
MIXING FREQUENCIES: 0, 0.5, 0.75, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5 GHz
DAMAGE LEVEL: 25 dBm (4V rms), 10 volts peak-to-peak.
OPTION 011: Digital Interface Bus for remote control and L.O.±I.F.
PRICE IN U.S.A.: $1950.
MANUFACTURING DIVISION: SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050 U.S.A.



Ali Bologlu

Ali Bologlu received the BSEE degree in 1962 and the MSEE degree in 1963, both from Michigan State University, and the degree of Electrical Engineer in 1965 from Stanford University. At HP since 1963, Ali has contributed to the design of the 5100A, 5102A, 5103A, 5105A, and 8660A/B Frequency Synthesizers, and was project leader for the 5354A Converter. He now has responsibility for microwave counter development. He's a member of IEEE. Born in Istanbul, Turkey, Ali now lives in Mountain View, California, where he devotes much of his free time to the local youth athletics program.

Interface Bus Expands Instrument Utility

by Bryce E. Jeppsen and Steven E. Schultz

THE PROLIFERATION OF computer-controlled instrument systems over the last decade testifies to the importance of marrying data-input and computational capabilities. However, most systems of this type have gone into production environments as a means of reducing test times and simplifying production decision-making. The cost, complexity of system integration, and elaborateness of operating procedures has restricted the use of such systems in the development laboratory. Nevertheless, the engineer would often prefer to work with computed quantities such as pulse jitter or linearity, rather than raw time-interval or frequency data.

A pair of recent developments now offer the engineer the tools he needs to look at computed quantities based on fundamental measurements. One is the programmable calculator, which brings computing power to the laboratory bench. The other is the new HP interface bus system, which greatly simplifies the assembly of instrument/calculator systems.[1] As the applications and ramifications of this "smart" interface technique become recognized, we can expect to see a profound change in the way bench instruments are used.

The new 5345A Counter is compatible with the bus interface. Systems including the 5345A, the 9820A Calculator, and a new line of ASCII-Programmable Modules are described, complete with software, in a new series of Application Notes, AN 174. Because of space limitations, only two of these systems are discussed here.

Pulse-Width Jitter Histograms

A typical counter/calculator system application is the measurement and analysis of pulse-width jitter, such as that of any pulsed or clock signal. A histogram or probability distribution provides insight into the statistical nature of the jitter. This insight is useful in analyzing the noise characteristics of the signal source. However, the effort and time required to collect and plot this data manually is almost prohibitive, so the measurement is rarely performed more than once, and that one measurement is assumed to be typical. Effects of temperature, power-supply variations, and the like may never be investigated.

Using the 5345A Electronic Counter with the new HP interface bus, this measurement may be made easily with the help of a calculator such as the HP 9820A. The equipment is connected as shown in Fig. 1.

To program the counter, it is only necessary to enter the number of measurements desired, the width of each bin, and the number of bins. Application Note 174-5 tells how this is done. Once these parameters are defined, measurements may begin.

As data is received, the calculator determines which bin each measurement falls in. When the specified number of measurements has been made, the calculator instructs the plotter to draw the histogram.

This system has been used to evaluate the overall quality of digital communications systems by measuring the time jitter between frames, and has proved valuable in PCM communications applications that require an analysis of the statistical nature of the time between error pulses from an error-bit-rate detector.

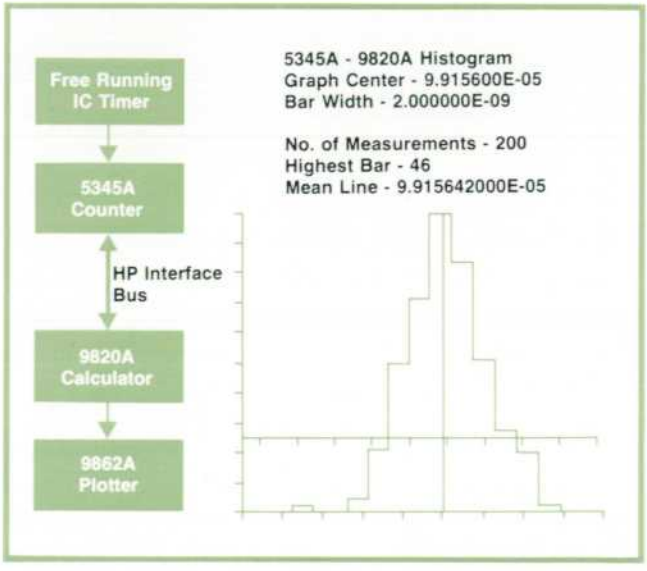


Fig. 1. *5345A Counter is compatible with the HP ASCII-coded interface bus, making it easy to assemble systems like this one, which plots a histogram showing the distribution of the pulse-width jitter of an integrated-circuit timer chip.*

ASCII Programmable Modules

The ASCII Programmable Modules make the 5345A Counter more versatile as a systems component. These modules can be used as "systems glue", performing necessary systems functions not performed by the major instruments. However, they are also designed to make the basic measurement instruments like the 5345A Counter more useful in bench-top environments. The modules may be used with or without a calculator in the system. Modules now available are:

59301A	ASCII-to-Parallel Converter
59303A	Digital-to-Analog Converter
59304A	Numeric Display
59306A	Relay Actuator
59307A	VHF Switch
59308A	Timing Generator
59309A	ASCII Digital Clock

Model 59301A ASCII-to-Parallel Converter interfaces the counter to standard digital printers to produce hard-copy records of measured data. Model 59303A Digital-to-Analog Converter can drive a standard strip-chart recorder to provide trend information. Model 59308A Timing Generator is useful in the monitoring of crystal warmup characteristics and similar applications.

Model 59304A Numeric Display can be used to display intermediate results without consuming valuable calculator processing time. The 59306A Relay Actuator can control high-frequency switches and attenuators, or simply switch bias voltages. Model 59307A VHF Switch is useful for switching high-frequency signals.

VCO Characteristics

An example of the usefulness of the 5345A/9820A combination in stimulus-response testing is a system to measure the characteristics of voltage-to-frequency conversion circuits. Voltage-controlled oscillators (VCO's) are present throughout electronic designs in phase-locked loops, modulators, and so on. It is often desirable to characterize the tracking characteristics of two similar oscillators. This can be done using the 5345A Counter, the 9820A Calculator, and three members of the ASCII-Programmable Module family: the 59303A Digital-to-Analog Converter, the 59304A Numeric Display, and the 59307A VHF Switch. The system is described in Application Note 174-4 and shown in Fig. 2.

The D-to-A converter is told by the calculator to apply voltages to the VCO's while the VHF switch alternately applies their frequency outputs to the 5345A Counter. The numeric displays give a real-time presentation of the applied voltage, the frequency outputs, and the frequency difference. The calculator generates a linearity plot for each VCO and a plot showing how well the two VCO's track.

The key to success in this experiment is the accuracy of the voltage applied to the VCO's from the digital-to-analog converter. This D-to-A converter has 10 mV resolution and accuracy, a dynamic range of +10 volts to −10 volts, and an operating temperature range of 0 to 55°. At room temperature the 59303A is typically accurate within 3mV. This D-to-A converter is also fully programmable. Various digit formats and output modes can be chosen, including a mode that adds in an offset for strip-chart recordings.

Acknowledgments

The authors would like to acknowledge the support given by John Dukes and Jim Sorden. The pillar of strength in the 5345A Interface and ASCII Programmable Module program has been Charlie Trimble, whose counsel and guidance has greatly contributed to the program's success. Technical support from Dave Ricci and product design by Eric Havstad and Carl Spalding is also appreciated.

References

1. G.E. Nelson and D.W. Ricci, "A Practical Inter-

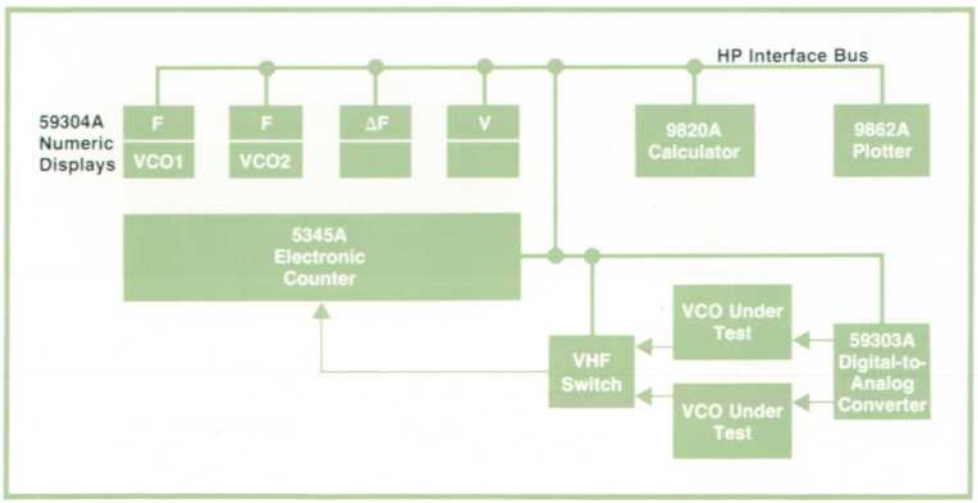


Fig. 2. *The ASCII-programmable Modules complement the 5345A in systems applications. Three types are used in this system, which characterizes the tracking characteristics of two similar voltage-tuned oscillators.*

face System for Electronic Instruments", Hewlett-Packard Journal, October 1972.
2. D.C. Loughry, "A Common Digital Interface for Programmable Instruments: The Evolution of a System", Hewlett-Packard Journal, October 1972.

Steven E. Schultz (right)
A 1970 BSEE graduate of the University of California at Berkeley, Steve Schultz is now working towards his master's degree at Stanford University. At HP since 1971, he helped design the digital I/O and mainframe boards for the 5345A Counter, and was project leader for five of the ASCII-Programmable Modules. Steve was born in Oakland, California. He's married, lives in Menlo Park, California, and says that most of his spare time is occupied by his master's studies and other obligations. Whenever he can, though, he indulges his many other interests which include radio controlled boats, British cars, sailing, electronics, and riding dirt motorcycles.

Bryce E. Jeppsen (left)
Bryce Jeppsen graduated from Brigham Young University in 1970 with BES and ME degrees, then joined HP and began working on the 5340A Microwave Counter only to be drafted into the U.S. Army in October of that year. While in the service he organized and taught courses in basic semiconductor electronics. In 1972, his service completed, Bryce returned to HP and electronic counters. He designed the 10590A Plug-In Adaptor and the digital circuitry and ASCII control for the 5353A Plug-In, and has written much of the series of application notes describing 5345A systems based on the HP interface bus. Bryce and his wife have three small children and live in Santa Clara, California, where they're busy working on their new home and participating in church activities.

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HEWLETT-PACKARD JOURNAL
JUNE 1974 Volume 25 • Number 10

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