DECEMBER 1983

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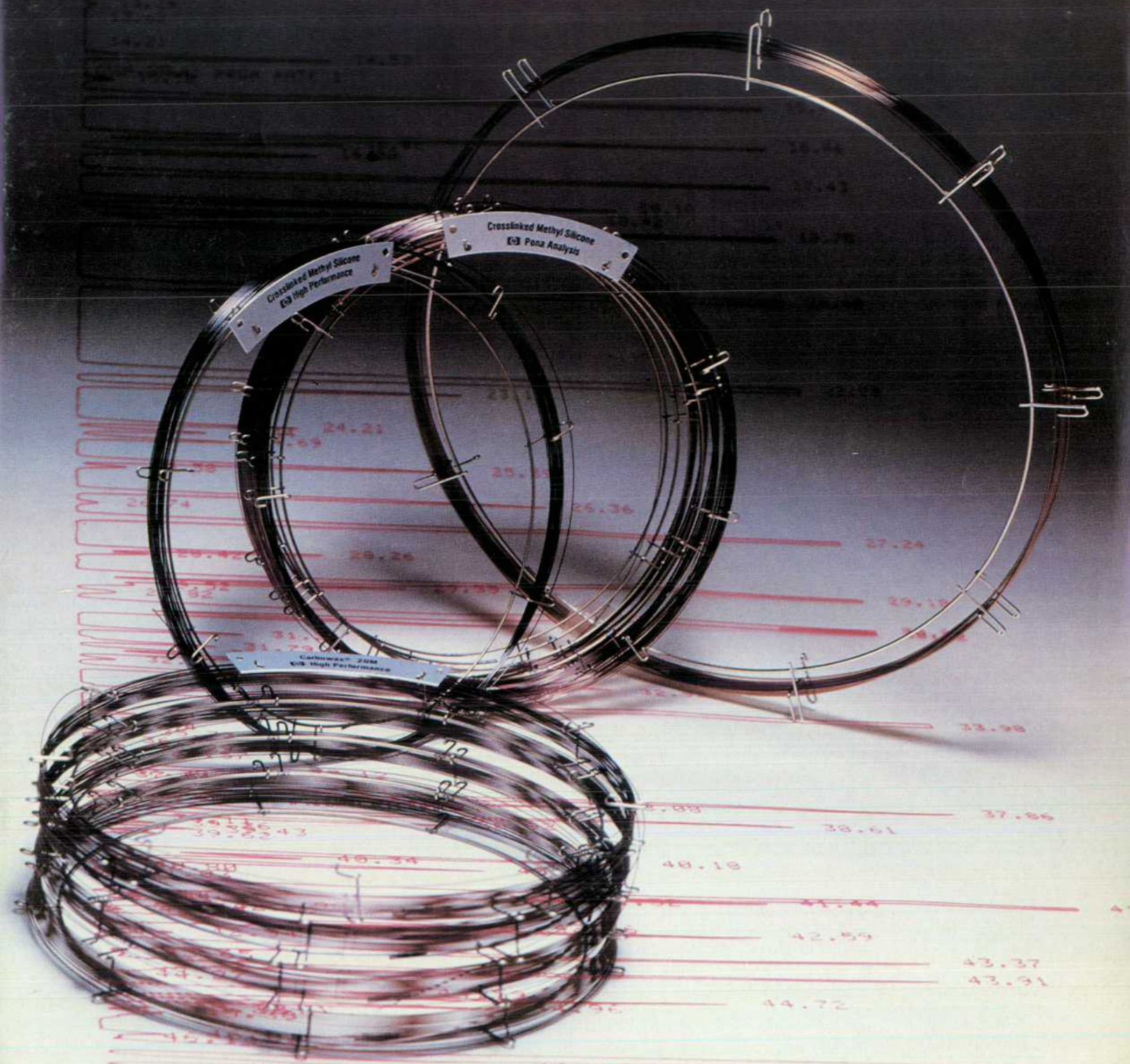

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In this Issue:

Sometimes a significant development doesn't get the attention it deserves. In 1979, when HP introduced the fused silica capillary column, there wasn't much fanfare outside of the gas chromatography community, even though here was a technological breakthrough if ever there was one. Nobody had tried before to make GC columns the way optical fibers are made, and the results were spectacular. The new columns had much greater separating power and results were much more reproducible, not just from run to run, but to an unprecedented degree, from column to column. On the occasion of their introduction of a new line of fused silica columns, the Series 530μ columns, we asked the engineers at HP's Avondale, Pennsylvania Division to start at the beginning and bring us up to date on this technology. Their story begins on page 35. On our cover this month you can see some fused silica columns—long, thin tubes, some as long as 50 meters, wound into coils of different sizes. The largest-diameter coil is one of the new Series 530μ columns. In the background is a chromatogram, a record of what a detector at the end of a fused silica capillary column saw after a vaporized sample of some compound—a rather complex one—was put in at the other end. Each type of molecule present in the sample comes out at a different time and causes a peak in the detector output. The gas chromatograph was an HP 5880A, similar to the instruments used recently to detect drug use by athletes, an application given wide attention in the news media.

Also in this issue you'll find articles completing the design story of the HP 77020A Ultrasound Imaging System we began in October. Here are the inside details of the sophisticated, creative design that makes this very complex instrument friendly and easy to use in clinical diagnosis. Three different hardware subsystems, each with its own microcomputer, are coordinated by the system software (page 6). The controller (page 3) has overall command of the instrument. The scanner (page 13) steers the beam of ultrasound and focuses the system dynamically so that features at different depths are always in focus. The display system (page 20) formats data from several sources for display and recording. A common theme in these articles is that of ingenuity over complexity—functions that might have been prohibitively expensive or complicated to implement are made practical by clever design.

December is our annual index issue. The 1983 index begins on page 30.

-R. P. Dolan

Control Hardware for an Ultrasound Imaging System

Coordinating the various subsystems, peripherals, and operator commands for HP's diagnostic imaging system requires sophisticated controller hardware.

by Richard H. Jundanian, Janet R. Accettura, and John N. Dukes

THE HP 77900A ULTRASOUND CONTROLLER provides the interface between the user and the HP 77020A Ultrasound Imaging System (Fig. 1).[1] It houses the primary video display, the front control panels, the system CPU, and the I/O system. The CPU (central processing unit) interfaces the 77020A to the operator by scanning the front-panel controls. Three printed circuit assemblies provide the interface hardware required to support the video cassette recorder (VCR), various physiological amplifiers, the stripchart recorder, and the video camera. The block diagram in Fig. 2 shows the assemblies that are included in the 77900A Controller.

CPU Card

The CPU card in the controller contains the microprocessor, a PHI chip, EPROM (electrically programmable read-only memory), and other control logic. Also located on the board are a four-digit, seven-segment LED display and a software reset switch for debugging software.

The microprocessor is a proprietary CMOS-SOS (silicon-on-sapphire) 16-bit-parallel microcontroller with TTL-compatible inputs and outputs. It operates as a synchronous device running on a single-phase clock and has bidirectional data and address buffers. The PHI chip controls the internal system bus based on the HP-IB (IEEE 488) and interfaces the rest of the system to the CPU card. A connector can be attached to this card to monitor the software when testing the system. Also located on this card are 4K words of software containing most of the kernel tests that run at system start-up.

Memory/Clock Card

The memory/clock card contains the CPU's memory stack, which is the majority of the controller's RAM and EPROM. This card incorporates a special memory bank-switching scheme (see page 8), volatile and nonvolatile RAM, a real-time clock, and timing logic.

The 16-bit microprocessor supports a 64K address space. The system designates 40K of this space for EPROM and 24K for testing and I/O. Since 40K is not sufficient for programming, bank switching is used, allowing a total of 80K words of program memory divided into seven banks and one common area. Bank switching is accomplished by loading an I/O register with the bank number desired, and addressing an ID PROM that contains the programmed logic needed to enable the appropriate EPROMs.

The controller's RAM is also located on the memory/clock card. 4K words of volatile RAM are used for the stack and scratchpad memory and 2K words of CMOS battery-backed RAM are used to store important system and user-entered information. Among the items stored in the nonvolatile memory is the data for the various analysis packages, system configuration, and patient ID.

The real-time clock on the memory/clock card generates the time and date needed for document annotation. It is also battery-backed to allow operation when the system is shut down.

VCR/Physio Card

The VCR/physio card in the controller is primarily used to monitor and control the VCR signals. Special level-shift-

Fig. 1. *HP Model 77020A Ultrasound Imaging System provides both M-mode and two-dimensional sector scans of human tissue for cardiac, obstetric, and abdominal examinations.*

ing buffers interface the card to the different VCRs that can be used with the 77020A System. Status and control registers monitor and control the present state of the chosen VCR. The counting circuit on the VCR/physio card monitors the frame count and an EPROM on the card controls the VCR frame-count logic, since different VCRs can have different count sequences.

Also located on the VCR/physio card is circuitry that accepts physiological data, digitizes it, and stores it in the 1K × 12-bit physio RAM. The digitizing circuitry consists of a discrete precision analog-to-digital converter (ADC) and its corresponding controls and a comparator located on the controller's analog card. The physio RAM is accessed by the system software to display the digitized physiological waveform.

TM/Frame Card

The TM/frame card provides line buffering of M-mode and frame data for output to the stripchart recorder. This requires two dual-port 1K × 5-bit memories. The card also contains a 1K × 8-bit memory for storing annotation information to be included on the stripchart copy.

The TM/frame card synchronizes a sample clock to the M-mode line for analog-to-digital conversion in the analog card. The digital data is then formatted and stored in memory. The TM/frame card also sends digital control information to the analog card to configure it for output to the stripchart recorder.

Analog Card

The analog card is responsible for the analog-to-digital and digital-to-analog data conversions, physiological sampling and mixing, and the generation of the necessary waveforms to drive the stripchart recorder, including the horizontal sweep, the input speed, and the video signal. The digital data is sent to the analog card from the TM/frame card. There are control lines to configure the analog card for output to the stripchart recorder. These include a horizontal sweep rate consistent with the recording mode as well as control for the proper speed output.

Stripchart Recorder Interface

The primary use of the stripchart recorder is to provide hard-copy recording for continuous real-time M-mode. The latent image is developed by passing current through the carbon backing of the recorder's dry silver paper. The stripchart recorder is internally gamma-corrected to compensate for the nonlinearities in the image density of its paper.

The recorder interface is responsible for providing each line of image data to the recorder. Control information is sent to the interface from the controller via the 16-bit microprocessor's address and data buses. The 35-bit parallel control data is latched into four microprocessor I/O ports to control the hardware on the TM/frame and analog cards.

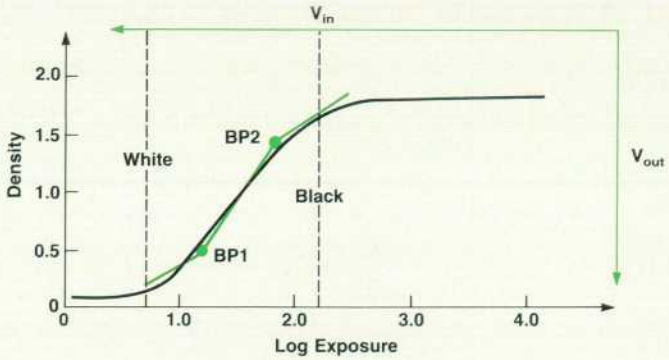

Fig. 3. *Black curve: Sample density versus exposure characteristic for dry silver paper. Color curve: Two-breakpoint approximation of black curve.*

The interface uses two 1K × 5-bit memories for buffering the image data. An image is generated by writing one line into one of the two memories and then configuring that memory to be the output memory. Meanwhile, the other memory is configured to accept the next image line. These dual memories are toggled between input and output to create the image. The display memory is accessed at an output rate that provides a 4-kHz sweep to the stripchart recorder. Continuity is ensured by not allowing a memory switch to occur before the end of a sweep. Since the input of data comes at a much slower rate than the sweep time, the same image line is repeated for several sweeps. The resulting gray-scale image is a smooth filled-in picture with no blank lines between data lines.

The M-mode data from the scanner is sent to the analog card where it goes through an ADC, is processed digitally, and then is sent to a digital-to-analog converter (DAC) for final output to the stripchart recorder. Some of the data is returned to the TM/frame card for use in selecting the recorder parameters.

The recorder interface can operate in one of three modes: a frame record mode, an M-mode recording mode, and a gray-scale test pattern. The frame record is generated by transferring a frozen image line-by-line from the 77020A's scan converter memory to the controller via the internal HP-IB.

An M-mode recording is formed by enabling the sampled M-mode data onto the memory data bus. This M-mode data

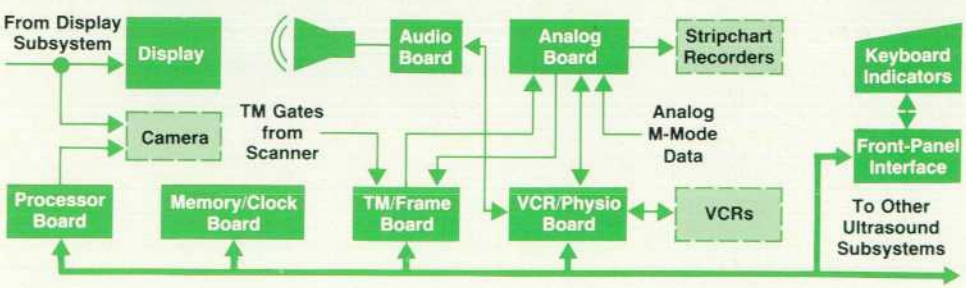

Fig. 2. *Block diagram of the 77900A Controller for the HP 77020A Ultrasound Imaging System.*

is sent to the recorder from the scanner as a video signal along with M-mode gates to synchronize the data conversion. Sampling is at a depth-dependent rate, and each sample is five bits of gray scale.

The gray-scale test bar pattern sent from the 16-bit microprocessor is used to set up the recorder's black-and-white front-panel controls.

The recorder interface can also display time and depth calibration marks on the stripchart recorder. For this purpose, there is a 1K × 8-bit memory on the TM/frame card written by the microprocessor. Each 1K × 1 column is used for a particular type of mark. One word from the memory represents one pixel on the paper. As the memory is read, any bit ANDed with its corresponding control gate can write a black mark on the paper. These marks are mixed with the video signal before going to the DAC on the analog card.

There is also a self-test mode activated by setting the control bits appropriately. The controller then has control of the interface clocks and can single-step the interface through any of its operations.

Audio Card

Beneath the 77900A's control panels is the multipurpose audio card, the driver for the 77020A System's speaker or audiophones. There are three different audio signals. One is an error tone, or beep, output whenever there is an operator error. The ECG R-wave tone, derived from the electrocardiographic R-wave, informs the operator of the electrical activity of the heart, which is useful for physiological timing. Finally, the VCR's audio track is routed through this card so that comments recorded by the operator with a microphone plugged into the front panel of the audio card can be heard during playback. There is a control for adjusting the volume of the R-wave tone and VCR audio track. Alongside the volume control are the system reset button and the black-and-white controls for the display's brightness and contrast.

Control Panels

The vertical control panel containing the imaging controls is connected to the system through the horizontal control panel, which contains the joystick, keyboard and control panel electronics. This panel is scanned by the microprocessor on the CPU card and contains the alphanumeric keyboard and the ECG and VCR controls.

60-Hz Display

The 77020A's primary display uses a noninterlaced raster scan to eliminate display flicker. The 77020A's scan converter provides the main display with 60 frames every second. The frame rate can be changed to 50 Hz by using internal jumpers. The display circuitry provides high-voltage regulation to prevent distortion of the image at high brightness settings.

Another important feature of the main display is gamma correction, which provides a linear gray scale to the user from a linear video input. This allows matching the different hard-copy outputs to the main display. Each output modality used in the ultrasound system introduces its own characteristic nonlinearity, which impacts the gray scale observed from that device. As a result each peripheral requires its own gamma correction. In the case of the stripchart recorder, the gamma correction is matched to the dry silver paper characteristic. Similarly, the Polaroid™ camera is gamma-corrected to match the Polaroid film characteristics. In the case of the primary display, the gamma correction is implemented to accommodate the CRT's characteristics and the logarithmic response of the observer's eye. The result is a linear density change on the output medium for a linear input video signal. The gamma correction curves have been implemented in an analog fashion in the primary display as well as in the peripherals. Two-breakpoint approximations (Fig. 3) to the required curves are adequate to provide the required linearity.

Camera

A camera is also available for hard copy of frame data. The 77020A's scan converter provides a composite video signal to a 1000-line monitor with a Polaroid camera mounted on the front. The shutter is controlled remotely from the 77020A's front panel. A fixed number of frames are sent to the camera from the display subsystem. Several types of Polaroid film are available for use with this camera. Gamma correction compensates for the nonlinearities in the film so that the gray scale for the copy appears the same as observed on the display.

Video Cassette Recorder

A VCR can be used to store real-time images and other video data and allow for their future playback and analysis. The VCR's audio track can record the physician's comments, the patient's heartsound, and R-wave timing information. To allow system software control and status monitoring by the 77020A, the remote control data is connected from the VCR to the controller's CPU via the previously described VCR/physio card.

Two different types of VCRs are supported directly by the system. The Sony 323MD has a Beta® video cassette format and the Panasonic NV8200 has a VHS® video format. These recorders can be mounted either inside the system cart, or on top of the controller when the stripchart recorder is mounted in the cart.

Reference

1. L.W. Banks, "An Ultrasound Imaging System," *Hewlett-Packard Journal*, Vol. 34, no. 10, October 1983.

CORRECTION

In the October issue, the formula for $f_{m\text{-}s}$ on page 20 left out a factor of 2π. The correct formula is

$$f_{m\text{-}s} = (v_{eff}/2\pi)\sqrt{1/LH}$$

Ultrasound System Software

Coordinating the operation of the complex subsystems in HP's ultrasound imaging system is a comprehensive software system using an internal bus based on the HP-IB.

Joseph M. Luszcz, William A. Koppes, David C. Hempstead, and Robert J. Kunz

SOFTWARE IS AN INTEGRAL PART of the HP 77020A Ultrasound Imaging System. It implements all control actions and gives the system its "personality." The software sets up the hardware, controls image acquisition, and processes physiological data such as ECG and heartsound waveforms. In addition, computational features such as cardiac and obstetric analysis are implemented in the system software.

The software is responsible for coordinating three subsystems: the 77200A Scanner (page 13), 77400A Display Subsystem(page 20), and 77900A Controller (page 3). Each subsystem contains its own 16-bit proprietary microprocessor.

The scanner software sets up and times the generation and reception of the acoustic lines used to create the ultrasound image. The display subsystem software sets up the high-speed interpolating hardware to accept the acoustic line data from the scanner. It also controls the writing of text and graphics and the video generation circuitry. Further, it supplies image data to the controller when needed to produce hard-copy records. The controller software continually monitors the state of the front-panel controls, along with any other inputs that might require a response by the system (such as the detection of the R wave in the ECG waveform). When an input is detected that demands a response by the system, the required changes are initiated by the controller software. In addition to implementing the operator interface and coordinating the system hardware, the controller software also controls the generation of all hard copy produced by the system.

Coordination of the three subsystems is accomplished by sending commands from the controller to the other subsystems over the 77020A System's internal HP-IB (IEEE 488). The processing of commands received by each subsystem typically results in the activation of one or more software modules within that subsystem. At the lowest level, data flow and processing changes are implemented by writing and reading various hardware registers. In some cases data is returned over the HP-IB in response to the transmitted command.

In addition to hardware control and system coordination, the ultrasound system software also provides a variety of data processing capabilities such as the sampling, compression, smoothing and display of physiological waveforms. Recently, a new software package was integrated into the system to allow a clinician to analyze the images generated on-line, and produce clinical reports. Without the flexibility provided by a software-based system, enhancements such as these would not be possible.

The HP-IB in the Ultrasound System

The three ultrasound subsystems communicate as devices on an internal bus based on the HP-IB structure. A proprietary LSI chip called PHI is used to interface the processor within each subsystem to this bus. The 77900A Controller serves as bus controller, while the 77400A Display Subsystem (DSS) and 77200A Scanner act as talkers and listeners with no control capability. A special protocol is followed by all subsystems using the bus. This protocol serves four purposes:

- It allows a command to be transmitted only when the destination device is ready to receive it.
- It provides several different priority levels for commands to the same device, permitting each subsystem to execute several commands concurrently at different priorities.
- It provides some synchronization between devices.
- It provides error checking and the ability to retransmit commands received in error.

Using the ultrasound system communication protocol, three different kinds of data transfers take place between the controller and the other subsystems. These are:

- Mnemonic commands—multiple-byte commands sent

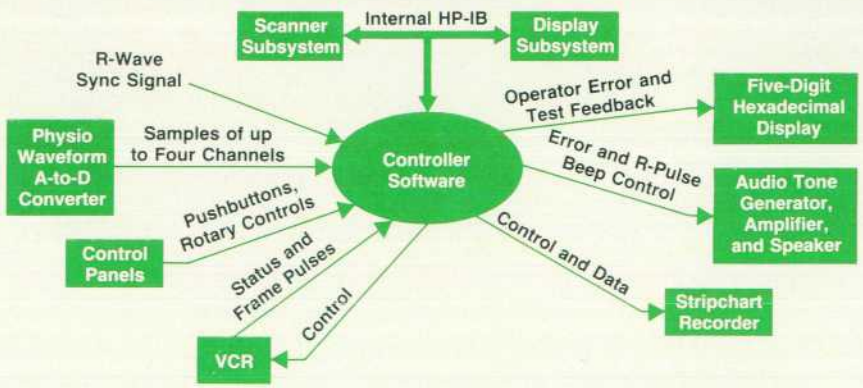

Fig. 1. *Environment for controller software system.*

by the controller subsystem, consisting of a secondary address marking the transfer as a mnemonic command, a byte indicating the command priority level, two ASCII bytes designating the command, optional parameter bytes, and a checksum byte.

- Secondary listen address commands—simple commands consisting of only a secondary listen address sent by the controller to the DSS or scanner.
- Input transfer with secondary talk address—data transfers from the DSS or scanner to the controller.

The protocol makes use of various HP-IB structures to transfer these three kinds of data while providing the desired handshaking and error detection. All transfers are between the controller and one of the noncontrolling devices, never between two noncontrollers. The key feature of the protocol is that a transfer can only take place with a device that has signaled its readiness to process a transfer with an affirmative parallel poll response.

When the system powers up or is reset, the internal HP-IB is prepared for communication by the bus start-up sequence. This sequence begins when the controller sends the interface clear signal IFC followed by remote enable REN. Each device responds with a service request SRQ and the controller confirms receipt of the SRQ by sending a specific secondary listen address to each device. On receipt of the secondary address, each device cancels the SRQ and responds affirmatively to a parallel poll, indicating it is ready to process the first command.

When the controller wishes to send a mnemonic command to a device, it first checks that the parallel poll response is affirmative from the device in question. The device is addressed with the secondary listen address 31 to indicate that a mnemonic command is being transmitted. Then command bytes are sent. When a command byte is received, the device changes its parallel poll response to negative. The last byte of the command is a checksum byte, but it is not transmitted by the controller until the parallel poll response from the addressed device is verified as negative. The device then compares the received checksum byte against the sum of the command bytes it has calculated. If they match, the parallel poll response is set true once again.

If a checksum mismatch is detected on the receipt of any mnemonic command, the device delays the setting of parallel poll true and SRQ is asserted instead. When the controller detects an SRQ, it conducts a serial poll to determine which device is requesting service, then inputs status bytes from that device to determine the reason for the SRQ. In this case, the status indicates a command checksum error has occurred, so the message is tagged to indicate this and is retransmitted when the device is available. After sending the status bytes, the device once more sets parallel poll true, indicating its readiness to receive another command (which may be a retransmission of the previous command).

One special type of mnemonic command is a primary command to the DSS. This command reinitializes the DSS into a new screen format, and any processing begun on the old screen format must be discarded so as not to clutter the new screen. A special secondary address (30) is sent instead of the standard address to identify the command as primary. When parallel poll is asserted after this command is received, the DSS clears its queues of all commands being processed except for the primary command, and the controller simultaneously discards all queued commands for the DSS, thereby setting the two subsystems to known and consistent states.

A device can process several commands concurrently at different priority levels. Separate queues are maintained for the device, one queue for each command level, and a command is sent to the device on a given priority level only after the previous command on that level has been completed. The first command byte is the level number, indicating to the device the priority this command is to be given. The controller is informed of the completion of processing the current command on a priority level through an SRQ followed by status bytes, similar to the way a checksum error is reported. When this is done, that priority level is tagged as available, and another command can be transmitted at that level.

In some instances, the message to be transmitted is very brief, such as a pulse indicating it is time to generate the next M-mode line for the primary display. Here, fast processing is important and the information content of the message is minimal. Instead of a mnemonic command, just a secondary listen address is transmitted as a code specifying the desired action, and no handshaking or error detection is performed. The only requirement is that the parallel poll response from the device must be affirmative before the secondary address is sent.

Often data must be transferred from the DSS or scanner to the controller. When this is done, a secondary talk address to the device indicates the type of data expected in the transfer. A checksum byte is sent as part of every input transfer, and the controller processes an error in a way appropriate to the type of transfer. In some cases, it just inputs the same information again, while in other cases, such as when only one column of a screen image has an error, action is taken only after several checksum errors occur.

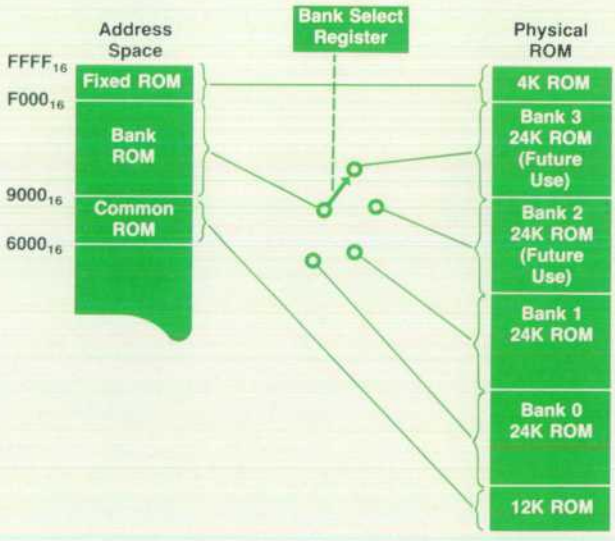

Fig. 2. *By using the bank-switching scheme diagrammed above, up to 96K of program ROM can be addressed by a 24K address space.*

77900A Controller Software Design

The controller software operates in an environment in which there are multiple inputs and outputs, each with its own set of timing considerations (see Fig. 1). Because of the varied requirements, a flexible and responsive software structure is needed. The structure chosen to meet these needs consists of a set of concurrent tasks and an interrupt processing capability. This concurrent program environment is created by using a real-time operating system.

The operating system is based upon an executive implemented for the HP 78500 Patient Information Center. This operating system is a compact software package providing priority scheduling of processes, critical regions, semaphores, interrupt processing and return, and a lowest-priority idle process allowing background debugging during software development.[1] A number of enhancements were made to this executive to meet the needs of the ultrasound system. These enhancements include dynamic memory allocation, message buffers sent with and without wait, and bank-switching memory control.

Dynamic memory is required to pass pieces of information from one process to another. This information is passed by using the message buffer facility. One example is the passing of the reception of a keystroke from the key scanning process to the process that performs the desired action for that keystroke. In this case, a block of memory containing the key process information is sent without wait to the keystroke processor.

Bank switching makes it possible to assign large amounts of program ROM (presently about 50K words) to a limited address space (36K) by providing several sets (banks) of physical memory in the same address space, with only one 24K bank enabled at a time (see Fig. 2). This bank switching is accomplished through the setting of the bank select register. One section of the ROM address space is not switchable and is called the common ROM area. Each process is loaded so that it and the subroutines it calls reside entirely in one bank and/or in the common ROM area. The priority scheduler (which itself resides in the common ROM area) selects the proper bank before branching to the address of the process being scheduled. Thus, program execution remains in the selected bank until an interrupt occurs and the scheduler is called upon to start another process.

Within the concurrent program environment created by the operating system, many processes are set up to perform the needed processing in the controller (see Fig. 3). Each process executes when required by some external event (signified by some interrupt) or as determined by the output requirements of the task. Some of the major processes are described in detail below.

Timekeeping. A processor interrupt occurs every 5 ms. Every fourth interrupt, a semaphore is signaled by the interrupt handler. A timekeeping process, KEEP_TIME, waits for the semaphore, and when it is received, a list of count values called the timetable is scanned. Items in this list are set by processes that require real-time intervals to be measured. Each counter is set to the number of milliseconds in the desired interval, and KEEP_TIME decrements each nonzero counter by 20 ms each time it runs. If a counter value becomes zero or negative, the corresponding process is signaled.

Keyboard Scanning. No key-scanning LSI interface chips are used in the 77020A Ultrasound System. Instead, the control panel is interfaced to the controller's microprocessor as memory, with each word containing the states (released or depressed) of eight keys. The key-scanning process KEY_SCAN is signaled every 20 ms by the timekeeping process.

Each time KEY_SCAN runs, it compares the state of each key with the last known state. If the state is different, a possible transition is noted for the key. During the next pass, KEY_SCAN checks the possible transition, and if the key still differs from its old state, a key transition is noted and a message indicating the keystroke is sent to the process KEY_ROUTINE_SELECT. Both downstrokes and upstrokes for a key can be processed. This double-pass key scanning

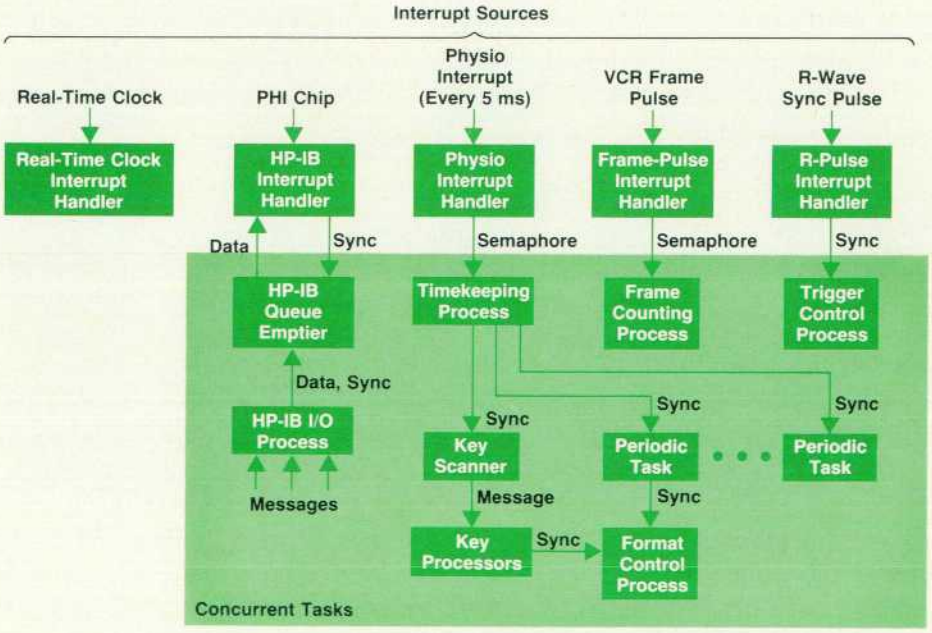

Fig. 3. *Modules and interrupt sources operating within the 77900A Controller's concurrent program environment.*

provides some noise immunity, since a key transition lasting less than 20 ms is rejected.

When KEY_ROUTINE_SELECT receives a key message from KEY_SCAN, it looks up the key in a table and finds the address of a subroutine to call. This subroutine performs the processing required for the selected key. As part of that processing, it may signal other processes or set a timetable value to begin repetitive processing (as for cursor motion control).

KEY_SCAN and KEY_ROUTINE_SELECT are separated in this way so that the keyboard scan rate is not affected by the amount of processing required for any one key. By making the scanning and processing independent, the operator enjoys a fast-response keyboard and the key processing can be done without regard for the effect of the processing time on keyboard performance.

HP-IB Input and Output. The scanner and display subsystems are interfaced to the controller much like peripheral devices are interfaced to a general-purpose computer. Processes in the controller communicate with the two external subsystems by sending read and write requests to the HP-IB I/O process via system messages (see Fig. 4). Each message contains the device address, the secondary address, the transfer length, and the source or destination address of the data in memory. The HP-IB I/O package then performs the requested bus transfer. For buffered output, the process builds the message in a dynamic memory block, and the HP-IB I/O software releases the memory after the transfer is completed. For input or unbuffered output, the message is sent to the HP-IB I/O process with wait. The sending process is immediately suspended and later restarted by the HP-IB I/O software after the transfer is completed.

A tree-like queue structure exists for handling the input and output requests pending for the HP-IB (see Fig. 5). The HP-IB I/O process adds the specified message to the proper message queue and signals the HPIB.Q_EMPTIER process. This process examines the queues and finds the next eligible message. It builds a data table called the driving table, which describes the characters that must be sent to and from the PHI interface chip for the desired transfer to occur. Then HPIB.Q_EMPTIER enables PHI interrupts, and an interrupt brings control to the PHI interrupt handler. Using the driving table as a guide, the interrupt handler reads and writes the required characters to the PHI chip. Upon completion of the transfer, the PHI interrupt handler updates the queue and signals HPIB.Q_EMPTIER to check for another transfer pending in the queue. If there is one, the pending message is processed in the manner just described. Otherwise, HPIB.Q_EMPTIER suspends operation and waits for a new signal indicating that the queue status has changed, whereupon it begins the above process all over again.

Display Formatting. Any process in the controller can change the variables describing the format of the display. When this is done, the process signals another process called the FORMATTER. The FORMATTER's job is to rebuild the format of the display by sending a set of HP-IB commands to the scanner and DSS. The first command of the set is the primary command. The primary command allows a synchronized clear of all pending DSS commands. The building of the new screen format can therefore proceed without interference from previously buffered commands. The primary command is followed by text and graphics commands to generate the desired display.

Video Cassette Recorder Control. Control of an external video cassette recorder (VCR) is provided through the 77020A's control panel or through the VCR's front-panel controls. Status lines from the recorder are monitored and the states of the 77020A and of the VCR are maintained by the controller software. If a 77020A VCR control is pressed, the software responds by updating the system state and setting a corresponding VCR state through a remote-control VCR interface. If instead the VCR controls are perturbed, the software recognizes the change of status and changes the 77020A System state to correspond to the new VCR state. The 77020A then displays the current VCR state on its control panel. If the current VCR state is a playback state, the DSS is commanded to select VCR input video as a signal source rather than scanner image data, and the scanner is commanded to stop scanning.

Stripchart Recorder Control. A finite state machine in the controller software controls the operation of the stripchart recorder (see Fig. 6). Valid state machine inputs consist of **CHART** and **FRAME** keystrokes and timing signals from the timekeeping processes. Using these inputs, a new stripchart state is selected, and the stripchart recorder is controlled to match its operation to the new state. This type of control permits features such as automatic paper development after recorder shutoff and proper paper speed changes when changing from **FRAME** to M-mode recording.

77200A Scanner Software Design

The software for the scanner performs three major functions. First, a scanning loop is run during normal system operation to control the scanning process. Second, the software handles the communication with the controller via the internal HP-IB. Finally, the software is responsible for taking control of scanner hardware functions during resident tests and for coordinating those tests within the scanner.

The loop software in the scanner accounts for about 2K of the 12K of code space currently used. Once the power-on sequence is completed, the scanner's microprocessor con-

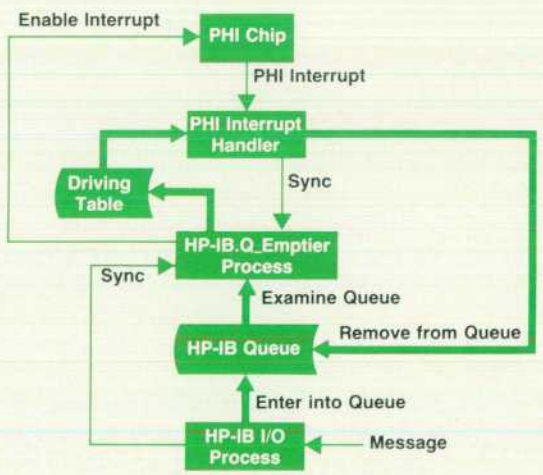

Fig. 4. *Implementation of HP-IB control by the 77900A Controller. For details of the HP-IB queue, see Fig. 5.*

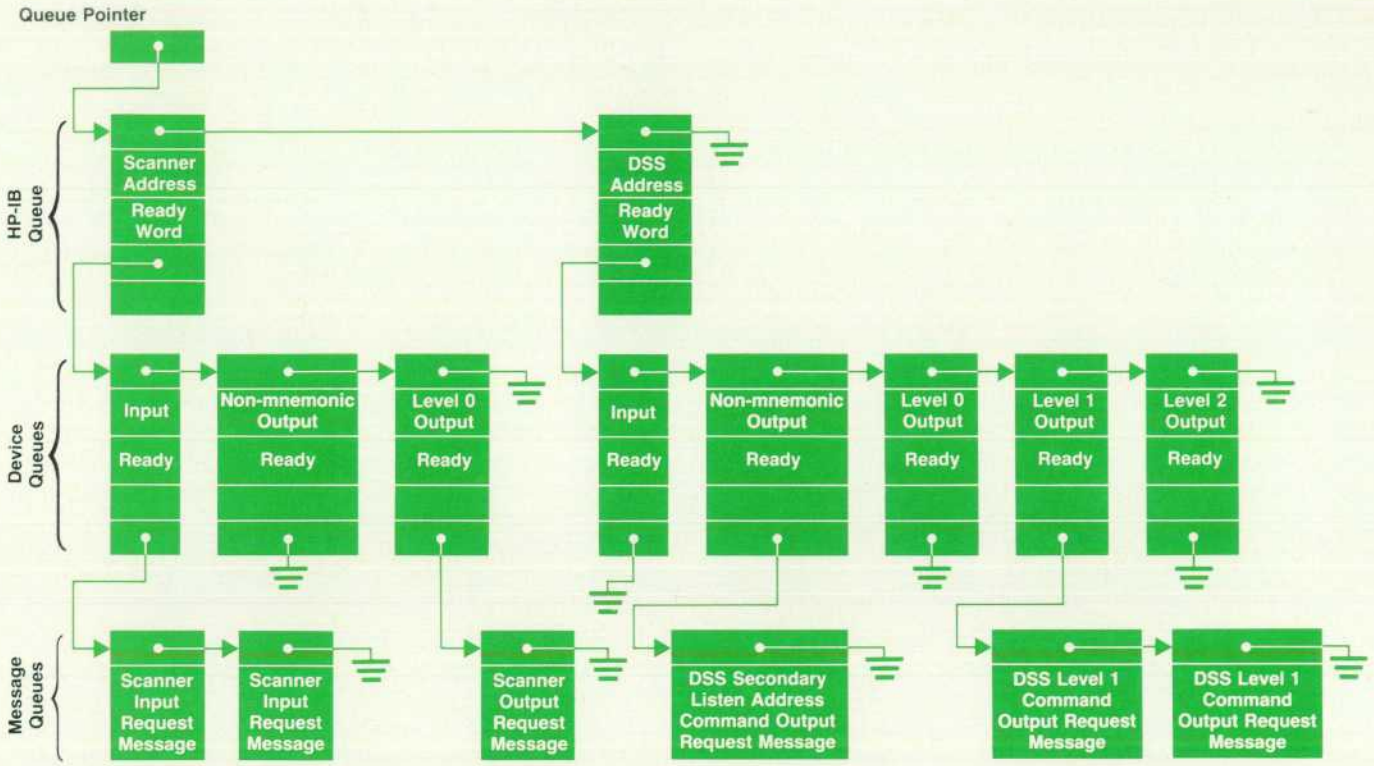

Fig. 5. *Outline of device and message queues for the HP-IB queue.*

tinually executes code in the scanning loop except for the occasional HP-IB command and associated processing requirements. This loop sets the hardware action of obtaining a line of acoustic data into motion. The sector display is made up of 121 radial acoustic rays originating at the face of the transducer. Each line is assigned a number, with 0 indicating the center line. Lines to the left of center have decreasing numbers, those to the right have increasing numbers. Scanning occurs from left to right and a complete sequence of 121 lines numbered from −60 to +60 constitutes a frame.

The line sequence is under software control to allow for two different modes of operation. In the sector-only mode, lines are transmitted in sequential order. In M-mode, scanning alternates between sector lines and M-mode lines. The M-mode lines provide high-speed data to the stripchart recorder for hard-copy output. In addition, the controller periodically commands the scanner to transmit an extra M-mode line to the display. The approximate rate of M-mode lines to the recorder is 900 Hz, while the rate to the display varies with the setting of the **CHART SPEED** control.

Acquiring data for a scan line involves a software-hardware handshake using a signal called BUSY (see Fig. 7). While the scanner is receiving acoustic information, BUSY is true. This signal disables the microprocessor's address and data buses from the motherboard to reduce digital noise in the sensitive acoustic receiver circuitry. In the meantime, the processor computes the control words for the next scan line. This process takes much less than the 208 μs available to the software. Therefore, interrupts are enabled and HP-IB commands are read from the bus and queued in memory for action after the end of the current frame. After calculating the control words, the processor enters a wait loop, polling the BUSY signal until a false logic level is detected. The processor then loads some hardware registers with control values for the next line and instructs the hardware that the next line is ready. A synchronous timer pulse initiates the process for the next line. The software must always lead the hardware from the time BUSY goes false to the synchronous timing pulse. This time is 67 μs in the worst case. The timing constraints result in 275 μs per line, yielding a 30.05-Hz frame rate for 121 lines.

As stated previously, the processor has time to accumu-

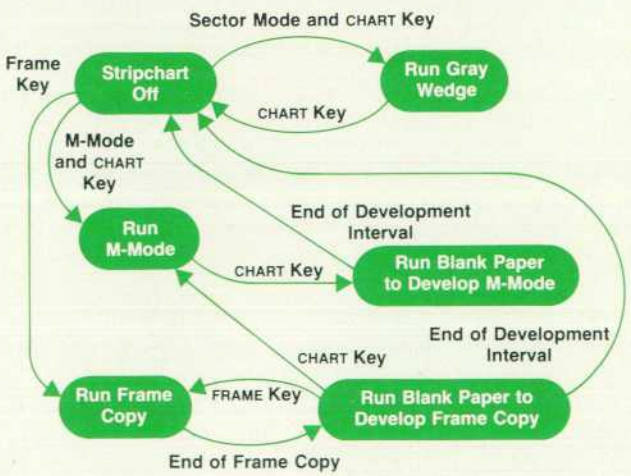

Fig. 6. *Simplified state machine for the 77020A's stripchart recorder.*

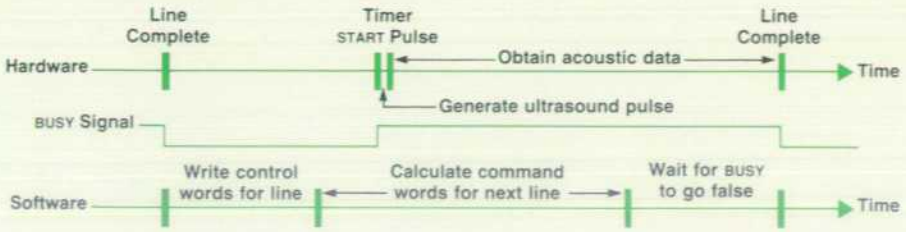

Fig. 7. *Interaction of the 77200A Scanner's main loop software with scanning hardware.*

late HP-IB commands during the time that the lines are being scanned. Secondary-address HP-IB commands are processed as they are received. In most cases, the action is taken immediately after reception of a command, as for M-mode triggers, requests for status, and the like. However, in the case of a secondary address indicating a mnemonic command to follow, the mnemonic and associated parameters are instead placed in a buffer for processing during the next interframe interval. At the end of the frame, a check is made to see if any mnemonic command is buffered, and if so, it is executed. Since all mnemonic commands change the display format and thereby destroy the frame-to-frame continuity, processing them between frames causes no violations of the 30-Hz frame rate.

77400A Display Subsystem Software Design

The DSS software controls the DSS hardware and maintains the displayed information, including sector display, M-mode tracings, physiological waveforms, characters, special symbols, and custom graphics. To perform this job, the software must coordinate the reception of HP-IB commands with real-time interrupts and generate correct images on the screen. To handle these requirements simultaneously, concurrent processing is required. An operating environment allowing concurrent processes with some operating system constructs is implemented by a task management system, or TMS (see Fig. 8).

Task Management System. TMS operation centers around a prioritized list of tasks, ready to execute, called the PROCESS_Q. This list maintains the status of each priority level. A level is either dormant, ready to run but not yet started, or currently executing. With this structure there can be only one task on a level at any time. There is no queueing on levels within the DSS. This allows the user to define the priority of a task, knowing that the task will run to completion before a lower-priority task executes. Thus commands that must execute quickly, such as those drawing the physiological waveforms, are able to interrupt lower-priority tasks such as the commands that draw characters. After the higher-priority task is completed, the interrupted lower-priority task is resumed.

Given the prioritized list of tasks, only a limited set of operating system constructs is needed. A few are used simply to allow the system to execute, such as putting a task on the list ready to run (dispatching a process), taking a task off the list when it has completed (exiting a process), selecting the highest-priority task ready to run (selecting next process), and initializing the list to start. Two additional constructs are needed in the DSS software: one to suspend a task in progress, allowing lower-priority tasks to run, and one to resume a suspended task.

HP-IB Command Processing. One of the major jobs of the DSS software is handling the HP-IB commands. The interrupt capability of the PHI chip is used to signal when bytes are received over the HP-IB. This allows a process to be dispatched to handle the command bytes as they come over the bus. This task is dispatched on the highest-priority level and therefore continues reading bytes until completion without any lower-priority tasks running. This task follows the ultrasound system's HP-IB protocol and carries out the handshake sequence. As the bytes of the command are read in, they are stored in a RAM buffer. There is a buffer for each level in the PROCESS_Q. Since all mnemonic commands are received with an HP-IB level, this level

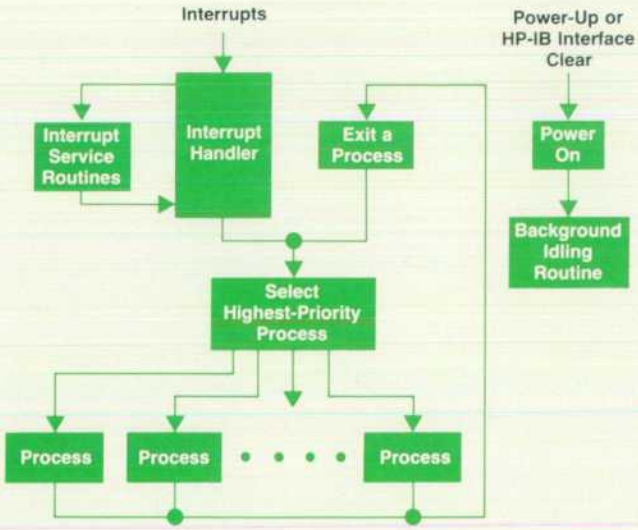

Fig. 8. *DSS software architecture.*

number is mapped into an internal PROCESS_Q level, and the bytes are stored in this level's buffer. Since only one task is running on any given level, there is no conflict in accessing the RAM buffers. After the entire command is received, action is taken based on the command type. If the command is not a primary command, it is immediately dispatched at a priority corresponding to the command level. If the command is a primary command, a special HP-IB handshake is performed to lock the controller and DSS together in time. With the two devices synchronized, all real-time commands in the queue and in progress are flushed, leaving no possibility of deadlock. After this handshake is completed, the primary command is dispatched for immediate execution.

When a task is dispatched, it is placed in PROCESS_Q ready to run. There is a separate task for each HP-IB command received. Each task interprets the parameters received over the HP-IB differently, getting them from the RAM buffer for its own level. When command execution is completed, the controller is notified through a service request and subsequent status transmission.

Display of Physiological Waveforms. Depending on the selected display format, one or four channels of physiological waveforms, such as ECG, heartsound, or pressure waveforms, can be displayed on the screen along with ultrasound image data. These channels are sampled in the controller and sent to the DSS for display, one column at a time. The rate at which columns are sent to the DSS determines the speed at which the waveform is presented on the screen; one column every 50 ms produces a display speed of 10 mm/s, while one column every 5 ms produces a 100-mm/s display speed. The DSS accepts these physiological data points and applies a smoothing algorithm, yielding a display of the physiological waveforms from the discrete display memory that doesn't look jagged or "steppy."

Quantitative Analysis

Besides the anatomical and functional information available in an ultrasound image, significant quantitative information can be obtained from both the two-dimensional and M-mode presentations. Two medical specialties in particular that can benefit from this kind of quantitative study are cardiology and obstetrics. The computational power of the 16-bit microprocessor used in the controller, together with the graphic display capabilities inherent in the DSS, provide an environment well suited to the implementation of a quantitative analysis capability.[2]

To manipulate the numerical values involved in measurements and calculations, a floating-point data representation is required. For this purpose, a software floating-point library provides the arithmetic functions ADD, SUBTRACT, MULTIPLY, DIVIDE, SQUARE ROOT and EXPONENTIAL. A data format is used that is very well suited to the microprocessor's instruction set. This format consists of a single- or double-word two's-complement mantissa with a single-word two's-complement exponent. All input values are stored with a single-word mantissa, while all intermediate calculations are carried out with double-word mantissas to maintain accuracy during the calculations. Final results are displayed with three-significant-digit precision.

Error Processing

Extensive error checking is built into the operating software in all three subsystems. A key feature of the error handling software is the use of an error log—a list of error codes recorded and maintained in nonvolatile memory. Errors detected in any subsystem are reported to the controller via the internal HP-IB. From the controller, they are reported to the operator and written to the error log. The contents of the error log can be retrieved by service personnel for diagnosis of many hardware faults. In addition, logging the existence of the errors gives valuable clues to resolving problems caused by errors that are difficult to reproduce.

For several types of errors, it is possible to report the error directly to the operator, log it, and continue normal operation. If recovery is not possible for the particular error being processed, the 77020A enters a state of operation known as default mode. In this state, the scanner software independently sets up the scanner to scan a fixed-depth sector and the DSS is similarly set up to display it, if possible. Only direct imaging controls such as **TRANSMIT** power, receive **COMPRESSION**, and **TGC** (time gain compensation) are active. When a nonrecoverable error occurs, it is not known whether the system hardware is capable of producing an image, but the attempt is made anyway. This permits emergency use of limited system capabilities in the presence of a hardware failure. Most users would choose not to use the system in this condition, but it is felt that the default mode operation is preferable to no operation at all, should the failure occur at an inopportune moment during a patient examination.

Resident Tests

The 77020A Ultrasound System has extensive self-test capability which can be used to verify that the system is functioning properly before it leaves the factory, and to isolate hardware failures in the field.

Every time the system is turned on or reset, a series of tests called core tests is run in each subsystem. If all three subsystems pass their core tests, the ability of the subsystems to work together is tested. Handshake tests make certain that all basic bus control functions are operational. Loop tests assure that the three subsystems can communicate with each other under normal bus protocol conditions.

Additional test sets can be run at the discretion of the user. The first of these is initiated by putting the system's test switch in the **BASIC** test position. **BASIC** tests are intended to verify the proper operation of all essential hardware not tested in the core test sequence because of the length of time required to execute them.

If the test switch is set to the **INTERACTIVE** test position, the system enters interactive test mode. The interactive tests are intended for use mainly by field service personnel to isolate hardware failures to at least the board level.

The self-test software used by the 77020A has been implemented in much the same way as the normal mode software. A software module in the controller, referred to as the resident test executive, has the responsibility for providing the user interface and for coordinating the execu-

tion of the tests. Test commands are entered through the keyboard and are interpreted by the resident test executive, which then sends out commands to the three subsystems. Each of the subsystems, including the controller, has a subsystem test coordinator which carries out the actual execution of the tests and reports the results back to the test executive. Communication with the controller's test coordinator is carried out using message buffers, whereas communication with the DSS and scanner test coordinators takes place over the HP-IB.

The results of the tests are displayed on the primary display and a five-digit hexadecimal display. The test results are redundantly displayed in case the DSS cannot output data to the primary display. In addition, each of the subsystems has its own hexadecimal display, located on the subsystem's processor card, which is used to indicate the failure of a core test. This allows testing each of the subsystems' core hardware independently.

Acknowledgments

Many people contributed to the 77020A Ultrasound System software effort. Rachel Kinicki, Larry Salant, Lou Schoof and Joe Sestrich were major contributors. Alwyn D'Sa and John McGee contributed to the DSS software effort, and John initiated the HP-IB command levels concept. Jim Fearnside, Al Langguth, Syd Karp and Rick Snyder contributed to the scanner software design. In addition, numerous hardware and software designers had a part in the resident self-test modules for the numerous system components.

The work and ideas of several others were used to strengthen the design. J. Evan Deardorff developed the original operating system upon which the controller operating system is based. Radha Basu did all the groundwork leading up to the resident self-test scheme used in the system.

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2. R.M. Kinicki, "Quantitative Analysis for Ultrasound Imaging," *Hewlett-Packard Journal*, Vol. 34, no. 10, October 1983.

Electronic Scanner for a Phased-Array Ultrasound Transducer

This subsystem controls the transmission and reception of ultrasound pulses by 64 transducer elements to scan a 90° sector and collect data for an ultrasound image.

by Ronald D. Gatzke, James T. Fearnside, and Sydney M. Karp

THE BEAM OF ULTRASOUND PULSES transmitted and received by the transducer for the HP 77020A Ultrasound Imaging System[1] is directed and focused by controlling the timing of the excitation and received signal for each transducer element. To understand how this works, consider the hypothetical phased-array system shown in Fig. 1. This system consists of n parallel channels, each with its own transmitter and receiver. Each transmitter outputs a short-duration ultrasound pulse into the human body. This pulse is partially reflected back to the transducer array by various structures and tissues in the body. The receivers detect the reflected acoustic energy and send the resulting signal from each element to a delay mechanism and a summing junction.

Transmit Steering and Focusing

By appropriate choices of the delay settings, beam steering can be done. If the transmit delays are set so that the delay τ_i for element i is equal to $(i-1)T$, then an acoustic wave is launched from element 1 at time 0, followed by a wave from element 2 at time T, and so on. Referring to Fig. 2a, these waves add together to form a composite plane wave traveling in a direction from the normal to the array according to the equation $\theta=\sin^{-1}(Tv/D)$, where v is the velocity of sound in the body, D is the centerline spacing of the elements, and T is the delay between adjacent elements. The composite wave also can be formed into a nonplanar wave by choosing a specific delay for each element. An appropriate combination of delays can result in a curved wavefront that converges (is focused) at a single point (see Fig. 2b).

Receive Steering and Focusing

Reception of a wave operates in a reverse manner. A planar wave reflected from a target located θ degrees away from the array's axis of symmetry arrives at each element at a different time. The response of each element is amplified, delayed, and then added to the other element responses by the summing junction (see Fig. 1). Constructive addition of the element responses occurs when the

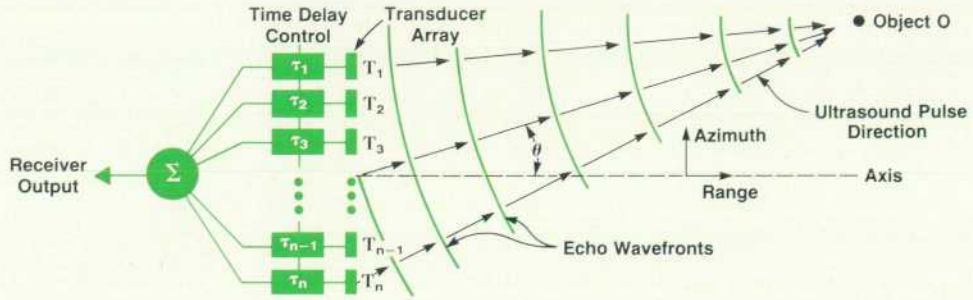


Fig. 1. *Block diagram of basic phased-array system.*

delay for each element i is adjusted to a value equal to $(i-1)(D/v)\sin\theta$.

In an actual imaging situation, waves reflected from targets in the body arrive at the array as curved wavefronts whose radius of curvature increases with the depth of the target. It is possible in a phased-array system to alter the delay settings dynamically so that the delay profile across the elements will track this variation in curvature as shown in Fig. 2b. This allows the array to be focused on targets at progressively increasing distances, providing the array with an extended depth of field.

Resolution

The resolving power of any ultrasound imaging system is dependent on the acoustic beamwidth, which can be checked by measuring the system's spatial impulse response. These beamplots are made by moving a small point reflector in an arc around the array. A typical result is shown in Fig. 3. The shape of the acoustic beam is controlled by the array element spacing, element weighting, number of elements, transducer response, the transmitted pulse waveform, and the receiver bandpass characteristics. In the narrowband case when the target is placed at infinity, sidelobes occur at $\theta=\sin^{-1}(m\lambda/W)$, where m is the sidelobe number (1, 2, 3,...), λ is the acoustic wavelength, and W is the width (aperture) of the array.

The sidelobe floor of the beam pattern is controlled by aperture width, transducer vibration modes, and the amount of error allowed when setting the delay for each element. Because body target scatter cross sections can vary as much as 50 dB, it is desirable to have the sidelobe floor more than 50 dB below the peak amplitude of the main beam.

If all elements have equal weighting (same gain), the sidelobe amplitudes fall off at the rate $4/(\pi(2m+1))^2$. Grating lobes arise because the array contains a number of discrete receivers rather than the ideal case where radiation is received continuously across the aperture. The peak of each grating lobe occurs whenever two adjacent elements satisfy the equation $(D/x\lambda)(\sin\theta-\sin\theta_o)=1$, where θ is the angle to the target, θ_o is the angle of the transmitted beam, and $x=1,2,3,.....$ These unwanted grating lobes lead to a false image (artifact). If the element spacing is made sufficiently small, say $D=\lambda/2$, then there is no combination of target and beam angles (for angles less than $\pm45°$) that satisfies the above grating lobe peak equation.

The elevation beamplot is similar to the azimuth plot with the exception that grating lobes are absent because the reflected pulse is received continuously across the height of the array.

Axial (target distance) resolution is determined by the system's time response. Short ultrasound pulses yield better axial resolution; therefore, large transducer and scanner bandwidths are required.

The spatial response of the system for any target can be found by performing the appropriate three-dimensional convolution with the system's impulse response. For a point target, this operation yields an ellipsoidal resolution cell as shown in Fig. 4. The azimuth and elevation resolutions remain approximately constant at a given depth for subtended angles less than $\pm45°$. However, as target depth increases, the resolution cell changes shape, becoming larger in both elevation and azimuth dimensions. Deep targets, then, are not as well resolved as shallow targets.

Physical Constraints

Several physical properties of ultrasound imaging must be considered in determining the best compromise for dif-

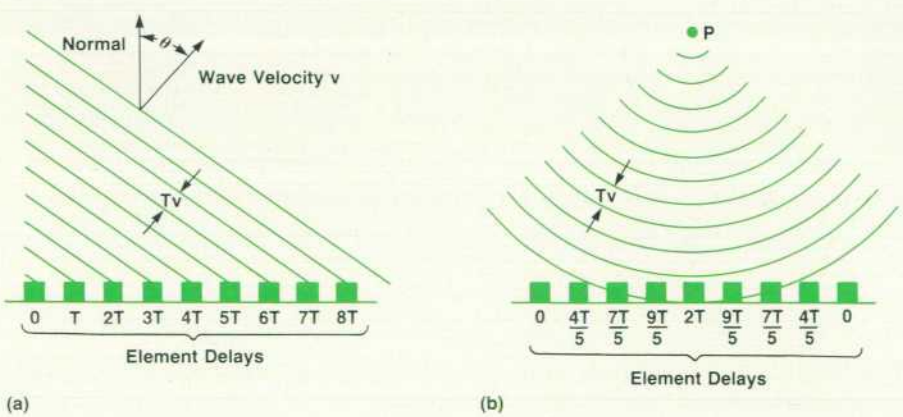


Fig. 2. *(a) Phased array radiating a plane wave at an angle θ with a velocity v. (b) Phased array radiating a wave focused at a point P.*

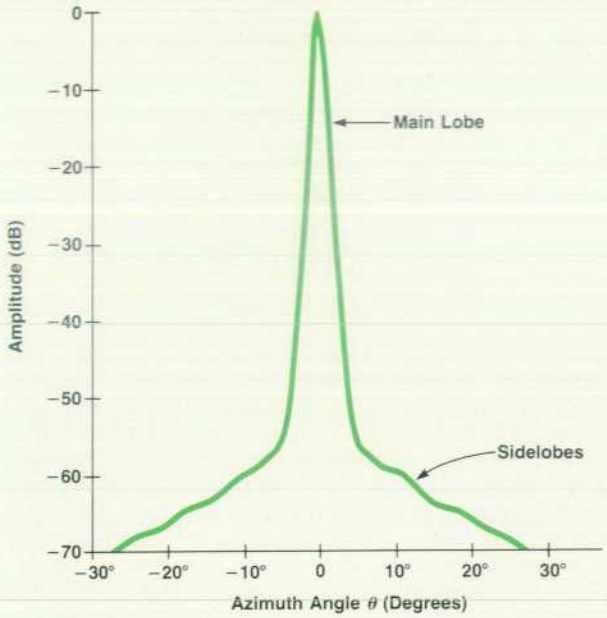
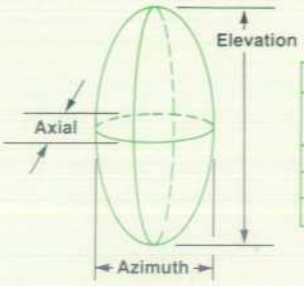


Fig. 3. *Plot of beam intensity versus azimuth angle for an acoustic beam directed normal to the phased-array transducer.*



−6-dB Resolution (mm)			
	Center Frequency (MHz)		
	2.5	3.5	5.0
Axial	1.4	0.9	0.9
Azimuth	2.0	2.0	1.4
Elevation	3.5	1.8	1.6

Fig. 4. *Definition of resolution cell with dimensions versus frequency for −6-dB response.*

fering imaging requirements. The 77020A operates at three frequencies: 2.5, 3.5, and 5.0 MHz. The higher-frequency transducers provide shorter pulse responses and acoustic wavelengths, so they provide better axial resolution.

The temptation to use high-frequency transducers for all imaging is tempered by the frequency-dependent nature of the attenuation of ultrasound in the human body. This attenuation, a function of both distance and frequency, is typically 0.7 dB/MHz-cm. Therefore, for any given target depth, a 5.0-MHz wave will experience twice the dB attenuation of a 2.5-MHz wave. This severely limits the maximum depth for ultrasound imaging. The 77020A can typically image targets 24 cm deep at 2.5 MHz, 16 cm deep at 3.5 MHz, and 13 cm deep at 5.0 MHz.

The dynamic range of the received ultrasound signal can span 100 dB from imaging bright shallow targets to dim distant targets. Because visual displays typically have a dynamic range less than 40 dB, it is customary in ultrasound imaging systems to increase the receiver gain with the depth of the source of the acoustic echoes. Since the time an echo is received is directly related to depth, this varying gain function is called TGC (time gain compensation). To map the 100 dB of input dynamic range into the 40 dB of display range, the TGC function must increase the receiver gain over a 60-dB range.

Hardware Architecture

Fig. 5 shows a functional block diagram of the 77200A Scanner. The 64-element transducer array is driven by 64 individually delayed pulse generators and FET amplifiers. The outputs of the transducer elements for a received pulse echo are amplified by the receiver boards and added together on the summing delay boards. The summed RF signal is processed and detected by the video processor and digitized for transmission to the 77400A Display Subsystem. The processor board determines the angle and the order in which each of the ultrasound scan lines is transmitted and received to form the ultrasound image. It also commands the coefficient memory board to load the delay settings for transmit and receive steering and focusing of

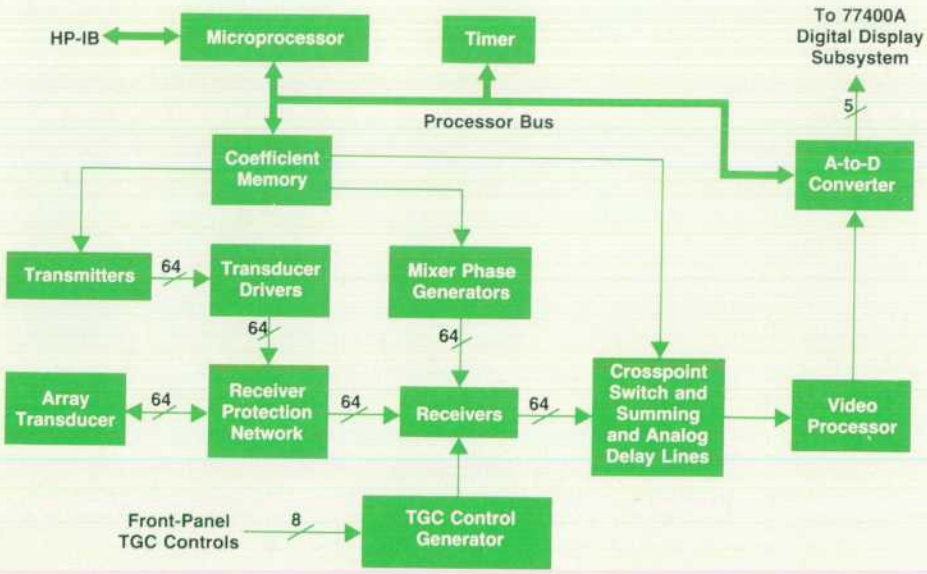


Fig. 5. *Block diagram of scanner system.*

A Mixing Scheme to Focus a Transducer Array Dynamically

by Robert N. McKnight

An acoustic echo from a point in the human body reaches each element in the transducer array after some propagation time. This time is different for each element and depends only on the distance between each element and the point because the velocity of sound (1540 m/s) in soft tissue is essentially constant. These differences in path length can be electronically compensated to focus the array on the point, in effect enhancing reception of the echoes from the desired point and suppressing reception of echoes from other areas of the body. This is done by using delay lines and phase shifters that are combined so that the echoes from the desired focal point are coherently summed (see Fig. 1). The delay line and phase shifter combinations are electrically varied very rapidly to focus the array at points deeper and deeper in the body along the direction of the incident ultrasound pulse. The result is that every point in the displayed ultrasound image is in focus.

However, it is not easy to implement a dynamically focused system of 64 array elements at a reasonable cost. To see why this is so, consider the requirements for dynamic focusing if it is implemented in a straightforward manner. From simple geometrical considerations, it can be shown that for a 64-element array with half-wavelength element spacing, a delay of up to 9 μs is required to scan a 90° sector electronically. The accuracy with

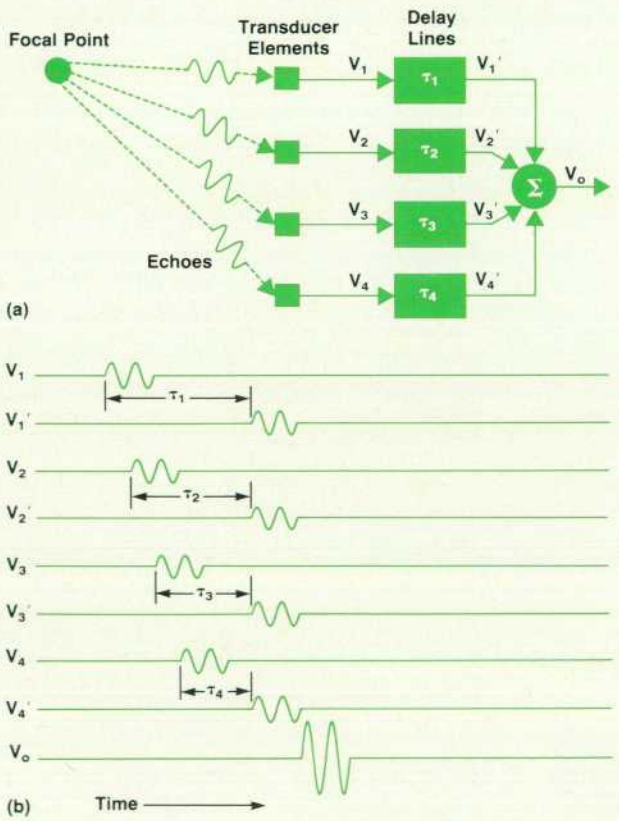


Fig. 1. *(a) Block diagram of simple transducer array system. (b) Signals received at each transducer, and signals after passing through the appropriate delay for each element.*

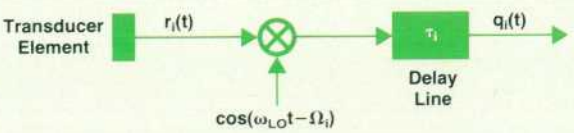


Fig. 2. *Diagram of single channel showing mixing and delay elements.*

which coherent summation for each point can be achieved depends on how well the echoes received by each element are aligned in time. This means that the delay chosen for each element must be accurate to within a fraction of a period for an acoustic wavelength. For example, at 2.5 MHz the acoustic wavelength in the body is 0.6 mm, corresponding to a period of about 0.4 μs. Hence, the delay line for each channel must be segmented into 200 or more delay elements to obtain adequate focusing. Thus a system of 64 such channels would require over 10,000 delay elements and as many switches to connect the received signals to the proper segment of each channel's delay line. This would be prohibitively expensive, and too bulky for a mobile system.

Let us alternatively suppose that the return echo can be readily modeled as a wave of the form $r(t) = A(t)\cos(\omega_o t + \phi(t))$, where the amplitude and phase are slowly varying relative to the center frequency ω_o. Given this situation, we can determine that coherent addition may be achieved by using coarsely quantized delay lines to align the amplitude envelopes and phase shifters to align the phases. Mathematically, the argument is analogous to that for the Shannon sampling theorem for a band-limited system, where the important parameter is the signal bandwidth, not merely the highest frequency. This tradeoff of delay line accuracy for phase shifters permits a substantial reduction in hardware complexity and cost without degrading performance.

A particularly useful way to implement the phase shifters is

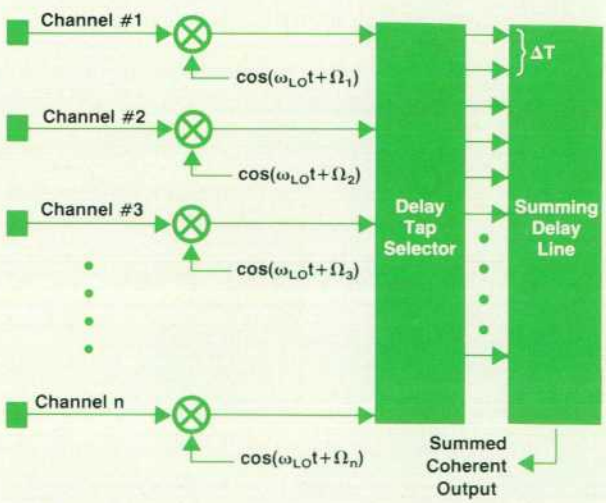


Fig. 3. *Simplified block diagram of system using mixers for each channel and a single tapped delay line to sum the channel signals. The phase Ω_i of the mixing frequency for each channel is chosen to provide the desired delay for that channel.*

with mixers. This is accomplished by generating from a very high-frequency clock a set of lower-frequency clocks all of the same frequency, but offset from each other by some small fraction of a period. Thus, we have a set of mixers whose local inputs are $\cos(\omega_{LO}t+\Omega_1)$, $\cos(\omega_{LO}t+\Omega_2)$,.....$\cos(\omega_{LO}t+\Omega_n)$. The use of mixers has the additional advantage of shifting the signal spectrum to lower frequencies, which relaxes certain component tolerances as well as delay line bandwidth requirements. The process of mixing before delay does add an additional phase correction term as we shall see, but this does not add complexity to the hardware.

To orient ourselves mathematically, let us consider the process of dynamic focusing during some comparatively short time between two adjacent focal points. If we perceive the signal as originating from the focal point at time $t=0$, then the signal received at the ith receiver channel at time $t=\tau_i$ is

$$r_i(t)=r(t-\tau_i)=A(t-\tau_i)\cos(\omega_o(t-\tau_i)+\phi(t-\tau_i))$$

Now if $\phi(t-\tau_i)=\phi_i$ at the focal point, then we see that the appropriate phase correction term to apply at the receiver is $\omega_o\tau_i-\phi_i$. Let us consider, however, what happens when we apply mixing before the delay (see Fig. 2). The signal at the mixer output is

$$\begin{aligned}&r_i(t)\cos(\omega_{LO}t-\Omega_i)\\&=(\tfrac{1}{2})A(t-\tau_i)\cos(\omega_{LO}t-\Omega_i-\omega_o(t-\tau_i)-\phi_i)\\&\quad+(\tfrac{1}{2})A(t-\tau_i)\cos(\omega_{LO}t-\Omega_i+\omega_o(t-\tau_i)+\phi_i)\end{aligned}$$

where the first term is the lower sideband product LSB and the second term is the upper sideband product USB.

From here on, we consider only the LSB assuming that the USB will ultimately be filtered out. We make the observation, however, that whatever phase correction Ω_i we apply to the LSB for phase coherence will not be the same for the USB. If we now allow the signal to pass through a delay of $m\Delta T$, we have the properly shifted phase coherent contribution of the ith channel given by

$$q_i(t)=(\tfrac{1}{2})A(t-\tau_i-m\Delta T)\cos((\omega_{LO}-\omega_o)(t-m\Delta T)-\Omega_i+\omega_o\tau_i-\phi_i)$$

where the phase correction term necessary for phase coherence is seen to be

$$\Omega_i=\omega_o\tau_i-\phi_i-(\omega_{LO}-\omega_o)m\Delta T$$

For proper alignment of the amplitude envelopes, the delay $m\Delta T$ is chosen such that the total delay $\tau_i+m\Delta T$ is approximately a constant over all channels.

This last simplification permits an architecture based on a common summing delay line rather than separate delay lines for each channel (Fig. 3).

the acoustic beam. Focusing for each scan line is done by altering the mixer phases individually for each of the 64 receiver channels.

Transmit Circuitry. The transmit delay circuitry is a master/slave system designed using conventional MSI digital technology. There are 32 master and 32 slave channels arranged in alternating fashion across the array. A master/slave cell is shown in Fig. 6. The master channel consists of counters which are loaded with the desired delay. A multiplexer selects one of several phase clocks to drive each counter and achieve the required delay between channels. The outputs of the master counters are pipelined through two flip-flops that are clocked 180° out of phase.

Each slave channel transmits at a variable time relative to the master channel on the right or on the left. The slave is programmed to select a master and one of that master's two flip-flops as a source to reclock a master transmit pulse in the slave's own output flip-flop. This ensures that for any relative delay needed by a slave, a pulse has already propagated through one of the two pipelined flip-flops and is available for reclocking. The slave's programming selects one of several different phase clocks to achieve the desired relative delay. Thus, the slave channels require no counters, greatly reducing the hardware required.

The digital pulse output of the transmit delay generator is applied to high-voltage driver stages. These stages use power MOSFETs to step up the voltage and current to the levels required to drive the transducer elements.

Receive Circuitry. The transducer array is connected to the receiver electronics through a protection network of high-voltage diodes. These diodes are forward-biased to provide low-impedance connections between each transducer element and its receiver. When the transmit driver stages fire, the high-voltage transient reverse-biases the diodes, blocking the high voltage from the receiver inputs.

The receiver section uses three groups of circuits (see Fig. 7). The output of each transducer element is coupled

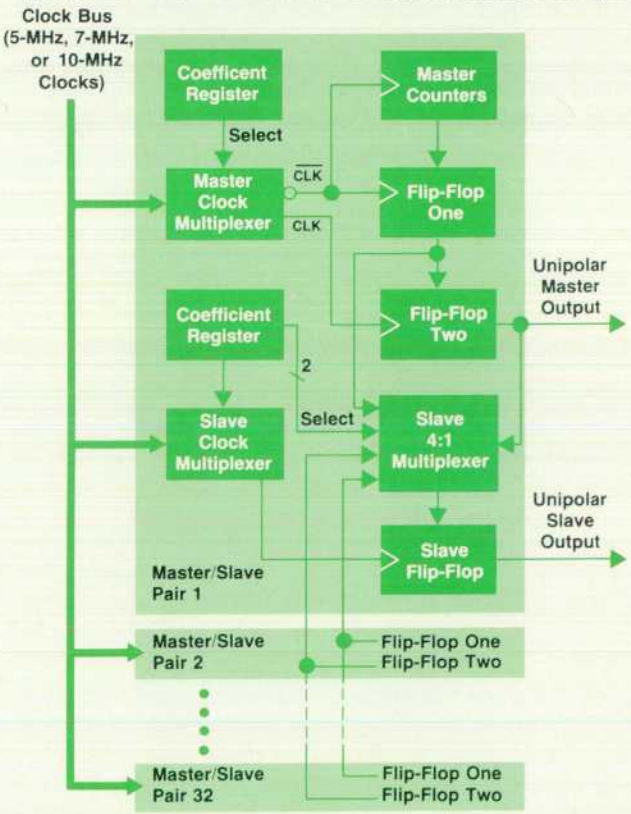


Fig. 6. *Master/slave cells for the 64 channel transmitters.*

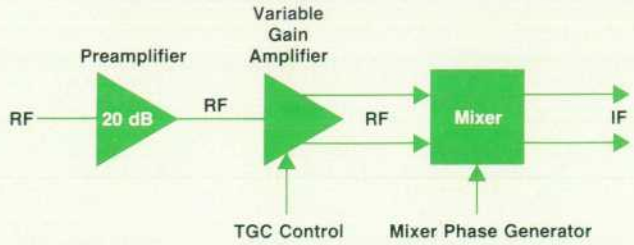


Fig. 7. *Receiver amplifier chain.*

to a low-noise amplifier whose input impedance matches the element's output impedance. A 2-dB noise figure is achieved by this stage. The amplified signal is then applied to the TGC amplifier, which adjusts its gain as a function of the time an echo is received. The gain can be varied over a 60-dB range by using a balanced differential amplifier whose output is directed either into the signal output path or to ground (see Fig. 8). The RF input to the TGC stage is converted into a current by Q1 and Q2. This current is applied to differential pairs Q3 and Q4, and Q5 and Q6. These devices divide the current, allowing only a fraction of the current to be coupled out of this stage. The TGC control voltage is varied with time and is synchronized with the transmit pulse. A nonlinear compensation circuit corrects for any nonlinearities in the differential stage attenuation response.

The TGC control voltage variation can be specified by the operator through the eight TGC controls on the front panel of the 77020A. These controls are successively sampled by an 8:1 multiplexer and applied to an integrator as shown in Fig. 9. A sample-and-hold circuit samples the integrated waveform each time a new TGC control setting is switched into the network, causing the integrator to ramp at a rate proportional to the difference between the old and new TGC values. The integrated output is then used to control the gain of the TGC stage.

The output of the TGC amplifier is applied to a balanced

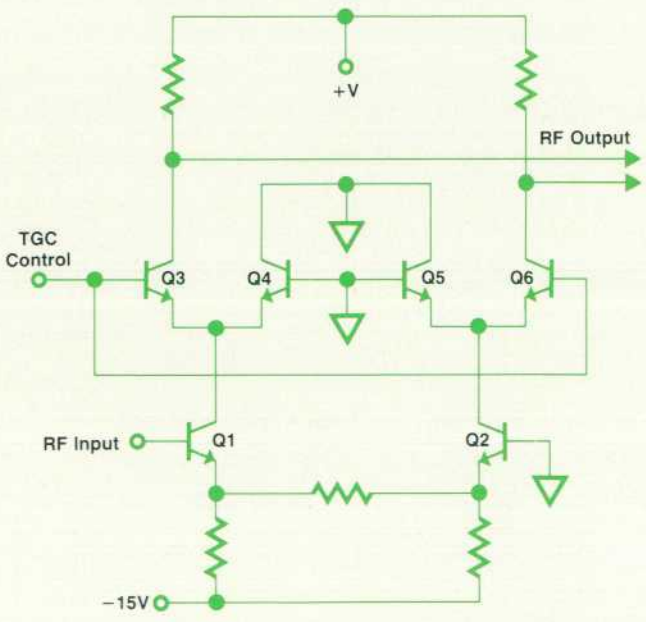


Fig. 8. *TGC (time gain compensation) variable gain cell.*

mixer. This mixer down-converts the RF signal to a lower-frequency IF signal to match the bandwidth of the succeeding delay stages. It also acts as a phase shifter to correct the phase of the received transducer signals.

Each mixer is driven by a mixer phase generator assigned only to that channel. This generator selects one of the phases of a digital clock. The selected phase is determined by a digital word appropriate to the observed target location. The clock is generated from the output of a ring counter operating at a multiple of the local oscillator frequency.

The output of each mixer is sent to a variable delay stage and then to a summing node where all receiver signals are combined to provide a coherent output for each scan line. The summing delay architecture used here (Fig. 10) allows a significant reduction in the number of expensive and bulky analog delay lines required. Individual receiver channels are connected via a crosspoint switch to one of the many taps in a single delay line. Each of the signals received from each element in the transducer array is individually guided to the appropriate delay tap. The set of receiver delays is different for each of the 121 scan lines that make up the ultrasound image.

The switch matrix is driven by the IF output from each receiver mixer. This IF signal is buffered by a differential-to-single-ended converter and fed to an M-position CMOS switch pole. The digital control word for each receiver is latched into a local memory in the tap selector to close the appropriate switch to connect the IF signal to the summing delay line. The IF signal for each receiver is then added to the differently delayed signals from the preceeding taps and the composite signal is delayed further by analog lumped-constant delay lines connected to the end of the summing delay line.

To maintain maximum phase accuracy in the summing delay line, all stages are dc coupled. A dc sense amplifier on the summing delay line output stage samples the output and provides a dc correction signal to each series-connected summing node to maintain the maximum dynamic range in this stage.

Video Processor

The output of the summing delay line is upconverted to a second IF and bandpass filtered to select the portion of the echo frequency spectrum to be detected and displayed (Fig. 11). At any depth, the echoes of interest can occupy a large dynamic range. In cardiac imaging, for example, the strength of the echoes from the muscle tissue (myocardium) at the back of the heart may be 45 dB below the strength of the echoes from the nearby interface of the heart with the lungs, yet both echoes may be of clinical interest.

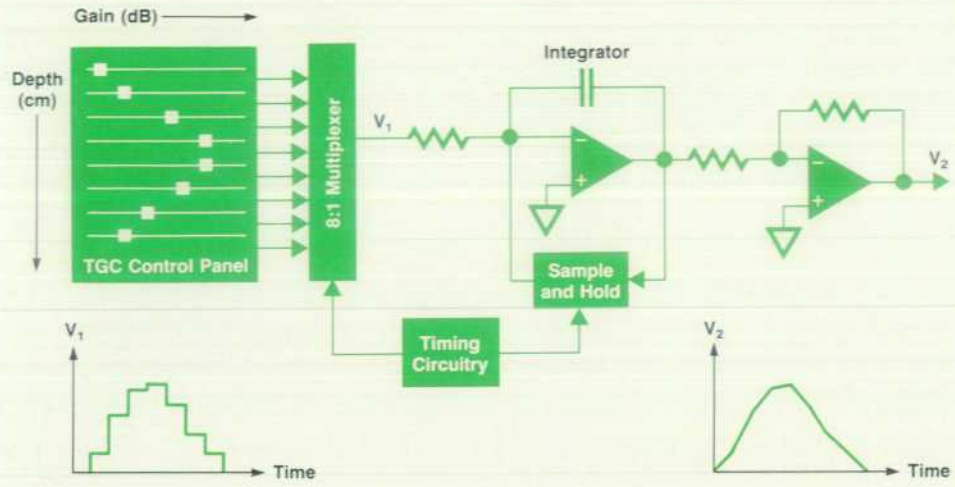


Fig. 9. *TGC control generator.*

It is a problem to display both of these echoes in the same image. If the gain is adjusted so that the heart-lung interface appears full white on the screen, the myocardial echoes will be invisible (the eye cannot distinguish differences in display intensities that are more than 25 dB below full white). If the gain is increased so that the myocardial echoes are clearly visible, the heart-lung interface portion of the display saturates and blooms on the screen.

Signal compression can make both signals visible at the same time without saturation. A continuously variable control on the front panel of the 77020A System allows the operator to vary the amount of compression. When compression is at a minimum, the echo-strength-to-display-brightness transfer function is linear. As compression is applied, the transfer function becomes more logarithmic.

By increasing the compression control, weaker echoes become more visible while strong echoes remain at the full-white level without saturation. Howver, too much compression makes acoustic noise visible. The compression level at which this clutter appears varies from patient to patient.

After compression, the signal is detected by full-wave rectification and low-pass filtering. In some diagnostic applications such as measuring wall thicknesses or chamber volumes, the operator is interested in detecting only wall boundaries. Under operator control the detected signal can be partially differentiated to emphasize edge structure.

After detection, the fully processed video signal is sent to an analog-to-digital converter (ADC), which digitizes the waveform and transmits it to the display subsystem described in the article on page 20.

Scanner Control

The primary control of the scanner is performed by a custom 16-bit silicon-on-sapphire microprocessor. This processor receives commands from the 77900A Controller via the 77020A System's internal HP-IB (IEEE 488) and a peripheral HP-IB interface (PHI) chip. The processor interprets the controller's commands and then programs control registers on various scanner cards via the scanner processor bus. The TGC card is programmed with the scanning depth so that it can distribute the TGC depth controls equally over the length of the acoustic scan line. Registers on the ADC card are programmed for sample rate and line type. The timer is programmed when to initiate loading coefficients, fire the transmitters, listen for echoes, and adjust the receive focal point. After all control registers are set up, the processor activates the timer and disconnects itself from all scanner buses to maintain a quiet scanner environment during the acquisition of the data for the scan line. The transmitting and receiving of the ultrasound pulse are then directed by the timer and coefficient memory cards. At the same time, the processor continues processing, preparing control register settings for the next scan line.

When the processor programs the sector angle, the coefficient memory card selects the coefficients corresponding to the angle of the scan line. Depending on the frequency and element spacing of the transducer probe, different sets of coefficients are selected.

The processor determines the sequence of sector and M-mode scan lines by programming a set of control bits before each line is fired. The architecture of a phased-array system allows lines to be fired at any angle in any sequence. This makes simultaneous two-dimensional and M-mode

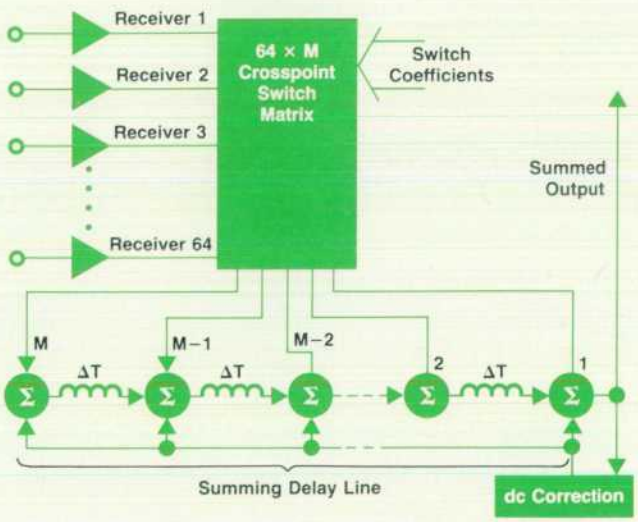


Fig. 10. *Crosspoint switch matrix and summing delay line circuit.*

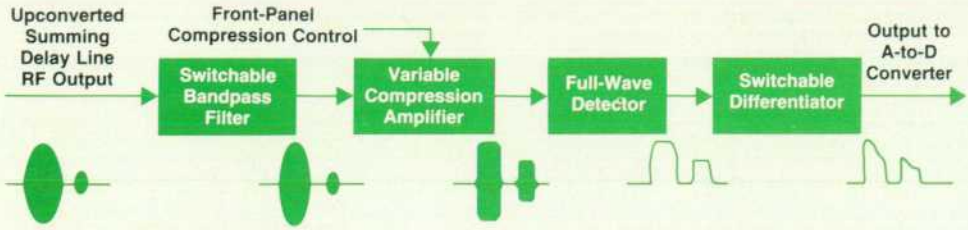


Fig. 11. *Video processing chain.*

scanning possible by interleaving M-mode and sector scan lines in the sequence.

A sequencer on the coefficient memory card addresses destination registers in the scanner to receive coefficients read out of memory onto a high-speed bus. The coefficients program transmitter delays, mixer phases, and delay line tap selections before transmitting an ultrasound pulse. After the pulse is transmitted, the mixers are updated with new coefficients to achieve dynamic focusing. This increases the imaging focal length with time as echoes return from targets deeper and deeper in the body.

The coefficient memory takes advantage of the symmetrical properties of the sector display geometry so that it need store coefficients for only one half of the sector. Thus coefficients used for the right side of the array when the right side of the sector is imaged can also be used for the left side of the array when the left side of the sector is imaged. Hardware on the coefficient memory card ensures that the correct coefficient is sent to the correct channel as a function of sector image half. This is accomplished by modifying the coefficient data and the destination addresses on the coefficient memory card.

Self-Test

The scanner has an extensive set of internal self-test programs run by its processor. This software locates faults to the board level, and in some cases, to the chip level. Digital tests exercise busing hardware, memories, and state machines. The processor isolates each analog path in turn by programming the tap selectors with the appropriate coefficients. The selected path is then stimulated by an internal test oscillator signal. A pair of synchronous detectors on the video card measure the resulting signal's amplitude and phase for comparison with required values.

Acknowledgments

Many people contributed to the development of the 77200A Scanner. Circuit designs were contributed by Jacques DesJardins, Jim Mniece, Bernie Savord, Arthur Dickey, and Sam Maslak. The mechanical design was done by Joe Fallica. The test software was written by Lou Schoof and Tony Fisher. The release to production was assisted by Charlie Grossman, Gary Trousill, and Jay Gaind. Service support planning was provided by Peter Dalis. Special thanks to the printed circuit layout and production departments without whose help this instrument would not have been possible.

The original concept of the summing delay line was invented by Rich Pering of HP Laboratories.

Reference

1. *Hewlett-Packard Journal*, Vol. 34, no.10, October 1983.

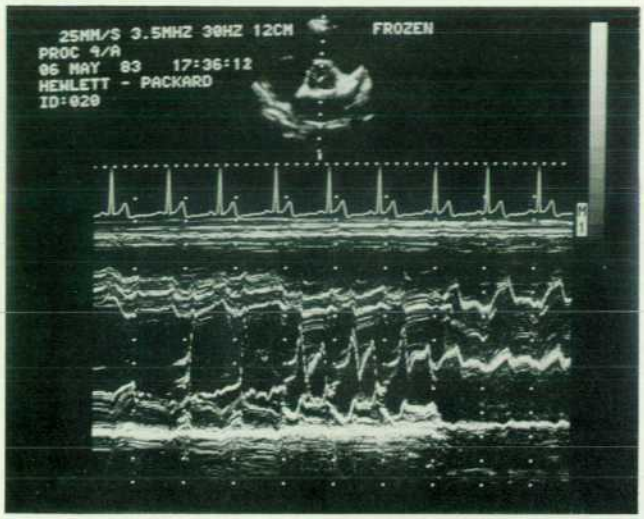
Display System for Ultrasound Images

This subsystem collects digital data from ultrasound scanning and physiological waveforms from other amplifiers and processes them for display in a rectangular raster-scan format.

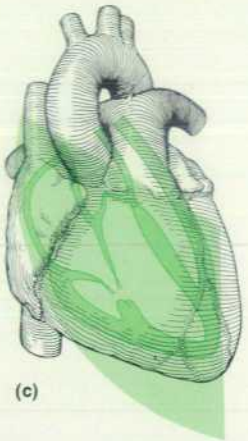
by Raymond G. O'Connell, James R. Mniece, and Alwyn P. D'Sa

THE 77400A DISPLAY SUBSYSTEM (DSS) in the HP 77020A Ultrasound Imaging System formats all image and system data for presentation on the display screen in real time under the supervisory control of the 77020A's controller, the 77900A (see article on page 3). In this imaging subsystem the data is input and output in a variety of ways. The controller sends ASCII command messages to the DSS via an internal bus based on the HP-IB (IEEE 488) to set the mode of operation and select a particular screen format.

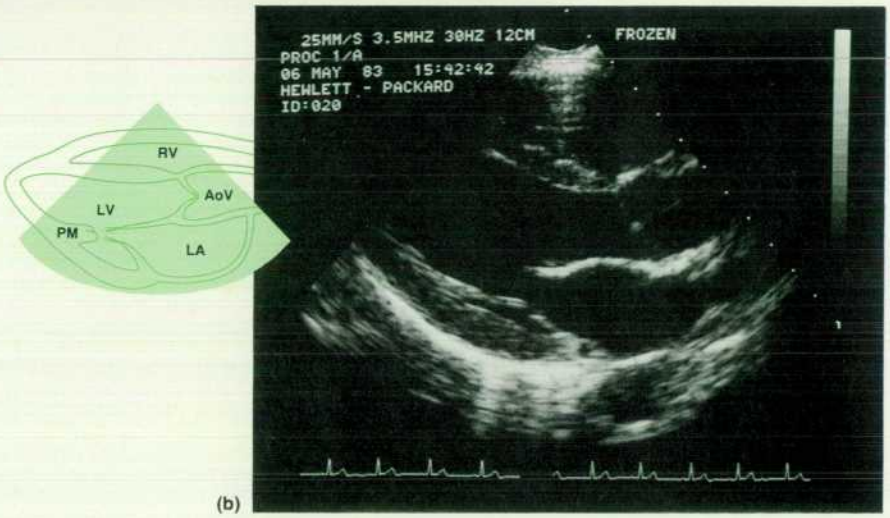
The digitized two-dimensional sector image data in polar coordinates is sent by the 77020A's scanner, the 77200A (see article on page 13), to the DSS via a high-speed data bus. This data is mapped into a rectangular image memory



(a)



(c)



(b)

Fig. 1. *(a) M-mode display. The location of the M-mode line in the sector image is indicated by a software-generated overlay (the vertical line of dots). (b) Full sector-scan display. Physiological waveforms can also be shown at the bottom of the display (heartbeat waveform shown here). The scan shows a cross section of the heart located as shown by the color overlay in (c).*

using the R-Theta scan conversion scheme described by Leavitt, Hunt, and Larsen.[1] Digitized M-mode data is also sent over the high-speed bus to the display subsystem and is mapped directly into the image memory in rectangular format. If the patient being examined by the 77020A is also connected to a monitoring device such as an electrocardiograph (ECG) or blood pressure amplifier, this physiological data can be sent by the 77020A's controller to the DSS over the HP-IB to be displayed with the image as analog waveforms (Fig. 1). In addition, the controller sends data to the DSS to direct placement of display cursors and calibration markers to denote the location of M-mode lines and to aid quantitative analysis procedures.

The 77020A can also be used to review previously recorded data with some measurement and computational capability. To do this, the image memory is also used for a still-frame function. Hence, video data can be stored in the 77020A's video cassette recorder (VCR) and later played back and digitized by the DSS for input into the image memory for analysis.

The display subsystem supplies four composite video outputs. Three of these outputs are standard interlaced RS-170 video in either 525-line NTSC or 625-line CCIR formats. The fourth output, which feeds the 77020A's primary display, is noninterlaced video. In this case the horizontal line rate is twice that of standard interlaced video. Thus, a frame of data is displayed in half the time required for a standard video frame. This faster raster refresh rate reduces flicker on the 77020A's display screen.

A final data output path from the DSS is a screen dump which transfers the contents of the display over the system HP-IB to the controller to be formatted for printout on the 77020A's stripchart recorder.

Design Goals

Several performance goals were set that had a significant effect on the design and architecture of the display subsystem. The first of these goals was the requirement for a flicker-free display to show M-mode data. This data normally forms many horizontal lines that flicker very strongly, causing operator eye fatigue. To reduce flicker, the display subsystem must supply data from the image memory at a 25-MHz rate and be able to form a noninterlaced display. This required the design of a custom CRT display for the 77020A because noninterlaced monitors in diagonal sizes less than 15 inches were not commercially available and most of the commercially available interlaced

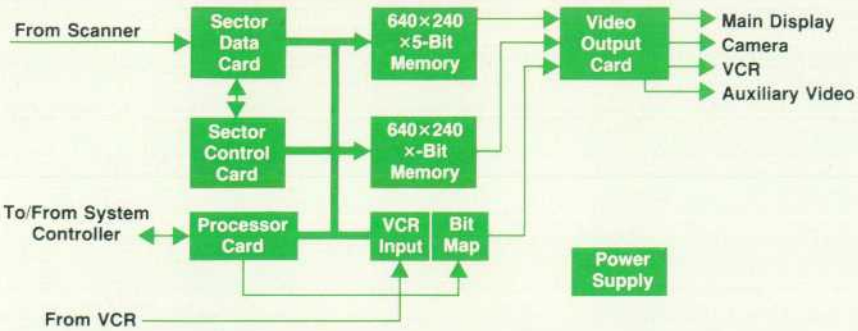


Fig. 2. *Block diagram of the 77400A Display Subsystem.*

monitors required a change in their active-line-to-retrace-time ratio.

Another important goal was to construct a fine-quality picture from the acoustic data. At that time, the state of the art was simply to transfer each acoustic sample directly to the nearest display pixel, and then filter the data to smooth the rough edges in the picture. The R-Theta conversion algorithm eliminates the distortion characteristic of these earlier techniques.[1]

Many of the early ultrasound systems for cardiac studies used an early portable VCR that had many advanced features, including an excellent freeze-frame display function made possible by a four-head design. Unfortunately, at that time in the project, this recorder was being discontinued and the then-new Beta® and VHS® machines did not have acceptable freeze-frame performance. To solve this problem, the 77020A stores the picture in its image memory. The picture is also coded so that the vertical frame placement can be sorted out, allowing the display subsystem to provide an excellent freeze frame from the VCR playback. The result is that the 77020A has the elements of a video time-base corrector with image store.

The importance of M-mode in the design is that it requires a rectangular section of the screen for its display with all pixels filled. To freeze the screen for a sector-scan display, only the data required to reconstruct the raster lines must be stored. But, to freeze an M-mode display, the data for each pixel must be stored, requiring a complete image memory.

In displaying the sector data, it is also important to be able to indicate on the image where the M-mode acoustic lines are recorded. A software-generated graphic overlay is used to display these lines instead of a hardware approach, because it allows measurements on the picture both during the scanning procedure and later when the data is played back (see Fig. 1a).

Another requirement is the display of physiological waveforms such as the ECG trace (see Fig. 1b). The goal is to display as smooth a waveform as possible with the available pixel density. The approach used is derived from a similar technique used in HP's patient monitors.[2]

One of the more important aspects of the display subsystem is its software (see article on page 6). Very heavy communication traffic occurs between the 77900A Controller and the display subsystem. Some of this is related to format changes and screen messages, but the bulk of the traffic is the transmission of physiological waveform data for display as part of the M-mode display, or the transmission of the ECG trace data for the sector-scan display mode. Because these samples can come as often as every 5 ms, a conflict arises when the display subsystem is busy drawing measurement cursors on the screen and a new physiological data sample becomes available. To resolve this conflict, the software has a prioritized structure that allows the controller to specify the priority of each command. Cursors are written at a low priority so that when a new data sample arrives, it can be sent as high priority, causing the cursor drawing to stop long enough to enter the new data before continuing.

Design

Fig. 2 shows a block diagram of the display subsystem. Besides the memory input bus, the processor card has another bus that goes to all of the cards in the subsystem. However, this bus is not shown in Fig. 2 so that the other paths of information flow are more visible. The memory cards in the center of the diagram serve the dual function of storing the image and decoupling the input data from the video output.

Memory System. The memory system is central to the operation of the display subsystem. It can accept data from the VCR at a 12.5-MHz rate, or accept vectors of data at a 5-MHz rate while allowing the processor to write to the screen at a 1.2-MHz rate. Meanwhile, the memory system also outputs two streams of data, each at a 12.5-MHz rate,

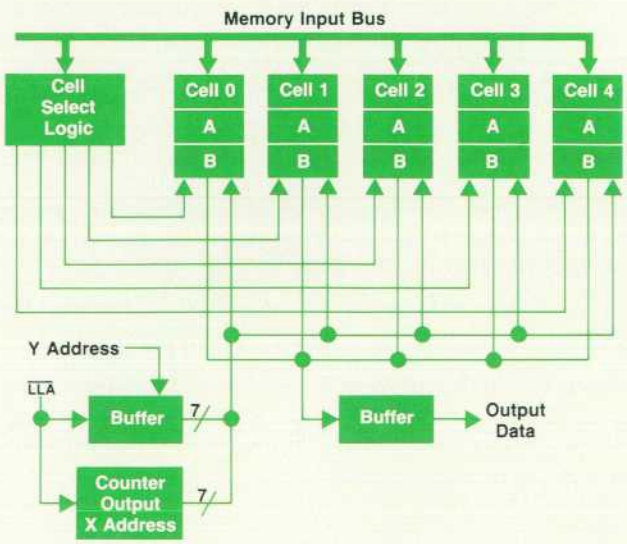


Fig. 3. *Block diagram of memory card for display subsystem.*

to the video output card. The image memory map is 640 pixels wide by 480 pixels high. Each pixel represents 5 bits of picture information (32 gray levels).

The memory system consists of two cards (Fig. 3), one for the even-numbered video lines, the other for the odd-numbered lines. Display systems usually have relatively low input data rates compared to the high rates required to feed the video system. This image memory is an exception. The memory is arranged as 128 five-pixel groups per line. To have a 12.5-MHz data rate from each card, ten separate RAM cells are read every 800 ns. Since the 16K dynamic RAMs used in the memory have a cycle time of 400 ns, this leaves 400 ns to write to the memory chips.

For writing or reading a horizontal (raster) line of data, this can be achieved. But when drawing random vectors, the data rate is limited, because of the possibility of having to rewrite to the same RAM before the 800-ns period is over. Because of the sector and M-mode display requirements, it is important that vertical vectors be written at a rapid rate. To solve this problem, the RAMs are organized in a "quilted" fashion so that vertical vectors pass through four different RAMs before repeating an access to the same RAM. This results in a worst-case vector data rate of 5 MHz.

To allow for a dual-port system, each memory cell, a group of five RAMs which stores the values for 16K pixels of the screen, is isolated with rotating buffers (Fig. 4). These buffers rotate quickly every 800 ns. Since the vector constraints ensure that no one memory cell is written more often than every 800 ns, the operation of these buffers is transparent to the user. The rotation also allows the memory timing to be arranged for optimizing the circuits. The rotating buffers allow the memory chips to go through their normal cycle without affecting the parallel-to-serial translation of data into serial groups of 5-bit words at the output of the card. Note that the address is multiplexed as well as the data. The result is many support circuits for each group of RAMs. To reduce the number of chips, the design takes advantage of the latching nature of dynamic RAMs. Since the data and address need only be applied during

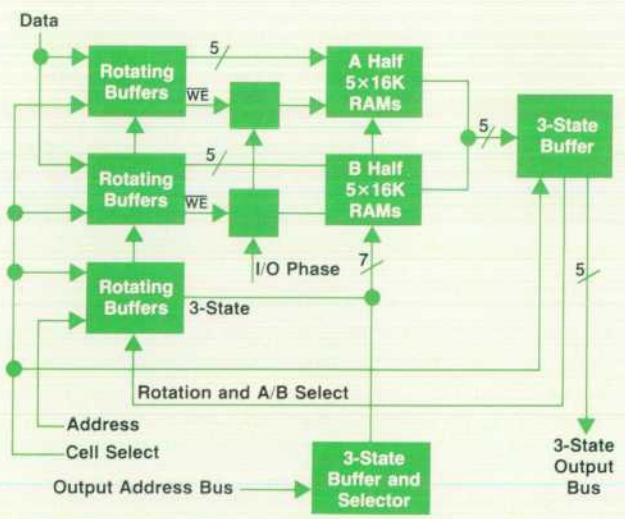


Fig. 4. *Block diagram of one of the five memory cells on the memory card.*

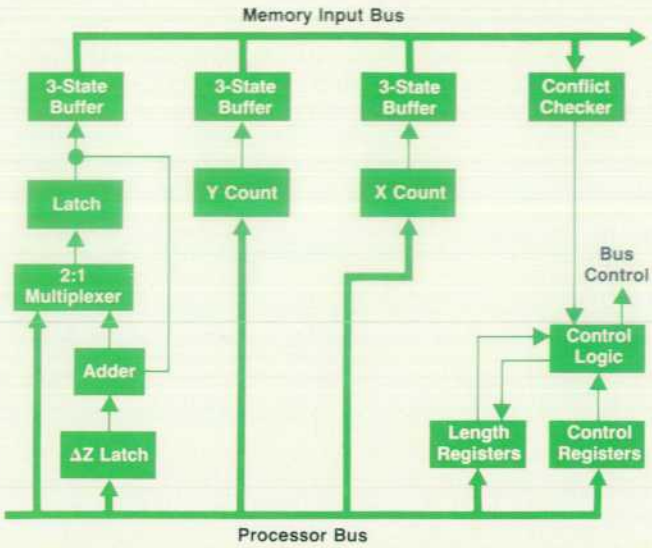


Fig. 5. *Block diagram for the interface between the processor bus and the memory input bus.*

part of the first 200 ns of a 400-ns cycle, the cells are grouped in pairs like the A and B cells shown in Fig. 3. There are five memory cells on each of the two memory cards. Every 200 ns, a new memory access is started. A typical sequence is to write A, write B, read A, read B. During each 200-ns period, the address bus to the chips is further multiplexed into row address and column address. Thus during each 800-ns period, the address bus within the cell has eight different 7-bit words.

The $\overline{\text{LLA}}$ signal line shown in Fig. 3 comes from the processor board, which holds the timing circuitry common to the memory boards. To start each line, the timing circuits send $\overline{\text{LLA}}$ to initialize the X output address counters and load the new Y address from the video output card. The common timing circuitry is also responsible for operation of the memory input bus. This is a 12.5-MHz time-sliced bus. It works in two distinct modes: VCR mode and image mode. In VCR mode the bus is operated by the VCR card which is alone on the bus. In image mode the two sector cards share access with the processor.

Fig. 5 is a block diagram of the processor interface. The processor interface is a crude vector system that serves two purposes: it draws vertical lines for the purpose of having smooth physiological waveforms on the screen, and it performs a fast screen erase, which avoids adding more circuitry on the memory cards. In operation, the processor first loads the number of pixels in the vector (the length), and then loads the starting X and Y addresses and their direction (±X,±Y). Finally, it loads the intensity Z and the delta intensity, which starts the process. Every 800 ns, this interface looks for a bus conflict. If there is none, it changes Z, X, and Y and the new data point is written to the image memory.

The display subsystem also contains a bit-map memory which allows the system to write cursors and measurement data on top of data moving in the image memory whether it is real-time image data or data played back from the VCR. This memory is not quilted and only the processor accesses

Video Recording of Ultrasound Images

An essential feature in a real-time ultrasound imaging system is the capability to store dynamic images for later viewing. The 77020A System produces complete scans at rates from 15 to 60 frames per second. Raw scanner data can be stored in digital format on a high-speed disc system, but for most users, videotape is more practical. One videotape cassette can store an hour or more of ultrasound images inexpensively.

The 77020A is compatible with either Beta® or VHS® video cassette recorders (VCRs). Although originally developed for home use, Beta and VHS recorders are now available in industrial versions that are compact, consume little power, and have excellent review capabilities—variable-speed playback in both forward and reverse, and improved freeze-frame quality.

In the 77020A System, the recorder has been integrated into the instrument. Some of the features are:

- Controlling and sensing operating states of the VCR from the ultrasound system
- Individual frame numbering
- Automatic tape positioning
- Digitally freezing a recorded frame
- Stabilizing the images in slow-motion and search modes.

The 77020A outputs normal interlaced video to the VCR simultaneously with the noninterlaced video to the system display. The 77020A can be purchased with either a 30-Hz, 525-line recorder or a 25-Hz, 625-line recorder. The 77400A Display Subsystem (DSS) is configured accordingly.

One problem with recording digitally generated video is the fast rise time (<20 ns) of the video digital-to-analog converter (DAC). This produces crisp images on TV monitors and multiformat cameras, but some VCRs are not designed to work with these fast rise times. The problem is the limited bandwidth that can be recorded at the relatively low writing speeds in these VCRs. During playback horizontal black streaks or "tails" appear to the right of white spots in the image.

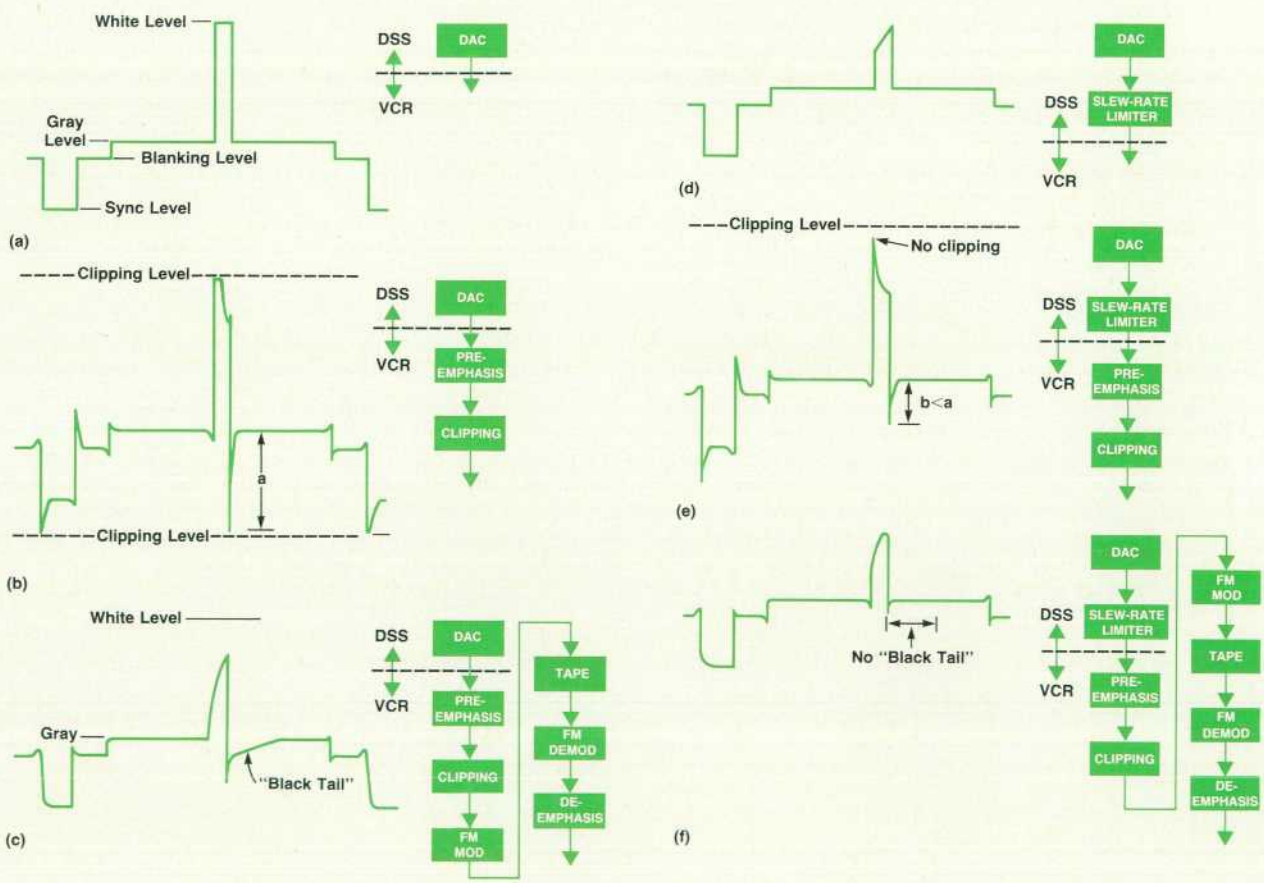


Fig. 1. *Video signal processing. (a) Original signal output from the display subsystem's digital-to-analog converter to the VCR. (b) Signal in (a) after preemphasis and clipping in the VCR. (c) Signal after playback. (d) Signal in (a) processed by a slew-rate limiter before going to the VCR. (e) Signal in (d) after preemphasis and clipping in the VCR. (f) Slew-rate-limited signal after playback.*

Fig. 1 shows one line from the video signal for a white object on a gray background at various points in the system. The recording preemphasis can be thought of as adding the first derivative to the signal. This produces large overshoots at step transitions (Fig. 1b). Because of the limited bandwidth that can be recorded, the signal is tightly clipped before arriving at the input to the FM modulator. The leading edge of the white pulse is clipped but the trailing edge is not. During playback this asymmetry leaves a dc residue after the white pulse. This produces the horizontal black tails in the image mentioned earlier (Fig. 1c).

To prevent this problem, the display subsystem output to the VCR is slew-rate limited above a threshold as shown in Fig. 1d (i.e., the slope cannot exceed a set value). The maximum slope is chosen such that the overshoot produced in preemphasis is not large enough to be clipped (see Fig. 1e). Thus the undershoot is minimized in playback and no black tails appear (Fig. 1f).

Another problem appears during slow-motion playback; the fields do not appear equally spaced in time. To force the fields into approximate alignment for viewing the video on an ordinary TV monitor, new vertical sync pulses are synthesized in the VCR to offset the interlacing problem. The 77020A must know exactly what line the VCR is playing back. If the synthesized vertical sync pulses are not positioned correctly, the DSS may assign the VCR lines to the wrong lines in memory, or even worse, interpret the even field as odd or vice versa.

To correct this problem, the DSS inserts a white half line in the first line of each field output to the VCR. During playback this line is detected and used to correct the Y counter. This white sync also carries the field information (encoded with phase as in the normal vertical sync).

-James R. Mniece

it during the write cycle. It has two characteristics that it shares with the image memory system. It generates two 12.5-MHz data streams and it acts on Y address information from the video output card in the same manner.

Video Output Card. The output card completes the timing of the memory system. It takes the $\overline{\text{LLA}}$ line from the memory timing circuits on the processor card and counts line numbers and the X positions within the lines. This timing block then generates horizontal and vertical sync for both interlaced and noninterlaced outputs (Fig. 6). These calculations are returned to the memory system as OY (output Y) address lines.

Having this control is central to the operation of the card. Consider the interlaced 525- or 625-line raster system. The total number of lines is odd so that the raster lines can be interlaced without interrupting the continuous rate of the horizontal sweep (see Fig. 7). This poses a problem if one wants to create a noninterlaced output that is exactly twice the speed of the interlaced one. Essentially, the line addresses for interlaced scanning are either a half line ahead or a half line behind the desired line addresses for noninterlaced scanning. To solve this problem and keep the size of the buses on the motherboard low, a line called OYP1 (output Y address plus one) is used. When activated, this line adds a one to the address of the even lines. The interlaced output is not affected, because at this time it is using odd-line data.

The output card performs a significant amount of data manipulation. The postprocessing RAMs act like data translation RAMs (Fig. 6). They are loaded by the processor under command of the 77900A Controller. Any pixel value in image memory can be remapped into any other pixel. This capability allows the system to gamma-correct data played back from the VCR. Another aspect of the postprocessing is the character output. Intensity level Z = 31 in the image memory is reserved for characters on the screen. This allows the characters to remain the same brightness regardless of the setting of the postprocessing RAMs. When this level is detected, a special character brightness is inserted.

After postprocessing, the data goes through the 625-line format converter. When using this format, the data formatter sums two adjacent lines every five lines to form a sixth line, creating a five-to-six conversion. This approach requires less image memory.

The last stage in the display process speeds the 12.5-MHz data up to 25 MHz so that it is compatible with the 60-frame-per-second display. While one interlaced line is output to the VCR, the two data streams feed half of a four-line buffer. The other half of the buffer outputs the previous two lines at twice the input speed. Essentially, all timing for the 77020A's display is twice that for an interlaced display.

VCR Card

To digitize the analog signal from the VCR and return the samples to the frame store requires a number of functions in the playback circuitry (Fig. 8). They include:

- AGC and dc restoration
- Analog-to-digital conversion using a sampling clock aligned with the phase of the VCR signal
- Time-base shifting to transfer video samples from sample clock to system clock
- Horizontal sync detection and proper X address generation for input to the image memory

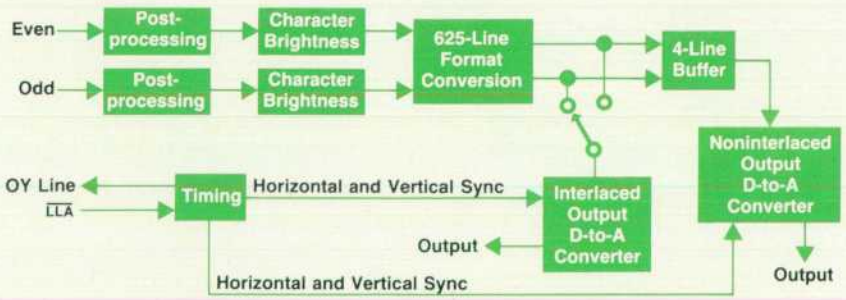


Fig. 6. *Block diagram of video output card for display subsystem.*

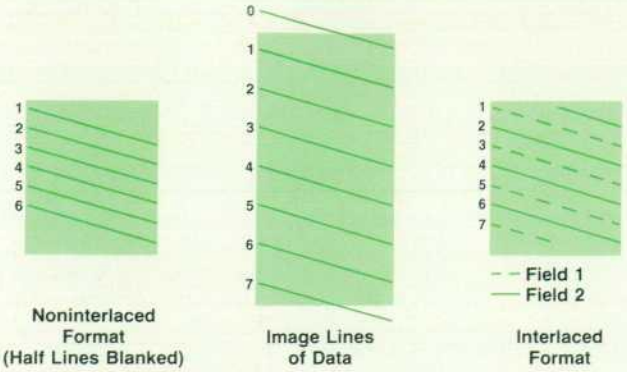


Fig. 7. *Comparison of interlaced and noninterlaced formats. Shaded areas represent the limits of the display.*

- Vertical sync detection and proper Y address generation for input to the image memory (both 30 and 25 Hz).

The signal from the VCR is digitized by a flash analog-to-digital converter (ADC) clocked at 12.5 MHz. The line period of the VCR signal is very close to the system line period and quite stable (the standard deviation of the line-to-line start interval is about 10 ns). Yet the phase of the video will vary from line to line relative to the system clock. To ensure that the ADC samples are taken at the same position in every line, a special sampling clock is used. This clock is the same frequency as the system clock (12.5 MHz) but it is aligned in phase with the horizontal sync (and thus the image signal) at the beginning of each line.

The sampling clock is generated by multiplying the system clock up to 100 MHz and then using the 100-MHz signal to clock a divide-by-eight counter (see Fig. 8). The divide-by-eight counter is cleared by the horizontal sync pulse and thus the phase of the 12.5-MHz output of the counter is determined to within 45° by the trailing edge of the horizontal sync pulse (see Fig. 9).

The digitized samples from the ADC must be written into the image memory. To do this, they must be aligned with the system clock. But if a sample transfer from a latch clocked with the sample clock directly to a latch clocked with the system clock is attempted, the process will not necessarily meet setup times on the receiving latch. For example, if the sample clock is only 45° ahead of the system clock, there will be less than 10 ns to transfer the data. With clock skew problems this would be unreliable.

To circumvent this problem, two latches are used to store alternate samples. One latch stores sample 0 for clock periods 0 and 1 and the other latch stores sample 1 for periods 1 and 2 (see Fig. 8). A multiplexer alternately selects the outputs of the sample clock latches to feed the system clock latch. The multiplexer is switched at times such that the samples are available at least one half clock cycle (40 ns) before they are clocked into the final latch and they remain available at least one half cycle after being clocked into the final latch.

Horizontal sync detection is done in a conventional manner and the detected pulse is used to synchronize the X counter.

Vertical sync detection and Y address generation are major functions of the display subsystem's VCR input circuitry. Conventional vertical sync detection is used and the detected pulse provides for coarse synchronization of the Y counter (line counter). The white-level sync comes along at the top of the image (about 20 lines after vertical sync) and clears the line counter, providing precise vertical positioning. The white-level sync is also used to correct the field bit. For playback of 25-Hz, 625-line data to the 77020A's image memory, the VCR input circuitry must undo the five-to-six-line interpolation described earlier. This is done by simply deleting the interpolated line. A modulo-6 counter is incremented on every vertical sync and every sixth line it causes the Y counter to be halted and the digitized signal is ignored.

High-Speed Search Playback

Some VCRs are capable of playback at higher speeds in either forward or reverse. The signal becomes very degraded with complete sync dropouts and time compression or expansion. In turn, the image produced on a video monitor when the VCR is in search mode is often severely

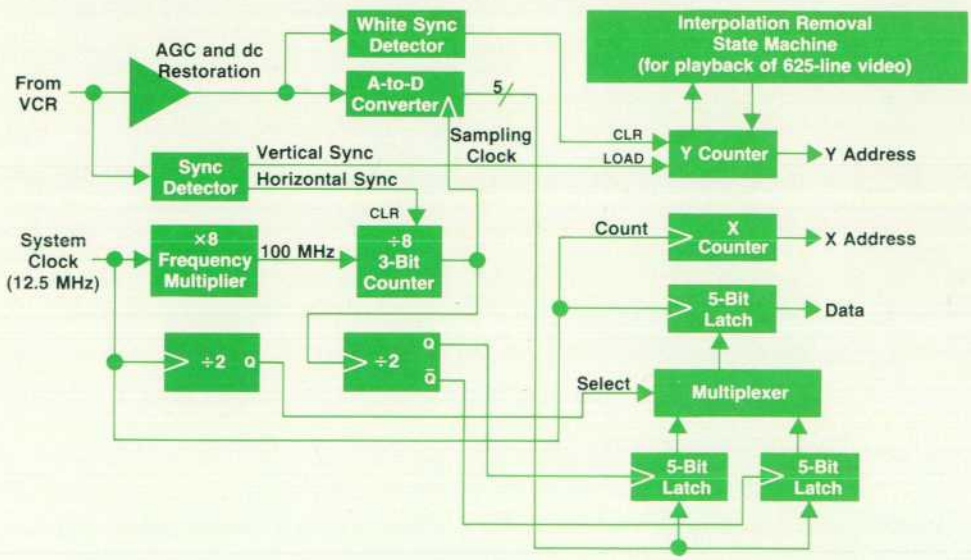


Fig. 8. *Input circuit for processing VCR playback signal.*

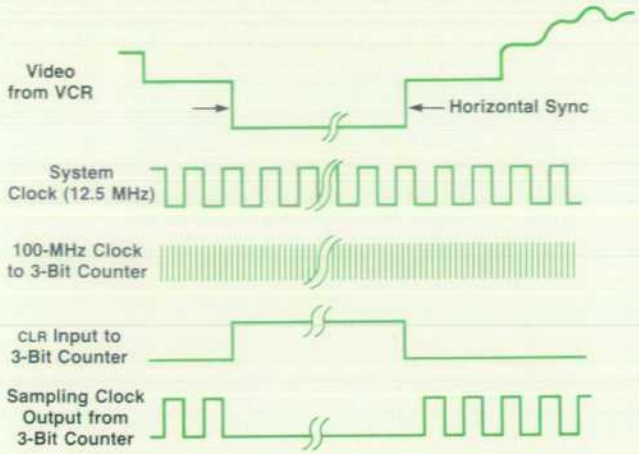


Fig. 9. *Phase alignment of sampling clock with video playback from VCR.*

degraded. There will be tearing of the displayed image when horizontal sync is lost, and if the signal has been compressed or expanded in time, the monitor may lose sync altogether until its horizontal hold control is adjusted.

The VCR input circuitry is more tolerant of these video signal distortions. Because the circuit is directly triggered by the horizontal sync rather than by an AFC circuit as in a TV monitor, it can recover from a loss of horizontal sync instantly with no tearing. The circuit is also more tolerant of variations in horizontal sync period.

Power Supply

The digital subsystem's power supply consists of four linear, low-voltage, regulated power supplies which provide a combined output power of 280W. The available power is 5V up to 40A, 12V up to 5A, −12V up to 1A and −5V up to 1A. The demand for such high power levels stems primarily from the 25-MHz and 12.5-MHz system clock rates which dictate the use of high-speed RAMs and several high-speed Schottky TTL parts in the scan converter design. The overall efficiency of the power supply is typically 40%. The decision to use a conventional linear supply rather than a more efficient switching supply was made in view of some of the notorious shortcomings of switchers in applications that require high currents with low output ripple and EMI (electromagnetic interference). A further constraint in the design was that the display subsystem leakage current had to be limited to less than 15 μA. The choice of a linear power supply eliminated the need for an additional isolation transformer, which would have been required with a switching supply. The power supply meets UL544 specifications, CSA 125 certifications, and the IEC 601-1 and VDE requirements for EMI.

A block diagram of the DSS power supply is illustrated in Fig. 10. The 5V supply is referenced to a stable 2.5V voltage reference source. The high-current capability to the output load is provided by a pair of series-pass Darlington power transistors, Q1 and Q2, which are configured to operate in parallel with grounded collectors. By grounding the collectors, thermal dissipation is improved, limiting junction temperatures to less than 160°C in a 65°C ambient. Hence, each transistor can provide up to 20A.

Regulation is provided by error amplifier U1, which monitors the load voltage and compares it with a preset voltage derived from the precision voltage reference. In addition, current-equalizing amplifier U2 monitors the current in the 5-mΩ sense resistors R1 and R2 in the emitter paths of Q1 and Q2 to ensure equal sharing of load current.

The foldback current-limiting circuit U3 senses the current in sense resistor R1. It forward-biases diode D1 and removes the base drive to Q1 in the event of a short circuit at the load. The regulated output voltage can be set as desired over a range from 4.5V to 5.5V with a single adjustment. The load and line regulation and the output noise

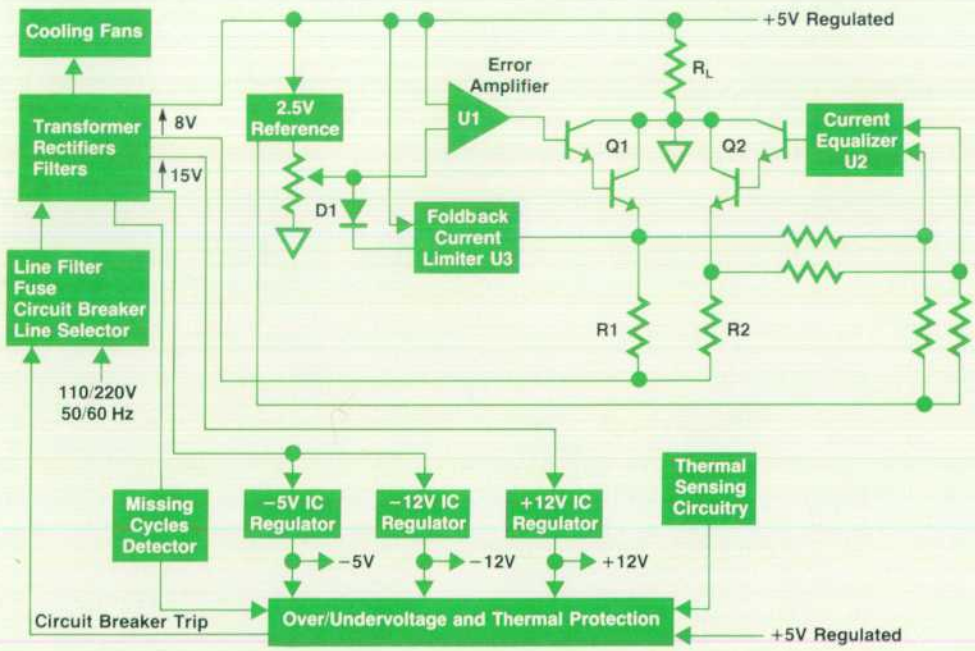


Fig. 10. *Block diagram of power supply for display subsystem.*

are in the millivolt range.

Commercially available monolithic IC voltage regulators are used to control the 12V, −12V and −5V supplies. They have built-in current-limiting and thermal protection circuits. These regulators, the power Darlingtons, and the high-current rectifiers are mounted on an extruded heat sink for power dissipation. Forced-air cooling restrains the internal temperature rise to less than 6°C.

The outputs of the individual power supplies are monitored for over/undervoltage conditions to protect both the supply and the loads connected to it. A high-temperature shutdown circuit monitors the power dissipation in the heat sink (nominally 150W). If any of the monitored parameters exceeds its specified limit, then the protection circuit disconnects the display subsystem from the ac power mains by tripping the circuit breaker. The missing-cycles detector monitors the ac power line voltage and provides some delay protection to the supply in the event of a momentary line fault by inhibiting the protection circuits from immediately tripping the circuit breaker. Additional protection against line transients and common-mode noise is provided by incorporating a Faraday shield in the power transformer design.

A final important consideration in the power supply design is powering-up the supplies in a defined sequence to ensure safe and reliable operation of the NMOS memory devices in the scan converter.

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Authors

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John N. Dukes

John Dukes received degrees from Oberlin College and Stanford University and for the last 20 years has been designing circuits at HP for "all sorts of useful gadgets," including microwave counters, laser interferometers, spectrophotometers, navigation receivers and, more recently, for medical instruments, the latter in the Applied Physics Laboratory of HP Laboratories. When not designing he plays baritone sax in a jazz big band, takes 3-D photographs, plays catch with an aspiring pitcher, and claims to be an ever more aggressive bicycle rider.

Richard H. Jundanian

Born in Worcester, Massachusetts, Rich Jundanian attended nearby Worcester Polytechnic Institute, earning a BSEE degree in 1980 and an MSEE degree in 1981. After working on cardiac monitor design for a university medical center, he joined HP as an R&D engineer and contributed to the 77900A Controller development. Rich is married and lives in Methuen, Massachusetts. Outside of work, he works with church youth groups and spends time restoring his car, a 1966 Mustang.

Janet R. Accettura

With HP since 1979, Jan Accettura is an R&D project engineer at HP's Andover Division. She contributed to the hardware design of the controller and primary display for the 77020A Ultrasound Imaging System. She attended Cornell University and earned a BSEE degree in 1979. Born in La Grange Park, Illinois, she now lives in Andover, Massachusetts. In her free time she enjoys hiking, sewing, outdoor sports, visiting her family in Wyckoff, New Jersey, and playing ultimate Frisbee (she was a member of the 1981 national championship team).

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William A. Koppes

A graduate of the University of Washington (BSEE, 1976) and the University of California at Berkeley (MSEE, 1978), Bill Koppes' work experience before joining HP in 1978 included development of an ink-jet printer and a positron emission tomography system. At HP he worked on the 77020A System software and currently manages a computer systems group. Born in Morristown, New Jersey, he is married and lives in Westford, Massachusetts. Outside of work, he enjoys scuba diving, playing racquetball, running, and music.

Joseph M. Luszcz

Educated in electrical engineering and computer science at Worcester Polytechnic Institute (BSEE, 1973) and Northeastern University (MSEE, 1983), Joe Luszcz is a project manager for ultrasound system software at HP's Andover Division. With HP since 1973, he worked on software for the 77020A and an ECG analysis system before assuming his current position. Joe is coauthor of a paper on medical analysis software and was born in Ware, Massachusetts. He has a wide variety of interests; the most important include his family, scuba diving, running, softball, and vegetable gardening. He is married, has three sons, and lives in Hudson, New Hampshire.

David C. Hempstead

Dave Hempstead joined HP in 1979 after receiving a BSEE degree from Rensselaer Polytechnic Institute. He worked on the software for the display subsystem and the resident test executive of the 77020A Ultrasound System and now is developing software for future products. Born in Morristown, New Jersey, he now lives in Methuen, Massachusetts, where he coaches basketball. He is married and is interested in home computers, video game development (he developed a video game for the 77020A which was available as an option), and home construction (he built the second story on his home).

Robert J. Kunz

Bob Kunz began work at HP in 1976 as part of a work-study program while he was studying electrical engineering at Rensselaer Polytechnic Institute. He received a BS degree in 1978 and an ME degree in 1979. He worked on the 5600C ECG Management System and the 47400A Off-Line Analysis System for the 77020A. Bob has many outside responsibilities, including teaching data base management systems at the University of Lowell and managing the HP engineering softball team. He is also president of the HP Ski Club and chairman of the local HP company picnic. He was born in Flushing, New York, is married, enjoys scuba diving, and lives in Derry, New Hampshire.

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James T. Fearnside

Jim Fearnside started work at HP in 1967 after receiving an MSEE degree from Stanford University. He also holds a BSEE degree awarded in 1966 by Cornell University. His work has resulted in three patents, one on a novel ECG electrode and two on ultrasound transducers. He currently is a section manager for imaging technology. Born in Boston, Massachusetts, he now lives in Lexington, Massachusetts with his wife and two children. Jim works with the local Boy Scout group and serves on the council of his church. His interests include investments, skiing, hiking, and sailing.

Sydney M. Karp

Born in New York City, Sydney Karp studied electrical engineering at Rensselaer Polytechnic Institute, receiving a BSEE degree in 1976. He then worked on radar signal processors before joining HP in 1979. He designed the master/slave transmitter cards and wrote the operating and self-test software for the 77200A Scanner. He lives in Somerville, Massachusetts and when not caring for his houseful of plants, enjoys photography, playing ice hockey, and attending Boston Bruins games.

Ronald D. Gatzke

With HP since 1969, Ron Gatzke has worked on ECG front-end design (78330, 78331, and 78620), and the 77200A Scanner. He currently is a project manager for ultrasound scanners. Ron is a contributor to a book about bioelectrode technology and coauthor of an earlier HP Journal article about the 78333A ECG Monitor. His work has resulted in three patents related to defibrillator ECG design. Born in Cleveland, Ohio, he studied electrical engineering at Case Western Reserve University (BS, 1966) and Northeastern University (MSEE, 1972). Ron is married, has one child, and lives in Lexington, Massachusetts. His interests include bicycling, running, and music—he plays the cello, piano, and harpsichord (which he built as a copy of a 1770 French instrument).

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Robert N. McKnight

With HP since 1972, Bob McKnight worked on disc memory products at the Boise Division before moving to the Andover Division to work on the 77200A Scanner. He is the author of a paper on disc drive servo systems and was educated at Carnegie-Mellon University (BSEE, 1972) and Stanford University (MSEE, 1979). Born in St. Marys, Pennsylvania, he is single and lives in Andover, Massachusetts. When not working, he enjoys cross-country skiing, racquetball, running, music, cooking, good restaurants, wine tasting, and going to the beach.

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Alwyn P. D'Sa

Alwyn D'Sa received his education in electrical engineering at the Indian Institute of Technology at Bombay (BTech, 1973), the University of Calgary (MSEE, 1975), and the Polytechnic Institute of New York (PhD, 1980). He began work at HP in early 1979 and contributed to the hardware and software design of the 77020A Ultrasound System. Currently, he is working on image analysis techniques. Alwyn is coauthor of a paper on digital temperature transducers and is a member of Sigma Xi. He is married and lives in Cambridge, Massachusetts. His interests include speech recognition, robotics (he is a member of the MIT Robotics Club), soccer, and sailing on the Charles River.

James R. Mniece

Born in Dearborn, Michigan, Jim Mniece was educated at the Massachusetts Institute of Technology, receiving a BSEE degree in 1971 and an MSEE degree in 1974. After serving as a Peace Corps volunteer in Jamaica and then working as a clinical engineer for Massachusetts General Hospital, Jim joined HP in 1979. He designed the VCR input circuitry for the 77020A and now works on scanner enhancements. He is married, lives in Waltham, Massachusetts, and is a member of the local nuclear freeze committee. He plays classical and jazz piano and enjoys camping.

Raymond G. O'Connell, Jr.

With HP since 1966, Ray O'Connell has contributed to the design of the 7822A Arrythmia Monitor, 78301 Control Station Display, 47201 Oximeter, and 7835A Delay. He also was project manager for the DSS, display, and VCR portions of the 77020A Ultrasound System. He currently is a project manager working on a new ultrasound processor. Ray received a BSEE degree from Worcester Polytechnic Institute in 1966 and an MBA degree from Northeastern University in 1976. Outside of work he enjoys swimming, sailing, and writing personal computer games. He was born in Annapolis, Maryland, now lives in Andover, Massachusetts, is married, and has four children.

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Bruce L. Ryder

Bruce Ryder joined HP in 1978 and was a member of the team that developed the drawing and external coating processes for fused silica capillary columns. Since then, he has continued to work on aspects of that technology and is now project leader for a new series of fused silica columns. A member of the American Physical Society and the IEEE, he received his BS degree in physics from Elizabethtown College in 1975 and his MSEE degree from Syracuse University in 1978. Before coming to HP, he did hardware design for respiratory therapy equipment and software design for ECG analysis. Born and raised in Pennsylvania, Bruce still lives there, in Strasburg, where he serves on the town's library and housing committees. He is married, has two children, and is interested in genealogy, photography, toy trains, and home computers.

Thomas J. Stark

Tom Stark was born in Gary, Indiana. He received his BS degree in chemistry from the University of New Mexico in 1972 and his PhD in chemistry from the University of California at Berkeley in 1977. He joined HP in 1979 and has done R&D for fused silica columns and development and testing for the 5890A GC. Before joining HP, he served four years in the U.S. Army, attaining the rank of Captain, and did process research in electronics manufacturing. A member of the American Chemical Society and the National Wildlife Federation, he has coauthored four papers on gas chromatography and one on organometallic reaction mechanisms. Tom is a runner with one marathon to his credit. He lives in a hybrid solar-and-wood-heated home in Landenberg, Pennsylvania and enjoys organic gardening and carpentry. He's married and has a son.

Paul A. Larson

With HP since 1979, Paul Larson has been responsible for product and process development for Ultra Performance and Special Performance fused silica columns. A native of Marquette, Michigan, he received his BS and MS degrees in chemistry from Michigan Technological University in 1970 and 1971, and his PhD in analytical chemistry from the University of Colorado in 1976. Before joining HP, he did postdoctoral research on ion-selective devices at the University of Wisconsin (Madison) for three years. He has published articles on gas and liquid chromatography, ion-selective FETs, and kinetics, and is a member of the American Chemical Society. A resident of Newark, Delaware, Paul is married, has two daughters, and is active in his church.

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Fused Silica Capillary Columns for Gas Chromatography

Here's how collaborative research between HP's chemical analysis and optoelectronics laboratories created a vastly superior GC column.

by Paul A. Larson, Bruce L. Ryder, and Thomas J. Stark

REMARKABLE THINGS can happen when unrelated technologies intersect. Investigation into quartz fiber optics by Hewlett-Packard Laboratories and chemical analysis research at HP's Avondale, Pennsylvania Division led to the development of a fused silica capillary column used in gas chromatography. Compared to the previously available packed or capillary columns made of either stainless steel or glass, fused silica capillary columns have vastly improved column-to-column reproducibility, resolution, and retention characteristics. Other benefits include the elimination of spontaneous column breakage, a highly inert inner-column surface, a wide dynamic temperature range, and rinsability.

The first columns made by HP Laboratories using fiber optics techniques were made of fused quartz. Later, fused silica was found to be superior. Since 1979, when the first fused silica capillary columns were introduced by HP, the technology has been refined and the list of available columns has been expanded.

This article summarizes the development of this technology, going back to its beginnings for a look at the early promising results, and then describing the present state of the art and the trends that may determine the future.

The Activity Problem

Gas chromatography (GC) separates a mixture of chemicals into its individual components. A stream of inert gas carries a vaporized sample through a column containing a nonvolatile chemical called the stationary phase. Those components of the sample with little or no affinity for the stationary phase remain in the gaseous state and pass through the column quickly. Other components may interact with the stationary phase and be temporarily removed from the gas stream; their passage through the column will be retarded by various amounts depending on their affinities. If the affinity is too great, some components may never emerge from the column. Thus the time from sample injection to component appearance—the retention time—is characteristic of the component identity, assuming that the column, gas velocity, temperature, and a few other parameters are held constant.[1]

The analytical chemist wants the only interactions within the column to be those between the sample components and the stationary phase. The column tubing should play no part, other than to support the stationary phase and to direct the gas stream from the point of injection to the point of detection. But in the real world, column tubing is far from inert. Interactions with sample components lead to band-spreading of the components and loss of resolution, irreversible adsorption of components, catalytic decomposition of some materials, and other interferences with the analysis process.

The first capillary columns were made of stainless-steel hypodermic needle stock. These were satisfactory for nonactive components such as hydrocarbons, but for little else. Other metals were not much better. Glass capillary tubing, made by drawing standard laboratory tubing down to capillary dimensions, proved to be a much lower-activity material. However, inert as glass is (relative to the metals), it is still too active for many compounds. The culprit seems to be metal ions from the glass ingredients which can form active sites at the glass surface. An enormous amount of research has gone into etching, leaching, coating, reacting, and other techniques intended to remove, conceal, or otherwise deactivate these sites. Most of the work has been done on soda-lime or borosilicate glasses, since these are the types most commonly found in the laboratory. The results have been, in general, disappointing and difficult to reproduce.

In 1978, HP's Avondale Division began a study of other

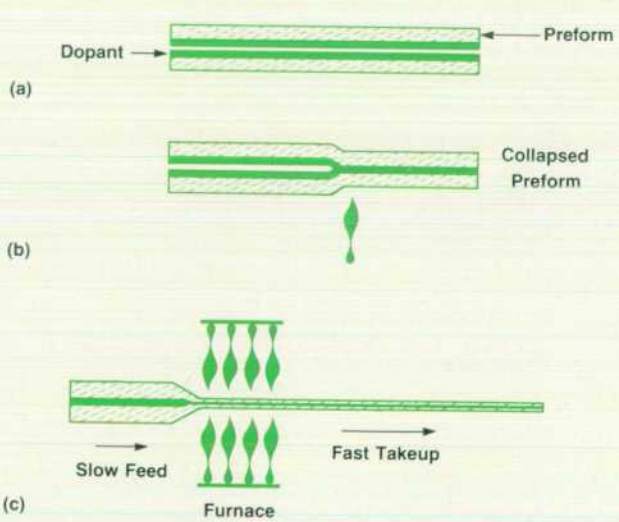

Fig. 1. *Three steps in the production of a refractive index gradient along the radius of an optical fiber. For gas chromatography columns, the first two operations are omitted.*

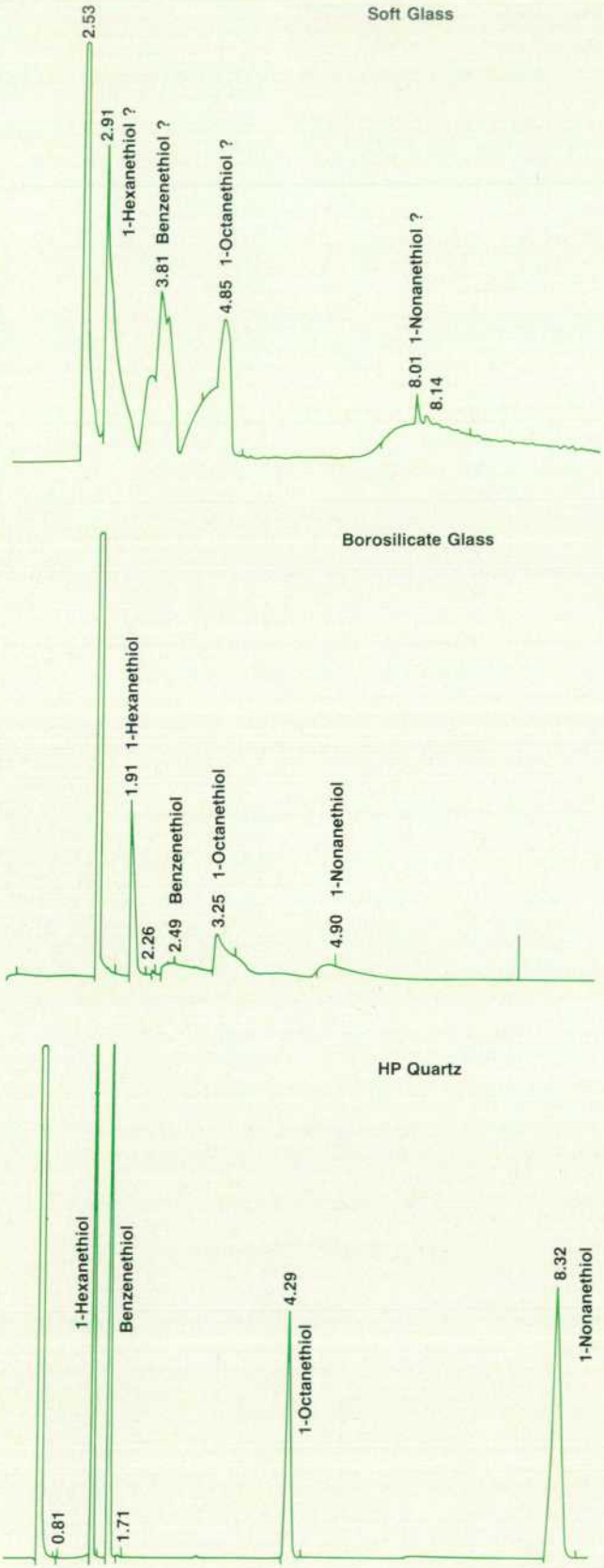

Fig. 2. *Reproductions of original chromatograms comparing the first fused quartz columns with the best previously available columns in a mercaptan analysis.*

types of glass to see if any of these offered advantages for GC work. Since the equipment then used to draw glass capillaries was quite unsophisticated, three engineers visited HP Laboratories to examine their quartz fiber optics drawing equipment.

One of the standard ways to produce a refractive-index gradient along the radius of an optical fiber is shown in Fig. 1. A hollow tube of the material (the preform) is coated on the inside with a dopant of some sort. The preform is heated to collapse the tube into a solid bar; during this stage the dopant diffuses into the material. Finally, the collapsed preform is drawn into a fiber of the required diameter.

The Avondale engineers reasoned that if the doping and collapsing operations could be omitted, this equipment should be usable for making capillary tubing. Did the HP Labs people think this possible? They did. Would they make some tubing for Avondale to study? They would try. The first batch of fused quartz capillary tubing arrived in Avondale one month later.

The First Fused Quartz Column

Since silicone rubbers are the workhorses of gas chromatography, one of them was selected as the stationary phase for the first column prepared from the HP Labs fused quartz tubing. The next four days were probably the noisiest period in the history of Avondale R&D, as the remarkable properties of the new tubing became evident. Everyone wanted to try difficult-to-analyze samples, and discussions of results were loud and enthusiastic.

Some idea of the excitement can be gathered from Figs. 2,3, and 4, where the quartz capillary is compared with glass capillaries. These are reproductions of some of the first chromatograms ever made with a fused quartz capillary column (the original chromatograms are no longer in presentable condition). Note that this is the first quartz capillary column ever made at Avondale and that the glass columns were the best available at the time.

Along with their foul odor, mercaptans (Fig. 2) are notorious for being difficult to analyze by gas chromatography. They are highly polar compounds and interact strongly with any active sites on the column. With a soft-glass column, peaks are so deformed that identification is quite uncertain. Borosilicate yields identifiable peaks, but they are not suitable for quantitative work. With the quartz column, the laboratory notebook comments "Peak shape and symmetry is outstanding!! Have never seen such good performance on mercaptans!"

The phenols in Fig. 3 are classified as priority pollutants by the United States Environmental Protection Agency. The sample contains 11 components. Seven of these were found using the borosilicate column; ten appeared with the quartz column.

Antiepileptic drugs are very active, with complex chemical structures and functional groups that interact strongly with column materials. To analyze these drugs, it is standard practice to use an assortment of reagents to block the active functional groups so that they will not interfere with the analysis. Since the quartz column seemed so inactive, it was decided to try to analyze nonblocked drugs. Fig. 4 shows the very good results obtained with nanogram

Fig. 3. *Reproductions of original chromatograms showing how the first fused quartz columns found ten of the eleven phenols in a sample while the glass column found only seven.*

amounts of these drugs, results that had never been achieved with such low levels on capillary columns.

Capillary columns contain very little stationary phase, typically a few hundred micrograms per meter of length. If this material is lost or damaged, the column is useless. Any surface activity on the inside of the tubing can cause the stationary phase to degrade into small volatile compounds. If the column is overheated, this reaction speeds up (each rise of 30°C approximately doubles the reaction rate) and the volatile products are swept out of the column.

Fig. 5 illustrates the very low surface activity of the fused quartz. When the column is heated up, the degradation products from the stationary phase cause a rise in the baseline. This is inevitable, but how much of it can be tolerated? Based on the results of these chromatograms, the maximum operating temperature for this stationary phase is above 300°C for quartz tubing, but less than 280°C if borosilicate tubing is used.

Some Mechanical Matters

Glass columns, after being drawn down to the required diameter, are passed through a heated curved tube. This softens the glass enough so that it can be formed into a coil. The curvature makes it possible to fit the column into the instrument, but it is necessary to straighten the ends of the coil before it can be attached to the rest of the chromatographic system.

Fused quartz has a softening temperature of about 1600°C, compared to 550°C for borosilicate glass. Forming a coil from the fused quartz capillary by bending it is simply not practical. Even if it were, the high softening temperature would make straightening of the ends very difficult.

Some earlier workers had investigated fused quartz, but concluded that it would not make a good column material because it was much too brittle. However, that tubing had relatively thick walls. Its cross section resembled a rather thick bar with a small hole down the center. Since brittleness is proportional to the fourth power of the outside diameter, the GC engineers realized that if the wall thickness could be reduced, it might be feasible to simply wrap the inherently straight tubing around a basket of some sort which would fit inside the GC oven.

Fig. 6 is a cross section of the first batch of fused quartz tubing. Wall thickness is comparable to the inside diameter. The silicone rubber coating on the outside protects the surface from scratches, which would cause stress concentration and rapid failure of the material on flexing. Fig. 7 illustrates the flexibility of the resulting columns.

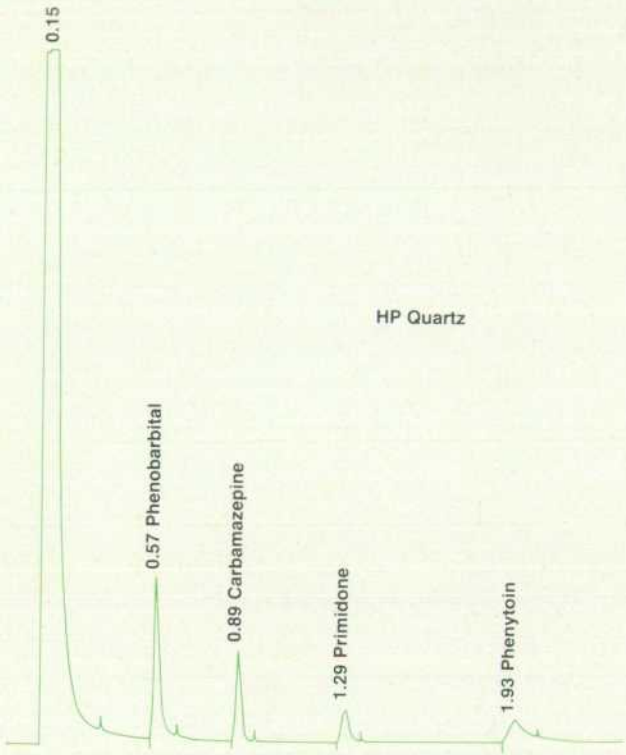

Fig. 4. *Fused quartz column performance on a sample containing antiepileptic drugs. These results had never before been achieved with such low concentrations on capillary columns.*

From Fused Quartz to Fused Silica

The design team experimented with different materials to improve the initial results. One change was from fused quartz to fused silica. Fused quartz is made from the mineral quartz and contains significant amounts of aluminum and iron (about 100 ppm of each). Fused silica, on the other hand, is made from purified silicon tetrachloride. This gas is fed to an oxygen/hydrogen flame where it is hydrolyzed to silicon dioxide and simultaneously fused. The fused silica contains less than 1 ppm of aluminum and iron. Although it is considerably more expensive, it yields tubing with much lower surface activity. The added expense for the raw material of fused silica tubing is largely offset by an increased yield of high-quality capillary tubing.

The silicone rubber initially used to protect the outside column wall from scratches has a temperature limit near 250°C. This is about 100° too low for chromatographic purposes. A number of alternate coatings with higher temperature limits were investigated. A polyimide resin was chosen and a satisfactory coating process developed.

Inside the Column

Fused silica is not totally inert, although it comes rather close. Because there is so little residual activity, it is quite difficult to deactivate that last trace. Extensive research has been done at Avondale and elsewhere to find the most effective approach to this problem. We now use a high-temperature silanization process, in which the residual active sites are converted to inactive methyl ether structures.

A truly inert material has one serious flaw, it is very

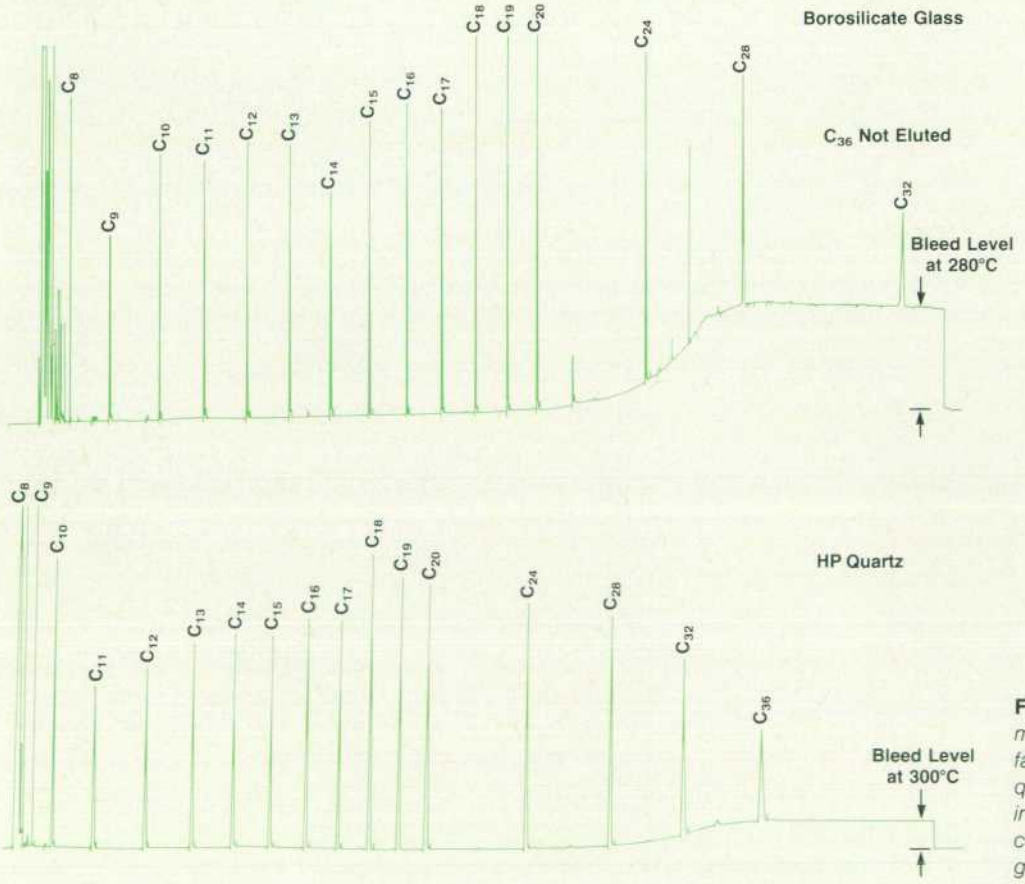

Fig. 5. *Reproductions of chromatograms showing the low surface activity of the first fused quartz columns. Maximum operating temperature was over 300°C compared with less than 280°C for glass.*

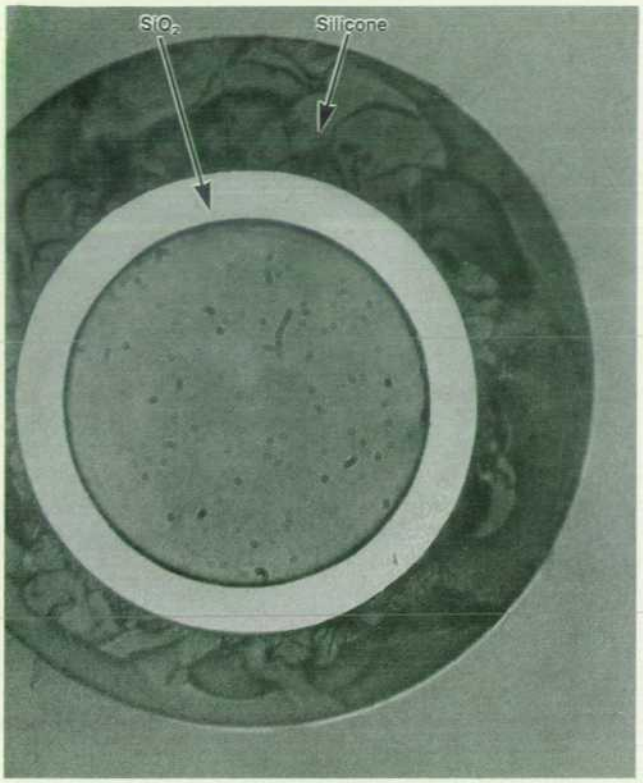

Fig. 6. *Cross section of the first fused quartz columns. Inside diameter is 150 μm. Outside diameter of the quartz tube is 189 μm.*

difficult to wet the surface (have you ever tried to paint Teflon™?). This limits the variety of stationary phases that can be supplied in fused silica columns. Fortunately, the very narrow peaks produced by these columns allow separations to be made that could not be done using the same stationary phase in a packed (broad peaks) column. There is no need for the very wide selection of stationary phases that were developed for packed columns. However, work continues on broadening the selection of phases that can be offered.

As mentioned earlier, there is very little stationary phase inside a capillary column, perhaps a few hundred micrograms per meter. Even a rather moderate overheating of the column can drive off a substantial fraction of this material; some of it is inevitably lost even in very careful operation. To complicate this problem, many samples contain high-boiling-point materials that remain on the column, gradually changing its characteristics. With packed columns, which contain a lot of stationary phase, this spurious material can be baked out. But the process would destroy a capillary column by driving off its small supply of stationary phase.

Two general approaches have been made to this problem. One is to bond the stationary phase to the silica surface chemically. The other, the one used by Avondale, is to convert the stationary phase into a nonvolatile, insoluble material inside the column.

Practically all stationary phases are polymers, often silicones of various types. These very long molecules give the low volatility that any phase must have. However, they are still soluble in appropriate solvents. If cross links are introduced between these long chains of atoms, a three-dimensional structure is formed. This structure is even less volatile than the original material, but more important, it cannot dissolve in anything without breaking some of the cross links.

The HP GC columns use cross-linked stationary phases that escape very slowly when overheated. They can be cleaned thermally and can even be washed with solvents without damaging the columns.

Where We Are Now

Hewlett-Packard produces several lines of fused silica capillary columns. The High Performance columns have approximately 200-micrometer inside diameters and come in various lengths. The stationary phases are cross-linked to reduce volatility and permit solvent washing when

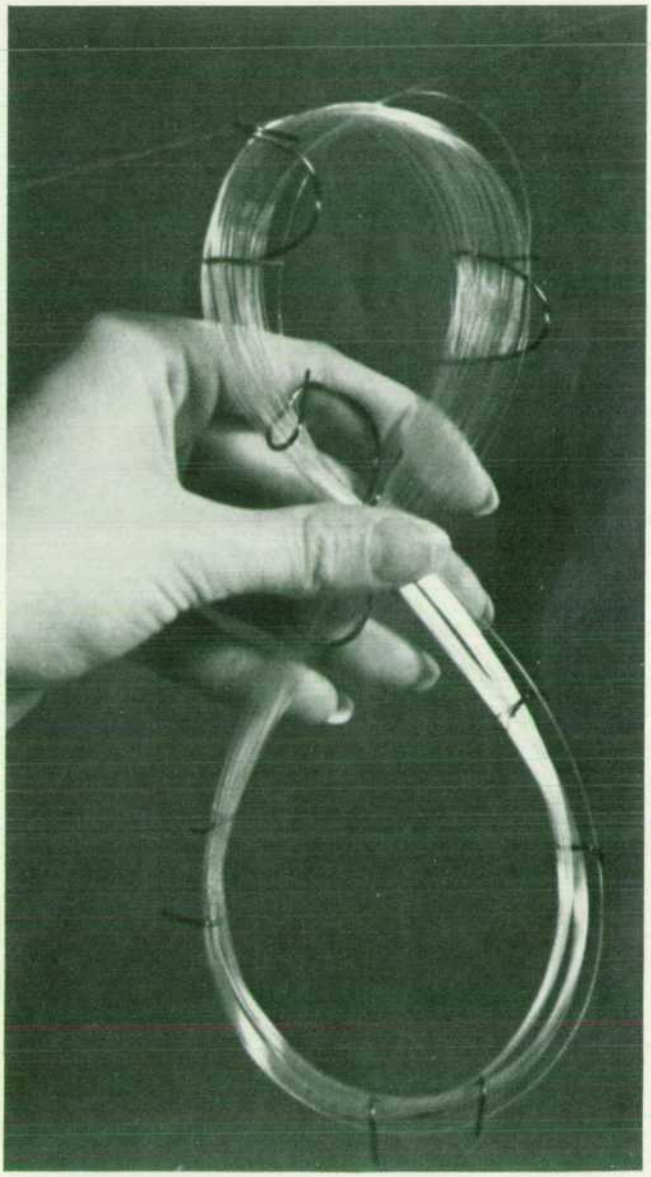

Fig. 7. *Flexibility of the fused quartz columns.*

needed. Chromatographic efficiency (ability to produce narrow peaks) is guaranteed.

The Ultra columns are similar, but provide even higher efficiency. In addition, they have exceptional retention-time reproducibility from column to column.

One objection to the use of capillary columns is their lack of sample capacity. This is the amount of sample that a column will accept and process without peak distortion caused by "flooding" of the stationary phase. Since capillaries have much less stationary phase per unit length than packed columns, they are more subject to sample overload.

The new Series 530μ columns address this problem. They have a wide (for a capillary column) inside diameter and accept a large amount of stationary phase. Sample capacity is comparable to that of a packed column. Separating power is less than for a narrow-bore capillary, but is better than that of a packed column because of the simplicity of the internal structure and the absence of a packing material. They are made of fused silica, with all the advantages of that material.

Acknowledgments

Many people were involved in the fused silica development, both at Avondale and at HP Labs, and we can mention only a few. Ron Hiskes, Chris Schantz, and their associates at HP Laboratories were extremely helpful in demonstrating the feasibility of producing fused quartz capillaries and transferring the technology to Avondale. Paul Bente of Avondale made the first columns from the fused quartz tubing and did the initial testing. Beverly Newton (Avondale) has been the manufacturing chemist for this product from the beginning. She has been the link between R&D and manufacturing and has contributed greatly to the success of the entire product line.

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