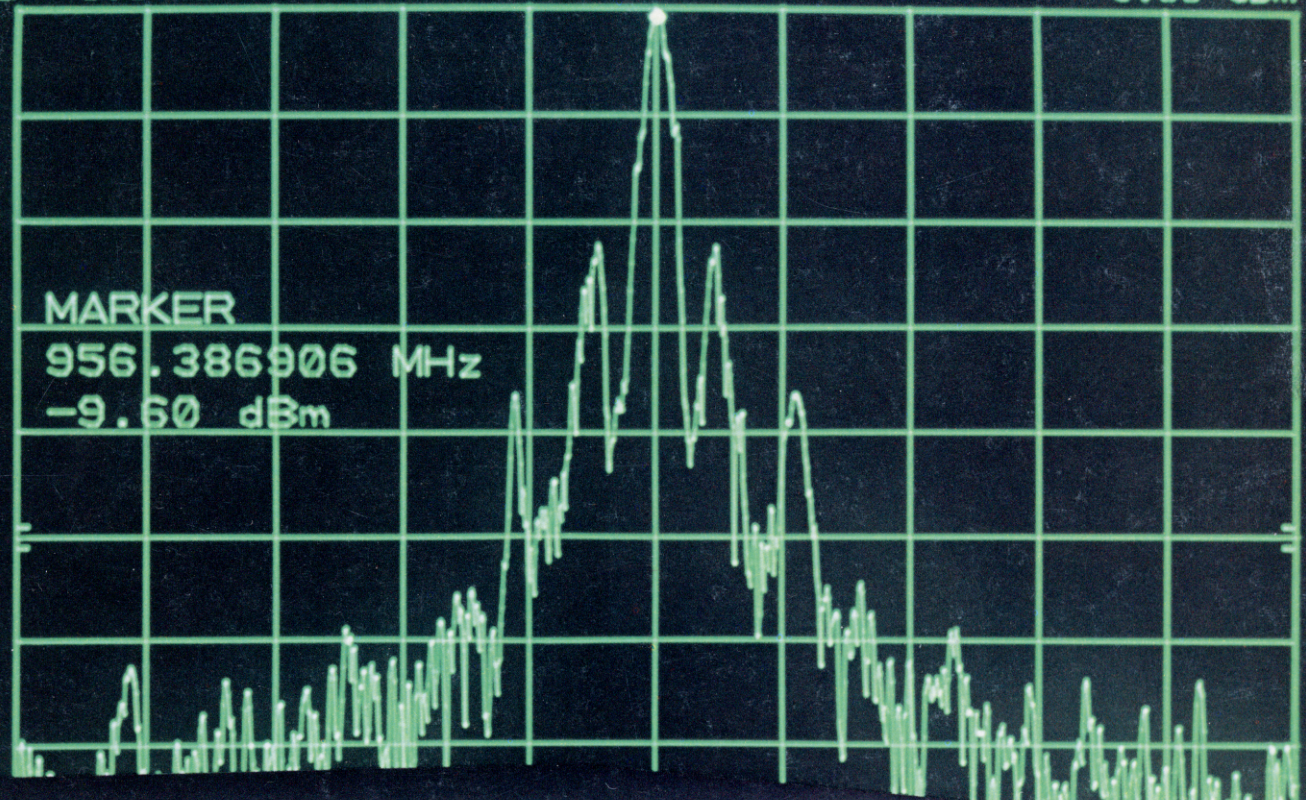8568A SPECTRUM ANALYZER   MKR 956.386906 MHz
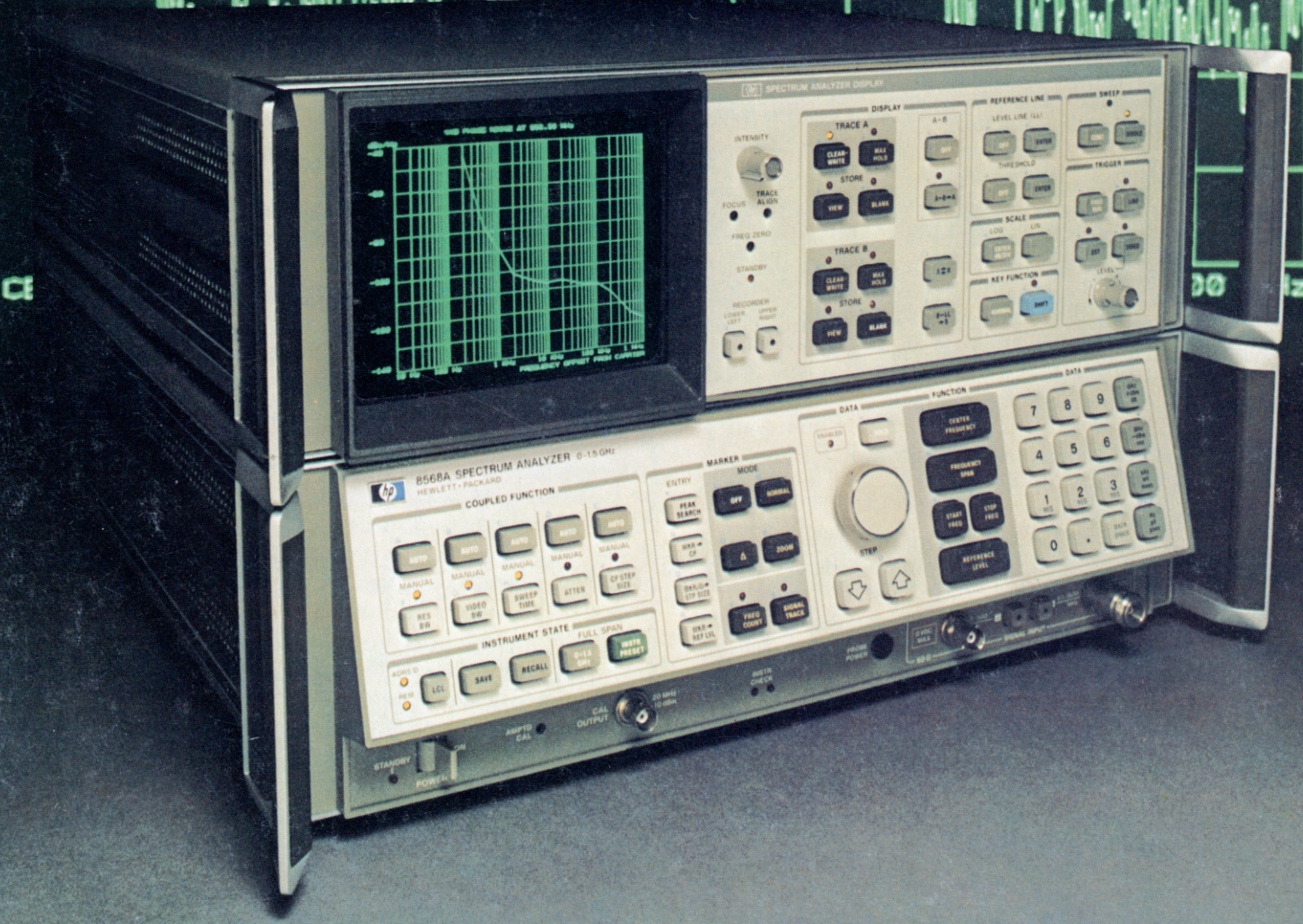
REF −8.8 dBm   ATTEN 10 dB   −9.60 dBm

hp

10 dB/

MARKER

956.386906 MHz

−9.60 dBm

The Next Generation RF Spectrum Analyzer

Unprecedented tuning accuracy, frequency stability, and resolution – combined with a new level of control provided by three digital processors – raise to significantly new levels the art and science of spectrum analysis in the 100-Hz-to-1500-MHz range.

by Steven N. Holdaway and M. Dee Humpherys

THE MAGNITUDE OF IMPROVEMENT in performance over older instrumentation provided by microprocessor-controlled instruments has been such that these new instruments clearly represent a new generation. The microprocessor's contribution to improved performance is not only in the obvious area of more comprehensive data analysis but to a greater extent in providing a level of control that allows the implementation of more complex and powerful measuring hardware.

Thus, with microprocessors controlling its operation, the new Hewlett-Packard Model 8568A Spectrum Analyzer, Fig. 1, achieves a significant improvement in signal-analysis capability over previous analyzers. With a measurement range of 100 Hz to 1500 MHz, and such features as synthesizer-controlled tuning, resolution bandwidths as fine as 10 Hz over the full tuning range, 90-dB log display, excellent spectral purity, and digital storage with display annotation, it makes a major contribution to the field of spectrum measurement. These features rely heavily upon the internal digital processors, which also give the analyzer unparalleled ease of operation and full HP Interface Bus* compatibility. Bus compatibility makes the power of spectrum analysis measurements practical and cost effective in production line applications as well as in unattended spectrum surveillance and similar applications.

Three-Way Improvement

Although Model 8568A is more powerful in many ways than its predecessors, its major contributions are in three areas.

First is improvement in frequency accuracy. In previous analyzers, the accuracy of the dial indication of the center frequency in the range up to 1500 MHz was limited to about ±10 MHz because the local oscillators were tuned open loop. The synthesized local oscillators in Model 8568A achieve a tuning accuracy
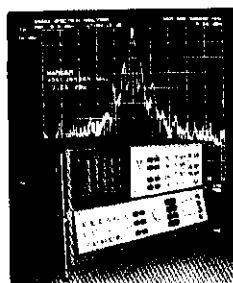
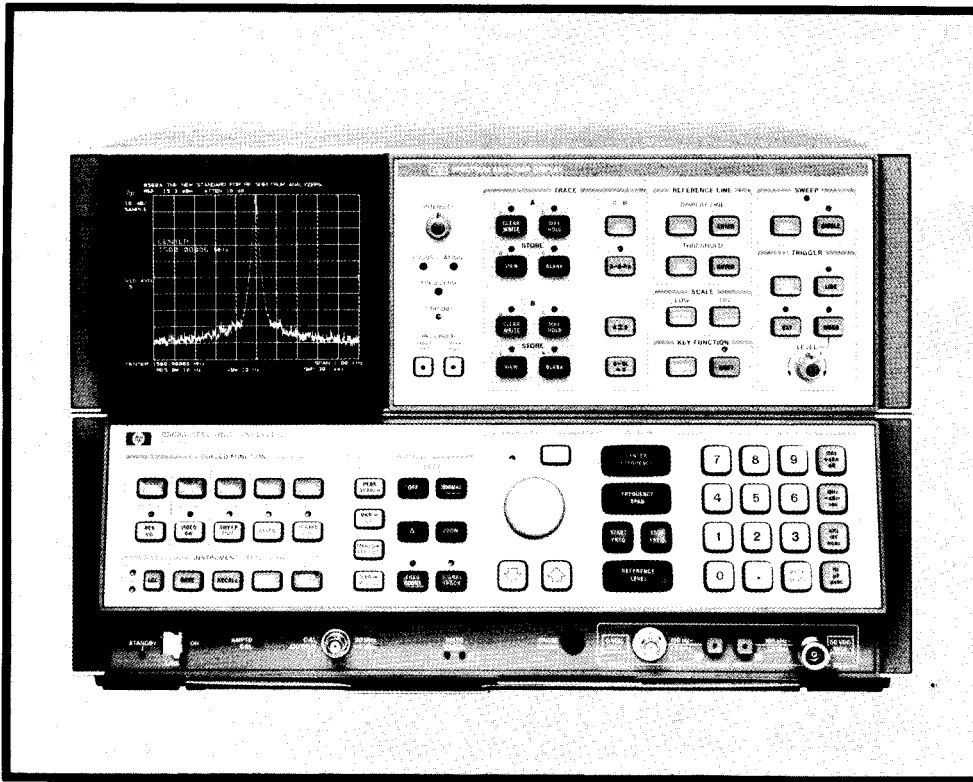**Cover:** *This spectrum analyzer not only displays RF spectra digitally, it can transfer the data to a computer for reformatting, and then display the result, as shown here. This is but one of many new capabilities of this instrument.*

In this Issue:

Fig. 1. *The new Hewlett-Packard Model 8568A Spectrum Analyzer uses three digital processors to greatly simplify detailed analyses of the spectra of signals over a wide range of frequencies, from 100 Hz to 1.5 GHz. Significant improvements in RF performance have also been achieved.*

within ±100 Hz of the selected frequency, an improvement in frequency accuracy of over 10,000 times. In addition, with the use of a "counter" marker, the frequency of a signal can be measured to within ±10 Hz with signal levels as low as −110 dBm.

This capability allows the user to make measurements far more rapidly and with greater accuracy than ever before, and it also provides the resolution and repeatability necessary to make remotely controlled measurements practical.

The second area of improvement is in resolution, that is, the ability to distinguish two signals that are separated either by a very small frequency difference or by a very large amplitude difference. To achieve high resolution, an analyzer must have not only narrow resolution bandwidths but also low phase noise and residual FM on its local oscillators, since the frequency conversion process superimposes this noise upon the signal being measured. The effect of phase noise is to mask very small signals that lie in the vicinity of larger ones, thus decreasing resolution.

The narrowest resolution bandwidth previously available in analyzers measuring above 110 MHz was 30 Hz. Model 8568A has 10-Hz minimum resolution bandwidth. This narrow bandwidth allows the measurement of powerline-related sidebands more than 60 dB down from the signal level at frequencies up to 1500 MHz.

Because of a new phase-lock technique, phase noise on the local oscillators has been reduced by over

20 dB. Phase noise is at least 80 dB down from the signal in all resolution bandwidths narrower than 3 kHz (Fig. 2). It is now possible to measure phase noise and low-level spurious responses on high-frequency oscillators directly without having to heterodyne the signal down into the range of a high-resolution, low-frequency analyzer.

This high resolution and low phase noise is complemented by a 90-dB logarithmic display that is accurate to within ±1.5 dB overall and within ±1 dB over the upper eight divisions of the display. This capability, along with the narrow resolution bandwidths and low phase noise, makes it possible to view and accurately measure signals whose power levels are more than eight orders of magnitude different from each other and separated in frequency by as little as 200 Hz.

An Approachable Instrument

The third area of contribution is in the human-machine interface. The keyboard, digital storage, and CRT readout of instrument control settings allow the user to take full advantage of the frequency accuracy and improved resolution.

The spectrum analyzer keyboard (see Fig. 1), although it appears significantly different from previous knob-controlled analyzers, provides a more convient and powerful means of front-panel control. Instead of having a separate control knob for each function, the keyboard has only one knob, a rotary pulse
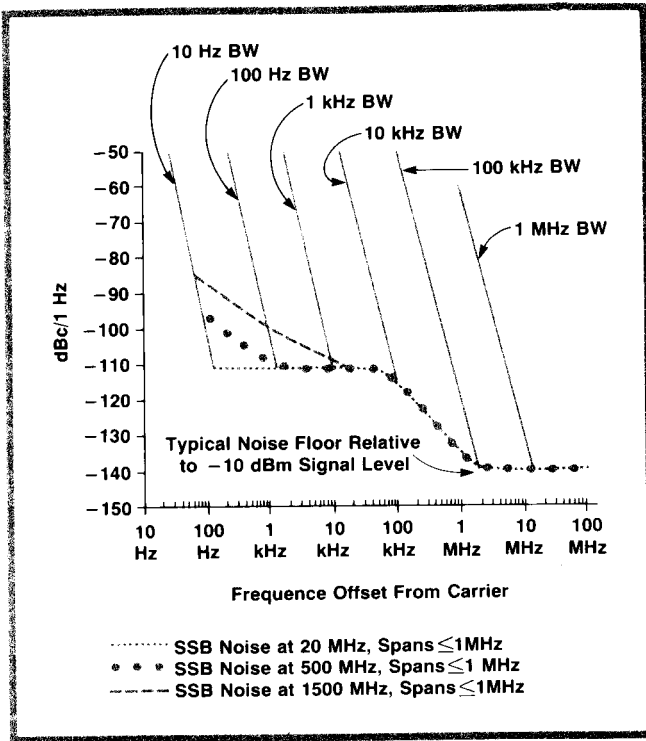
Fig. 2. *Typical single-sideband noise in the new Model 8568A Spectrum Analyzer as a function of frequency offset from the carrier.*

generator that along with step keys and a numeric key pad can be assigned to control any analyzer parameter simply by pressing that parameter's key. All parameters are set in this manner and their values are displayed on the CRT. With a choice of three different means of setting values (knob, step, digits) the operator can use the one that is most convenient for each particular parameter. For example, to narrow in on a signal he might use the knob first to tune the signal to the center of the display, then the step keys to reduce the frequency span, and finally, the numeric keys to set a particular reference level.

The analyzer's main microprocessor automatically adjusts the sensitivity of the knob and step keys for the current range of each parameter. When center frequency is selected, for example, 1½ rotations of the

knob moves the signal from one edge of the graticule to the other regardless of the frequency span, and the step keys move the signal in one-division increments. The constant sensitivity of the knob with respect to the displayed frequency span eliminates the need for the coarse, fine and, in some cases, extra-fine tuning controls of older analyzers.

The microprocessor also makes the frequency-stabilizing phase-lock process completely transparent to the user. The old frustration of running up against a stop on the tuning control just before getting the signal to the center of the screen is now gone.

If the exact frequency of the signal is known, it can be entered directly from the key pad, and the analyzer will move to that frequency with sufficient accuracy to place the signal typically within 1/5 division of center screen, even in narrow frequency spans.

Such spectrum analyzer parameters as resolution bandwidth, video bandwidth, sweep time, and input attenuation are automatically assigned appropriate values by the microprocessor when the frequency span is chosen. These parameters can also be set manually from the keyboard using the knob, step keys, or numeric keys.

Marker Convenience

The microprocessor also makes possible display markers, another new feature that eases operational difficulties. A marker can be positioned at any point on the displayed spectrum by means of the DATA controls. The frequency and amplitude of that point are then displayed on the CRT, thus simplifying and speeding the measurement of the signal.

Pressing the MARKER Δ mode key creates two markers, one fixed where it was positioned previously and the other movable (Fig. 3). The frequency and amplitude readouts are now the frequency and amplitude differences between the two markers. This simplifies relative measurements such as those involving spurious and modulation sidebands.

Digital Storage and Display

The digital storage unit has its own digital proces-
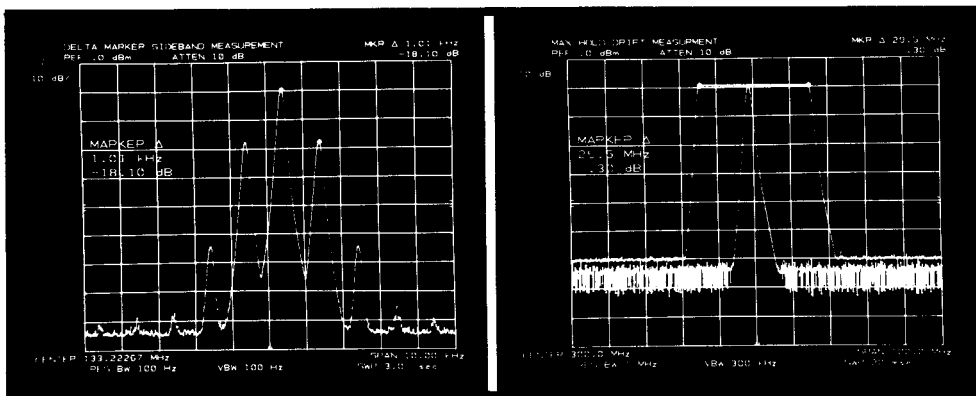
Fig. 3 *(left). When the MARKER Δ MODE key is pressed, the tunable marker becomes fixed and a second, movable marker is added. The display annotation then shows the frequency and amplitude differences between the two.*

Fig. 4 *(right). The MAX HOLD mode retains and displays the maximum signal level that occurs at each frequency during several successive frequency scans. This shows peak FM deviation or frequency drift.*

sor for handling the digitizing, storing, and displaying of data (the third processor controls the HP-IB interface). The storage/display processor also handles the storing and display of control settings and the generation of the graticule. Data and characters stored in the memory are traced on the CRT by a vector line generator at a rate independent of the rate at which the measurement is being made. Up to three signal traces can be stored and displayed along with the display annotation. Each trace is stored with 1000×1000-point resolution.

The display processor has access to the stored trace information. It can subtract one trace from another as when "normalizing" a trace by subtracting from a measurement errors stored during a calibration sweep. It can also perform a function called MAX HOLD where each new data point is stored only if it is larger than the data point already in memory at that horizontal location. This provides a means of determining the amount of FM or frequency instability on a signal (Fig. 4).

Since the keyboard approach to front-panel control does not provide for indicating parameter values on the panel itself, the display becomes the primary means of annunciating operating conditions. To avoid unnecessary interference with signal trace data, all status information, with one exception, is displayed on the periphery of the 10×10-division graticule. The one exception is the "active function" readout that displays the function whose value is changed by operator entries. For example, Fig. 3 displays MARKER Δ as the active function, and an operator entry from the knob, step, or digit keys will reposition the movable marker on the trace.

These display features, while improving the human-machine interface, impose critical constraints on the CRT. For example, any CRT beam defocussing is most pronounced at the corners, where status information is written in small characters. Also, graticule lines are written at full beam intensity be-
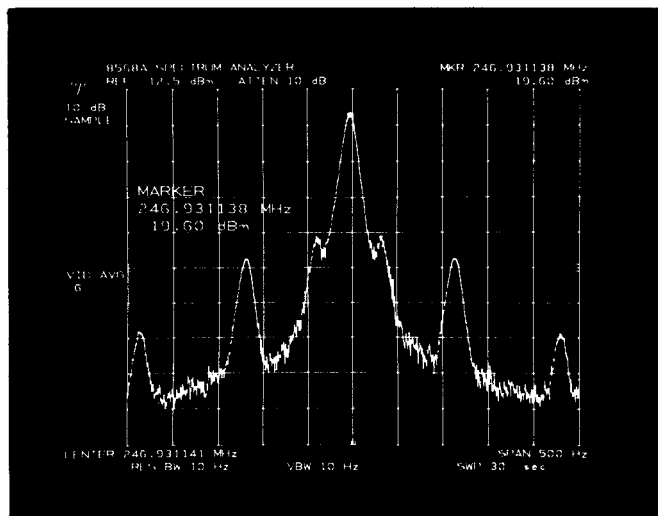
Fig. 5. *The trace is sharp everywhere on the CRT. (This is a VHF oscillator test showing 30-, 60-, and 120-Hz sidebands.)*

cause of the large beam deflections incurred, a condition that normally causes significant defocussing. These constraints require the choice of a high-resolution CRT with tight control of beam spot size as well as adequate brightness over the full tube face. Standard oscilloscope CRTs, optimized for other needs, do not meet these requirements, but the high-resolution CRT used in the HP Model 1332A Display most nearly meets these requirements and is used in the new spectrum analyzer (Fig. 5). An improved CRT contrast filter was also developed to meet the diverse requirements of high visual contrast, RFI suppression, and operator safety.

HP-IB Compatibility

In addition to the keyboard interface, Model 8568A is also the first spectrum analyzer to be fully programmable via the HP Interface Bus. All front-panel control settings, except for video trigger level and CRT intensity, can be set by way of the bus, and all of

Fig. 6. *Frequency spectra obtained by Model 8568A, such as the one at left, can be sent via the HP interface bus to a computing controller, reformatted into a log-frequency plot, and sent back to Model 8568A for display (center). The computing controller can also derive tabular data for display by the analyzer (right).*

5

A Precision, Digitally-Controlled Spectrum Analyzer for the 20-Hz-to-40-MHz Frequency Range

by Robert E. Temple

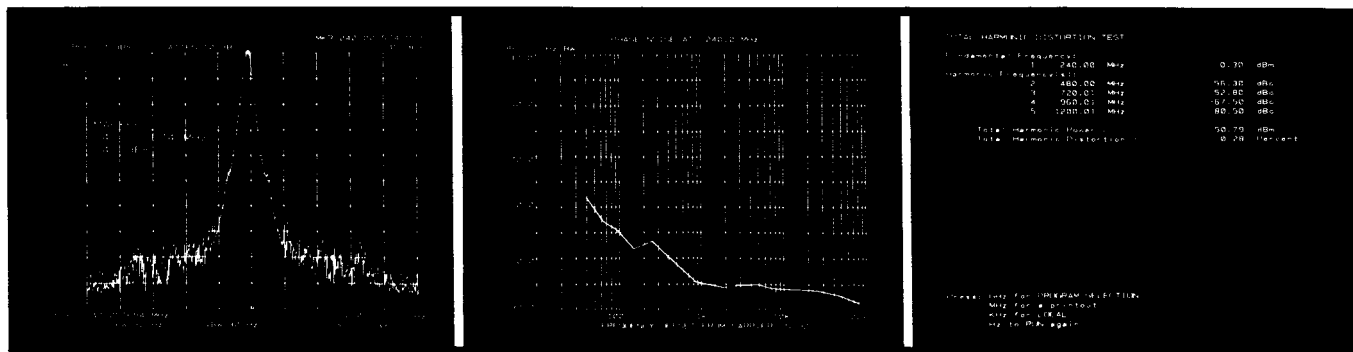Spectrum analyzer performance approaching that of a precision wave analyzer has been achieved by applying microprocessor control to an instrument for use in the audio-to-high-frequency (20 Hz - 40 MHz) range.

Amplitude measurements made by this analyzer (Model 3585A) are accurate within ±0.5 dB over the entire frequency range and an amplitude range of +30 dBm to −75 dBm. Even at −95 dBm, amplitude accuracy is within ±0.8 dB. This is achieved by a microprocessor-controlled calibration routine that uses an internal crystal-controlled 10-MHz reference signal to measure and compensate for frequency-tuning and system-gain errors, and an extremely flat internal tracking generator that measures and compensates for frequency-response and attenuator-ranging errors.
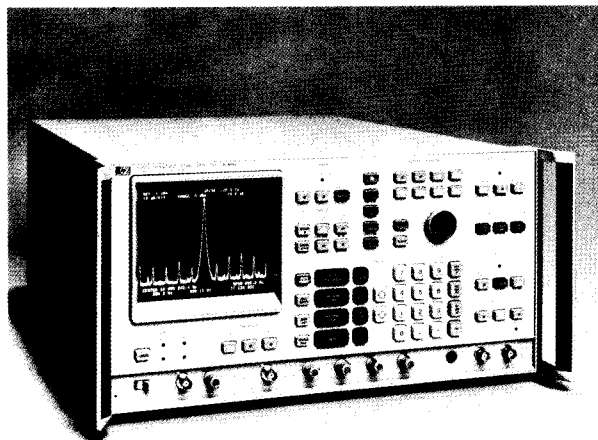
The total measurement range is −135 dBm to +30 dBm. The amplitude of any point identified by a movable marker on the displayed spectrum is measured and presented numerically on the CRT with 0.01-dB resolution, and the frequency is measured using a counter function with 0.1-Hz resolution.

Frequency measurements are accurate within ±0.3 Hz ±1×10⁻⁷/month. This accuracy was made possible by the use of synthesizer techniques, the tuning range of this instrument allowing all the local oscillator frequencies to be synthesized. Thus, the local oscillator frequencies are known precisely at any point in the tuning sweep so the signal at the output of the IF section can be measured by a counter and converted arithmetically by the microprocessor to arrive at the value of the input signal frequency.

Model 3585A is a triple-conversion receiver. The synthesizer that generates the local oscillator signals uses the fractional-N technique[1] to obtain very small frequency steps with phase coherence between steps. The frequency sweep is thus essentially continuous. In addition, a tracking generator output is derived from the synthesizer so the analyzer can be used for swept-frequency measurements of amplitude response.

The stability and low phase noise of the synthesizer enable the narrowest resolution bandwidth (3 Hz) to be used over the full frequency range to 40.1 MHz. Thus, Model 3585A can measure low-level frequency components lying very close to much larger frequency components. For example, it can measure

50-Hz or 60-Hz power line sidebands more than 80 dB below carriers with frequencies as high as 40 MHz.

Noise and distortion products generated internally are more than 80 dB below a −25-dBm full-scale input when using resolution bandwidths as wide as 3 kHz. Thus, it is not necessary to use narrow bandwidths with resultant very slow sweeps to find low-level signal-related distortion products.

Digital Control

Control of Model 3585A Analyzer by a microprocessor gives it many of the operating features of Model 8568A described in this issue. Thus, it has keyboard control of the instrument functions with variable parameters (center frequency, reference level, etc.) set by a knob, step keys, or numeric entry. Information that defines the displayed spectrum is presented on the CRT.

Resolution bandwidth, video bandwidth, and sweep time are automatically set by the choice of frequency span to simplify narrowing in on a signal. Instrument operation is further simplified by automatic ranging of the input attenuator in 5-dB steps with concurrent tracking of the reference level. Hence, the largest signal within the range of the instrument is automatically placed near the top of the CRT graticule.

The acquired spectrum is digitized into 1001 data points and stored in memory for repetitive read-out and display on the CRT. A second data memory allows retention of a reference spectrum for later display or for A−B measurements. The instrument can also operate in an offset mode for relative measurements, and in a MAX HOLD mode for measuring frequency drift or FM.

Model 3585A is fully HP-IB compatible for automating measurements or for further processing of acquired data. For example, the amplitudes of a signal's harmonics can be measured and transferred over the HP-IB to a computing controller for calculation of total harmonic distortion.

Automatic Calibration

The calibration routine occurs automatically about once every two minutes or whenever any control settings that affect instrument calibration are changed (center frequency, resolution bandwidth, etc.). First, the internal 10-MHz reference signal is switched to the analyzer input, the synthesizer tuning is swept across a narrow band of frequencies centered on the reference

Robert E. Temple
Raised in Newburyport, Massachusetts, Bob Temple earned a BA degree in physics at Harvard University and then migrated westwards to the University of Colorado where he obtained MS (1969) and PhD (1971) degrees in electrical engineering. In 1969, he joined HP's Loveland Instrument Division in Colorado where he worked on the 3320A and 3330A/B Frequency Synthesizers before becoming co-project leader on the Model 3585A. Bob is now a production engineer.

frequency, and the peak response is noted. The offset of the peak from 10 MHz is then applied to the synthesizer as a correction factor. This assures that the analyzer's tuning is always within 0.1 Hz of that indicated.

Once the analyzer is tuned precisely to the reference, the amplitude of the resulting video signal is measured and compared to the value that should result. Any difference is used to adjust the IF and video gain to give the correct value.

The internal tracking generator, which uses precision limiters to obtain a very flat frequency response, is then switched to the input and tuned initially to 10 MHz. Its level is measured and stored as a reference. It is then tuned to the center of the selected frequency span in synchronism with the analyzer's tuning and measured again. Any difference with respect to the level at 10 MHz is stored as a correction factor for subsequent measurements. Next, the input attenuator is stepped through all 12 ranges (−25 dBm full scale to +30 dBm full scale) and the video output measured at each step and compared to references to derive additional correction factors. The entire routine takes from less than a second to several seconds depending on the resolution bandwidth selected.

Reference
1. J. Gibbs and R. Temple, "Frequency Domain Yields Its Data to Phase-Locked Synthesizer," Electronics, 27 April 1978.

Steven N. Holdaway
Born in Pleasant Grove, Utah, Steve Holdaway obtained BSEE and ME degrees at Brigham Young University (1971) before joining HP in Palo Alto, where he worked initially on the 8558A Spectrum Analyzer and then as project manager for the RF section of Model 8568A. Now living in Santa Rosa, California, with his wife and four children (ages 2 to 7 years), Steve is active in church and youth work, does some cabinetry and gardening, and is learning to play the piano.

M. Dee Humpherys
Dee Humpherys joined HP in 1964 and worked on microwave spectrometers, spectrum analyzers, signal generators, and as project manager for the 8568A IF/display section. A native of Wyoming, Dee obtained BES and MSEE degrees at Utah's Brigham Young University. Now living in Santa Rosa, California, Dee is involved in church and youth activities, renovating his home, and camping and cross-country touring in his van with his wife and five children (ages 1 to 12).

the information stored in the analyzer is available to the bus controller. The bus controller can also write into the analyzer's memory. This allows the user to take data, reformat it into a more convenient form such as a log frequency plot or a tabular list, and then write the information in the new format into digital storage, as shown in Fig. 6.

The display can also be used by the bus controller to give visual prompts to the operator and to draw test setups. Portions of the analyzer's keyboard may be enabled even during remote operation to allow the operator to make responses on the keyboard to questions the controller can ask via the display (Fig. 7)

Design details that led to the performance improvements described above are examined in the following articles.

Acknowledgments

Fig. 7. The controller in an HP-IB system can use the CRT of the Model 8568A Spectrum Analyzer for graphics displays, such as a listing of available test programs (left) and diagrams of test set-ups (right).

ABRIDGED SPECIFICATIONS
HP Model 8568A Spectrum Analyzer

Frequency

MEASUREMENT RANGE: 100 Hz to 1500 MHz dc coupled; 100 kHz to 1500 MHz ac coupled.

DISPLAYED RANGE: From 100 Hz full span to 1500 MHz full span.

RESOLUTION: 3-dB bandwidths of 10 Hz to 3 MHz in 1,3,10 sequence.

SPECTRAL PURITY: Noise sidebands >80 dB below peak of CW signal at frequency offsets $\geqslant 30 \times$ resolution bandwidth setting, for resolution bandwidths $\leqslant 300$ Hz.

ACCURACY

CENTER FREQUENCY: $\pm$(2% of frequency span + frequency reference error $\times$ tune frequency + 10 Hz) using error correction.

MARKER FREQUENCY COUNT: Frequency reference error $\times$ displayed frequency ± 2 counts (span $\leqslant 100$ kHz).

FREQUENCY REFERENCE ERROR (aging rate): $<1 \times 10^{-9}$/day (2×10^{-7}/yr).

Amplitude

MEASUREMENT RANGE: -135 dBm to $+30$ dBm or equivalent in dBmV, dBμV; 40 nV to 7V.

DISPLAYED RANGE: 10,5,2,1 dB/div and linear calibration; 10-division vertical scale.

DYNAMIC RANGE

SPURIOUS RESPONSES: Second harmonic distortion and third-order intermodulation distortion $\leqslant 70$ dB below signal levels that are $\leqslant -30$ dBm at the input mixer.

AVERAGE NOISE LEVEL: < -135 dBm in 10-Hz resolution bandwidth.

ACCURACY: Measurement accuracy is a function of technique. The following sources of uncertainty can be summed to determine achievable accuracy.

CALIBRATOR UNCERTAINTY: ± 0.2 dB.

FREQUENCY RESPONSE UNCERTAINTY: ± 1.0 dB.

COMPARISON UNCERTAINTY (resulting from one of the following techniques for comparing the unknown signal with the calibration level):

REPOSITIONING SIGNAL TO CALIBRATION LEVEL: ± 0.7 dB.

USING MARKER: ± 1.7 dB.

Sweep

TIME: 20 ms full span to 1500 s full span. With zero frequency span, 1 μs full sweep to 1500 s full sweep.

TRIGGER: Free run, line, video, or external.

MODE: Continuous or single (by trigger after arming).

Input

RF INPUTS: 100 Hz to 1500 MHz, 50Ω dc coupled (BNC fused); 100 kHz to 1500 MHz, 50Ω ac coupled (type N).

MAX INPUT LEVEL

AC: $+30$ dBm (1 watt) continuous power; 100 watts, 10 μs pulse into $\geqslant 50$ dB attenuation.

DC: 0 volts dc coupled input; ± 50 volts for ac coupled input.

ATTENUATOR: 70-dB range in 10-dB steps.

Output

DISPLAY: X, Y, and Z outputs for auxiliary CRT display.

RECORDER: Horizontal sweep (X), video (Y), and penlift/blanking (Z) to drive an X-Y recorder.

AUXILIARY: 21.4-MHz IF, 2—3.7-GHz 1st LO, Calibrator, Frequency Reference.

Instrument State Storage

Up to 6 sets of user defined control settings may be saved and recalled.

Remote Operation

All analyzer control settings (with the exception of video trigger level, focus, align, intensity, frequency zero, and amplitude cal) may be programmed via the Hewlett-Packard Interface Bus (HP-IB).

General

POWER: 100, 120, 220, 240V ($+5\%$, -10%), 50 to 60 Hz, approximately 450 VA.

DIMENSIONS: 280 mm H $\times$ 425 mm W $\times$ 560 mm D (11 $\times$ 16¾ $\times$ 22 in).

WEIGHT: 45 kg (100 lb).

OPTIONS: 75Ω input impedance (Opt 001); 400-Hz powerline operation (Opt 400).

PRICE IN U.S.A.: 8568A, $27,800. Opt 001, $200. Opt 400, $400.

MANUFACTURING DIVISION: SANTA ROSA DIVISION
1400 Fountain Grove Parkway
Santa Rosa, California 95404 U.S.A.

ABRIDGED SPECIFICATIONS
HP Model 3585A Spectrum Analyzer

Frequency

MEASUREMENT RANGE: 20 Hz to 40.1 MHz.

DISPLAYED RANGE: 0 Hz full span to 40.1 MHz full span.

RESOLUTION: 3-dB bandwidths of 3 Hz to 30 kHz in 1,3,10 sequence.

ACCURACY

CENTER FREQUENCY: $\pm 1 \times 10^{-7}$/mo.

MARKER

NORMAL: $\pm .2\%$ of full span $\pm$ resolution bandwidth $\pm 1 \times 10^{-7}$/mo.

COUNTER: $\pm .3$ Hz $\pm 1 \times 10^{-7}$/mo.

Amplitude

MEASUREMENT RANGE: -135 dBm to $+30$ dBm.

DISPLAYED RANGE: 10,5,2,1 dB/div. over 10-division scale.

DYNAMIC RANGE: Harmonic distortion and third-order intermodulation distortion >80 dB below signals equal to or less than input range.

AVERAGE NOISE LEVEL: < -135 dBm in 3-Hz resolution bandwidth.

ACCURACY: Best achievable accuracy over measurement range is$\pm .5$ dB to ± 1.3 dB depending on level.

Display

TRACE: Two memories, A and B, each 1001 points horizontally by 1024 points vertically can be displayed. A is updated by analyzer sweep, B by transfer from A. Can display A–B and MAX HOLD in A.

TRACE DETECTION: Positive peak signal excursions between horizontal data points are retained and displayed.

Sweep

TIME: 200 ms full sweep to 11,603 hrs full sweep.

TRIGGER: Free run, line, or external.

MODES: Continuous, single, or manual.

Input

SIGNAL INPUTS

50Ω and 75Ω; return loss >26 dB.

1 MΩ; $\pm 3\%$ shunted by <35 pf.

MAXIMUM INPUT LEVEL

50/75Ω; $+30$ dBm (1 watt).

1 MΩ; 22 Vrms.

Output

TRACKING GENERATOR: 0 dBm to -11 dBm.

DISPLAY: X,Y, and Z outputs for auxiliary CRT display.

RECORDER: Horizontal sweep (x), video (y), and penlift/blanking outputs to drive an X-Y recorder.

AUXILIARY: 350 kHz IF, video, 10-MHz frequency reference.

INSTRUMENT STORAGE: Up to three sets of user defined control settings may be saved and recalled.

REMOTE OPERATION: All analyzer control settings (with the exception of tracking generator level, CRT intensity, focus, astigmatism, and graticule) may be programmed via the Hewlett-Packard Interface Bus (HP-IB).

General

POWER: 100, 120, 200, 240V ($+5\%$, -10%), 48 to 66 Hz, <250 VA.

DIMENSIONS: 229 mm H $\times$ 426 mm W $\times$ 635 mm D (9 $\times$ 16¾ $\times$ 25 in).

WEIGHT: 39.9 kg (88 lb).

PRICE IN U.S.A.: $17,500.

MANUFACTURING DIVISION: LOVELAND INSTRUMENT DIVISION
815 Fourteenth Street, S.W.
Loveland, Colorado 80537 U.S.A.

Signal Processing in the Model 8568A Spectrum Analyzer

by Steven N. Holdaway, David H. Molinari, Siegfried H. Linkwitz, and Michael J. Neering

HIGH RESOLUTION AND PROGRAMMABILITY in the Model 8568A Spectrum Analyzer impose rigid requirements on the performance of the analyzer's RF system, shown in block diagram form in Fig. 1. Measurement accuracy requires a knowledge of the exact amount of frequency translation that occurs as the input signal is converted to the fixed intermediate frequency where bandwidth filtering occurs, and the local oscillator's residual FM must be held to less than 1 Hz, a level commensurate with the 10-Hz narrowest resolution bandwidth of Model 8568A. The 90-dB display range called for a reduction in the local oscillator's phase noise of 20 dB over that of the best of previous analyzers operating up to 1500 MHz.

It was clear that merely improving on previous methods of stabilizing the RF system would not give the desired performance because these methods stabilize only the first local oscillator. Furthermore, they provide no frequency information about any of the local oscillators. Therefore, to achieve the required low phase noise, plus frequency stability and accuracy, a new phase-lock system that locks all the local oscillators in one loop was devised.

The new phase-lock system, shown in Fig. 2, uses a second frequency-conversion path driven by the same local oscillators that drive the measurement signal path. The input to this "pilot" path is derived from a 20-MHz reference that is accurately controlled in frequency and that has very low phase noise.

The reference frequency is formed into very narrow pulses in a comb generator to obtain harmonics to greater than 1500 MHz. The 20-MHz harmonic closest to the selected center frequency is converted to the IF in the pilot path and appears at the phase detector as f_{pl3}. This is compared with a 20-MHz signal from the reference oscillator and the resulting correction signal tunes the first local oscillator in the proper direction to achieve phase lock. Once the loop is locked, any phase noise, instability, or drift in any of the three local oscillators is cancelled by the loop.

Tuning the instrument to center frequencies between the harmonics of 20 MHz is accomplished by offsetting the frequency of the third local oscillator using accurately controlled frequency-synthesis techniques. This causes the first local oscillator to change frequency by an equal but opposite amount.

Removing Oscillator Aberrations

How the phase noise, instability, and drift in any of the three local oscillators is cancelled can be shown by examining the relationship between the four frequencies f_{in}, nf_{ref}, f_{sl3}, and f_{pl3} shown in Fig. 2. Taking into account the frequency conversion at each mixer it can be shown that:

$$f_{in} = f_1 - f_2 - f_3 - f_{sl3}$$
$$nf_{ref} = f_1 - f_2 - f_3 + f_{os} - f_{pl3}$$

It can be seen in the first equation that the IF output frequency, f_{sl3}, is a function of the input frequency, f_{in}, plus all the local oscillator frequencies, f_1, f_2, and f_3. Since the term $(f_1 - f_2 - f_3)$ appears in both equations, we can solve for f_{in} in terms of nf_{ref}, f_{sl3}, f_{pl3}, and
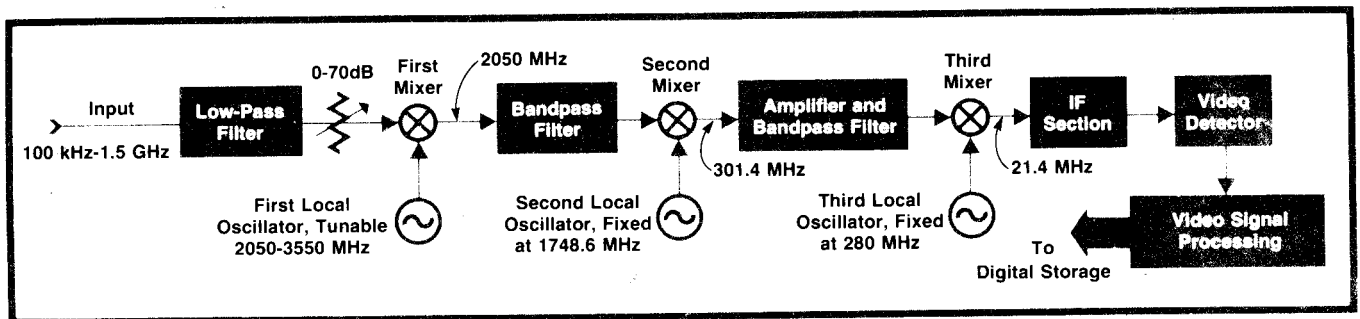
Fig. 1. *The basic concept in Model 8568's RF section follows traditional practice in that the input signal is up-converted to 2 GHz so image frequencies can be removed by low-pass filtering at the input, then down-converted to the 20-MHz IF in two steps so unwanted sidebands from the mixing processes can be removed. Resolution bandwidth filtering occurs in the IF section.*
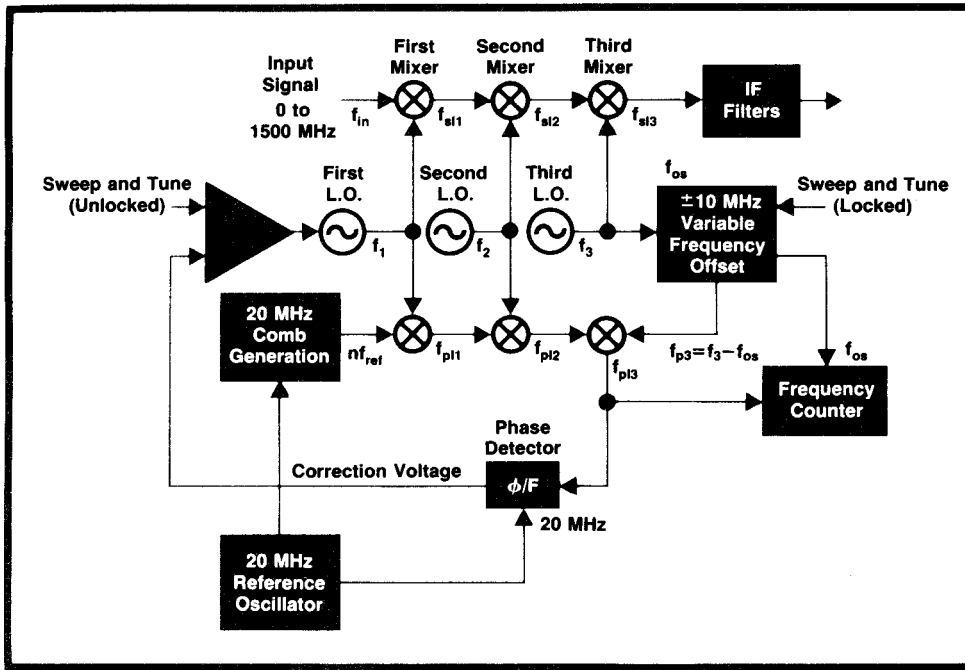
Fig. 2. Skeleton block diagram of Model 8568A's RF section includes the pilot path (lower row of mixers). It is part of a phase-lock loop that locks the entire frequency-conversion process to a crystal-controlled reference oscillator.

f_{os} (the amount of offset applied to the third local oscillator).

$$f_{in} = nf_{ref} + f_{pl3} - f_{sl3} - f_{os}$$

Notice that in this last equation local oscillator frequencies f_1, f_2, and f_3 have no influence on the IF output frequency, f_{sl3}. It should be further noted that this relationship was derived with the phase lock loop open. By closing the loop, we force f_{pl3} to equal f_{ref}. Making this substitution in the last equation we get:

$$f_{in} = (n+1)f_{ref} - f_{os} - f_{sl3}$$

Thus, with the loop closed, the relationship between f_{in} and f_{sl3} is modified by only two factors: $(n+1)f_{ref}$ which is related to the harmonic of the reference frequency that the loop is locked to, and f_{os}. Since f_{ref} is a fixed frequency, it can be made to have very low phase noise (-130 dBc 100 Hz from the center frequency), accuracy, and stability ($<1 \times 10^{-9}$/day aging rate). The offset frequency, f_{os}, has a range of only ±10 MHz at a center frequency of 250 MHz and by proper use of frequency synthesis, is made to have a phase noise of -110 dBc 100 Hz from the carrier.

Thus, at frequencies below 200 MHz, there is a phase-noise floor at -110 dBc due to f_{os}. At higher frequencies, phase noise from the reference f_{ref}, proportional to the harmonic number, n, begins to dominate. For example, if the tuned frequency is 1500 MHz (n=75), phase noise due to f_{ref} in a 10-Hz resolution bandwidth is $[120$ dB $- (20\log75)]$ dB or

>80 dB down 100 Hz from the center frequency. This is very low compared to systems that lock only the first LO to a 1-MHz reference that requires harmonic numbers of 2000 and up when multiplying up to the 2-4 GHz range of the first LO. These high harmonic numbers result in at least a 66-dB degradation in phase noise over that of the reference. In contrast, the new system operates at harmonics from 1 to 75.

Determining the Frequency

Another benefit of the phase-lock system is that it provides a means for determining the frequency of the input signal very accurately. Returning to the last equation, the frequency of the input, f_{in}, can be computed if f_{ref}, f_{os}, and f_{sl3} are known. The reference f_{ref} is known precisely. The IF, f_{sl3}, can be taken as the center frequency of the IF filters which, for the crystal filters of the narrow resolution bandwidths, have a center frequency that is known within ±100 Hz. The only unknown is then the offset, f_{os}. The implementation of the offset provides an output in the range of 10 to 30 MHz to a built-in counter, so the offset can be determined precisely.

Thus, the analyzer's center frequency—that is, the frequency that if injected into the input would give maximum response at the output of the IF filters when the frequency sweep is at center screen—can be set very accurately by selecting the proper harmonic of f_{ref} and setting f_{os} for the proper amount of offset.

To sweep the analyzer about the selected center frequency, the offset oscillator is swept. The phase-lock system then causes the first LO to sweep an equal but opposite amount. However, the maximum sweep width of the offset oscillator is 1 MHz, so for fre-

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The Display System in the Model 8568A Spectrum Analyzer

by Michael J. Neering and Larry O. Bower

The display system in the Model 8568A Spectrum Analyzer goes beyond the digital-storage and character-generating systems found in previous spectrum analyzers where the user made readings by comparing the trace on the CRT to a reference line on a fixed graticule. Besides digitizing and displaying data, the display system in Model 8568A provides display capabilities such as marker readout, graticule generation, presentation of three data traces and labels for measurement documentation, and other features normally found only in graphics display equipment. These capabilities simplify the operation of Model 8568A and make the measurement results easy to interpret.

A block diagram of the display system is shown below. The system is built around a 12-bit digital processor responsible for the three tasks of signal processing, communications with the instrument's main processor, and display processing. The signal processing task includes detection, digitization, storage into memory, and the data calculations for the max hold and normalization functions. Communications with the main processor are handled between sweeps or while the progress of the sweep is suspended. Information going to the main processor includes measurement data, memory contents, and present position of the frequency sweep. Information coming from the main processor includes signal conditioning commands, processed data, and the description of the CRT display contents. The display description is sent in the form of a display program and stored in memory. The display program, by allowing looping and the use of subroutines, is a more efficient means of describing the display than an ordered list of X-Y pairs.

The third task, that of display processing, occurs on a coroutine basis with the first two tasks. The display processing objective is to execute the display program line by line and create the picture on the CRT. As the processor decodes the display program, it sends X and Y pairs to the line generator, which connects X-Y points in sequence to create smooth lines on the display.

In the normal operating mode of the display system, the incoming video signal is sampled, stored digitally, and displayed on the CRT. However, when the sweep is so fast that the processor cannot sample, digitize, and store the signal into memory fast enough, digital storage is bypassed and the video signal goes directly to the CRT. A fast sweep generator then provides the horizontal deflection. Sweep times of 1 μs to 10 ms are handled in this manner. The direct display is interlaced with the digitally-stored display to create a combination of a conventional CRT signal display and digitally-generated graphics.

Display Processor

The control firmware for the display processor is contained in 1024 32-bit words of ROM. The firmware is divided into two sections: operating firmware and test firmware. The operating firmware is in turn divided into two coroutines: display program execution and signal processing with main processor I/O.

The control hardware for the display processor has an algorithmic state machine (ASM) structure. The basic ASM structure is augmented with hardware capability for link storage between the firmware coroutines. The link saves the next address and next qualifier of the coroutine that was exited. The coroutines resolve conflicts in memory access and accumulator sharing within their respective firmware, such as saving the contents of the accumulator.

A data manipulator is also contained in the display processor. The key to its implementation was providing the ability to process measurement and display data within the required time. The data manipulator centers on sixteen 12-bit registers divided equally between the coroutines. Data can be transferred directly to and from the register bank without involving the accumulator, so the usual bottlenecks that arise when using a single accumulator do not exist. An ALU performs the operations of transfer, inversion, and, or, addition, and subtraction. Operands for the ALU are supplied from the register bank, the accumulator, or a ROM that has sixteen data constants for each coroutine. With these constants, the ALU can increment, decrement, clear, or load any of the registers.

The speed of the display processor is dictated by the requirement for simultaneous signal processing and display processing. The maximum rate of signal processing is 20 μs per data point (a 1,000 point sweep in 20 ms). To get all traces and characters on screen without flicker, the display processing must generate one line segment every 5 μs. At the time of the
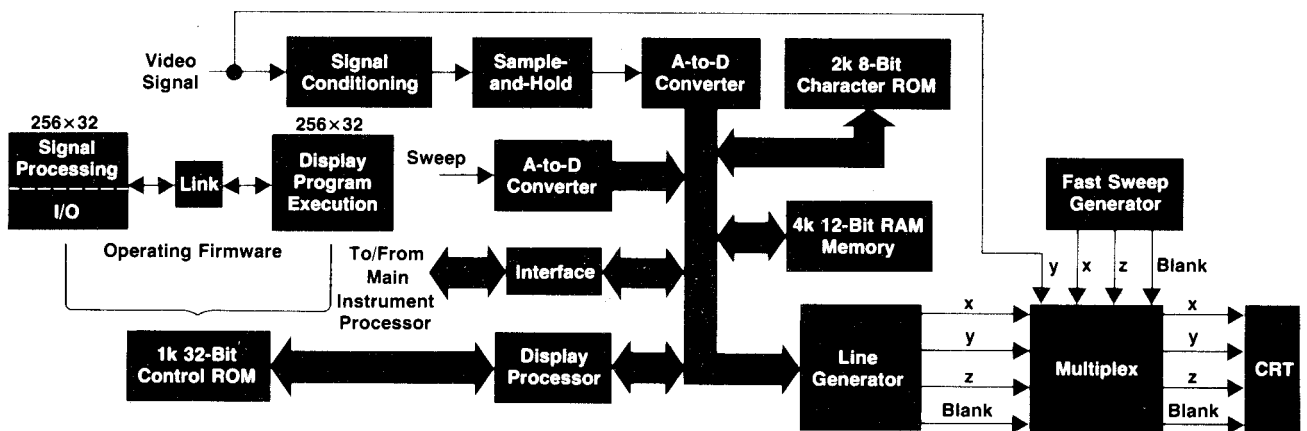
display system design, no monolithic or bit-slice microprocessor capable of handling these speeds was available. Instead it was necessary to use available medium-scale integrated-circuit logic and apply pipelining concepts to the controller and data manipulator. By overlapping the fetch and execute phases of each microinstruction, a new microinstruction is executed every 125 ns, just fast enough to meet the speed requirements.

Display Features

The display system contributes a number of features to the Model 8568A, all intended to give complete documentation of measurement conditions to enhance the interpretation of data. The electronically generated graticule eliminates the effect of CRT and deflection amplifier drift on the relative position of the data and graticule and it also makes the display simpler to photograph. By appropriate positioning of the graticule, two rows of characters can be written both above and below the graticule, and short labels may appear along the left side. This allows adequate space for displaying all the control settings and measurement parameters. Part of the display area is set aside for user-entered titles.

Nearly 200 characters and two 1000-point data traces may be displayed without flicker. If some flicker is tolerable, the third data trace may be displayed simultaneously. The easy access to the data traces provided by the display system, coupled with the ability to draw and randomly position simple symbols, allow the main processor to position one or more markers directly on the data trace. Readout of the marker amplitude and frequency appears outside the graticule.

Many operator visual aids are provided by the display system. The most significant is that of giving feedback to the operator as he manipulates the front panel control. This is especially useful in recording the entry of parameters.

Any user-designed display program may be loaded into the display system memory. By this technique, a full sequence of display pictures may be created to cause animation, to give step-by-step measurement instructions, to diagram measurement set-ups, to draw circuit schematics, and to display annotated results of measurement parameter conversions.

Larry O. Bower

Larry Bower joined HP's Loveland Instrument Division upon getting his BSEE degree from the University of Illinois (1969). At HP, he worked on a number of DVM's and related products and was project leader on an 8-bit microprocessor before transferring to HP's Santa Rosa Division to work on Model 8568A's display processor. A native of Chicago suburbia, Larry is married and has a 5-year-old daughter. He's a home computerist and also enjoys sailing his own boat on San Francisco Bay.

quency spans greater than this, the analyzer is momentarily tuned to the desired center frequency and the correction voltage on the phase-lock feedback loop is retained on a capacitor. The phase-lock loop is then opened and the first LO is swept once over the desired frequency range. At the end of the sweep, the loop is locked up again at the center frequency.

The IF Section

Corresponding improvements in performance were made to the IF section. For example, the excellent close-in noise performance of the RF section makes the use of a full 100-dB display feasible (90 dB calibrated) but a 100-dB logarithmic amplifier with bandwidth wide enough for the 3-MHz resolution bandwidth would raise the noise floor on the display more than a division above the bottom graticule line. To lower the noise floor on the narrower bandwidths, a switchable bandwidth filter is included within the logarithmic amplifier chain. Gain, attenuation, and filtering are also distributed within the IF in such a way as to not degrade the performance level established by the RF section.

For all resolution bandwidths, synchronously-tuned (non-ringing) filters are used so there are no spurious responses caused by energy stored in the filters when a large-amplitude signal is swept through. Five poles are used for all bandwidths less than 30 kHz to maintain a typical 10:1 shape factor

(ratio of filter bandwidth at 60 dB and 3 dB points). Metalized glass inductors eliminate problems with the susceptibility to temperature, humidity, and time of the very-high-Q ferrite devices used in earlier analyzers.

The greatest improvement in performance, however, can be attributed to the computing power of Model 8568A. The error-correction routine in the analyzer's resident programs measures the amplitude errors in the IF section, using an internal calibration test signal, and corrects them with a programmable, calibrated attenuator built into the IF section separate from the reference-level attenuators. The calibration attenuator is programmable in 0.1-dB steps over a range of 0 to 15.9 dB and is accurate to 0.1 dB over its entire range.

Video Signal Conditioning

The video processing technique used in Model 8568A was dictated by the requirements of digital storage. During a frequency sweep, 1000 samples of the video signal are taken and stored. However, simply taking and storing 1000 samples does not give adequate results with all combinations of resolution bandwidth, frequency span, and sweep time.

Consider, for example, an often-encountered spectrum analyzer input: short duration RF pulses occurring at a relatively low repetition rate. When the

analyzer sweeps across the RF pulse spectrum, the output of the video detector is a series of short pulses. The shape of these pulses corresponds to the impulse response of the spectrum analyzer system (approximately Gaussian) and their rise time is 0.12 μs when the resolution bandwidth is at its widest setting (3 MHz). Representing this signal with sampled data would require a sampling rate higher than 6 MHz but there are other limiting factors, such as CRT resolution

A high-quality CRT display might have a 10-cm horizontal axis and a resolution of 40 lines/cm. RF spectrum analyzers typically sweep no faster than 20 ms per sweep, so multiple video signals occurring within a 50-μs sweep segment (20 ms × 1/400) will not be resolved but will appear on the display as a single vertical line having the amplitude of the largest video signal and an intensity proportional to the summation of all the signals occurring within that segment. Thus, a peak detector that retains the peak value encountered during each 50-μs period would permit sampling at a 20-kHz rate for the 20-ms sweep. However, the information contained in the intensity modulation would be lost, corresponding to the loss of information resulting from the use of the slower sampling rate (as compared to 6 MHz).

Wideband impulse-type signals are not the only ones that can cause difficulties for the conversion process. CW signals can also be misrepresented when the analyzer is set for a high-aspect-ratio display (aspect ratio is defined as the ratio of frequency span to resolution bandwidth). Because the video signal resulting from a CW signal during a frequency sweep is a replica of the shape of the resolution-bandwidth filter response curve, at least five samples must be taken within the −3-dB points on the response curve to assure that the peak amplitude is captured with less than 0.1-dB error. This would limit the aspect ratio to 200 for a 1000-point display using sampled data.

For larger aspect ratios, a peak detector enables the peak amplitude to be captured by only one sample per data point. The trade-off is a sacrifice in frequency accuracy of 0.1% of the frequency span, but this is well within the visual resolution of the displayed spectrum.

Resolving Anomolies

A peak detector can give a misleading representation of noise. With noise as the input signal, the video signal can be considered as a tightly packed random sequence of individual impulse responses. However, a peak detector retains only the noise peaks and information on the variance is lost. Indeed, this can lead to erroneous results in measurements of low-level signals that are barely above the noise level. The peak-detected waveform may look very much like a

video-averaged waveform whereas the peak is much higher than the true average because of the noise fluctuations.

For this reason, Model 8568A has both a negative peak detector and a positive peak detector driven in parallel by the video detector. The general scheme is to display the positive peak values for the odd-numbered data points and the negative peak values for the even-numbered points, giving a realistic reconstruction of noisy signals. However, this introduces a complication because it is desired to retain only the positive peak values of clean signals so amplitude measurement accuracy is preserved. Therefore, the video processor in Model 8568A displays positive and negative peaks alternately only when noise is present. Otherwise, only the positive peaks are displayed. Fig. 3 illustrates the concept.

A block diagram of the video processor is shown in Fig. 4. The video signal is applied to the positive and negative peak detectors simultaneously. Before the start of a sweep, the switches in the peak detectors are closed and the capacitors charge to the value of the video signal. At the start of the sweep, the display's digital processor opens the switches and the positive peak detector tracks increases in the video signal while the negative peak detector tracks decreases. For example, the output of the positive peak detector increases only when the video signal increases above the value already stored on the capacitor and, of course, it never decreases.

When the processor determines the end of a data position (sampling interval), it selects the output of one of the two peak detectors to represent the signal at the A-to-D converter. If it selected the positive peak
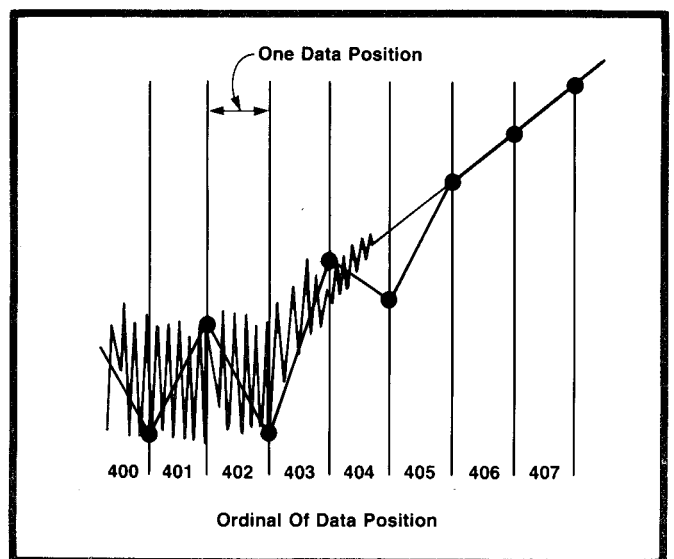
Fig. 3. *A portion of a spectrum display is expanded here to show how Model 8568A's video processing system reacts to signal characteristics.*
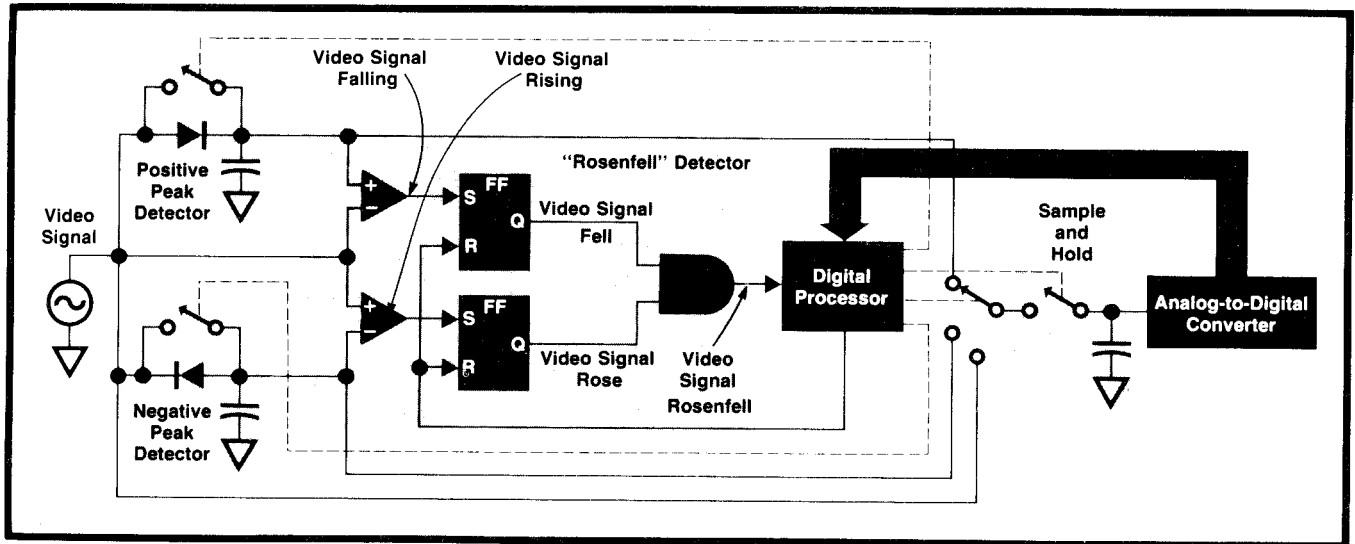
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Fig. 4. *Block diagram of the video processing system. The "rosenfell" detector responds to noise in the signal by detecting signal slope reversals during a data position.*

detector, it would then close the corresponding switch, re-initializing the capacitor to the present value of the video signal. If it had selected the negative peak detector, it would not reset the positive peak detector but would retain the value stored on the capacitor for use in the next data position. However, for reasons given later, the negative peak detector is re-initialized at the end of every data position.

Detecting Noise

The most important information the processor needs to decide which peak detector to choose is whether or not the incoming signal contains noise. As shown in Fig. 3, a noisy video signal is characterized by many variations and large deviations. Noise is present in each of the ordinals 400 through 404 and the signal rises and falls repeatedly. However, in ordinals 405 through 407 there is no noise and the signal increases monotonically. Using these signal properties, it is a relatively simple matter to determine whether or not a data position contains noise.

The "rosenfell" detector of Fig. 4 tells the processor when noise is present. The input stage of the rosenfell detector consists of two comparators. The upper comparator detects when the instantaneous video signal is less than the positive peak detector output, which can only mean that the video signal is falling. In a similar manner, the other comparator indicates when the video signal is rising.

Whenever the video signal falls, it causes the "fell" flip-flop to be set and whenever it rises, it causes the "rose" flip-flop to be set. If the video signal both rose and fell within a data position, the AND gate would send a "rosenfell" indication to the processor, signifying the presence of noise within the data position.

Both flip-flops are reset at the beginning of the next data position.

To Reset or Not

The success of the detection technique at reconstructing the video signal hinges on the rules for resetting the peak detectors. The signal in the upper row of photos in Fig. 5 demonstrates the importance of resetting the positive peak detector only when it had been chosen to represent the signal for the data position. The aspect ratio for this case is 3000, so the video signal rises out of the noise, reaches its maximum, and returns to the noise level all within one data position. The rosenfell detector would indicate the presence of noise and, if the ordinal were even, the processor would choose the negative peak detector output. However, since the positive peak detector is not reset on this data position, it holds the maximum signal value for the next data position, where the positive peak value is chosen. Thus, the video signal is reconstructed appropriately.

The lower signal of Fig. 5 demonstrates the importance of resetting the negative peak detector at the end of every data position. When a noise-free video signal reverses direction at its peak, the rosenfell detector sees both a rise and a fall and indicates that noise is present within the data position. Then if the processor is also at an even ordinal, the negative peak value would be chosen. But, since the negative peak detector was reset to the value of the signal at the beginning of the data position, its value will be only slightly different from the positive peak detector value and the smooth reconstruction of the video signal is not disturbed perceptibly. At the next data position, the positive peak detector, which retained the maximum value, is chosen.

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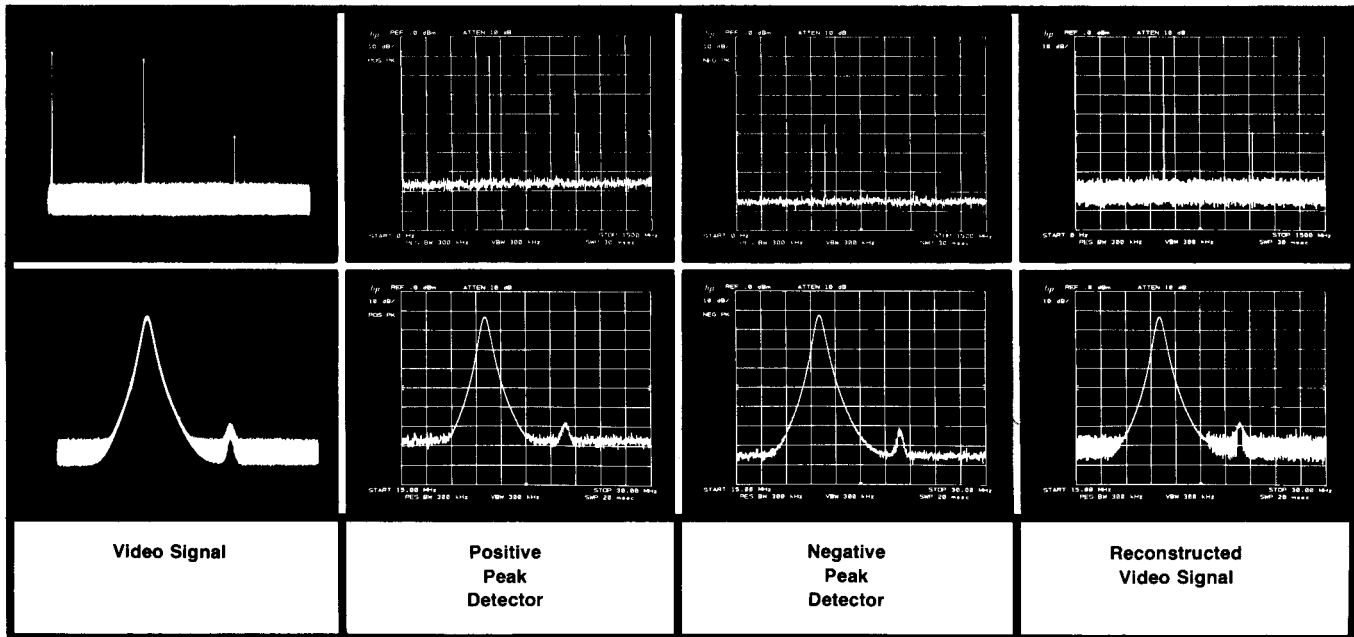
Fig. 5. *CRT photos illustrate how the peak detectors in the Model 8568A Spectrum Analyzer react to signals with high-aspect-ratio sweeps (top row) and with low-aspect-ratio sweeps (bottom row).*

When the analyzer is used for measuring noise or when it operates in a digital averaging mode, the rosenfell detector is bypassed and the video signal is sampled directly by the A-to-D converter.

Digital Extension

The hardware implementation of this detection technique could encounter some practical problems when the analyzer sweeps slowly. The duration of a data position can become as long as 1.5 seconds and a peak value captured by either peak detector could be lost because of gradual discharge of the detector capacitor. This becomes a problem whenever the data position is 75 μs or longer; that is, the sweep time is 75 ms or longer. To avoid the loss of these values the

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processor retrieves the values of both peak detectors from the A-to-D converter at least once every 30 μs, obtaining as many as 50,000 positive and negative peak detector values for the 1.5-second data positions. The processor, however, saves only the maximum and minimum values and at the end of the data position, chooses one or the other to represent the signal for that data position according to the same algorithm described above. These peak values, which the processor stores in its registers, are then reset whenever the peak detectors are reset. In effect, the processor simply extends the range of the peak detec- tors by carrying out the detection process digitally.

The A-to-D converter has 10-bit resolution, equivalent to a resolution of 0.1%. At the end of each data position, the display system processor takes the chosen value, performs any calculations that may be called for (max hold, A−B), and stores the result in memory along with sweep position information. The measurement data can be stored in any one of three areas (A, B, or C) reserved for these data arrays. During the display cycles, the data from any one of these areas can be displayed individually or simultaneously with data from the other areas. ⌷

Developing the Digital Control System for the Model 8568A Spectrum Analyzer

by Michael S. Marzalek and Lynn M. Wheelwright

WHY USE A MICROPROCESSOR to control a spectrum analyzer?—because it greatly enhances operator convenience, enabling him to make complex, time-consuming measurements in a fraction of the time required by previous analyzers.

A microprocessor allows such functions as automatic phase lock and automatic control of resolution bandwidth, video bandwidth, sweep time, and input attenuation. It makes possible automatic self-calibration and troubleshooting diagnostics, and it provides such features as peak search and track modes, plus much more.

The choice of a microprocessor for the Model 8568A Spectrum Analyzer was governed by the desired measurement resolution. Model 8568A has a frequency resolution of 1 Hz at 1500 MHz, which requires 10 decimal digits or 31 binary bits to represent a frequency. Thus, either a 10-digit BCD processor or one that handles double-precision 16-bit words is needed. At the time that development work on this instrument was getting under way, the only processor that appeared capable of doing the job was one under development in the desktop computer R and D labs at HP's Loveland, Colorado, facility. This microprocessor[1,2] is 16 bits wide and it also has 12-digit BCD capability. The instruction set and processing speed are sufficient to permit real-time parameter modification with the tuning knob while also servicing the scan, the automatic phase lock, and the display update. These capabilities also enhance the HP-IB operation.

A block diagram of the digital control organization of the Model 8568A is shown in Fig. 1. The display system uses medium-scale integrated circuits for its digital processor and the HP-IB interface uses an HP-designed 8-bit microprocessor that is optimized for high-speed control functions. The main microprocessor is the above-mentioned 16-bit device.

It was decided to design the hardware on a modular basis with a minimum amount of interfacing between modules. The primary interface is to the 50-line main microprocessor bus. Since there are many modules on the bus, time was spent in minimizing the circuitry needed to interface to the bus. By restricting some of the flexibility of the bus, the bus needs only one medium-scale integrated circuit to decode the data strobe for eight bus addresses (the whole instrument uses 40 bus addresses).

Software Development System

In developing the software for the main microprocessor, a method had to be found to develop the software quickly and efficiently so that the software could be used in the development and evaluation of the hardware. New ideas had to be tested easily and rapidly.

One area where software was particularly needed as an optimization tool was the front panel—it was known that the panel would change as the design progressed. New ideas and functions had to be im-
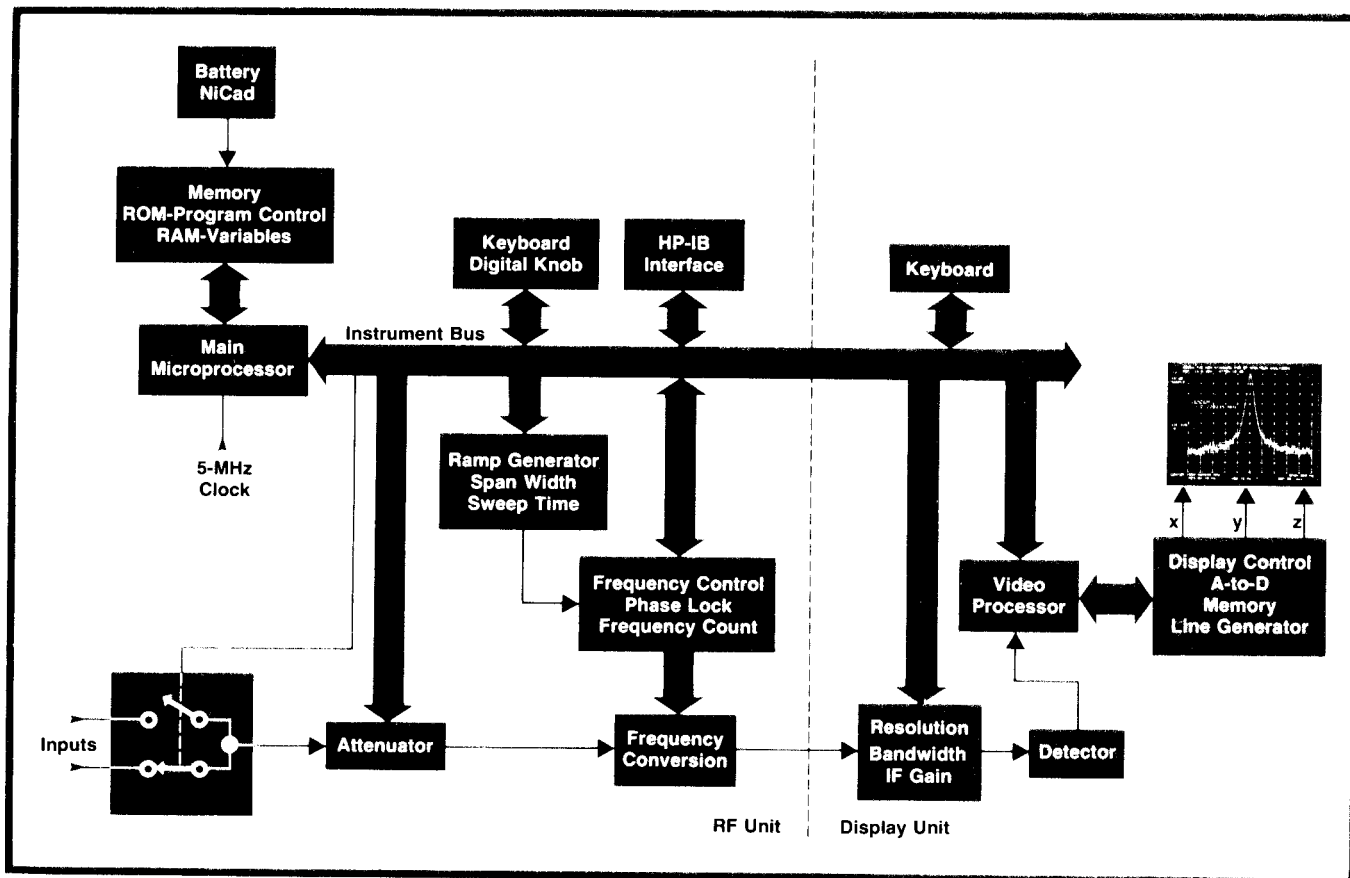
Fig. 1. *Block diagram of the digital control portion of the Model 8568A Spectrum Analyzer. Up to six sets of control settings can be stored in the memory and recalled by use of the* SAVE, RECALL *and number keys. A battery prevents loss of stored data when the instrument power is turned off.*

plemented rapidly so they could be evaluated. The software had to map the front-panel keys onto the hardware capabilities to allow the front-panel operating characteristics to be described without worrying about the implementation. This was especially important because of the high degree of interaction between the user and the spectrum analyzer. Also, the HP-IB interface should operate the instrument the same way the front panel does and all measurement and control parameters should be available to the HP-IB controller in fundamental units (Hz, dBm).

Since the microprocessor hardware was not available initially, the software needed to be hardware independent. The first instrument prototype actually used a minicomputer as a controller. As the design progressed, various configurations of the microprocessor were used as they became available.

To deal with these design constraints, a high-level language (ALGOL) was used for writing the instrument's control programs. There were several reasons for this:

■ It was expected that the axiom of 10 lines of debugged code per day (regardless of language) would hold true. Therefore, the more efficient the language

is at stating the control algorithms, the faster the programs can be written.

■ Software modules more than 1000 lines long are hard to comprehend. Fewer lines means better understanding.

■ A high-level language allows transport of the program from one processor to another without a major rewrite.

■ Documentation is considerably simpler in a high-level language.

■ Where the speed or efficiency of the language was insufficient, there was always the possibility of resorting to assembly language, though improvements in the compiler or high-level code would be tried first.

■ Enough software tools would be developed to allow concentration on program design instead of the frustrations of getting the program implemented.

■ The language, once developed, could be applied to other products.

Implementation

Because no ALGOL compiler existed for the main microprocessor, a metacompiler[3] was used to develop an ALGOL compiler with enhancements for dealing

Control of Model 8568A Spectrum Analyzer through the HP Interface Bus

by Rex A. Bullinger

Programming convenience consistent with strict adherence to the IEEE 488-1975 Interface Standard was the primary consideration during development of the HP-IB interface for the Model 8568A Spectrum Analyzer.

Towards this end, it was desired that the user could read a program listing without frequent reference to a table listing the mnemonic codes for the instrument's functions. Experience has shown that two-character mnemonics provide good program readability with adequate programming efficiency, so a set of two-character mnemonic codes was developed for the programming commands.

Altogether there are 171 mnemonics. Seventy-eight relate directly to the primary operations of the front-panel keys, 61 to the shifted functions, and the remaining 32 to programming functions not on the front panel, such as output formatting, display commands, etc. It may seem a bit overwhelming at first to have 171 commands, but almost half of them relate directly to primary front-panel operations. So, if front-panel operation is familiar, so are the mnemonics. Very few of the remaining 93 commands are necessary to do beginning programming and do not need to be considered until the user is ready to exploit more of the instrument's potential.

Most mnemonics are obvious, such as CF for center frequency. Certain others use a numeral for the second character. For example, the mnemonics for the MARKER MODE keys have an M as the first character and a numeral to indicate which of the four keys is intended, such as M1 for MARKER OFF.

To program the secondary functions of the front-panel keys,—i.e., those functions selected by the SHIFT key—first the mnemonic KS is given and then a single ASCII character corresponding to the desired key. These characters are printed in blue adjacent to the keys (see cover photo). For example, the mnemonic KSW invokes the error-correction routine.

With 171 instrument commands available, a great deal of flexibility is available to the programmer. However, inherent in this kind of flexibility can be many programming traps, especially in view of the analog and digital nature of the instrument. Considerable effort was devoted to eliminating as many traps as possible, and those that could not be eliminated are documented.

An example of the kind of trap that remains has to do with the delimiting of variables. The input format requires that all input variables be delimited, either with a units key (MHz, mV, msec, etc.) or a carriage return (CR), line feed (LF), comma (,), semicolon (;), or end of text (ETX). However, for mnemonics associated with the display, such as DA (display storage address), GR (graph), and PA (plot absolute), there are no units or other explicit delimiters. Therefore, implied delimiting is allowed for these. That is, the presence of a non-numeric character following a display numeric input automatically delimits the variable. This allows inputs like DA 3072 DW 1056,. Note that the comma is needed to delimit the 1056 because of the absence of a succeeding non-numeric character.

HP-IB Address

An internal multibank switch can be used for setting the HP-IB address for the instrument. However, in a departure from conventional practice, whenever the switch is set to 31 the address can be entered at the front panel and stored in the analyzer's CMOS memory. This is much more convenient than setting the internal switch.

The address is set by pressing the SHIFT and ZOOM keys in sequence and then entering a delimited decimal (0-30). The decimal address is then displayed on the CRT along with the corresponding ASCII characters for the listen and talk addresses. In addition the stored address is displayed on the CRT whenever the instrument is turned on. In the event the address is lost, 18 is used as a default address.

Operator Interaction

To enable the power of the instrument to be augmented by an external controller more easily, an HP-IB service request (SRQ) can be made from the front panel. This allows the instrument to be used under local control on the bench in the normal manner and then placed under control of an external controller when some assistance is needed in a particular measurement. The instrument is then returned to local control after the external controller has performed the required task.

The SRQ is activated by pressing the SHIFT and LIN keys in sequence. The external controller then takes control of the instrument and performs the required task. The external controller can also act in an interactive manner with the user, with the CRT and keyboard serving as a terminal. For instance, the command EE (enable entry) allows the operator to enter numeric values, such as selection of a particular test from a menu displayed on the CRT. As an example, the external controller could make the marker the active parameter and instruct the operator to use the knob to place the marker on a particular signal. The controller could then perform the required analysis on this signal.

Implementation

The HP-IB interface uses 8-bit microprocessor architecture. This frees the main instrument controller from handling the HP-IB protocol. In addition, the power of the microprocessor allows pre-processing of the incoming data. This is mainly concerned with interpreting the mnemonics for the main instrument controller, which defines the front-panel keys in terms of the single ASCII code character printed adjacent to each key. For example, when the HP-IB microprocessor receives CF, it converts it to v, the character adjacent to the CENTER FREQUENCY key, and passes it to the main controller.

Rex A. Bullinger

Rex Bullinger spent four years with the U.S. Air Force in computer maintenance operations before entering San Diego State University where he obtained a BS degree in physics (1974). He joined HP upon graduation, working on investigative projects before doing the HP-IB interface for Model 8568A. Born in Kansas, raised in Los Angeles, Rex enjoys skiing and flying, and he gets involved in professional fireworks displays as a pyrotechnic operator.

with ROM-based systems, i.e., look-up tables, equivalence for gaining access to control registers, and multiple data types for dealing with the instrument's control and display functions. The metacompiler was also used to develop an assembler that generates relocatable code, a loader (link editor) to link all the software modules together, and cross-reference table generators for the ALGOL and assembly languages. In support of the other processors in the instrument, a microassembler was written for the display processor and a cross-reference table generator was written for the HP-IB microprocessor (an assembler for it already existed).

Development work began using an HP Model 2100A Computer as the processor. Hardware to monitor the instrument's I/O bus was developed to allow program execution to be monitored.

The first microprocessor system used RAM instead of PROM to facilitate program turnaround time. It was not uncommon to edit and recompile several times a day as experimentation with the control algorithms progressed. When the time came to build several prototype instruments, the switch to an EPROM memory system was made so the instruments could be packaged in final form—a necessary part of testing for interference among the instrument modules. A hardware EPROM programmer capable of programming an entire 32K-byte memory board was also developed.

The HP-IB interface was operational very early in the project. Thanks to this, the instrument was thoroughly exercised throughout its development, a very useful capability when doing environmental testing or looking for limit conditions.

The decisions made on software development provided a means of trying new ideas quickly, leading to the development and implementation of many novel and powerful control functions. Assembly language, on the other hand, is written in such detail that most people apply patch after patch to salvage code already written. The total amount of code written for this project was less, even including the compiler, than if we had used an assembler only. The adjacent tables show the amount of code written. The final result discloses that an average of 12.5 lines of code—and this was in the high-level language—was written per working day during the course of the project.

The Control Program

The control software was designed to contribute both to ease of instrument operation and to measurement capability. To simplify operation, several functions are automatically controlled for the user unless overridden. For example, the resolution bandwidth tracks the frequency span to maintain a nearly constant aspect ratio (span/resolution bandwidth), video bandwidth tracks resolution bandwidth, and sweep time is a function of resolution bandwidth, video bandwidth, and frequency span. The data knob and step keys are automatically scaled to the parameter they control. In particular, the center frequency tuning increments are always a fixed percentage of the frequency span so signals are moved on the display at consistent rates.

The display marker allows readout of measurement data to the full resolution of the instrument. Both stored data and current measurement data can be analyzed using the marker. The delta marker, described previously, makes relative measurements possible. Entry of marker data into the control settings, such as marker frequency into center frequency or marker level into the reference level, is possible. The delta marker frequency difference can be entered into the center frequency step size to speed analysis of harmonics or multiplexed channels.

Another control feature, activated by the PEAK SEARCH key, causes the instrument to search for the highest signal on the display and place the marker on

Table 1. Development Tools

Software Tool	Language	Number of Source Lines	Number of Machine Instructions
ALGOL compiler	Tree Meta	1132	25747
ASSEMBLER	Tree Meta	300	10709
	HP 2100 ass'y	400	
LOADER	Tree Meta	200	7094
OPTIMIZER	Tree Meta	185	7646
Subroutines shared by above	HP 2100 ass'y	1340	included in above
XREFS	Tree Meta	230	6900
Other tools	Tree Meta	450	12750

Table 2. Instrument Firmware

Routine	Language	Number of Source Lines	Number of Machine Instructions
Main control	ALGOL	2325	12672
Math and service routines	Assembly	1915	1429
Processor verify routine	Assembly	390	291
Speed critical routines	Assembly	560	456

it. This is very useful when the analyzer is operating under HP-IB control because it frees the controller from reading and processing all the measurement data to find the maximum signal response.

One of the most useful capabilities of Model 8568A is the SIGNAL TRACK mode. After the marker is placed on the desired signal and the SIGNAL TRACK mode is enabled, the microprocessor searches for the maximum signal in the immediate vicinity and, at the conclusion of the sweep, retunes the analyzer to position this maximum at center screen with the marker at its peak. This simplifies measurements of sidebands and phase noise on drifting signals.
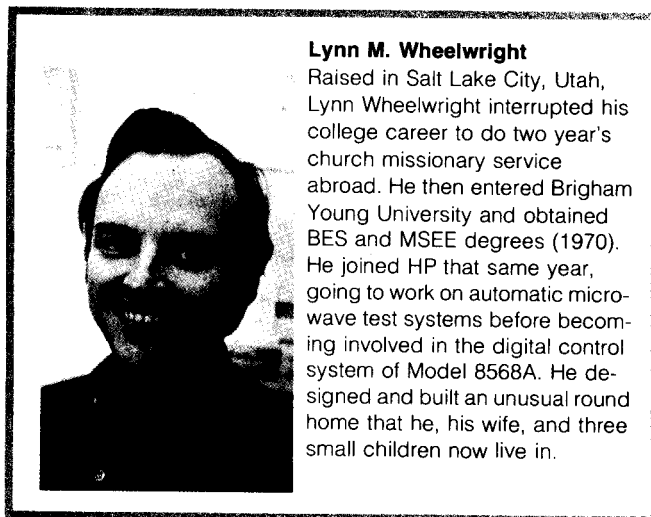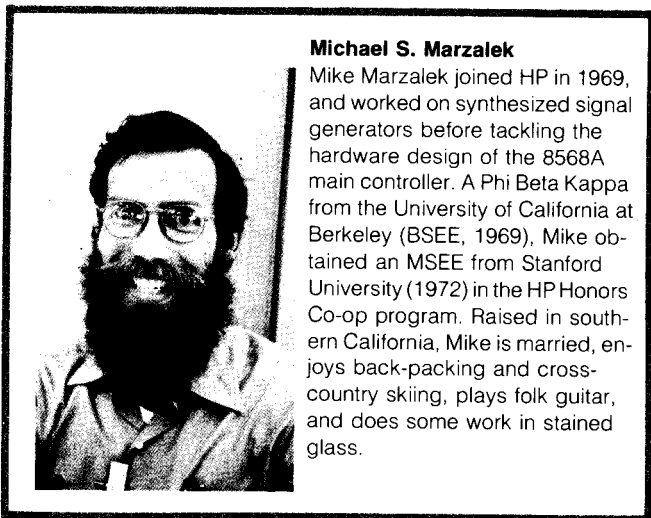
Another benefit of the SIGNAL TRACK mode is that the operator can use the marker to select a signal for analysis in a wide span and then, after enabling the SIGNAL TRACK mode, program the analyzer for a narrow span. The analyzer then automatically reduces the span in half-decade steps until the desired span is reached, all the while keeping the chosen signal centered on the display.

Measurement data can be averaged digitally over as many successive sweeps as desired by pressing the SHIFT key, then the VIDEO BW key followed by numeric entry of the number of sweeps to be averaged. Usually only a few sweeps need be averaged to disclose whether or not averaging helps—e.g., are oscillator sidebands emerging from the noise?

As explained in the article that follows, diagnostic features help in finding failures and in making adjustments, greatly simplifying repair and calibration of the instrument.

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Michael S. Marzalek
Mike Marzalek joined HP in 1969, and worked on synthesized signal generators before tackling the hardware design of the 8568A main controller. A Phi Beta Kappa from the University of California at Berkeley (BSEE, 1969), Mike obtained an MSEE from Stanford University (1972) in the HP Honors Co-op program. Raised in southern California, Mike is married, enjoys back-packing and cross-country skiing, plays folk guitar, and does some work in stained glass.

Lynn M. Wheelwright
Raised in Salt Lake City, Utah, Lynn Wheelwright interrupted his college career to do two year's church missionary service abroad. He then entered Brigham Young University and obtained BES and MSEE degrees (1970). He joined HP that same year, going to work on automatic microwave test systems before becoming involved in the digital control system of Model 8568A. He designed and built an unusual round home that he, his wife, and three small children now live in.

Designing Serviceability into the Model 8568A Spectrum Analyzer

by David D. Sharrit

THE COMPLEXITY OF THE MODEL 8568A Spectrum Analyzer presented several challenges to the serviceability goals set for the instrument. Microcomputer control, the keyboard front panel, the digi-tally-stored display, and the pilot-signal phase-lock loop are new and very different from previous spectrum analyzers with which production and field repair people are familiar. For this instrument to be

```
.54 dB
-.48 dB   -18 Hz
-.22 dB   -15 Hz
-.13 dB   -14 Hz
-.09 dB    -5 Hz
-.07 dB   -25 Hz
-.05 dB  -150 Hz
-.04 dB   350 Hz
.38 dB   6.500 kHz
.09 dB   6.500 kHz
.14 dB  17.500 kHz
.20 dB  -5.000 kHz
.26 dB 180.000 kHz
.35 dB
.48 dB
-.05 dB
-.07 dB
-.04 dB
.33 dB
-.06 dB
-.33 dB
-.25 dB
-.31 dB
-.16 dB
-.12 dB
.00 dB
.01 dB
-.03 dB
-.03 dB
.14 dB  .20 dB  -.02 dB  .06 dB  .22 dB  .34 dB
```

Fig. 1. *Correction factors generated by the error-correction routine can be listed on the CRT to give a check on IF system performance.*

serviced and repaired to the component level in a reasonable amount of time, serviceability had to be designed in, beginning with the first prototype.

Serviceability was implemented by designing self checks into the digital processors, by taking advantage of the processing power of the analyzer to assist in analog troubleshooting, and by designing for signature-analysis[1] troubleshooting of the digital circuitry.

Troubleshooting from the Front Panel

The system was designed so that most faults occurring in the analyzer's frequency-tuning portions are automatically indicated on the CRT display. Each of three phase-lock loops within the instrument has a lock indicator circuit that generates a flag. If any of these flags indicates an unlock condition when the loop should be locked, the appropriate error message is displayed on the CRT, such as 275 UNLOCK, 249 UNLOCK, and YTO UNLOCK. If either of two counter-locked frequencies controlled by the microprocessor cannot be tuned close enough, then either VTO UNCAL or YTO ERROR is displayed. In most cases, these messages make it possible to isolate the fault to two or three internal assemblies.

The instrument's design is such that normal front-panel operations can be used for quick and accurate troubleshooting of analog portions of the instrument. Because exact center frequencies can be keyed in, because markers can be used to read out frequency, frequency difference, amplitude, and amplitude difference, and also because the internal counter can measure and display the input frequency, such tasks as verifying tuning accuracy and bandwidth accuracy are much simpler than before. In addition, the correc-

tion factors generated by the amplitude error-correction routine can be displayed on the CRT, giving the user a quick check on IF section performance (Fig. 1).

Each front-panel key has a secondary function that is accessed with the SHIFT key. For example, pressing the SHIFT key before the FREQUENCY SPAN key is pressed activates the error-correction routine. Several of the shift functions were designed into the analyzer to facilitate troubleshooting. One tells the microprocessor to count and display the actual sweep time, using the internal 10-MHz standard as a clock. It is thus possible to verify the various sweep times without using any external test equipment. This function simultaneously checks the operation of the internal counter.

Other shift functions enable the direct frequency counting of the signal IF, pilot IF, and VTO signals (the VTO generates the frequency offset for the pilot IF path). Another permits direct front-panel control of the digital-to-analog converters (DACs) that normally are controlled by the frequency-tuning algorithms. As an example of how this might be used, the DACs that control the VTO can be set to the end points, 0 and 1023, and the VTO frequency counted at each end point. This enables verification of the VTO oscillator, its tuning range, and the DACs that tune it, all from the front panel.

Making the Unknown Visible

Because of the complexity of the frequency-tuning algorithms, it is not easy for the technician to use the tuning equations to determine many of the internal control settings at a given center frequency and frequency span. One shift function, FREQUENCY DIAGNOSTICS ON, displays most of these settings. These include the tuning DAC settings, the harmonic number, the divide-by-M phase lock numbers, and the calculated frequencies for the VTO and the pilot third LO. Once these numbers are obtained, it is possible to probe the internal circuitry to verify proper operation.

Because the tuning algorithm for the YTO (YIG-tuned first local oscillator) is an iterative process, some failures cause the microprocessor to spend a long time trying to phase lock the YTO before deciding a failure has occurred, in which case it would display an error message and then initiate a sweep. To avoid this time delay during troubleshooting, a shift key function and an internal test point are provided to perform a phase-lock, flag-inhibit function. This tells the microprocessor to ignore errors when tuning the YTO and to sweep as though everything were all right. This essentially corresponds to opening the loop, permitting the analyzer to be tuned during troubleshooting without the microprocessor's con-

Computer-Based Production-Line Testing
of the Model 8568A Spectrum Analyzer

by John C. Faick

Thorough testing and alignment of an instrument as versatile and complex as the Model 8568A Spectrum Analyzer requires multitudinous tests and many hours of test time. For example, to verify with a high level of confidence that the IF/Display section meets specifications, about 600 measurements are made, each requiring different settings of the analyzer and the associated test signal source. Obviously, automatic control of these settings could reduce test time while reducing the potential for human error.

Computer-based production testing of the Model 8568A evolved naturally, since Model 8568A's HP-IB capability required a means of checking the HP-IB interface, which is most readily done with an HP-IB controller. Thus, the decision was made to equip each production-line test station with automatic test equipment controlled by a Model 9825A Desktop Computer. Since the Model 8568A Spectrum Analyzer can be controlled through its HP-IB port, and since many of the basic instruments required for test and alignment of the spectrum analyzer are HP-IB compatible, it was possible to set up semiautomated test stations with practically none of the custom fixtures usually required for automated testing.

Test Station Operation

At each test station, the spectrum analyzer under test is connected to the same HP-IB bus as the test instruments. The analyzer's CRT display then serves as a graphics display for the technician, showing test menus (Fig. 1), instructions for test procedures, and the results of measurements.

When a test is run, the name of the assembly and circuit function being checked or adjusted, the measurement units in use (volts, dBm, etc.), test set-up instructions, and the test limits are displayed on the CRT. When measurements are made, numerical and graphical data as appropriate can also be presented on the CRT. The computer can also process the data, such as determining when the measurement results are within test specifications.

Based on test results, the computer can set up the next test or display what further adjustments are needed in the current test. Control information, such as which key to press to go on to the next step or to abort the test, may also be displayed (Fig. 2). If a hardware failure is suspected, the technician can stop the program and place the test station in a manual mode for troubleshooting the problem with other instruments he has at his disposal.
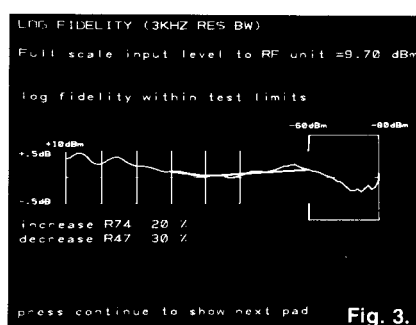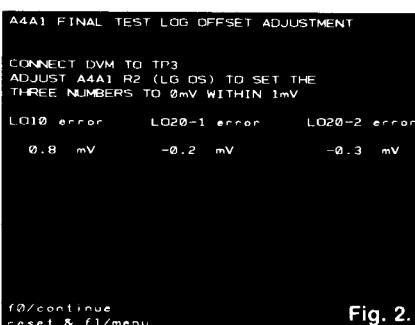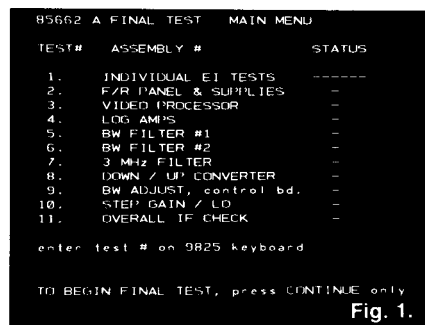
Benefits Achieved

The computer-based test stations have reduced the test time to about half that required for comparable instruments that were tested manually. Also, the automated testing enables far more measurements to be made, achieving much more thorough testing. An example here is the time-consuming search for spurious responses throughout the frequency range in the RF section, which can now be run unattended.

The computer-based testing excels at interactive adjustments that prove difficult or at least frustrating to make manually. An example is the adjustments for linearizing the tuning curve of the varactor-tuned oscillator used to offset the third local oscillator. In a manual test, the technician would have to measure the tuning curve with a special engineering test instrument, calculate the tuning sensitivities, and decide which of four potentiometers to adjust. When the adjustment is made, the process would be repeated until the tuning characteristic is within test limits.

With the computer-based system, the computer controls a voltage source used to tune the VTO and reads a frequency counter that measures the oscillator frequency. The tuning curve is measured and the results are applied to an algorithm that decides which potentiometer needs adjustment. This is then displayed on the CRT. The measurement sequence is repeated about once per second so operator interaction is practically on a real-time basis.

Another example of a difficult manual adjustment that was simplified through computer control concerns the alignment of the log amplifier. This amplifier, operating at the 21.4-MHz IF, has nine limiting amplifier stages. Small gain variations resulting from the tolerances allowed on the components in each stage cause errors in the logarithmic transfer-function curve.

The alignment procedure consists of measuring errors in the curve by stepping the input signal amplitude through the full 90-dB dynamic range in 1-dB steps, measuring the output at each step and calculating the error. The computer stores the error voltage at each level and plots the error curve on the CRT (Fig. 3). It then uses an algorithm to decide which of certain resistors within the amplifier needs to be changed, determines the percent change in value needed, and displays this information. The technician then loads the new value resistor and repeats the process until all stages are aligned and the error curve is within test limits. The complete procedure takes about 30 minutes, whereas to do the test manually it is estimated that one



```
8568A  FINAL  TEST      MAIN MENU

TEST#    ASSEMBLY #                STATUS

   1.     INDIVIDUAL  EI  TESTS       ------
   2.     F/R PANEL & SUPPLIES        -
   3.     VIDEO PROCESSOR             -
   4.     LOG  AMPS                   -
   5.     BW  FILTER  #1              -
   6.     BW  FILTER  #2              -
   7.     3  MHz  FILTER              -
   8.     DOWN / UP  CONVERTER        -
   9.     BW  ADJUST, control bd.     -
  10.     STEP GAIN / LO              -
  11.     OVERALL  IF  CHECK          -

enter test # on 9825 keyboard


TO BEGIN FINAL TEST, press CONTINUE only
```

Fig. 1.

```
A4A1  FINAL  TEST  LOG OFFSET ADJUSTMENT


CONNECT DVM TO TP3
ADJUST A4A1 R2 (LG OS) TO SET THE
THREE NUMBERS TO 0mV WITHIN 1mV

LO10 error        LO20-1 error        LO20-2 error

  0.8   mV          -0.2   mV          -0.3   mV



f0/continue
reset & f1/menu
```

Fig. 2.

```
LOG FIDELITY (3KHZ RES BW)

Full scale input level to RF unit =9.70 dBm


log fidelity within test limits


increase R74   20 %
decrease R47   30 %


press continue to show next pad
```

Fig. 3.

Final Steps

Following the alignment procedures, the instrument covers are put on and a final electrical inspection is made, checking the electrical parameters to production-line limits. This test is run mostly unattended and no adjustments are made to the instrument's internal assemblies. If any measured parameter falls outside the test limits, the instrument is sent back to the alignment station for recalibration. Then the final electrical inspection is repeated.

At the successful completion of a final inspection, the measured data is recorded on tape along with the instrument's serial number and the date. All data for a production run is stored on one minicartridge. The minicartridge is then stored in a library as archival proof of performance.

Besides shortening test time while conducting more thorough tests, computer-controlled testing also provides more uniform testing. This is because precise control is maintained over actual test methods. As an added bonus, operator training is simplified because the computer performs most instrument settings and displays the procedures for each test.
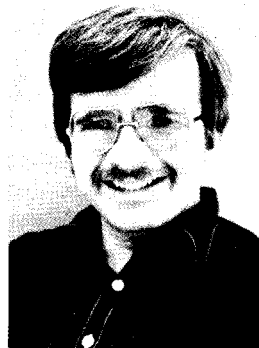
John C. Faick
Raised in Tucson, Arizona, John Faick earned BSEE (1972) and MSEE (1974) degrees at the University of Arizona and then joined HP's Santa Rosa Division. Initially he worked on the 8565A Microwave Spectrum Analyzer and then went on to the IF and display portions of Model 8568A. John's married. For relaxation, he enjoys photography, listening to music, and playing racquet ball.

tinually trying to correct for the YTO tuning failure.

The power of the internal microprocessor can be further enhanced by connecting an external controller such as the Model 9825A Desktop Computer to the analyzer through the HP interface bus. This permits automated testing and alignment procedures (see box).

Troubleshooting the Digital Section

All the troubleshooting aids just described assume that the digital sections are operating properly. The design of the main microprocessor, the display processor, and the HP-IB interface microprocessor permits independent verification and troubleshooting of each. Each has its own test software and can operate independently for testing purposes.

To provide an overall system go/no-go test, two red LEDs were added to the front panel (INSTR CHECK). Whenever the instrument is turned on or the INSTR PRESET key is pressed, the two LEDs are turned on. The main processor then goes through a self check of internal working registers, performs a checksum of the program memory, pattern checks the display memory, and reads the keyboard to verify that there are no stuck keys or stuck I/O lines. If all these checks pass, then the two LEDs are turned off. If a bad bit is detected in the display memory, LED I stays on; if the I/O-keyboard check failed, LED II stays on. Both LEDs' staying on indicates the probability of a failure in the main microprocessor or the program memory.

Grounding an internal test point forces the processing circuits to cycle repeatedly through this test plus an additional RAM test. Monitoring the amount of time spent in each check provides an indication of the particular ROM, RAM, or display storage bit that

failed.

When a problem with the display processor or display memory is suspected (LED I remains on), jumpering two test points enables a special set of test ROMs and disables the normal ROMs. A special CRT test pattern is then displayed, verifying the display processor and memory independently from the main microprocessor, the interface circuits, and the interconnect cable.

Troubleshooting with Signature Analysis

Once a digital failure has been detected and the suspect processor has been identified by the self-check routines, the problem becomes one of finding the faulty IC. This is done with signature analysis, using the Model 5004 Signature Analyzer.[2]

Designing for signature analysis requires very little hardware, but the few items that are required are essential. One of these is a jumper plug to open the feedback from the ROM outputs to the processor so the processor can free-run through all memory locations. The signature analyzer can then be used to verify all ROM outputs by comparing the signature at each output with the known good signature.

Once the ROM and the processor's program counter have been verified and the jumper plug replaced, the ROM programs become the stimulus for testing other devices on the processor bus. Several different stimulus programs are stored in ROM. The first program simply outputs various bit patterns on the bus to check the processor and the output bus. The remaining test programs check, usually one at a time, the other circuits on the bus such as the ALUs, RAMs, displays, keyboard scanners, counters, and so on.

Each test program supplies a synchronous, com-

pletely defined, repetitive stimulus that checks the functions of each circuit under test. The stimulus program cannot, of course, rely on any feedback from the device being tested or any device not previously verified; otherwise, it would not be possible to guarantee that the stimulus signals are valid. However, once the ALU is verified, it can be used to generate the test pattern for the RAMs and this basic "kernel" grows until the entire system is verified or the original fault found.

For each stimulus program, then, feedback paths need to be opened. This can sometimes be done in software by simply ignoring certain bus outputs, but it often requires grounding test points that have been designed in to permit qualifiers, interrupts, and so on to be inhibited. In addition, all asynchronous timing is either inhibited or tested only at times when it can be guaranteed to appear synchronous.

Inputs to the system from external sources have to be defined and preferably stimulated by the processor. Two special test extender boards were designed to break internal feedback paths and connect processor-controlled outputs to the external inputs for each board. This permits a complete check of the entire board, including the interface circuitry.

The only additional hardware required to properly implement signature analysis was the test points for connecting the start, stop, and clock inputs of the signature analyzer.

Troubleshooting Aids

The signatures are documented on multicolored diagrams that are removable from the service manual. Printed in black on these diagrams are the good signatures for the IC pins. A green verification path shows the output signatures that must be checked to verify that the board is operating properly. When a bad signature is located, information in red indicates what IC pins should be probed next to backtrack the fault to its origin. Printed in red next to the signature of an input pin is the IC number and pin number of the source of that input, so backtracking can be performed without continually referring to the schematic. Also printed on the diagram are the setup requirements for the test, such as the jumpers required to enable the stimulus test program and the start, stop, and clock test points for the signature analyzer.

Reference

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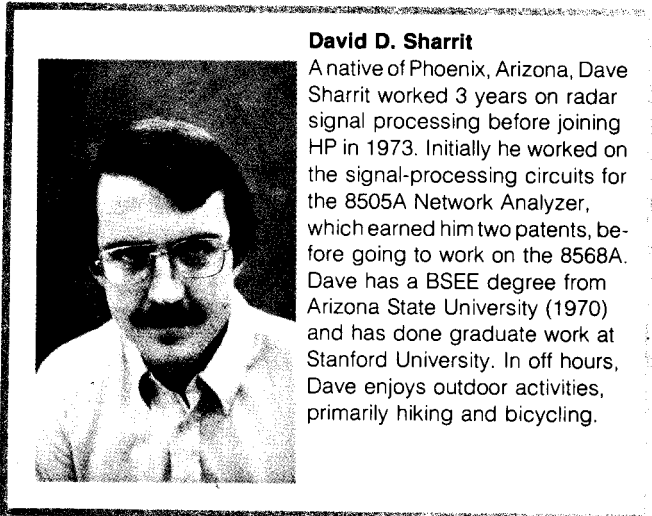
David D. Sharrit

A native of Phoenix, Arizona, Dave Sharrit worked 3 years on radar signal processing before joining HP in 1973. Initially he worked on the signal-processing circuits for the 8505A Network Analyzer, which earned him two patents, before going to work on the 8568A. Dave has a BSEE degree from Arizona State University (1970) and has done graduate work at Stanford University. In off hours, Dave enjoys outdoor activities, primarily hiking and bicycling.

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