SECTION 2 - TROUBLESHOOTING

1. Theory of Operation

A. General

The System Theory of Operation provides general theory of operation information of the ATC-600A-2 with functional analysis of Transponder and DME simulation. The Functional Theory of Operation is a description of the signal flow through the various systems and assemblies in the ATC-600A-2.

B. System Theory of Operation

(1) Transponder Operation (2-2-1, Figure 1)

The PRF for transponder interrogations is generated by the 260 Hz PRF Oscillator (Q101/Q110), an unijunction oscillator, at a fixed rate of 235 pps.

(a) SLS Circuits

The SLS and RF Leveler Assembly provides for attenuation of the P2 Pulse by 9 dB through the 0/OFF/-9 dB SLS Switch. From the XPDR Signal PC Board Assembly, Pin S, the transponder pulses are applied to the two one-shots, X17501A and X17501B.

NOTE: Normally, when the 0/OFF/-9 dB SLS Switch is in the center (OFF) position, only P1 and P3 are present. In the 0 dB (up) or the -9 dB (down) position, P2 is added to the pulse train. This function is performed by the XPDR Signal PC Board Assembly and the 0/OFF/-9 dB SLS Switch through Pin 17 of the XPDR Signal PC Board Assembly.

If the 0/OFF/-9 dB SLS Switch is in the 0dB position, Pin 3 of X17501A is held at a logic 0 level, and X17501A is inoperable. X17501B operates when the 0/OFF/-9 dB SLS Switch is in the 0dB or the -9dB position, but has no effect when the 0/OFF/-9 dB SLS Switch is in the 0dB position. When the 0/OFF/-9 dB SLS Switch is in the -9dB position, +6.5 V is applied to R17504, placing a high level on X17501A Pin 3 and enabling X17501A to also operate on incoming pulses. X17501A is further enabled to operate when X17501B applies a high level to X17501A Pin 2 until X17501B is fired. When the trailing edge of P1 is applied to the one-shots with the 0/OFF/-9 dB SLS Switch in the 0dB position, X17501A does not fire. Q17501 remains off or is nonconducting. If the 0/OFF/-9 dB SLS Switch is placed in the -9dB position, X17501A fires, along with X17501B, on the trailing (negative-going edge) of P1. The approximate time of X17501A is 4 μs. During that 4 μs, the inverted Q of X17501A goes low, causing Q17501 to turn on. The collector of Q17501 goes to +5 V and pulls on the attenuator portion of the leveler, consisting of 132 Ω resistor, 182 Ω resistor, two associated PSO-83B diodes and 76.8 Ω resistor. An adjustment for the amount of signal attenuation is provided by R17519. R17519 is set to provide 9 dB of signal attenuation from the normal (P1 and P3) level. X17501A resets in 4 μs, providing 9 dB of signal attenuation during the P2 pulse time; however, X17501B does not reset for 30 μs to keep X17051A from operating again during the time of the P3 pulse.

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(b) Interrogation

In either A/C interlace mode, the time of the P3 Pulse One-Shot (X103/X114) is altered on a two-to-one basis by the divide-by-three circuit that follows the 260 Hz PRF Oscillator (Q101/Q110). Q103 is on for two PRF outputs and off for one PRF output. Therefore, the timing of the P3 pulse one-shot (X103/X114) is 8 μs for two output PRF cycles and 21 μs for one output PRF cycle, forming the two-to-one A/C interlace pattern. When the P3 pulse one-shot (X103/X114) timing is completed, the output one-shot (X104) is triggered, forming P3 of the interrogation. Positive sync is taken from the A or C portion of the divide-by-three circuit to observe the interrogation pulses referenced to the 8 μs or 21 μs P3 timing. In Mode B, sync is taken from the P2 pulse one-shot (X102/X109) only.

(c) Reply

The reply gating one-shot (X122/X102) is triggered when the P3 pulse one-shot (X103/X114) resets. As the reply gating one-shot (X122/X102) sets, a reset pulse is sent to the XPDR pulse storage register (X121/X101, X108/X105, X109/X110 and X110/X115), output control flip-flop (X106B/X118), altitude register clock control flip-flop (X114B/X107) and the entire altitude register on the Altitude Register PC Board Assembly. The system is cleared to accept new reply pulses. Detected Video Input is applied to Pin A of the XPDR Signal PC Board Assembly and is squared by Q109. If the reply gating one-shot (X122/X102) is set, the pulses are fed to the XPDR pulse storage register. F1 is first to enter and F2 is last to enter.

CLOCK PULSES

The first pulse into the XPDR pulse storage register sets the register clock control flip-flop (X114A/X106). The register clock control flip-flop (X114A/X106), in turn, enables a gate (X119B/X123). The register clock control flip-flop (X114A/X106) also allows pulses from the 20.68 MHz PRF oscillator (Q101/Q110) to be applied to the divide-by-three circuit and to trigger one-shot (X113/X112). The pulses from one-shot are the clock pulses to the XPDR pulse storage register. The clock rate is 1.45 μs, the spacing of the reply pulses.

F1 PULSE

As each reply pulse enters the Test Set, the pulse is clocked into the XPDR pulse storage register as a high (Logic 1) or a low (Logic 0) level. After a maximum of 17 pulses are stored, the first framing pulse (F1) is in the final position. When FI reaches the end of the XPDR pulse storage register, F1 causes the register clock control flip-flop (X114A/X106) to reset, and stop the clock to the XPDR pulse storage register. F1 also enables the NUMERICAL Readout to be unblanked and enables the XPDR % RPLY/DME PRF Meter to show percent reply. When the MODE Switch is set to A/C CODE, the XPDR pulse storage outputs (A1-D4) are applied directly to the NUMERICAL Readout. A set of transistor switches are enabled to decode and display numerically the pilot's code received. When the MODE Switch is set to A/C ALT, the XPDR pulse storage register outputs (A1-D4) are applied to a set of three comparators on the Altitude Register PC Board Assembly.

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ALTITUDE CODE

Resetting the register clock control flip-flop (X114A/X106) when all pulses are loaded into the XPDR pulse storage register, sets the altitude register clock control flip-flop (X114B/X107), which gates an altitude clock frequency to the Digital Display Assembly. On the Digital Display Assembly, a series of four counters start at an altitude (preset) of -1000 feet and count up at the altitude clock frequency rate. Simultaneously, on the Altitude Register PC Board Assembly, the altitude clock is running a counter designed to count in the fashion of the altitude code, a form of Gray Daytex Code. In summary, the counter on the Digital Display Assembly and the counter on the Altitude Register PC Board Assembly clock together, starting at -1000 feet, counting up to 0, and then up to a maximum of +126700 feet. When the counter on the Altitude Register PC Board Assembly reaches the same count (numerically) as the inputs from the XPDR pulse storage register, the comparators enable X202, and the altitude coincidence output is formed. The altitude coincidence output is applied back to the XPDR Signal PC Board Assembly and resets the alt register clock control flip-flop (X114B/X107), stopping the altitude clock, and stopping the counters on the Digital Display Assembly. The counters on the Digital Display Assembly indicate the received altitude. The NUMERICAL Readout, which is blanked during the counting process, is unblanked to display the received altitude.

IDENT PULSE

An IDENT pulse applied to the transponder loads into the last position of the XPDR pulse storage register. The IDENT pulse activates X110/X115 of the XPDR pulse storage register which lights the IDENT PULSE Indicator (SPI). A pulse is applied to the framing pulse control flip-flop (X106A/X118) 5.8 μs before the XPDR pulse storage register is fully loaded. As the framing pulse control flip-flop (X106A/X118) sets, the framing pulse delay one-shot (X107/X119) is triggered. The time of the framing pulse delay one-shot (X107/X119) is varied with the FRAMING PULSE SPACING Control. When the framing pulse delay one-shot (X107/X119) resets, a short pulse, a product of the action of X107/X119 and X117C/X103B is applied to X117C/X103B. The other input to Gate (R124/R137) is the input to the XPDR pulse storage register. The framing pulse delay one-shot (C118/C121) timing is approximately 5.8 μs, which places the input to Gate (X117C/X103B) at the timing of the F2 pulse to the XPDR pulse storage register. If the two are in coincidence, Gate (X117C/X103B) is enabled, setting the output control flip-flop (X106B/X118). When the output control flip-flop (X106B/X118) is set, the F2 PULSE SPACING Indicator is off. If the framing pulse delay one shot (CR117/CR121) time is varied greater or less than the coincidence time of the F2 pulse, the output control flip-flop (CR106/CR121) is not set, and (Q104/Q108) is turned on to light the F2 PULSE SPACING Indicator.

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NO ALT

X106B/X118 through X107/X119 are used to sense pulses present between F1 and F2 of the reply. If no pulses are present, Q113/Q106 is off, which enables X118A/X111C. X118A/ X111C lights the NO ALT Indicator. In Mode A operation (either Mode A only or A/C Interlace) Q113/Q106 is turned on continuously through R140/R150 and CR105/CR126. Any one pulse between F1 and F2 also turns Q113/Q106) on, which turns the NO ALT Indicator off.

INVALID ALT

On the Altitude Register PC Board Assembly, a circuit senses the C1, C2 and C4 pulses. For a received altitude code to be valid, at least one C pulse must be present; however, C1 and C4 cannot be present at the same time in valid altitude code reception. Q213, Q214 and Q215 are inverters for the C1, C2 and C4 pulses. The invalid sensing circuit (Q213 through Q217 and X201) ascertains whether a valid or invalid reply is being received. The output of X201C is high if the received code is invalid.

INTERROGATION SPACING

The timing of P2 and P3 (relative to P1 of the interrogation) can be slewed with the INTERROGATION SPACING Control, which changes the P2 pulse one-shot (X102/X109) timing. Changing the P2 pulse one-shot (X102/X109) timing shifts P2 and P3 together. In Mode A (B), the P3 spacing is set to 8 μs (17 μs) by a separate internal control and is varied, as are the spacings in the A/C interlace modes, with the INTERROGATION SPACING Control.

ALTITUDE ENCODER

When an encoding altimeter is tested through the ALTITUDE ENCODER INPUT Connector, pulse inputs A1-D4 are applied to the Digital Display Assembly where the pulse inputs are routed to the A1-D4 lines coming from the XPDR pulse storage register on the XPDR Signal PC Board Assembly. The pulse inputs simulate transponder operation for the Test Set. Therefore, a transponder cannot be operated while pulses A1-D4 are being processed. The PRF rate (235 pps) is used to initiate the reset, altitude clock and counter action. One pulse, simulating F1, is loaded into the XPDR pulse storage register. All circuitry operates as if a transponder is being tested. The altitude clock causes the counters to find the altitude being applied and to display the correct information. The P3 pulse one-shot (X103/X114) sets the no reply flip-flop (X105A/X106) on each transponder interrogation that contains no reply pulse output. When reply pulses are present, the first pulse (FI) resets the no reply flip-flop (X105A/X106).

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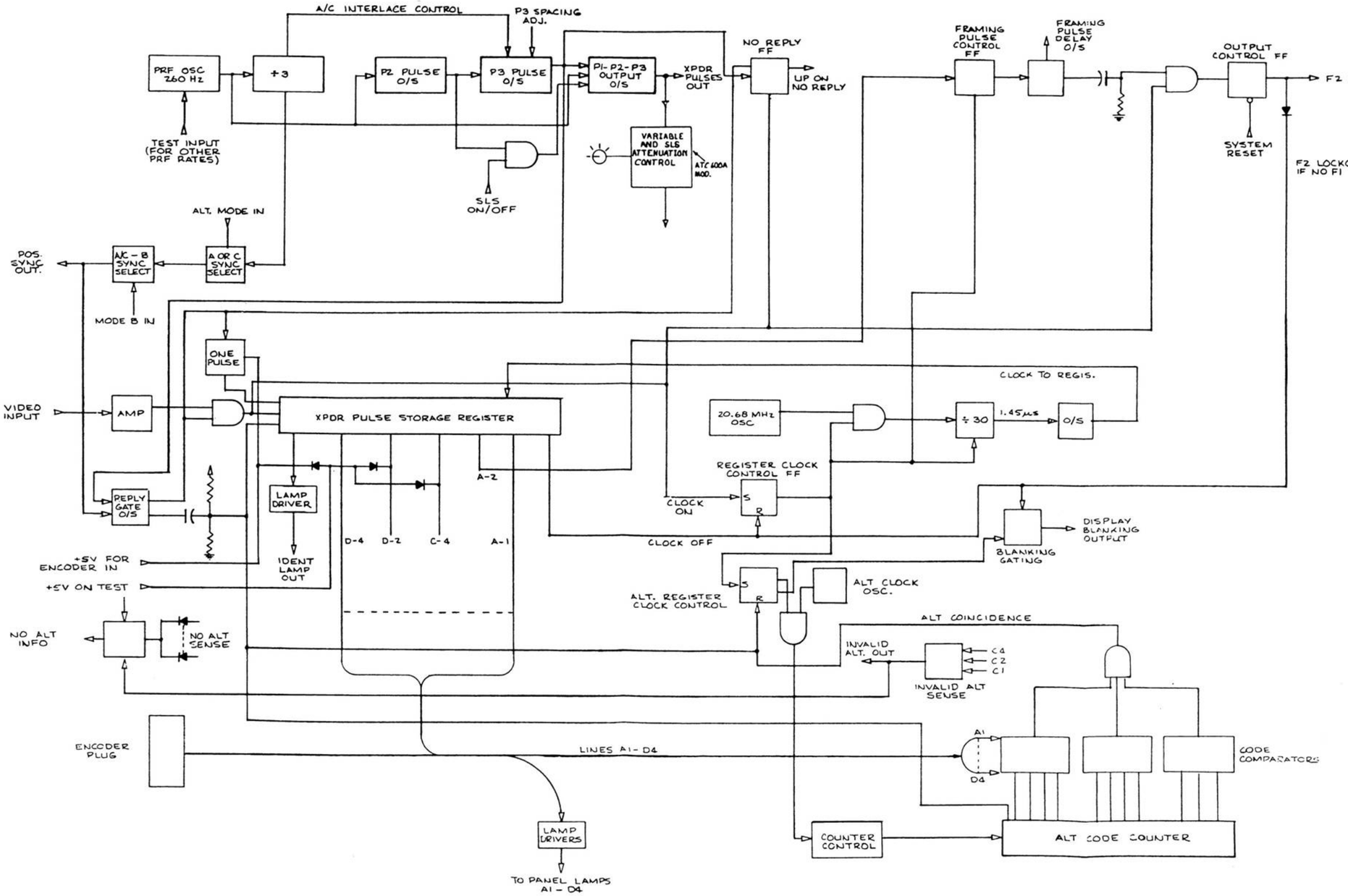

XPDR Block Diagram
Figure 1

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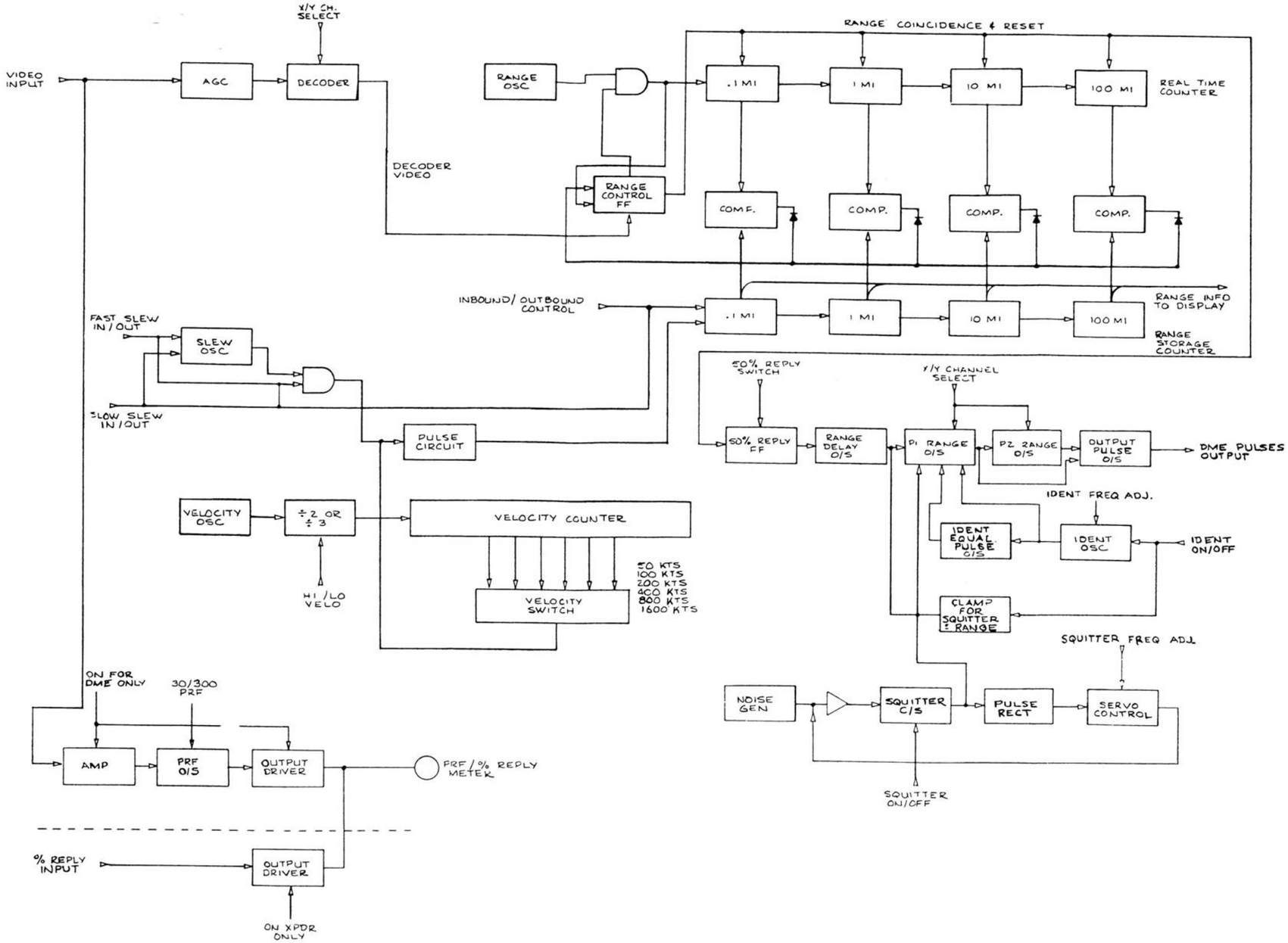

DME Block Diagram
Figure 2

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1030 MHz SIGNAL LEVELING

The RF Frequency/Power Monitor Assembly provides 1030 MHz signal leveling to the diode switch and provide for varying the 1030 MHz signal level from -66 to -79 dBm (with a properly positioned remote test antenna or with a 34 dB pad) through the XPDR SIGNAL LEVEL Control. The signal from the 1030 MHz oscillator is applied to the leveler block, and the RF level is detected by the HP2800 diode. The dc level is applied to the inverting input of X17502. Three trimpots (R17507 [-66 dBm set], R17511 [-79 dBm set] and R17514 [linearity adjust]) and the XPDR SIGNAL LEVEL Control (R17575) set the reference level on the other input of X17502. If the 1030 MHz oscillator is too high, the amplifier output goes more negative and reduces the conduction of the input PSO-83B Diode. This decreases the signal level to the one desired. The XPDR SIGNAL LEVEL Control can vary the reference level to cause output RF levels from the Test Set (including coaxial cable and space loss) to vary from -66 to -79 dBm (with a properly positioned remote test antenna or a 34 dB pad). The output from the SLS and RF Leveler PC Board Assembly is applied to the diode switch.

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(2) DME Operation (2-2-1, Figure 2)

The detected video input is applied to the AGC (Q301-Q304) on the DME Signal PC Board Assembly. FET (Q301) is used as a gain control for the incoming signal. The signal at the collector of Q303 is constant in peak to peak amplitude for a very wide range of input signal levels. This is necessary to assure proper range timing and delay for a variance of DME output powers, antenna installations, etc. The differential transistor pair (Q305 and Q306) sense the 50% point of the input signal from Q303 and form a spike for P1 from Q307 to begin range reply timing. The spike from Q307 is applied to one-shot (X301), which has a time of 9 µs in X Channel and 32.5 µs in Y Channel.

On initial setting, one-shot (X301) applies a negative pulse through C308 as the decoder video output signal. At this time, one-shot (X301) also resets flip-flop (X303A). When one-shot (X301) resets, X302 is set, which has a time of approximately 6 µs (±1.5 µs) from the input pulse spacing of 12 µs in X Channel and 36 µs in Y channel. During the time X302 is reset, the second input pulse (P2) is applied from the AGC . The pulse has no effect on one-shot (X301), except to set X303A. (If P2 is greater or less than approximately 3 µs, X303A is not set). If X303A is set, Q308 is maintained off. If X303A is left reset for an appreciable length of time, Q308 is brought into conduction and clamps out pulses from the decoder output. R322, C308 and R323 form an averaging delay, to prevent Q308 from turning swiftly on and off each time X303A toggles.

(a) Range

The range counter clock consists of a 6.473 MHz oscillator, which produces pulses in 1/80 NM steps. The oscillator includes a crystal (Y1) and Gates (X4C and X4D). The range clock output is gated and inverted by NOR Gate (X1A) into the clock input of X5 Pin 14.

The divide-by-eight output of X5 produces one clock output to X6 for every 0.1 NM. In the Velocity Mode, X5 is preset by X11 via X10, so that one pulse for every eight clock pulses into X5 Pin 14 is detected by X1B, which provides one clock pulse to X3B for every 0.1 NM.

X6 through X8 are serially connected divide-by-ten down counters with BCD inputs. X9 is a binary output four-bit ripple-down counter connected in series to X8. X6 through X9 are preset to the desired range output delay by the output lines of X13-X16.

When the range count of X6-X9 reaches zero, MIN pulses from X6-X9 Pin 12 are sent to the inputs of NAND Gate (X2). Pin 8 of X2 goes low and, after being inverted by X1C, pulls Pin 7 of X3B up, enabling X3B to be clocked.

As X5 reaches a count of zero, Pin 8 of X1B goes high. The next clock pulse on X5, Pin 14 clocks X5 away from zero, causing X1B, Pin 18 to go low. This high to low transition clocks X3B through Pin 5. X3B Pin 9 clocks X3A, which brings X3A Pin 12 to the high state. This is the end of range output. The same high output state on X3A Pin 12 is sent to X1A Pin 3, causing that NOR Gate to change state and halting the down counting of the range counters X5-X9. The inverted Q output of X3A is used to reset X3B. X3A is reset by the next range start input on the Range/Velocity PC Board Assembly, Pin 17. When the inverted Q of X3A goes low, the load lines of X5-X9 are pulled low, and X5-X9 are again loaded with the outputs of X11 and X13-X16.

(b) Velocity

A 6.990506 MHz oscillator (Y2 and X18) provides a conditioned clock pulse to X19 Pin 14. X19 acts as a divide-by-eight counter, with the output going to X20A and X20B.

Depending on the state of the HI/LO VELOCITY Line, X20 acts as a divide-by-three or a divide-by-two counter. When the LO Velocity Range is selected on the VELOCITY HI/LO RANGE Switch, X20B Pin 6 is pulled high by R12, allowing X20B to be cloaked on Pin 5. The Q output of X20B provides a gating pulse to X20A Pin 14. One output pulse results on X2CA Pin 13 for every three clock pulses that enter X20A Pin 1.

When the HI Velocity Range is selected on the VELOCITY HI/LO RANGE Switch, Pin 6 of X20B is pulled to ground, shutting off X20B. The Q output of X20B goes high, allowing X20A to toggle normally. (X20A acts as a divide-by-two counter.)

X21 is a CMOS 12-stage ripple-up counter that provides one output pulse on Pin 1 for every 4096 input pulses on Pin 10. The output at X21 is used as the 2400/1600 knots velocity rate clock output to clock X17.

The divide-by-2, divide-by-1, divide-by-8, divide-by-16 and divide-by-32 outputs of X17 are used as the 1200/800, 600/800, 300/200, 150/100 and 75/50 knots velocity rate clock outputs.

In the Velocity Mode, one of the velocity rate clock outputs is returned to the Range/Velocity PC Board Assembly, Pin 18 via the DME RANGE/VELOCITY Switch. The velocity rate clock goes to the base of drive transistor Q1. The output of Q1 is conditioned by Schmitt trigger X18E to provide negative clock pulses to the synchronous up/down counters X11 and X13-X16.

When the Range/Velocity PC Board Assembly is first turned on, a reset circuit (C4, R6 and R5) provides a brief low state on the load line of X11 and X13-X16, resetting X11 and X13-X16 to a count of zero.

X11 is a synchronous up/down four-bit binary counter. X11 Pin 13 provides one ripple clock output to X16 Pin 4 for every 16 clock pulses on the clock line. In the Velocity Mode, X11 Pins 6 and 7 provide a preset signal for X5. The preset in the VELOCITY Mode causes the range output pulses to step in increments of 0.025 NM.

X16, X13 and X14 are synchronous up/down counters with BCD (binary-coded decimal) outputs. X16 accepts the ripple clock gating input from X11, and the clock pulses from the clock line, to provide a BCD output to X12. In the Velocity Mode, this BCD is selected by X12 and updates the programming on the 0.1 NM range counter (X6). X16 Pin 13 also outputs one enable pulse to X13 for every ten clock pulses received by X16 Pin 4.

X13-X15 operate in a similar manner as X16, updating the programming on the 1.0, 10 and 100 NM range counters, with the exception that X15 has a binary output.

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(c) 50% Reply

The range output pulse is applied to the 50% reply flip-flop (X367-B) and to Gate X304 on the DME Signal PC Board Assembly. In normal operation, the 50% reply flip-flop (X303B) is held reset, and all input signals are passed directly through Gate X304 to the range delay one-shot (X305). If the IDENT/50% RPLY Switch is in the 50% RPLY (down) position, the 50% reply flip-flop (X303B) toggles on the input signal and inhibits Gate X304 on every other input pulse. Only every other input signal fires the range delay one-shot (X305). The range delay one-shot (X305) sets the P1 range one-shot (Q310 and Q311) for the precise time of 50 μs in X Channel (56 μs in Y Channel), providing the proper range delays. When the P1 range one-shot (Q310 and Q311) resets and fires the output pulse one-shot (X307) for 3.5 μs, P1 pulse of the reply is produced. When the P1 range one-shot (Q310 and Q311) resets again and P2 range one-shot (X306) is set. After 12 μs in X Channel (30 μs in Y Channel), the P2 range one-shot (X306) resets, firing the Output Pulse One-Shot (X307) again for 3.5 μs (nominal) and forming the P2 pulse of the reply. Q309 assures that the collector of Q310 is pulled up on initial firing of the P1 range one-shot (Q310 and Q311). This assures accurate, repeatable timing of the critical 50 μs (or 56 μs) range delay.

(d) IDENT Tone

The IDENT Tone is activated when the IDENT/50% RPLY Switch is in the IDENT (up) position. When the IDENT/50% RPLY Switch is activated, +11 V is applied to the IDENT oscillator (X311). The IDENT oscillator (X311) output fires the P1 range one-shot (Q310 and Q311), initiating the P1 and P2 reply pulses (as though for a range reply). Each time the IDENT oscillator (X311) puts out a signal, X311 also fires the IDENT equalizing pulse one-shot (X308), which is set for 100 μs. When the IDENT equalizing pulse one-shot (X308) resets, X308 fires the P1 range one-shot (Q310 and Q311), causing the second pulse pair (P1 and P2) to appear in the output. The second pulse pair is spaced 100 μs from the first pair.

(e) Squitter

When +11 V is applied to the IDENT oscillator (X311), +11 V is also applied to the squitter/range clamp (Q312 and Q313), which clamps out all squitter input and range reply pulses. When the IDENT tone is on, no squitter or reply pulses should appear in the output. Squitter is generated by using a zener diode (ZD301) as a noise source. The zener noise is further amplified by a noise generator (Q314, Q315 and Q316). The noise signal in the emitter of Q316 operates the squitter one-shot (X309) on a controlled basis. The squitter one-shot (X309) output triggers the reply one-shots and operates driver Q318. The output is rectified by the pulse rectifier (CR316 and CR317). The average dc level of the pulse rectifier (CR316 and CR317) is filtered and applied to the servo control (X310). The reference level for the servo control (X310) is set by the squitter frequency adjust (R375). As the squitter frequency varies, the dc rectified level varies, changing the output level of the servo control (X310). The servo control (X310) controls the bias to Q317. C329 regulates an average dc level to the servo control (X310). Squitter frequency averages 2700 Hz at the squitter one-shot (X309) output over a long period of time. Squitter is turned on and off when the squitter one-shot (X309) is enabled or disabled.

(f) DME PRF

Output pulses from the XPDR Signal PC Board Assembly and the DME Signal PC Board Assembly are applied to the Regulator/Timer PC Board Assembly, to operate the Q521 and Q522 modulators. The output from Q522 is applied to the diode switch to turn the RF on and off to form output pulses. DME PRF is measured through Q520 and X503, detecting RF input video. (This circuit is used in DME Mode only.) The one-shot timing is changed to switch between the two PRF ranges (0-30 and 0-300 pps). Q519 is the meter driver.

(g) Slew Operation

When outbound slew is selected by the SLOW SLEW Switch or FAST SLEW Switch, Pins V and 3 on the Range/Velocity PC Board Assembly go low. All other slew inputs float up. With Pin 3 on the Range/Velocity PC Board Assembly low, X22B Pin 6 is high, turning off CRI, and allowing the base of Q2 to be pulled to +5 V by R8. One end of C14 is grounded through the SLOW SLEW Switch. Q2, C11 and C14 are the sources for the slow slew clock.

When SLOW SLEW Switch is set to IN (up) position and VELOCITY IN/OUT Switch is set to IN (up) position, Pin 2 on the Range/Velocity PC Board Assembly is grounded and Pin 3 on the Range/Velocity PC Board Assembly floats up. X22C Pin 8 is low, causing X22D Pin 11 to go high. With X22D Pin 11 high, X11 and X13-X16 count down.

FAST SLEW IN or OUT is similiar to SLOW SLEW IN, with the exception that one side of C14 is no longer connected to ground. The frequency of the slew oscillator is determined by the value of C11 alone.

(h) Range Mode Operation

When Range Mode is selected, the velocity outputs are disabled at the DME RANGE/VELOCITY Switch. X11 and X13-X16 may be manually slewed to the desired range, using the SLOW SLEW Switch or FAST SLEW Switch.

In Range Mode, Pin 1 on the Range/Velocity PC Board Assembly is held to ground. With Pin 1 on the Range/Velocity PC Board Assembly at ground, the outputs of X10C and X10D remain low, programming X5 to start counting at zero.

X12 Pin 1is held to ground in the Range Mode, causing X12 to select data from Pins 2, 5, 14 and 15, which are tied to ground. With this data selected, the lines to the 0.1 NM digit are held down, and the digit displays only a 0. This presents a zero input to X6. With X5 and X6 both having 0 as the input, the Range Mode steps in units of 1.0 NM, instead of units of 0.025 NM.

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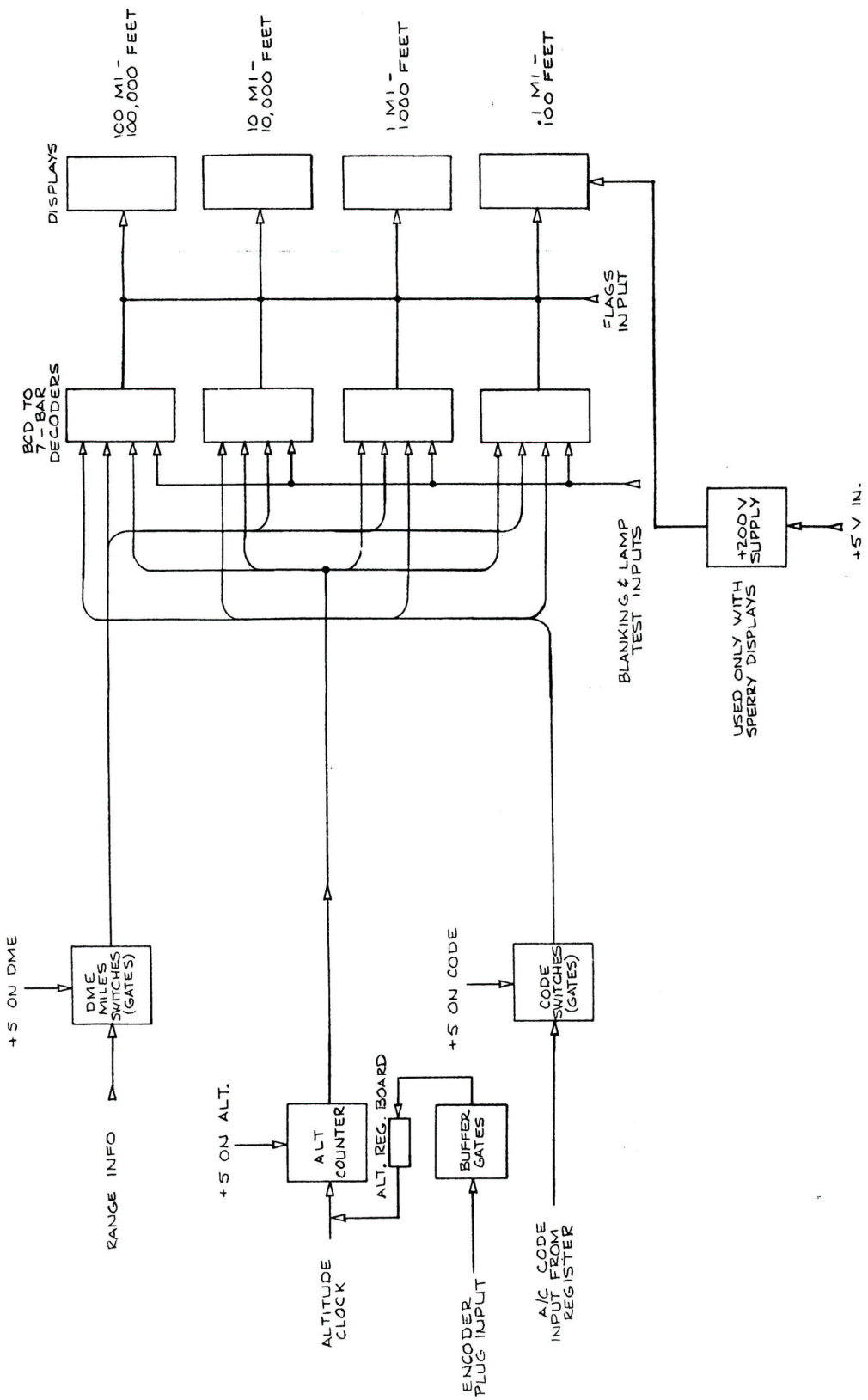

Display Block Diagram
Figure 3

C. Functional Theory of Operation

(1) Display (2-2-1, Figure 3)

The Digital Display Assembly consists of four 7-segment LED displays and one CPLD for decoding/driving the displays. There are three sources of input to the decoder/driver. The code input in A/C CODE Mode and the altitude counters output in A/C ALT Mode give transponder input to the decoder/driver. In DME Mode, range information is applied to the decoder/driver to show range in 0.1 NM increments.

NOTE: Even though range is displayed in 0.1 NM increments, the range in Velocity Mode is actually counted-up in 0.25 NM steps.

When the ALTITUDE ENCODER INPUT Connector is used, the connector input line pulses are gated through the Digital Display Assmebly and back onto the code lines that come from the XPDR pulse storage register on the XPDR Signal PC Board Assembly.

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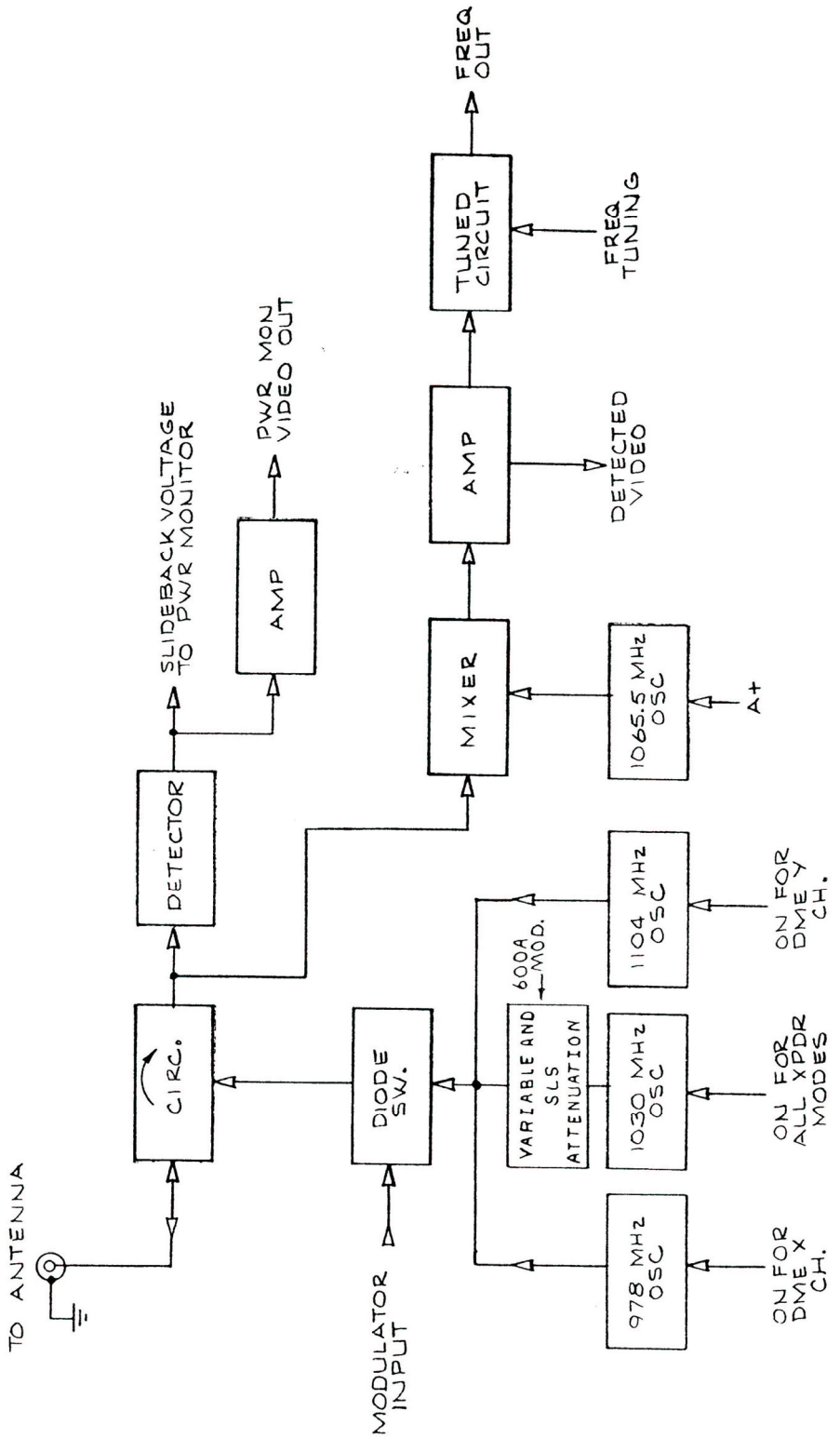

RF Section Block Diagram
Figure 4

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(2) RF Section (2-2-1, Figure 4)

Three oscillators - a 1030 MHz for transponder interrogations, a 978/979 MHz for DME 17X/18X Channel replies and a 1104 MHz for DME 17Y Channel replies are incorporated in the RF Oscillators Assembly to generate RF output. A separate 1065.5 MHz oscillator is used primarily in the RF section to beat against the input frequency of the UUT. All the oscillators are identical except for the 17X/18X oscillator, which has two crystals. When Channel 17X is selected, +11 V power is applied to E2 (J8 Pin 8) and E3 (J8-3). When 18X is selected, +11 V power is applied to E1 (J8-9) and E3 (J8-3) through the DME CHANNEL Switch (S8).

The oscillator (Q1501) frequency is determined by one of the crystals (Y1501 or Y1502). CR1501 enables the oscillator's feedback current through Y1501 in Channel 17X. CR1502 enables the oscillator's feedback current through Y1502 in Channel 18X. The oscillator output is buffered and amplified by Q1502 and Q1503. The output of the buffer drives a multiplier. The fundamental frequency (97.8 or 97.9 MHz) is multiplied by 10 to produce the final output frequency at CRI2001. Z12001 is a bandpass filter tuned to the 10th harmonic of the oscillator. L1505 and C1515 form a tank circuit tuned to the fundamental frequency. When Channel 17Y is selected, +11 V power is applied to J8-4 and sent to the 1104 oscillator. The 1030 oscillator has 11 V power applied when the MODE Switch (S20) is in any XPDR mode. Each single crystal-controlled oscillator, tuned for peak output and proper frequency by L702, drives amplifiers Q702 and Q703. The output of Q702 and Q703 is peaked by L704 and C711 and is applied to the snap diode (CR701, CR702, or CR703). A two-sectioned, tuned filter (filter cavities) on each oscillator picks off the 10th harmonic of the crystal frequency and applies the 10th harmonic to the output connector of the RF Oscillators Assembly.

The outputs of the three oscillators on the RF Oscillators Assembly are summed in the Diode Switch Block Assembly. Only one of the oscillators in the RF Oscillators Assembly operates at one time. The 1065.5 MHz oscillator operates continuously. The video input to the Diode Switch Block Assembly is used to modulate the RF output of the selected RF oscillator into a series of DME or XPDR RF pulses. The output of the Diode Switch Block Assembly is applied through the circulator to the RF INPUT/OUTPUT Connector. Incoming RF is processed by RF Frequency/Power Monitor Assembly through CR801 and CR802. CR801, in conjunction with associated circuitry, acts as an input power detector. The power measuring circuit on the Regulator/Timer PC Board Assembly provides a slide-back voltage for constant power readings. The detected power monitor video from CR801 is amplified by Q801 and is applied to the power circuit on the Regulator/Timer PC Board Assembly. On the Regulator/Timer PC Board Assembly, the detected power monitor video is applied to the power monitor one-shot (X501). The output of the power monitor one-shot (X501) operates the pulse integrator (Q517) and the power calibrate (X502B). The detected power monitor video fires the power monitor one-shot (X501) until the output of the power calibrate (X502B) becomes great enough to reverse the bias on CR801. A bias reverse on CR801 stops the power monitor one-shot (X501). The voltage at the output of the power calibrate (X502B) is applied to the FREQ/PWR Meter for power measurement.

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(2) RF Section (cont)

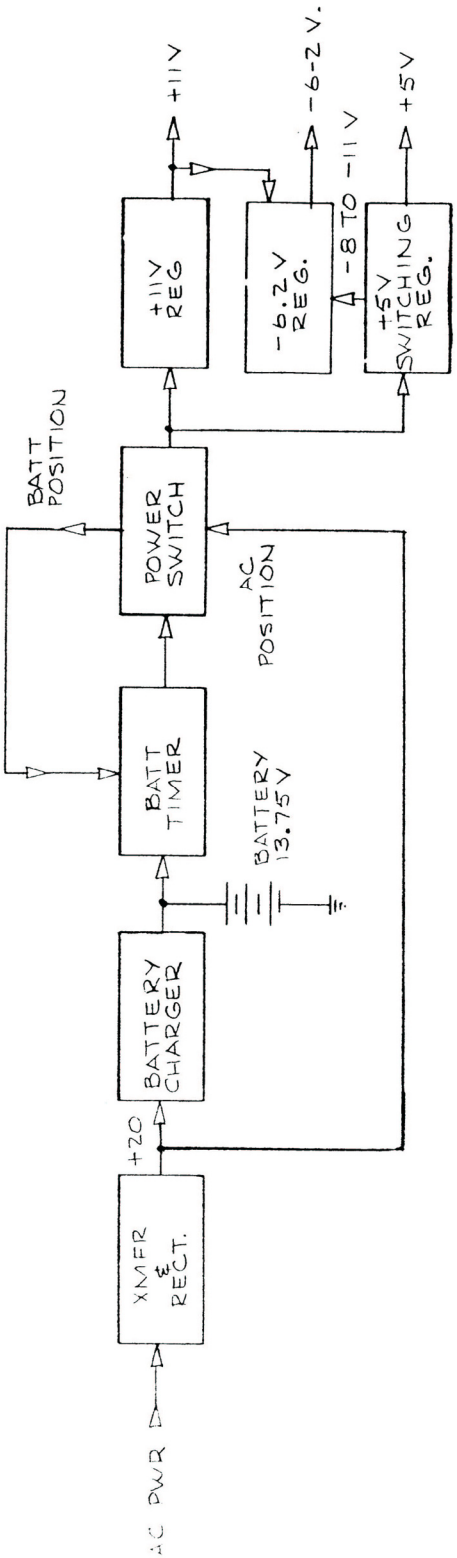
For frequency measurement, the incoming RF is applied through CR802 and is combined with the output of the 1065.5 MHz local oscillator. The resultant signal is amplified by Q802 and is applied to an Amplifier Q803. The signal is then routed through a tuned circuit (L803, C808, C809 and C810). The capacitance of C808 is adjusted by the XMTR FREQ Control and is varied until the tuned circuit is tuned to the incoming RF signal from Q803. The output peaks at that time and is applied to the Regulator/Timer PC Board Assembly, amplified by Q518 and X502A, and then applied to the FREQ/PWR Meter. The detected video from the incoming RF is processed through Q802 and separated for DME and XPDR inputs. DME detected video is routed through R809 and C813 to the video input (Pin 4) on the DME Signal PC Board Assembly for decoding and processing. The XPDR detected video is routed through L807 and C814 to an Amplifier (Q805). The signal at the collector of Q805 is then routed to the detector input (Pin A) on the XPDR Signal PC Board Assembly for processing.

(3) Power Supply (2-2-1, Figure 5)

Power for the Test Set comes from two sources: an external ac source (115 or 240 V) or a built-in battery of 13.2 V (2.0 A/Hr) capacity. Both power sources are mounted on the Power Supply Assembly.

AC power is converted by a transformer and a rectifier to +20 Vdc whenever the Test Set is connected to an external ac source. There is no ac line switching in the Test Set. The +20 Vdc is applied continuously to the Battery Charger circuit on the Regulator/Timer PC Board Assembly. Whenever the Test Set is plugged into external ac power, the battery is being charged. The charger is self-limiting to charge a discharged battery at a high rate and to trickle-charge a fully-charged battery. In ac operation, the +20 Vdc is applied by the PWR/BAT Switch to the Regulator/Timer PC Board Assembly and to the 5 Volt Regulator PC Board Assembly. On the Regulator/Timer PC Board Assembly, the +20 Vdc is regulated to +11 V and is applied to the +11 V. +11 V is also internally applied on the Regulator/Timer PC Board Assembly to the -6.2 V regulator. Negative voltage developed by the +5 V regulator is also applied to the Regulator/Timer PC Board Assembly and is dropped to -6.2 V. The +5 V within the Test Set is applied at all times the Test Set is energized.

When the Test Set is powered by the battery, a timer of approximately 8 minutes performs the actual power switching. When the PWR/BAT Switch is pressed down once, the timer is activated and the battery voltage is applied to the remainder of the power system. After approximately 8 minutes, the Test Set shuts off. Pressing the PWR/BAT Switch a second time turns the Test Set off before the timer runs out.



Power Supply Block Diagram
Figure 5

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