APPENDIX C - PAL EQUATIONS

1. Equation Definitions

   $\overline{XXX}$ =Active Low Signal

   * =AND

   → =Go To

   / =Invert

   : =On Clock Rising Edge

   + =OR

2. Digital IF PC Board Assembly

   A. Digitizer Control PAL (U26015)

      (1) Pin Assignments

PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	CLK1	6	A14	11	OE	16	DRDY
2	CLK2	7	A15	12	DIG CLK	17	RAM WR
3	DS	8	TRIG	13	LOWB	18	RAMQ
4	STRB	9	RCO	14	NC	19	RAMI
5	A0	10	GND	15	ENA	20	V_{CC}

      (2) Equations

      DIG CLK =/NC*/RAM WR*CLK2 + NC + RAM WR

      LOWB =/(/A14*A15*/STRB*/DS)

      NC :=RCO + NC*TRIG

      ENA :=/(RAM WR*NC + /ENA*NC)

      DRDY :=/[RAM WR*ENA + /DRDY*/(/A14*A15*/STRB*/DS)*TRIG]

      RAM WR :=NC

      RAMQ =CLK2*/NC*/RAM WR + (NC+RAM WR)*/(A0*/A14*A15*/STRB*/DS)

      RAMI =CLK2*/NC*/RAM WR + (NC+RAM WR)*/(/A0*/A14*A15*/STRB*/DS)

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B. DSP External RAM Access/System Interface PAL (U26016)

(1) Pin Assignments

PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	IS	6	R/$\overline{W}$	11	A15	16	DPCS
2	STRB	7	A10	12	DPOE	17	SROE
3	DS	8	A11	13	RDYCS	18	SRWE
4	BUSY	9	A14	14	READY	19	SRCS
5	Q	10	GND	15	J	20	V_{CC}

(2) Equations

DPOE =/(A15*A14*/DS*/STRB*(R/$\overline{W}$)]

RDYCS =/[/IS*/STRB*/(R/$\overline{W}$)]

READY =(/IS + DS*IS + /DS*/A15 + /DS*A15*/A14 + Q)*BUSY

J =A15*A14*/DS

DPCS =/(A15*A14*/DS)

SROE =/[/A15*/A11*A10*/DS*/STRB*(R/$\overline{W}$) + /A15*A11*A10*/DS*STRB*(R/$\overline{W}$)]

SRWE =/[/A15*/A11*A10*/DS*/STRB*/(R/$\overline{W}$) + /A15*A11*A10*/DS*STRB*/(R/$\overline{W}$)]

SRCS =/(/A15*A11*A10*/DS + /A15*A11*/A10*/DS)

3. Front Panel Pulse PC Board Assembly

A. LCD Control PAL (U27029) Pin Assignments

PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	NC	8	NC	15	NC	22	NC
2	CLK0	9	IO CH RDY	16	R83	23	ARDY
3	BALE	10	RESET	17	E	24	DIR
4	$\overline{WR}$	11	$\overline{BMCS0}$	18	R/W	25	$\overline{MEMR}$
5	$\overline{RD}$	12	R81	19	NC (Q2)	26	$\overline{MEMW}$
6	DT/RN	13	R82	20	NC (Q1)	27	NC (WAIT)
7	$\overline{PCS5}$	14	GND	21	NC (Q0)	28	V_{CC}

B. LCD Control PAL (U27029) Equations

E :=/Q2*Q1 + Q2*/Q1 + Q2*/Q0

R/W =/(DT/RN)

Q2 =Refer to Appendix C, 3C.

Q1 =Refer to Appendix C, 3C.

Q0 =Refer to Appendix C, 3C.

ARDY=/(/WAIT + /IO CH RDY)

DIR =/(/$\overline{\text{BMCS0}}$ */$\overline{\text{RD}}$)

$\overline{\text{MEMR}}$ =/(/$\overline{\text{BMCS0}}$ */$\overline{\text{RD}}$)

$\overline{\text{MEMW}}$ =/(/$\overline{\text{BMCS0}}$ */$\overline{\text{WR}}$)

WAIT :=/Q2*/Q1*/Q0 + Q2*Q1*Q0

C. LCD Control PAL (U27029) Wait State Assignments

S0 =/Q2*/Q1*/Q0 (000) S0 :=COND1 →S1 + →S0

S1 =/Q2*/Q1*Q0 (001) S1 :=COND0 →S0 + →S2

S2 =/Q2*Q1*/Q0 (010) S2 :=COND0 →S0 + →S3

S3 =/Q2*Q1*Q0 (011) S3 :=COND0 →S0 + →S4

S4 =Q2*/Q1*/Q0 (100) S4 :=COND0 →S0 + →S5

S5 =Q2*/Q1*Q0 (101) S5 :=COND0 →S0 + →S6

S6 =Q2*Q1*/Q0 (110) S6 :=COND0 →S0 + →S7

S7 =Q2*Q1*Q0 (111) S7 :=COND0 →S0 + →S7

Conditions:

COND0 =RESET + PCS5

COND1 =/PCS5*(/WR+/RD)

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