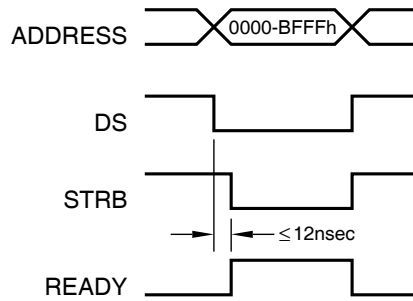
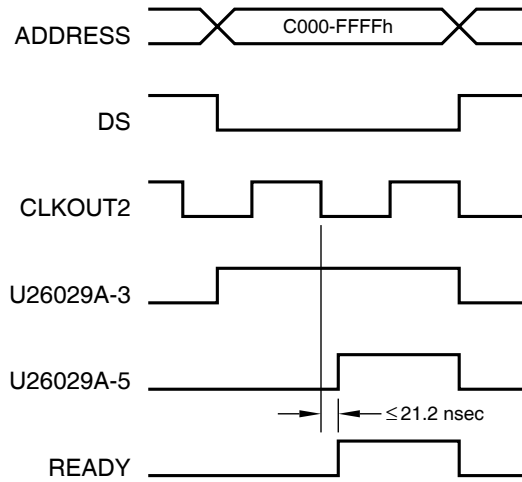


APPENDIX D - TIMING DIAGRAMS



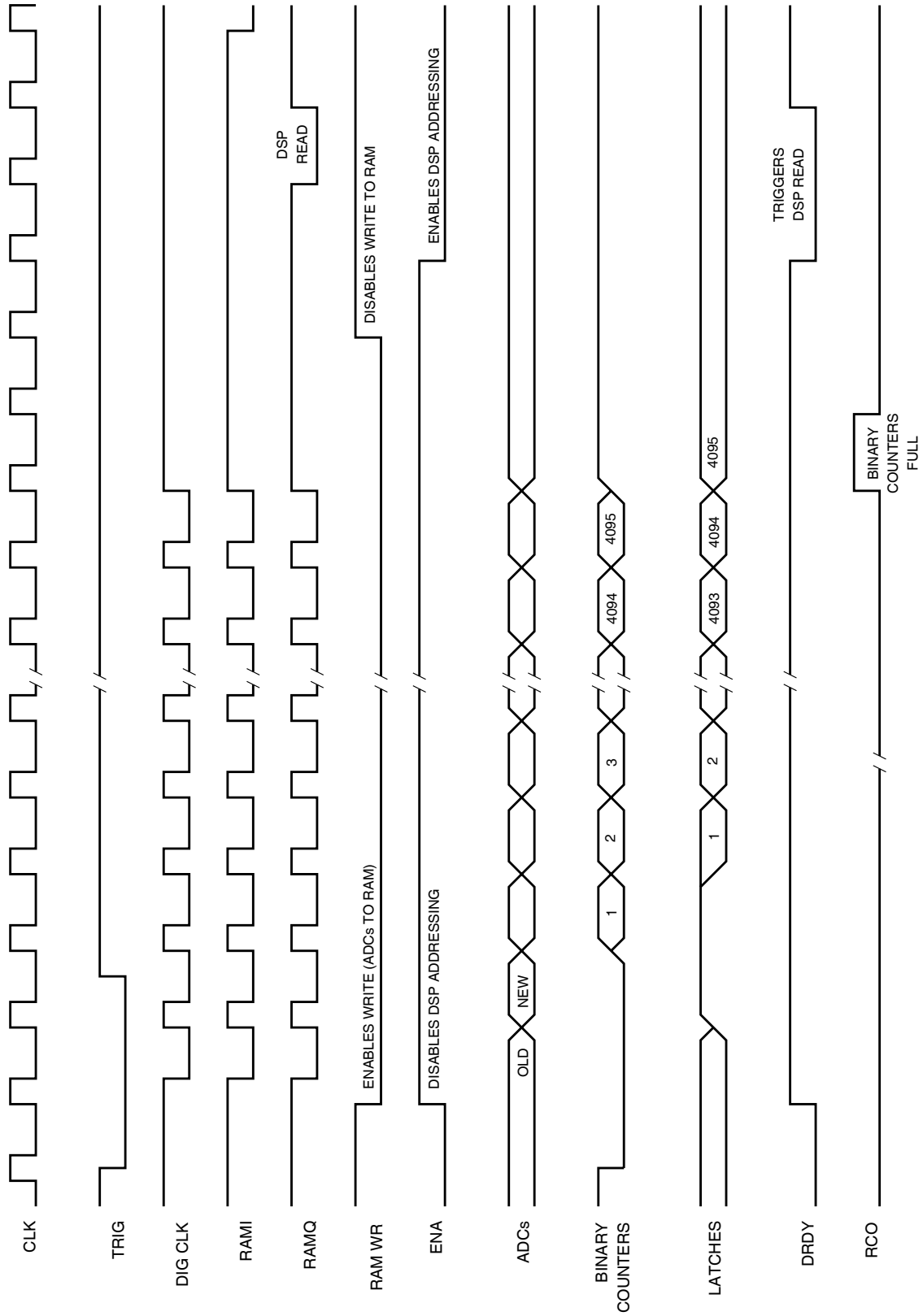
0 WAIT STATES



1 WAIT STATE

8514011

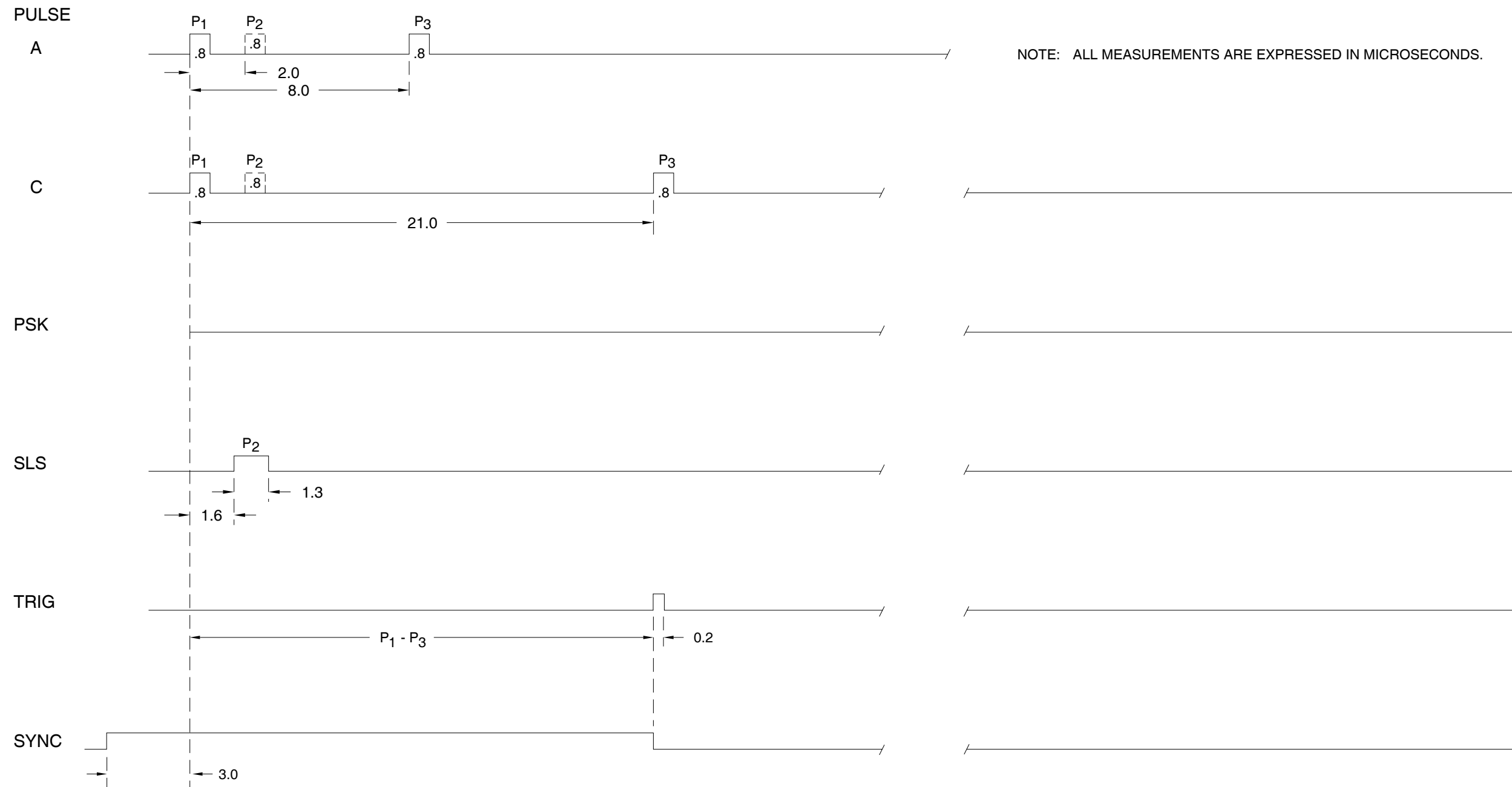
System Interface PAL Wait States
Figure 1



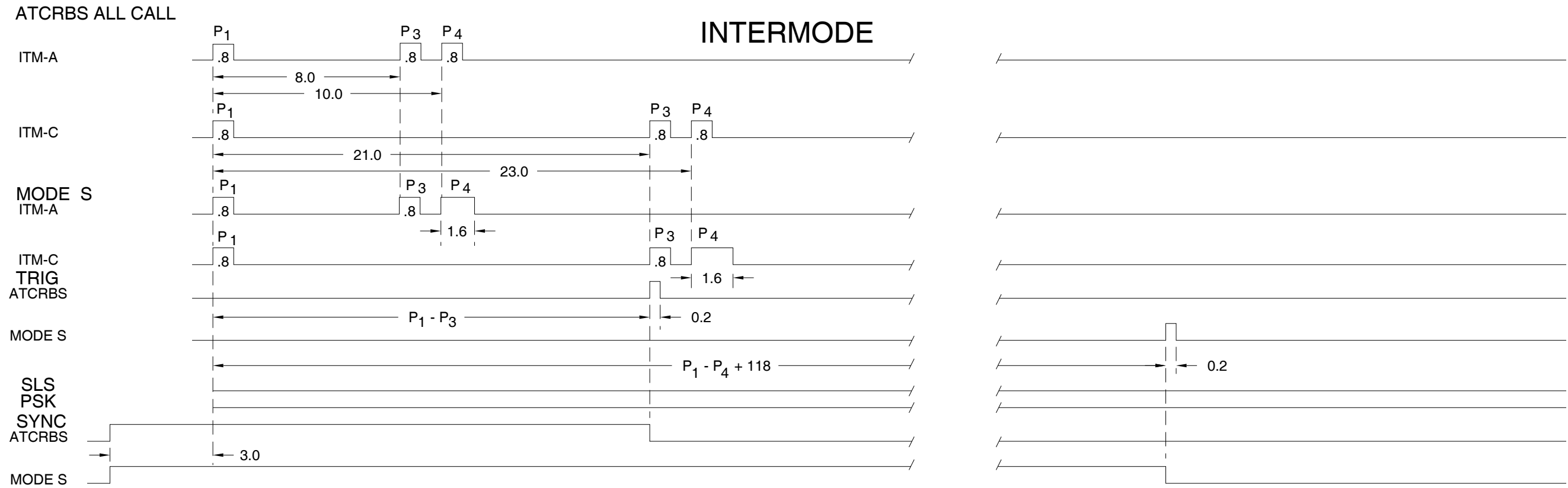
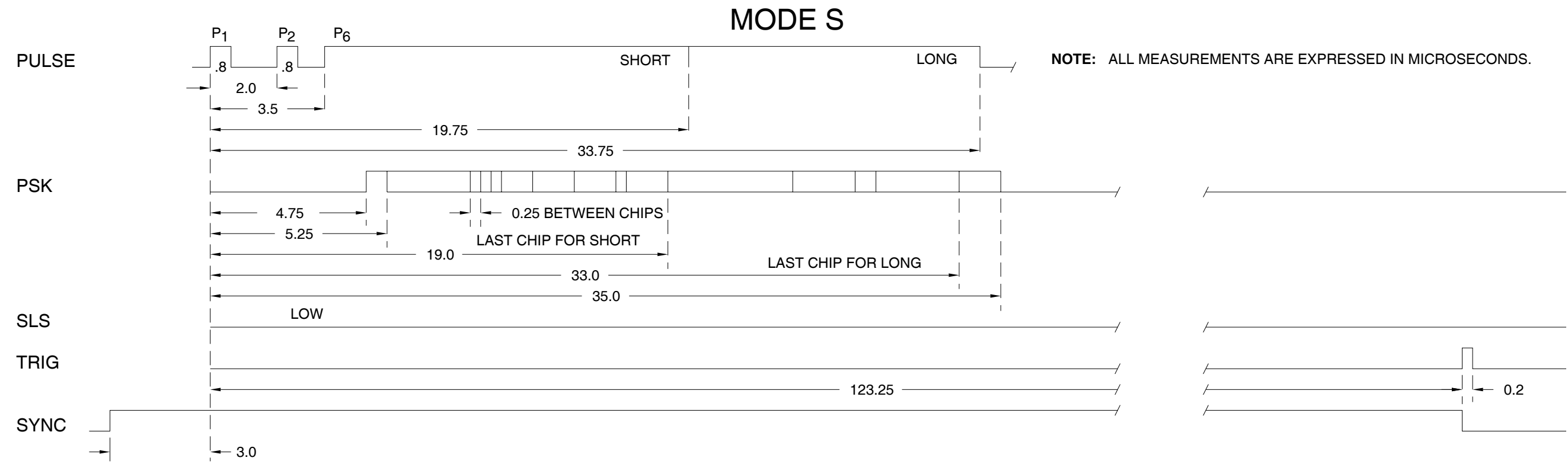
8514006

Digitizer
Figure 2

ATCRBS

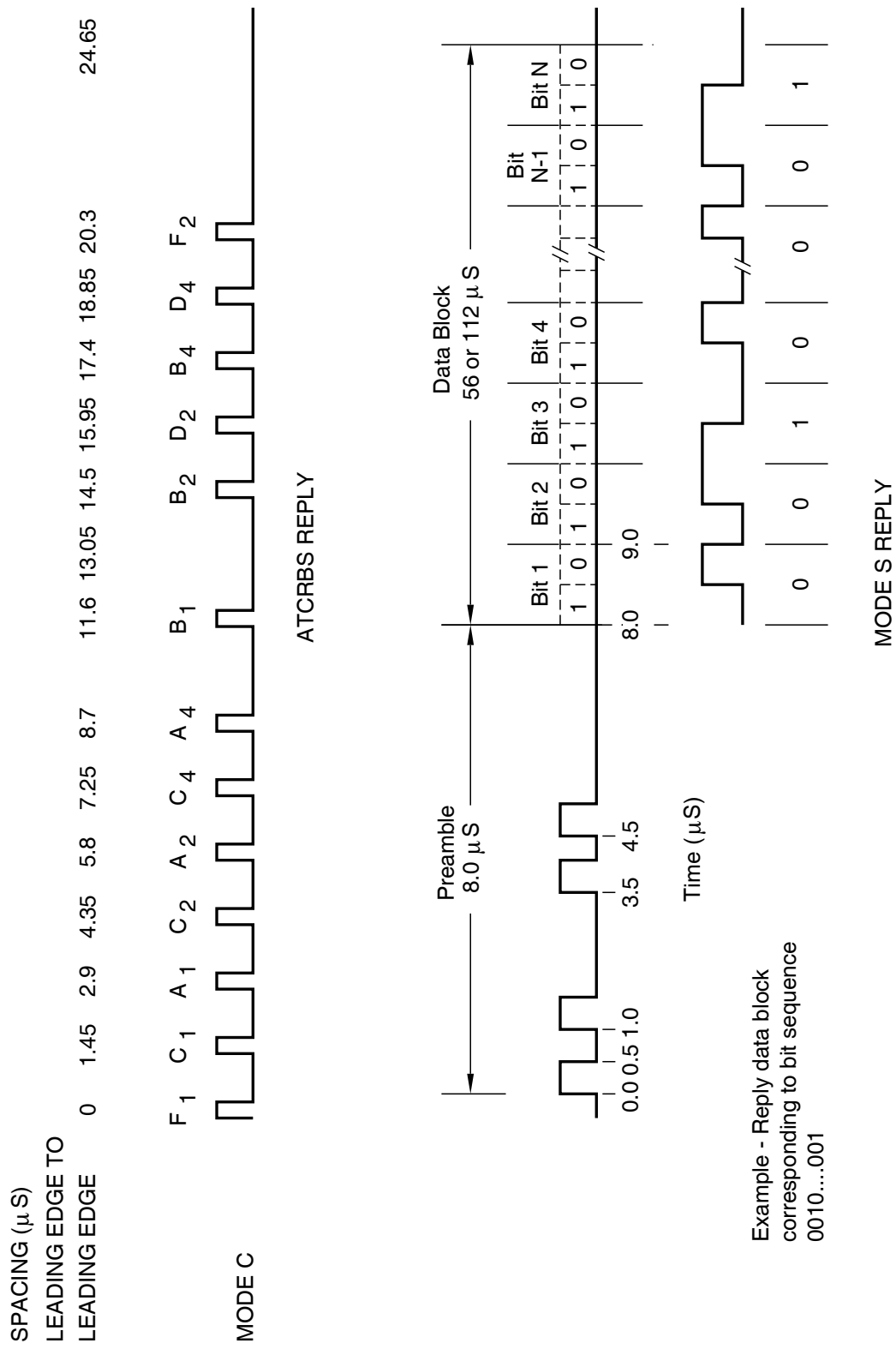


8114007
ATCRBS Interrogation Sequence
Figure 3

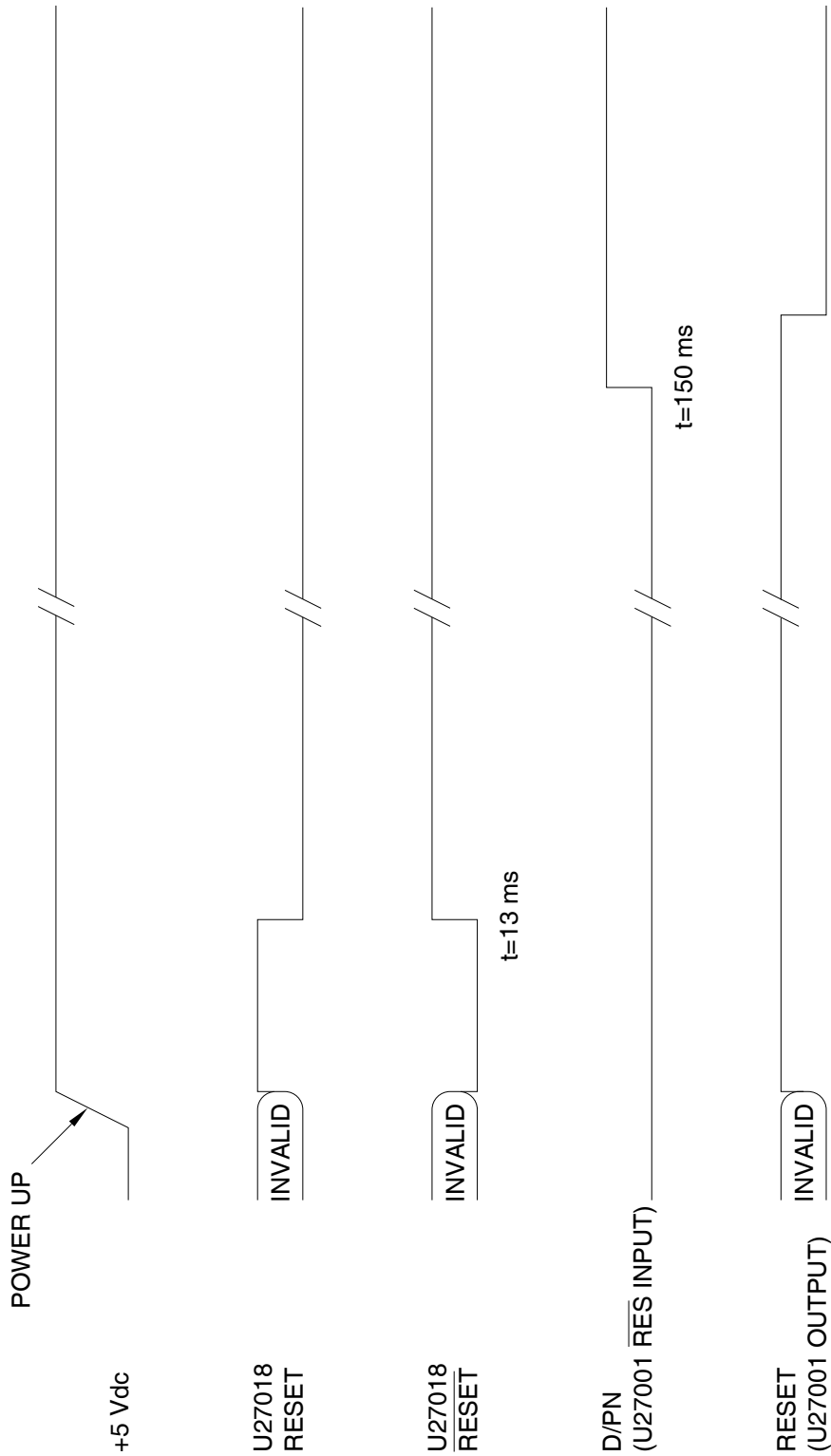


Mode S/Intermode Interrogation Sequences
Figure 4

8114006

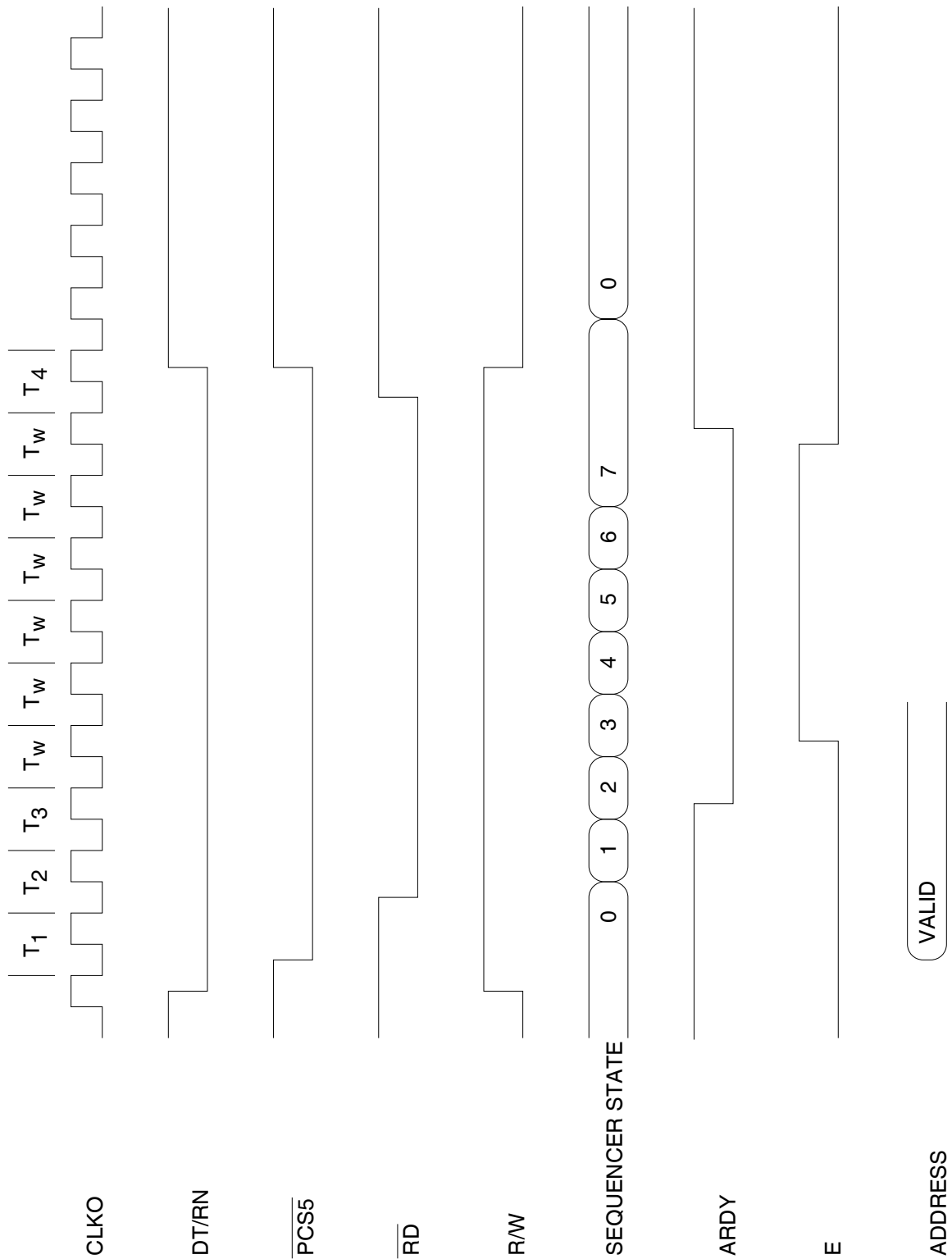


ATCRBS/Mode S Replies
Figure 5



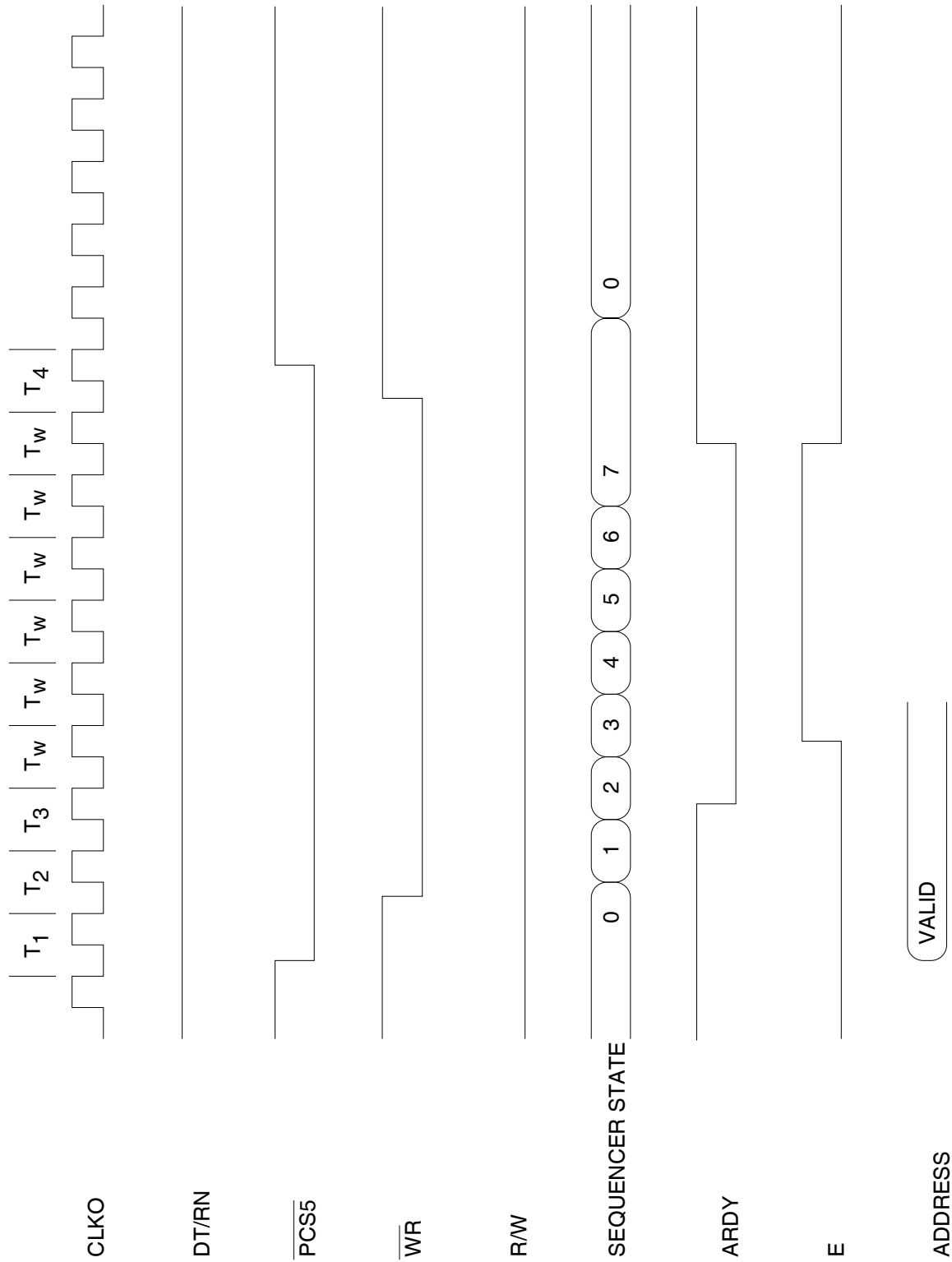
LCA Components Reset
Figure 6

NOTE: LCA COMPONENTS ARE DONE PROGRAMMING AT $t=150\text{ ms}$. EITHER COMPONENT HOLDS D/PN LOW. BOTH MUST BE FINISHED PROGRAMMING FOR D/PN TO GO HIGH.



LCD Read Cycle
Figure 7

NOTE: T_w IS WAIT STATE.



LCD Write Cycle
Figure 8

NOTE: DT/RN IS HIGH WHILE R/W IS LOW.
 T_w IS WAIT STATE.