SECTION 2 - TROUBLESHOOTING

1. Theory of Operation

A. General

Theory of Operation is divided into three levels:

- System Theory of Operation

  Contains a simplified description of signal flow through the ATC-601-2 with accompanying block diagram.

- Functional Theory of Operation

  Contains simplified descriptions of how the various functions of the ATC-601-2 operate.

- Module Theory of Operation

  Contains a detailed description of each assembly in the ATC-601-2.

Refer to 1-2-2, Figures 2 and 3 in the ATC-601-2 Operation Manual for location of controls, connectors and indicators identified with numeric characters. Refer to appropriate schematics and assembly drawings in para 2-2-3 for controls, connectors, indicators and components identified with alphanumeric characters.

B. System Theory of Operation

The ATC-601-2 Ramp Test Set simulates a ground or air interrogator, transmitting Modes A, C, S and Intermode interrogations. The Test Set analyzes reply pulses, provides reply pulse information and indicates failure to comply with accepted guidelines (RTCA DO-181). Refer to Appendix E for interrogation and reply signals.

C. Functional Theory of Operation

(1) Transmit (2-2-1, Figure 1)

Interrogations are controlled and produced from the Front Panel Pulse PC Board Assembly. Pressing the RUN/STOP Key (9) initiates a trigger that causes the Front Panel Pulse PC Board Assembly to transmit specific pulse and Phase Shift Keying (PSK) information (depending on the current Test Set test function) to the Driver PC Board Assembly. The Driver PC Board Assembly drives the pulse and DPSK information to modulate a 30 MHz signal in the Analog IF Assembly. After amplification and frequency mixing by the Mixer PC Board Assembly, a modulated 1030 MHz interrogation signal is transmitted through the RF I/O Connector (15) or ANTENNA Connector (16) to the unit under test (UUT).

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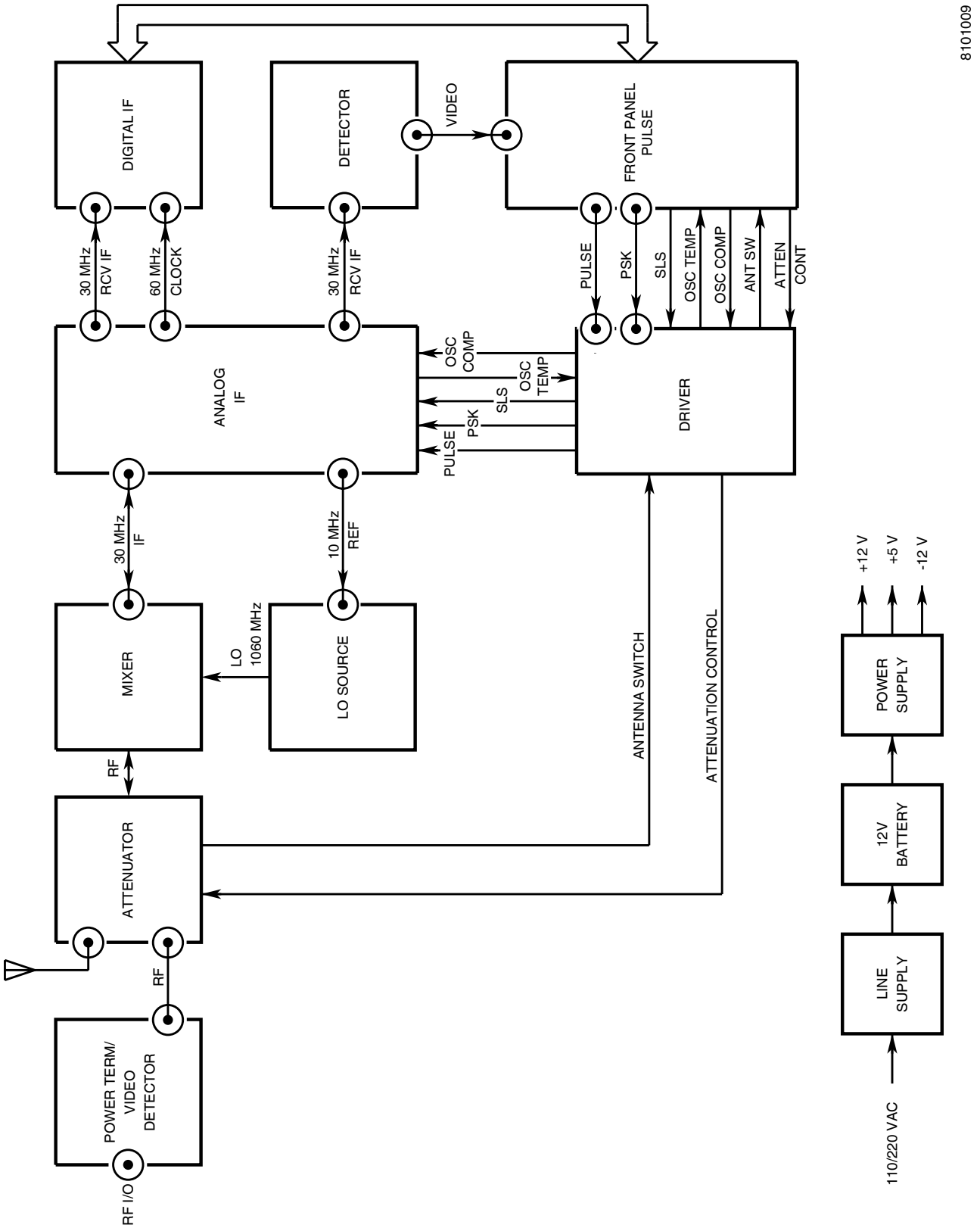

System Block Diagram
Figure 1

(2) Receive (2-2-1, Figure 1)

Replies from the UUT are received on an RF signal at ≈1090 MHz, through the RF I/O Connector (15) or ANTENNA Connector (16). The signal is mixed down to 30 MHz by the Mixer PC Board Assembly, filtered and amplified by the Analog IF Assembly and sent to the Detector and Digital IF PC Board Assemblies. The 30 MHz signal is split into two quadrature phase signals, converted to digital samples and analyzed by the Digital IF PC Board Assembly. Measurement data is stored on the Digital IF PC Board Assembly and accessed by the Front Panel Pulse PC Board Assembly. Reply VIDEO from the Detector Assembly is decoded by the Front Panel Pulse PC Board Assembly. Information is processed, compared with stored guideline information and displayed.

(3) Testing

The ATC-601-2 uses three interrogation processes when testing transponders:

- Background Interrogations

  Background Mode A interrogations are transmitted continuously during any transponder test. Two background interrogations are sent between ATCRBS test interrogations. Eight background interrogations are sent between Mode S test interrogations. Background interrogations determine transponder sensitivity or MTL. Digital-to-Analog Converters (DACs) on the Front Panel Pulse PC Board Assembly provide the voltage used by the Driver PC Board Assembly to drive current through attenuation diodes on the Attenuator PC Board Assembly. Attenuation increases if reply is received or decreases if no reply is received. The attenuation level reached when 50% reply rate occurs is used to calculate MTL on the Digital IF PC Board Assembly. Replies to background interrogations are used by the Digital IF PC Board Assembly to measure power and frequency. Mode C background interrogations are used in the MTL Difference test to verify MTL is the same for both Mode A and Mode C interrogations. Background interrogations are verified using Diagnostics. Refer to para 1-2-3C in ATC-601-2 Operation Manual.

  NOTE: All interrogation and reply signals are attenuated to obtain 50% replies to background interrogations. Displayed MTL is ≈0.6 dB higher than the average background level to indicate the 90% reply point.

- Mode Test

  Mode A, Mode C and Mode S (UF11) interrogations are transmitted in a programmed sequence. Replies determine UUT operating modes. Mode test is the first test run in Auto Test and each Single Test. Mode test uses foreground interrogations. Foreground level is ≈4 dB higher than background level.

- Test Interrogations

  Test interrogations are programmed from ROM to Video RAM by the Processor on the Front Panel Pulse PC Board Assembly according to specific test functions. Test interrogations are transmitted at foreground level and verified using Diagnostics. Refer to para 1-2-3C in ATC-601-2 Operation Manual.

The ATC-601-2 has five testing functions. Test Parameters (Setup Menu), Auto Test, Single Test and Power Test are functions used in testing transponder operation. Self Test is used in evaluating ATC-601-2 operation.

(a) Test Parameters

Information loaded in the Setup Menu is stored in RAM on the Front Panel Pulse PC Board Assembly and used for calculating reply delay and UUT power output.

Reply delay is calculated using the best 8 of 13 replies. Delays are figured in two parts. Total delay (interrogation to reply) is measured with counters on the Digital IF PC Board Assembly, triggered by the Pulse Generator on the Front Panel Pulse PC Board Assembly until reply pulse (50% amplitude) is received. Distance information in Setup Menu is used to figure range delay. The Processor on the Front Panel Pulse PC Board Assembly subtracts the fixed range delay from the average total delay to obtain reply delay.

Refer to para 2-2-1C(3)(d) for calculating UUT power output function.

(b) Auto Test

Auto Test operation control and sequence program, stored in ROM on the Front Panel Pulse PC Board Assembly, directs the Processor on the Front Panel Pulse PC Board Assembly to initiate interrogation pulse generation. Specific interrogations are sent using the transmit function described in para 2-2-1C(1). Replies are received using the receive function described in para 2-2-1C(2). After the series of tests are complete or terminated, results stored in RAM (Front Panel Pulse PC Board Assembly) are entered onto the DISPLAY (14).

NOTE: The Auto Test function stores reply information for all Single Tests. Only modes tested, modes passed, modes failed, UUT Frequency, UUT ERP, UUT MTL and UUT Diversity Isolation are displayed in Auto Test.

(c) Single Test

Single Test operates the same as Auto Test, except each test is one programmed loop. When accessed, each Single Test screen displays latest reply information stored in RAM on the Front Panel Pulse PC Board Assembly. When operating, the program stored in ROM on the Front Panel Pulse PC Board Assembly continues testing until manually terminated.

(d) Power Test

Power Test is a loop program stored in ROM on the Front Panel Pulse PC Board Assembly. The test transmits Mode A background interrogations. Refer to para 2-2-1C(3), Background Interrogations, for MTL calculation. The Digital IF PC Board Assembly splits incoming signals into two quadrature phases to calculate amplitude of F_1 reply pulse. Two power calculations, average and instantaneous, use four samples of each F_1 reply pulse. Average power is calculated using the amplitude of all replies received during Power Test. A small correction factor is subtracted from average power calculations, to offset multipath effects. Instantaneous power is average power calculated using amplitude from replies to latest 100 interrogations. Distance information from the Setup Menu is calculated into path loss on the Front Panel Pulse PC board Assembly. Antenna gain and cable loss from the Setup Menu are added with the path loss and power calculations to provide displayed power readings.

(e) Self Test (2-2-1, Table 1)

Self Test runs as follows:

TEST	THEORY

Non-Volatile RAM Battery (only run on power-up)

Processor on Front Panel Pulse PC Board Assembly reads non-volatile RAM battery bit status from RAM on the Front Panel Pulse PC Board Assembly. Status is set only on power-up.

1. Battery

   Processor on Front Panel Pulse PC Board Assembly reads BATTEST line from Power Supply Assembly through Status Buffer on Front Panel Pulse PC Board Assembly.

2. LO Control

   Processor on Front Panel Pulse PC Board Assembly enables Local Oscillator (LO) through LED Control Register on Front Panel Pulse PC Board Assembly. Processor reads Status Buffer on Front Panel Pulse PC Board Assembly to verify LO is On. LO is then disabled through LED Control Register. Processor reads Status Buffer again to verify LO is Off.

3. Dual Port RAM (DPR)

   Processor on Front Panel Pulse PC Board Assembly writes a sequence using AA55h to fill DPR on Digital IF PC Board Assembly. Processor reads DPR and compares with sequence written. Process repeats using 55AAh. Process repeats a third time loading a number sequence starting at 0000h and increasing one for each address loaded. First two processes verify DPR data transfer. Third process confirms all addresses are being verified.

   NOTE: If DPR test fails, Self Test skips other RAM tests and goes to LED test.

TEST	GROUP	VERIFIES	FAILURE CODE (H)	RUNNING ORDER
Non-Volatile RAM Battery	Power Supply/ Battery	Battery has sufficient power for RAM to retain memory.	00000020	Only on power-up
Battery	Power Supply/ Battery	Voltage is within correct voltage range.	00000010	1
LO Control	RF	Valid ON/OFF status	00000001	2
RAM	Digital	Dual Port RAM (DPR)	01000000	3
		Video RAM	02000000	4
		Display RAM	08000000	5
		Non-Volatile RAM	04000000	6
LED	Digital	Interrogation and reply drivers	80000000	7
Reply Decoder	Digital	Unsolicited Mode S reply (squitter)	00000400	8
		Solicited Mode S reply	00000200	9
		Solicited ATCRBS reply	00000100	10
Pulse Wrap	Digital	PULSE to DPSK timing	00800000	11
UART	Digital	RS-232 loop back	00400000	12
Attenuator #1	Digital	Level at end line diodes	10000000	13
Attenuator #2	Digital	Level at midline diodes	20000000	13
LO Compensation	Digital	DCXO control voltage	40000000	15
LO Detect	RF	LO is locked.	00000002	16
RF Detect	RF	TX level out/Attenuation	00000004	17
DSP Initialization	Digital	Handshake routine	00000040	18
IF Loop	RF	Background level (0 dB)	00020000	19
		SLS/Foreground ratio (9 dB)	00100000	20
		DSP does not measure a non-existent signal.	00200000	21

NOTE: Multiple failures are indicated by the sum of the error codes.

NOTE: If DPR Test fails, subsequent RAM tests are not run.

Self Test
Table 1

4. Video RAM

   Processor on Front Panel PC Board Assembly tests Video RAM on Front Panel Pulse PC Board Assembly in same fashion as DPR on Digital IF PC Board Assembly.

5. Display RAM

   Processor on Front Panel PC Board Assembly copies current screen and transfers visibility to unused secondary page on Liquid Crystal Display (LCD). Processor tests Display RAM on Front Panel Pulse PC Board Assembly using primary page and in same fashion as DPR on Digital IF PC Board Assembly. After test, screen and visibility are returned to primary page.

6. Non-Volatile RAM

   Contents of non-volatile RAM on Front Panel PC Board Assembly are transferred to DPR on Digital IF PC Board Assembly. Processor on Front Panel PC Board Assembly tests non-volatile RAM in same fashion as DPR. After test, original contents are restored in non-volatile RAM.

7. LED

   Processor on Front Panel PC Board Assembly turns On Interrogation and Reply LEDs on Front Panel LED PC Board Assembly through LED Control Register on Front Panel PC Board Assembly. Processor verifies On status through Status Control Register on Front Panel PC Board Assembly. After ≈80 ms, Off status is verified through Status Control Register.

8. Reply Decoder (Unsolicited Mode S reply)

   Processor on Front Panel PC Board Assembly programs Video RAM chips on Front Panel PC Board Assembly with DF11 Mode S squitter. Pulse Generator on Front Panel PC Board Assembly sends squitter from Video RAM chips through RF Assembly to Reply Decoder on Front Panel PC Board Assembly. Decoded reply is stored in RAM on Front Panel PC Board Assembly. Processor compares decoded reply with squitter sent.

   NOTE: Reply Decoder tests fail if RF Assembly is not functioning.

9. Reply Decoder (Solicited Mode S reply)

   Processor on Front Panel PC Board Assembly sends trigger to Reply Decoder on Front Panel Pulse PC Board Assembly to prepare for (solicited) Mode S reply. Processor tests Reply Decoder in same fashion as unsolicited Mode S reply.

10. Reply Decoder (Solicited ATCRBS reply)

    Processor on Front Panel PC Board Assembly tests Reply Decoder on Front Panel Pulse PC Board Assembly using solicited ATCRBS reply in same fashion as solicited Mode S reply.

11. Pulse Wrap

    Processor on Front Panel PC Board Assembly sets up Pulse Generator on Front Panel PC Board Assembly to send a pulse on the $\overline{\text{PULSE}}$ and DPSK lines. Processor uses internal Timer 1 to verify programmed distance between PULSE and DPSK pulses is eight counts (≈3.2 μs).

12. UART

    Processor on Front Panel PC Board Assembly configures UART (RS-232 Interface on Front Panel Pulse PC Board Assembly) to loop back. Processor sends message and verifies reception.

13. Attenuator #1/Attenuator #2

    Processor on Front Panel PC Board Assembly writes values to attenuation DACs on Front Panel PC Board Assembly. Processor reads corresponding status from Analog-to-Digital Converter (ADC) on Front Panel PC Board Assembly to verify DACs are correctly converting attenuation voltage data.

15. LO Compensation

    Processor on Front Panel PC Board Assembly writes values to a DAC on Front Panel PC Board Assembly. Processor reads corresponding status from ADC on Front Panel PC Board Assembly to verify DAC is correctly converting LO compensation voltage data.

16. LO Detect

    Processor on Front Panel PC Board Assembly turns On Local Oscillator on LO Source PC Board Assembly through an LED Control Register on Front Panel PC Board Assembly. Processor verifies LO Detect voltage is 0.35 to 3.1 Vdc by reading 71 to 635 from ADC on Front Panel PC Board Assembly. Test fails if LO is not locked (≈7.5 Hz trapezoidal waveform present at TP27033 on Front Panel Pulse PC Board Assembly).

17. RF Detect

    Pulse Generator on Front Panel PC Board Assembly sends CW at MTL+4 dB with 0 dB attenuation. $\overline{\text{PULSE}}$, $\overline{\text{SLS0}}$ and $\overline{\text{SLS1}}$ lines are activated on Front Panel PC Board Assembly. After going through transmit portion of RF Assembly, the signal returns on RF DETECT line to the ADC on Front Panel PC Board Assembly. Processor on Front Panel PC Board Assembly verifies level after digital conversion. Test is repeated with 3 dB attenuation set by Attenuator Control on Front Panel PC Board Assembly through Driver PC Board Assembly to Attenuator PC Board Assembly. Processor checks 3 dB difference by verifying ratio of unattenuated level to attenuated level is 2 (±0.4).

18. DSP Initialization

    Processor on Front Panel Pulse PC Board Assembly resets Digital IF PC Board Assembly through LED Control Register on Front Panel PC Board Assembly. After reset, Digital Signal Processor (DSP) on Digital IF PC Board Assembly controls RDY output to Status Buffer on Front Panel PC Board Assembly. Processor verifies DSP ready status through Status Buffer.

19. IF Loop (Background level)

    Pulse Generator on Front Panel PC Board Assembly activates $\overline{\text{PULSE}}$ and $\overline{\text{SLS0}}$ lines through Driver PC Board Assembly to modulate 30 MHz CW signal on Analog IF PC Board Assembly. CW signal at background level is sent from Analog IF PC Board Assembly to Digital IF PC Board Assembly. DSP on Digital IF PC Board Assembly measures power level. Processor on Front Panel Pulse PC Board Assembly verifies correct level after digital conversion.

TEST THEORY

20. IF Loop (Foreground/SLS ratio)

    Pulse Generator on Front Panel PC Board Assembly activates $\overline{\text{PULSE}}$, $\overline{\text{SLS0}}$ and $\overline{\text{SLS1}}$ lines through Driver PC Board Assembly to modulate 30 MHz CW signal on Analog IF PC Board Assembly. CW signal at foreground level (MTL+4 dB) is sent from Analog IF PC Board Assembly to Digital IF PC Board Assembly. DSP on Digital IF PC Board Assembly measures power level. Process repeats with $\overline{\text{SLS0}}$ and $\overline{\text{SLS1}}$ lines deactivated to send CW at SLS level (MTL-5 dB). DSP measures power level. Processor on Front Panel Pulse PC Board Assembly checks for 9 dB difference by verifying ratio of foreground level to SLS level is 3 (±1).

21. IF Loop (valid DSP measuring)

    LO is turned Off, disabling CW signal on Analog IF PC Board Assembly. Processor on Front Panel Pulse PC Board Assembly verifies DSP does not measure noise floor as a valid signal.

D. Module Theory of Operation

(1) Power Supply

The Power Supply consists of the Line Supply Assembly and the Power Supply Assembly.

(a) Line Supply Assembly

The Line Supply Assembly is an ac to dc converter containing a power transformer, bridge rectifier and filter.

The AC PWR Connector (J10050) (7) on the Front Panel Assembly is connected to the Line Supply Assembly through P/J11062. Transformer T33001 has two primary windings connected in parallel when 115 VAC is selected by double pole, double throw Switch S15001. The two primary windings are connected in series if 230 VAC is selected. The secondary winding of T33001 is connected to a full wave rectifier BR33001 mounted on the side panel heat sink. Unregulated voltage from BR33001 is applied to the crowbar circuit (over-voltage protection), filtered by C33003 and sent through P33049 to the Power Supply Assembly.

The crowbar circuit includes CR15001, CR15002, R15001, R15002 and Q15001. If voltage becomes excessive, Q15001 turns on, effectively shorting the bridge output and disabling Fuse F12001. F12001 opens when the line reaches approximately 160 VAC (115 VAC operation) or 320 VAC (230 VAC operation).

(b) Power Supply Assembly (2-2-1, Figure 2)

1 Battery Charger

The Battery Charger operates on 15 to 22 V source from the Line Supply Assembly through P23047. The CHARGE Indicator (1) illuminates red when charging and green when battery is more than 80% charged. The CHARGE Indicator (1) is Off when no ac power is applied or the ATC-601-2 is operating.

The Battery Charger requires Test Set power Off and a partially charged battery to initialize. With no battery, the Battery Charger is inoperable. If ATC-601-2 power is On (DISPLAY [14] is illuminated and screen is shown), the Battery Charger is disabled.

When ac power is first applied with Test Set power Off, the Battery Charger provides constant current to the battery. When the battery achieves a 75% charge, voltage across the battery rises rapidly and the Battery Charger switches to voltage regulation mode (at ≈14.6 V).

The 15 V source voltage is applied to the Power Supply Assembly at P23047-8 and P23047-15. Input to the switching section goes through a low-pass filter (C14032, L14006, C14023 and C14038) to Converter/Transformer T14001. Output of T14001 is rectified by CR14003 and filtered by C14001, providing the battery voltage at J11048-1. CR14015 and CR14014 provide back-up voltage separation between the battery, Battery Charger and Output Supply. The battery is grounded through Current Sense Resistor R14001. Regulator U14001 operates on three inputs. The peak current on FET Q23002 is fed back to the Current Sense input (U14001-7). The battery charge voltage is fed back and sensed across a voltage divider (R14003, R14080 and R14007). R14007 (ADJ BATT CHARGER VOLTAGE) adjusts the operating float voltage (14.6 Vdc with charged battery). The charging current sensed at R14001 sets up the reference voltage formed across diodes CR14001 and CR14002. Thermistor RT14001 controls bias current on CR14001 and CR14002. The reference input to U14001-1 is a function of temperature and establishes trickle charge control between 0° C and 70° C. R14073 (GAIN ADJ) controls excess voltage. The pulse output (U14001-13) controls Gate Drivers Q14001 and Q14002. Q14001 and Q14002 drive the Transformer T14001 through Q23002.

The ac voltage at T14001 (E14004) is rectified by CR14011 and C14026. Rectified voltage feeds constant current source Q14015. Q14015 provides ≈20 mA to the CHARGE Indicator (1) through P12001-3. When the line from Q14015 is sourcing current, the CHARGE Indicator (1) is red. When Q14013 and Q14014 are turned on, Q14015 shuts off and sink current through CR14010 causes the CHARGE Indicator (1) to illuminate green. Three conditions must be met to obtain a green indication on the CHARGE Indicator (1):

- Charging current (<≈400 mA) is sensed by U14006C.
- Regulator U14001 is in voltage regulation mode when the compensation output (TP14001) is <≈4 V. The compensation output is sensed by U14006D.
- Regulator U14001 produces enough power to trickle charge the battery when the compensation output (TP14003) is >≈2 V. This indicates a battery is connected and the battery has no open cells. The compensation output is sensed by U14006B.

2 Output Supply

The Output Supply is dependent upon the battery line for the input power. Input voltage to the Output Supply varies with the charge level of the battery. The Output Supply provides operating voltages for the Test Set and is controlled by the POWER Key (11). The Battery Charger is switched Off when the Output Supply is operating.

The POWER Key (11) is connected to P/J23047-1. A switch closure to ground at R14017 turns Q14017 On momentarily, clocking J-K Flip-Flop U14002B connected as a one-shot. At switch closure, U14002B-2 produces a single 100 ms pulse, set by R14019 and discharge time of C24010. The trailing edge of the pulse (going positive) clocks J-K Flip-Flop U14002A. When toggled On, U14002A-15 goes high turning On the Output Supply and U14002A-14 goes low activating $\overline{\text{SHUTDOWN}}$ line to turn Off the Battery Charger. The high at U14002A-15 activates Q14004, Q14005 and Q14006. Q14006 drives the Regulator U14003. Q14005 drives the low voltage sensing circuit.

U14003 regulates using three inputs. Current limit control through FET Q23001 is sensed at U14003-6. The +5 V feedback voltage is set by R14074 and sensed at U14003-1. Feedback current through R14025 sets the negative error sensing input at U14003-2. The pulse output (U14003-13) controls Gate Drivers Q14007 and Q14008 which drive the Transformer T14002 through Q23001. Two outputs from T14002 are rectified, filtered and regulated to provide +12 and -12 Vdc. The other output is rectified and filtered to provide +5 Vdc, regulated by U14003.

The battery voltage is sensed through Q14005 across Voltage Divider R14062, R14060 and R14061. When the battery voltage drops below a threshold determined by temperature (≈+11.3 V at 25° C), U14008C drives a low level through R14068 to the Front Panel Pulse PC Board Assembly causing two blocks to appear on the DISPLAY (14) in the lower left corner (low power indication) and the Battery Test portion of the Self Test to fail. As the battery voltage drops further (to ≈+10.4 V at 25° C), Comparator U14008B senses the low voltage and a high level output activates Q14012. U14002A resets and shuts off the Output Supply. If the Keypad is inactive for ≈15 minutes during operation, Power Disable (PWRDIS) line from the Front Panel Pulse PC Board goes high to Comparator U14008A-6. The high level output causes U14002A to reset and shut off the Output Supply.

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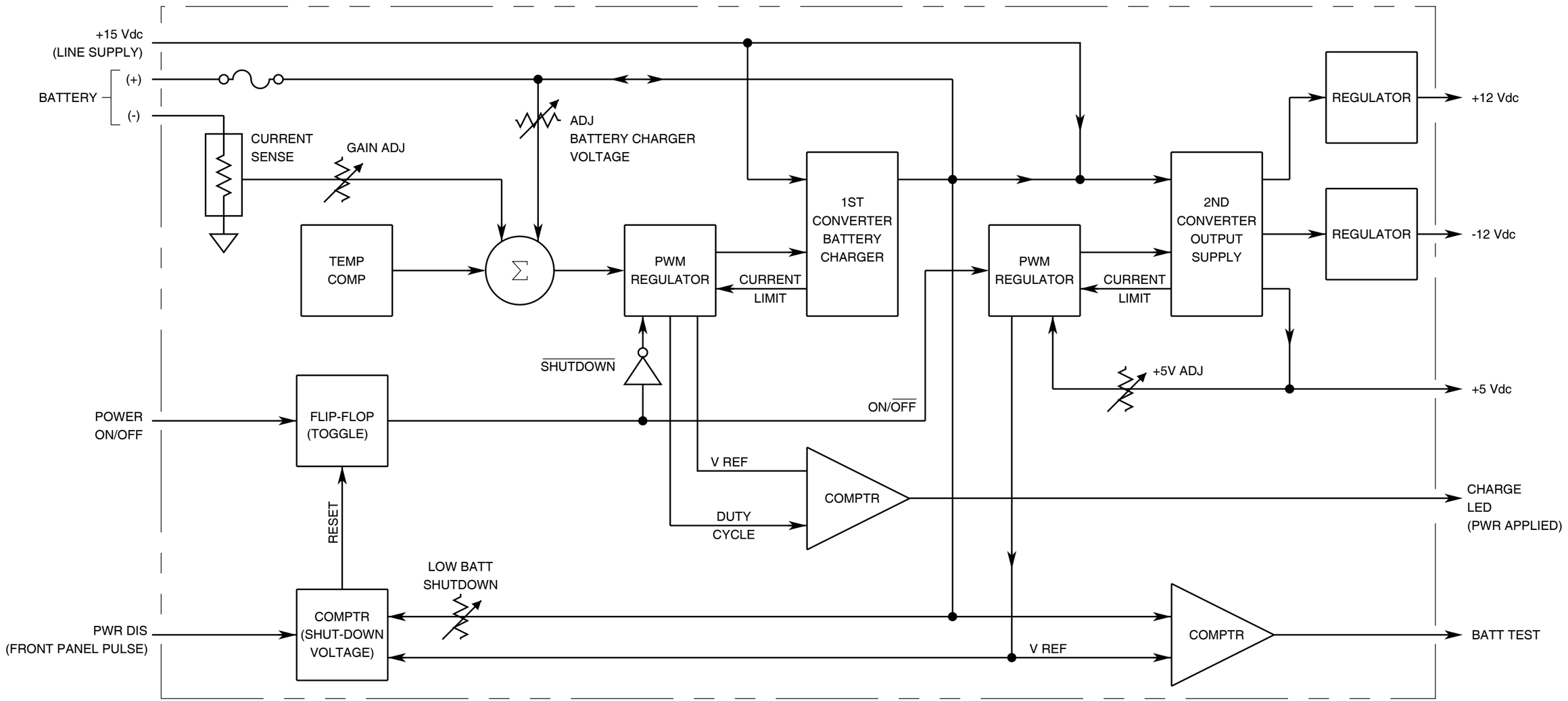

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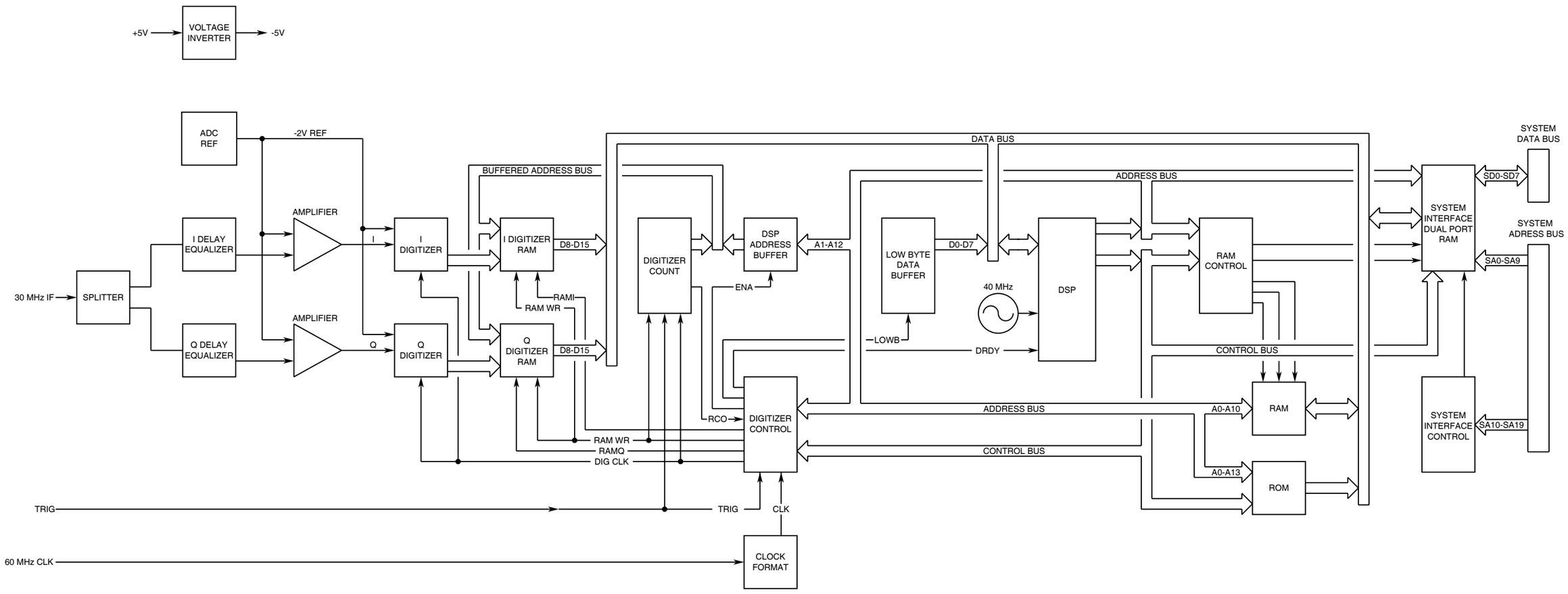
Power Supply Assembly Block Diagram
Figure 2



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Digital IF PC Board Assembly Block Diagram
Figure 3

(2) Digital IF PC Board Assembly (2-2-1, Figure 3)

The Digital IF PC Board Assembly consists of:

Receive IF
Digitizer
Digital Signal Processor (DSP)
System Interface
Voltage Inverter

The Digital IF PC Board Assembly changes the incoming reply signals from analog to digital and accurately calculates power, frequency, pulse spacing, pulse width, pulse amplitude and reply delay. The Receive IF splits the signal in two and provides a complex representation of the original reply signal. The analog signals are converted to digital by the Digitizer and stored into memory. The DSP conducts calculations with the digital information and provides the results to the Front Panel Pulse PC Board Assembly through the System Interface. The Voltage Inverter provides the necessary voltage to operate the Digital IF PC Board Assembly.

(a) Receive IF

The 30 MHz signal from the Analog IF Assembly, verified at TP26017, goes through a 6 dB resistive splitter (R26032, R26033 and R26034) providing two signals while maintaining 12.8 MHz of bandwidth. Delay equalizers cause a 90° phase difference between the two signals to provide a sine and cosine representation of the received IF signal. Delay equalizers are first order constant-resistance time-domain circuits. One delay equalizer (L26001-L26004, C26057-C27060 and R26011) provides the in phase (I) signal. The other delay equalizer (L26005-L26008, C26061-C27066 and R26012) provides the quadrature phase (Q) signal. C26061 and C26063 (φ ADJ) maintain the 90° phase difference between the two signals. R26011 (I LEVEL ADJ) and R26012 (Q LEVEL ADJ) keep amplitude of both signals equal.

Transformers (T26001 and T26002) convert I and Q signals from bipolar to polar. High-speed integrating operational amplifiers (U26031 and U26032) provide approximately seven times amplification for an output of 2 Vp-p at 30 MHz. The midpoints or zero references (≈-1 V) used in the integration process are tapped from resistor networks (R26018, R26017 and R26023, R26024) across the ADC reference voltage (≈-2 V). R26017 and R26023 (ADC ZERO) also compensate for temperature drift. Diodes CR26006 and CR26007 protect the ADCs by effectively shorting positive voltages (0.4 V) to ground. The I signal is verified at TP26019 and the Q signal is verified at TP26020.

(b) Digitizer

The Digitizer consists of five main circuits:

1 ADC Reference

The ADC reference provides the -2 V reference voltage for the flash ADCs. CR26002 drops 2.5 V. Low Offset Amplifier U26027 and current gain transistor Q26002 convert the 2.5 V to -2 V. The non-adjustable ADC reference voltage (1.96 to 2.08 V) is present at test point TP26023. The -2 V reference is used by flash ADCs (U26001 and U26002) and Receive IF operational amplifiers (U26031 and U26032). Each flash ADC draws 23 mA nominal, 40 mA maximum, and the operational amplifier circuits use 0.7 mA. The ADC reference circuit supplies a maximum of 300 mA.

2 Flash ADCs

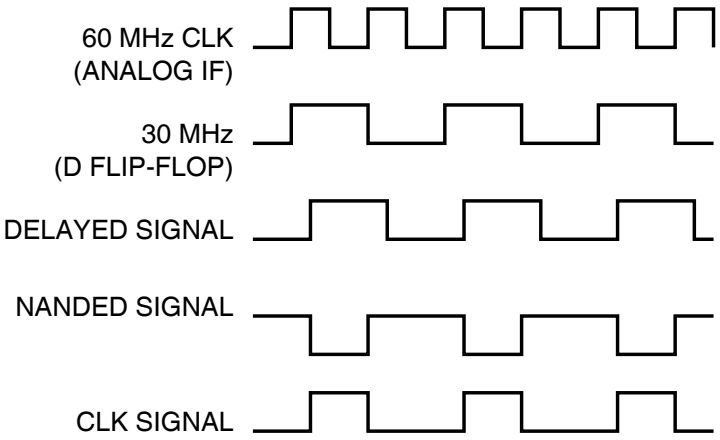
Flash ADCs U26001 and U26002 convert the input analog signals from the Receive IF to digital 8-bit signed values (twos complement). Input signals are set from -2 to 0 V. Voltages >0 V overflow the ADCs. Digital output values range from 80h (-128 decimal), corresponding to -2 V, to 7fh (+127 decimal), corresponding to 0 V. The 30 MHz digital clock from U26015 controls ADC operation.

3 RAM

Digitized data is written into four high-speed RAM chips (U26010- U26013) at a 30 MHz rate. Each RAM chip has a 4k by 4 byte capacity. The RAM chips have separate inputs from outputs. Flash ADCs only write into the RAM chips and the DSP (U26003) only reads from the RAM chips. Address lines are shared by the digitizer control circuit and DSP.

4 Clock Format

The clock format converts the 60 MHz sine wave from the Analog IF Assembly into a 30 MHz TTL clock with a 33% duty cycle. Refer to 2-2-1, Figure 4 for the clock format timing diagram. Transistor Q26001, inverting Schmitt triggers (U26023A and U26023B) and associated circuitry convert the 60 MHz input to TTL. D Flip-Flop U26024A divides the signal by two and the 30 MHz output provides both inputs to NAND Gate U26025A. Because DL26001 delays one input by 5 ns, U26025A has a 67% duty clock output. After being inverted by NAND Gate U26025B, the 30 MHz TTL clock has a high time of 10.67 to 12.67 ns. The clock format output is verified at TP26022.



Clock Format Timing Diagram
Figure 4

5 Digitizer Control

The digitizer control circuit consists of a Programmable Array Logic (PAL) circuit (U26015), three binary counters (U26017, U26018 and U26019), two flip-flops (U26020 and U26028) and two address register buffers (U26021 and U26022). U26015 directs digitizing of data into RAM and reading of data out of RAM. Refer to 2-2-1, Table 2 for description of U26015 inputs and outputs. Refer to Appendix D for PAL equations and Appendix E for timing diagrams.

FLOW	U26015 PINS	NAME	DESCRIPTION
Input	1 and 2	CLK	30 MHz TTL clock with 33% duty cycle from clock format
Input	3	DS	Data Select signal from DSP is high unless made low (active) for communicating to external data memory (DPR).
Input	4	STRB	Strobe signal from DSP is high unless made low (active) to indicate external bus cycle.
Input	5, 6 and 7	A0, A14 and A15	Address lines from DSP
Input	8	TRIG	Inverted trigger from Front Panel Pulse PC Board indicates start of process.
Input	9	RCO	Ripple Count Out from binary counters indicates end of digitizing the data.
Output	12	DIG CLK	Digitizer Clock
Output	13	LOWB	Low Byte selects Line Driver U26026 to keep data lines (D0-D7) low during RAM read.
Output	15	ENA	Enable Address activates two address register buffers (U26021 and U26022) connecting DSP to digitizing RAM.
Output	16	DRDY	Low Data Ready signal indicates digitizing RAM is ready for DSP to read.
Output	17	RAM WR	RAM Write controls RAM access (low for ADCs writing to RAM and high for DSP reading from RAM).
Output	18	RAMQ	Enables Q digitizer RAM.
Output	19	RAMI	Enables I digitizer RAM.

Digitizer PAL Inputs and Outputs
Table 2

Digitizing sequence is:

STEP	ACTION

1. U26023C inverts high TRIG output from Front Panel Pulse PC Board Assembly to low, resetting Binary Counters U26017, U26018 and U26019.
2. On the first rising edge of the clock pulse after TRIG goes low:
   - RAM WR goes low to enable the ADCs to write to RAM.
   - ENA goes high to disable DSP addressing.
   - DRDY goes high indicating data is not ready for DSP to read.
3. RAM WR going low enables Flip-Flops U26020 and U26028 to address RAM by latching address lines to the output of Binary Counters U26017, U26018 and U26019.
4. DIG CLK, RAMI and RAMQ become synchronous with CLK on the first falling edge of the clock pulse after RAM WR goes low.
5. TRIG returns to high and the binary counters start counting on the first rising edge of DIG CLK. Binary Counters U26017, U26018 and U26019 are cascaded together to provide a count from 0 to 4095 (the capacity of the digitizer RAM chips).
6. With each DIG CLK count, the ADCs convert incoming analog data into another byte.
7. With each DIG CLK count, the byte of converted data from the prior clock cycle is stored in the next address in RAM, as stepped by the binary counters (U26017, U26018 and U26019) and latched by the flip-flops (U26020 and U26028).
8. Process continues until the binary counters are full and RCO output U26019-15 goes high.
9. DIG CLK, RAMI and RAMQ stop synchronous operation with CLK and stay high.
10. After U26015 internal switching allows ADCs to write last byte of data into RAM, RAM WR goes high setting RAM for DSP to read.
11. ENA goes low to enable DSP to address digitizing RAM.
12. DRDY goes low to trigger DSP for reading digitizer RAM. DRDY stays low until a read is done at any digitizer RAM address.
13. DSP reads RAMQ (quadrature phase data) using an odd address. A15 and A0 are high while A14, DS and STRB are low.

    DSP reads RAMI (quadrature phase data) using an even address. A15 is high while A0, A14, DS and STRB are low.

(c) Digital Signal Processor (DSP)

U26003 is a TMS320C25 DSP. Two external EPROM chips, U26004 and U26005, provide 8k by 16 bits of ROM containing the program code for U26003. U26003 selects the EPROM chips at addresses from 0 to 3FFFh while the PS (U26003-47) and STRB (U26003-49) lines are both low through OR Gate U26034A. Two external 2k by 8 RAM chips (U26008 and U26009) and internal DSP RAM provide ≈2.6k by 16 bits of RAM. Interface to external RAM is accomplished with the 16V8A PAL U26016. Addresses from 400 to BFFh with STRB low cause SRCS (U26016-19) to go low, selecting the RAM chips. SROE (read) or SRWE (write) goes low depending on R/$\overline{W}$ line (U26003-48). Data lines D0-D7 access U26008 and data lines D8-D15 access U26009. External RAM is contiguous to the internal RAM located through 3FFh. RAM is accessed with no wait states.

The DSP operates using a 40 MHz clock provided by U26035. Inverting Schmitt Trigger U26036A converts clock output to TTL.

In operation, the DSP performs calculations, controlled by ROM, on the data in digitizer RAM. Results are stored in RAM available to the DSP. After reading the digitizer RAM chips, the DSP performs mathematical operations to determine:

- Position of any pulse
- Width of any pulse
- Rise time of any pulse
- Power of any pulse
- Difference in power between pulses
- Frequency of the IF
- Phase changes in the IF

(d) System Interface

The System Interface consists of PAL U26016 and Dual Port RAM (DPR) U26007. The RDY line (P26006-A7), when high, indicates the Digital IF PC Board Assembly is ready to communicate. The RDY line is reset at power-up or when system is reset by the Front Panel Pulse PC Board Assembly. IS, STRB and R/$\overline{W}$ goes low to U26016 causing RDYCS to go low. RDYCS clocks D Flip-Flop U26024B and a high on data line D0 sets the RDY line high. The DSP accesses the DPR at addresses C000 to C3FFh through the PAL. When DS is low with A14 and A15 high (valid DPR address), a high (U26016-15) is sent to J-K Flip-Flop U26029A to add a wait state. On the falling edge of CLK2, U26029A output goes high to U26016-5, setting READY high. When a valid address other than a DPR address is accessed, READY line is set high without a wait state. Refer to wait state timing diagrams in Appendix E. When the DPR is accessed by the Front Panel Pulse PC Board Assembly, the BUSY line from the DPR (U26007-3) goes low causing the READY line to remain low.

(e) Voltage Inverter

The Voltage Inverter converts the +5 V input to a -5 V output. The Voltage Inverter is a pulse width modulated circuit consisting of a relaxation oscillator, Transistor Q26004, Switcher Pass Device Q26005, Clamp Diode CR26005 and associated filtering components.

The relaxation oscillator consists of Comparator U26037, Voltage Divider R26036 and R26037, Resistor R26039 and Capacitor C26079. R26039 and C26079 provide the time constant, setting the oscillation frequency. The voltage divider sets the voltage limitations of the oscillator (centered around +5 V). Comparator U26037 sends a pulse output to control Q26005. The pulse (≈10 V) is based on the input from Transistor Q26004 and the voltage divider.

Transistor Q26004 works as differential amplifier and provides feedback current to modulate duty cycle offset by R26038. R26040 and R26041 provide feedback voltage (≈-0.7 V) on emitter of Q26004. R26041 (-5V ADJ) sets level of feedback necessary to maintain the -5 V output. Diodes CR26003 and CR26004 compensate for voltage drop across the base to emitter of Q26004. C26080 provides lead compensation to dampen feedback loop ringing caused by the delay from input to output.

The pulse output from Comparator U26037 causes current to flow through Q26005 ≈50% of the time. The other part of the time current flows through CR26005. The voltage drop across CR26005 goes from +0.5 to -10 V during the duty cycle averaging out to -5 V. C26081 provides a dc block between the modulating circuit and the output. L26009 and L26010 provide filtering and modulation allowance.

(3) Front Panel Pulse PC Board Assembly (2-2-1, Figure 7)

The Front Panel Pulse PC Board Assembly consists of:

Processor
Pulse Generator
Reply Decoder
Display Control
Keypad Interface
RS-232 Interface
Attenuator Control
Oscillator Compensation
Analog-to-Digital Converter
Status Buffer
LED Control Register
Digital IF PC Board Assembly Access

The Front Panel Pulse PC Board Assembly controls the general operation of the ATC-601-2 Test Set by providing an interface to the user, generating interrogations, decoding replies and controlling both the Digital IF PC Board and RF Assemblies.

(a) Processor

The Processor has four major components: Microprocessor U27001, two 64k ROMs (U27012, U27013) and 32k non-volatile SRAM U27017. U27001, a multi-functional 80188 microprocessor, receives instruction data from the two 64k ROMs and carries out assignments as instructed. U27001 uses 11 chip selects. Refer to 2-2-1, Table 3 for chip select definition. Chip select lines are active low. SRAM U27017 has internal battery back-up to prevent loss of memory.

CHIP SELECT	LINE	SELECTION	ADDRESSES
Upper	$\overline{\text{UCS}}$	64k ROM (U27012)	F0000-FFFFFh
Lower	$\overline{\text{LCS}}$	32k SRAM (U27017)	00000-08000h
Mid-Range	$\overline{\text{MCS0}}$	Digital IF PC Board Assembly (U26007)	C0000-CFFFFh
	$\overline{\text{MCS1}}$	Pulse Generator (U27022)	D0000-DFFFFh
	$\overline{\text{MCS2}}$	64k ROM (U27013)	E0000-EFFFFh
Peripheral	$\overline{\text{PCS0}}$	Control Decoder (U27008)	400-47Xh
	$\overline{\text{PCS1}}$	RS-232 Interface (U27030)	480-487h
	$\overline{\text{PCS2}}$	Keypad Interface (U27027)	500h
	$\overline{\text{PCS3}}$	Control Decoder (U27037)	580-5FXh
	$\overline{\text{PCS4}}$	Control Decoder (U27036)	600-67Xh
	$\overline{\text{PCS5}}$	LCD Controller (U27048)	680-681h

Microprocessor U27001 Chip Selects
Table 3

Instruction sequence is:

STEP	ACTION

1. Address latch enable (BALE) line (U27001-61) to Transparent Latch U27010 goes high, allowing U27001 to set address where data is to be received through data lines to U27010.
2. When address is valid, BALE goes low, causing lower 8 bits of address to be latched onto U27010 address lines. Lower Address Latch U27010 allows U27001 to receive data on data lines without changing address selected.
3. $\overline{UCS}$ line (U27001-34) is low to enable U27012. Read ($\overline{RD}$) line (U27001-62) goes low to enable data byte at address selected (initial address is FFFF0) to be sent to U27001.
4. Data is processed and instruction is carried out in same fashion. BALE goes high, chip is selected, valid address is latched and data is read from or written to address. Write ($\overline{WR}$) line (U27001-63), goes low and $\overline{RD}$ line stays high when sending data to an address.

U27001 also provides Direct Memory Access (DMA) capabilities for Reply Decoder U27044. DRQ0 (U27001-18) and DRQ1 (U27001-19) lines set up DMA, allowing a direct read or write to memory.

DMA sequence is:

STEP	ACTION

1. DRQ0 (from Reply Decoder [U27044-A9], ATCRBS Decoder) or DRQ1 (from Reply Decoder [U27044-B9], Mode S Decoder) goes high (DMA request).
2. U27001 finishes current instruction or bus cycle.
3. DMA takes control and programmed action is initiated.

There are four interrupt lines used on U27001. INT0 (U27001-45) goes high from U27030, informing U27001, a transmit or receive action is required at the RS-232 Interface. INT1 (U27001-44) is high when activated by Keypad operation. Pressing any key generates an interrupt. INT2 (U27001-42) is activated by Pulse Generator U27022 and INT3 is controlled by Reply Decoder U27044.

U27001 operates using an external 20 MHz clock source. D Flip-Flop U27007B divides 40 MHz Oscillator G27001 output by two. The 20 MHz clock is fed into U27001-59. U27001 divides the 20 MHz by two, providing the 10 MHz Clock used internally and sent out on CLKO line U27001-56.

Two internal timer circuits are utilized by the Processor. Timer 1 is used to measure distance between PULSE and DPSK pulses during the Pulse Wrap portion of the Self Test. These pulses are generated by the Pulse Generator. A single output pulse is programmed in Video RAM for each signal. The two pulses are then combined into a set-reset type circuit located in the Pulse Generator, Logic Cell Array (LCA) U27022, and fed to Timer 1 for measurement. Timer 2 provides an internal 4.255 ms interrupt used for interrogation intervals.

A reset circuit consisting of Supervisor U27018, Q27001 and associated components provide a delay after power-up or brown-out. The delay (≈15 ms) allows the +5 V from the Power Supply Assembly and 40 MHz Oscillator G27001 to stabilize. Reset is activated manually through S27001 (low ground to U27018-2) or automatically if the +5 V sensed at U27018-7 drops below approximately 4.55 V. U27018 output initiates Logic Cell Array (LCA) programming. The low at U27018-5 is sent to the Reply Decoder and Pulse Generator. The high at U27018-6 activates Q27001 allowing the low ground at the emitter to be felt on the D/PN line (reset to U27001). The LCA components, Pulse Generator U27022 and Reply Decoder U27044, hold the D/PN line low until programming is complete. U27001 resets and sends out another reset (U27001-57) to other logic components on the Front Panel Pulse PC Board Assembly and Digital IF PC Board Assembly. Reset output is maintained until the +5 V line reaches ≈4.7 V. Refer to Appendix E for reset timing diagram.

The Power Disable circuit saves on battery power when the Keypad is inactive. U27001 monitors Keypad activity and if no key is pressed for approximately 15 minutes, D Flip-Flop U27007A is accessed with $\overline{\text{PCS0}}$+1Xh through U27008 and a low is sent on D0 causing PWRDIS to go high to the Power Supply Assembly. The comparator on the Power Supply Assembly resets the flip-flop and disables the Output Supply, switching off the power. PWRDIS returns to low upon power-up or after reset.

(b) Pulse Generator

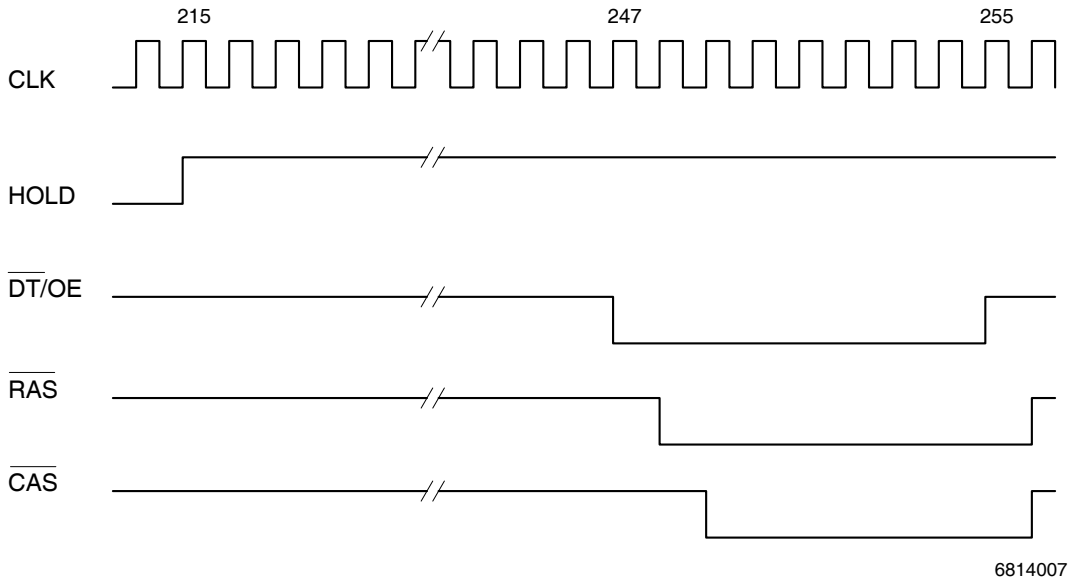
The Pulse Generator section of the Front Panel Pulse PC Board Assembly consists of programmable LCA U27022, Video RAM chips U27023 and U27024, Serial Access Memory (SAM) Counter Reset U27006, Buffer/Driver U27004, Multiplexers (MUX) U27015 and U27016, Delay DL27001, Schmitt Trigger Inverter U27025A, Control Decoder U27008 and PROM U27003.

The Video RAM chips are dual port with random access available to U27001 and serial access to U27022. U27001 reads and writes to the Video RAM chips with access controlled through U27022. Video RAM chips U27023 and U27024 are accessed when $\overline{\text{MCS1}}$, BALE and either $\overline{\text{WR}}$ or $\overline{\text{RD}}$ are activated. Addresses are selected using Multiplexers U27015 and U27016. When $\overline{\text{RAS}}$ goes low, the select line to U27015 and U27016 stays high because the output at U27022-43, changing to high (inverted low by U11025A) when $\overline{\text{RAS}}$ goes low, is delayed 10 ns through DL27001. This allows A8 through A15 to be latched to the Video RAM chips, selecting the row address. After the delay, the multiplexers with the select line low are set to latch A0 through A8 to the Video RAM chips, selecting the column address when $\overline{\text{CAS}}$ goes low. $\overline{\text{DT}}$/OE goes low for a read operation or $\overline{\text{RWR}}$ goes low for a write operation.

Serial access by U27022 is a read only function. The Video RAM chips transfer rows (256 bytes/row) of data into internal serial access registers. Data is sent from the registers to U27022, one byte each clock count. Serialized data is sent out from U27022 with each bit line connected to a specific output according to 2-2-1, Table 4.

VIDEO RAM	PIN NO	U27022	PIN NO
VS0	24	$\overline{\text{BPULSE}}$	28
VS1	29	$\overline{\text{BSLS0}}$	30
VS2	31	BDPSK	32
VS3	33	BTRIG	34
VS4	36	BSYNC	37
VS6	38	$\overline{\text{BSLS1}}$	39

Pulse Generator Serialized Data Output
Table 4



Pulse Generator Data Transfer Timing Diagram
Figure 5

Refer to 2-2-1, Figure 5. Pulse Generator serial sequence is:

STEP	ACTION

1. U27001 programs pulses into the Video RAM chips, as directed by ROM and initiated by the Keypad.
2. U27001 programs a stop byte (10010000) into an address XXFEh (255th byte) corresponding to the desired row to end on.
3. U27001 programs 256 bytes of cleared memory (00h).
4. U27001 programs the starting address using the $\overline{\text{STADD}}$ line ($\overline{\text{PCS0}}$+2Xh) through U27008 for access.
5. U27001, through U27008 ($\overline{\text{PCS0}}$+4Xh), sends a low on the $\overline{\text{START}}$ line to U27022 initiating the start of data transfers and setting the internal counter to 191h.

STEP	ACTION

6. After the 215th byte of cleared memory, U27022 HOLD output (pin 53) goes high to request access to the address lines from U27001.

7. HLDA input (pin 20) goes high informing U27022 that U27001 relinquishes address line control.

8. After 247 bytes, $\overline{DT}$/OE goes low to set up the Video RAM chips for a data transfer to the serial access registers.

9. $\overline{RAS}$ goes low on the next clock count. Row address, determined by the programmed starting address, is selected.

10. $\overline{CAS}$ goes low on the following clock count and a zero address from U27006 (enabled by U27022) causes the data transfer to start at address zero in the serial access registers.

11. After 255 bytes of cleared memory is shifted out of the serial access registers, $\overline{DT}$/OE goes high, triggered by internal counter in U27022. U27022 internal counter tracks 256 clock counts.

12. Data transfer occurs. 256 new bytes from the selected row are loaded into the serial access registers.

13. Each data transfer is followed by a $\overline{CAS}$ before $\overline{RAS}$ refresh.

    NOTE: When no data transfers are occurring, refresh still takes place every 12.8 µs.

14. With each 50 ns (20 MHz) clock count, one byte (one bit for each output) is shifted out of the serial access registers to U27022.

15. Data transfer is repeated every 12.8 µs with each successive row as stepped by internal counter in U27022. New rows are transferred and sent out until the programmed stop byte is encountered. After the stop byte, the last row is transferred and continually shifted out of the serial access registers until the next transfer.

    NOTE: The last row transferred is usually the 256 bytes of cleared memory. For CW transmissions, the last row contains all ones.

16. The stop byte also initiates an interrupt (INT2) to U27001.

    NOTE: If another interrupt is received during operation, Microprocessor U27001 manually stops Pulse Generator operation by activating the $\overline{STOP}$ line ($\overline{PCS0}$+3Xh).

Buffer/Driver U27004 is used to isolate and boost signals off the Front Panel Pulse PC Board Assembly. Buffer U27014D drives the External DPSK Out signal out of the Test Set through the Motherboard PC Board Assembly and COMM Connector (3). Configuration PROM U27003 stores information for reprogramming U27022 on power-up. External PULSE, External DPSK and External SYNC from the COMM Connector (3), when connected, are isolated and converted to TTL before entering the Pulse Generator.

(c) Reply Decoder

Reply Decoder U27044 is a programmable LCA component with more functional capacity than the Pulse Generator. Two independently operating decoders, one each for Mode S and ATCRBS, are incorporated into U27044. The programmed internal operation allows for two operating modes, solicited and monitor (receive all). In solicited mode, the Reply Decoder looks for a reply after receiving a trigger input (U27044-P10) from Pulse Generator U27022. U27022 sends the trigger indicating an interrogation is being transmitted and a reply is expected. Replies are received within
12.8 μs for Mode S and 6.4 μs for ATCRBS, as verified by the Reply Decoder, to be counted as valid. In monitor mode, the Reply Decoder looks for all incoming replies and the trigger input is ignored. When valid replies are received (U27044-P9), the Reply Decoder transfers data to RAM using DMA. Mode S data is transferred by DMA channel #1 (DRQ1) and ATCRBS data is transferred by DMA channel #0 (DRQ0).

Reply Decoder is controlled through an internal control register setup by U27001. Refer to 2-2-1, Table 5 for control register bit definition. Control register sequence is:

STEP	ACTION

1. $\overline{\text{PCS4}}$ +60h through U27036 causes $\overline{\text{ENDEC}}$ (U27044-P11) to go low.
2. $\overline{\text{WR}}$ (U27044-P12) goes low.
3. Data is written to U27044 (A13, B13, C13, D13, A12, B12, C12 and D12) setting the control register.

Mode S sequence is:

STEP	ACTION

1. If in solicited mode, BTRIG is sent from U27022-34 to U27044-P10.
2. U27044 looks for a reply on VIDEO (U27044-P9), inverted by U27051A. If solicited, the start of reply must be received within
   12.8 μs of BTRIG signal to be valid.
3. Mode S reply decoder verifies detected reply contains Mode S preamble. BEGIN (U27044-G1) goes high when detected preamble is valid and control register D2 is high.
4. Mode S reply message is received and DMA1 is activated through DRQ1 (U27044-B9) going high.

BIT #	DEFINITION	SETTING	RESULT
D0	Mode S Function Reset	0	Normal operation
		1	Mode S decoder is reset. All incoming replies and triggers are ignored. DMA line (DRQ1) is cleared.
D1	Mode S Receive All	0	Solicited Mode (12.8 µs reply delay window)
		1	Monitor Mode (Receive All)
D2	Mode S External Trigger Enable	0	BEGIN line disabled
		1	Valid preamble sets BEGIN line to high (1).
D3	Not Used		
D4	ATCRBS Function Reset	0	Normal operation
		1	ATCRBS decoder is reset. All incoming replies and triggers are ignored. DMA line (DRQ0) is cleared.
D5	ATCRBS Receive All	0	Solicited Mode (6.4 µs reply delay window)
		1	Monitor Mode (Receive All)
D6	Not Used		
D7	Video Invert	0	Incoming VIDEO not inverted (Self Test)
		1	Incoming VIDEO inverted (normal operation)

Reply Decoder Control Register Bit Definition
Table 5

STEP	ACTION

5. $\overline{PCS4}$ +61h causes $\overline{ENDEC}$ (U27044-P11) to go low and A0 (U27044-N7) to go high, selecting Mode S reply decoder.

6. $\overline{RD}$ (U27044-P13) goes low.

7. Mode S message is transferred as it is received, one byte at a time, from U27044 (A13, B13, C13, D13, A12, B12, C12 and D12) to RAM Chip U27017. Refer to 2-2-1, Table 6 for reply data byte formation.

STEP	ACTION

8. U27044 verifies message length and presence of message bits, setting Mode S status register byte accordingly. The Mode S status register byte uses two bits. The first bit (D0) indicates valid reply status. A low (0) indicates invalid reply data or a high (1) indicates valid reply data is received. Bit D1 shows the solicited reply status. A low (0) indicates unsolicited reply and a high (1) indicates reply, being within the reply delay window, is a valid reply responding to the interrogation. Bits D2 through D7 are not used.
9. When all data is transferred and last DMA request goes high for transfer of Mode S status register byte, INT3 (U27044-C9) goes high to U27022.
10. Mode S status register is transferred, control register is written to for Mode S reset ($\overline{PCS4}$+60h-D0) and interrupt is cleared at $\overline{PCS4}$+63h.

ATCRBS sequence is:

STEP	ACTION

1. If in solicited mode, BTRIG is sent from U27022-34 to U27044-P10.
2. U27044 looks for a reply on VIDEO (U27044-P9), inverted by U27051A. If solicited, reply must be received within 6.4 μs of BTRIG signal, to be valid. ATCRBS status register solicited reply status bit D0 is set. A low (0) indicates unsolicited reply or a high (1) indicates reply, being within the reply delay window, is a valid reply responding to the interrogation.

   NOTE: Bits D1 through D7 are not used by ATCRBS status register byte.
3. ATCRBS reply decoder verifies detected reply contains correctly positioned F_1 and F_2 pulses.
4. DMA0 is activated through DRQ0 (U27044-A9) going high.
5. $\overline{PCS4}$+62h causes $\overline{ENDEC}$ (U27044-P11) to go low, A0 (U27044-N7) and A1 (U27044-N6) to go high, selecting ATCRBS reply decoder.
6. $\overline{RD}$ (U27044-P13) goes low.
7. When complete ATCRBS reply is received, reply data is transferred, one byte at a time, from U27044 (A6, B6, C6, D6, A5, B5, C5 and D5) to RAM U27017. Refer to 2-2-1, Table 6 for reply data byte formation.
8. When all data is transferred and last DMA request goes high for transfer of ATCRBS status register byte, INT3 (U27044-C9) goes high to U27022 only if in monitor (JTB27001 jumper installed).
9. ATCRBS status register is transferred, control register is written to for ATCRBS reset ($\overline{PCS4}$+60h-D4) and interrupt is cleared at $\overline{PCS4}$+63h.

MODE	TRANSFER ORDER	BIT NUMBER							
	BYTE #	D7	D6	D5	D4	D3	D2	D1	D0
Mode S	1	1	2	3	4	5	6	7	8
	2	9	10	11	12	13	14	15	16
	3	17	18	19	20	21			
(Short	7	 51			52	53	54	55	56
Message)	8	. . . . . Mode S status register							
or (Long	14	 107			108	109	110	111	112
Message)	15	. . . . . Mode S status register							
ATCRBS	1 (HIGH)	SPI	Null2	Null1	X	A4	A2	A1	B4
	2 (LOW)	B2	B1	C4	C2	C1	D4	D2	D1
	3	. . . . . ATCRBS status register							

Reply Data Byte Information
Table 6

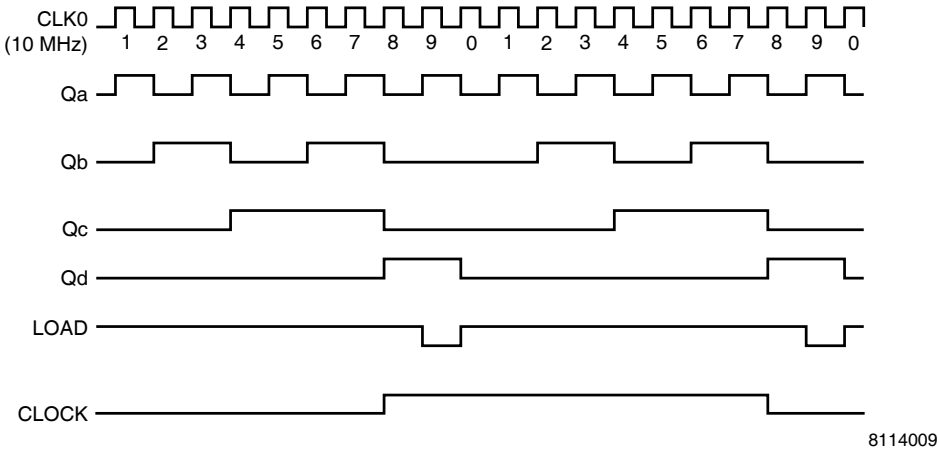
(d) Display Control

Three separate circuits make up the Display Control. The Liquid Crystal Display (LCD) Data Control circuit controls the information entered onto the DISPLAY (14). The Contrast Control and Backlight Control circuits use Digital-to-Analog Converters (DACs) to adjust physical characteristics of the LCD.

1 LCD Data Control

LCD Data Control is accomplished with a 500 kHz Clock, LCD Controller U27048, LCD Control PAL U27029 and Display RAM U27049.

Refer to 2-2-1, Figure 6 for 500 kHz Clock timing. Counter U27039 divides the 10 MHz clock input by 10 (NAND Gate U27011C resets U27039 on each nine count). The 1 MHz output clocks D Flip-Flop U27007B, configured to change state with each clock, providing a 500 kHz clock with a 50% duty cycle. The 500 kHz clock is verified at test point TP27004.



500 kHz Clock Timing Diagram
Figure 6

LCD Controller U27048, an HD61830 Graphic Display Controller operating in the character mode, acts as a memory mapped device to the Processor. U27001 reads from and writes to U27048 on a byte wide basis. U27001 selects U27048 by activating $\overline{PCS5}$, accessing the data register at address X0h (RS input U27048-18 low) and the instruction register at address X1h (RS input U27048-18 high).

U27048 has six outputs to the LCD. D1 is the serial data output for the upper half of the screen and D2 is the serial data output for the lower half of the screen. FLM is the frame signal for display synchronization. CL1 is the display data latch signal for LCD drivers and CL2 is the display data shift clock for LCD drivers. M converts the LCD driving signal to an ac waveform.

PAL U27029 inserts wait states in the processor bus cycle. Refer to Appendix D for PAL equations. U27029 also generates the Enable (U27048-16) and Read/Write (U27048-17) signals for U27048. Wait states, inserted before the ARDY line to U27001 goes low, are required because LCD Controller U27048 operates slower than the microprocessor. Refer to Appendix E for timing diagrams.

Display RAM U27049 stores pixel data (character codes) for U27048 and is accessed by U27001 through U27048.

2 Contrast Control

Contrast Control is based on the input voltage obtained from CR22001 on the Analog IF PC Board Assembly. Ambient temperature conditions are sensed by CR22001 and the resulting voltage (2.73 V at 0° C, changes 33.94 mV/°C) is sent through a differential amplifier U27034C to the ADC (U27045-1). Refer to para 2-2-1D(3)(i) for ADC operation. The information sent from U27045 causes U27001 to send adjustment data to DAC U27032, selected by $\overline{ENCON}$ ($\overline{PCS4}$+1Xh through U27036) going low. U27032 provides a bipolar output of -5 to +5 V, used to control the contrast on the LCD. The -5.1 V, used in powering the LCD, is provided by the voltage drop across Zener Diode CR27011.

3 Backlight Control

Backlight Control is based on the input voltage obtained from R13001 on the Front Panel LED PC Board Assembly. Ambient light conditions are sensed by R13001 and the resulting voltage drop is applied to the ADC (U27045-26). Refer to para 2-2-1D(3)(i) for ADC operation. Information sent from U27045 causes U27001 to send adjustment data to DAC U27033, selected by $\overline{ENBLT}$ ($\overline{PCS4}$+0Xh through U27036) going low. U27033 provides a corresponding voltage output through Driver U27034A with Q27005 to drive Inverter Supply U27035. U27035 provides the increased voltage levels necessary to run the backlight. Capacitors C27082 and C27083 provide noise suppression in the operational amplifier feedback circuit. Zener Diodes CR27016 and CR27017 are clamped to ground to protect circuit if backlight is not connected.

(e) Keypad Interface

Keypad Interface consists of Buffer/Latch U27027, NAND Gate U27011B, resistors, transistors and diodes. U27027 is selected by U27001 with $\overline{PCS2}$. Keypad data, activated when low, is defined in 2-2-1, Table 7.

When the Keypad is inactive, Resistive Network RN27001 holds the row and column lines to a high impedance. When a key is pressed, a row and column line are connected together.

	COLUMN BIT		
ROW BIT	**D1 ($\overline{COL1}$)**	**D2 ($\overline{COL2}$)**	**D3 ($\overline{COL3}$)**
D4 ($\overline{ROW1}$)	AUTO TEST Key (13)	PWR TEST Key (12)	RUN/STOP Key (9)
D5 ($\overline{ROW2}$)	SETUP Key (4)	SELF TEST Key (6)	SLEW Key (↓) (8)
D6 ($\overline{ROW3}$)	SELECT Key (↑) (10)	SELECT Key (↓) (10)	SLEW Key (↑) (8)
D7 ($\overline{ROW4}$)	Not used		
NOTE: D0 is $\overline{ANT\ SW}$ from the ANTENNA PUSH BUTTON Switch (21).			

Keypad Data Definition
Table 7

Keypad Sequence Example is:

STEP	ACTION

1. Pressing the AUTO TEST Key (13) connects row 1 with column 1. Circuit is closed and current flows.
2. Current flowing at the base turns Q27002 on, allowing the low ground on the emitter through the collector and Diode CR27001 to NAND Gate U27011B. The high output sends an interrupt (INT1) to the Microprocessor (U27001-44).
3. The low through Q27002 is also sent through U27027 when selected by U27001 with $\overline{PCS2}$. The low on collector of Q27002 is felt at U27027-4, causing D0 to be read low by U27001 indicating the pressed key is in column 1. The low on the base of Q27002 is felt at U27027-11, causing D4 to be read low indicating the pressed key is in row 1.

(f) RS-232 Interface

RS-232 communications are provided by an INTEL 82510 Universal Asynchronous Receiver-Transmitter (UART U27030). U27030 is selected by U27001 with $\overline{PCS1}$+(addresses from X0h to X7h). Driver/Receiver U27028 drives the serially transmitted signal off the Front Panel Pulse PC Board Assembly through P/J25014 to J10053 COMM Connector (3) and buffers incoming handshake and data signals. U27030 generates an interrupt (INT0) when servicing is required. U27001 polls the internal status registers to determine the cause of the interrupt (TXD or RXD).

(g) Attenuator Control

Two DACs having 0 to 10 Vdc outputs control attenuation. U27041, an 8-bit DAC, provides a +5 V reference and ATTEN1 voltage used to set current on the Driver PC Board Assembly for attenuator end line pin diodes on the Attenuator PC Board Assembly. R27041 (+5V REF ADJ) adjusts the +5 V reference, verified at TP27002. U27041 is accessed by U27001 when $\overline{\text{ENATT1}}$ ($\overline{\text{PCS4}}$+5Xh through U27036) goes low. U27042, a 12-bit DAC, provides the ATTEN2 voltage used to set current on the Driver PC Board Assembly for attenuator midline pin diodes on the Attenuator PC Board Assembly. U27041 is accessed by U27001 when $\overline{\text{ENATT2}}$ ($\overline{\text{PCS4}}$+4Xh through U27036) goes low. Address lines A0-A3 are used to select the data transfer process. Refer to 2-2-1, Table 8. Both output levels are read from ADC U27045.

ADDRESS	OPERATION	BITS
4Eh	Load low nibble	D0-D3
4Dh	Load middle nibble	D4-D7
4Ch	Load low byte (optimum method)	D0-D7
4Bh	Load high nibble	D0-D3, D3 = MSB
47h	Transfer data	XX
43h	Load high nibble and transfer data (optimum method)	D0-D3, D3 = MSB

Attenuator #2 Operation Selection
Table 8

(h) Oscillator Compensation

Oscillator Compensation is based on the input voltage obtained from CR22001 on the Analog IF PC Board Assembly. R27037 (TEMP COMP ADJ) is adjusted at the factory and used in board level calibrations. Ambient temperature conditions are sensed by CR22001. The resulting voltage (2.73 V at 0° C, changes 33.94 mV/°C) is applied through Differential Amplifier U27034C to ADC U27045-1. Refer to para 2-2-1D(3)(i) for ADC operation. Information sent from U27045 causes U27001 to send adjustment data to DAC U27043, selected by $\overline{\text{ENOSC}}$ ($\overline{\text{PCS4}}$+2Xh through U27036) going low. U27043 provides a 0 to 10 V output. Operational Amplifier U27050 and associated components offset, scale and low-pass filter to achieve the desired +2 to +8 Vdc output. Output level is read from ADC U27045.

(i) Analog-to-Digital Converter

ADC U27045 is used for both normal operation and Self Test operation. Refer to 2-2-1, Table 9 for analog input description.

ADC sequence is:

STEP	ACTION

1. U27001 selects channel address with $\overline{\text{PCS3}}$+1X through Control Decoder U27037 and, with $\overline{\text{WR}}$ active, through NOR Gate U27038B (ADLTCH). The high output is sent to U27045-22 along with specific lower address (A0-A2), latching the desired channel to the ADC.

STEP ACTION

2. The start A/D conversion command is sent using address $\overline{PCS3}$+0Xh through U27037, and with $\overline{WR}$ active, through NOR Gate U27038C (SOC). The high output is sent to U27045-6. Conversion begins and End of Conversion (EOC) line to Status Buffer U27026 goes low (within 18 µs from when start command was issued).

3. U27001 polls the EOC signal from the Status Buffer and when the conversion is finished (≈48µs), EOC goes high.

4. Data is read from output Buffer U27046 using address $\overline{PCS3}$+2Xh through U27037, and with $\overline{RD}$ active, through NOR Gate U27038D (DEN). The high output is sent to U27045-9 and through Inverter U27038A to activate U27046. Two data reads are required to receive all 10 bits. Data is sent out in the following fashion:

Data Bit Locations:		D7	D6	D5	D4	D3	D2	D1	D0
First Read:	Bit #	10	9	8	7	6	5	4	3
Second Read:	Bit #	2	1	X	X	X	X	X	X

Bit 10 = MSB, Bit 1 = LSB

INPUT	ADDRESS	DESCRIPTION
PHOTO RES Channel 0	$\overline{PCS3}$+10h	Voltage across Photo Resistor R13001 (Front Panel LED PC Board Assembly), set by ambient light conditions, is used in making Backlight Control adjustments.
RF DETECT Channel 1	$\overline{PCS3}$+11h	Provides indication if RF carrier is present (Self Test). 2.5 V (±0.125 V) indicates passing status (only active in CW mode).
Channel 2	$\overline{PCS3}$+12h	Not used
OSC T RD Channel 3	$\overline{PCS3}$+13h	Voltage across Diode CR19001 (Analog PC Board Assembly), controlled by ambient temperature conditions, is used in making Contrast Control and Oscillator Compensation adjustments.
LO DETECT RD Channel 4	$\overline{PCS3}$+14h	Local Oscillator Detect (Self Test), Pass-constant level between 0.35 and 3.1 Vdc, Fail-oscillation (at ≈7.5 Hz) or level outside Pass voltage window (0 to 0.35, 3.1 to 4.14 V).
ATTEN1 BIT Channel 5	$\overline{PCS3}$+15h	Provides level of Attenuator #1 DAC output (DAC output ÷ 2.5 [± 10%])
ATTEN2 BIT Channel 6	$\overline{PCS3}$+16h	Provides level of Attenuator #2 DAC output (DAC output ÷ 2.5 [± 10%])
OSC COMP BIT Channel 7	$\overline{PCS3}$+17h	Provides oscillator compensation level (DAC output ÷ 2.5 [± 10%])

Analog Input to ADC Description
Table 9

(j) Status Buffer

Status Buffer U27026 enables the current condition of several signals to be read and is accessed with address $\overline{PCS0}$+0Xh through U27008. Refer to 2-2-1, Table 10.

BIT #	DEFINITION	SETTING	RESULT
D0	Current state of INTERR LED output from LED Control Register	0	LED is Off
		1	LED is On
D1	Current state of REPLY LED output from LED Control Register	0	LED is Off
		1	LED is On
D2	Conversion status of ADC (EOC)	0	Conversion in progress
		1	Conversion complete
D3	Ready status of DSP on Digital IF PC Board Assembly	0	DSP not ready
		1	DSP ready and working
D4	Monitor Enable status (JTB27001)	0	Enter Monitor (jumper installed)
		1	Normal operation (jumper not installed)
D5	ac Power status (CHARGE LED)	0	ac Power connected (Q27008 activated)
		1	ac Power not connected (Q27008 turned Off)
D6	Battery Charge Level status (BATTEST)	0	Battery ≈70% discharged (≈36 minutes left)
		1	Battery is charged
D7	Current state of LO CONTROL output from LED Control Register	0	Local Oscillator is enabled
		1	Local Oscillator is shut down

Status Buffer Bit Definition
Table 10

(k) LED Control Register

LED Control Register U27040 controls INTERR Indicator (18), REPLY Indicator (20), Local Oscillator and Digital IF PC Board Assembly reset operation. Refer to 2-2-1, Table 11. U27040 is accessed with address $\overline{PCS4}$+3Xh through U27036.

BIT #	DEFINITION	SETTING	RESULT
D0	Interrogation LED (INTERR Indicator [18])	0	Sets LED ready for turn On
		1	Initially Off or turns LED On for timed period
D1	Reply LED (REPLY Indicator [20])	0	Sets LED ready for turn On
		1	Initially Off or turns LED On for timed period
D2	LO Control	0	Enables Oscillator
		1	Shuts down Oscillator
D3	DSP Reset	0	Enables Digital IF PC Board
		1	Resets Digital IF PC Board
D4 to D7	Not used		

LED Control Register Bit Definition
Table 11

LED bit locations D0 and D1 are set high on power-up. An LED is turned on by writing zero and then one to the respective bit location in the control register. The zero to one transition triggers One-Shot Timer U27047. The high level output from U27047, timed for ≈62 ms, activates transistor Q27006 or Q27007 turning on the respective indicator.

(l) Digital IF PC Board Assembly Access

DPR U26007 on the Digital IF PC Board Assembly is accessed using $\overline{MCS0}$. Access is controlled by PAL U27029. DIR goes high to activate data lines through Transceiver U27009. $\overline{MEMR}$ goes low to read DPR or $\overline{MEMW}$ goes low to write to DPR.

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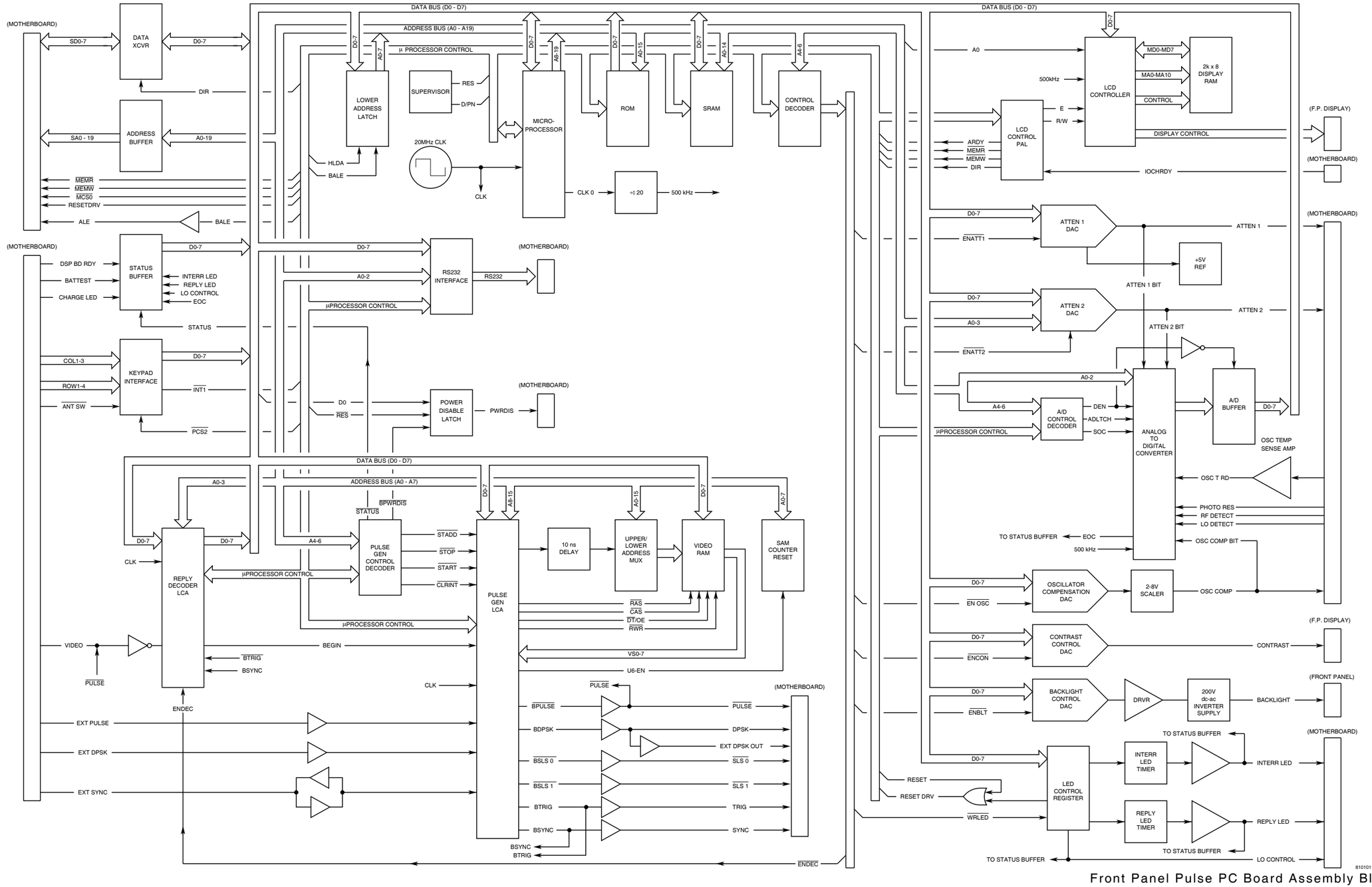
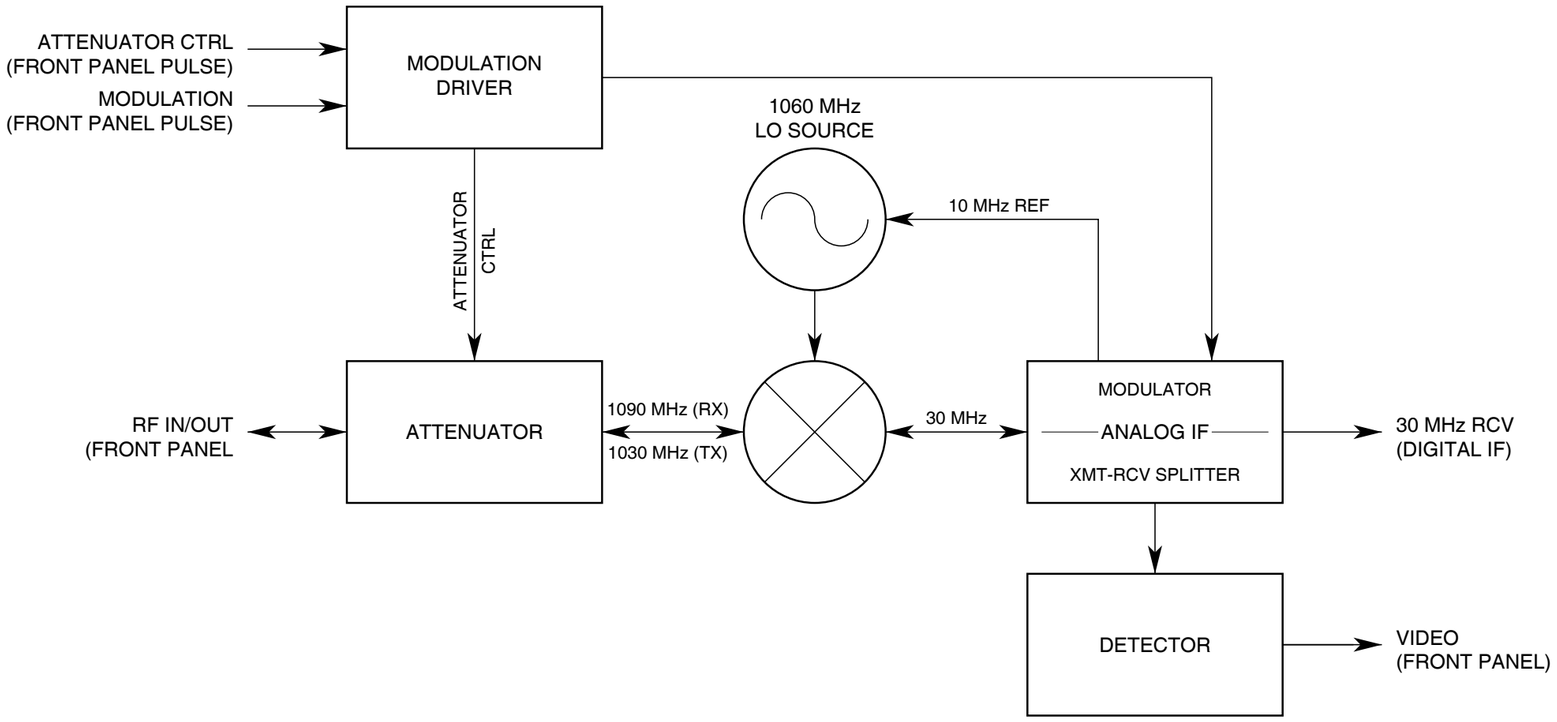


Front Panel Pulse PC Board Assembly Block Diagram
Figure 7



8101001

RF Assembly Block Diagram
Figure 8

(4) RF Assembly (2-2-1, Figure 8)

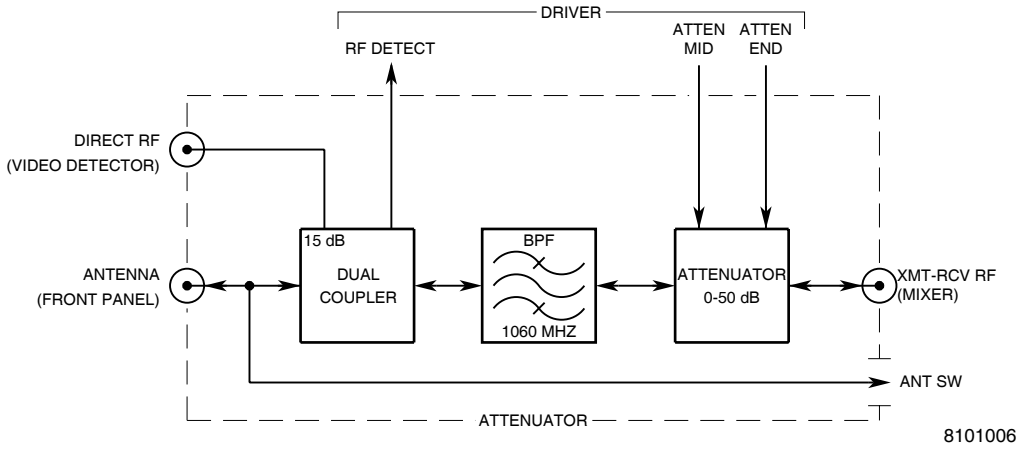
The RF Assembly consists of:

SSB Assembly
Driver PC Board Assembly
Detector Assembly
Analog IF Assembly

(a) SSB Assembly

The Single-Sideband (SSB) Assembly provides a two-way conversion between an IF of 30 MHz and an RF of 1030 MHz (transmit) or 1090 MHz (receive). The SSB Assembly consists of the Attenuator PC Board Assembly, LO Source PC Board Assembly and Mixer PC Board Assembly.

1 Attenuator PC Board Assembly (2-2-1, Figure 9)



Attenuator PC Board Assembly Block Diagram
Figure 9

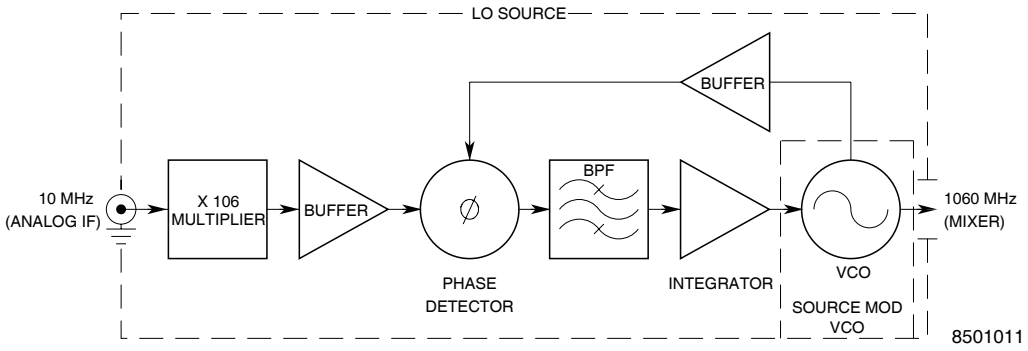
The Attenuator PC Board Assembly provides 0 to 50 dB of variable attenuation for measurement and testing purposes. The Attenuator PC Board Assembly consists of a dual coupler, bandpass filter and pin diode attenuator.

Dual Coupler HY31001 provides two RF signals, 15 dB down from the calibrated level at the ANTENNA Connector (J10057) (16). On transmit, one signal drives biased Diode Detector CR31001. CR31001 provides a dc level proportional to RF level and is used for the RF Detect test (Self Test). On receive or transmit, the signal is coupled, 15 dB down, to the RF I/O Connector (J10058) (15) through the Video Detector PC Board Assembly and Power Termination Assembly.

Microstrip Bandpass Filter HY31002 rejects signals outside the 300 MHz bandwidth (passes 910 to 1210 MHz signals).

The pin diode attenuator consists of four pin diodes (CR31003-CR31006) and associated components. The pin diodes are spaced 1/4 wavelengths apart and act as current controlled resistors. The Driver PC Board Assembly supplies the controlling current. Midline diodes (CR31004 and CR31005) provide most of the attenuation and end line diodes (CR31003 and CR31006) match the circuit. C31013 and C31015 (ATTEN 1060 MHz ADJ) tune out series inductance.

2 LO Source PC Board Assembly (2-2-1, Figure 10)



LO Source PC Board Assembly Block Diagram
Figure 10

The LO Source PC Board Assembly provides a 1060 MHz signal using a Voltage Controlled Oscillator (VCO). The frequency is kept tuned by a Multiplier, Phase Detector, Error Amplifier (Integrator) and Temperature Compensator.

The Digitally Controlled Crystal Oscillator (DCXO) from the Analog IF Assembly provides the 10 MHz frequency reference to the Multiplier. The reference signal drives the base of high current amplifier Q24002. Current controller Q24001 uses the regulated +11 V from the Driver PC Board Assembly to bias Q24002. The high level current output from Q24002 drives the multiplying veractor, Snap Diode CR24002. R24049 sets the voltage reference for CR24002. L24002 and C24004 provide impedance matching to increase the multiplying efficiency of CR24002. CR24002 generates 10 MHz spectral lines. C24005 and Z24001 form a Tank Circuit tuned to 1060 MHz, enhancing the 106th harmonic. The signal, monitored at TP16002, is fed into a three-stage linear Buffer amplifier consisting of saturable transistors, Q24003; Q24004 and Q24005. The Buffer amplifier, tuned to 1060 MHz, increases the power of the desired harmonic and drives an input to Phase Detector HY24001.

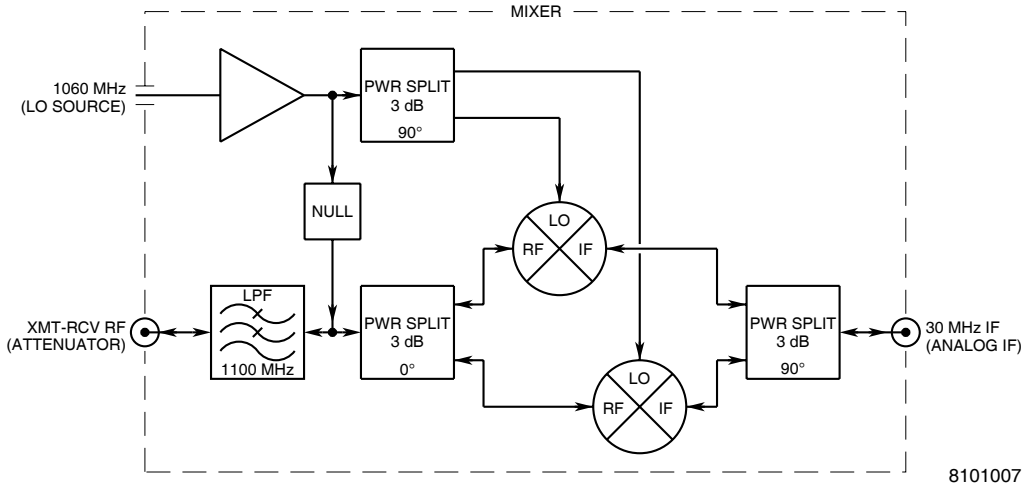
The other HY24001 input is from the Voltage Controlled Oscillator (VCO). Oscillating transistor Q24006, driven with a regulated +11 V from the Driver PC Board Assembly, is matched to the frequency determining element, Resonator Z24013 with Z24024, Z24025, Z24026, C24027, C24028 and C24029. Temperature compensator C24047 and Varactor CR24004 keep the oscillator tuned to 1060 MHz. Power is coupled off the oscillator through Z24014 and is fed through a Buffer amplifier, composed of saturable transistors Q24007, Q24008 and Q24009. The Buffer, also tuned to 1060 MHz, drives the local oscillator input to HY24001.

HY24001 and CR24003 form a Phase Detector providing a dc error voltage proportional to the phase difference detected between the VCO and Multiplier inputs. This voltage is filtered by Bandpass Filter C24021, L24006 and C24022 and sent to Integrator U24001.

When the output frequency of the VCO is the same as the output frequency of the Multiplier (Reference), the Phase Detector voltage (checked at TP16003) output to U24001 is minimal, causing negative feedback. U24001 and associated circuitry act as a phase-locked loop filter. When the frequencies of the VCO and Multiplier become different, U24001-3 becomes more positive. As the frequencies continue to be different, U24001 becomes a Wien Bridge Oscillator. The ac output is fed to the VCO tuning Varactor CR24004. CR24004 adjusts the resonating frequency, fed to HY24001, until error voltage is reduced down and U24001 becomes a phase-locked loop filter again. R24022 (OFFSET) sets a voltage level compensating for imbalances in the Phase Detector and/or Buffers and R24025 (DEVIATION) sets the ac deviation voltage limit to prevent the VCO from setting on the 105th or 107th harmonics.

Q24010 and Q24011 provide temperature compensation. While Q24010 exponentially increases current with temperature, Q24011 is the high impedance load providing temperature compensated voltage to VCO Varactor CR24004. VCO Tune Voltage, nominally 4 Vdc, is checked at TP16001 and is set by R24026 (TUNING).

3 Mixer PC Board Assembly (2-2-1, Figure 11)



Mixer PC Board Assembly Block Diagram
Figure 11

The Mixer PC Board Assembly uses the 1060 MHz source signal to convert the 30 MHz transmit signal to 1030 MHz and the 1090 MHz receive signal to 30 MHz. The Mixer PC Board Assembly consists of a low-pass filter, LO amplifier, mixer null and single-sideband mixer.

The low-pass filter (C18022, L18016, C18023, L18017 and C18024) removes odd harmonics passed by the Attenuator PC Board Assembly. The low-pass filter consist of a lumped element five pole filter with an elliptical response and provides 1.5 GHz of bandwidth.

The LO amplifier (Q18001, Q18002, Q18003, Q18004 and associated components) provides the necessary gain (≈20 dBm output) to drive the single-sideband mixer after driving the mixer null. Input from the LO Source PC Board Assembly (≈0 dBm) is fed to base of transistor Q18002. Q18002 is constant-current biased through Q18004 collector for a gain of ≈10 dB at base of Q18003. Q18003 is constant-current biased through Q18001 collector for another gain of ≈10 dB.

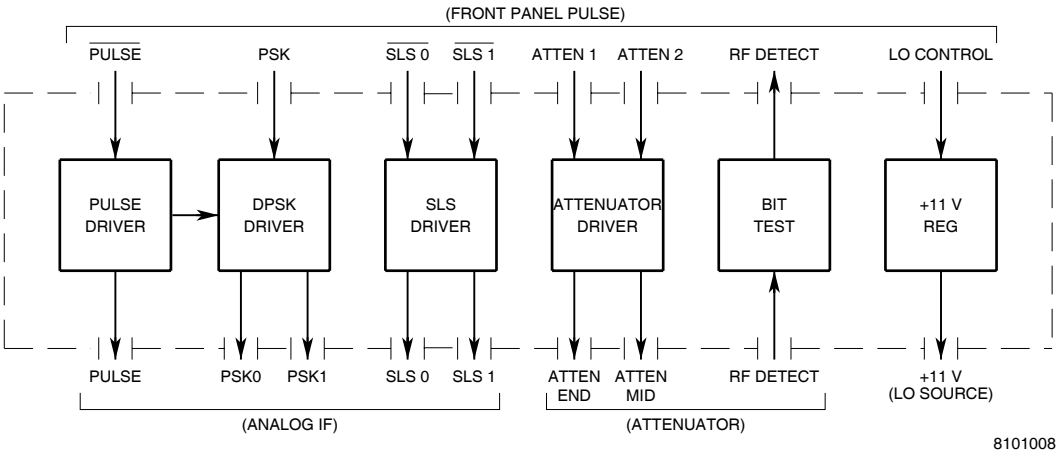
The mixer null adds four vectors, set 90° apart with phase shifts along Transmission Line HY18001. The amplified LO source signal is fed into discrete splitter (L18020, C18031, R18022, L18021 and C18032). One signal is sent to the single-sideband mixer. The other is used as a reference by the mixer null. HY18001 and the summing network filter out 1060 MHz at any phase from the transmit and receive signals going through the single-sideband mixer at Power Splitter HY18002. R18007 and R18008 (1060 MHz NULL ADJ) control the level. L18018 and L18019 tune out stray capacitance on adjusting resistors.

The single-sideband mixer splits the transmit (30 MHz IF), receive (1090 MHz) and LO source (1060 MHz) signals into two each. The resulting signals are phase shifted and summed together, canceling the image sideband (upper sideband on transmit, lower sideband on receive). The LO source signal is split by quadrature microstrip HY18003. One signal at 0° is fed into High-Level Mixer MXR18002 and the other signal at 90° is fed into High-Level Mixer MXR18001. C18034 (1090 MHz NULL PHASE ADJ) sets phase of LO source signal input to MXR18001 for complete sideband cancellation.

On transmit, the 30 MHz signal from the Analog IF PC Board Assembly is split by T18001, C18017 and R18014. The two signals, 90° apart, pass through all-pass filters tuned to maintain equal levels (R18013 and R21015, 1090 MHz NULL AMPLITUDE ADJ) and 90° separation (C18013 and C18015, 1090 MHz NULL PHASE ADJ) One signal (in phase) is fed into MXR18002. MXR18002 mixes the 30 MHz with the 1060 MHz for a mixed output of 1090 MHz and 1030 MHz. The other signal (90° out of phase) is fed into MXR18001. MXR18001 mixes the 30 MHz at 90° with the 1060 MHz at 90° for an output of 1090 MHz at 180° and 1030 MHz at 0°. The signals are added together through Power Splitter HY18002 with the 1090 MHz signals canceling each other leaving the 1030 MHz transmit signal.

On receive, the 1090 MHz signal from the Attenuator PC Board Assembly is split through Power Splitter HY18002. One signal is fed into MXR18002. MXR18002 mixes the 1090 MHz with the 1060 MHz (both in phase) for a mixed output of 30 MHz. (2150 MHz is out of bandwidth.) The other signal is fed into MXR18001. MXR18001 mixes the 1090 MHz at 0° with the 1060 MHz at 90° for an output of 30 MHz at -90°. Signals are sent through the respective all-pass filters and are added together through T18001. Adding the 90° separation factor sets the 30 MHz signal from MXR18001 back to 0°.

(b) Driver PC Board Assembly (2-2-1, Figure 12)



Driver PC Board Assembly Block Diagram
Figure 12

The Driver PC Board Assembly drives the modulating and level control signals from the Front Panel Pulse PC Board Assembly to the Analog IF PC Board and Attenuator PC Board Assemblies. The Driver PC Board Assembly also provides the +11 V for the LO Source PC Board Assembly, the voltage to bias pin attenuator diodes on the Video Detector PC Board Assembly and voltage sources from the Power Supply Assembly to the rest of the RF Assembly. The Driver PC Board Assembly consists of the attenuator drivers, +11 V regulator, SLS level drivers, modulation drivers, RF BIT level driver and Direct Connect Power Adjust.

ATTEN2 line voltage from Front Panel Pulse PC Board Assembly (0 to 10 Vdc) across R20005 sets a voltage controlled current source supplying collector current for half of Q20001. The other half of Q20001 remains constant as determined by R20052 and R20009. Q20001 and associated components form a logarithmic converter. Q20002 and associated components form an exponential amplifier. Both amplifier circuits cascaded together form a power function converter with independent adjustments for gain (R20010, 50 dB ADJ OFFSET) and exponent (R20016, 10 dB ADJ SLOPE). R20009 (ZERO VOLT ADJ) allows independent adjustment of R20010 and R20016. Operational amplifier U20002B, set by power function converter (Q20002-1) and Q20003 feedback, biases Q20003, controlling current flow through midline attenuator diodes on the Attenuator PC Board Assembly. The output voltage of RT20002 and associated components provide temperature compensation for pin diode slope changes over temperature. ATTEN1 line voltage (0 to 10 Vdc from Front Panel Pulse PC Board Assembly) across linear converter amplifier controls the current through end line pin attenuator diodes on the Attenuator PC Board Assembly. Operational amplifier U20001A, set by ATTEN1 line voltage and Q20005 feedback inputs, biases Q20005, controlling current flow. R20019 (VSWR 50 dB ADJ) sets the reference current through Q20005.

Voltage regulator U20008 provides the +11 V to operate the Multiplier on the LO Source PC Board Assembly. U20008 is switched On or Off by the LED Control Register on the Front Panel PC Board Assembly.

SLS level drivers U20005B and U20005C invert the active low $\overline{SLS0}$ and $\overline{SLS1}$ signals from the Front Panel Pulse PC Board Assembly. The output signals, SLS0 and SLS1, bias the SLS gain amplifier output level diodes. Refer to 2-2-1, Table 13 for transmit gain settings.

Modulation drivers convert the modulating signals from the Front Panel Pulse PC Board Assembly to levels necessary to modulate the 30 MHz IF on the Analog IF PC Board Assembly. Active low $\overline{PULSE}$ is inverted by U20006C and sent to Analog IF PC Board Assembly as active high PULSE. $\overline{PULSE}$ is also inverted by U20006A to enable DPSK modulation. DPSK modulation is set according to 2-2-1, Table 12. Phase is only shifted when $\overline{PULSE}$ is active (during P_6 of Mode S interrogation).

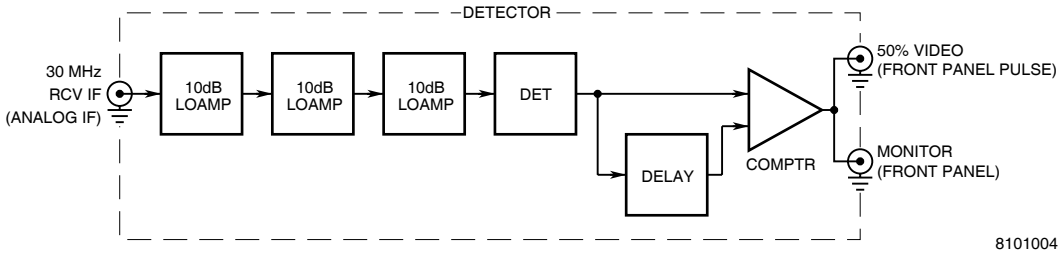
PSK	$\overline{PULSE}$	U20006A OUT	U20005D OUT	U20006B OUT/PSK1	U20005A OUT/PSK0	PHASE
Low	Low	High	High	Low	High	0°
High	Low	High	Low	High	Low	180°
High	High	Low	High	High	High	N/A
Low	High	Low	Low	High	High	N/A

DPSK Modulation
Table 12

The RF BIT level driver biases the diode detector CR31001 on the Attenuator PC Board Assembly. Transmit level detected across CR31001 is used in setting the RF DETECT line during the RF Detect test (Self Test). U20007 output is 0 Vdc when nothing is detected to 2.8 Vdc when transmit level is highest (MTL+4 dB with no attenuation). CR20001 matches U20007-3 input and R20029 (ZERO ADJ) adjusts bias to set U20007 output to 0 Vdc when nothing is transmitted (U20007-3 input ≈-0.3 Vdc). R20032 (RF DET ADJ) sets output voltage to correct level when Test Set is transmitting.

R20020 (DIRECT CONNECT POWER ADJ) adjusts the voltage from 0 to +12 Vdc to bias the pin attenuator diode on the Video Detector PC Board Assembly. R20020 calibrates the RF I/O Connector (J10058) (15) level to -48.25 dB relative to the ANTENNA Connector (J10057) (16) level.

(c) Detector Assembly (2-2-1, Figure 13)



Detector Assembly Block Diagram
Figure 13

The Detector Assembly converts the 30 MHz, pulse modulated input from the Analog IF PC Board Assembly to a TTL level output, preserving original pulse width. The TTL level signal is sent to the Reply Decoder on the Front Panel Pulse PC Board Assembly for decoding. The output signal is monitored through the MONITOR Connector (J10056) (19) on the Front Panel Assembly. The Detector Assembly has a detection range of ≈30 dB (-27 dBm to +3 dBm). Detector Assembly circuits, located on the Detector PC Board Assembly, include the Logarithmic Amplifiers, Detector and Comparator.

1 Logarithmic Amplifiers

The Detector PC Board Assembly has three stages of cascade coupled Logarithmic Amplifiers (Q21001, Q21002, Q21003 and associated components) providing a total gain of ≈30 dB. Each amplifier has ≈10 dB gain, calculated by the collector impedance (set by resistors R21004, R21011 and R21018) divided by the emitter impedance. The resting current through emitter logging diodes (CR21001, CR2002 and CR21003) shunts the emitter resistance, effectively causing the small emitter impedance to change with the input level. With low input levels, emitter impedance is low and gain is high. As input level increases, emitter impedance increases logarithmically and gain decreases, approaching unity gain until compression is reached.

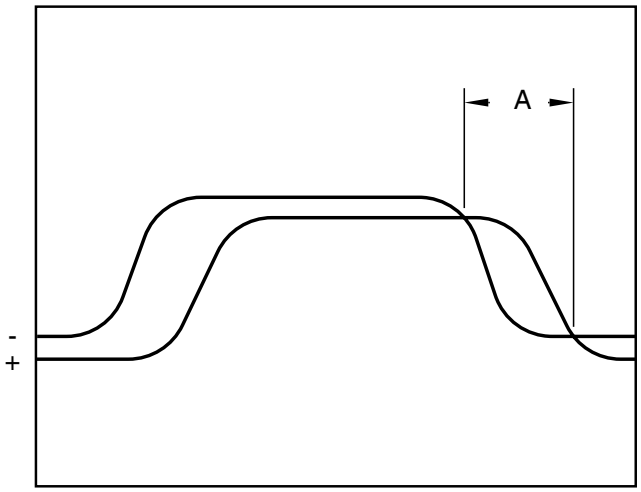
2 Detector

The balanced Detector preserves envelope detection efficiency and consists of an unbalanced to balanced Transformer T21001, Diode CR21004, dual transistor buffer (Q21005 and Q21008) and detector filter (C21018, L21006, C21019, C21020, L21007, C21021, C21022 and R21039). CR21004 balances the output of T21001 and provides a 60 MHz positive half-wave, the width of the modulating pulse, to the dual transistor buffer. The detector filter has a 6.5 MHz bandwidth and a flat time delay response to preserve pulse shape. The detector filter removes the 60 MHz from the detected pulse.

3 Comparator

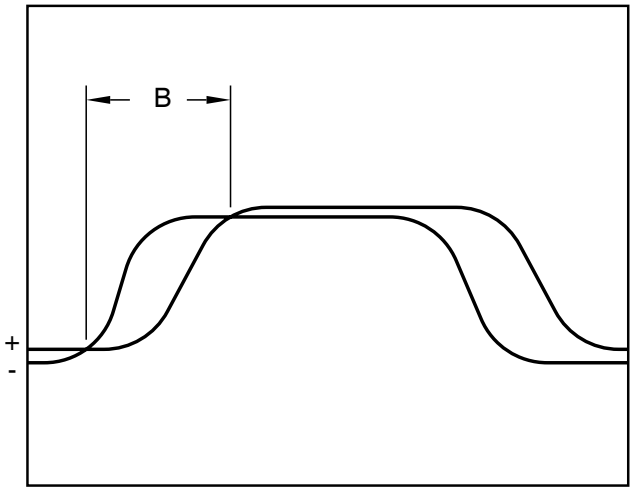
After detection, the signal is split into two paths: primary and delayed. Buffers Q21008 and Q21009, provide the load for the detector filter. The delayed signal at Q21009 emitter is set through the delay filter (C21024, L21008, C21025, C21026, L21009, C21027, L21010 and C21028). The delay filter has a bandwidth of ≈10 MHz and a flat time delay of 120 ns. The delayed signal is referenced using a resistor network (R21060 and R21046) and applied to the positive inputs to Comparators U21001A, U21001B and U21004A. The primary signal is split. One primary signal is dc adjusted by R21061 to provide a higher level than the delayed signal and is applied to the negative input to trailing edge Comparator U21001A. Refer to 2-2-1, Figure 14 for trailing edge comparator input signals. The other primary signal, applied to the negative input to leading edge Comparator U21001B, is set lower than the delayed signal. Refer to 2-2-1, Figure 15 for leading edge comparator input signals. When preserving correct pulse width, slicing occurs at the 50% amplitude points for a linear pulse. Offsetting input signals cause the comparators to slice pulse 6 dB down (≈-0.15 V), compensating for the level set by the Logarithmic Amplifiers. Comparator outputs provide the clocks for D Flip-Flops U21002A and U21002B. The pulses, shown in 2-2-1, Figure 16; have widths about equal to the filter delay (A and B) and are spaced (rising edge to rising edge) approximately equal to the input pulse width minus the filter delay (C). U21002A, triggered by the leading edge clock, has a negative pulse output to NAND Gate U21003A. U21002B, triggered by the trailing edge clock, resets U21002A through U21003B and U21003C. U21002A $\overline{Q}$ output provides the other input to NAND Gate U21003A. R21058 (PULSE WIDTH) and C21035 provide a timed delay in triggering the One-shot U21003D to reset U21002B. The timed delay provides compensation for the filter delay, offset between flip-flops and comparator delays. The original pulse shape is restored at the output of U21003A. Reset Comparator U21004A and associated circuitry reset U21002A at low signal levels when there is a high output (U21003A-3) with a low input (U21004A-4). The Detector Assembly output is sent to the Reply Decoder on the Front Panel Pulse PC Board Assembly and MONITOR Connector (J10056) (19) on the Front Panel Assembly, balanced by R21056 and R21057 for 50 Ω impedance matching.

NOTE: The leading edge comparator is set to be more sensitive than the trailing edge comparator to eliminate flip-flop reset during DPSK transitions.



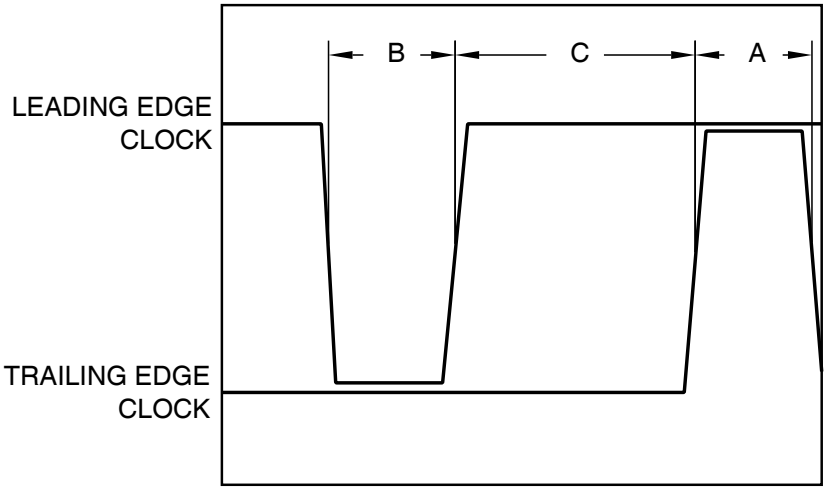
8116015

Trailing Edge Comparator Input Signals
Figure 14



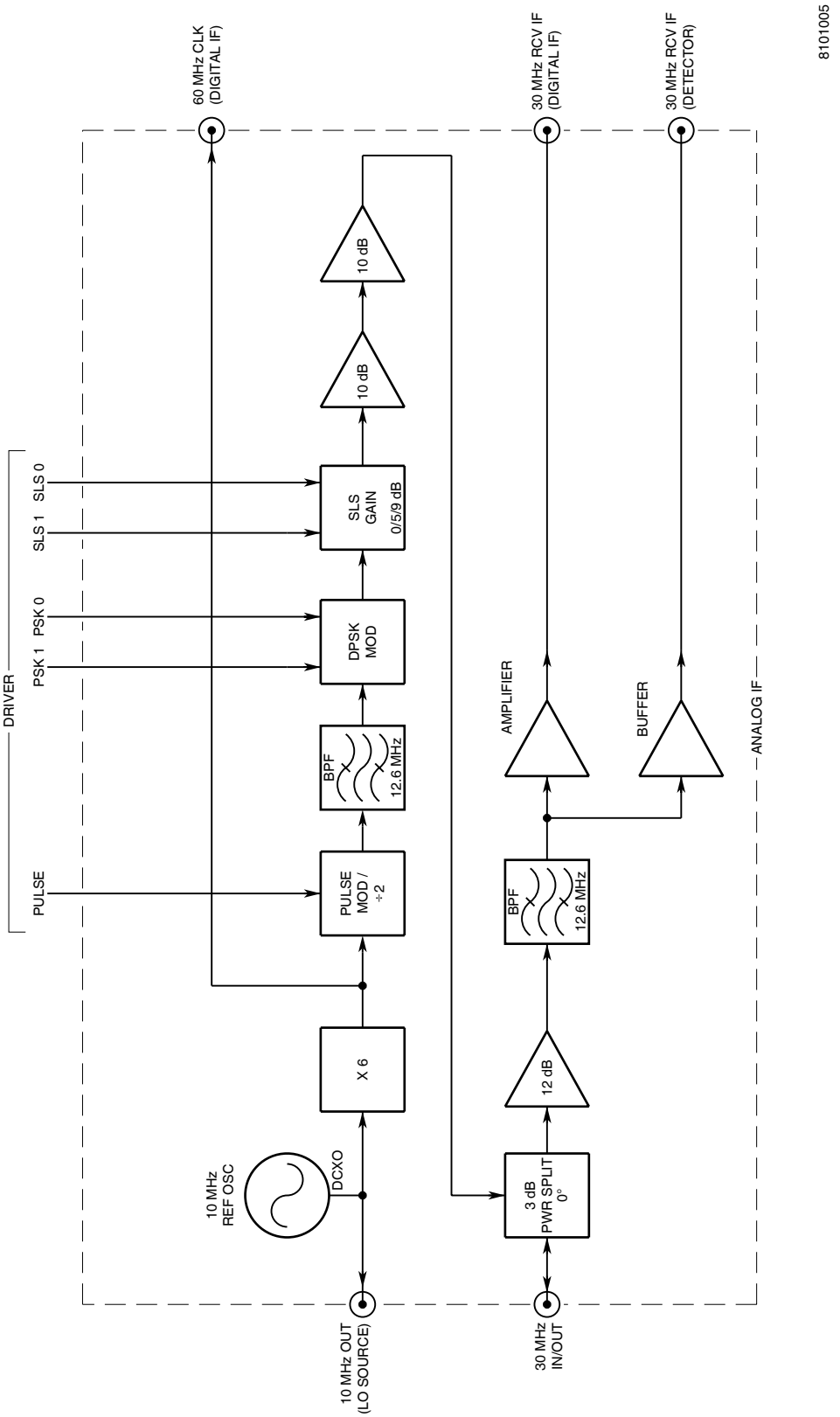
8116016

Leading Edge Comparator Input Signals
Figure 15



8116017

Detector Comparator Pulses
Figure 16



Analog IF Assembly Block Diagram
Figure 17

(d) Analog IF Assembly (2-2-1, Figure 17)

The Analog IF Assembly provides the 10 MHz reference used by the LO Source PC Board Assembly, provides the 60 MHz clock for the Digital IF PC Board Assembly, adds pulse and DPSK modulation to transmit signal and provides temperature compensation. The Analog IF Assembly circuits, contained on the Analog IF PC Board Assembly are: 10 MHz DCXO, Transmit and Receive.

1 10 MHz DCXO

The Digitally Controlled Crystal Oscillator (DCXO) provides a temperature compensated 10 MHz signal. The temperature of the oscillator is transmitted as a voltage to the ADC (Front Panel Pulse PC Board Assembly) by temperature sensor (CR22001). R22001 calibrates CR22001 output voltage. The Front Panel Pulse PC Board Assembly uses the temperature sensor voltage to set contrast on the DISPLAY (14) and provide the correct voltage to drive the DCXO for an output of 10 MHz (±30 Hz) across the temperature range (-20° to +50° C). The corrected voltage (+2 to +8 Vdc) across CR22002 drives the oscillator (Y22001, Q22001 and associated circuitry). C22004 adjusts frequency. At 27° C, R22001 is adjusted to provide +3 Vdc (FL19007) and C22004 is adjusted for 10 MHz (±3 Hz). After amplification by Q22002, the 10 MHz signal is split. One signal is buffered by Q22003 for 1 Vp-p output to the LO Source PC Board Assembly. The other signal is buffered by Q22004 in the Transmit section.

2 Transmit

The 10 MHz signal from the DCXO passes through low-pass filter (C22018, L22002 and C22019) to the X6 Multiplier Transistor Q22005. The 60 MHz bandpass filter (L22003, L22005, L22007, and associated components tuned to the sixth harmonic) provides 60 MHz with a 3 MHz bandwidth. After amplification by Q22006, the 60 MHz signal is split. One signal is buffered by Q22007 for 1 VP-P clock output to the Digital IF PC Board Assembly. The other signal clocks D Flip-Flop U22001B. U22001B, pins 8 and 12 are connected together to divide the signal by two for a 30 MHz output. The active low pulse signal from the Front Panel Pulse PC Board Assembly pulse modulates the signal through U22001B-10.

Resistors R22040 and R220041 reduce amplitude by 10 (checked at TP22003). The transmit bandpass filter is a four pole Bessel wideband filter consisting of four series resonators (C22036-L22010, C22038- L22011, C22040-L22012 and C22042-L22012). The transmit filter is centered at 30 MHz with a 3 dB bandwidth across 12.6 MHz. Signal delay, from U22001B through the transmit filter, shapes the transmit pulse by providing ≈70 ns of rise time.

Mixer MXR22001 adds DPSK modulation. Phase shifting of 0° or 180° is controlled by PSK0 and PSK1 inputs from the Driver PC Board Assembly and set by the Front Panel Pulse PC Board Assembly. When PSK0 is Low and PSK1 is High, phase shift is 0°. When PSK0 is High and PSK1 is Low, phase shift is 180°.

SLS gain amplifier Q22008 provides three output levels according to the SLS0 and SLS1 input lines from the Driver PC Board Assembly. SLS0 line level biases diodes CR22007 and CR22013). SLS1 line level biases diodes CR22006 and CR22012. Refer to 2-2-1, Table 13. R22049 (TX GAIN) adjusts output level of amplifier Q22009. Q22009 provides 10 dB gain for a maximum output of +10 dBm. Inductive coupler L22020 decreases current and increases voltage. Q22010 is the final output amplifier, increasing the 30 MHz IF signal level to ≈+18 dBm. Q22010 emitter circuitry (RT22001, R22055 and R22056) provides temperature compensation for the total transmit circuits. L22027 provides 40 dB isolation between transmit and receive. C22055 and R22062 (ISOLATION) are adjusted for maximum isolation.

SLS0	SLS1	GAIN	NAME	TO UUT
Low	Low	0 dB	SLS	MTL-5
High	Low	5 dB	Background	MTL
High	High	9 dB	Foreground	MTL+4
Low	High	Not Applicable		

Transmit Gain Settings
Table 13

3 Receive

The receive signal, 30 MHz IF from the Mixer PC Board Assembly, is reduced 3 dB by L22027 and applied to Amplifier Q22011. Q22011 amplifies signal 12 dB and provides a 50 Ω output to drive the receive filter. The receive bandpass filter is a four pole Bessel wideband filter comprises series resonators L22029-C22060, L22030-C22062, L22031-C22064 and L22032-C22066. The receive filter has a flat time domain response between the 3 dB points and is centered at 30 MHz with a 12.6 MHz bandwidth. Output is split into two signals. Q22013 buffers and sends one signal to the Detector PC Board Assembly through J19033. Emitter-follower Q22012 amplifies the other signal. R22073 (RX GAIN) adjusts received level. Q22014, with a 50 Ω output, drives the 30 MHz receive signal to the Digital IF PC Board Assembly through J17034 (≈+3 dBm). Q22014 emitter circuitry (RT22002, R22082 and R22084) provides temperature compensation for the total receive circuits.

(5) Front Panel Assembly

The Front Panel Assembly consists of:

Video Detector PC Board Assembly
Power Termination Assembly
Front Panel LED PC Board Assembly
LCD
Keypad

(a) Video Detector PC Board Assembly

The Video Detector PC Board Assembly provides a linear display of UUT replies on the oscilloscope when Test Set is directly connected to UUT. The Video Detector PC Board Assembly also provides a calibrated attenuation of the direct connection signal.

The direct connection receive signal from the Power Termination Assembly or transmit signal from the Attenuator PC Board Assembly is split by a resistive power splitter (R30010, R30002 and R30003). One signal is linearly detected by Schottky Barrier Diode CR30001. Capacitor C30003 is a printed element to provide for fast detection. The detected signal is sent to the REPLY VIDEO Connector (J10054) (17). On receive, the other signal has attenuation level set across a resistive divider (R30011 and R30012). Current through Pin Diode CR30002, controlled by the biasing voltage set on the Driver PC Board Assembly, provides ≈1 dB of attenuation adjustment. Attenuation level is calibrated for accurate power and MTL measurements. On transmit, the other signal is attenuated before splitting and going to the Power Termination Assembly.

(b) Power Termination Assembly

The Power Termination Assembly provides a 50 Ω termination for the UUT and protects the ATC-601-2 Test Set against excessive incoming power through the RF I/O Connector (J10058) (15). The Power Termination Assembly is in the transmit and receive circuit only when a direct connection with UUT is used. The Power Termination Assembly connects the RF I/O Connector (J10058) (15) through P/J28028 with the Video Detector PC Board Assembly through P/J28029.

Transmit and Receive signals are reduced 20 dB across Directional Coupler HY28001. Excessive incoming power and stray spikes are dissipated off through R28002. C22001 and L22001 keep the circuit frequency balanced for 50 Ω impedance.

(c) Front Panel LED PC Board Assembly

The Front Panel LED PC Board Assembly consists of three indicator circuits and a light sensor used in the LCD Backlight Control circuit.

The INTERR Indicator (18) illuminates red when an interrogation is transmitted. When activated, a ground on the emitter of Q27006 (Front Panel Pulse PC Board Assembly) completes the circuit across LED CR13001.

The REPLY Indicator (20) illuminates red when a valid reply is received. When activated, a ground on the emitter of Q27007 (Front Panel Pulse PC Board Assembly) completes the circuit across LED CR13002.

The CHARGE Indicator (1) illuminates only when the Battery Charger on the Power Supply Assembly is operating. The CHARGE Indicator (1) illuminates green (battery is >80% charged) when current flows from the +15 V source through LED CR13003 to the Power Supply Assembly (BATT CHARGER LED line). The circuit is completed through CR27010 and the activated transistors, Q27013 and Q14014.

The CHARGE Indicator (1) illuminates red (battery requires charging) when current flows from the Battery Charger on the Power Supply Assembly through CR27011 and the activated Q27015 to LED CR13003.

Voltage across light sensitive Photo Resistor R13001 is sent to the ADC on the Front Panel Pulse PC Board Assembly. The Front Panel Backlighting voltage to the LCD is adjusted accordingly.

(d) LCD (Modified LCD Display PC Board Assembly)

The LCD is a 64 line by 240 column dot display. The LCD requires 4.75 to 5.25 V (J12059-7) to run logic. +5 V is nominal for ATC-601-2. The LCD drive voltage required is -5.25 to -4.75 V (J12059-9). -5.1 V is nominal for ATC-601-2.

(e) Keypad

The Keypad, consisting of ten keys, is contained in the ATC-601-2 Overlay. When activated, each key momentarily closes contacts between a row ($\overline{\text{ROW}}$) line and column ($\overline{\text{COL}}$) line. Row and column lines go to the Front Panel Pulse PC Board Assembly. Keys operate with <20 ms switch bounce.