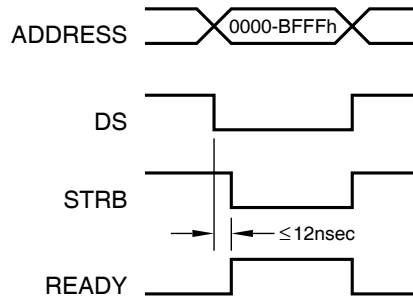
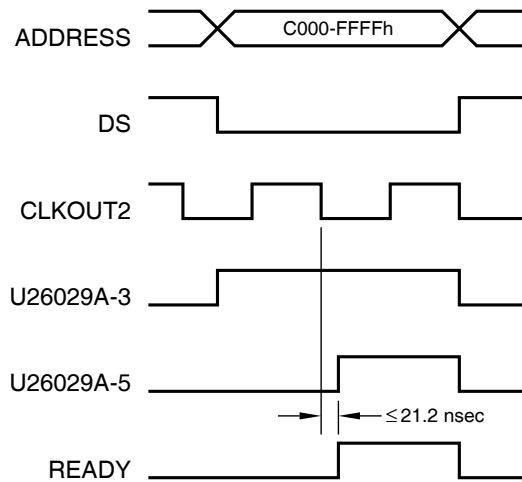


## APPENDIX D - TIMING DIAGRAMS

### 1. Digital IF PCB Assy



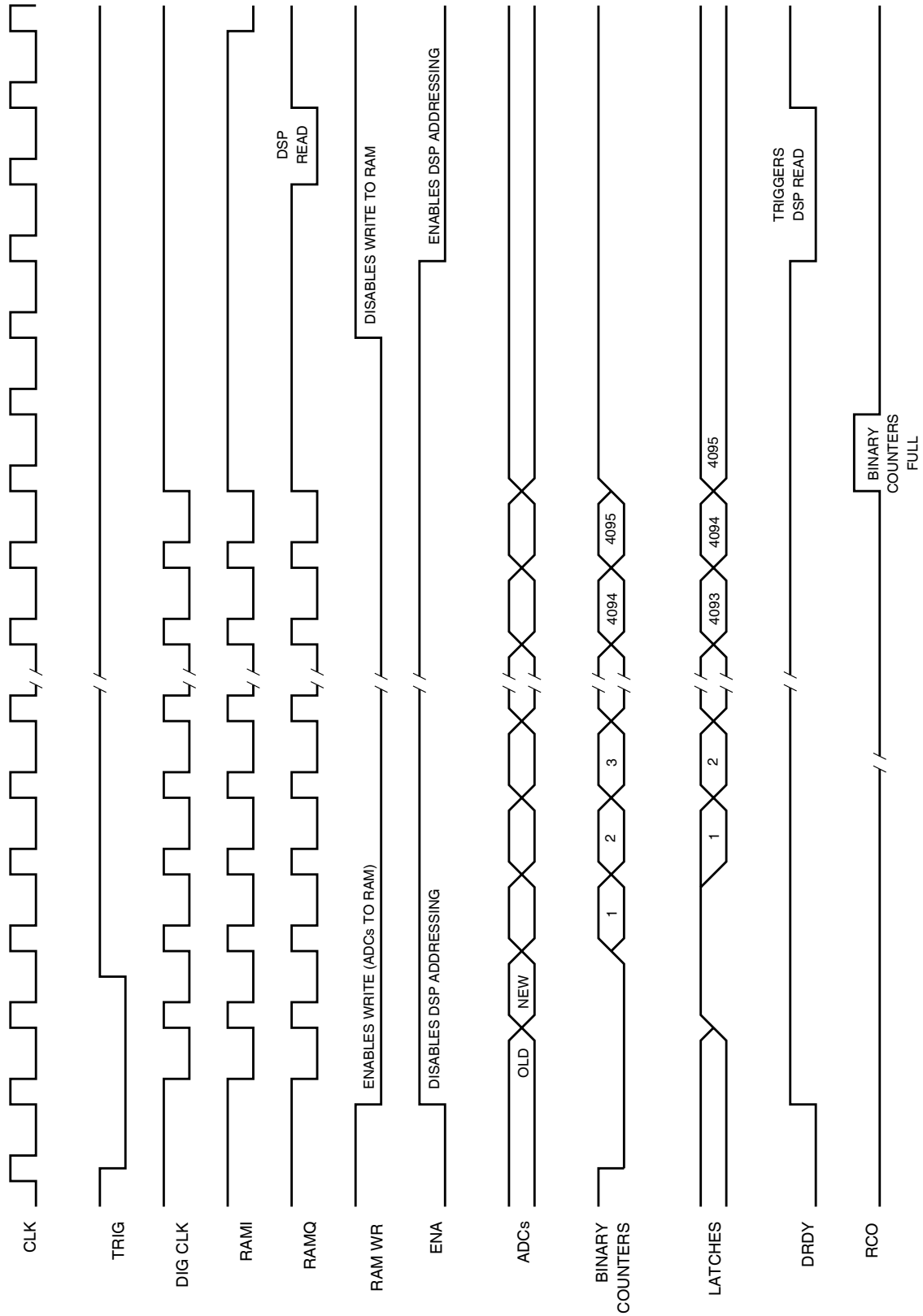
0 WAIT STATES



1 WAIT STATE

8514011

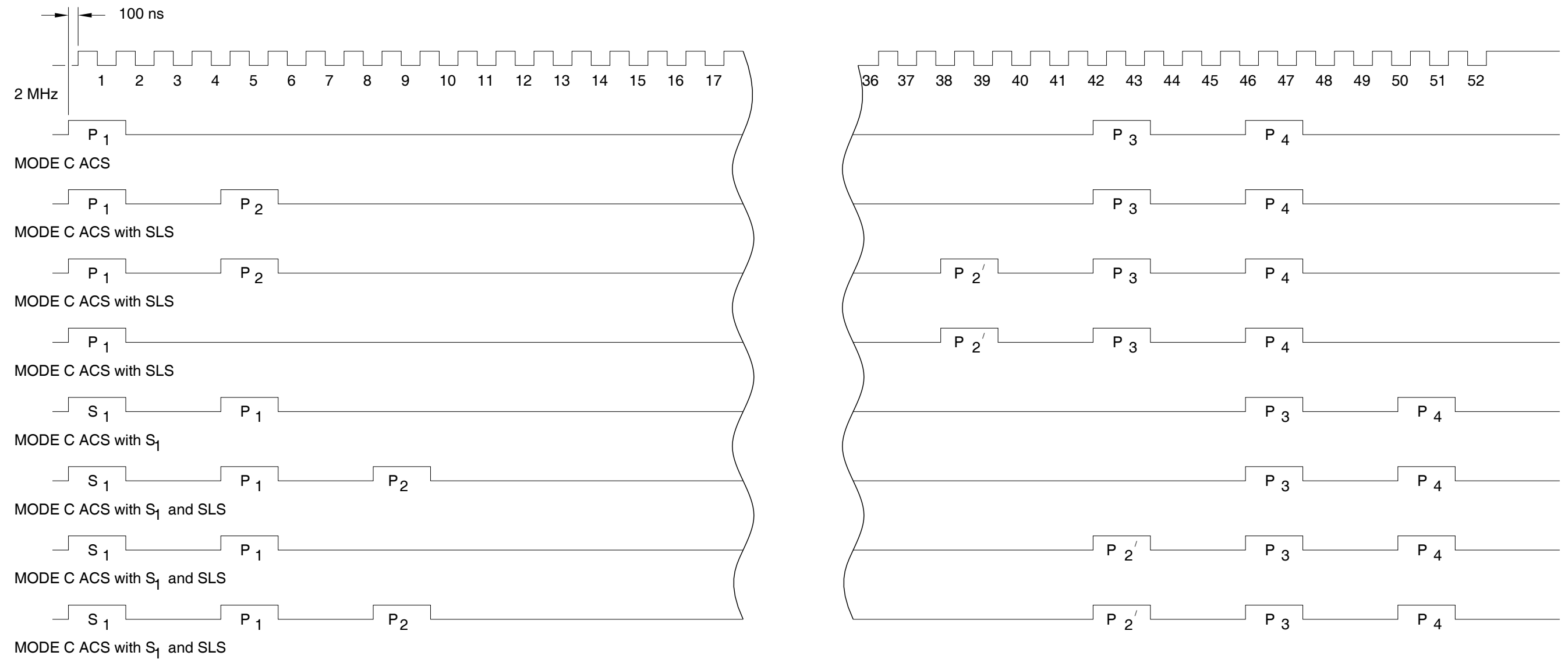
System Interface PAL Wait States  
Figure 1



8514006

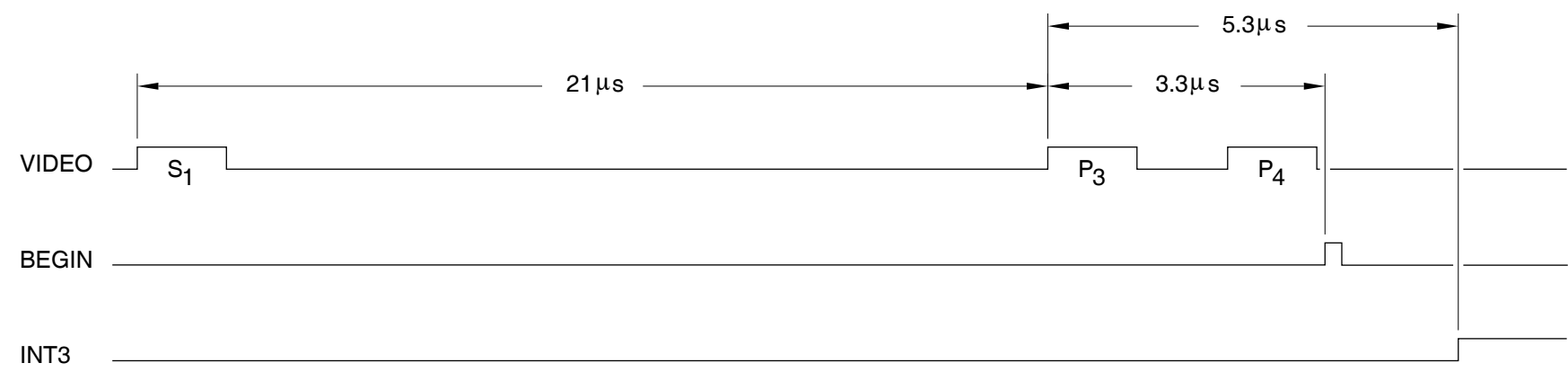
Digitizer  
Figure 2

2. Front Panel Pulse PCB Assy

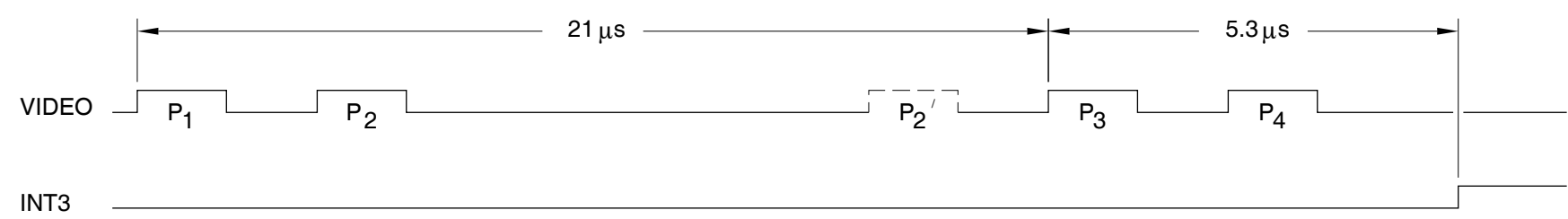


**NOTE:** P<sub>2</sub>' IS AN ADDITIONAL SLS CONDITION.

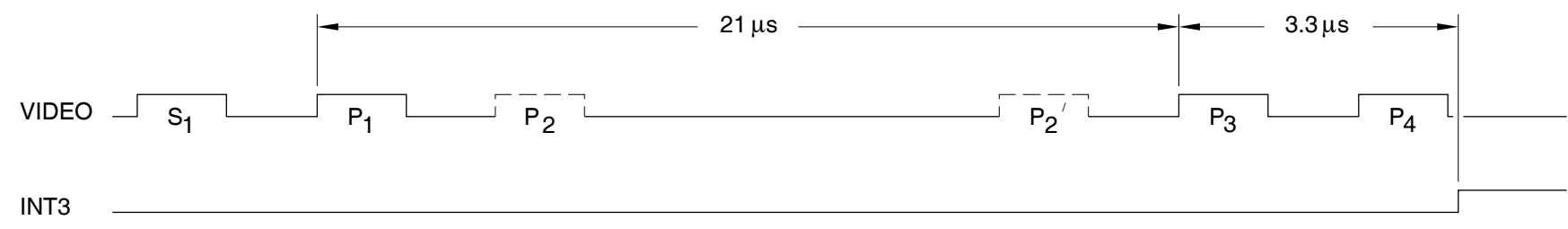
8514001  
Mode C Timing  
Figure 3



MODE C ALL CALL with NO SUPPRESSION



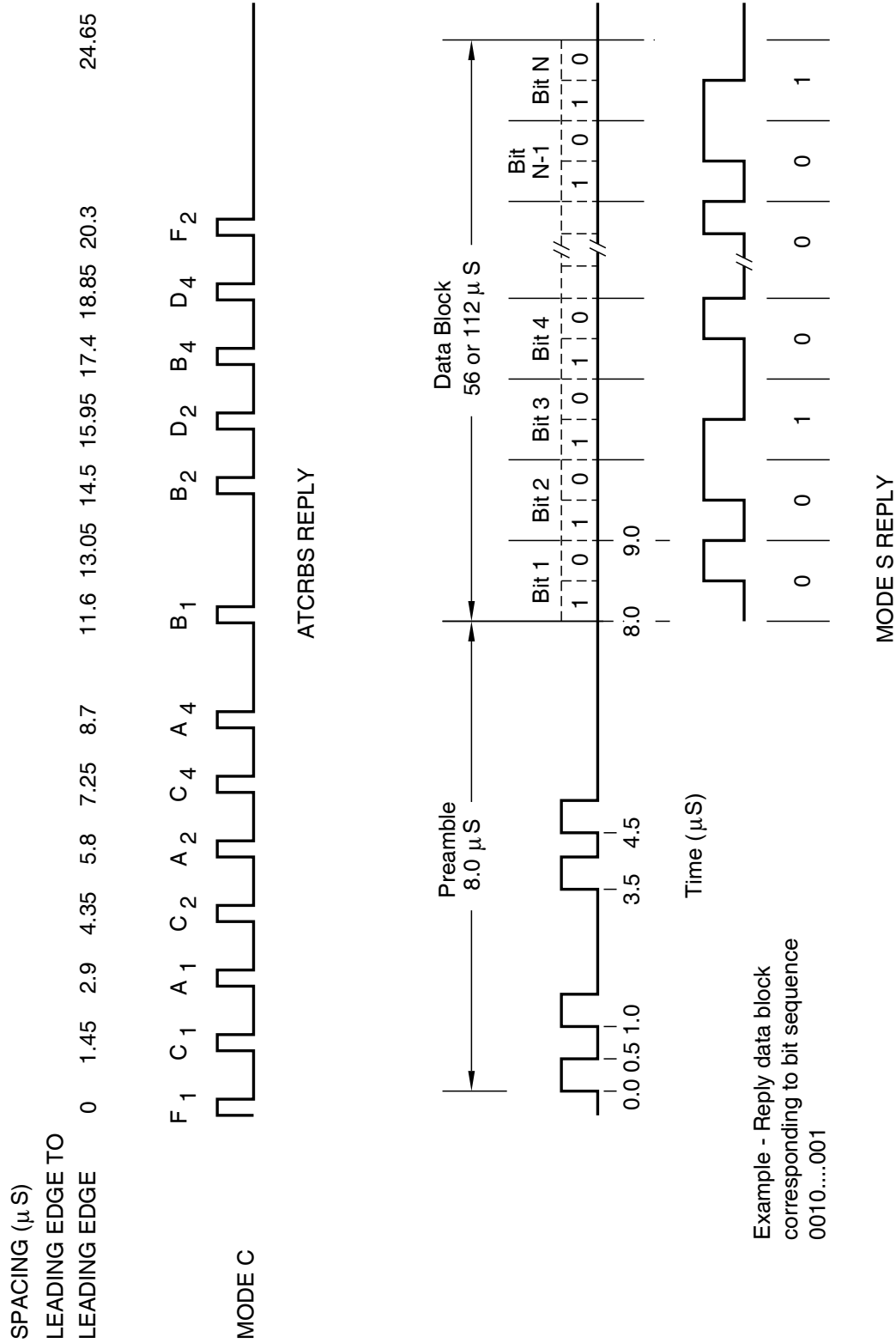
MODE C ALL CALL with SLS



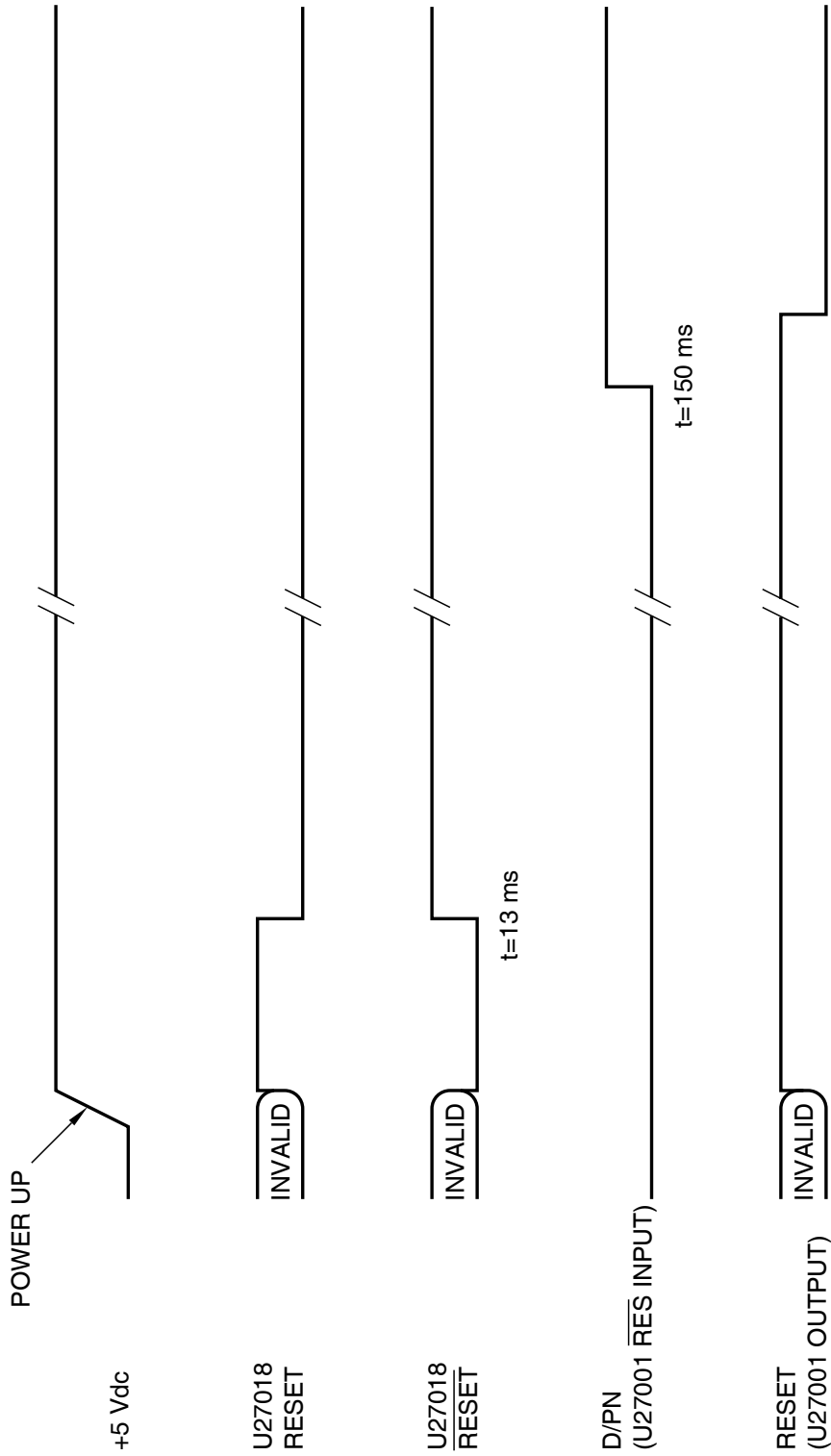
MODE C ALL CALL with S<sub>1</sub> PULSE (with or without SLS)

ATCRBS Interrogations Interrupt and Pulse Generator Trigger Timing  
Figure 4

8514002

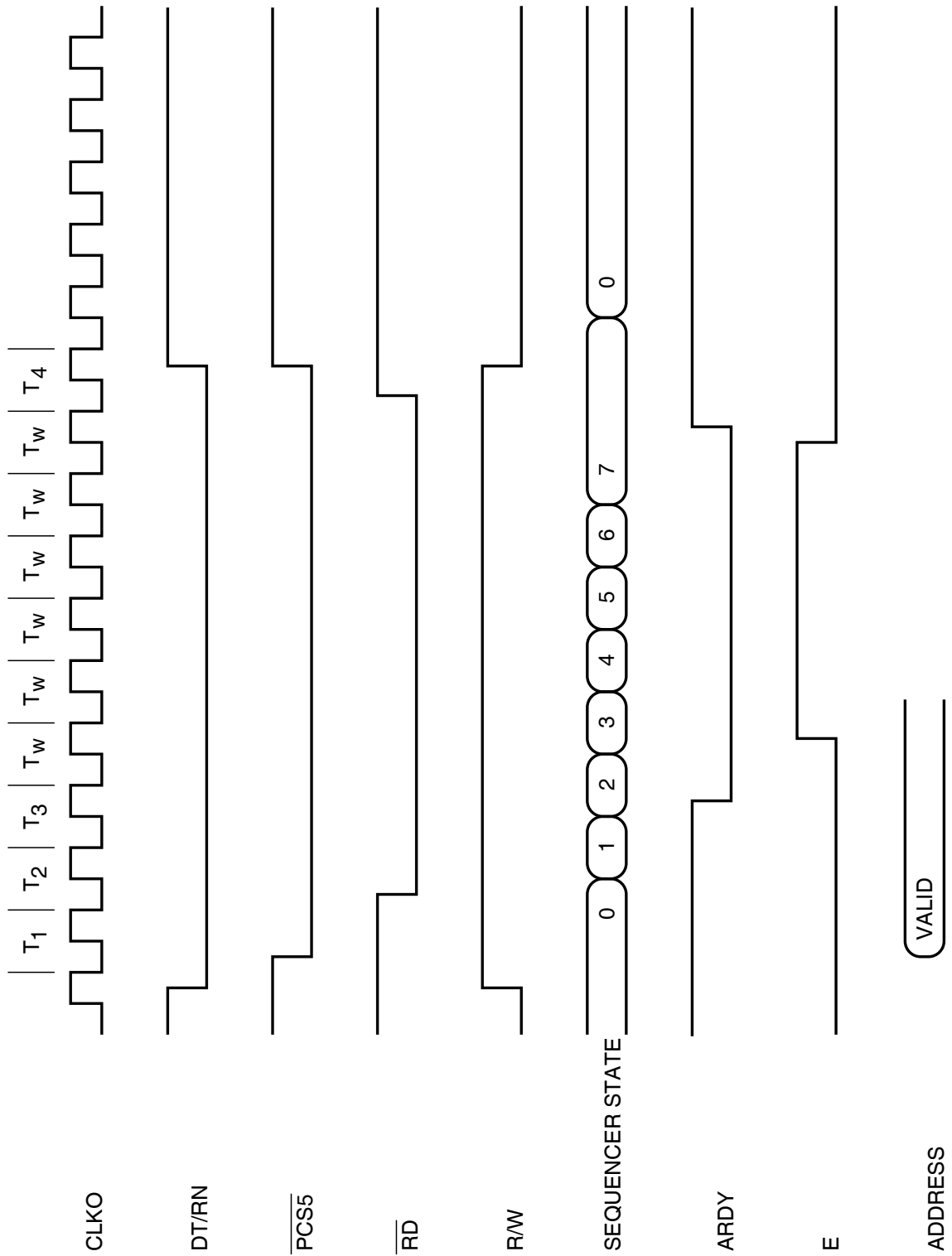


ATCRBS/Mode S Replies  
Figure 5

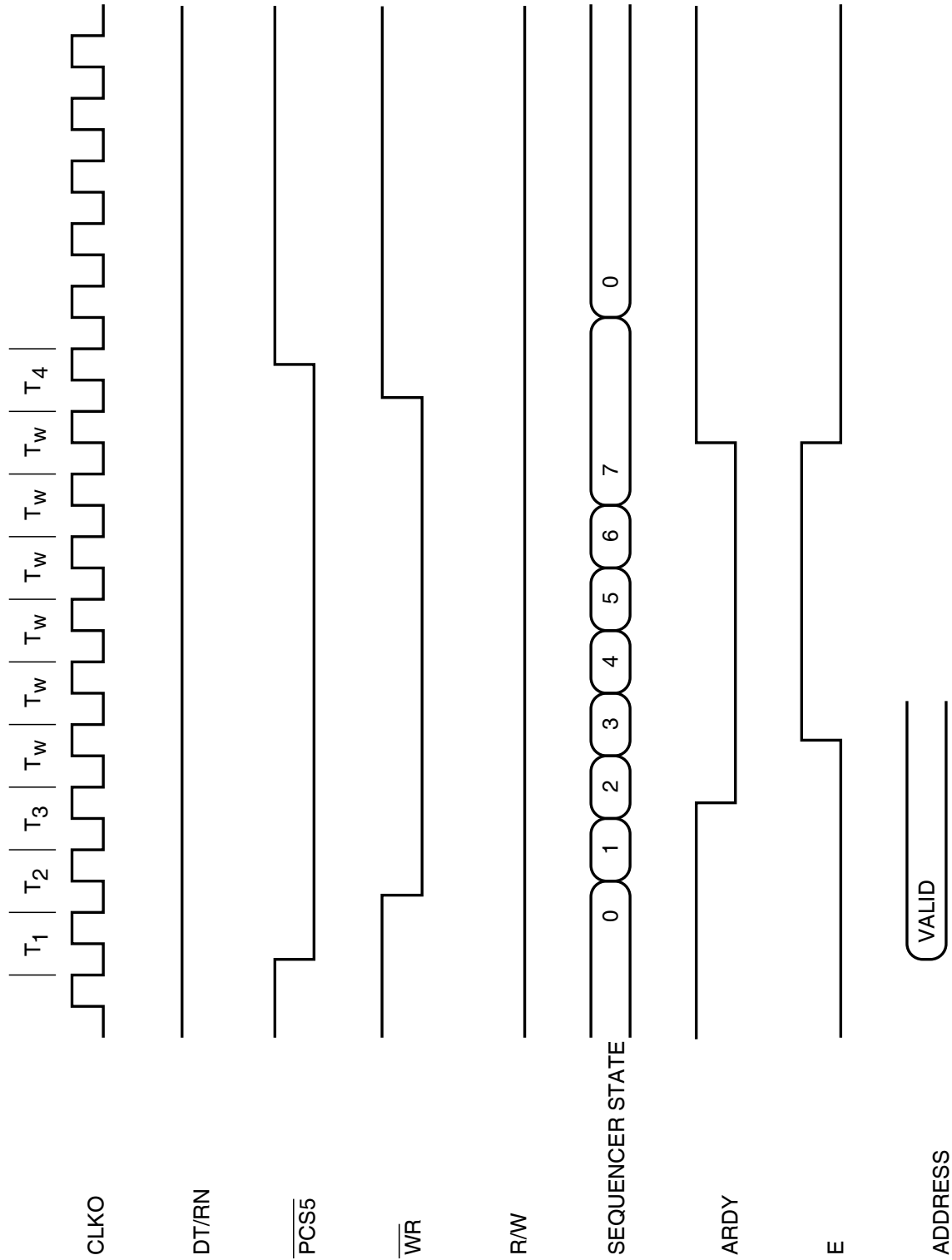


LCA Components Reset  
Figure 6

**NOTE:** LCA COMPONENTS ARE DONE PROGRAMMING AT  $t=150\text{ ms}$ . EITHER COMPONENT HOLDS D/PN LOW. BOTH MUST BE FINISHED PROGRAMMING FOR D/PN TO GO HIGH



LCD Read Cycle  
Figure 7



LCD Write Cycle  
Figure 8

8114004