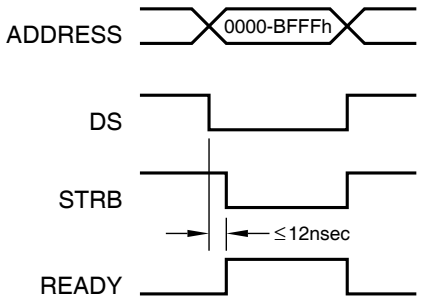
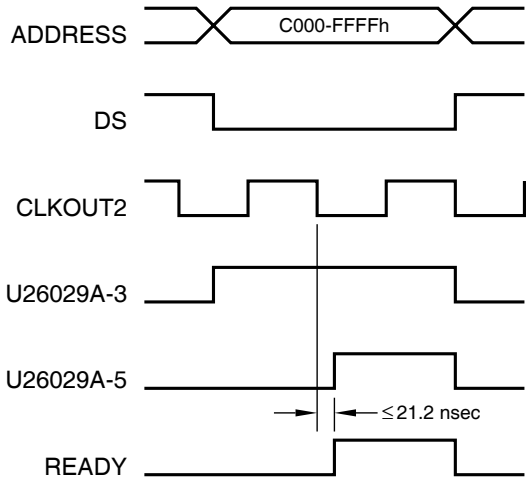
APPENDIX D - TIMING DIAGRAMS

1. Digital IF PCB Assy



0 WAIT STATES



1 WAIT STATE

8514011

System Interface PAL Wait States
Figure 1

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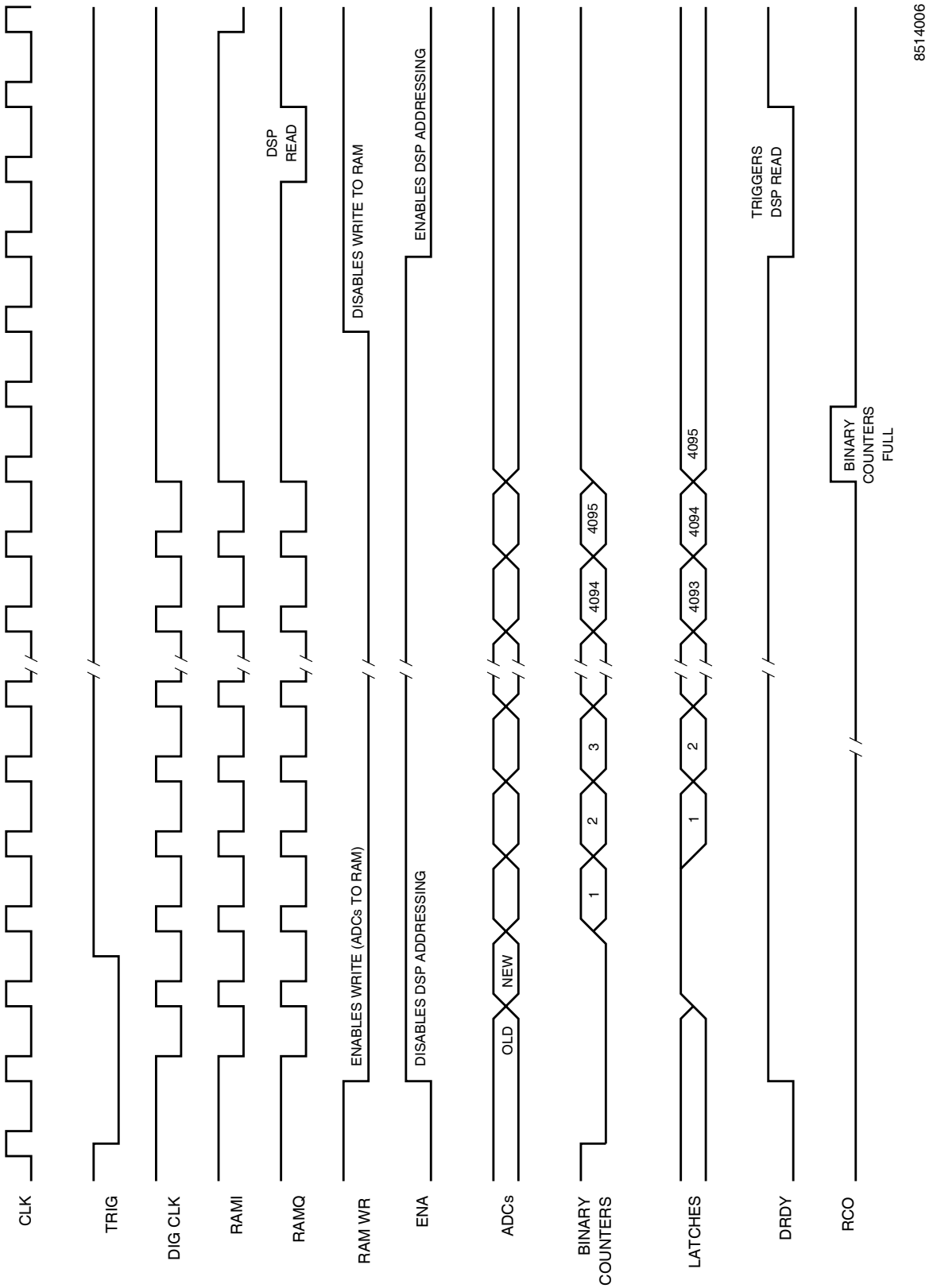

Digitizer
Figure 2

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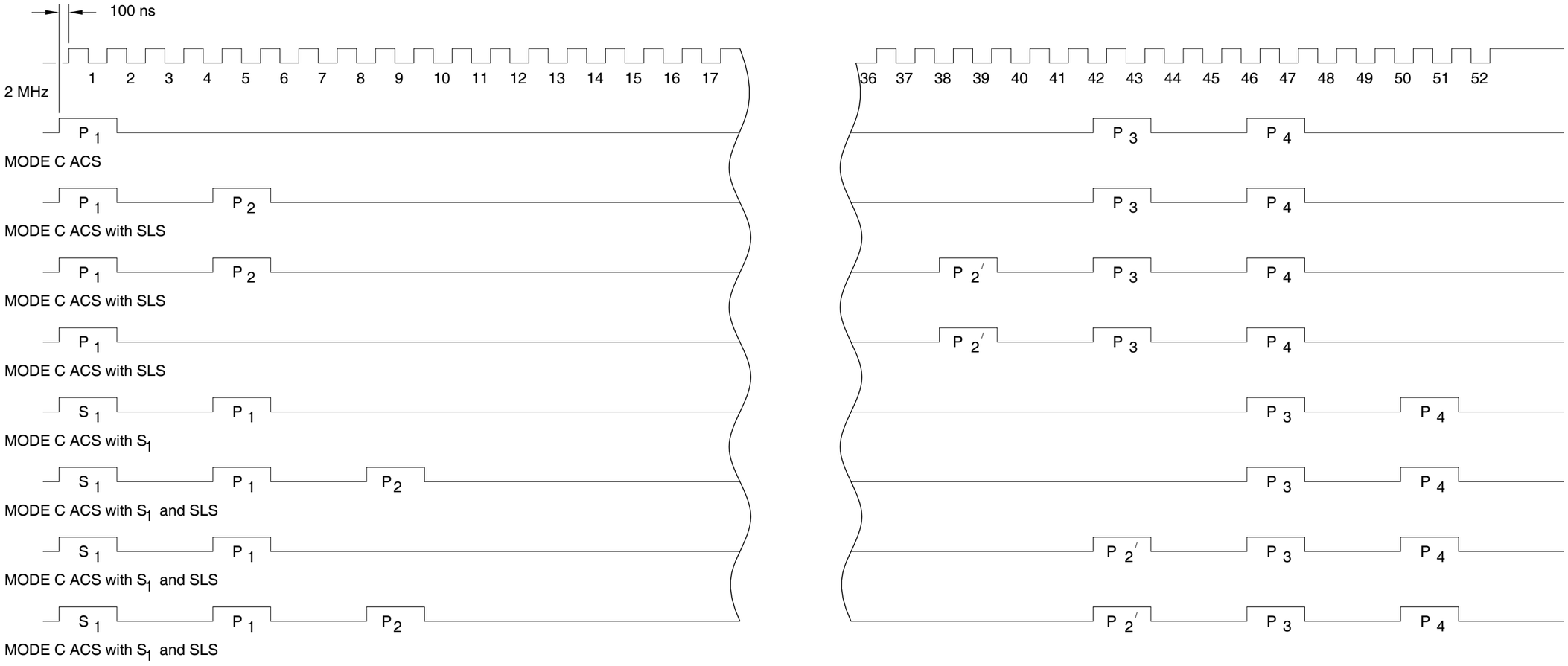
2. Front Panel Pulse PCB Assy



NOTE: P_2' IS AN ADDITIONAL SLS CONDITION.

8514001

Mode C Timing
Figure 3

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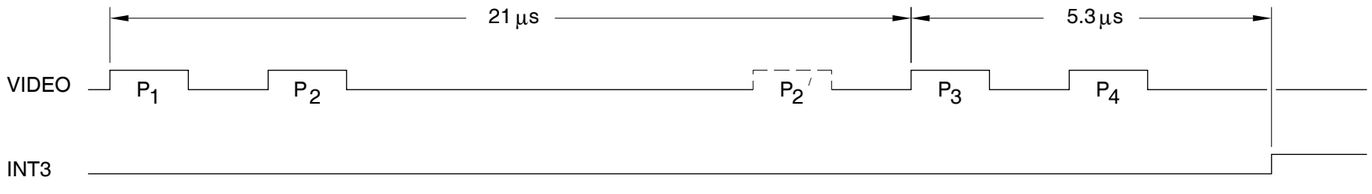
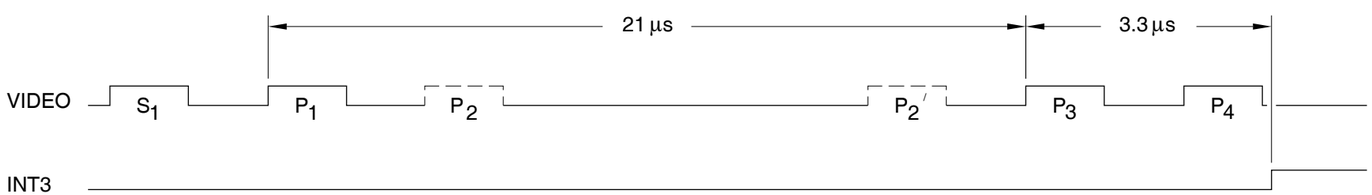
MODE C ALL CALL with NO SUPPRESSION



MODE C ALL CALL with SLS



MODE C ALL CALL with S_1 PULSE (with or without SLS)

8514002

ATCRBS Interrogations Interrupt and Pulse Generator Trigger Timing
Figure 4

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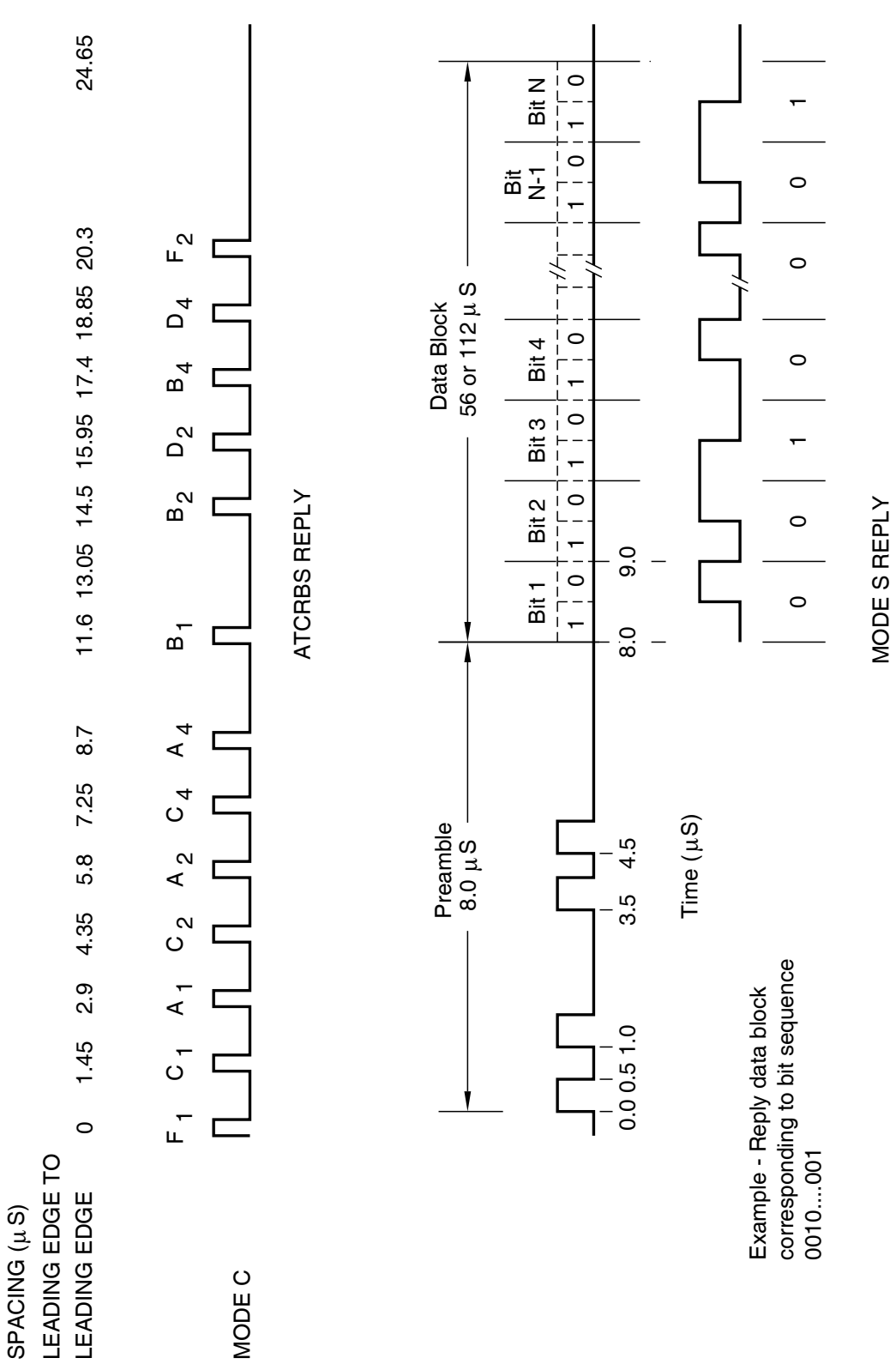

ATCRBS/Mode S Replies
Figure 5

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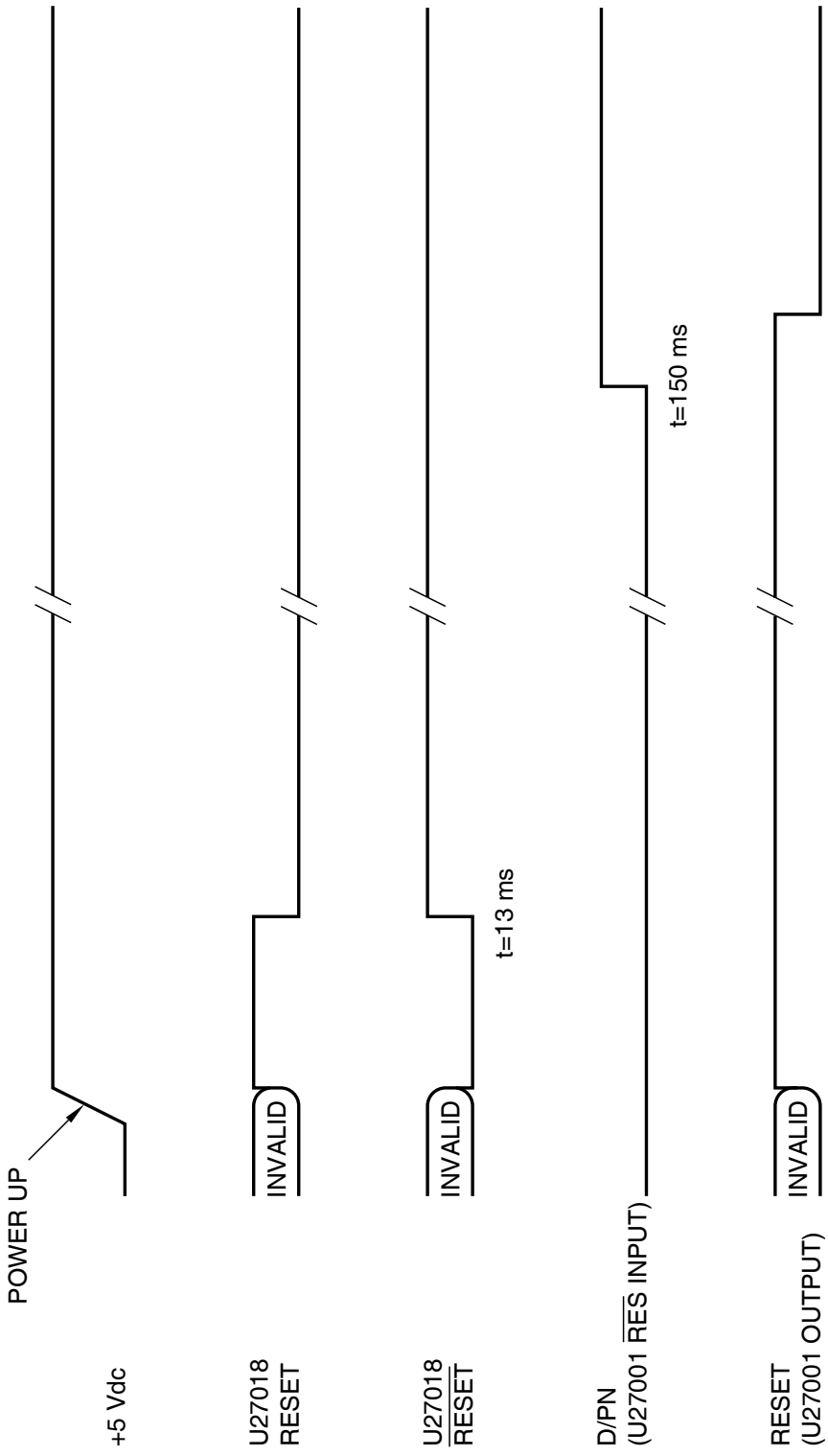

LCA Components Reset
Figure 6

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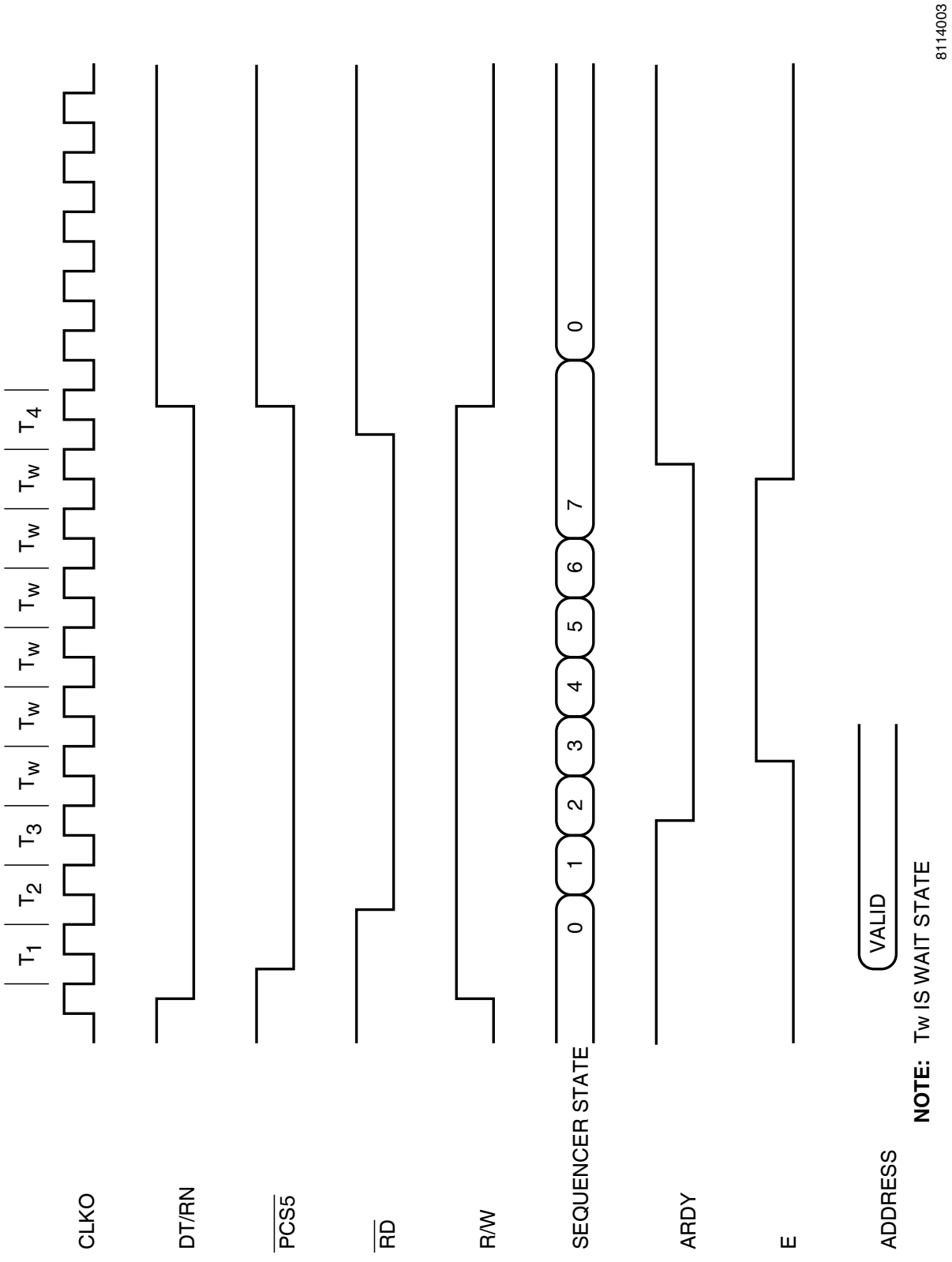

LCD Read Cycle
Figure 7

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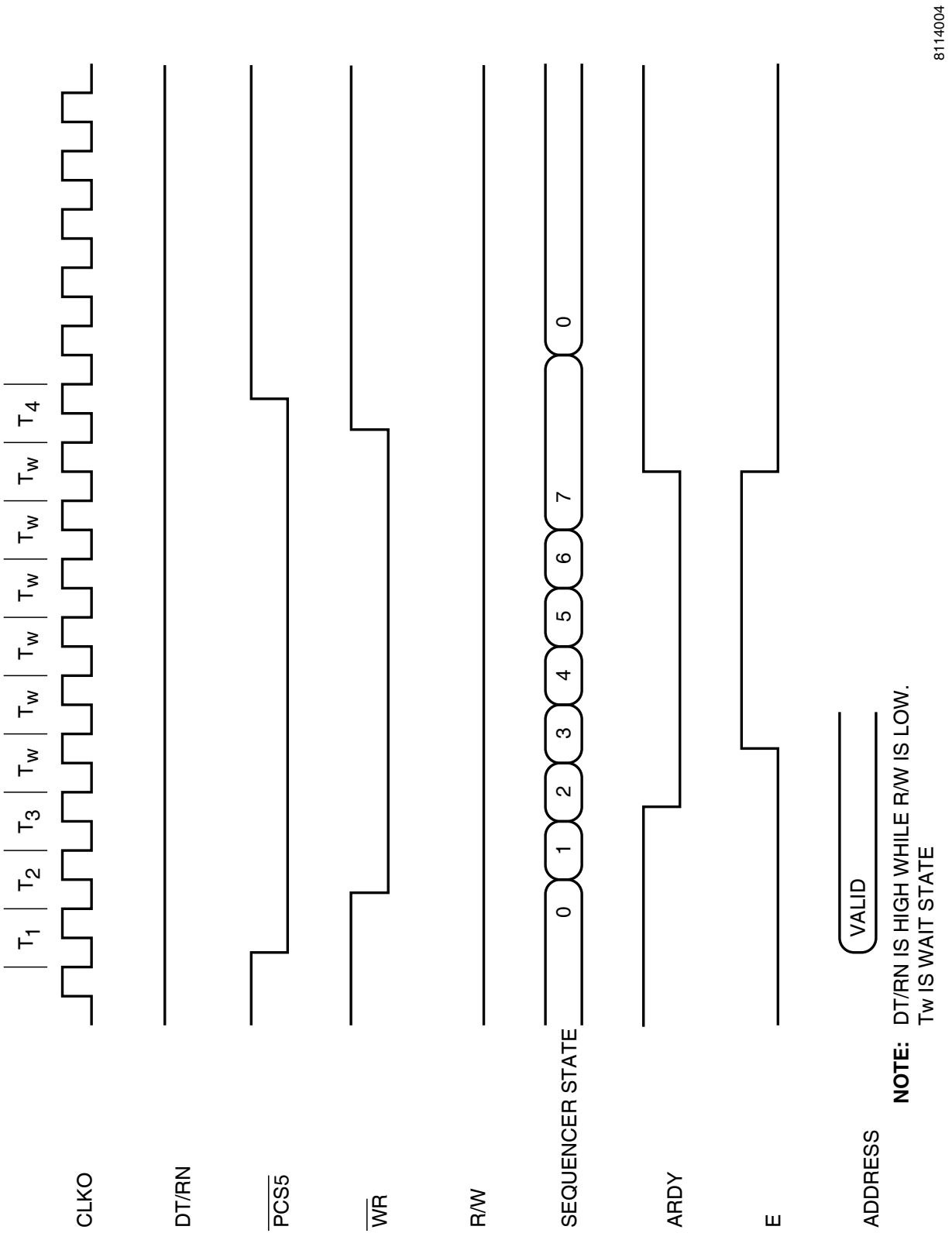

LCD Write Cycle
Figure 8

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