SECTION 2 - TROUBLESHOOTING

1. Theory of Operation

A. General

Theory of Operation is divided into three levels:

- System Theory of Operation

  Contains a simplified description of signal flow through the TCAS-201-2 with accompanying block diagram.

- Functional Theory of Operation

  Contains simplified descriptions of how the various functions of the TCAS-201-2 operate.

- Module Theory of Operation

  Contains a detailed description of each assembly in the TCAS-201-2.

Refer to Appendix G, Figures 1 and 2 for location of external controls, connectors and indicators. Refer to appropriate schematics and assembly drawings in para 2-2-3 for internal controls, connectors, indicators and components.

B. System Theory of Operation (2-2-1, Figure 1)

The TCAS-201-2 Ramp Test Set provides three simulations:

- Active Mode C or Mode S Transponder transmits continually changing replies to interrogations from a specific TCAS interrogator or unit under test (UUT).
- Mode C or Mode S Reply Generator transmits preset replies to interrogations from a specific TCAS interrogator or UUT.
- TCAS Interrogator Monitor decodes information from interrogations received from any interrogator transmitting in the operating mode of the TCAS-201-2.

UUT interrogations are received on an RF carrier signal at ≈1030 MHz, through the RF I/O Connector or ANTENNA Connector. The signal is mixed down to 30 MHz by the Mixer PCB Assy. The Analog IF Assy filters and amplifies the signal for the Digital IF PCB Assy and Detector Assy. The 30 MHz signal is converted to a digital signal and analyzed by the Digital IF PCB Assy. Mode S information data, stored on the Digital IF PCB Assy, is accessed by the Front Panel Pulse PCB Assy. The Detector Assy sends Differential Phase Shift Keying (DPSK) modulation to the Decoder Assy and interrogation Video with a Threshold comparison signal to the Front Panel Pulse PCB Assy. The Decoder Assy decodes and sends DPSK data to the Front Panel Pulse PCB Assy. The Front Panel Pulse PCB Assy verifies the data and/or video. If the interrogation is determined to be valid, the Front Panel Pulse PCB Assy initiates replies as instructed by the operating test function. The Front Panel Pulse PCB Assy also controls interrogation information shown on the DISPLAY.

Replies are controlled and produced from the Front Panel Pulse PCB Assy. When in Scenario Test or Reply Test functions, the Front Panel Pulse PCB Assy replies when correct interrogations are received. The Front Panel Pulse PCB Assy transmits specific pulse information according to operation screen settings, to the Driver PCB Assy. The Driver PCB Assy drives the pulse information to modulate a 30 MHz signal in the Analog IF Assy. After amplification and frequency mixing by the Mixer PCB Assy, a modulated 1090 MHz reply signal is transmitted through the RF I/O Connector or ANTENNA Connector to the UUT.

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C. Functional Theory of Operation

(1) Scenario Test

The TCAS-201-2 simulates a moving Mode C or Mode S transponder when Scenario Test is initiated. Once a second, the Front Panel Pulse PCB Assy calculates a new position for the TCAS-201-2. Using range rate information from the Scenario Test screen, the Front Panel Pulse PCB Assy calculates and implements a new reply delay for simulating the updated position. Using the altitude rate from the Scenario Test screen, the Front Panel Pulse PCB Assy calculates new altitude data for the next Mode C or Mode S reply. Screen edits are incorporated at any time during operation.

(2) Reply Test

The TCAS-201-2 simulates a stationary Mode C or Mode S transponder (reply generator) when Reply Test is initiated. The Front Panel Pulse PCB Assy sets replies according to information loaded into the applicable Reply Test screen. Information is updated only when edits are made to the Reply Test screen.

(3) Monitor

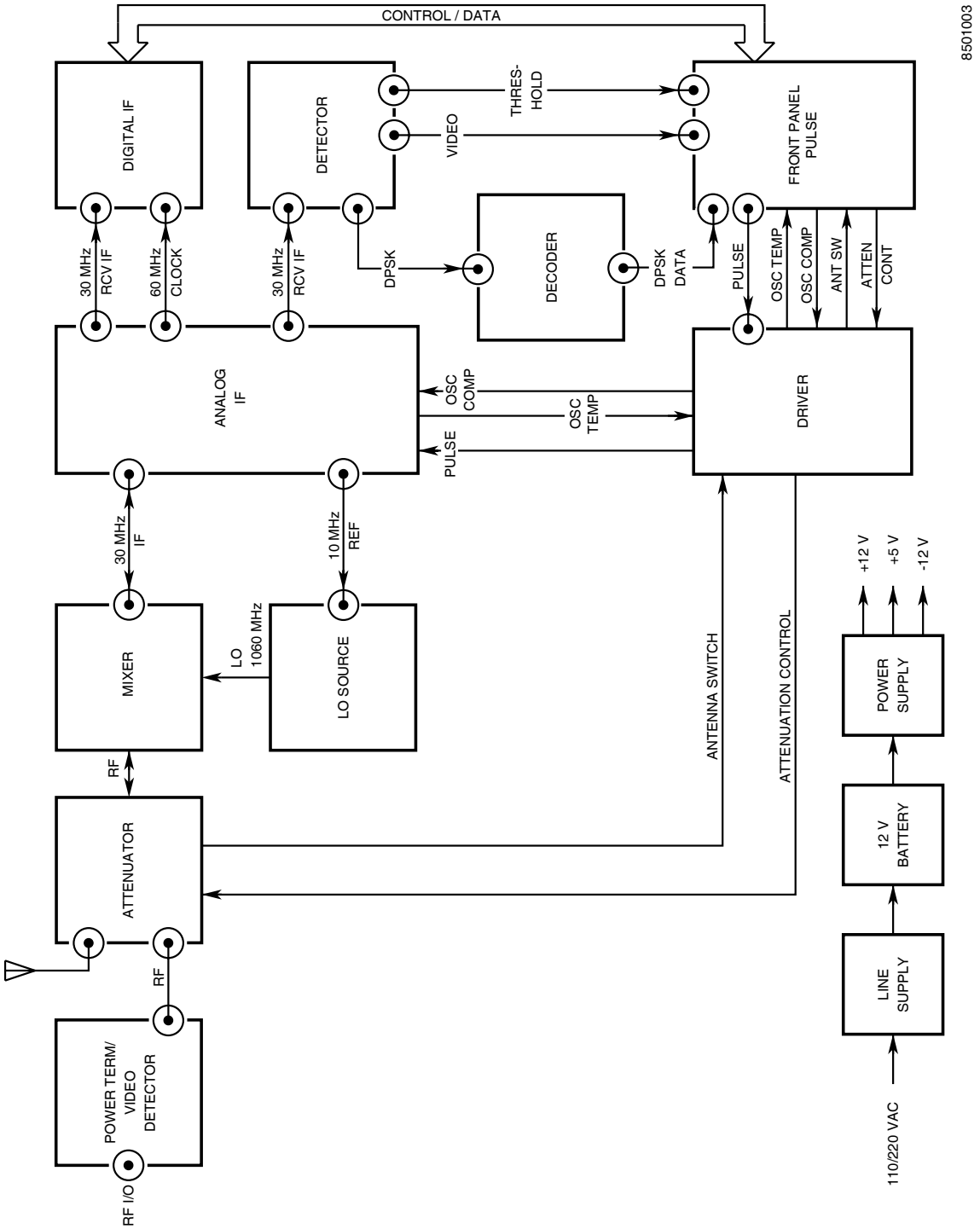
The TCAS-201-2 monitors the Whisper-Shout sequence in ATCRBS operation and UF0 and UF16 interrogations including the TCAS Broadcast in Mode S operation. In ATCRBS operation, the Front Panel Pulse PCB Assylooks for suppression pulses (S_1 and/or P_2). If suppression pulses are received and test was initiated from Scenario or Reply Test screen, the trigger to start the TCAS-201-2 reply is not sent. Suppression pulse information is sent to the DISPLAY. In Mode S operation, the Front Panel Pulse PCB Assy sends interrogation data information, stored on the Digital IF PCB Assy, to the DISPLAY.

(4) Power & Frequency

Power & Frequency is a cyclic program stored in ROM on the Front Panel Pulse PCB Assy. The test transmits Mode S squitters starting with the address loaded in the Mode S Reply Test screen ***AA:*** field and using up to 512 different addresses. Detected interrogations, received as a result of the squitters, are sent to the Digital IF PCB Assy for power and frequency calculations. The Digital IF PCB Assy splits incoming signals into two phases (In and Quadrature) to calculate amplitude of P_6 interrogation pulses and phase shifts between digitized P_6 interrogation pulse samples before SPR.

Two power calculations, current and average, use multiple samples of each P_6 interrogation pulse. Average power is calculated using the amplitude of all interrogations received during entire Power & Frequency test run. A small correction factor is subtracted from average power calculations, to offset multipath effects. Current power is average power over latest one second interrogation sequence. The latest interrogation sequence contains the number of interrogations indicated in the ***INTERRS:*** field. The Front Panel Pulse PCB Assy uses distance information from Setup #1 Menu to calculate path loss. Antenna gain and cable loss from Setup #1 Menu are added with the path loss and power calculations to provide displayed power readings.

Two frequency calculations, current and average, are calculated using multiple samples of In phase and Quadrature phase signals. Frequency is determined by change in phase during a sample period. Average frequency is calculated using an average of all samples received during entire Power & Frequency test run. Current frequency is average frequency over latest one second interrogation sequence.



System Block Diagram
Figure 1

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(5) Self Test (2-2-1, Table 1)

Self Test runs as follows:

- Non-Volatile RAM Battery (only run on power-up)

  The Processor on Front Panel Pulse PCB Assy reads the non-volatile RAM battery bit status from the RAM on the Front Panel Pulse PCB Assy. Status is set only on power-up.

- Battery

  The Processor on the Front Panel Pulse PCB Assy reads the BATTEST line from the Power Supply Assy through the Status Buffer on the Front Panel Pulse PCB Assy.

- LO Control

  The Processor on the Front Panel Pulse PCB Assy enables the Local Oscillator (LO) through the LED Control Register on the Front Panel Pulse PCB Assy. The Processor reads the Status Buffer on the Front Panel Pulse PCB Assy to verify the LO is On. The LO is then disabled through the LED Control Register. The Processor reads the Status Buffer again to verify the LO is Off.

- Dual Port RAM (DPR)

  The Processor on the Front Panel Pulse PCB Assy writes a sequence using AA55h to fill the DPR on the Digital IF PCB Assy. The Processor reads the DPR and compares with the sequence written. The process repeats using 55AAh. The process repeats a third time using a number sequence starting at 0000h and increasing one for each address loaded.

  NOTE: If the DPR test fails, Self Test skips the other RAM tests and goes to the LED test.

- Video RAM

  The Processor on the Front Panel PCB Assy tests the Video RAM on the Front Panel Pulse PCB Assy in the same manner as the DPR on the Digital IF PCB Assy.

- Display RAM

  The Processor on the Front Panel PCB Assy copies the current screen and transfers visibility to the unused secondary page on the Liquid Crystal Display (LCD). The Processor tests the Display RAM on the Front Panel Pulse PCB Assy using the primary page and in the same manner as the DPR on the Digital IF PCB Assy. After the test, the screen and visibility are returned to the primary page.

- Non-Volatile RAM

  Contents of the non-volatile RAM on the Front Panel PCB Assy are transferred to the DPR on the Digital IF PCB Assy. The Processor on the Front Panel PCB Assy tests the non-volatile RAM in the same manner as the DPR. After the test, the original contents are restored to the non-volatile RAM.

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TEST	GROUP	VERIFIES	FAILURE CODE (h)	RUNNING ORDER
Non-Volatile RAM Battery	Power Supply/ Battery	Battery has sufficient power for RAM to retain memory.	00000020	Only on power-up
Battery	Power Supply/ Battery	Voltage is within correct voltage range.	00000010	1
LO Control	RF	Valid ON/OFF status	00000001	2
RAM	Digital	Dual Port RAM (DPR)	01000000	3
		Video RAM	02000000	4
		Display RAM	08000000	5
		Non-Volatile RAM	04000000	6
LED	Digital	Interrogation and reply drivers	80000000	7
UART	Digital	RS-232 loop back	00400000	8
Attenuator #1	Digital	Level at end line diodes	10000000	9
Attenuator #2	Digital	Level at midline diodes	20000000	10
LO Compensation	Digital	DCXO control voltage	40000000	11
LO Detect	RF	LO is locked.	00000002	12
RF Detect	RF	TX level out/Attenuation	00000004	13
DSP Initialization	Digital	Handshake routine	00000040	14
NOTE: Multiple failures are indicated by the sum of the error codes.				
NOTE: If DPR Test fails, subsequent RAM tests are not run.				

Self Test
Table 1

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- LED

  The Processor on the Front Panel PCB Assy turns On the Interrogation and Reply LEDs on the Front Panel LED PCB Assy through the LED Control Register on the Front Panel PCB Assy. The Processor verifies On status through the Status Control Register on the Front Panel PCB Assy. After ≈80 ms, Off status is verified through the Status Control Register.

- UART

  The Processor on the Front Panel PCB Assy configures the UART (RS-232 Interface on the Front Panel Pulse PCB Assy) to loop back. The Processor sends a message and verifies the reception.

- Attenuator #1/Attenuator #2

  The Processor on the Front Panel PCB Assy writes values to the attenuation Digital-to-Analog Converters (DACs) on the Front Panel PCB Assy. The Processor reads the corresponding status from the Analog-to-Digital Converter (ADC) on the Front Panel PCB Assy to verify the DACs are correctly converting attenuation voltage data.

- LO Compensation

  The Processor on Front Panel PCB Assy writes values to a DAC on the Front Panel PCB Assy. The Processor reads the corresponding status from the ADC on the Front Panel PCB Assy to verify the DAC is correctly converting LO compensation voltage data.

- LO Detect

  The Processor on the Front Panel PCB Assy turns On the Local Oscillator on the LO Source PCB Assy through an LED Control Register on the Front Panel PCB Assy. The Processor verifies the LO Detect voltage is 0.35 to 3.1 Vdc by reading 71 to 635 from the ADC on the Front Panel PCB Assy. The test fails if the LO is not locked (≈7.5 Hz trapezoidal waveform present at TP27033 on the Front Panel Pulse PCB Assy).

- RF Detect

  The Pulse Generator on the Front Panel PCB Assy sends a CW signal with no attenuation. After going through the transmit portion of the RF Assy, the signal returns on the RF DETECT line to the ADC on the Front Panel PCB Assy. The Processor on the Front Panel PCB Assy verifies the level after digital conversion. The test is repeated with 3 dB attenuation set by the Attenuator Control on the Front Panel PCB Assy through the Driver PCB Assy to the Attenuator PCB Assy. The Processor checks for the 3 dB difference by verifying the ratio of unattenuated level to attenuated level is 2 (±0.4).

- DSP Initialization

  The Processor on the Front Panel Pulse PCB Assy resets the Digital IF PCB Assy through the LED Control Register on the Front Panel PCB Assy. After reset, the Digital Signal Processor (DSP) on the Digital IF PCB Assy controls the RDY output to the Status Buffer on the Front Panel PCB Assy. The Processor verifies the DSP is ready status through Status Buffer.

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D. Module Theory of Operation

(1) Power Supply

(a) Line Supply Assy

The Line Supply Assy is an ac to dc converter containing a power transformer, bridge rectifier and filter.

The AC PWR Connector (J10050) on the Front Panel Assy is connected to the Line Supply Assy through P33049A. Transformer T33001 has two primary windings connected in parallel when 115 VAC is selected by double pole, double throw Switch S15001. The two primary windings are connected in series if 230 VAC is selected. The secondary winding of T33001 is connected to Full Wave Rectifier BR33001, mounted on the side panel heat sink. Unregulated voltage from BR33001 is applied to the crowbar circuit (over-voltage protection), filtered by C33003 and sent through P33049B to the Power Supply Assy.

The crowbar circuit includes CR15001, CR15002, R15001, R15002 and Q15001. If voltage becomes excessive, Q15001 turns on, effectively shorting the bridge output and disabling Fuse F12001. F12001 opens when the line reaches approximately 160 VAC (115 VAC operation) or 320 VAC (230 VAC operation).

(b) Power Supply Assy (2-2-1, Figure 2)

1 Battery Charger

The Battery Charger operates on 15 to 22 V source from the Line Supply Assy through P23047. The CHARGE Indicator illuminates red when charging and green when battery is more than 80% charged.

The Battery Charger requires Test Set power Off and a partially charged battery to initialize. With no battery, the Battery Charger is inoperable. If TCAS-201-2 power is On (DISPLAY illuminates and shows screen), the Battery Charger is disabled.

When ac power is first applied with Test Set power Off, the Battery Charger provides constant current to the battery. When the battery achieves a 75% charge, voltage across the battery rises rapidly and the Battery Charger switches to voltage regulation mode (at ≈14.2 V).

The 15 V source voltage is applied to the Power Supply Assy at P23047-8 and P23047-15. Input to the switching section goes through a low-pass filter (C14032, L14006, C14023 and C14038) to Converter/Transformer T14001. Output of T14001 is rectified by CR14003 and filtered by C14001, providing the battery voltage at J11048-1. CR14015 and CR14014 provide back-up voltage separation between the battery, Battery Charger and Output Supply. The battery is grounded through Current Sense Resistor R14001. Regulator U14001 operates on three inputs. The peak current on FET Q23002 is fed back to the Current Sense input (U14001-7). The battery charge voltage is fed back and sensed across a voltage divider (R14003, R14080 and R14007). R14007 (ADJ BATT CHARGER VOLTAGE) adjusts the operating float voltage (14.2 Vdc with charged battery). The charging current sensed at R14001 sets up the reference voltage formed across diodes CR14001 and CR14002. Thermistor RT14001 controls bias current on CR14001 and CR14002. The reference input to U14001-1 is a function of temperature and establishes trickle charge control between 0° C and 70° C. R14073 (GAIN ADJ) controls excess voltage. The pulse output (U14001-13) controls Gate Drivers Q14001 and Q14002. Q14001 and Q14002 drive the Transformer T14001 through Q23002.

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The ac voltage at T14001 (E14004) is rectified by CR14011 and C14026. Rectified voltage feeds constant current source Q14015. Q14015 provides ≈20 mA to the CHARGE Indicator through P12001-3. When the line from Q14015 is sourcing current, the CHARGE Indicator illuminates red. When Q14013 and Q14014 are turned on, Q14015 shuts off and sink current through CR14010 causes the CHARGE Indicator to illuminate green. Three conditions must be met to obtain a green indication on the CHARGE Indicator:

- Charging current (<≈400 mA) is sensed by U14006C.
- Regulator U14001 is in voltage regulation mode when the compensation output (TP14001) is <≈4 V. The compensation output is sensed by U14006D.
- Regulator U14001 produces enough power to trickle charge the battery when the compensation output (TP14003) is >≈2 V. This indicates a battery is connected and the battery has no open cells. The compensation output is sensed by U14006B.

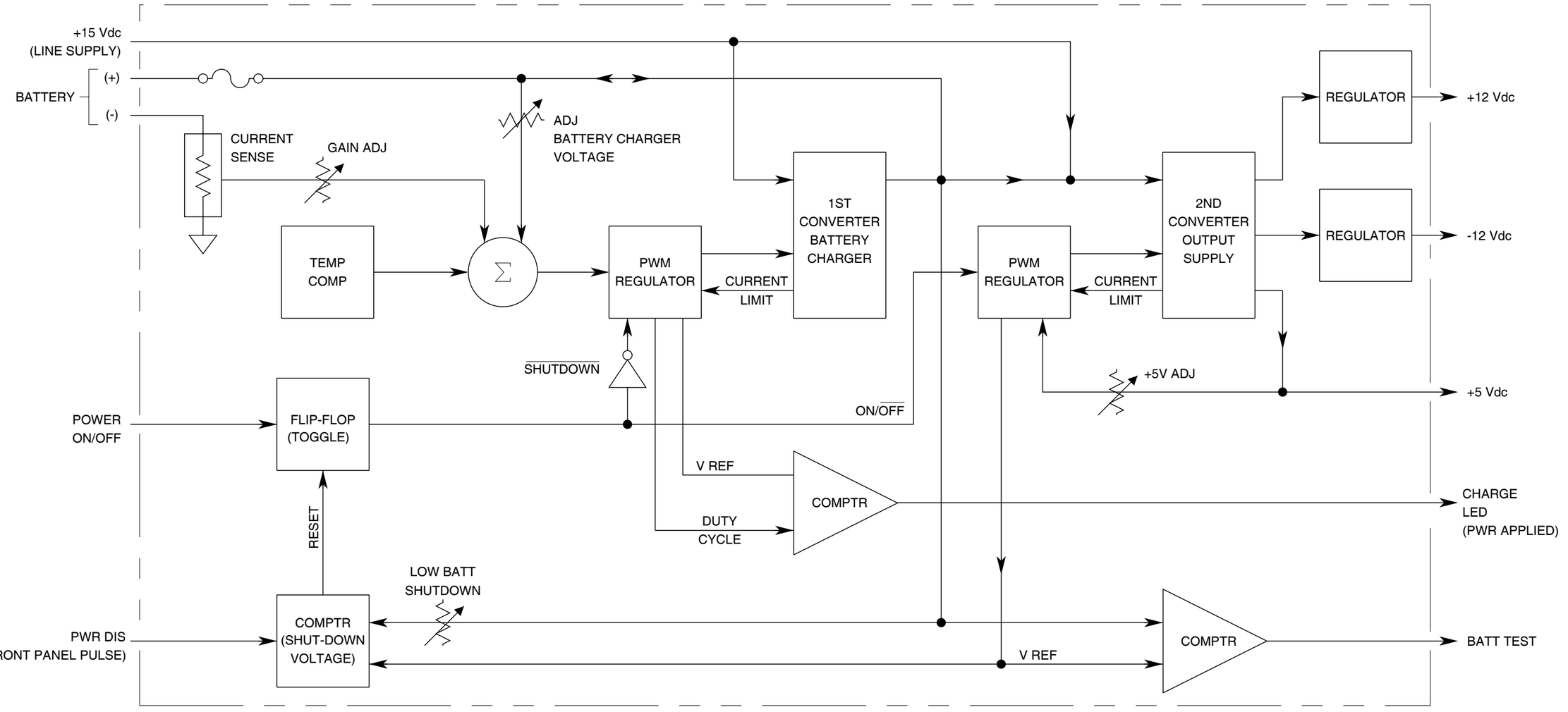
2 Output Supply

The Output Supply is dependent upon the battery line for the input power. Input voltage to the Output Supply varies with the charge level of the battery. The Output Supply provides operating voltages for the Test Set and is controlled by the POWER Key. The Battery Charger is switched Off when the Output Supply is operating.

The POWER Key is connected to P12001-1. A switch closure to ground at R14017 turns Q14017 On momentarily, clocking J-K Flip-Flop U14002B connected as a one-shot. At switch closure, U14002B-2 produces a single 100 ms pulse, set by R14019 and discharge time of C24010. The trailing edge of the pulse (going positive) clocks J-K Flip-Flop U14002A. When toggled On, U14002A-15 goes high turning On the Output Supply and U14002A-14 goes low activating SHUTDOWN line to turn Off the Battery Charger. The high at U14002A-15 activates Q14004, Q14005 and Q14006. Q14006 drives the Regulator U14003. Q14005 drives the low voltage sensing circuit.

U14003 regulates using three inputs. Current limit control through FET Q23001 is sensed at U14003-6. The +5 V feedback voltage is set by R14074 and sensed at U14003-1. Feedback current through R14025 sets the negative error sensing input at U14003-2. The pulse output (U14003-13) controls Gate Drivers Q14007 and Q14008. Q14007 and Q14008 drive Transformer T14002 through Q23001. Two outputs from T14002 are rectified, filtered and regulated to provide +12 and -12 Vdc. The other output is rectified and filtered to provide +5 Vdc, regulated by U14003.

The battery voltage is sensed through Q14005 across Voltage Divider R14062, R14060 and R14061. When the battery voltage drops below a threshold determined by temperature (≈+11.3 V at 25° C), U14008C drives a low level through R14068 to the Front Panel Pulse PCB Assy. ***** LOW BATTERY ***** appears in the right half of the fifth line on the DISPLAY and the Battery Test portion of the Self Test fails. As the battery voltage drops further (to ≈+10.4 V at 25° C), Comparator U14008B senses the low voltage and a high level output activates Q14012. U14002A resets and shuts off the Output Supply. If the Keypad is inactive for ≈15 minutes during operation, Power Disable (PWRDIS) line from the Front Panel Pulse PCB Assy goes high to Comparator U14008A-6. The high level output causes U14002A to reset and shut off the Output Supply.



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Power Supply Assy Block Diagram
Figure 2

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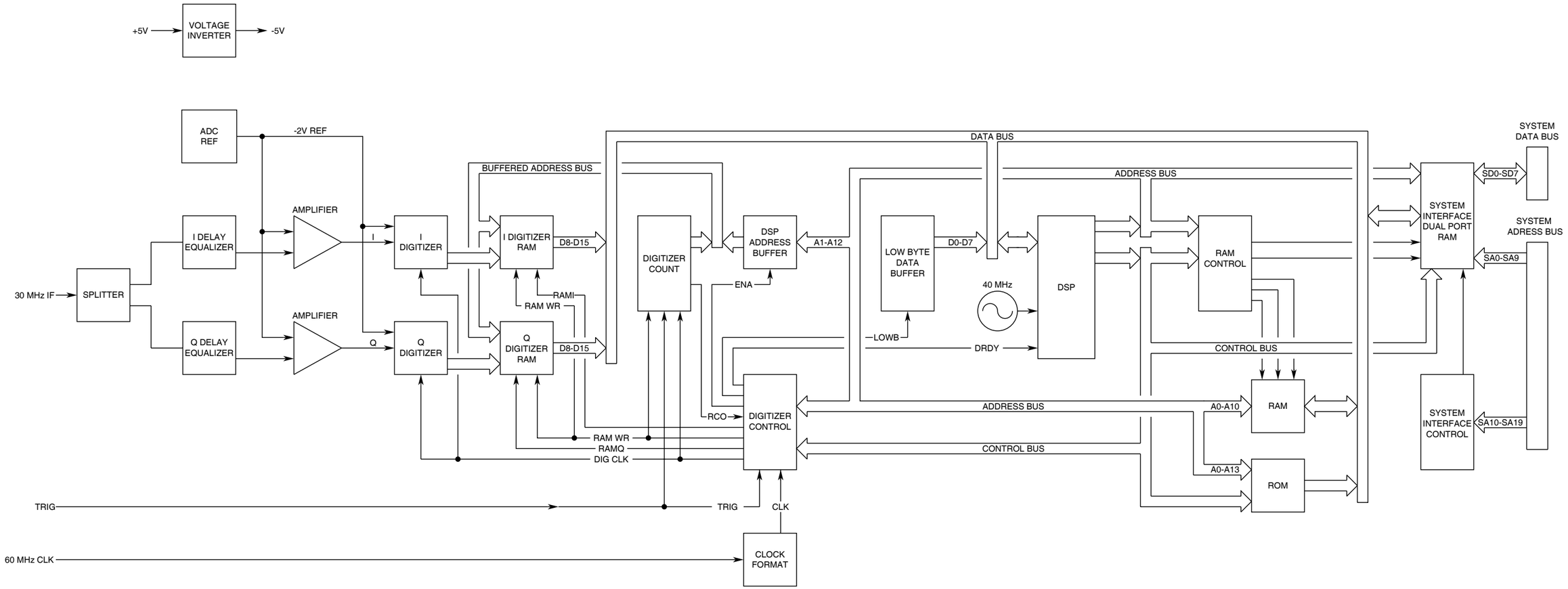

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Digital IF PCB Assy Block Diagram
Figure 3

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(2) Digital IF PCB Assy (2-2-1, Figure 3)

The Digital IF PCB Assy changes the incoming interrogation signals from analog to digital and accurately calculates power and frequency. The Receive IF splits the signal in two and provides a complex representation of the original interrogation signal. The analog signals are converted to digital by the Digitizer and stored into memory. The DSP conducts calculations with the digital information and provides the results to the Front Panel Pulse PCB Assy through the System Interface. The Voltage Inverter provides the necessary voltage to operate the Digital IF PCB Assy.

(a) Receive IF

The 30 MHz signal from the Analog IF Assy, verified at TP26017, goes through a 6 dB resistive splitter (R26032, R26033 and R26034) providing two signals while maintaining 12.8 MHz of bandwidth. Delay equalizers cause a 90° phase difference between the two signals to provide a sine and cosine representation of the received IF signal. Delay equalizers are first order constant-resistance time-domain circuits. One delay equalizer (L26001-L26004, C26057-C27060 and R26011) provides the in-phase (I) signal. The other delay equalizer (L26005-L26008, C26061-C27066 and R26012) provides the quadrature phase (Q) signal. C26061 and C26063 (φ ADJ) maintain the 90° phase difference between the two signals. R26011 (I LEVEL ADJ) and R26012 (Q LEVEL ADJ) keep amplitude of both signals equal.

Transformers T26001 and T26002 convert I and Q signals from bipolar to polar. High-speed integrating operational amplifiers (U26031 and U26032) provide approximately seven times amplification for an output of 2 Vp-p at 30 MHz. The midpoints or zero references (≈-1 V) used in the integration process are tapped from Resistor Networks R26018-R26017 and R26023-R26024 across the ADC reference voltage (≈-2 V). R26017 and R26023 (ADC ZERO) also compensate for temperature drift. Diodes CR26006 and CR26007 protect the ADCs by effectively shorting positive voltages (0.4 V) to ground. The I signal is verified at TP26019 and the Q signal is verified at TP26020.

(b) Digitizer

1 ADC Reference

The ADC reference provides the -2 V reference voltage for the flash ADCs. CR26002 drops 2.5 V. Low Offset Amplifier U26027 and current gain transistor Q26002 convert the 2.5 V to -2 V. The non-adjustable ADC reference voltage (1.96 to 2.08 V) is present at TP26023. The -2 V reference is used by flash ADCs (U26001 and U26002) and Receive IF operational amplifiers (U26031 and U26032). Each flash ADC draws 23 mA nominal, 40 mA maximum, and the operational amplifier circuits use 0.7 mA. The ADC reference circuit supplies a maximum of 300 mA.

2 Flash ADCs

Flash ADCs U26001 and U26002 convert the input analog signals from the Receive IF to digital 8-bit signed values (two's complement). Input signals are set from -2 to 0 V. Voltages >0 V overflow the ADCs. Digital output values range from 80h (-128 decimal), corresponding to -2 V, to 7Fh (+127 decimal), corresponding to 0 V. The 30 MHz digital clock from U26015 controls ADC operation.

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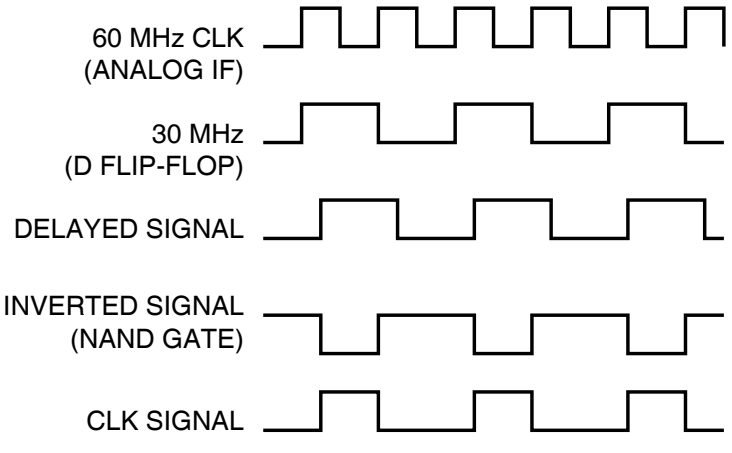
3 RAM

Digitized data is written into four high-speed RAM chips (U26010 through U26013) at a 30 MHz rate. Each RAM chip has a 4k by 4 byte capacity. The RAM chips have separate inputs and outputs. Flash ADCs only write into the RAM chips and the DSP (U26003) only reads from the RAM chips. Address lines are shared by the digitizer control circuit and DSP.

4 Clock Format

The clock format circuit converts the 60 MHz sine wave from the Analog IF Assy into a 30 MHz TTL clock with a 33% duty cycle. Refer to 2-2-1, Figure 4 for the clock format timing diagram. Transistor Q26001, inverting Schmitt triggers (U26023A and U26023B) and associated circuitry convert the 60 MHz input to TTL. D Flip-Flop U26024A divides the signal by two and the 30 MHz output provides both inputs to NAND Gate U26025A. Because DL26001 delays one input by 5 ns, U26025A has a 67% duty clock output. After being inverted by NAND Gate U26025B, the 30 MHz TTL clock has a high time of 10.67 to 12.67 ns. The clock format output is verified at TP26022.



Clock Format Timing Diagram
Figure 4

5 Digitizer Control

The digitizer control circuit consists of a Programmable Array Logic (PAL) circuit (U26015), three binary counters (U26017, U26018 and U26019), two flip-flops (U26020 and U26028) and two address register buffers (U26021 and U26022). U26015 directs digitizing of data into RAM and reading of data out of RAM. Refer to 2-2-1, Table 2 for description of U26015 inputs and outputs. Refer to Appendix C for PAL equations and Appendix D for timing diagrams.

FLOW	U26015 PINS	NAME	DESCRIPTION
Input	1 and 2	CLK	30 MHz TTL clock with 33% duty cycle from clock format circuit
Input	3	DS	Data Select signal from DSP is high unless made low for communicating with external data memory (DPR).
Input	4	STRB	Strobe signal from DSP is high unless made low (active) to indicate external bus cycle.
Input	5, 6 and 7	A0, A14 and A15	Address lines from DSP
Input	8	TRIG	Inverted trigger from Front Panel Pulse PCB Assy indicates start of process.
Input	9	RCO	Ripple Count Out from binary counters indicates end of digitizing the data.
Output	12	DIG CLK	Digitizer Clock
Output	13	LOWB	Low Byte selects Line Driver U26026 to keep data lines (D0-D7) low during RAM read.
Output	15	ENA	Enable Address activates two address register buffers (U26021 and U26022) connecting DSP to digitizing RAM.
Output	16	DRDY	Low Data Ready signal indicates digitizing RAM is ready for DSP to read.
Output	17	RAM WR	RAM Write controls RAM access (low for ADCs writing to RAM and high for DSP reading from RAM).
Output	18	RAMQ	Enables Q digitizer RAM.
Output	19	RAMI	Enables I digitizer RAM.

Digitizer PAL Inputs and Outputs
Table 2

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Digitizing sequence:

- U26023C inverts high TRIG output from Front Panel Pulse PCB Assy to low, resetting Binary Counters U26017, U26018 and U26019.
- On the rising edge of the first clock pulse after TRIG goes low:

  RAM WR goes low to enable the ADCs to write to RAM.

  ENA goes high to disable DSP addressing.

  DRDY goes high indicating data is not ready for DSP to read.
- RAM WR going low enables Flip-Flops U26020 and U26028 to address RAM by latching address lines to the output of Binary Counters U26017, U26018 and U26019.
- DIG CLK, RAMI and RAMQ synchronize with CLK on the falling edge of the first clock pulse after RAM WR goes low.
- TRIG returns to high and the binary counters start counting on the first rising edge of DIG CLK. Binary Counters U26017, U26018 and U26019 are cascaded together to provide a count from 0 to 4095 (the capacity of the digitizer RAM chips).
- With each DIG CLK count, the ADCs convert incoming analog data into another byte.
- With each DIG CLK count, the byte of converted data from the prior clock cycle is stored in the next address in RAM, as stepped by the binary counters (U26017, U26018 and U26019) and latched by the flip-flops (U26020 and U26028).
- Process continues until the binary counters are full and RCO output U26019-15 goes high.
- DIG CLK, RAMI and RAMQ stop synchronous operation with CLK and stay high.
- After U26015 internal switching allows ADCs to write last byte of data into RAM, RAM WR goes high setting RAM for DSP to read.
- ENA goes low to enable DSP to address digitizing RAM.
- DRDY goes low to trigger DSP for reading digitizer RAM. DRDY stays low until a read is done at any digitizer RAM address.
- DSP reads RAMQ (quadrature phase data) using an odd address. A15 and A0 are high while A14, DS and STRB are low.
- DSP reads RAMI (quadrature phase data) using an even address. A15 is high while A0, A14, DS and STRB are low.

(c) Digital Signal Processor (DSP)

U26003 is a TMS320C25 DSP. Two external EPROM chips, U26004 and U26005, provide 8k by 16 bits of ROM containing the program code for U26003. U26003 selects the EPROM chips at addresses from 0 to 3FFFh while the PS (U26003-47) and STRB (U26003-49) lines are both low through OR Gate U26034A. Two external 2k by 8 RAM chips (U26008 and U26009) and internal DSP RAM provide ≈2.6k by 16 bits of RAM. Interface to external RAM is accomplished with the 16V8A PAL U26016. Addresses from 400 to BFFh with STRB low cause SRCS (U26016-19) to go low, selecting the RAM chips. SROE (read) or SRWE (write) goes low depending on R/$\overline{W}$ line (U26003-48). Data lines D0-D7 access U26008 and data lines D8-D15 access U26009. External RAM is contiguous to the internal RAM located through 3FFh. RAM is accessed with no wait states.

The DSP operates using a 40 MHz clock provided by U26035. Inverting Schmitt Trigger U26036A converts clock output to TTL.

In operation, the DSP performs calculations, controlled by ROM, on the data in digitizer RAM. Results are stored in RAM available to the DSP. After reading the digitizer RAM chips, the DSP performs mathematical operations to determine the power of P_6 pulse and the UUT frequency.

(d) System Interface

The System Interface consists of PAL U26016 and Dual Port RAM (DPR) U26007. The RDY line (P26006-A7), when high, indicates the Digital IF PCB Assy is ready to communicate. The RDY line resets at power-up or when system is reset by the Front Panel Pulse PCB Assy. IS, STRB and R/$\overline{W}$ goes low to U26016 causing RDYCS to go low. RDYCS clocks D Flip-Flop U26024B and a high on data line D0 sets the RDY line high. The DSP accesses the DPR at addresses C000 to C3FFh through the PAL. When DS is low with A14 and A15 high (valid DPR address), a high (U26016-15) is sent to J-K Flip-Flop U26029A to add a wait state. On the falling edge of CLK2, U26029A output goes high to U26016-5, setting READY high. When a valid address other than a DPR address is accessed, READY line is set high without a wait state. Refer to wait state timing diagrams in Appendix D. When the DPR is accessed by the Front Panel Pulse PCB Assy, the BUSY line from the DPR (U26007-3) goes low causing the READY line to remain low.

(e) Voltage Inverter

The Voltage Inverter converts the +5 V input to a -5 V output. The Voltage Inverter is a pulse width modulated circuit consisting of a relaxation oscillator, Transistor Q26004, Switcher Pass Device Q26005, Clamp Diode CR26005 and associated filtering components.

The relaxation oscillator consists of Comparator U26037, Voltage Divider R26036 and R26037, Resistor R26039 and Capacitor C26079. R26039 and C26079 provide the time constant, setting the oscillation frequency. The voltage divider sets the voltage limitations of the oscillator (centered around +5 V). Comparator U26037 sends a pulse output to control Q26005. The pulse (≈10 V) is based on the input from Transistor Q26004 and the voltage divider.

Transistor Q26004 works as differential amplifier and provides feedback current to modulate duty cycle offset by R26038. R26040 and R26041 provide feedback voltage (≈-0.7 V) on emitter of Q26004. R26041 (-5V ADJ) sets level of feedback necessary to maintain the -5 V output. Diodes CR26003 and CR26004 compensate for voltage drop across the base to emitter of Q26004. C26080 provides lead compensation to dampen feedback loop ringing caused by the delay from input to output.

The pulse output from Comparator U26037 causes current to flow through Q26005 ≈50% of the time. The other part of the time current flows through CR26005. The voltage drop across CR26005 goes from +0.5 to -10 V during the duty cycle averaging out to -5 V. C26081 provides a dc block between the modulating circuit and the output. L26009 and L26010 provide filtering and modulation allowance.

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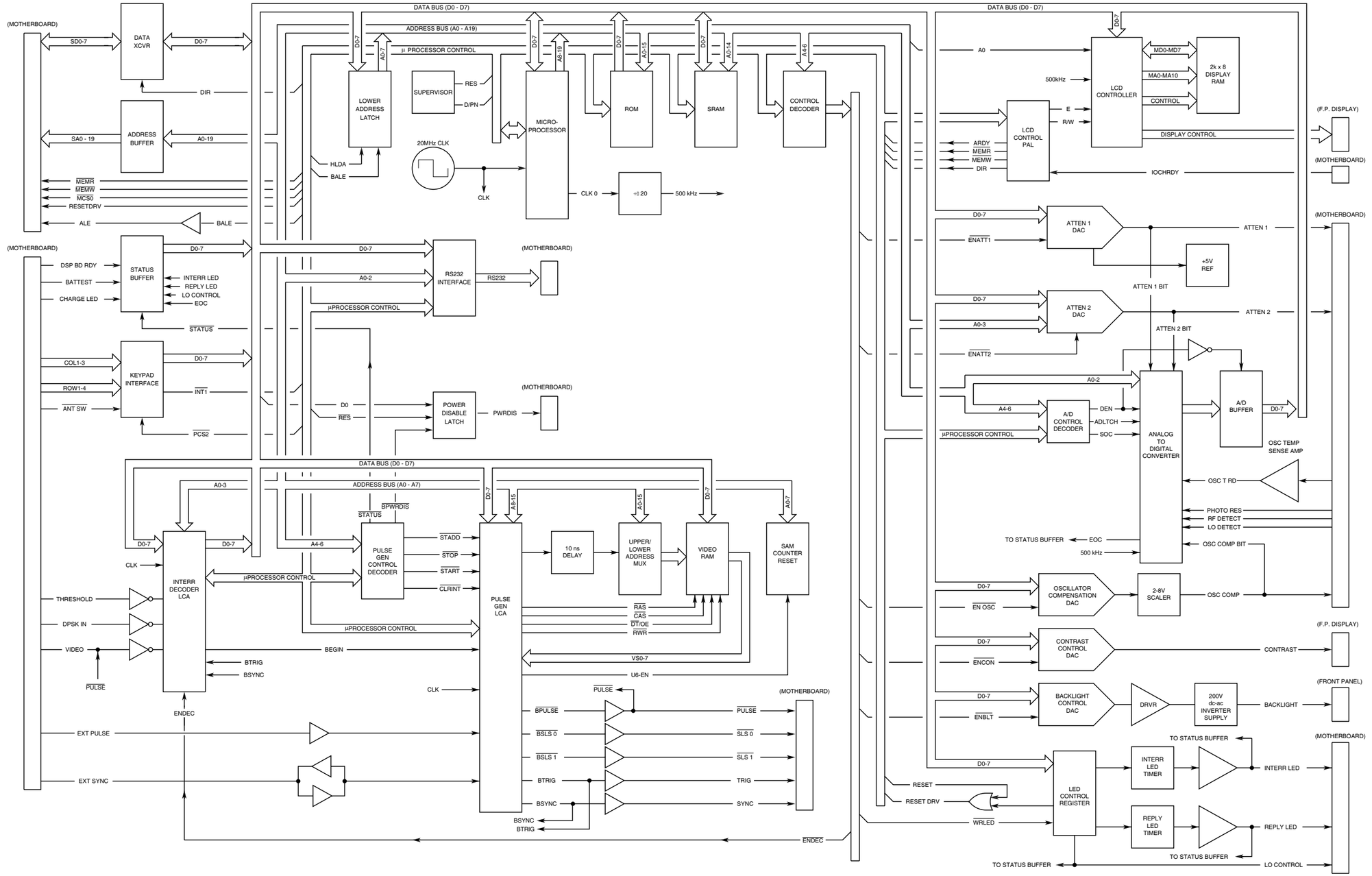

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Front Panel Pulse PCB Assy Block Diagram
Figure 5

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(3) Front Panel Pulse PCB Assy (2-2-1, Figure 5)

The Front Panel Pulse PCB Assy controls the general operation of the TCAS-201-2 Test Set by providing an interface to the user, decoding interrogations, generating replies and controlling both the Digital IF PCB Assy and RF Assy.

(a) Processor

The Processor has four major components: Microprocessor U27001, two 64k ROMs (U27012 and U27013) and 32k non-volatile SRAM U27017. U27001, an 80188 microprocessor, receives instruction data from the two 64k ROMs and carries out assignments as instructed. U27001 uses 11 chip selects. Refer to 2-2-1, Table 3 for chip select definition. Chip select lines are active low. SRAM U27017 has internal battery back-up to prevent loss of memory.

CHIP SELECT	LINE	SELECTION	ADDRESSES
Upper	$\overline{UCS}$	64k ROM (U27012)	F0000-FFFFFh
Lower	$\overline{LCS}$	32k SRAM (U27017)	00000-08000h
Mid-Range	$\overline{MCS0}$	Digital IF PCB Assy (U26007)	C0000-CFFFFh
	$\overline{MCS1}$	Pulse Generator (U27022)	D0000-DFFFFh
	$\overline{MCS2}$	64k ROM (U27013)	E0000-EFFFFh
Peripheral	$\overline{PCS0}$	Control Decoder (U27008)	400-47Xh
	$\overline{PCS1}$	RS-232 Interface (U27030)	480-487h
	$\overline{PCS2}$	Keypad Interface (U27027)	500h
	$\overline{PCS3}$	Control Decoder (U27037)	580-5FXh
	$\overline{PCS4}$	Control Decoder (U27036)	600-67Xh
	$\overline{PCS5}$	LCD Controller (U27048)	680-681h

Microprocessor U27001 Chip Selects
Table 3

Instruction sequence:

- Address latch enable (BALE) line (U27001-61) to Transparent Latch U27010 goes high, allowing U27001 to set address where data is to be received through data lines to U27010.
- When address is valid, BALE goes low, causing lower 8 bits of address to be latched onto U27010 address lines. Lower Address Latch U27010 allows U27001 to receive data on data lines without changing address selected.
- $\overline{UCS}$ line (U27001-34) is low to enable U27012. Read ($\overline{RD}$) line (U27001-62) goes low to enable data byte at address selected (initial address is FFFF0) to be sent to U27001.
- Data is processed and instruction is carried out in same fashion. BALE goes high, chip is selected, valid address is latched and data is read from or written to address. Write ($\overline{WR}$) line (U27001-63), goes low and $\overline{RD}$ line stays high when sending data to an address.

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U27001 also provides Direct Memory Access (DMA) capabilities for Interrogation Decoder U27044. DRQ0 (U27001-18) line sets up DMA, allowing a direct read or write to memory. DRQ0 from Interrogation Decoder (U27044-A9) goes high to initiate DMA request. U27001 finishes current instruction or bus cycle before allowing access. Data at address $\overline{PCS4}$+6Dh (Pulse Generator start address) is sent to Pulse Generator U27022. DMA is reset low at start of read cycle from address $\overline{PCS4}$+6Dh.

There are four interrupt lines used on U27001. INT0 (U27001-45) goes high from U27030, informing U27001, a transmit or receive action is required at the RS-232 Interface. INT1 (U27001-44) is high when activated by Keypad operation. Pressing any key generates an interrupt. INT2 (U27001-42) is activated by Pulse Generator U27022 and INT3 is controlled by Interrogation Decoder U27044.

U27001 operates using an external 20 MHz clock source. D Flip-Flop U27007B divides 40 MHz Oscillator G27001 output by two. The 20 MHz clock is fed into U27001-59. U27001 divides the 20 MHz by two to provide the 10 MHz Clock used internally and sent out on CLKO line U27001-56.

Two internal timer circuits are utilized by the Processor. Timer 0 measures the Whisper-Shout step interval in ATCRBS Monitor mode. Timer 0 also tracks the intervals when the DSP on the Digital IF PCB Assy is detecting a Mode S interrogation. Intervals are timed to prevent a new interrogation from overwriting the interrogation currently being detected. Timer 2 is the software system timer, providing 10 ms resolution for scheduling software processes and measuring ATCRBS Whisper-Shout sequence intervals and Mode S Surveillance intervals.

A reset circuit consisting of Supervisor U27018, Q27001 and associated components provide a delay after power-up or brown-out. The delay (≈15 ms) allows the +5 V from the Power Supply Assy and 40 MHz Oscillator G27001 to stabilize. Reset is activated manually through S27001 (low ground to U27018-2) or automatically if the +5 V sensed at U27018-7 drops below approximately 4.55 V. U27018 output initiates Logic Cell Array (LCA) programming. The low at U27018-5 is sent to the Interrogation Decoder and Pulse Generator. The high at U27018-6 activates Q27001 allowing the low ground at the emitter to be felt on the D/PN line (reset to U27001). The LCA components, Pulse Generator U27022 and Interrogation Decoder U27044, hold the D/PN line low until programming is complete. U27001 resets and sends out another reset (U27001-57) to other logic components on the Front Panel Pulse PCB Assy and Digital IF PCB Assy. Reset output is maintained until the +5 V line reaches ≈4.7 V. Refer to Appendix D for reset timing diagram.

A Power Disable circuit saves on battery power when the Keypad is inactive. U27001 monitors Keypad activity and if no key is pressed for approximately 15 minutes, D Flip-Flop U27007A is accessed with $\overline{PCS0}$+1Xh through U27008 and a low is sent on D0 causing PWRDIS to go high to the Power Supply Assy. Comparator U14008A on the Power Supply Assy resets Flip-Flop U14002A and disables the Output Supply, switching off the power. PWRDIS returns to low on power-up or after reset.

(b) Pulse Generator

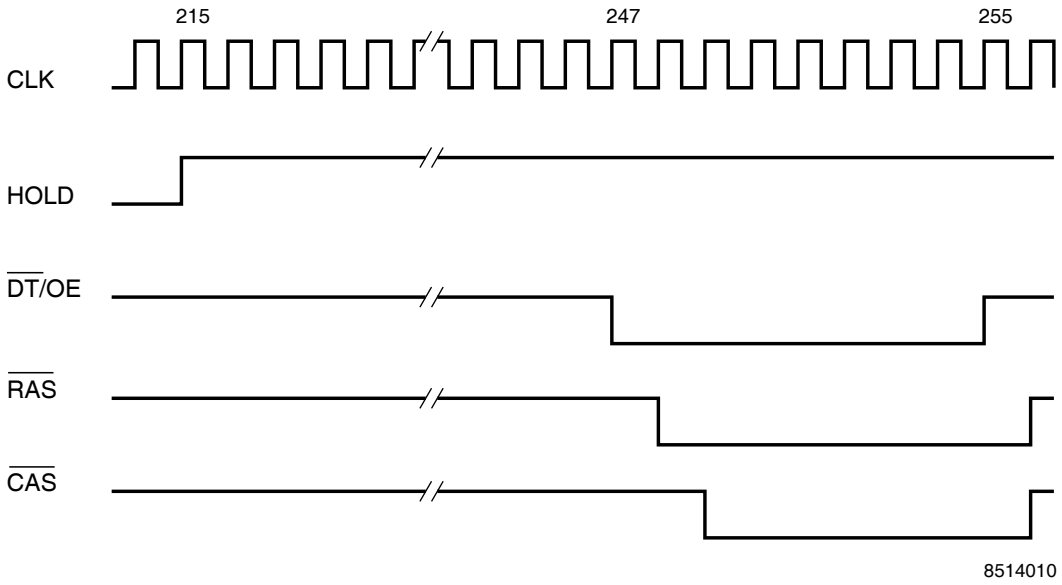
The Pulse Generator section of the Front Panel Pulse PCB Assy consists of programmable LCA U27022, Video RAM chips U27023 and U27024, Serial Access Memory (SAM) Counter Reset U27006, Buffer/Driver U27004, Multiplexers (MUX) U27015 and U27016, Delay DL27001, Schmitt Trigger Inverter U27025A, Control Decoder U27008 and PROM U27003.

The Video RAM chips are dual port with random access available to U27001 and serial access to U27022. U27001 reads and writes to the Video RAM chips with access controlled through U27022. Video RAM chips U27023 and U27024 are accessed when $\overline{\text{MCS1}}$, BALE and either $\overline{\text{WR}}$ or $\overline{\text{RD}}$ are activated. Addresses are selected using Multiplexers U27015 and U27016. When $\overline{\text{RAS}}$ goes low, the select line to U27015 and U27016 stays high because the output at U27022-43, changing to high (inverted low by U11025A) when $\overline{\text{RAS}}$ goes low, is delayed 10 ns through DL27001. This allows A8 through A15 to be latched to the Video RAM chips, selecting the row address. After the delay, the multiplexers with the select line low are set to latch A0 through A8 to the Video RAM chips, selecting the column address when $\overline{\text{CAS}}$ goes low. $\overline{\text{DT}}$/OE goes low for a read operation or $\overline{\text{WR}}$ goes low for a write operation.

Serial access by U27022 is a read only function. The Video RAM chips transfer rows (256 bytes/row) of data into internal serial access registers. Data is sent from the registers to U27022, one byte each clock count. Serialized data is sent out from U27022 with each bit line connected to a specific output according to 2-2-1, Table 4.

VIDEO RAM	PIN NO	U27022	PIN NO
VS0	24	$\overline{\text{BPULSE}}$	28
VS1	29	$\overline{\text{BSLS0}}$ Not Used (low)	30
VS2	31	BDPSK Not Used	32
VS3	33	BTRIG	34
VS4	36	BSYNC	37
VS6	38	$\overline{\text{BSLS1}}$ Not Used (low)	39

Pulse Generator Serialized Data Output
Table 4



Pulse Generator Data Transfer Timing Diagram
Figure 6

Pulse Generator serial sequence:

- U27001 programs pulses into Video RAM chips, as directed by ROM and initiated by Keypad entry (setting operating mode and pressing RUN/STOP Key). During Scenario Test, U27001 reprograms Video RAM chips once every second, updating for new range delay.
- U27001 programs stop bytes (10010000) into addresses XXFEh (255th byte) designating the desired rows to end with.
- U27001 programs 256 bytes of cleared memory (00h).
- U27001 programs starting addresses using STADD line ($\overline{PCS0}$+2Xh) through U27008 for access.
- For Mode S operation with Squitters selected, U27001 sets $\overline{START}$ line low through U27008 ($\overline{PCS0}$+4Xh) to U27022. Data transfers start with internal counter set to 191h in preparation to transmit Mode S (DF11) squitters.

  For Mode S operation after receiving valid interrogation, Interrogation Decoder U27044 determines reply to be transmitted. U27044 uses DMA to send starting address of correct reply in Video RAM, to Pulse Generator U27022. U27001 retrieves starting address from U27017 when needed by the Pulse Generator. The BEGIN line (U27044-G1) from Interrogation Decoder goes high to the Pulse Generator (U27022-19) initiating start of data transfers and setting internal counter to 191h.
- After the 215th byte of cleared memory, U27022 HOLD output (pin 53) goes high to request access to the address lines from U27001.
- HLDA input (pin 20) goes high informing U27022 that U27001 relinquishes address line control.

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Pulse Generator serial sequence (cont):

- After 247 bytes, $\overline{DT}$/OE goes low to set up Video RAM chips for a data transfer to the serial access registers.
- $\overline{RAS}$ goes low on the next clock count. The row address, determined by programmed starting address, is selected.
- $\overline{CAS}$ goes low on the following clock count and the zero address from U27006 (enabled by U27022) causes a data transfer to start at address zero in the serial access registers.
- After 255 bytes of cleared memory is shifted out of the serial access registers, $\overline{DT}$/OE goes high, triggered by an internal counter in U27022. U27022 internal counter tracks 256 clock counts.
- The data transfer occurs. 256 new bytes from the selected row are loaded into the serial access registers.
- Each data transfer is followed by a $\overline{CAS}$ before $\overline{RAS}$ refresh.

  NOTE: When no data transfers are occurring, refresh still takes place every 12.8 µs.

- With each 50 ns (20 MHz) clock count, one byte (one bit for each output) is shifted out of the serial access registers to U27022.
- A data transfer occurs every 12.8 µs with each successive row as stepped by the internal counter in U27022. New rows are transferred and sent out until the programmed stop byte is encountered. After the stop byte, the last row is transferred and continually shifted out of the serial access registers until next transfer.

  NOTE: The last row transferred is usually the 256 bytes of cleared memory. For CW transmissions, the last row contains all ones.

- The stop byte also initiates an interrupt (INT2) to U27001.

  NOTE: If another interrupt is received during operation, Microprocessor U27001 manually stops Pulse Generator operation by activating the $\overline{STOP}$ line ($\overline{PCS0}$+3Xh).

Buffer/Driver U27004 is used to isolate and boost signals off the Front Panel Pulse PCB Assy. Configuration PROM U27003 stores information for reprogramming U27022 on power-up. External PULSE and External SYNC from the COMM Connector, when connected, are isolated and converted to TTL before entering the Pulse Generator.

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(c) Interrogation Decoder

Interrogation Decoder U27044 is a programmable LCA component. U27044 decodes Mode C All Calls in ATCRBS and UF0 or UF16 interrogations in Mode S. Microprocessor U27001 selects U27044 through U27036 when $\overline{PCS4}$ is activated with addresses 60 to 6Fh. Refer to 2-2-1, Table 5 for address descriptions.

ADDRESS	DESCRIPTION	BITS	READ/WRITE
60h	Control Register	D0-D7	Write Only
61h	TCAS-201-2 Address, Bits 0-7	D0-D7	Write Only
62h	TCAS-201-2 Address, Bits 8-15	D0-D7	Write Only
63h	TCAS-201-2 Address, Bits 16-23	D0-D7	Write Only
64h	Not Used		
65h	Not Used		
66h	Not Used		
67h	Not Used		
68h	Manual Trigger for DSP Digitizer	XX-XX	Write Only
69h	Status Register	D0-D7	Read Only
6Ah	Rcvd Mode S Address, Bits 0-7	D0-D7	Read Only
6Bh	Rcvd Mode S Address, Bits 8-15	D0-D7	Read Only
6Ch	Rcvd Mode S Address, Bits 16-23	D0-D7	Read Only
6Dh	Pulse Generator Start Address	D0-D7	Read Only
6Eh	Not Used		
6Fh	Not Used		

Interrogation Decoder Address Descriptions
Table 5

U27001 controls the Interrogation Decoder by setting an internal control register. Refer to 2-2-1, Table 6 for control register bit definition.

BIT #	DEFINITION	SETTING	RESULT
D0	Reset	0	Released
		1	Interrogation Decoder is reset. All incoming interrogations and triggers are ignored. INT3 and DRQ0 lines are cleared.
D1	Mode of Operation	0	ATCRBS
		1	Mode S
D2	Invert Video	0	Incoming VIDEO is not inverted (testing).
		1	Incoming VIDEO is inverted (normal operation).
D3	Invert Threshold	0	Incoming THRESHOLD is not inverted (testing).
		1	Incoming THRESHOLD is inverted (normal operation).
D4	Disable DSP Trigger	0	DSP trigger is enabled.
		1	DSP trigger is disabled.
D5	Disable Pulse Generator Trigger	0	Pulse Generator trigger is enabled (Scenario Test and Reply Test functions).
		1	Pulse Generator trigger is disabled (Monitor function).
D6	Not Used		
D7	Not Used		

Interrogation Decoder Control Register Bit Definition
Table 6

Control register sequence:

- $\overline{\text{PCS4}}$+60h through U27036 causes $\overline{\text{ENDEC}}$ (U27044-P11) to go low.
- $\overline{\text{WR}}$ (U27044-P12) goes low.
- Data is written to U27044 (A13, B13, C13, D13, A12, B12, C12 and D12) setting the control register.

U27001 also sets the TCAS-201-2 address used to verify if interrogations are intended for the Test Set. U27044 has three internal, 8-bit TCAS-201-2 address registers. The TCAS-201-2 address registers are initialized on power-up to last address loaded into Mode S Reply Test screen ***AA:*** field.

Interrogation Decoder functions depend on mode of operation.

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Mode S sequence:

- U27044 samples VIDEO input (U27044-P9), inverted by U27051A and THRESHOLD input (U27044-B1), inverted by U27051E. Acceptable interrogations must be received on both lines.
- U27044 internal DPSK decoder is enabled when P_1, P_2 and P_6 pulses are detected.
- After 100 to 150 ns following the rising edge of P_1, U27044 sends a 50 ns trigger on BTRIG through Buffer/Driver U27004 to DSP digitizer.
- U27044 DPSK decoder looks for SPR. When SPR is detected, the contents of P_6 are decoded.
- U27044 verifies:

  Interrogation received is UF0 or UF16.

  AP field contains TCAS-201-2 address.

  RL and AQ field settings for selecting the desired reply.
- U27044 uses DMA to send the address of the applicable reply in Video RAM to Pulse Generator U27022. If RL and AQ are both zero, DF0 tracking is the correct reply located at address 23h. If RL is one and AQ is zero, DF16 tracking is the correct reply located at address 6Fh. If RL is zero and AQ is one, DF0 acquisition is the correct reply located at address FFh. If RL and AQ are both one, DF16 acquisition is the correct reply at address 47h.
- U27044 sets internal status register.
- At 128 µs after SPR, U27044 sends 100 ns pulse on the BEGIN line to trigger Pulse Generator for reply.
- U27044 sets INT3 high for an interrupt to U27001.
- $\overline{RD}$ (U27044-P13) goes low. U27001 reads U27044 status register and Rcvd Mode S address. Refer to 2-2-1, Table 7 for status register bit definition.
- U27001 writes to U27044 control register twice to reset and release Interrogation Decoder ($\overline{PCS4}$+60h-D0), clearing the interrupt.

ATCRBS sequence:

- U27044 samples the VIDEO input (U27044-P9), inverted by U27051A and the THRESHOLD input (U27044-B1), inverted by U27051E. Acceptable interrogations must be received on both lines.
- When pulses are detected, U27044 verifies Mode C All-Call spacing. Refer to Appendix D, Figure 3.
- If the interrogation is a valid Mode C All-Call with no suppression, at 3 µs after the rising edge of P_3, U27044 sends a pulse on the BEGIN line to trigger the Pulse Generator for reply. Refer to Appendix D, Figure 4.

BIT #	DEFINITION	SETTING	RESULT
D0	Address Test	0	Interrogation Address differs from TCAS-201-2 Address.
		1	Interrogation Address matches TCAS-201-2 Address.
D1	UF0	0	Interrogation is not UF0.
		1	Interrogation is UF0.
D2	UF16	0	Interrogation is not UF16.
		1	Interrogation is UF16.
D3	RL	0	RL field (data bit 9) in interrogation is set to zero.
		1	RL field (data bit 9) in interrogation is set to one.
D4	AQ	0	AQ field (data bit 14) in interrogation is set to zero.
		1	AQ field (data bit 14) in interrogation is set to one.
D5	N_SPR	0	SPR is detected.
		1	SPR is not detected.
D6	Not Used		
D7	Not Used		

Interrogation Decoder Status Register Bit Definition For Mode S
Table 7

- U27044 sets the internal status register.
- U27044 sets INT3 high for an interrupt to U27001.
- $\overline{RD}$ (U27044-P13) goes low. U27001 reads U27044 status register. Refer to 2-2-1, Table 8 for status register return code.

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ATCRBS sequence (cont):

- U27001 writes to U27044 control register twice to reset and release Interrogation Decoder ($\overline{PCS4}$+60h-D0), clearing the interrupt.

INTERROGATION PULSES PRESENT						RETURNED CODE
S_1	P_1	P_2	$P_{2'}$	P_3	P_4	
	X			X	X	46h
	X	X		X	X	66h
	X	X	X	X	X	6Eh
	X		X	X	X	4Eh
X	X			X	X	63h
X	X	X		X	X	73h
X	X		X	X	X	67h
X	X	X	X	X	X	77h
NOTE: Most significant bit (D7) is invalid and masked off.						
NOTE: $P_{2'}$ is an additional SLS condition.						

Interrogation Decoder Status Register Return Code For ATCRBS
Table 8

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(d) Display Control

Three separate circuits make up the Display Control. The Liquid Crystal Display (LCD) Data Control circuit controls the information entered onto the DISPLAY. The Contrast Control and Backlight Control circuits use Digital-to-Analog Converters (DACs) to adjust visual characteristics of the LCD.

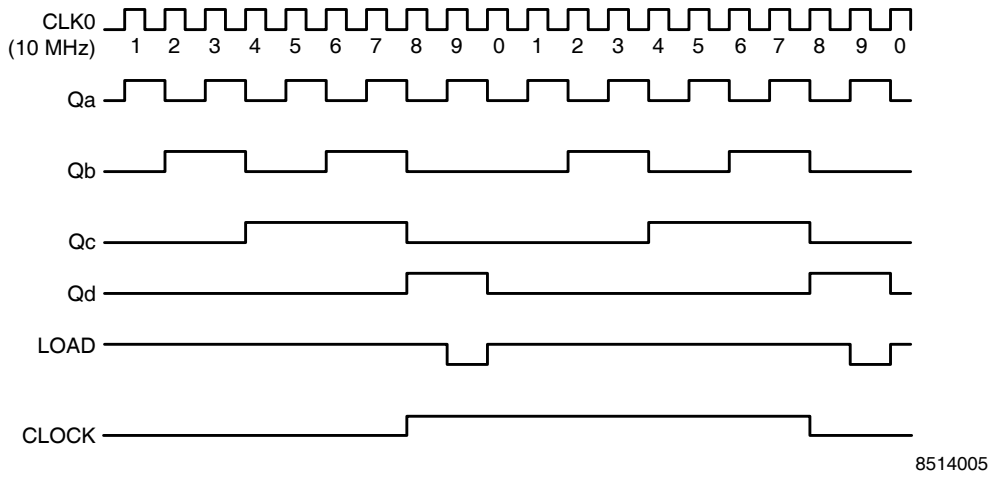
1 LCD Data Control

LCD Data Control is accomplished with a 500 kHz Clock, LCD Controller U27048, LCD Control PAL U27029 and Display RAM U27049.

Refer to 2-2-1, Figure 7 for 500 kHz Clock timing. Counter U27039 divides the 10 MHz clock input by 10 (NAND Gate U27011C resets U27039 on each nine count). The 1 MHz output clocks D Flip-Flop U27007B, configured to change state with each clock, providing a 500 kHz clock with a 50% duty cycle. The 500 kHz clock is verified at test point TP27004.

LCD Controller U27048, an HD61830 Graphic Display Controller operating in the character mode, acts as a memory mapped device to the Processor. U27001 reads from and writes to U27048 on a byte wide basis. U27001 selects U27048 by activating $\overline{\text{PCS5}}$, accessing the data register at address X0h (RS input U27048-18 low) and the instruction register at address X1h (RS input U27048-18 high).

U27048 has six outputs to the LCD. D1 is the serial data output for the upper half of the screen and D2 is the serial data output for the lower half of the screen. FLM is the frame signal for display synchronization. CL1 is the display data latch signal for LCD drivers and CL2 is the display data shift clock for LCD drivers. M converts the LCD driving signal to an ac waveform.



500 kHz Clock Timing Diagram
Figure 7

PAL U27029 inserts wait states in the processor bus cycle. Refer to Appendix C for PAL equations. U27029 also generates the Enable (U27048-16) and Read/Write (U27048-17) signals for U27048. Wait states, inserted before the ARDY line to U27001 goes low, are required because LCD Controller U27048 operates slower than the microprocessor. Refer to Appendix D for timing diagrams.

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Display RAM U27049 stores pixel data (character codes) for U27048 and is accessed by U27001 through U27048.

2 Contrast Control

Contrast Control is based on the input voltage obtained from CR22001 on the Analog IF PCB Assy. Ambient temperature conditions are sensed by CR22001 and the resulting voltage (2.73 V at 0° C, changes 33.94 mV/°C) is sent through a differential amplifier U27034C to the ADC (U27045-1). Refer to para 2-2-1D(3)(i) for ADC operation. The information sent from U27045 causes U27001 to send adjustment data to DAC U27032, selected by $\overline{\text{ENCON}}$ ($\overline{\text{PCS4}}$+1Xh through U27036) going low. U27032 provides a bipolar output of -5 to +5 V, used to control the contrast on the LCD. The -5.1 V, used in powering the LCD, is provided by the voltage drop across Zener Diode CR27011.

3 Backlight Control

Backlight Control is based on the input voltage obtained from R13001 on the Front Panel LED PCB Assy. Ambient light conditions are sensed by R13001 and the resulting voltage drop is applied to the ADC (U27045-26). Refer to para 2-2-1D(3)(i) for ADC operation. Information sent from U27045 causes U27001 to send adjustment data to DAC U27033, selected by $\overline{\text{ENBLT}}$ ($\overline{\text{PCS4}}$+0Xh through U27036) going low. U27033 provides a corresponding voltage output through Driver U27034A with Q27005 to drive Inverter Supply U27035. U27035 provides the increased voltage levels necessary to run the backlight. Capacitors C27082 and C27083 provide noise suppression in the operational amplifier feedback circuit. Zener Diodes CR27016 and CR27017 are clamped to ground to protect circuit if backlight is not connected.

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(e) Keypad Interface

Keypad Interface consists of Buffer/Latch U27027, NAND Gate U27011B, resistors, transistors and diodes. U27027 is selected by U27001 with $\overline{PCS2}$. Keypad data, activated when low, is defined in 2-2-1, Table 9.

When the Keypad is inactive, Resistive Network RN27001 holds the row and column lines to a high impedance. When a key is pressed, a row and column line are connected together.

	COLUMN BIT		
ROW BIT	**D1 ($\overline{COL1}$)**	**D2 ($\overline{COL2}$)**	**D3 ($\overline{COL3}$)**
D4 ($\overline{ROW1}$)	MON Key	RPLY TEST Key	SCEN Key
D5 ($\overline{ROW2}$)	PWR TEST Key	RUN/STOP Key	SLEW Key (↓)
D6 ($\overline{ROW3}$)	SELECT Key (↑)	SELECT Key (↓)	SLEW Key (↑)
D7 ($\overline{ROW4}$)	Not Used	SELF TEST Key	SET/CONT Key
NOTE: D0 is $\overline{ANTSW}$ from the ANTENNA PUSH BUTTON Switch.			

Keypad Data Definition
Table 9

Keypad sequence example:

- Pressing the MON Key connects row 1 with column 1. Circuit is closed and current flows.
- Current flowing at the base turns Q27002 on, allowing the low ground on the emitter through the collector and Diode CR27001 to NAND Gate U27011B. The high output sends an interrupt (INT1) to the Microprocessor (U27001-44).
- The low through Q27002 is also sent through U27027 when selected by U27001 with $\overline{PCS2}$. The low on collector of Q27002 is felt at U27027-4, causing D0 to be read low by U27001 indicating the pressed key is in column 1. The low on the base of Q27002 is felt at U27027-11, causing D4 to be read low indicating the pressed key is in row 1.

(f) RS-232 Interface

RS-232 communication is provided by an INTEL 82510 Universal Asynchronous Receiver-Transmitter (UART U27030). U27030 is selected by U27001 with $\overline{PCS1}$ (addresses from X0h to X7h). Driver/Receiver U27028 drives the serially transmitted signal off the Front Panel Pulse PCB Assy through P/J25014 to J10053 COMM Connector and buffers incoming handshake and data signals. U27030 generates an interrupt (INT0) when servicing is required. U27001 polls the internal status registers to determine the cause of the interrupt (TXD or RXD).

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(g) Attenuator Control

Two DACs having 0 to 10 Vdc outputs control attenuation. U27041, an 8-bit DAC, provides a +5 V reference and ATTEN1 voltage used to set current on the Driver PCB Assy for attenuator end line pin diodes on the Attenuator PCB Assy. R27041 (+5V REF ADJ) adjusts the +5 V reference, verified at TP27002. U27041 is accessed by U27001 when $\overline{\text{ENATT1}}$ ($\overline{\text{PCS4}}$+5Xh through U27036) goes low. U27042, a 12-bit DAC, provides the ATTEN2 voltage used to set current on the Driver PCB Assy for attenuator midline pin diodes on the Attenuator PCB Assy. U27041 is accessed by U27001 when $\overline{\text{ENATT2}}$ ($\overline{\text{PCS4}}$+4Xh through U27036) goes low. Address lines A0-A3 are used to select the data transfer process. Refer to 2-2-1, Table 10. Both output levels are read from ADC U27045.

(h) Oscillator Compensation

Oscillator Compensation is based on the input voltage obtained from CR22001 on the Analog IF PCB Assy. R27037 (TEMP COMP ADJ) is adjusted at the factory and used in board level calibrations. Ambient temperature conditions are sensed by CR22001. The resulting voltage (2.73 V at 0° C, changes 33.94 mV/°C) is applied through Differential Amplifier U27034C to ADC U27045-1. Refer to para 2-2-1D(3)(i) for ADC operation. Information sent from U27045 causes U27001 to send adjustment data to DAC U27043, selected by $\overline{\text{ENOSC}}$ ($\overline{\text{PCS4}}$+2Xh through U27036) going low. U27043 provides a 0 to 10 V output. Operational Amplifier U27050 and associated components offset, scale and low-pass filter to achieve the desired 2 to 8 Vdc output. Output level is read from ADC U27045.

ADDRESS	OPERATION	BITS
4Eh	Load low nibble	D0-D3
4Dh	Load middle nibble	D4-D7
4Ch	Load low byte (optimum method)	D0-D7
4Bh	Load high nibble	D0-D3, D3 = MSB
47h	Transfer data	XX
43h	Load high nibble and transfer data (optimum method)	D0-D3, D3 = MSB

Attenuator #2 Operation Selection
Table 10

(i) Analog-to-Digital Converter

ADC U27045 is used for both normal operation and Self Test operation. Refer to 2-2-1, Table 11 for analog input to ADC description.

INPUT	ADDRESS	DESCRIPTION
PHOTO RES Channel 0	$\overline{PCS3}$+10h	Voltage across Photo Resistor R13001 (Front Panel LED PCB Assy), set by ambient light conditions, is used in making Backlight Control adjustments.
RF DETECT Channel 1	$\overline{PCS3}$+11h	Provides indication if RF carrier is present (Self Test). 2.5 V (±0.125 V) indicates passing status (only active in CW mode).
Channel 2	$\overline{PCS3}$+12h	Not Used
OSC T RD Channel 3	$\overline{PCS3}$+13h	Voltage across Diode CR19001 (Analog PCB Assy), controlled by ambient temperature conditions, is used in making Contrast Control and Oscillator Compensation adjustments.
LO DETECT RD Channel 4	$\overline{PCS3}$+14h	Local Oscillator Detect (Self Test): Pass - constant level between 0.35 and 3.1 Vdc, Fail - oscillation (at ≈7.5 Hz) or level outside Pass voltage window (0 to 0.35, 3.1 to 4.14 V).
ATTEN1 BIT Channel 5	$\overline{PCS3}$+15h	Provides level of Attenuator #1 DAC output (DAC output ÷ 2.5 [±10%])
ATTEN2 BIT Channel 6	$\overline{PCS3}$+16h	Provides level of Attenuator #2 DAC output (DAC output ÷ 2.5 [±10%])
OSC COMP BIT Channel 7	$\overline{PCS3}$+17h	Provides oscillator compensation level (DAC output ÷ 2.5 [±10%])

Analog Input to ADC Description
Table 11

ADC sequence:

- U27001 selects channel address with $\overline{PCS3}$+1X through Control Decoder U27037 and, with $\overline{WR}$ active, through NOR Gate U27038B (ADLTCH). The high output is sent to U27045-22 along with specific lower address (A0-A2), latching the desired channel to the ADC.
- The start A/D conversion command is sent using address $\overline{PCS3}$+0Xh through U27037, and with $\overline{WR}$ active, through NOR Gate U27038C (SOC). The high output is sent to U27045-6. Conversion begins and End of Conversion (EOC) line to Status Buffer U27026 goes low (within 18 µs from when start command was issued).
- U27001 polls the EOC signal from the Status Buffer and when the conversion is finished (≈48 µs), EOC goes high.

ADC sequence (cont):

- Data is read from output Buffer U27046 using address $\overline{PCS3}$+2Xh through U27037, and with $\overline{RD}$ active, through NOR Gate U27038D (DEN). The high output is sent to U27045-9 and through Inverter U27038A to activate U27046. Two data reads are required to receive all 10 bits. Data is sent out as follows:

Data Bit Locations:	D7	D6	D5	D4	D3	D2	D1	D0
First Read (Bit #):	10	9	8	7	6	5	4	3
Second Read (Bit #):	2	1	X	X	X	X	X	X

Bit 10 = MSB, Bit 1 = LSB

(j) Status Buffer

Status Buffer U27026 enables the current condition of several signals to be read and is accessed with address $\overline{PCS0}$+0Xh through U27008. Refer to 2-2-1, Table 12.

BIT #	DEFINITION	SETTING	RESULT
D0	Current state of REPLY LED output from LED Control Register	0	LED is Off.
		1	LED is On.
D1	Current state of INTERR LED output from LED Control Register	0	LED is Off.
		1	LED is On.
D2	Conversion status of ADC (EOC)	0	Conversion in progress
		1	Conversion complete
D3	Ready status of DSP on Digital IF PCB Assy	0	DSP not ready
		1	DSP ready and working
D4	Monitor Enable status (JTB27001)	0	Enter Monitor (jumper installed)
		1	Normal operation (jumper not installed)
D5	ac Power status (CHARGE LED)	0	ac Power connected (Q27008 activated)
		1	ac Power not connected (Q27008 turned off)
D6	Battery Charge Level status (BATTEST)	0	Battery ≈70% discharged (≈36 minutes left)
		1	Battery is charged.
D7	Current state of LO CONTROL output from LED Control Register	0	Local Oscillator is enabled.
		1	Local Oscillator is shut down.

Status Buffer Bit Definition
Table 12

(k) LED Control Register

LED Control Register U27040 controls REPLY Indicator, INTERR Indicator, Local Oscillator and Digital IF PCB Assy reset operation. Refer to 2-2-1, Table 13. U27040 is accessed with address $\overline{PCS4}$+3Xh through U27036.

BIT #	DEFINITION	SETTING	RESULT
D0	Reply LED (REPLY Indicator)	0	Sets LED ready for turn On
		1	Initially Off or turns LED On for timed period
D1	Interrogation LED (INTERR Indicator)	0	Sets LED ready for turn On
		1	Initially Off or turns LED On for timed period
D2	LO Control	0	Enables Oscillator
		1	Shuts down Oscillator
D3	DSP Reset	0	Enables Digital IF PCB Assy
		1	Resets Digital IF PCB Assy
D4 to D7	Not Used		

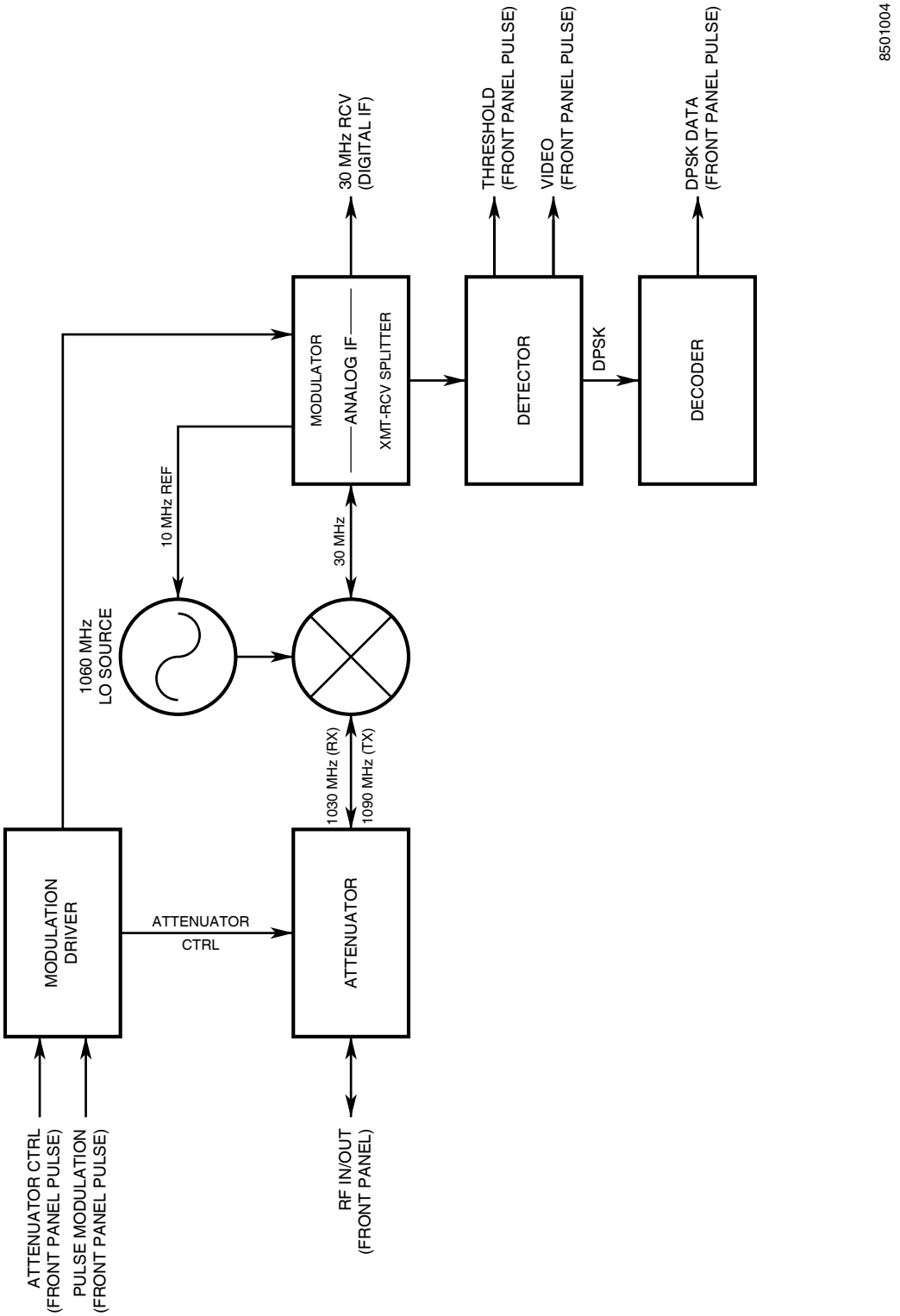
LED Control Register Bit Definition
Table 13

LED bit locations D0 and D1 are set high on power-up. An LED is turned on by writing zero and then one to the respective bit location in the control register. The zero to one transition triggers One-Shot Timer U27047. The high level output from U27047, timed for ≈62 ms, activates transistor Q27006 or Q27007 turning on the respective indicator.

(l) Digital IF PCB Assy Access

DPR U26007 on the Digital IF PCB Assy is accessed using $\overline{MCS0}$. Access is controlled by PAL U27029. DIR goes high to activate data lines through Transceiver U27009. $\overline{MEMR}$ goes low to read DPR or $\overline{MEMW}$ goes low to write to DPR.

(4) RF Assy (2-2-1, Figure 8)



RF Assy Block Diagram
Figure 8

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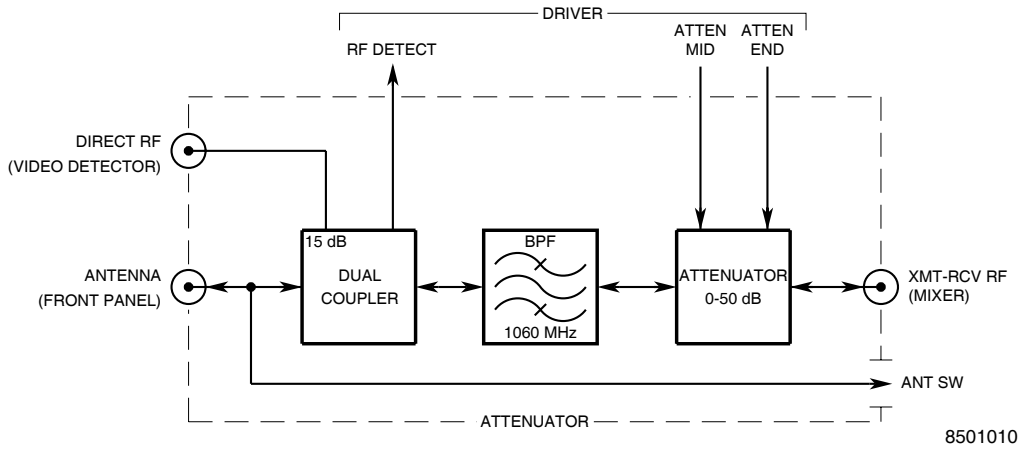
(a) SSB Assy

The Single-Sideband (SSB) Assy provides a two-way conversion between an IF of 30 MHz and an RF of 1090 MHz (transmit) or 1030 MHz (receive). The SSB Assy consists of the Attenuator PCB Assy, LO Source PCB Assy and Mixer PCB Assy.

1 Attenuator PCB Assy (2-2-1, Figure 9)



Attenuator PCB Assy Block Diagram
Figure 9

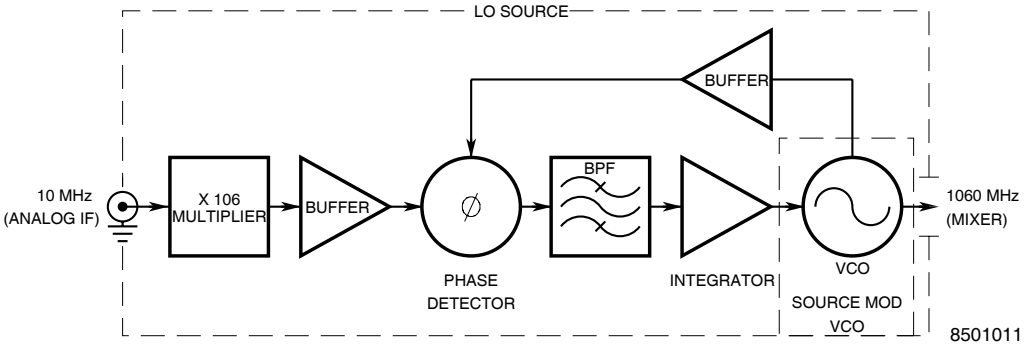
The Attenuator PCB Assy provides 0 to 50 dB of variable attenuation for measurement and testing purposes. The Attenuator PCB Assy consists of a dual coupler, bandpass filter and pin diode attenuator.

Dual Coupler HY31001 provides two RF signals, 15 dB down from the calibrated level at the ANTENNA Connector (J10057). On transmit, one signal drives biased Diode Detector CR31001. CR31001 provides a dc level proportional to RF level and is used for the RF Detect test (Self Test). On receive or transmit, the signal is coupled, 15 dB down, to the RF I/O Connector (J10058) through the Video Detector PCB Assy and Power Termination Assy.

Microstrip Bandpass Filter HY31002 rejects signals outside the 300 MHz bandwidth (passes 910 to 1210 MHz signals).

The pin diode attenuator consists of four pin diodes (CR31003-CR31006) and associated components. The pin diodes are spaced 1/4 wavelength apart and act as current controlled resistors. The Driver PCB Assy supplies the controlling current. Midline diodes (CR31004 and CR31005) provide most of the attenuation and end line diodes (CR31003 and CR31006) match the circuit. C31013 and C31015 (ATTEN 1060 MHz ADJ) cancel out series inductance.

2 LO Source Assy and Source Module VCO PCB Assy (2-2-1, Figure 10)



LO Source Assy and Source Module VCO PCB Assy Block Diagram
Figure 10

The LO Source Assy and Source Module VCO PCB Assy provide a 1060 MHz signal using a Voltage Controlled Oscillator (VCO). The frequency is kept tuned by a Multiplier, Phase Detector, Error Amplifier (Integrator) and Temperature Compensator.

The Digitally Controlled Crystal Oscillator (DCXO) from the Analog IF Assy provides the 10 MHz frequency reference to the Multiplier. The reference signal drives the base of High Current Amplifier Q24002. Current Controller Q24001 uses the regulated +11 V from the Driver PCB Assy to bias Q24002. The high level current output from Q24002 drives the multiplying varactor, Snap Diode CR24002. R24049 sets the voltage reference for CR24002. L24002 and C24004 provide impedance matching to increase the multiplying efficiency of CR24002. CR24002 generates 10 MHz spectral lines. C24005 and Z24001 form a tank circuit tuned to 1060 MHz, enhancing the 106th harmonic. The signal, monitored at TP16002, is fed into a three-stage linear buffer amplifier consisting of Saturable Transistors Q24003, Q24004 and Q24005. The buffer amplifier, tuned to 1060 MHz, increases the power of the desired harmonic and drives an input to Phase Detector HY24001.

The other HY24001 input is from the Voltage Controlled Oscillator (VCO) on the Source Module VCO PCB Assy. Oscillating transistor Q24001, driven with a regulated +11 V from the Driver PCB Assy, is matched to the frequency determining element, Resonator HY34001. Temperature Compensator C34007 and Varactor CR34001 keep the oscillator tuned to 1060 MHz. Power is coupled off the oscillator through Z24014 and is fed back to the LO Source PCB Assy through a buffer amplifier, composed of Saturable Transistors Q24007, Q24008 and Q24009. The buffer, also tuned to 1060 MHz, drives the local oscillator input to HY24001.

HY24001 and CR24003 form a Phase Detector providing a dc error voltage proportional to the phase difference detected between the VCO and Multiplier inputs. This voltage is filtered by Bandpass Filter C24021, L24006 and C24022 and sent to Integrator U24001.

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When the output frequency of the VCO is the same as the output frequency of the Multiplier (Reference), the Phase Detector voltage (checked at TP16003) output to U24001 is minimal, causing negative feedback. U24001 and associated circuitry act as a phase-locked loop filter. When frequencies of the VCO and Multiplier become different, U24001-3 becomes more positive. As the frequencies continue to be different, U24001 becomes a Wien Bridge Oscillator. The ac output is fed to the VCO tuning Varactor CR34001. CR34001 adjusts the resonating frequency fed to HY24001, until error voltage is reduced down and U24001 becomes a phase-locked loop filter again. R24022 (OFFSET) sets a voltage level compensating for imbalances in the Phase Detector and/or buffers. R24025 (DEVIATION) sets the ac deviation voltage limit to prevent the VCO from setting on the 105th or 107th harmonics.

Q24010 exponentially increases current with temperature to provide temperature compensated voltage to VCO Varactor CR34001. VCO Tune Voltage, nominally 4 Vdc, is checked at TP16001 and set by R24026 (TUNING).

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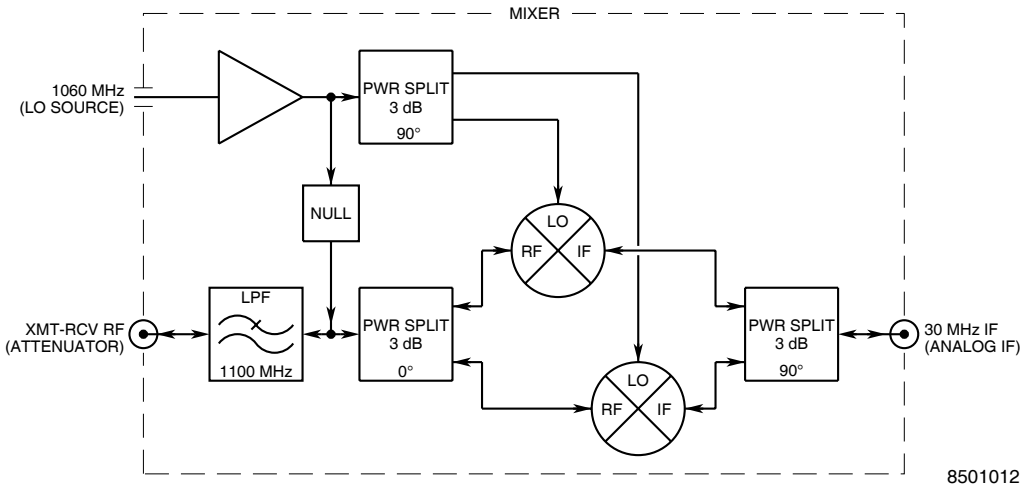
3 Mixer PCB Assy (2-2-1, Figure 11)



Mixer PCB Assy Block Diagram
Figure 11

The Mixer PCB Assy uses the 1060 MHz source signal to convert the 30 MHz transmit signal to 1090 MHz and the 1030 MHz receive signal to 30 MHz. The Mixer PCB Assy consists of a low-pass filter, LO amplifier, mixer null and single-sideband mixer.

The low-pass filter (C18022, L18016, C18023, L18017 and C18024) removes odd harmonics passed by the Attenuator PCB Assy. The low-pass filter consist of a lumped element five pole filter with an elliptical response and provides 1.5 GHz of bandwidth.

The LO amplifier (Q18001, Q18002, Q18003, Q18004 and associated components) provides the necessary gain (≈20 dBm output) to drive the single-sideband mixer after driving the mixer null. Input from the LO Source PCB Assy (≈0 dBm) is fed to base of transistor Q18002. Q18002 is constant-current biased through Q18004 collector for a gain of ≈10 dB at base of Q18003. Q18003 is constant-current biased through Q18001 collector for another gain of ≈10 dB.

The mixer null adds four vectors, set 90° apart with phase shifts along Transmission Line HY18001. The amplified LO source signal is fed into the discrete splitter (L18020, C18031, R18022, L18021 and C18032). One signal is sent to the single-sideband mixer. The other is used as a reference by the mixer null. HY18001 and the summing network cancel out 1060 MHz at any phase from the transmit and receive signals going through the single-sideband mixer at Power Splitter HY18002. R18007 and R18008 (1060 MHz NULL ADJ) control the level. L18018 and L18019 cancel stray capacitance on adjusting resistors.

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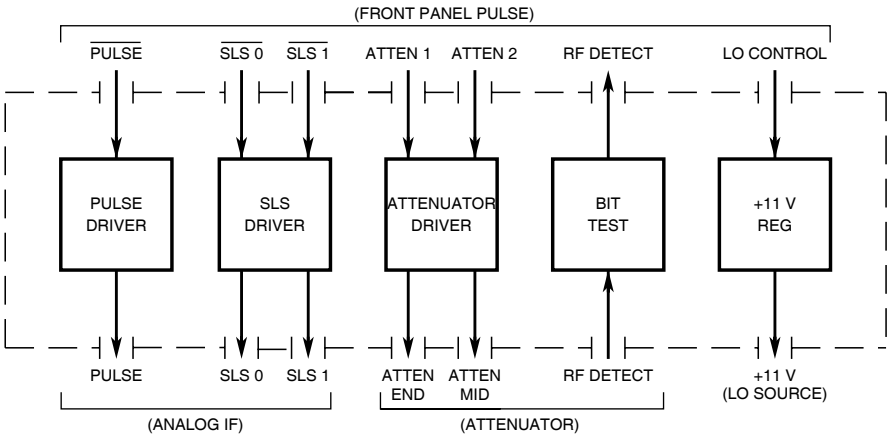
The single-sideband mixer splits the transmit (30 MHz IF), receive (1030 MHz) and LO source (1060 MHz) signals into two each. The resulting signals are phase shifted and summed together, canceling the image sideband (lower sideband on transmit, upper sideband on receive). The LO source signal is split by quadrature microstrip HY18003. One signal at 0° is fed into High-Level Mixer MXR18002 and the other signal at 90° is fed into High-Level Mixer MXR18001. C18034 (1030 MHz NULL PHASE ADJ) sets phase of LO source signal input to MXR18001 for complete sideband cancellation.

On receive, the 1030 MHz signal from the Attenuator PCB Assy is split through Power Splitter HY18002. One signal is fed into MXR18002. MXR18002 mixes the 1030 MHz with the 1060 MHz (both in phase) for an output of 30 MHz. (2090 MHz is out of bandwidth.) The second signal is fed into MXR18001. MXR18001 mixes the 1030 MHz at 0° with the 1060 MHz at 90° for an output of 30 MHz at 90°. T18002 changes phase 180° for an output of 30 MHz at -90°. Signals are sent through the respective all-pass filters and are added together through T18001. Adding the 90° separation factor sets the 30 MHz signal from MXR18001 back to 0°.

On transmit, the 30 MHz signal from the Analog IF PCB Assy is split by T18001, C18017 and R18014. The two signals, 90° apart, go through all-pass filters tuned to maintain equal levels (R18013 and R21015, 1030 MHz NULL AMPLITUDE ADJ) and 90° separation (C18013 and C18015, 1030 MHz NULL PHASE ADJ). One signal (in phase) is fed into MXR18002. MXR18002 mixes the 30 MHz with the 1060 MHz for a mixed output of 1030 MHz and 1090 MHz. The second signal (90° out of phase) is shifted another 180° by T18002 and is fed into MXR18001. MXR18001 mixes the 30 MHz at -90° with the 1060 MHz at 90° for an output of 1030 MHz at 180° and 1090 MHz at 0°. The signals are added together through Power Splitter HY18002. The 1030 MHz signals cancel each other leaving the 1090 MHz transmit signal.

(b) Driver PCB Assy (2-2-1, Figure 12)



Driver PCB Assy Block Diagram
Figure 12

The Driver PCB Assy drives the pulse and level control signals from the Front Panel Pulse PCB Assy to the Analog IF PCB Assy and Attenuator PCB Assy. The Driver PCB Assy also provides the +11 V for the LO Source PCB Assy, the voltage to bias pin attenuator diodes on the Video Detector PCB Assy and voltages from the Power Supply Assy to the rest of the RF Assy. The Driver PCB Assy consists of attenuator drivers, +11 V regulator, SLS level drivers, pulse modulation driver, RF BIT level driver and Direct Connect Power Adjust.

ATTEN2 line voltage from Front Panel Pulse PCB Assy (0 to 10 Vdc) across R20005 sets a voltage controlled current source supplying collector current for half of Q20001. The other half of Q20001 remains constant as determined by R20052 and R20009. Q20001 and associated components form a logarithmic converter. Q20002 and associated components form an exponential amplifier. Both amplifier circuits cascaded together form a power function converter with independent adjustments for gain (R20010, 50 dB ADJ OFFSET) and exponent (R20016, 10 dB ADJ SLOPE). R20009 (ZERO VOLT ADJ) allows independent adjustment of R20010 and R20016. Operational amplifier U20002B, set by power function converter (Q20002-1) and Q20003 feedback, biases Q20003, controlling current flow through midline attenuator diodes on the Attenuator PCB Assy. The output voltage of RT20002 and associated components provide temperature compensation for pin diode slope changes over temperature. ATTEN1 line voltage (0 to 10 Vdc from Front Panel Pulse PCB Assy) across linear converter amplifier controls the current through end line pin attenuator diodes on the Attenuator PCB Assy. Operational amplifier U20001A, set by ATTEN1 line voltage and Q20005 feedback inputs, biases Q20005, controlling current flow. R20019 (VSWR 50 dB ADJ) sets the reference current through Q20005.

Voltage regulator U20008 provides the +11 V to operate the Multiplier and VCO on the LO Source PCB Assy. U20008 is switched On or Off by the LED Control Register on the Front Panel PCB Assy.

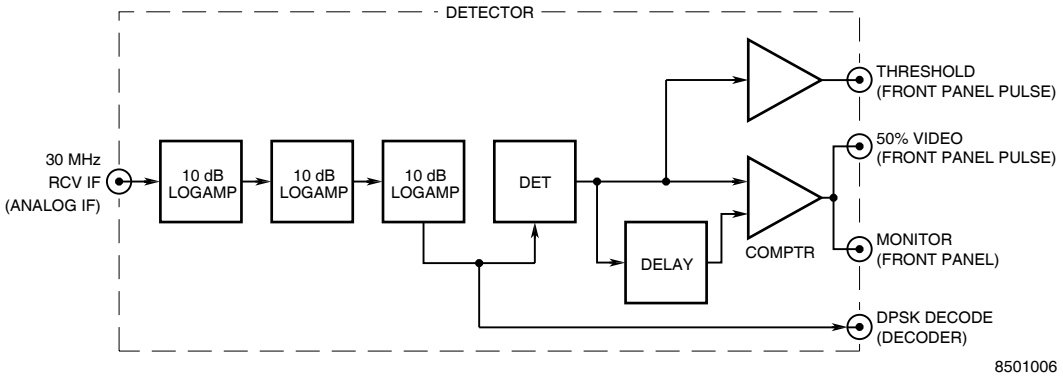
SLS level drivers U20005B and U20005C invert the active low $\overline{\text{SLS0}}$ and $\overline{\text{SLS1}}$ signals from the Front Panel Pulse PCB Assy. The high output signals, SLS0 and SLS1, bias the SLS gain amplifier output level diodes. $\overline{\text{SLS0}}$ and $\overline{\text{SLS1}}$ are both activated during normal operation.

The pulse modulation driver converts the reply pulse signal from the Front Panel Pulse PCB Assy to the level necessary to modulate the 30 MHz IF on the Analog IF PCB Assy. Active low $\overline{\text{PULSE}}$ is inverted by U20006C and driven to Analog IF PCB Assy as active high PULSE.

The RF BIT level driver biases Diode Detector CR31001 on the Attenuator PCB Assy. Transmit level detected across CR31001 is used in setting the RF DETECT line during the RF Detect portion of Self Test. U20007 output is 0 Vdc when nothing is detected to 2.8 Vdc when transmit level is highest (no attenuation). CR20001 matches U20007-3 input and R20029 (ZERO ADJ) adjusts bias to set U20007 output to 0 Vdc when nothing is transmitted (U20007-3 input ≈-0.3 Vdc). R20032 (RF DET ADJ) sets output voltage to correct level when Test Set is transmitting.

R20020 (DIRECT CONNECT POWER ADJ) adjusts the voltage from 0 to +12 Vdc to bias the pin attenuator diode on the Video Detector PCB Assy. R20020 calibrates the signal level at the RF I/O Connector (J10058) to -48.25 dB relative to the signal level at the ANTENNA Connector (J10057).

(c) Detector Assy (2-2-1, Figure 13)



Detector Assy Block Diagram
Figure 13

The Detector Assy converts the 30 MHz, pulse modulated input from the Analog IF PCB Assy to TTL level, preserving original pulse width. The TTL level signal is sent with a threshold comparison signal to the Interrogation Decoder on the Front Panel Pulse PCB Assy for decoding. The output signal is monitored through the MONITOR Connector (J10056) on the Front Panel Assy. The Detector Assy also provides the DPSK modulated signal to the Decoder Assy. The Detector Assy has a detection range of ≈30 dB (-27 to +3 dBm). Detector Assy circuits (Logarithmic Amplifiers, Detector and Comparators) are located on the Detector PCB Assy.

1 Logarithmic Amplifiers

The Detector PCB Assy has three stages of cascade coupled Logarithmic Amplifiers (Q21001, Q21002, Q21003 and associated components) providing a total gain of ≈30 dB. Each amplifier has ≈10 dB gain, calculated by the collector impedance (set by resistors R21004, R21011 and R21018) divided by the emitter impedance. The current through emitter logging diodes (CR21001, CR2002 and CR21003) shunts the emitter resistance, effectively causing the small emitter impedance to change with the input level. With low input levels, emitter impedance is low and gain is high. As input level increases, emitter impedance increases logarithmically and gain decreases, approaching unity gain until compression is reached.

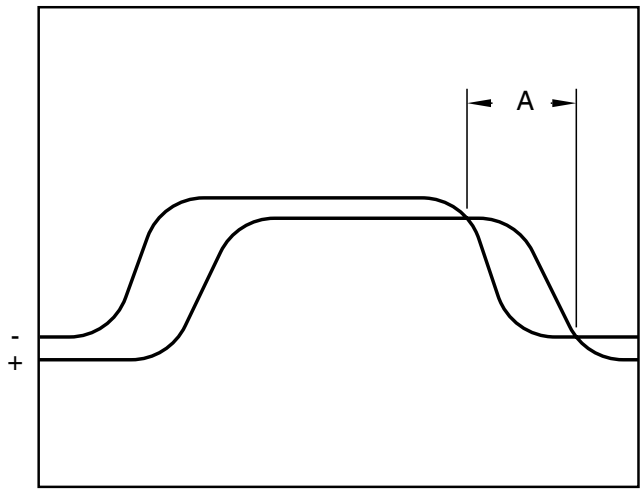
After amplification, the signal is split. Q21007 buffers one signal through J32067 to the Decoder Assy for DPSK decoding. The other signal is sent to the Detector.

2 Detector

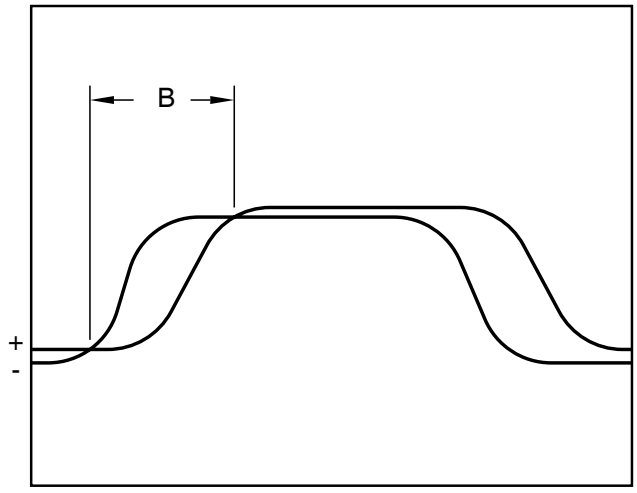
The balanced Detector preserves envelope detection efficiency and consists of an unbalanced to balanced Transformer T21001, Diode CR21004, dual transistor buffer (Q21005 and Q21008) and detector filter (C21018, L21006, C21019, C21020, L21007, C21021, C21022 and R21039). CR21004 balances the output of T21001 and provides a 60 MHz positive half-wave, the width of the modulating pulse, to the dual transistor buffer. The detector filter has a 6.5 MHz bandwidth and a flat time delay response to preserve pulse shape. The detector filter removes the 60 MHz from the detected pulse.

3 Comparator

After detection, the signal is split into two paths: primary and delayed. Buffers Q21008 and Q21009, provide the load for the detector filter. The delayed signal at Q21009 emitter is set through the delay filter (C21024, L21008, C21025, C21026, L21009, C21027, L21010 and C21028). The delay filter has a bandwidth of ≈10 MHz and a flat time delay of 120 ns. The delayed signal is referenced using a resistor network (R21060 and R21046) and applied to the positive inputs to Comparators U21001A, U21001B and U21004A. The primary signal is split. One primary signal is dc adjusted by R21061 to provide a higher level than the delayed signal and is applied to the negative input to trailing edge Comparator U21001A. Refer to 2-2-1, Figure 14 for trailing edge comparator input signals. The other primary signal, applied to the negative input to leading edge Comparator U21001B, is set lower than the delayed signal. Refer to 2-2-1, Figure 15 for leading edge comparator input signals. When preserving correct pulse width, slicing occurs at the 50% amplitude points for a linear pulse. Offsetting input signals cause the comparators to slice the pulse 6 dB down (≈-0.15 V), compensating for the level set by the Logarithmic Amplifiers. Comparator outputs provide the clocks for D Flip-Flops U21002A and U21002B. The pulses, shown in 2-2-1, Figure 16; have widths (A and B) approximately equal to the filter delay and are spaced (C) (rising edge to rising edge) about equal to the input pulse width minus the filter delay.



Trailing Edge Comparator Input Signals
Figure 14



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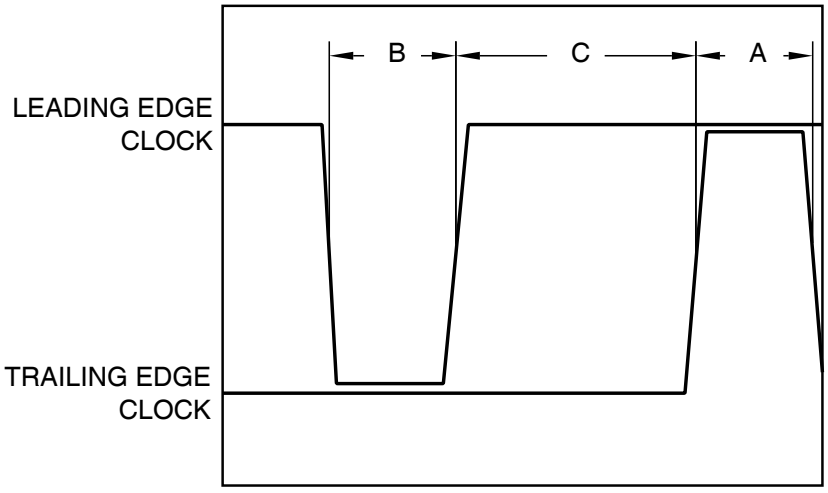
Leading Edge Comparator Input Signals
Figure 15



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Detector Comparator Pulses
Figure 16

U21002A, triggered by the leading edge clock, has a negative pulse output to NAND Gate U21003A. U21002B, triggered by the trailing edge clock, resets U21002A, through U21003B and U21003C. U21002A $\overline{Q}$ output is the other input to NAND Gate U21003A. R21058 (PULSE WIDTH) and C21035 provide a timed delay in triggering One-shot U21003D, to reset U21002B. The timed delay provides compensation for the filter delay, offset between flip-flops and comparator delays. The original pulse shape is restored at the output of U21003A. Reset Comparator U21004A and associated circuitry reset U21002A at low signal levels when there is a high output (U21003A-3) with a low input (U21004A-4). The Detector Assy output is sent to the Interrogation Decoder on the Front Panel Pulse PCB Assy and MONITOR Connector (J10056) on the Front Panel Assy, balanced by R21056 and R21057 for 50 Ω impedance matching.

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NOTE: The leading edge comparator is set to be more sensitive than the trailing edge comparator to eliminate flip-flop reset during DPSK transitions.

The threshold comparator, U21004B, compares the incoming pulse level with the threshold level. The threshold level set by R21048 (THRESHOLD) simulates minimum triggering level (MTL). When the simulated range attenuates the incoming signal to a level less than the threshold level, U21004B output stays low. The TCAS-201-2 does not reply because the interrogation level is below MTL. R21049, R21063 and RT21001 compensate for changes in output from the Logarithmic Amplifiers due to temperature. CR21006, C21041 and R21064 stretch pulses to prevent chopping off valid, received pulse signal.

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(d) Analog IF Assy (2-2-1, Figure 17)

The Analog IF Assy provides the 10 MHz reference used by the LO Source PCB Assy, 60 MHz clock for the Digital IF PCB Assy, pulse modulation for transmit signal and temperature compensation. The Analog IF Assy circuits, contained on the Analog IF PCB Assy are: 10 MHz DCXO, Transmit and Receive.

1 10 MHz DCXO

The Digitally Controlled Crystal Oscillator (DCXO) provides a temperature compensated 10 MHz signal. The oscillator temperature is transmitted as a voltage to the ADC (Front Panel Pulse PCB Assy) by temperature sensor (CR22001). R22001 calibrates CR22001 output voltage. The Front Panel Pulse PCB Assy uses the temperature sensor voltage to set contrast on the DISPLAY and provide the correct voltage to drive the DCXO for an output of 10 MHz (±30 Hz) across the temperature range (-20° to +50°). The corrected voltage (+2 to +8 Vdc) across CR22002 drives the oscillator (Y22001, Q22001 and associated circuitry). C22004 adjusts frequency. At 27°C, R22001 is adjusted to provide +3 Vdc (FL19007) and C22004 is adjusted for 10 MHz (±3 Hz). After amplification by Q22002, the 10 MHz signal is split. One signal is buffered by Q22003 for 1 Vp-p output to the LO Source PCB Assy. The other signal is buffered by Q22004 in the Transmit section.

2 Transmit

The 10 MHz signal from the DCXO passes through low-pass filter (C2201-28, L22002 and C22019) to X6 Multiplier Transistor Q22005. The 60 MHz bandpass filter (L22003, L22005, L22007 and associated components tuned to the sixth harmonic) provides 60 MHz with a 3 MHz bandwidth. After amplification by Q22006, the 60 MHz signal is split. One signal is buffered by Q22007 for 1 Vp-p clock output to the Digital IF PCB Assy. The other signal clocks D Flip-Flop U22001B. U22001B, pins 8 and 12 are connected together to divide the signal by two for a 30 MHz output. The active low pulse signal from the Front Panel Pulse PCB Assy pulse modulates the signal through U22001B-10.

Resistors R22040 and R220041 reduce amplitude by 10 dB (checked at TP22003). The transmit bandpass filter is a four pole Bessel wideband filter consisting of four series resonators (C22036-L22010, C22038-L22011, C22040-L22012 and C22042-L22012). The transmit filter is centered at 30 MHz with a 3 dB bandwidth across 12.6 MHz. Signal delay, from U22001B through the transmit filter, shapes the transmit pulse by providing ≈70 ns of rise time.

The transmit signal flows through Mixer MXR22001 with no change. (DPSK modulation is not applied.) SLS Gain Amplifier Q22008 provides full amplification, controlled by diodes CR22007, CR22013, CR22006 and CR22012. SLS0 and SLS1 lines are both high during normal operation.

R22049 (TX GAIN) adjusts output level of Amplifier Q22009. Q22009 provides ≈10 dB signal gain. Inductive coupler L22020 decreases current and increases voltage. Q22010 is the final output amplifier, increasing the 30 MHz signal approximately another 10 dB. Q22010 emitter circuitry (RT22001, R22055 and R22056) provides temperature compensation for all of the transmit circuits. L22027 provides 40 dB isolation between transmit and receive. C22055 and R22062 (ISOLATION) are adjusted for maximum isolation.

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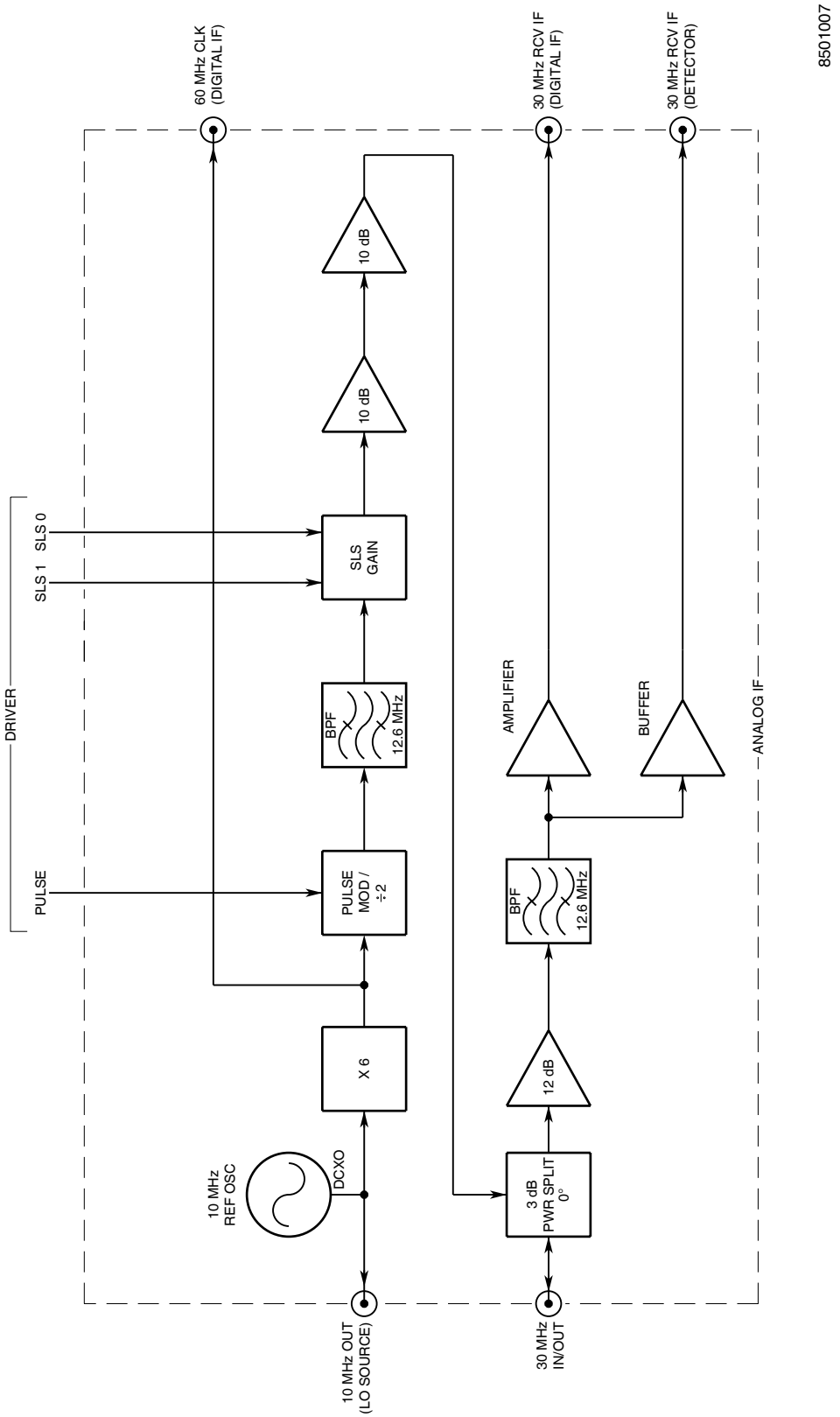

Analog IF Assy Block Diagram
Figure 17

3 Receive

The receive signal, 30 MHz IF from the Mixer PCB Assy, is reduced 3 dB by L22027 and applied to Amplifier Q22011. Q22011 amplifies signal 12 dB and provides a 50 Ω output to drive the receive filter. The receive bandpass filter is a four pole Bessel wideband filter comprising series resonators L22029-C22060, L22030-C22062, L22031-C22064 and L22032-C22066. The receive filter has a flat time domain response between the 3 dB points and is centered at 30 MHz with a 12.6 MHz bandwidth. Output is split into two signals. Q22013 buffers and sends one signal to the Detector PCB Assy through J19033. Emitter-follower Q22012 amplifies the other signal. R22073 (RX GAIN) adjusts received level. Q22014, with a 50 Ω output, drives the 30 MHz receive signal to the Digital IF PCB Assy through J17034 (≈+3 dBm). Q22014 emitter circuitry (RT22002, R22082 and R22084) provides temperature compensation for all of the receive circuits.

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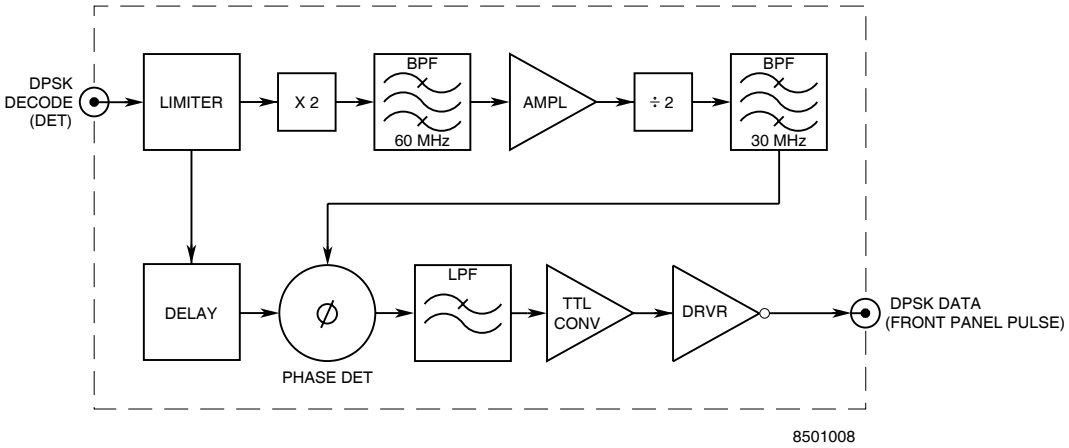
(e) Decoder Assy (2-2-1, Figure 18)



Decoder Assy Block Diagram
Figure 18

The Decoder Assy converts the DPSK modulated incoming interrogation signal to a digital output used by the Interrogation Decoder on the Front Panel Pulse PCB Assy.

The limiter (Q36001 and associated components) squares the amplified 30 MHz receive signal from the Detector Assy. Limiting occurs at the level set by feedback through R36006. Feedback also increases bandwidth. The signal is buffered by Q36002 and split in two.

One signal, the control signal, is sent to both inputs of Doubler (X2) MXR36001. When phase shifts occur, MXR36001 provides a 60 MHz output shifted 360°, keeping the phase constant. The bandpass filter (L36002, C36010, L36004, C36009, C36008, L36003, C36007, R36016 and C36011) removes energy from phase shift transitions (≈20 MHz), 30 MHz carrier bleed through and other unwanted harmonics from the control signal. L36003 and L36004 are adjusted for 60 MHz at TP36001.

Two stage amplifier-limiter composed of Q36005, Q36006 and associated components boost the control signal to drive Flip-Flop U36001A. CR36001 limits the signal to the +5 V source from the Power Supply Assy. U36001A divides the signal by two to get 30 MHz again. L36010, C36024 and R36023 filter out unwanted harmonics. R36034 sets level for Phase Detector MXR36002 input.

The other signal, the DPSK signal off of Q36002 emitter, is buffered by Q36003. L36001, C36004, R36011 and associated components form a variable phase shift delay, adjusted to keep DPSK signal phase synchronized to 0° or 180° from control signal. C36004 is adjusted for maximum output through Buffer Q36004 to Phase Detector MXR36002.

Phase Detector MXR36002 provides a positive output when both signals are in phase and a negative output when the DPSK signal is 180° from the control signal.

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A low-pass filter (C36015, L36005, C36016, L36006 and C36017) removes 30 MHz, 60 MHz and all harmonics. The remaining dc signal is applied to TTL Converter U36002A. U36002A is a comparator with hysteresis providing a stable digital representation (TTL level) of the DPSK modulation status. NAND Gate U36003A inverts and drives digital DPSK data to Front Panel Pulse PCB Assy.

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(5) Front Panel Assy

(a) Video Detector PCB Assy

The Video Detector PCB Assy provides a linear display of UUT interrogations on the oscilloscope when Test Set is directly connected to UUT. The Video Detector PCB Assy also provides a calibrated attenuation of the direct connection signal.

The direct connection receive signal from the Power Termination Assy or transmit signal from the Attenuator PCB Assy is split by a resistive power splitter (R30010, R30002 and R30003). One signal is linearly detected by Schottky Barrier Diode CR30001. C30003 is a printed element to provide for fast detection. The detected signal is sent to the INTERR VIDEO Connector (J10054). On receive, the other signal has attenuation level set across a resistive divider (R30011 and R30012). Current through CR30002, controlled by the biasing voltage set on the Driver PCB Assy, provides ≈1 dB of attenuation adjustment. Attenuation level is calibrated for accurate power and MTL measurements. On transmit, the other signal is attenuated before splitting and going to the Power Termination Assy.

(b) Power Termination Assy

The Power Termination Assy provides a 50 W termination for the UUT and protects the TCAS-201-2 Test Set against excessive incoming power through the RF I/O Connector (J10058). The Power Termination Assy is in the transmit and receive circuit only when a direct connection with UUT is used. The Power Termination Assy connects the RF I/O Connector (J10058) through P/J28028 with the Video Detector PCB Assy through P/J28029.

Transmit and Receive signals are reduced 20 dB across Directional Coupler HY28001. Excessive incoming power and stray spikes are dissipated off through R28002. C22001 and L22001 keep the circuit frequency balanced for 50 Ω impedance.

(c) Front Panel LED PCB Assy

The Front Panel LED PCB Assy consists of three indicator circuits and a light sensor used in the LCD Backlight Control circuit.

The INTERR Indicator illuminates red when a valid interrogation is received. When activated, a ground on the emitter of Q27007 (Front Panel Pulse PCB Assy) completes the circuit across LED CR13001.

The REPLY Indicator illuminates red when a reply is transmitted. When activated, a ground on the emitter of Q27006 (Front Panel Pulse PCB Assy) completes the circuit across LED CR13002.

The CHARGE Indicator illuminates only when the Battery Charger on the Power Supply Assy is operating. The CHARGE Indicator illuminates green (battery is >80% charged) when current flows from the 15 V source through LED CR13003 to the Power Supply Assy (BATT CHARGER LED line). The circuit is completed through CR27010 and the activated transistors, Q27013 and Q14014. The CHARGE Indicator illuminates red (battery requires charging) when current flows from the Battery Charger on the Power Supply Assy through CR27011 and the activated Q27015 to LED CR13003.

Voltage across light sensitive Photo Resistor R13001 is sent to the ADC on the Front Panel Pulse PCB Assy. The Front Panel Backlighting voltage to the LCD is adjusted accordingly.

(d) LCD (LCD Display PCB Assy [Modified])

The LCD is a 64 line by 240 column dot display. The LCD requires 4.75 to 5.25 V to run logic. The TCAS-201-2 uses a nominal +5 V. The LCD drive voltage required is -5.25 to -4.75 V. -5.1 V is nominal for TCAS-201-2.

(e) Keypad

The Keypad, consisting of 12 keys, is contained in the TCAS-201-2 Overlay. When activated, each key momentarily closes contacts between a row ($\overline{\text{ROW}}$) line and column ($\overline{\text{COL}}$) line. Row and column lines go to the Front Panel Pulse PCB Assy. Keys operate with <20 ms switch bounce.

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