AC–DC Transfer Standard Measurements and Generalized Compensation With the AC Josephson Voltage Standard

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***Abstract*—We present ac–dc transfer standard measurements using the National Institute of Standards and Technology's pulse-driven ac Josephson voltage standard source. We have investigated the frequency dependence for several output voltages up to 200 mV for frequencies from 2.5 to 100 kHz. We found that, as the frequency increases, the ac–dc differences for the two arrays on the same chip do not agree. We explored this deviation in ac–dc difference for the two arrays by investigating different configurations of the probe cabling and wiring, chip carriers, and on-chip circuit design. We found that the circuit design produced the greatest improvement, particularly at the highest frequency (100 kHz), where the deviation in ac–dc difference was reduced by more than 60%. In this paper, we also demonstrate tenfold higher output voltages and improved operating margins for arbitrary (nonsinusoidal) waveforms. These enhancements were accomplished by implementing a more general current bias to the arrays having the same harmonic content as that of the synthesized arbitrary waveform.**

***Index Terms*—Digital–analog conversion, Josephson arrays, quantization, signal synthesis, standards, superconductor-normal-superconductor (SNS) devices, voltage measurement.**

I. Introduction

FROM THE first conception of a pulse-driven ac Josephson voltage standard (ACJVS) in 1996 [1], there have been continuous developments for more than ten years at the National Institute of Standards and Technology to increase the performance of this system [2]–[10]. The first metrologically useful systems were implemented in 2006 and included the successful demonstration of a 100 mV rms ACJVS system [7], [8]. Other research toward pulse-driven ac synthesis, which focused on different junction technologies and unique circuit designs, was completed by a European Union-funded collaboration [11] and other National Metrology Institutes [12]–[14]. Although much progress has been made toward increasing the output voltage and making precision quantum-based ac voltages, many improvements are still needed, such as in increasing the practical output voltage above 200 mV rms, extending the useful measurement bandwidth above 100 kHz, and evaluating and removing various sources of systematic measurement errors. In this paper, we focus on evaluating the major systematic error sources at frequencies above 10 kHz, as well as on increasing the output voltage of arbitrary voltage waveforms.

The ac–dc transfer standard measurements presented in [8], [9], and [15] showed the advantage of using the ACJVS voltage source for precision ac voltage measurements. Those circuits, as well as the ones measured in this paper, have two identical Josephson arrays ("left" and "right") that are connected in series and can be independently biased to produce half the total voltage. Those prior measurements illuminated significant challenges when measuring the ACJVS with such rms detectors. In the most recent papers [8], [9], voltages from 2 mV up to 100 mV rms were investigated in the frequency range from 2.5 kHz to 50 kHz. As the frequency increased, an increasing disagreement was found between the measured ac–dc difference for the two arrays on the same chip. We expect the left–right array disagreement to be caused by error voltages produced by inductance in the circuits or input–output coupling from bias signals [15]. As described in this paper, we have attempted to determine the source of these errors by experimentally investigating different ACJVS chips and transmission-line circuits that were found to improve the agreement in ac–dc difference between the left and right arrays.

We also describe an important improvement in the generation of arbitrary waveforms that are more complicated than sine waves. Until now, the compensation bias to the arrays [15]–[17] was performed with only a sine wave or, at most, a pair of sine waves. Compensation by a generalized (more complicated) waveform was not previously implemented. Typically, these more complex waveforms were synthesized with relatively low voltages (less than 30% maximum voltage), because such low voltages did not require compensation bias [9]. Furthermore, for complicated waveforms such as the two-tone and the 10 dB step-function, which used two sine-wave compensation biases, only one array could be operated at a time [9]. This paper describes the development of a simple software routine to extract the relevant audio-frequency signals from the digital

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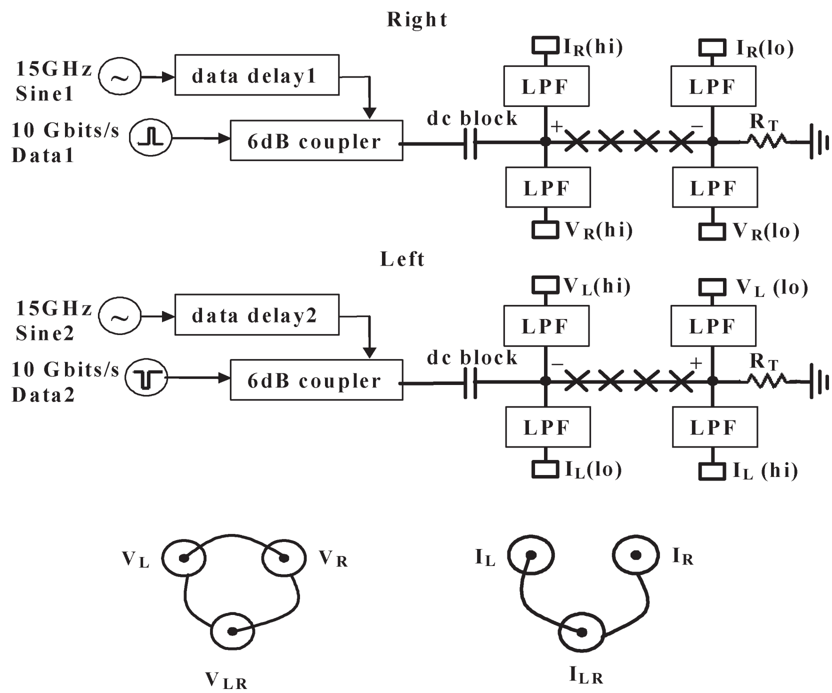

Fig. 1. Circuit design showing the most recent wiring configuration of the ACJVS (short-top).

codes used for the pattern-generator output, so the appropriate compensation-bias signals can be applied to the arrays with arbitrary function generators in the same fashion as is currently done for sine-wave synthesis. Consequently, both arrays can be operated simultaneously, and arbitrary waveforms can be synthesized with peak voltages up to 280 mV.

II. Probe Circuit

Fig. 1 shows the most recent wiring configuration of the ACJVS. We will call this the "short-top" wiring configuration, because the arrays are connected at room temperature in the top of the cryoprobe head. We use the following notations: $V =$ voltage; $I =$ current; $R =$ right array; $L =$ left array; $LR =$ both arrays in series; hi = high; and lo = low/ground. The "short-top" wiring-configuration details are as follows (see Fig. 1):

1) There are twisted-pair magnet wire for current and voltage leads.
2) The right and left arrays are connected in series by connecting the voltage leads V_R and V_L at the BNC connectors in the room-temperature probe head at the "top" of the cryoprobe. Fig. 1 shows the BNC connections (center dot = hi, circle = lo) for the output voltages and the current biases.
3) This configuration allows independent and simultaneous measurement of all output voltages, including both individual arrays and their series-combined voltage V_{LR}.

   In contrast, we tested two other wiring configurations (not shown schematically) that are quite similar to the "short-top" one. Referring to Fig. 1, the differences are as follows:
4) "short-lo" wiring:
   a) nontwisted-pair cables;
   b) V_R(lo) and V_L(lo) are directly connected on the chip carrier with a superconductive wire;
   c) V_R(hi) and V_L(hi) are connected on the chip carrier to the V_{LR}(hi) and V_{LR}(lo) leads, respectively;
   d) I_R(lo) is closer to the dc block than I_R(hi) (opposite to that indicated in Fig. 1);
   e) I_R(lo) and I_L(lo) are connected on the chip carrier to the I_{LR}(hi) and I_{LR}(lo) leads, respectively;
   f) this configuration allows measurement of only the voltage sum of the two arrays (V_{LR}); however, it is possible to measure each array individually while the other array is unbiased, provided that the total bias current remains below the critical current of the array.
5) "short-hi" wiring:
   a) V_R(hi) and V_L(hi) are directly connected on the chip carrier with a superconductive wire;
   b) V_R(lo) and V_L(lo) are connected on the chip carrier to the V_{LR}(hi) and V_{LR}(lo) leads, respectively;
   c) I_R(lo) and I_L(hi) are connected on the chip carrier to the I_{LR}(hi) and I_{LR}(lo) leads, respectively;
   d) as in the "short-lo" configuration, this allows measurement of the voltage sum V_{LR} of the two arrays (left and right arrays), and the measurement of an individual array output voltage only when the other array is unbiased.

The dc blocks shown in Fig. 1 have a pass band of 10 MHz to 18 GHz and are responsible for attenuating the audio-frequency signals with the expectation that they effectively remove the low-frequency common mode voltage on the termination resistor (R_{T}). However, the low-frequency part of the original digital-code signal is necessary to properly bias the arrays [16]. These low-frequency signals are then separately reapplied to each array as "current compensation" through the I_R and I_L

TABLE I
AC–DC DIFFERENCE FOR 200 mV RMS VOLTAGE VERSUS FREQUENCY ON THE 220 mV FLUKE 792A INPUT RANGE

f (kHz)	ac-dc difference (µV/V)
2.5	7
5	16
10	-7
20	32
50	18
100	90

connections. Because these currents do not flow through R_T, they do not produce a low-frequency common mode signal.

The measurements described in this paper were performed with double-stacked superconductor–normal-conductor–superconductor Josephson junction arrays with Nb/a-$\mathrm{Nb_xSi_{1-x}}$/Nb multilayers that are described in [10]. Two different superconducting integrated-circuit designs were used: one with a maximum ac output voltage of 100 mV rms and the other with 200 mV rms output. The larger voltage is made possible by use of twice as many junctions (2560 junctions per array) and tapered transmission lines [10].

III. AC–DC TRANSFER STANDARD MEASUREMENTS

Due to the new chip design [10], ac–dc transfer standard measurements for 200 mV rms output voltage are possible for the first time and are presented in this paper. Our 200 mV measurements were performed in a manner similar to those done with 100 mV circuits [8]. Each ac–dc difference measurement is the average of eight consecutive difference measurements of the triple-voltage sequence: $V_{+\mathrm{dc}}$, V_{ac}, and $V_{-\mathrm{dc}}$. A 10 s delay is programmed between each voltage measurement to ensure that all biases have switched and that the transfer standard has stabilized. For each of the 24 voltage measurements, the output of the transfer standard is averaged over 20 power-line cycles by use of a nanovoltmeter. The measurement sequence for an ac–dc difference at a single frequency is completed in 5–6 min. Table I shows the ac–dc difference for 200 mV as a function of frequency on the 220 mV input range of a Fluke 792A transfer standard.[1] The ac–dc difference values are comparable to the 100 mV measurement results published in [7] and [8]. Similar to [7] and [8], the frequency-dependent difference has a minimum at 10 kHz and increases for higher frequencies.

In order to investigate in detail the frequency dependence of the ACJVS for ac–dc transfer standard measurements, we performed measurements using different chip designs (100 or 200 mV [7]), different chip carriers (flex bonded or spring finger contacts [6]), and different wiring configurations ("short-lo," "short-hi," or "short-top"). We also checked the performance of flex-bonded carriers for the new 200 mV and for the 100 mV chips.

[1]The commercial instruments are identified in this paper only in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment identified is necessarily the best available for the purpose.

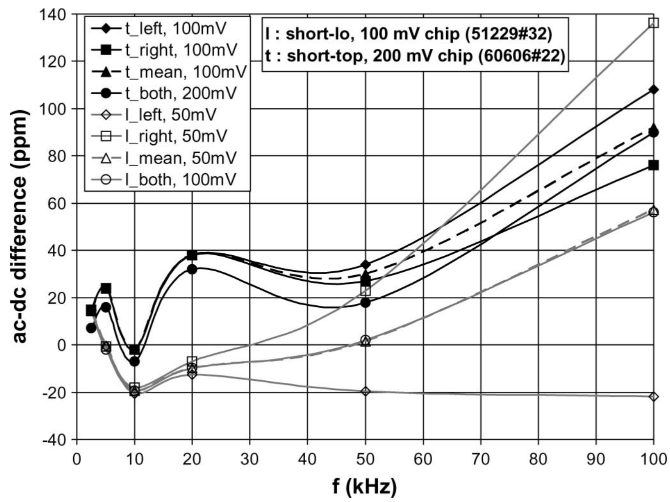

Fig. 2. Comparison of ac–dc difference versus frequency response for "short-top" (t) configuration at 100 and 200 mV and "short-lo" (l) at 50 and 100 mV.

In Fig. 2, we compare the ac–dc difference versus frequency response of [7], when "short-lo" wiring for a 100 mV chip was used, with the response for the 200 mV chip in the "short-top" wiring configuration. For the "short-top" configuration, we observe significantly closer agreement between the ac–dc differences of the left and right arrays for all frequencies, particularly at 100 kHz. Possible reasons for the clear difference between these configurations are investigated in more detail as follows (cf. Table II). In Fig. 2, we also show the mean value of the ac–dc difference of the left and right arrays, which is in good agreement with the ac–dc difference at twice the voltage for both arrays operating together. The lines between the dots are merely a guide for the eyes. Note that we do not expect the 50, 100, and 200 mV ac–dc differences to be the same, because there is some amplitude dependence to the ac–dc difference values of the 792A.

Fig. 3 shows the difference between left and right array ac–dc differences versus frequency from the data of Fig. 2. This difference was calculated by subtracting the left-array ac–dc difference from that for the right array. For the 100 mV chip with the "short-lo" wiring, this difference is about 160 μV/V at 100 kHz. On the other hand, the left–right array difference (L–R difference) of only 32 μV/V at 100 kHz for the 200 mV circuit with "short-top" wiring is smaller by 80% than that for the "short-lo" configuration.

Since the Josephson arrays are known to be on "operating margins" and are therefore generating error-free perfectly quantized waveforms, any frequency-dependent differences between the left and right array voltages are probably caused by frequency-dependent errors that most likely occur at the synthesis frequency, such as input–output coupling and unblocked signals from the dc blocks [7], [8], [15]. In order to determine the source of the improvements in the most recent measurement and to shed light on the most likely cause of the measurement errors, we measured the ac–dc difference at 100 kHz for many different circuit configurations and chips. The results are presented in Table II. Each row of this table is an average of several ac–dc difference measurements. One

TABLE II
L–R DIFFERENCE FOR AC–DC MEASUREMENTS USING DIFFERENT CHIPS, CABLES, AND WIRING AT 100-kHz FREQUENCY

Array RMS Voltage (mV)	Wafer#chip	Design	Probe Cables	Wiring	Chip Carrier	L-R Difference (μV/V)
50	51229#32	18I	non twisted pair	short-lo	Spring fingers	**160**
50	51229#33	18H1	non twisted pair	short-lo	Flex bonded	**150**
50	51229#35	18H1	twisted pair	short-top	Spring fingers	**146**
50	51229#53	18H1	twisted pair	short-top	Spring fingers	**145**
50	51229#33	18H1	non twisted pair	short-hi	Flex bonded	**140**
50	51229#33	18H1	twisted pair	short-top	Flex bonded	**131**
50	51229#25	18I	twisted pair	short-top	Spring fingers	**131**
50	51229#33	18H1	twisted pair	short-hi	Flex bonded	**123**
50	51229#24	18H1	twisted pair	short-top	Spring fingers	**112**
100	60606#43	20B	twisted pair	short-top	Spring fingers	**64**
100	60606#55	20B	twisted pair	short-top	Spring fingers	**57**
100	60606#22	20B	twisted pair	short-top	Flex bonded	**37**
100	60606#22	20B	twisted pair	short-top	Spring fingers	**32**
100	60606#35	20B	twisted pair	short-top	Flex bonded	**31**

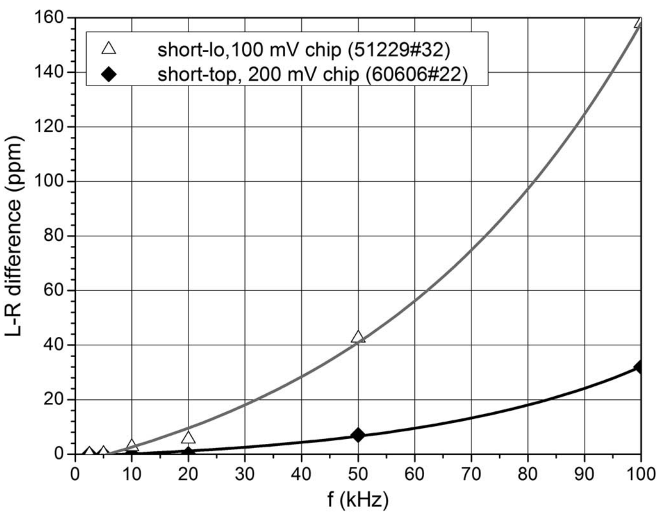

Fig. 3. L–R difference versus frequency for the "short-lo" configuration at 50 mV per single array and the "short-top" configuration at 100 mV.

possible error source is crosstalk between the compensation-current input and the voltage-output leads. Any systematic error from the input–output coupling should be reduced in the "short-top" wiring configuration, because twisted-pair cables were used, and they should reduce crosstalk at higher frequencies. Unfortunately, measurements with twisted-pair leads appear to produce only a small improvement in the data in Table II. Similarly, the type of chip carrier (flex bonded or spring fingers) appears to have no significant influence on the L–R difference.

The average values of the L–R difference from the original data used to make Table II are (134 ± 1) μV/V for the 100 mV chips and (49 ± 2) μV/V for the 200 mV chips, which is much smaller (taking into account only the type-A uncertainty). Either the wafer run or the chip design appears to be the most important factors for determining the L–R ac–dc difference. More wafer runs with different chip designs must be measured to further investigate this effect and determine the error source.

For completeness, we note a few additional measurement details that we took into consideration. First, a 3 MHz filter is required at the ACJVS output to remove digitization harmonics (above 10 MHz) from the measured rms voltage. The large filter capacitance produces a frequency-dependent voltage. Thus, we tune the transfer function of the output transmission line and filter to ensure a flat frequency response of the output voltage between 2.5 kHZ and 100 kHz. A resistance of about 60 Ω correctly tunes the transfer function. This method of calibration is described in detail in [8]. We also note that the drift of the device-under-test (Fluke 792A) output versus time and temperature should have no influence on the measured ac–dc difference, because this drift is expected to be the same for both ac and dc voltages.

IV. GENERALIZED WAVEFORM COMPENSATION

In order to provide arbitrary waveform-compensation current to the arrays, we used an Agilent 33250A Arbitrary Waveform Generator (AWG). Arbitrary waveforms with up to 64 000 points with a resolution of 12 b can be loaded directly into the memory of this instrument. For optimum ACJVS performance, the compensation waveform must be nominally identical to the analog signal that we intend to synthesize. One could reconstruct this generalized waveform from the predetermined amplitude and phase of each harmonic. However, we chose to extract the waveform from the 1 b digital waveform already created for the 10 Gb/s pattern generator. We performed a straightforward digital-to-analog conversion of the 4 Mb digital code of the pattern generator. The length of the resulting code was matched to the memory of the AWG. This way, the single-bit pattern-generator code was transformed into a multibit bipolar code with the appropriate normalized amplitude. A short program was developed to perform this conversion and to send the code to the volatile memory of the two AWGs that were used to supply the compensation bias to the two arrays.

We demonstrated the usefulness of general compensation bias by investigating several arbitrary waveforms with peak voltages up to the 300 mV maximum possible output voltage for our two-array ACJVS circuits. Fig. 4 shows a 10 dB-step waveform with 14 odd harmonic tones starting at 2.5 kHz and spaced at 5 kHz. The amplitude of each consecutive harmonic was designed to be precisely 10 dB lower than the amplitude of the previous harmonic. As a result of the general compensation, we were able, for the first time, to simultaneously operate both arrays and produce this record output voltage for

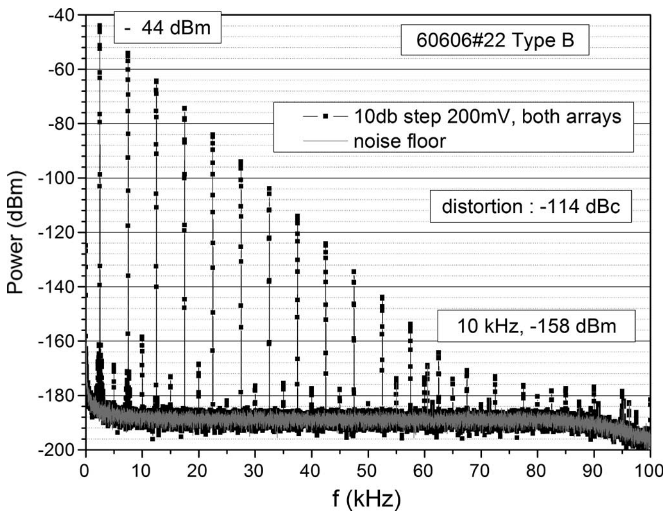

Fig. 4. Using generalized compensation bias on both arrays, a 10 dB-step waveform with 200 mV rms amplitude for the fundamental 2.5 kHz tone was realized.

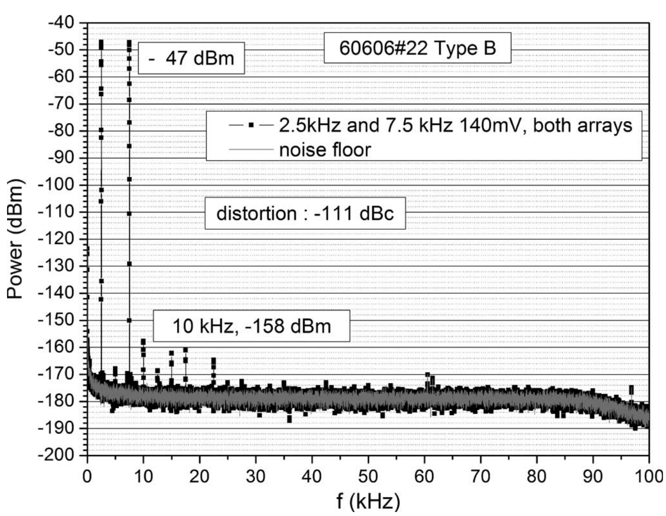

Fig. 5. Two-tone waveform synthesized with general compensation producing two 140 mV rms tones.

a precision arbitrary waveform. A maximum output voltage of 200 mV rms for the fundamental 2.5 kHz tone was generated, which is a tenfold improvement over previous measurements [9], [17]. The low distortion of -114 dBc is unprecedented and is probably a characteristic of the digitizer measurement electronics.

A two-tone waveform [7] with larger amplitude was also demonstrated. Again, for the first time, both arrays can be operated simultaneously to double the total output voltage over that which was previously demonstrated. Fig. 5 shows the measured frequency spectrum of this waveform, showing two tones at 2.5 kHz and 7.5 kHz. General compensation allows us to synthesize this two-tone waveform with 140 mV rms amplitude for each tone and produce a high-quality low distortion of -111 dBc.

We also synthesized a multitone waveform with multiple odd harmonic tones of equal amplitude up to 400 kHz [7], which is not shown here. The low 0.5 mV rms amplitude of these tones was chosen in order to achieve operating margins without compensation bias [9]. However, with general compensation, the operating-current margins for this waveform were improved by about 200 % (3 mA versus about 1 mA available current range).

V. Conclusion

The left–right array difference for ac–dc transfer standard measurements was successfully reduced by changing the chip design, the probe cables, and the wiring of the chip. For 100 mV chips, we measured an average left–right array difference of 134 μV/V at 100 kHz. Using the new 200 mV chips, we dramatically decreased the difference to 49 μV/V. However, there was still a measurable difference between the left and right arrays, indicating that further improvements are necessary, as well as further measurements and research to determine the sources of these errors.

By implementing generalized compensation biases for the ACJVS, we improved the performance of the ACJVS for complicated arbitrary waveforms, including higher amplitudes and better operating margins. The ac output voltage was doubled due to the fact that, for the first time, both arrays can be operated at the same time for these arbitrary waveforms. Most importantly, the ACJVS system can now synthesize arbitrary waveforms with amplitude up the same peak voltage that is possible for single-tone sine waves.

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