BURR - BROWN®

PCM54
PCM55

DESIGNED FOR AUDIO

ABRIDGED DATA SHEET

16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- **PARALLEL INPUT FORMAT**
- **16-BIT RESOLUTION**
- **15-BIT MONOTONICITY (typ)**
- **–92dB TOTAL HARMONIC DISTORTION (K Grade)**
- **3μs SETTLING TIME (Voltage Out)**
- **96dB DYNAMIC RANGE**
- **±3V or ±1mA AUDIO OUTPUT**
- **OPERATES ON ±5V (PCM55) to ±12V (PCM54) SUPPLIES**
- **28-PIN DIP (PCM54)**
- **24-LEAD SOIC (PCM55)**

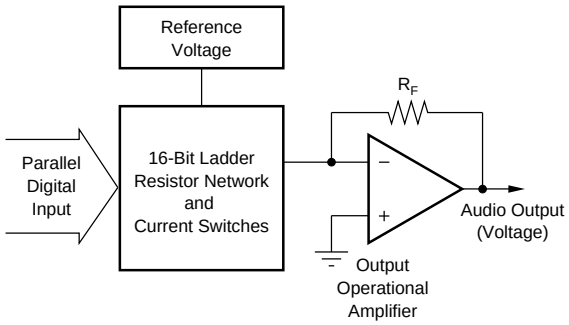
DESCRIPTION

The PCM54 and PCM55 family of converters are parallel input, fully monotonic, 16-bit digital-to-analog converters that are designed and specified for digital audio applications. These devices employ ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

These converters are completely self-contained with a stable, low noise, internal, zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V (PCM55) to ±12V (PCM54). Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero, PCM54 only) to further improve THD specifications if desired.

A current output (I_{OUT}) wiring option is provided. This output typically settles to within ±0.006% of FSR final value in 350ns (in response to a full-scale change in the digital input code).

The PCM54 is packaged in 28-pin plastic DIP package. The PCM55 is available in a 24-pin plastic miniflatpak.



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SPECIFICATIONS

ELECTRICAL

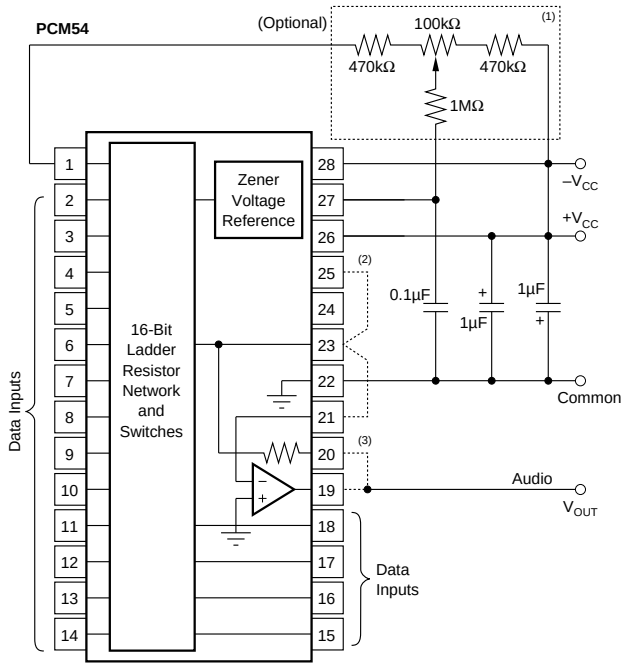
At +25°C, $\pm V_{CC}$ = 12V, unless otherwise noted.

PARAMETER	PCM54HP, PCM55HP MIN	PCM54HP, PCM55HP TYP	PCM54HP, PCM55HP MAX	PCM54JP, PCM55JP MIN	PCM54JP, PCM55JP TYP	PCM54JP, PCM55JP MAX	PCM54KP MIN	PCM54KP TYP	PCM54KP MAX	UNITS
DIGITAL INPUTS										
Resolution		16			*			*		Bits
Dynamic Range		96			*			*		dB
Logic Levels (TTL/CMOS Compatible):										
V_{IH}	+2.4		+5.25	*		*	*		*	V
V_{IL}	0		+0.8	*		*	*		*	V
I_{IH}, V_{IN} = +2.7V			+40			*			*	µA
I_{IL}, V_{IN} = +0.4V			–0.5			*			*	mA
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error		±2			*			*		%
Bipolar Zero Error		±30			*			*		mV
Differential Linearity Error at Biploar Zero[1]		±0.001			*			*		% FSR[2]
Noise (rms) (20Hz to 20kHz) at Bipolar Zero		12			*			*		µV
TOTAL HARMONIC DISTORTION[3]										
(16-Bit Resolution)										
V_O = ±FS at f = 991Hz		–94	–82		*	–88	*	*	–92	dB
V_O = –20dB at f = 991Hz		–74	–68		*	*	*	–80	–74	dB
V_O = –60dB at f = 991Hz		–34	–28		*	*	*	–40	–34	dB
MONOTONICITY		15			*			*		Bits
SETTLING TIME (to ±0.006% of FSR)										
Voltage Output: 6V Step		3			*			*		µs
1LSB Step		1			*			*		µs
Current Output (1mA Step): 10Ω to 100Ω Load		350			*			*		ns
1kΩ Load[4]		350			*			*		ns
Deglitcher Delay (THD Test)[5]		2.5	4		*	*		*	*	µs
Slew Rate		10			*			*		V/µs
WARM-UP TIME	1			*			*			Min
ANALOG OUTPUT										
Voltage Output: Bipolar Range		±3			*			*		V
Output Current	±2			*			*			mA
Output Impedance		0.1			*			*		Ω
Short-Circuit Duration		Indefinite to Common			*			*		
Current Output:[6]										
Bipolar Range (±30%)		±1			*			*		mA
Bipolar Output Impedance (±30%)		1.2			*			*		kΩ
POWER SUPPLY REQUIREMENTS										
Voltage: $+V_{CC}$ (PCM54)	+4.75	+12	+15.75	*	*	*	*	*	*	V
$-V_{CC}$ (PCM54)	–4.75	–12	–15.75	*	*	*	*	*	*	V
$+V_{CC}$ (PCM55)	+4.75	+5	+7.5	*	*	*	*	*	*	V
$-V_{CC}$ (PCM55)	–4.75	–5	–7.5	*	*	*	*	*	*	V
Supply Drain: $+V_{CC}$		+13	+20		*	*		*	*	mA
$-V_{CC}$		–16	–25		*	*		*	*	mA
TEMPERATURE RANGE										
Operating	0		+70	*		*	*		*	°C
Storage	–55		+100	*		*	*		*	°C

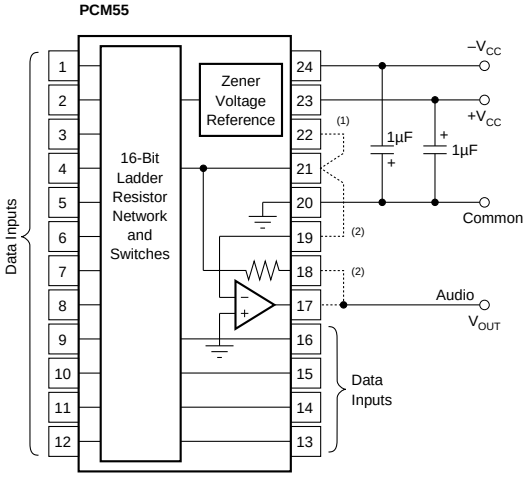
* Specifications same as for PCM54HP.

NOTES: (1) Externally adjustable. If external adjustment is not used, connect a 0.01µF capacitor to Common to reduce noise pickup. (2) FSR means Full-Scale Range and is 6V for ±3V output. (3) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. Burr-Brown may calculate THD from the measured linearity errors using equation 2 in the section on "Total Harmonic Distortion," but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) Deglitcher or sample/hold delay used in THD measurement test circuit. See Figures 2 and 3. (6) Output amplifier disconnected.

CONNECTION DIAGRAMS



NOTES: (1) MSB error (BPZ differential linearity error) can be adjusted to zero using this external circuit. (2) Connect to bipolar operation ($+V_{CC} \geq 8.5V$ for unipolar operation). (3) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 19 and pin 21, and a 1kΩ resistor between pin 21 and pin 22 to reduce possible noise effects.



NOTES: (1) Connect for bipolar operation. ($+V_{CC} \geq 8.5V$ for unipolar operation). (2) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 17 and pin 19, and a 1kΩ resistor between pin 19 and pin 20 to reduce possible noise effects.

PIN ASSIGNMENTS

PIN	PCM54-DIP	PIN	PCM54-DIP
1	Trim	15	Bit 13
2	Bit 1 (MSB)	16	Bit 14
3	Bit 2	17	Bit 15
4	NC	18	Bit 16 (LSB)
5	Bit 3	19	V_{OUT}
6	Bit 4	20	R_{FB}
7	Bit 5	21	SJ
8	Bit 6	22	Common
9	Bit 7	23	I_{OUT}
10	Bit 8	24	NC
11	Bit 9	25	I_{BPO}
12	Bit 10	26	$+V_{CC}$
13	Bit 11	27	MSB Adjust
14	Bit 12	28	$–V_{CC}$

PIN ASSIGNMENTS

PIN	PCM55-SOIC	PIN	PCM55-SOIC
1	Bit 1 (MSB)	13	Bit 13
2	Bit 2	14	Bit 14
3	Bit 3	15	Bit 15
4	Bit 4	16	Bit 16
5	Bit 5	17	V_{OUT}
6	Bit 6	18	Feedback Resistor
7	Bit 7	19	Summing Junction
8	Bit 8	20	Common
9	Bit 9	21	Current Output
10	Bit 10	22	Bipolar Offset
11	Bit 11	23	$+V_{CC}$
12	Bit 12	24	$–V_{CC}$

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM54HP	28-Pin DIP	215
PCM54JP	28-Pin DIP	215
PCM54KP	28-Pin DIP	215
PCM55HP	24-Pin SOIC	178
PCM55JP	24-Pin SOIC	178

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

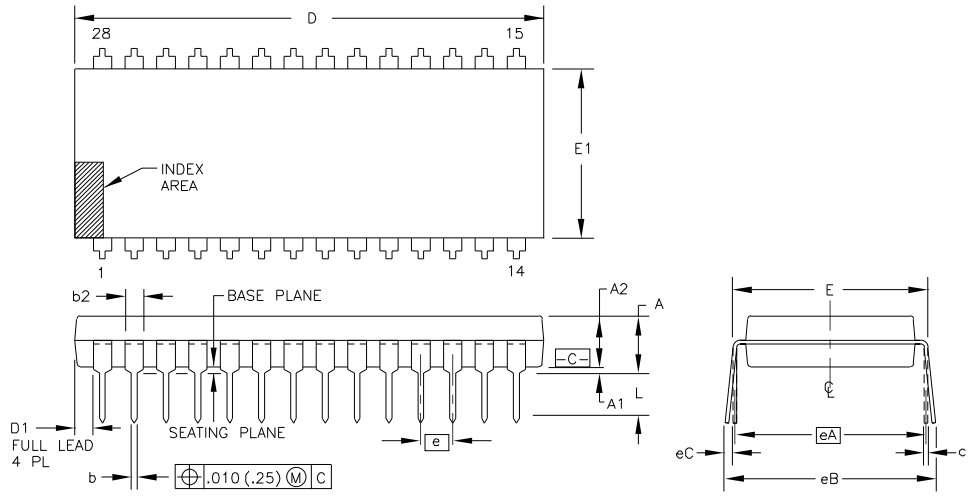
DC Supply Voltage	±18VDC
Input Logic Voltage	–1V to +5.5V
Power Dissipation	PCM54 800mW, PCM55 400mW
Storage Temperature	–55°C to +100°C
Lead Temperature, (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	THD at FS	PACKAGE
PCM54HP	0.008	28-pin DIP
PCM54JP	0.004	28-pin DIP
PCM54KP	0.0025	28-pin DIP
PCM55HP	0.008	24-lead SOIC
PCM55JP	0.004	24-lead SOIC

PACKAGE DRAWINGS

Package Number 215 - 28-Pin Plastic, Double-Wide DIP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.250	--	6.35	3
A1	.015	--	0.38	--	3
A2	.125	.195	3.18	4.95	
b	.014	.022	0.36	0.56	
b2	.030	.070	0.76	1.78	9
c	.008	.015	0.20	0.38	
D	1.380	1.565	35.05	39.75	4
D1	.005	--	0.13	--	4
E	.600	.625	15.24	15.88	5
E1	.485	.580	12.32	14.73	4
e	.100 BASIC		2.54 BASIC		
eA	.600 BASIC		15.26 BASIC		5
eB	--	.700	--	17.78	6
eC	.000	.060	0.00	1.52	6

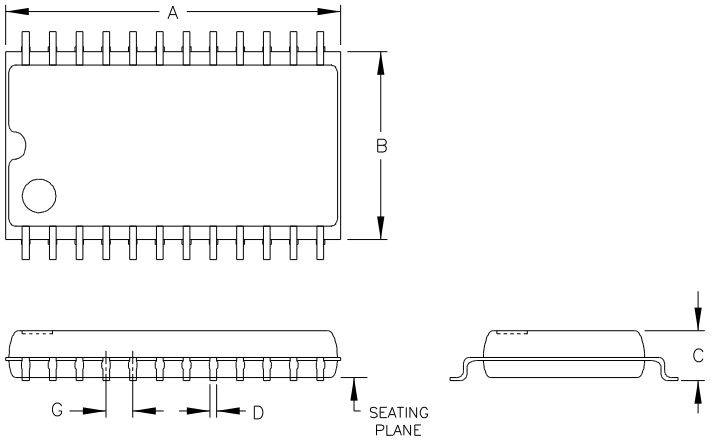
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
L	.115	.200	2.92	5.08	3
N	28		28		7

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM C .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ215	REV.: J
JEDEC NUMBER: MS-011-AB	

Package Number 178 - 24-Pin SOIC



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.614	.630	15.60	16.00	
B	.346	.362	8.80	9.20	
C	--	.098	--	2.50	
D	.012	.020	0.30	0.50	
G	.046	.054	1.17	1.37	

NOTES:

PACKAGE NUMBER: ZZ178	REV.: A
JEDEC NUMBER: NONE	