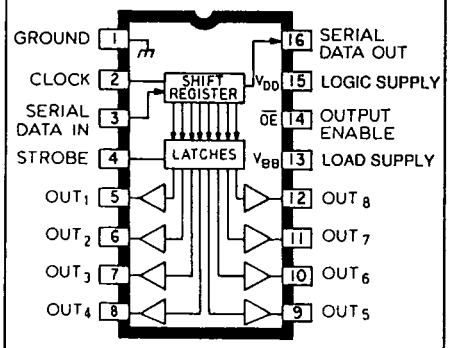
5895

T-51-15

BiMOS II 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

UCN5895A



Dwg. No. A-12,639

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Output Voltage, V_{OUT}
(UCN5895A/EP) . . . . . 50 V
(UCN5895A-2) . . . . . 25 V
Logic Supply Voltage Range,
V_{DD} . . . . . 4.5 V to 12 V
Driver Supply Voltage Range, V_{BB}
(UCN5895A/EP) . . . . . 5.0 V to 50 V
(UCN5895A-2) . . . . . 5.0 V to 25 V
Input Voltage Range,
V_{IN} . . . . . -0.3 V to V_{DD} + 0.3 V
Continuous Output Current,
I_{OUT} . . . . . -250 mA
Allowable Package Power Dissipation,
P_D . . . . . See Graph
Operating Temperature Range,
T_A . . . . . -20°C to +85°C
Storage Temperature Range,
T_S . . . . . -55°C to +150°C

Caution: CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

UCN5895A and UCN5895EP BiMOS II serial-input, latched source drivers are designed for use in applications requiring low output-saturation voltages and currents to -250 mA per driver. Each driver combines an 8-bit CMOS register, associated latches and control circuitry (strobe and output enable), with saturated bipolar emitter-follower outputs. Typical loads are low-voltage LEDs and incandescent displays. They can also be used with multiplexed LED displays, thermal printers, or electromagnetic printers within their output limitations.

The UCN5895A and UCN5895EP are rated for operation with supply voltages to 50 V and feature a minimum output sustaining voltage of 35 V. The more economical UCN5895A-2 is for use with supply voltages to 25 V (15 V sustaining). Under normal operating conditions, at +25°C, all outputs will source -120 mA continuously without derating. Similar drivers, featuring Darlington outputs for increased output ratings, are the UCN5890A and UCN5891A.

BiMOS II devices can operate at greatly improved data-input rates. With a 5 V supply, they will typically operate at better than 5 MHz. At 12 V, significantly higher speeds are obtained.

The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

These devices are rated for continuous operation over the temperature range of -20°C to +85°C. Because of limitations on package power dissipation, the simultaneous operation of all output drivers may require a reduction in duty cycle. The UCN5895A and UCN5895A-2 are supplied in standard 16-pin dual in-line plastic packages with copper lead frames for increased allowable package power dissipation. The UCN5895EP is supplied in a 20-lead plastic leaded chip carrier for minimum area, surface-mount applications.

FEATURES

- Low Output-Saturation Voltage
- Source Outputs to 50 V
- Output Current to -250 mA
- 3.3 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic & Latches

Always order by complete part number, e.g., **UCN5895A-2**.

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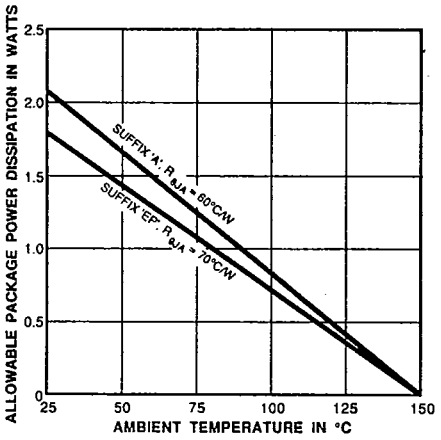
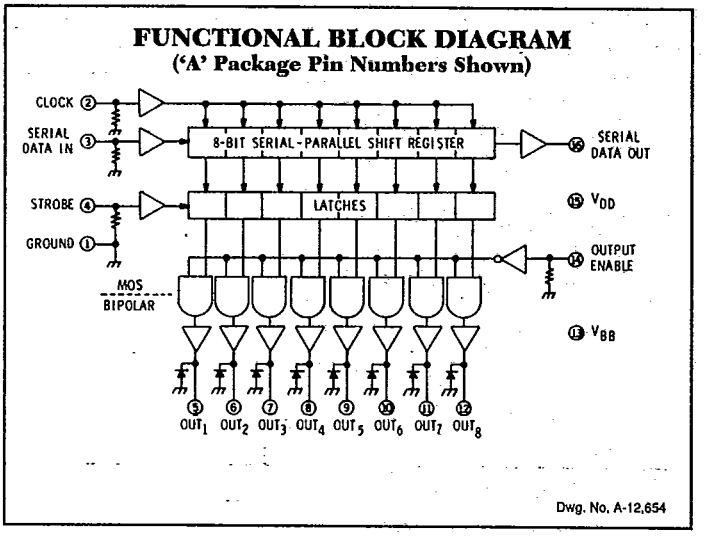
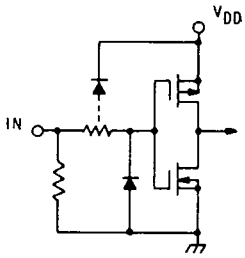


Dwg. GP-026



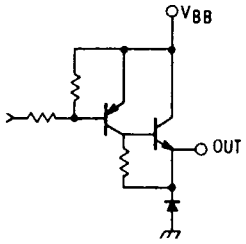
Dwg. No. A-12,654

TYPICAL INPUT CIRCUIT



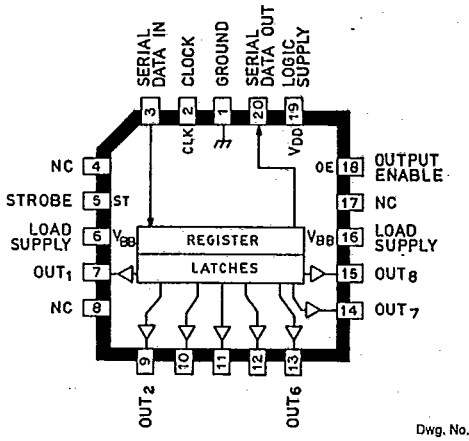
Dwg. No. A-12,520

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,655

UCN5895EP



Dwg. No. A-14,368

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BiMOS II 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

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ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 50 V (UCN5895A/EP) or 25 V (UCN5895A-2), V_{DD} = 5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	T_A = +25°C	—	-50	µA
		T_A = +70°C	—	-100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = -60 mA	—	1.1	V
		I_{OUT} = -120 mA	—	1.2	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = -120 mA, L = 2 mH, UCN5895A/EP only	35	—	V
		I_{OUT} = -120 mA, L = 2 mH, UCN5895A-2 only	15	—	V
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	V_{DD} = 5 V to 12 V	-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	50	µA
		V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	100	—	kΩ
		V_{DD} = 12 V	50	—	kΩ
Clock Frequency	f_{CLK}		3.3	—	MHz
Serial Data-Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 12 V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	Output Enable to Output, I_{OUT} = -120 mA	—	2.0	µs
Turn-OFF Delay	t_{PHL}	Output Enable to Output, I_{OUT} = -120 mA	—	10	µs
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10	mA
		All outputs OFF	—	200	µA
	I_{DD}	V_{DD} = 5 V, All outputs OFF, Inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, Inputs = 0 V	—	200	µA
		V_{DD} = 5 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	V_R = 25 V, T_A = +25°C	—	50	µA
		V_R = 25 V, T_A = +70°C	—	100	µA
Diode Forward Voltage	V_F	I_F = 120 mA	—	2.0	V

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

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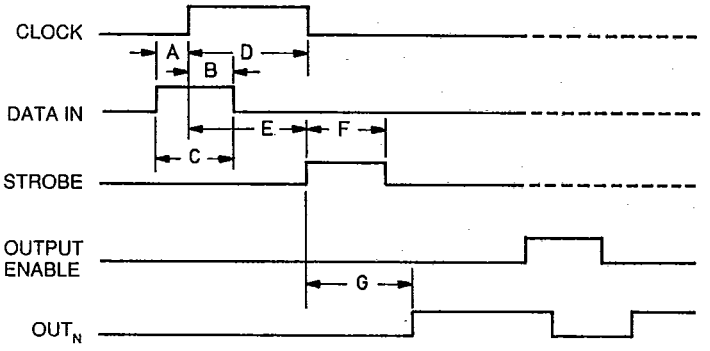

Dwg. No. A-12,649A

TIMING CONDITIONS
(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**
C. Minimum Data Pulse Width ..... **150 ns**
D. Minimum Clock Pulse Width ..... **150 ns**
E. Minimum Time Between Clock Activation and Strobe ..... **300 ns**
F. Minimum Strobe Pulse Width ..... **100 ns**
G. Typical Time Between Strobe Activation and Output Transition ..... **1.0 µs**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

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BiMOS II 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

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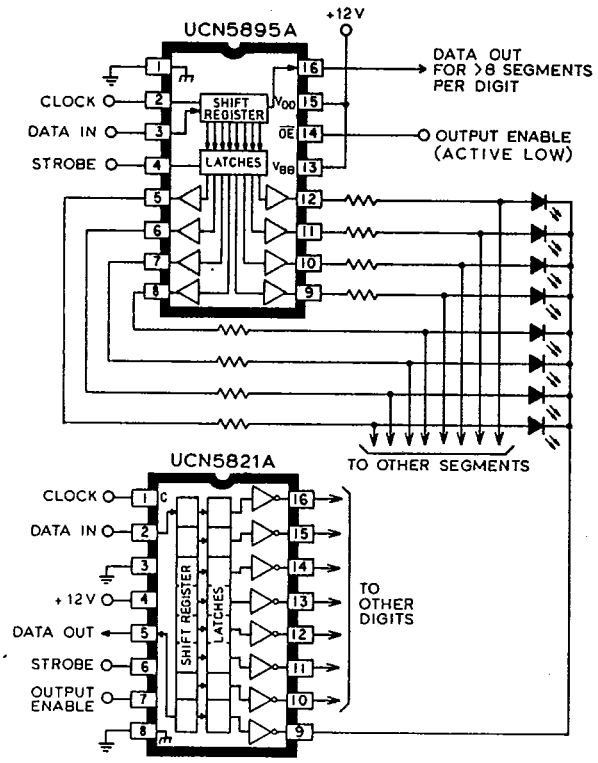
TYPICAL APPLICATION



Dwg. No. B-1541

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	⌐	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⌐	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⌐	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State