Built-in Sequencer Accelerates Testing

Test sequencing instruments lower test time, equipment cost, and rack space.

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Abstract

Narrowing profit margins are driving electronic manufacturers to reduce production costs, including the cost of testing. Generally, this involves efforts to reduce test time, which is increasingly difficult as products grow in complexity. Greater test complexity presents another problem: fitting more test functions into limited production space. The profit pinch is exacerbated by the current practice of concentrating product testing at the functional level, at the end of the line, where failed units carry a heavy burden of sunk production costs. This calls for a shift to more up-front testing to eliminate bad parts earlier in the process, and requires fast, flexible test systems that lower manufacturers' cost of ownership. A new generation of SMUs with a sophisticated built-in test sequencer and intercommunication bus is making all this possible. This article explains how these features can be used to build compact and economical systems for fast multi-channel component testing.

Most electronic manufacturers are faced with global competition, increasing product complexity, and decreasing profit margins, while product life cycles are shrinking. These forces are driving efforts to reduce product costs, including the cost of testing, which tends to grow with product complexity. The integration of analog, digital, and even RF circuitry on a single IC chip means higher density and pin counts. Higher pin counts require more test channels to maintain acceptable throughput. Test system density must also increase to stay within limited production space.

Currently, production ATE systems can be categorized as bulky, high cost mainframe-based systems, slow instrument-based systems using PC control, or fast instrument-based systems that are extremely complex to develop. None of these are optimized for production processes. Manufacturers need to improve the performance of existing test stands, plus new test techniques, instruments, and systems that minimize the cost of testing and ongoing ownership costs. These solutions should allow the systems to take on more of the test burden earlier in a production cycle, thereby reducing high cost end-of-the-line testing. In short, test systems should:

- Shorten test time
- Minimize test stand rack space
- Reduce development time
- Lower ownership costs

Matching Test Equipment to the Application

A common production need is a set of repetitive test sequences that apply a voltage or current, measure the response of a device under test (DUT), compare it to acceptable limits, and make a pass/fail decision. This is especially true in early stages of production.

Simple 2- to 4-pin devices. This DUT category includes diodes, LEDs, transistors,

Figure 1. Keithley Model 260X System SourceMeter® Instrument

linear regulators, MEMs switches, relays, etc. For 2-terminal devices, a fairly simple source-measure procedure can be used. Three- and four-terminal devices require more complex testing and fast transient response on two test channels to generate accurate I-V curves. With fast component handlers (10ms/part), instrument speed is very important.

Component arrays. Examples include arrays of resistive chips, transient voltage suppressors, ferrite beads, and flip-chips. Tests performed on these devices are the same as those for discrete versions of these components. However, all individual devices must pass the tests before an array is approved. For high throughput, parallel multi-channel testing is needed.

IC/RFIC/component-on-wafer testing. In the early stages of production, a wide variety of complex, low-power devices require measurements of quiescent and leakage current at nanoamp levels. In addition, all the DUTs on a wafer require a simple set of DC measurements to check basic functionality. Because there are thousands of DUTs per wafer, fast, multi-channel testing is mandatory.

Other complex devices/modules. Some examples include power supplies, data acquisition cards, and hybrid ICs. Such testing requires diverse instruments and measurements that can range from DC to RF. It often requires tight timing between source-measure sequences and multiple instruments to accurately characterize DUTs. Scalable instruments and test equipment modules are usually needed to construct a customized system with a large number of parallel channels.

Select the Test System Architecture

Consider architectures in the following broad categories:

Single box/single channel I-V solutions are often acceptable for testing less cost sensitive devices that can tolerate the lower speed of a sequential source-measure procedure. Multiple source-measure units (SMUs) can be used with or without switch matrixes to form a multi-channel system, but this arrangement has limited rack density and throughput. In smaller systems, SMUs are typically used under PC control via GPIB

and/or external trigger lines. Typically, test programs for the PC utilize SCPI command calls.

Parallel I-V systems are designed for multiple DUT testing or for multi-channel testing of more complex devices. Depending on the DUT, test system throughput could be limited by the instrument, application program, or DUT settling time. Limitations in existing parallel channel systems include sequential channel hopping (i.e., no simultaneous measurements), limited voltage or current range, lack of flexibility, bulky equipment, and high cost.

Scalable multi-channel systems often include diverse instruments to test complex electronic modules. The two most common types are integrated functional testers and I-V test systems built from open API (application program interface) instrumentation. Open API means that individual instruments are components in a customized test solution, as opposed to a functional or parametric tester that is a complete prepackaged (turnkey) system. SMUs are often a core component in both architectures. Broadband instrumentation (signal generators, oscilloscopes, spectrum analyzers, etc.) tends to be added externally. In turnkey systems, much of the hardware and software integration has been done for the user. The disadvantage is relatively high cost. By contrast, open API systems offer users and system integrators a high degree of flexibility with the potential for lower cost.

Ways to Lower Test Costs

Four system parameters have been identified as the key to lowering test costs: shorter test times, reduced development time, smaller system size, lower cost of ownership. Each parameter is multidimensional.

Shorten Test Times. Taking aside test fixture loading, there are a few distinct intervals that take up the greatest portion of test cycle time. Depending on system design, these time intervals include:

- Source application, including signal transients
- DUT settling time
- Measurement, including range change if applicable
- Trigger delays
- Data communications
- Program execution, including pass/fail

and binning decisions
- Test fixture movement and/or electrical switching times

The first level of test time improvement is gained by switching from individual source and measure instruments to an integrated SMU system. This cuts down on trigger delays and data communications time between separate instruments and a PC controller. If the SMU can store and execute a test sequence without PC control, this cuts down on relatively slow GPIB traffic and PC latencies.

Some SMUs have program memory that can run up to 100 predefined tests, make limit comparisons, perform conditional program branching, and work with or without a PC. In a single channel system, this type of SMU allows significant test time improvement in a straightforward manner. However, it's much more complicated in a multiple SMU system due to the difficulty in managing multiple triggers and test sequencers.

Because of this difficulty, older SMUs have a sequencer that only uses command cues, i.e., they store multiple GPIB commands that can be executed with a single SCPI call from a PC. These SMUs do not have logic to perform limit testing, or make instantaneous pass/fail decisions. They also do not have a DUT handler interface; consequently, there is a great deal of GPIB traffic. Furthermore, many older designs do not allow parallel channel testing – channels are accessed sequentially, so throughput improvement is marginal.

New SMUs Increase Throughput. A new class of SMUs with a test script processor and high speed control bus solve the problems just described. These SMUs allow easy multi-channel scalability and simple programming. Yet, they can run complex, high-speed test sequences by sharing the resources of multiple SMUs. For example, Keithley Series 2600 System SourceMeter® Instruments can be used in a master-slave arrangement for true parallel channel measurements. Therefore, a test engineer can take full advantage of other SMU features, such as:

- 4-quadrant operation (source or sink +/− voltage or current)
- Voltage and current sweep capabilities
- Wide dynamic range of source and measurement

- Fast transient response
- Picoamp sensitivity
- Resolution as fine as 6½ digits
- Memory for 100s of test sequences
- High-speed for fast pass/fail testing
- Digital I/O for general IO, trigger coordination, and component handler interface

In addition, the newest units have pulse and low frequency arbitrary waveform generator capabilities that can be applied to each channel. This simplifies complex testing by providing a universal analog I/O pin for a wide range of applications.

With these features, dramatic gains in throughput can be realized by changing the system programming approach. Instead of using PC-based control, the SMU's test sequencer and program memory control testing. Throughput is further enhanced with Keithley's Test Script Processor (TSP®), high-speed sequencer, and fast control bus (TSP-Link®). Multiple SMUs can be used as if they are part of the same physical unit for high-speed multi-channel testing. The TSP-Link technology employs embedded trigger lines and a 100Mbit/s serial bus that allow parallel I-V sweeps across multiple units with low trigger jitter (critical for high bandwidth applications). Since ranging can consume a lot of source-measure time, these units have a wide dynamic range and seamless range switching to significantly speed up test sequences.

Figure 2 illustrates a multiple SMU system of this type. Throughput is comparable to mainframe-based systems.

Decrease Development Time

Having these SMU features in a single box means there is less for a system designer to integrate, and software development time is reduced. Additionally, Keithley's Test Script Processor (TSP) provides an intuitive command language similar to Basic as a simple programming interface. With TSP and Keithley's free Test Script Builder software,
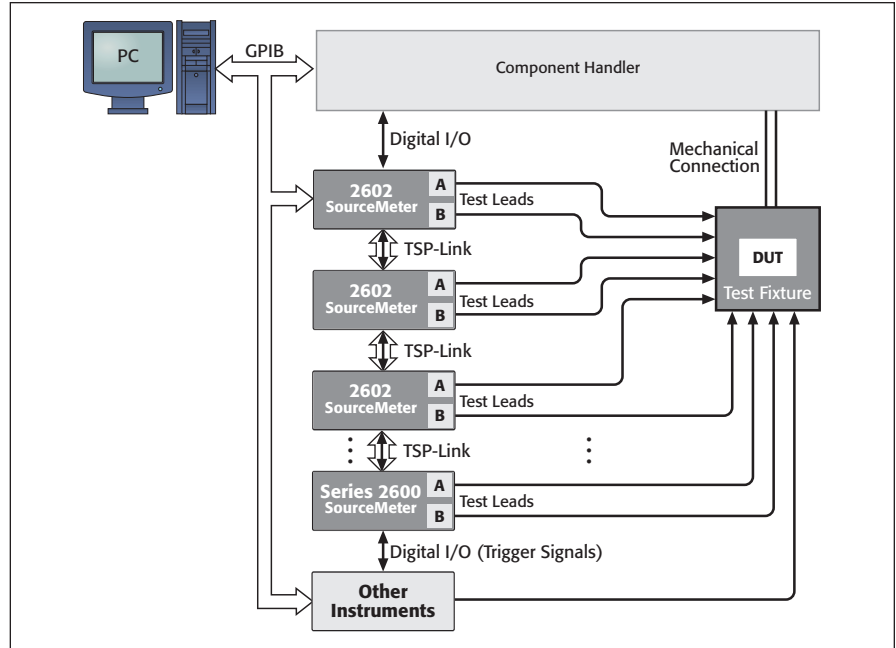

Figure 2. Keithley TSP-based multiple SMU test system.

it is easy to create complex test sequences controlling multiple SMU channels acting as a single entity. Evolving test requirements are easily accommodated with a minimum of SMU hardware changes.

Reduce Rack Space

The new Keithley units come in a high-density, 2U half-rack design. In the transition to higher pin count devices, this may allow a multi-channel system to remain in one rack. (Many test systems require 16 or fewer channels, but the Keithley systems accommodate up to 128.)

Lower Cost of Ownership

A rack-and-stack SMU system eliminates mainframe overhead and reduces hardware costs. When the test system needs to be changed, reusable SMU hardware and reduced software development also lower costs. In addition, a smaller test system footprint on the production floor generally equates to lower ownership cost. For smaller systems,

a rack-and-stack design offers significant advantages over mainframe systems, which have a high cost per channel unless most of the card slots are filled. For this reason, future mainframe expansions are also expensive.

Summary

The new generation of SMUs, exemplified by the Keithley Series 2600 Systems, satisfies electronic manufacturers' needs for cost effective automated systems that rapidly test high pin count devices or multiple devices in a production test fixture. These SMUs can easily add new capabilities and capacity to existing test stands and lower capital investment in new stands. They offer easy scalability, simpler system integration, and small test stand footprints. Test systems developed with these new SMUs can truly lower the cost of ownership while increasing flexibility, performance, and reliability.