IBIN-PS/2
Interface for IBM PS/2 and Compatibles with Microchannel Architecture

The IBIN-PS/2 interface plugs into any of the expansion slots in IBM PS/2 Models 50, 55SX, 60, 70 and 80 or compatibles, and serves as an interface between the computer and the Models 500A, 500P, and 575. The interface card contains POS circuitry, address buffering and decoding, data buffering, configuration and status information, a programmable interval timer, and interrupt generation circuitry.

Software Support

The IBIN-PS/2 interface card requires the use of Soft500 Version 5.2 or later, Quick500 Version 1.2 or later, or KDAC500. If third-party data acquisition software is used, it must support the features and operation of the IBIN-PS/2. Note: Even if you plan to use third-party software exclusively, you will need the "@6571.ADF" file included with your Keithley software to install the IBIN-PS/2 in your computer.

Reading TIME/DATE with Keithley 500-Series Software

The CLOCKREAD command of Soft500 V5.2 and Quick500 V1.2, and the KDCLOCK command in KDAC500 default to reading the battery-backed clock and calendar located on the computer's mother board. This operation supplies time and date information within a test program even though the IBIN-PS/2 does not have a battery-backed clock and calendar of its own. To set time and date, use the standard computer set-up program, or other utility suggested by the computer manufacturer. Do not use the SETCLOCK utility which may be included with the Keithley software.

Installing the IBIN-PS/2 Interface Card

CAUTION

Turn power off before installing or removing the interface card.

To install the IBIN-PS/2 interface card you will need a backup copy of the Reference diskette that was provided with your computer. The Reference diskette contains various programs and files that are essential to installing new peripherals in your computer. If you do not have a back-up copy of the Reference diskette, you must make one according to the instructions provided with your computer.

The installation procedure for the IBIN-PS/2 interface card consists of several steps. First, the interface card itself must be physically installed in the computer. Then the computer must be reconfigured to recognize the interface card. Once the computer is properly configured, the Soft500, Quick500, or KDAC500 installation should be run in order to check for correct operation (even if you are planning to run other software exclusively).

The following directions and illustrations show the IBM Personal System/2 Model 50. For other models, consult the documentation which accompanies the computer.

IBIN-PS/2 Hardware Installation

Install the IBIN-PS/2 into a vacant expansion slot as follows: Make sure the PS/2 is turned off, and unplug the power cord. Check that the cover is unlocked, and then loosen the thumbscrews at the rear of the system unit. Remove the cover by sliding it forward approximately two inches, and then lifting it (see Figures 1 and 2).

A rear panel opening is provided at the end of each expansion slot for mounting I/O connectors. If a slot is unused, then this opening will be covered by a metal plate held in place by a thumbscrew (Figure 3). Loosen the thumbscrew (use a coin if it is too tight) and remove the cover plate from the desired expansion slot.

Carefully install the IBIN-PS/2 card by fitting the DB25 connector through the rear panel and firmly pressing it into the expansion slot until the card clicks into place (Figure 4). With the board firmly in place, tighten the thumbscrew.

Slide the cover back on and tighten the thumbscrews, lock the cover lock, and reconnect the cables and power cords to the rear of the computer. Plug the power cord into an electrical outlet.

Finally, attach the interface cable to the connector (J2) on the interface card at the rear of the computer. Never strain the connection between cable and connector. The other end of the cable should be plugged into the mating connector on the rear panel of the Series 500. Avoid entangling the interface cable in 60 cycle AC power lines or other noisy lines.

The system is now ready for hardware configuration and software installation.

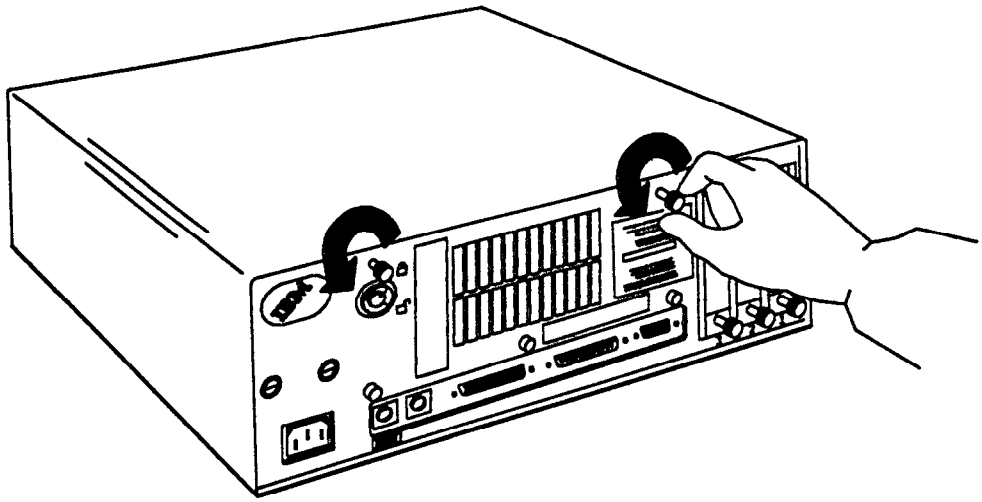


Figure 1. Removing PS/2 Cover Screws

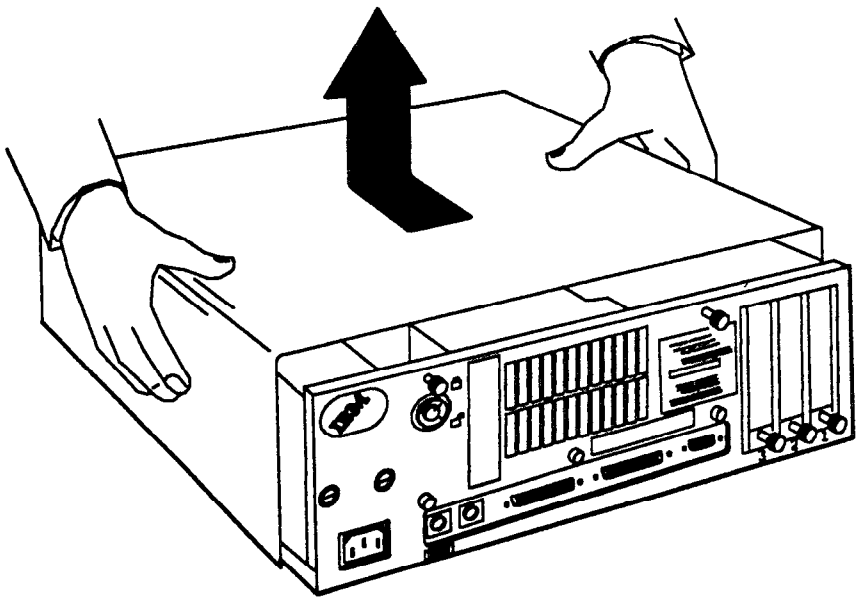


Figure 2. Removing PS/2 Cover

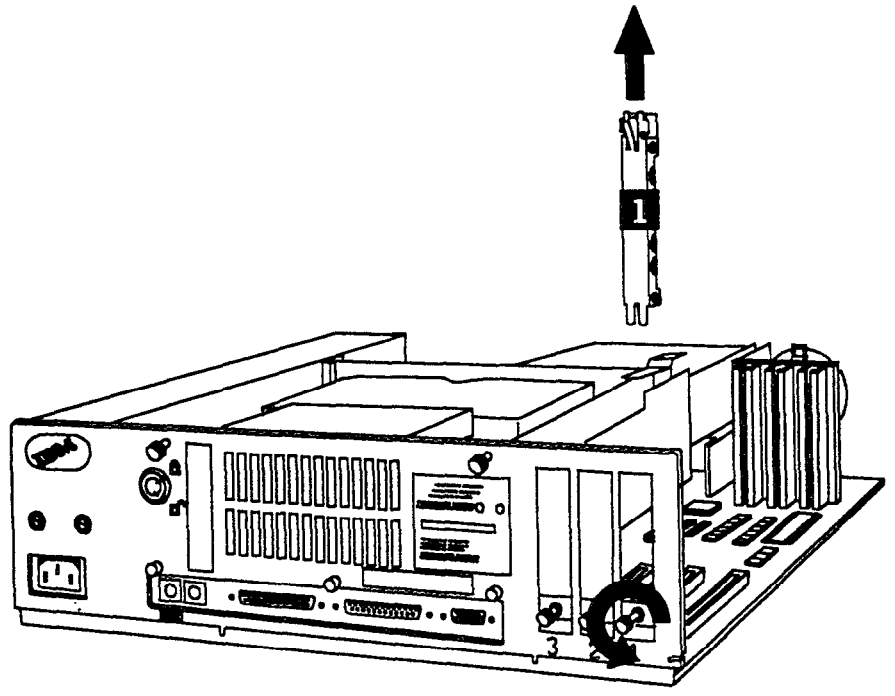


Figure 3. Removing Expansion Slot Cover

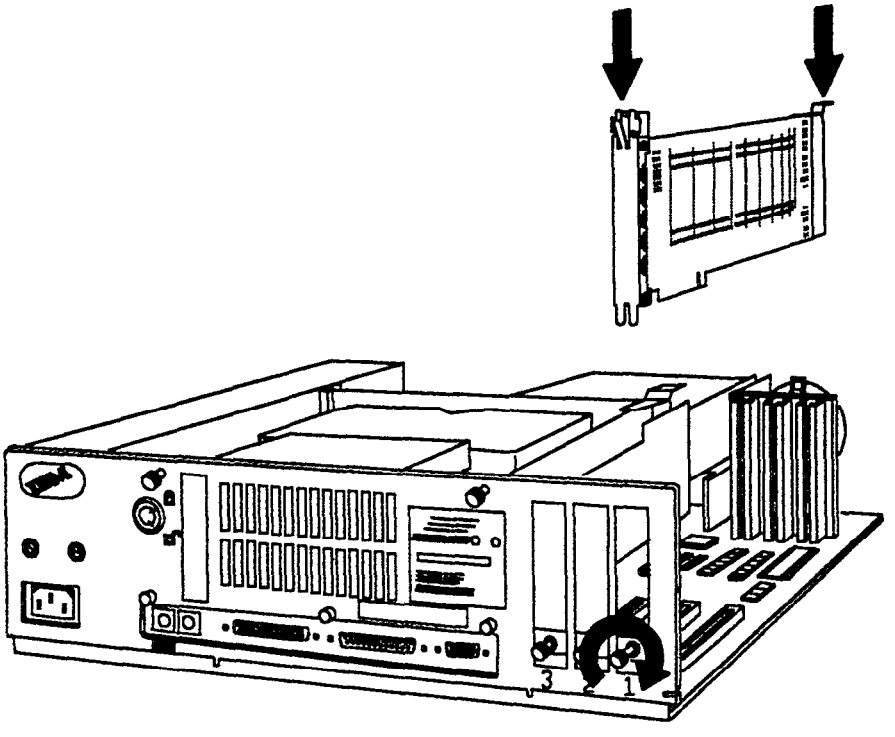


Figure 4. Installing IBIN-PS/2

IBIN-PS/2 Hardware Configuration

There are no hardware switches to set when installing the interface card into your computer. The PS/2 family of computers uses a different method for selecting a particular hardware configuration called "software switches". The following discussion details the procedure for setting these switches using the configure program supplied by IBM.

Insert the back-up copy of the Reference diskette into drive A: and turn the computer and display on. The system should boot from the Reference diskette and display the start-up screen with IBM logo. You may notice "165" on the display screen during the power-on self-test. This number indicates that the computer has noticed (correctly) that there has been a change in hardware configuration.

NOTE

You will not be able to use the computer until it has been set for the new configuration using the Reference diskette.

If the computer does not boot-up, first check that you are using a back-up copy of the Reference diskette and that it is correctly inserted in drive A:. If you do not have a back-up copy, turn the power off, remove the IBIN-PS/2 interface, and follow the instructions that came with the Reference diskette to make a back-up copy. Then re-install the IBIN-PS/2 interface and re-boot the computer with the new back-up Reference diskette.

If the computer still does not boot, check to see that all cables and circuit boards are installed correctly. If everything appears to be correct, but the computer still does not boot from the back-up copy of the Reference diskette, then contact Keithley Data Acquisition and Control for assistance.

Once the Reference diskette has booted, you should press the <Enter> key to continue. At this point you should see the first two screens indicating that the computer has detected a change in the configuration. The second of these screens asks: "Automatically configure the system? (Y/N)". As we are not yet ready for automatic configuration, you should answer "No" by pressing the "N" key.

You should then see a menu. Use the <Up>/<Down> arrow keys to choose item 5, "Copy an option diskette" from the menu. Then press <Enter> to perform the indicated operation. "Copy an option diskette" is used to copy the configuration files from the Keithley 500-Series software diskette ("the New Option Diskette") to the back-up copy of the Reference diskette ("the Product 2 diskette"). Follow the displayed instructions to copy the files.

Now the system is ready for configuration. Select item 3, "Set Configuration", and press <Enter>. From the configuration menu choose item 2, "Change Configuration", and press <Enter>.

Now, check that the address shown for IBIN-PS/2 is 0CFF80. If necessary, use the cursor keys to move to the address entry for the PS/2 interface. Press the <F5> or <F6> keys to toggle to the address 0CFF80. When you are done, press <F10> to save the information, and then press <Enter>. Press <Esc> twice. Eject the diskette, and then press <Enter> to restart the system.

Conclude with software installation program.

Installing More Than One IBIN-PS/2 in a Personal System/2

Install the IBIN-PS/2 interfaces in the PS/2 expansion slots. Consult the IBM and IBIN-PS/2 documentation for instructions on opening the computer and installing the IBIN-PS/2 cards. When you are done installing the interfaces, replace the cover.

Consult the previous section which describes running the IBM-supplied hardware configuration program. As necessary, follow the instructions for copying the reference diskette and option diskette.

Now the system is ready for configuration. Select item 3, "Set Configuration", and press <Enter>. From the configuration menu choose item 2, "Change Configuration", and press <Enter>. Use the cursor keys to move to the address entry for each PS/2 interface. Select a different address for each IBIN-PS/2 card by pressing the <F5> or

<F6> keys to toggle up or down through the available addresses. Suggested addresses are 0CFF80 for the interface in the lowest-numbered slot, 0CFB80 for the second interface, 0CF780 for the third interface, and so on. There are many possible addressed which should be compatible with any other hardware you may have in the PS/2. Confirm that no other hardware is using the addresses you have assigned for the IBIN-PS/2 cards.

Use the cursor keys to move the interrupt entries for each PS/2 interface. The IBM Configuration program should already have set the interrupt level for the IBIN-PS/2 interfaces to "10". Let the address for the IBIN-PS/2 in the lowest-numbered slot at "10". Use the cursor keys to move to the interrupt level for each of the other interfaces, and then disable the interrupt by pressing the <F5> key to select "Not Used".

When you are done, press <F10> to save the information.

Press <Esc> twice. Eject the diskette, and then press <Enter> to restart the computer.

Conclude with software installation.

Parameters (OPTIONAL)

Hardware configuration is normally automatic, but it is possible to modify the configuration by using the Change Configuration option on the Reference diskette. Change Configuration allows you to set the IBIN-PS/2 interface hardware parameters: Memory Mapped Base Address and Interrupt Level. The parameters should be set according to the following guidelines:

The Memory Mapped Base Address selects the address range of the interface in the PS/2 system memory map. This is normally set for a starting location of hex CFF80 (the factory default), but can be configured over the addressing range of Hex C0380 through FFF80. This setting determines only 8 bits of the Series 500's address region, the other 12 bits are hard-wired as follows.

MSB 11xx	xxxx	xx11	1000	LSB 0000
C	0	3	8	0
C	0	7	8	0
C	0	B	8	0
C	0	F	8	0
C	1	3	8	0
.	.	.	.	.
.	.	.	.	.
D	0	3	8	0
.	.	.	.	.
.	.	.	.	.
E	0	3	8	0
.	.	.	.	.
.	.	.	.	.
F	F	F	8	0

"x" = user-configurable address bit.

Note that many of the possible address for the Keithley interface will conflict with other hardware already in the system, such as fixed disks, video adapters, and expansion memory, so the practical range of addresses is fewer than the hardware provides for. The configure program limits your choices to areas where the IBIN-PS/2 has been used successfully.

Memory conflicts occur when the computer attempts to read an address occupied by more than one piece of hardware. These problems can be manifest as error messages at boot-up, or failure of the hardware or Keithley system to operate properly. If this occurs, examine the memory usage of all the hardware in your computer, and make changes where necessary. Usually, changing the address of the Keithley interface is all that is required. Normally, the configuration program will prevent you from getting into trouble when changing these parameters.

You should have no technical difficulty finding usable addresses, although you may have to do some research to find out what addresses are free in your computer.

The Interrupt Level for the IBIN-PS/2 interface board should normally be set to 10 which is the highest priority interrupt available on the PS/2 bus. This interrupt is used

to provide timing for data acquisition. The higher the priority of the interrupt, the less jitter will occur on the timing of the data acquisition. If your timing must be fast, such as 1 to 100 milliseconds, you should use the higher priority interrupt. If your timing requirements are slower, such as 0.1 to 1 second, you may consider using a lower priority interrupt. The "Not Used" option may be selected for programs that do not use the interface card to generate interrupts.

Interrupt level 10 has the highest priority followed by levels 11, 15, 3, 4, 5, and 6 with the lowest priority.

Software Installation

The system is now ready for software installation. Refer to the Keithley or third-party software manual for details on installing your software. If you are using a third-party software package, make sure that it is compatible with the IBIN-PS/2 before you start. Consult the manufacturer's documentation.

Theory of Operation

The interface to the Series 500 is provided through connector J2. The connector contains five address lines (MBA0-MBA4), a read/write (MBR/W), and a select line (MBSEL) which control the Series 500. The connector also contains an eight bit data bus (MBD0-MBD7), a mother board interrupt request line (MBIRQ), and 5 lines for power (+5V) and ground. Figure 5 shows the component layout of the IBIN-PS/2 interface. Refer to Component Layout.

Address Decoding Circuitry-Global

The interface is memory-mapped to the host computer and responds to READ and WRITE commands. It does not respond to the INT and OUT peripheral commands used by most peripheral devices.

The interface maps into a 128-byte region of memory which may be positioned by the user in one of the 256 region defined by the address bits MA10-MA17 which are stored in programmable option select (POS) register 3. See Section 3 of Installing The interface Card, hardware Parameters, for more information.

The address decoding circuitry, U14, U17, U18 and U22, uses the microchannel address lines, the read/write lines (S0 and S1), the M/-IO line, the -CMD line, and POS register 3 (the base memory address). The POS register, U17, is initialized at power-up with memory address bits 10-17, the interface address. U18, an 8 bit comparator, compares the stored address with incoming microchannel addresses. Address bits A7-A9, A18 and A19 are checked for logic "1" by U22, A21-A23 are checked for logic "0" by U14, and A20 is checked for logic "0" by U18. The read/write lines -S0, -S1 are also used in U14 as part of the decoding. The result is a signal, -CD SFDBK, that represents "IBIN is addressed" on pin 19 of U14. U14 is also used to create several other decoding and timing signals as follows:

pin 18	CD CHRDY - Data ready signal to the microchannel bus (wait state generator)
pin 17	/CDSEL - Latched version of "IBIN" is addressed"
pin 15-16	/BS0 and /BS1 - Latched versions of S0 and S1, read and write
pin 14	MBSEL - Select pulse for use by external chassis, gated by MBEN
pin 13	CMDRC - from -CMD - Used as time delay for CD CHRDY and MBSEL
pin 12	SETLRC - from -CMD - Used as time delay for MBSEL

Address Decoding Circuitry-Local

U9a and U6 provide the local decoding of the following regions of the local address map:

U9a	pin 12	/READ - General purpose read/-write line - POS or memory map
	pin 13	/IOR - I/O space read for POS
	pin 14	/IOW - I/O space write for POS
	pin 15	/CONTEN - Control registers for TIMER GLOBAL (offsets Hex 60-63)
U6	pin 6	/8254CS - Selects the 8254 (U1) registers (offsets Hex 40-43)
	pin 4	/MBEN - Selects the external chassis address space (offset Hex 00-1D)
	pin 10	/CLRINT - Clear interrupt latch
	pin 11	/RSTAT - Read the status register TIMER STATUS
	pin 12	/WCONFIG - Write to configure register TIMER GLOBAL

Programmable Option Select (POS) Registers and Logic

U5 decodes the particular address of a POS location using the SETUP signal from U21 and the three buffered address signals from U21, BA0-BA2. U3 provides the interface ID value. U11 stores the interrupt level value. U17 stores the base memory address as discussed earlier. U7b holds the card enable flag and is reset from a buffered version of the microchannel reset signal on power up (U10c).

Configuration and Status Registers

U4 is a set of latches that hold the three configuration bits for TIMER GLOBAL. Pin 7 is the Interrupt Enable flag, pin 15 and pin 10 are the configure bits that control the clock signals to the 8254 (U1) timer chip. U2 buffers the status signals onto the data bus using the RSTAT signal discussed earlier. The five status bits reflect the output of the three counters of the 8254 (pins 2, 4 and 6), the external chassis interrupt signal (pin 12) and the interrupt latch value (pin 14).

Interrupt Latch and Drivers

U13 and U12 drive the interrupt lines on the microchannel bus. U7A uses the output of counter 0 of the 8254 (U1) to clock the interrupt enable signal, INTEN, stored in U4. Provisions for external chassis interrupts are also provided through U10d.

Address and Data Latching/Buffering

U21 is used to latch the required bus signals on -CMD. These include address bits A0-A6 and the SETUP signal indicating a POS access. U15 and U19 buffer the data bus between the microchannel, and IBIN circuitry, and the external chassis. U20 buffers the address and the control signals to the external chassis.

Programmer Model for the Memory Map

A summary of memory locations used with the interface card is given in Table 1. These addresses correspond to the "Command A" and "Command B" functions associated with each module in the Series 500 module library. Note that some modules also use "Command C" and "Command D" for special functions. Collectively, these addresses are labeled "CMDA", "CMDB", "CMDC", and "CMDD".

Table 1. Memory Map Locations and Functions

(Presumes prior execution of a DEF SEG=CFF8 command)

Function/Use		Location (hex)
Slot 1	CMDA	xxx00
	CMDB	xxx01
	CMDC	xxx1A
	CMDD	xxx1B
Slot 2	CMDA	xxx02
	CMDB	xxx03
	CMDC	xxx18
Slot 3	CMDA	xxx04
	CMDB	xxx05
	CMDC	xxx19
Slot 4	CMDA	xxx06
	CMDB	xxx07
Slot 5	CMDA	xxx08
	CMDB	xxx09
Slot 6	CMDA	xxx0A
	CMDB	xxx0B
Slot 7	CMDA	xxx0C
	CMDB	xxx0D
Slot 8	CMDA	xxx0E
	CMDB	xxx0F
Slot 9	CMDA	xxx10
	CMDB	xxx11
Slot 10	CMDA	xxx12
	CMDB	xxx13
R/W COUNTER 0		xxx40
R/W COUNTER 1		xxx41
R/W COUNTER 2		xxx42
COUNTER CONTROL		xxx43
TIMER GLOBAL		xxx60
TIMER STATUS		xxx61
CLEAR INTERRUPT		xxx62
SET INT LEVEL		xxx63

The programmable interval timer can be used to time events, create software delays, and generate periodic interrupts to the PS/2. The timer consists of three independent 16 bit counters, which can be cascaded together to create longer timing intervals. The timer uses a 1.02MHz input which is generated by dividing the 14.31818MHz OSC pin on the microchannel bus by 14 using U16. This allows the timer to have a resolution of 977ns. The least significant counter allows timing up to 64.1ms. Two cascaded counters allow up to almost 70 minutes, and three cascaded counters allow timing up to 8.7 years.

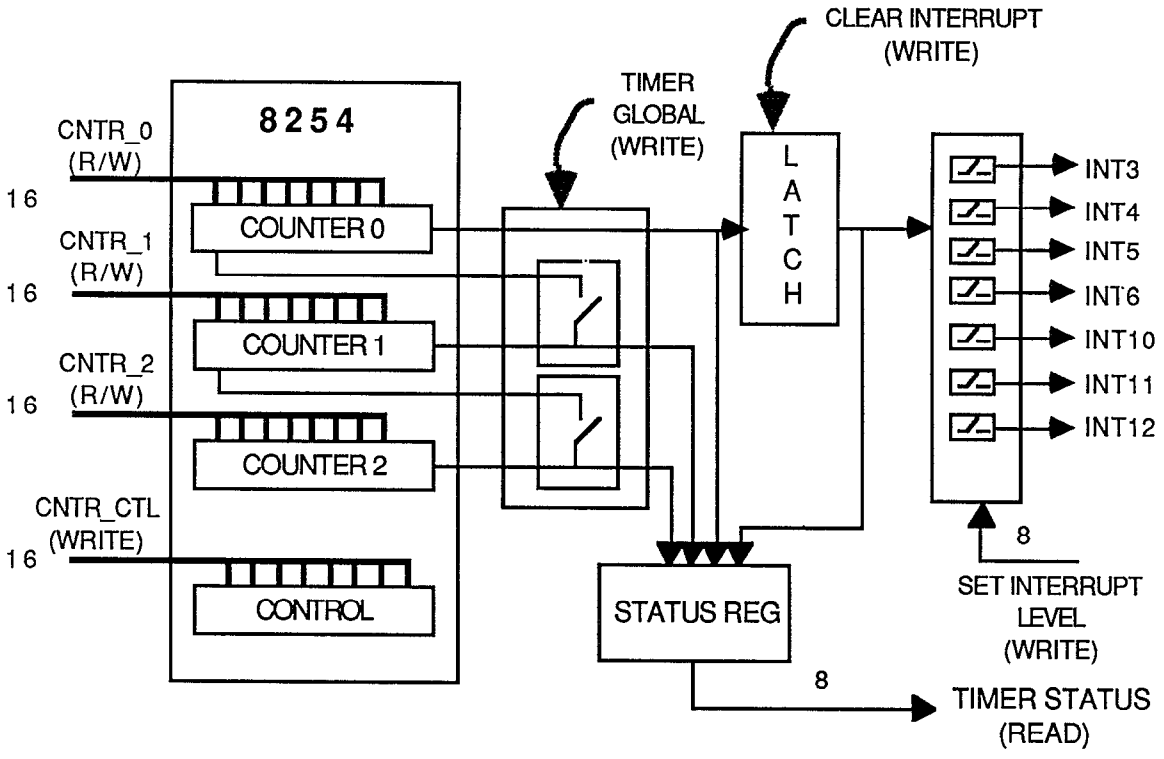


Figure 5. Functional Block Diagram of IBIN-PS/2 Timer Circuit

R/W COUNTER 0

Location: xxx40

This location is used to load counter 0 with the interval count, as well as to read the interval from that counter. Data to this location is always sent as two bytes in succession. The first WRITE (or READ) is the low byte of the count, and the second WRITE (or READ) the high byte. The read or write must be issued twice for the counter to function. The counter automatically makes the low byte register available first followed by the high byte register.

A write to COUNTER CONTROL (see discussion below) must always precede any R/W COUNTER commands.

R/W COUNTER 1

Location: xxx41

This location is used in the same way as R/W COUNTER 0, except it applies to counter 1.

R/W COUNTER 2

Location: xxx42

This location is used in the same way as R/W COUNTER 0, except it applies to counter 2.

COUNTER CONTROL

Location: xxx43

An access to the COUNTER CONTROL location always precedes the R/W COUNTER commands discussed above, indicating to the timer which of the three counters is to be addressed, and in what mode that counter will be used. COUNTER CONTROL should always be followed by two successive R/W COUNTER commands for the specified counter.

The counters can be used in three modes: interrupt generator, carry generator, and latch mode. Counter 0 cannot be used as a carry generator, and counters 1 and 2 cannot

generate interrupts. This functionality is due to the TIMER GLOBAL circuitry discussed below.

The interrupt mode allows counter 0 to produce periodic interrupts. When two or three counters are linked, the carry generator mode causes the terminal count of one counter to trigger the count in another counter (see Table 2). The counters can be used for timing events and creating software delays by masking off the interrupts using the TIMER GLOBAL location.

Table 2. Values Written to COUNTER CONTROL

Mode	Counter 0	Counter 1	Counter 2
Interrupt Generator	00110100 Hex 34 52 (Decimal)	Not used	Not used
Carry Generator	Not used	01110100 Hex 74 116	10110100 Hex B4 180
Latch	00000000 Hex 00 0	01000000 Hex 40 64	10000000 Hex 80 128

In general, the count is always carried from counter 2 to counter 1 to counter 0. When linked, counter 0 is always the carrier of counts generated by higher numbered counters, and should be set to interrupt mode. The higher numbered counters should be set to carry generator mode. When only counters 2 and 1 are linked, counter 1 should be set to interrupt mode, and counter 2 to carry generator mode.

The latch mode is used to read the counters. The latch transfers the count into an intermediate register, allowing a stable reading without disturbing the count in progress. Table 3 describes the bit configuration of values written to the counter control location.

Table 3. Bit Configuration of Values Written to COUNTER CONTROL

D7	D6	D5	D4	D3	D2	D1	D0
(----SC----)		(---W/L---)		0	1	0	0

Explanation:

SC (Select Counter)	Counter 0 = 00 Counter 1 - 01 Counter 2 - 10
W/L (Write/Latch)	Latch = 00 Write = 11

TIMER GLOBAL

Location: xxx60

This location is used to set mode of the timer circuitry. In any routine involving the timer, this command should be issued prior to the COUNTER CONTROL and R/W COUNTER commands. If it is not issued, all interrupt and carry functions will be off.

The lower three bits of this location determine whether the interrupt circuitry of the timer is enabled, and whether any of the counters will be linked with the carry generator.

When the computer is first turned on or when the system is rebooted, all functions associated with this command are initialized to off.

Table 4 provides a summary of values written to the TIMER GLOBAL location. Table 5 describes the bit configuration of these values.

Table 4. Values Written to TIMER GLOBAL

Mode	No Carry	Carry 1-0	Carry 2-1	Carry 2-1-0
Counter 0 interrupt off.	0000 H00 0	0001 H01 1	0010 H02 2	0011 H03 3
Counter 0 interrupt on.	0100 H04 4	0101 H05 5	0110 H06 6	0111 H07 7

Table 5. Bit Configuration of Values Written to TIMER GLOBAL

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	INT	2-1	1-0

Explanation:

X	Not used	
INT	Interrupt ON/OFF	(OFF=0, ON=1)
2-1 Carry	Counter 2 - Counter 1	(OFF=0, ON=1)
1-0 Carry	Counter 1 - Counter 0	(OFF=0, ON=1)

TIMER STATUS

Location: xxx61

The TIMER STATUS location can be read to view the output status of the interrupt circuitry and the three counters of the 8254 (u1) counter/timer. The status of the interrupt latch is assigned to bit 7 of this location, and the status of counters 0, 1 and 2 are assigned to bits 0, 1 and 2, respectively (See table 6).

Table 6. Bit Configuration of Values Read from TIMER STATUS

D7	D6	D5	D4	D3	D2	D1	D0
INT	X	X	X	X	C2	C1	C0

Explanation:

X	Not used
INT Interrupt status	1 = Active interrupt 0 = No interrupt
C2 Counter 2 status	1 = Output line high 0 = Ouptut line low
C1 Counter 1 status	1 = Output line high 0 = Output line low
C0 Counter 0 status	1 = Output line high 0 = Output line low

If there is more than one device generating interrupts in the system, the interrupt processing routine must determine whether the interrupt received was generated by the Series 500 unit. Each time the Series 500 generates an interrupt, bit 7 of the TIMER STATUS location is set to 1. This bit is cleared to 0 when the CLEAR INT command is issued.

The other bits in this location are used in software delay routines. Each of these bits is set independently, and can be read separately. When a counter is first loaded, the bit is set to 1. Halfway through the count, the bit is set to 0, and at the terminal count, the bit is reset to 1. A delay routine waiting for the terminal count should first check for 0, and when 0 has been read, check for 1.

CLEAR INTERRUPT

Location: xxx62

This location is used to clear the interrupt status bit of the timer status location to 0, and is used in interrupt service routines to allow the generation of subsequent interrupts. It should be issued after saving the registers and assessing the source of the interrupt (see TIMER STATUS) but before other actions in the interrupt service routine. If this command is not issued, no further interrupts will be generated.

Writing any number to this location will clear the interrupt circuitry (0 is often used for convenience, but is not required).

USING QEMM WITH THE IBIN-PS/2

When using the IBIN-PS/2 in a computer running the "QEMM" memory manager, note the following:

1. The line in CONFIG.SYS which invokes QEMM should "exclude" the address range of the IBIN-PS/2. For instance, if the IBIN-PS/2 is located at 0CFF80(hex), a typical line might take the form:

   DEVICE = C:QEMM386.SYS **EXCLUDE CFF0-CFFF**

2. An error message advising "Unknown Microchannel ID 6571" may occur during boot-up. This error message is caused by the QEMM software being unable to recognize the IBIN-PS/2 card. QEMM contains a file which lists compatible microchannel cards. This file is called "MCA.ADL", and does not include the IBIN-PS/2. There are three solutions:

- You may simply ignore the error message and press <Enter> to continue.
- You may suppress the error message by adding No Pause On Error ("NOPE") to the "DEVICE = ..." line shown above:

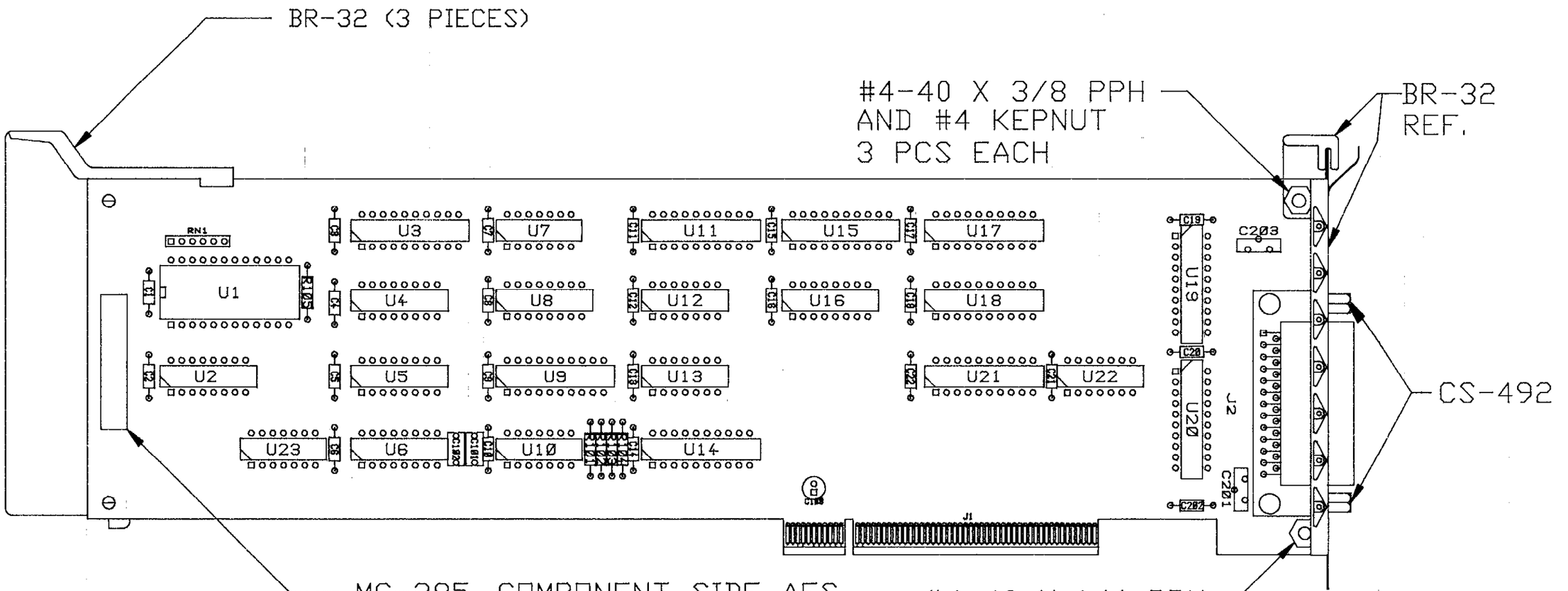
  DEVICE = C:QEMM386.SYS EXCLUDE CFF0-CFFF **NOPE**

- You may add the IBIN-PS/2 information to the MCA.ADL file. The QEMM manual contains instructions for this operation.

See your memory manager software documentation for specific details.

NO. 501-170

LTR	ECO NO.	REVISION	ENG.	DATE
E	14575	BOARD COMPLETELY RE-DESIGNED ADDED: R104,R105,C22,C203,U23 CHANGED: C201,U20	SAS	4-29-91



NOTE:
FOR COMPONENT INFORMATION, REFER TO
BILL OF MATERIALS 501-973

500	500-IBIN-PS2	1
MODEL	NEXT ASSEMBLY	QTY
USED ON		

DO NOT SCALE THIS DRAWING	DIMENSION TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 4-10-91	SCALE 1:1	TITLE COMPONENT LAYOUT SERIES 500 PS/2 INTERFACE
KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139	XX=+/-.015 ANG.=+/-1°	DRN. SAS	ENG. APPR.	
	XXX=+/-.005 FRAC.=+/-1/64	MATERIAL N/A	B	NO. 501-170
	SURFACE MAX. 63	FINISH N/A		

U15 74LS645 /READ

U5 74LS138

U3A U3B 74LS240

U11 74LS794

U12A U12B U12C U12D U13A U13B U13C U13D 74LS38

U19 74LS645

U21 74LS373 /DSTRB

R105 3.3K

5X3.9K RN1

U17 74LS794

U7B 74LS74

R103 4.7K /WRINT

U10D 74LS14

U10F 74LS14

U23A 74LS00

U20 74ALS533

J2

PCPWR PCGND

PINS 14,21 ARE PCPWR. THESE PINS SUPPLY POWER FOR THE ANALOG PWR SUPPLY ON EXTERNAL DEVICES. THIS PWR SHOULD BE ROUTED DIRECT FROM THE P82 EDGE CONNECTOR.

PIN 22 IS PCVCC. THIS PIN PROVIDES VCC PWR TO THE EXTERNAL DEVICES. THIS PWR SHOULD BE ROUTED FROM THE PWR GRID ON THIS ASSY.

PCVCC AND PCPWR SHOULD BE TIED TOGETHER AT THE P82 EDGE CONNECTOR ONLY TO REDUCE NOISE IN THE EXTERNAL EQUIPMENT TIED TO J2.

GND ON PINS 13,26 IS PCGND. THIS GND SHOULD BE RUN DIRECT TO THE P82 CONNECTOR EDGE TO MINIMIZE NOISE IN CHASSIS CONNECTED TO J2.

GND ON PINS 33,34 IS DGND. THIS GND SHOULD RUN TO THE GND NET OF THIS CIRCUIT DIRECTLY. DGND AND PGND SHOULD BE TIED TOGETHER ONLY AT THE P82 CONNECTOR EDGE.

J1

C103 10uF

U18 74LS688

U22 7430

U14 16L8

U9 16L8

U6A U6B 74LS139

U4 74LS175

U10C 74LS14

U7A 74LS74

U8 74LS153

U1 8254

U2 74LS367

U16 74LS163

U10E 74LS14

R102 1K

U10A 74LS14

C101 1500pF

R104 22

R101 1K

U10B 74LS14

C102 150pF

C201 C-386-270P

C202 .1uF

C203 C-386-270P

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11

C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22

C1..C22 .1uF BYPASS CAPS

UNUSED DEVICES

U23B U23C U23D 74LS00

KEITHLEY

KEITHLEY INSTRUMENTS CLEVELAND, OHIO 44139

TITLE

SERIES 500 PS/2 INTERFACE SCHEMATIC

SIZE	MODEL	NO.	ECO	REV
D	500	501-176	14575	E

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