7002 High Density Switch System

SYSTEM

CAPACITY: 10 plug-in cards per mainframe.

MEMORY: Battery backed-up storage for 500 switch patterns.

SWITCH SETTLING TIME: Automatically selected by the mainframe. For different switchcards, 7002 will be set to the slowest relay settling time. Additional time from 0 to 99999.999 seconds can be added in 1ms increments.

TRIGGER SOURCES:

External Trigger (TTL-compatible, 600ns minimum pulse, rear panel BNC).
IEEE-488 bus (GET, *TRG)
Trigger Link
Manual (front panel)
Internal Timer, programmable from 1.0ms to 99999.999 seconds in 1.0ms increments.

STATUS OUTPUT: Channel Ready (TTL-compatible signal, rear panel BNC). Low going pulse (10µs typical) issued after relay settling time.

SWITCHING SEQUENCE: Break-before-make (programmable).

MAINFRAME DIGITAL I/O: 4 open collector outputs (30V maximum, 100mA maximum sink current, 10Ω output impedance), 1 TTL compatible input, 1 common, 1+5V.

RELAY DRIVE: 3.5A maximum for all 10 card slots.

CARD SIZE: 32mm high × 114mm wide × 272mm long (1¼ in × 4½ in × 10¾ in).

CARD COMPATIBILITY: Fully compatible with all 7001 cards.

ANALOG BACKPLANE

SIGNALS: Four 3-pole rows (Hi, Lo, Guard). These signals provide matrix and multiplexer expansion between cards within one mainframe.

MAXIMUM VOLTAGE: 250V DC, 250V RMS, 350V AC peak, signal path to signal path or signal path to chassis.

MAXIMUM CURRENT: 1A peak.

PATH ISOLATION:

$>10^{10}\Omega$, <50pF path to path (any Hi, Lo, Guard to another Hi, Lo, Guard)
$>10^{10}\Omega$, <50pF differential (Hi to Lo or Hi, Lo to Guard).
$>10^{9}\Omega$, <75pF path to chassis.

CHANNEL CROSSTALK: <–65dB @ 1MHz (50Ω load).

BANDWIDTH: <3dB loss at 30MHz (50Ω load).

THROUGHPUT

EXECUTION SPEED OF SCAN LIST (channels or memory locations per second):

	CHANNELS	MEMORIES
Break-Before-Make	OFF 300	243
	ON 270	189

TRIGGER EXECUTION TIME (maximum time from activation of Trigger Source to start of switch open or close[2]):

SOURCE	LATENCY	JITTER
GET[1]	200 µs	<15 µs
*TRG[2,3]	3.0 ms	
Trigger Link	200 µs	<10 µs
External	200 µs	<10 µs
Timer		<25 µs

[1] Excluding switch settling time.

[2] Assuming no IEEE-488 commands are pending execution.

[3] Display Off.

IEEE-488 COMMAND EXECUTION TIME

COMMAND	EXECUTION TIME[1]
CLOS (@1!1)	<8ms + Relay Settle Time
OPEN (@1!1)	<8ms + Relay Settle Time
MEM:REC M1	<9ms + 2×Relay Settle Time (BBM ON) < 9ms + Relay Settle Time (BBM OFF)

[1] Measured from the time at which the command terminator is taken from the bus to relay energize. With display OFF.

GENERAL

DISPLAY: Dual-line vacuum fluorescent. 1st line: 20-character alphanumeric. 2nd line: 32-character alphanumeric. Channel status LED grid.

LIGHT PEN OPTION: Provides interactive programming of channels, cross points, scan lists, and memory.

REAR PANEL CONNECTORS:

IEEE-488; 9-pin DB9 Female; 8-pin micro DIN for Trigger Link; 8-pin micro DIN for Trigger Link expansion; BNC for External Trigger; BNC for Channel Ready

POWER: 100V to 240V rms, 50/60Hz, 110VA maximum.

EMC: Complies with European Union Directive 89/336/EEC, EN61326-1.

SAFETY: Conforms to European Union Directive 73/23/EEC, EN61010-1.

EMI/RFI: Meets VDE 0871B and FCC Class B.

ENVIRONMENT: Operating: 0°C to 50°C, <80% RH (0°C to 35°C). **Storage:** –25°C to +65°C.

DIMENSIONS, WEIGHT: 178mm high × 438mm wide × 448mm deep (7 in × 17¼ in × 17⅝ in). Net weight 9.1kg (20 lb).

IEEE-488 BUS

STANDARDS CONFORMANCE: Conforms to SCPI-1990, IEEE-488.2 and IEEE-488.1.

MULTILINE COMMANDS: DCL, LLO, SDC, GET, GTL, UNT, UNL, SPE, SPD.

UNILINE COMMANDS: IFC, REN, EOI, SRQ, ATN.

INTERFACE FUNCTIONS: SH1, AH1,T5, TE0, L4, LE0, SR1, RL1, PP0, DC1,DT1, C0, E1.

Specifications subject to change without notice.

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