KEITHLEY INSTRUMENTS, INC.

MODEL 720

VARIABLE APERTURE INTEGRATING
ANALOG TO DIGITAL CONVERTER

INSTRUCTION MANUAL

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INSTRUCTION MANUAL

Model 720

Variable Aperture Integrating
Analog to Digital Converter

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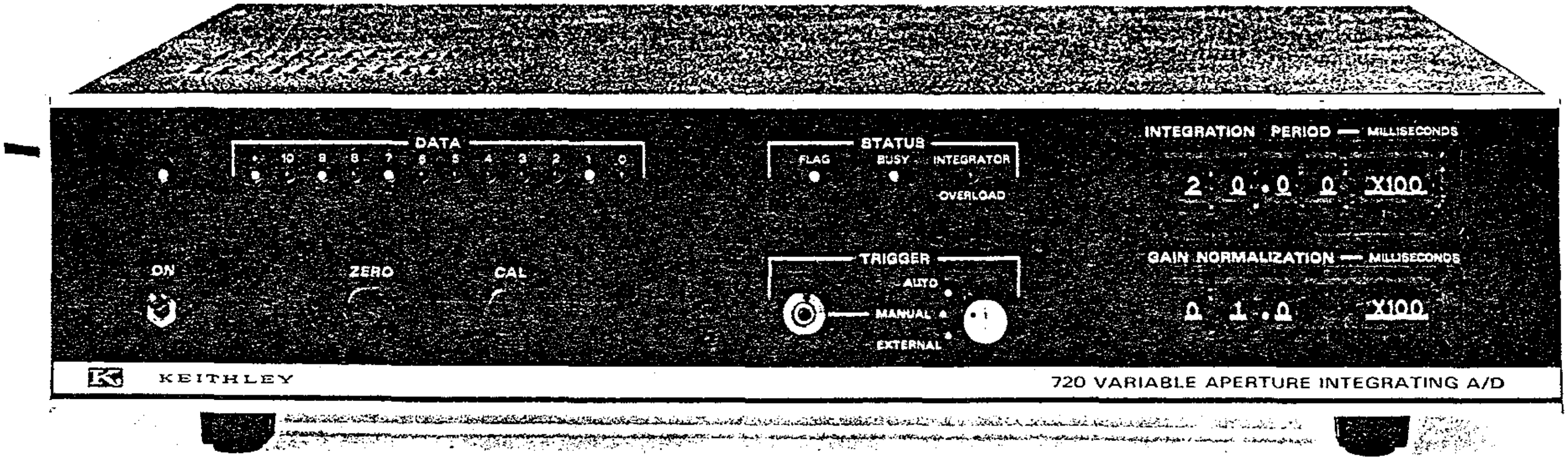
MODEL 720

The Model 720, a Variable Aperture Integrating Analog to Digital Converter, is designed to do analog signal preprocessing more efficiently and with greater ease and flexibility than using conventional high speed sampling and numerical signal processing techniques. The digital interface has been structured for straightforward interfacing.



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Specifications

Model 720

Variable Aperture Integrating A/D

Calibrated at 25°C±3°C
Warranted for 1 Year

Input:	Gain times average level must not exceed 2 volts for on-scale indication.
Input Impedance:	9 kilohms to 100 kilohms.
Maximum Allowable Input:	150 Volts rms for a gain normalization setting greater than 05.7 decreasing to 20 Volts rms for the gain normalization setting of 00.1.
Gain:	Adjustable from 10^{-4} to 10^{3}. Nominal gain equals Integration Period divided by Gain Normalization. Absolute gain (digital bits per volt) is continuously adjustable with front panel trim.
Linearity:	±0.1% of full range.
Integration Period:	1 millisecond to 10 seconds settable in 10 microsecond, 100 microsecond, or 1 millisecond steps with front panel controls.
Integration Period Accuracy (90 Days):	±(0.01% + 2 microseconds).
Integration Period Stability:	±0.002%/°C; ±0.0001%/day.
Gain Normalization:	1 millisecond to 10 seconds settable in 100 microsecond, 1 millisecond, or 10 millisecond steps with front panel controls.
Gain Normalization Accuracy (90 days):	±0.4% between switch settings.
Gain Normalization Stability:	±0.05%/°C
Zero Stability:	±0.08% of full range/°C; ±0.05% of full range/day after 1 hour warm-up.
Reset Period:	300 microseconds. May be internally adjusted to 150 microseconds when X100 Gain Normalization multiplier is not used.
CMRR:	100dB dc to 200Hz, 80dB to 10kHz.
NMRR:	For $f=n/T_I$, greater than 60dB at $T_I \geq$ 10 milliseconds, decreasing to 40dB at T_I = 1 millisecond, where f is frequency, T_I is integration period, and n is an integer. For all other $f>1/T_I$, NMRR $\geq$ 9dB + 20dB per decade to a maximum of 60dB.

Display: 11 data bits, polarity, busy, integrator overload, flag, and power on.

Trigger: Front Panel switch selects:

Manual: Front panel trigger initiates one conversion.

Automatic: Continuous conversion internally triggered at the end of the reset period.

External: External trigger initiates one conversion.

Digital Output: Data: Offset binary positive logic represents each of 11 data bits and polarity (+ = "1").

Flag ($\overline{\text{Flag}}$): Logic "1" ("0") appears for greater than 1 millisecond (depending on integration period). No change in output data is made during this interval.

Integrating: Logic "1" during integration.

Integrator Overload: Logic "1" (appearing with data output) indicates an overload occurred during integration.

Busy: Logic "1" during integration, A/D conversion, and reset periods.

Control Settings: BCD (8421) positive logic represents each of 4 digits of Integration Period control setting, each of 3 digits of Gain Normalization control setting, Integration Period multiplier setting (2-bit code), Gain Normalization multiplier setting (2-bit code), trigger setting (2-bit code).

Output Logic Levels: Logic "1" ≡ open collector to Digital Lo. (10 kilohm pull-up resistor to +5 volts installed. May be customer removed.)

Logic "0" ≡ closure to Digital Lo(output device MC858P or equivalent).

Remote Controls: External Trigger: Transition from Logic "1" to Logic "0" initiates one conversion. Integration begins within 2 microseconds after transition. (Input device 7413 or equivalent.)

Integrate: Transition from Logic "1" to Logic "0" initiates integration within 1 microsecond. Transition from Logic "0" to Logic "1" terminates integration within 1 microsecond and initiates A/D conversion and reset. (Input device 7413 or equivalent).

Remote Controls (Cont'd.):

Flag ($\overline{\text{Flag}}$) Reset: Logic "0" resets Flag ($\overline{\text{Flag}}$) to logic "0" ("1"). Flag reset state held until the first end-of-conversion after release.

Strobes: 14 lines for serializing all outputs except Busy in multiples of 4 bits. Logic "1" inhibits controlled output lines.

Control Logic Levels: Logic "1" ≡ either an open circuit or a voltage between 3.0 and 5.5 volts referenced to Digital Lo.

Logic "0" ≡ closure to Digital Lo within 0.5 volt while sinking 2.5 milliamperes.

Isolation: Analog Lo to Digital Lo: 10^7 ohms shunted by 1500 picofarads, 500 volts peak.

Digital Lo to Chassis Ground: 10^5 ohms shunted by 0.01 microfarads. Isolation is sufficient to accommodate operating system ground differentials.

Operating Environment: 15°C to 35°C, 0% to 80% relative humidity. Storage: -30°C to 70°C.

Power: 90-110, 105-125, 195-235, or 210-250 volts (switch selected), 50-60Hz, 75 watts.

Connectors: Input: Teflon insulated triaxial.

Output: 2 connectors; 37-pin AMP type 205209-1 and 50-pin AMP type 205211-1.

Digital Lo, Chassis Ground: binding posts.

Analog Lo: Banana jack.

Dimensions, Weight: Style M 3½ in. full-rack, overall bench size 4 in. high x 17¼ in. wide x 15½ in. deep (100 x 435 x 390 mm); net weight 17 pounds (7,4 kg).

Accessories Furnished: Model 6011 input cable: 3 ft. (1 m) triaxial cable with triaxial connector and three alligator clips. Mating Output connectors; hardware for standard 3½ in. x 19 in. rack mounting, 15½ in. (390 mm) depth behind front panel.

Accessories Available:

- Model 1532 Low-Thermal Test Leads ....
- Model 1533 Mating Connector: for Special Triaxial Input.................
- Model 1534 Special Low-Thermal Triaxial Cable (10 ft.).........................
- Model 6011 Input Cable (extra) ....
- Model 7024-3 Triax-to-triax(3 ft)........
- Model 7024-10 Triax-to-triax(10 ft)......
- Model 7801-720 Instrument Interface to System 1...........................
- Model 720 Variable Aperture Integrating A/D.......................
- Model 6012 Triax to Coax VHF Adaptor ....

MODEL 720 - VAI A/D

OPERATING INSTRUCTIONS

GENERAL:

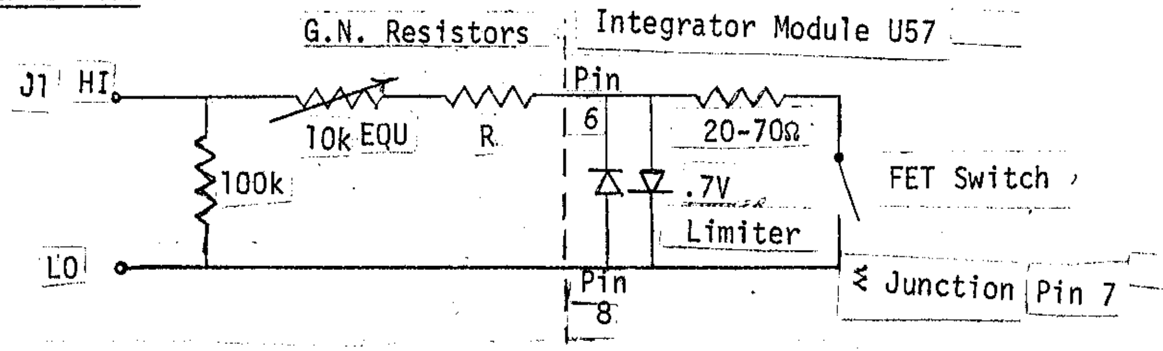
The Model 720 implements the following equation:

$$V_{out} = \frac{1}{\text{Gain Normalization}} \int_0^{T_{integration}} V_{in}(t)\,dt$$

For example; if G.N. and T_I are equal and 1 volt is applied to the input, V_o will read 1000 (millivolts). If G.N. is twice T_I, V_o will read 500 millivolts.

The output is calibrated for 1 millivolt/bit or 2047 to -2048 full scale. However using the front panel gain adjustment full scale can be adjusted to ±2000, i.e., ±2 volts full scale.

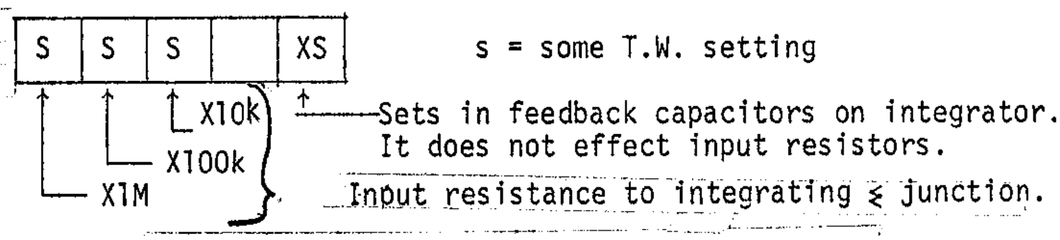
INPUT IMPEDANCE



This schematic shows the equivalent input circuit of the 720. The value of R depends on the Gain Normalization setting (see below). The FET switch is closed only during the integrating period and open at all other times.

The gain normalization (G.N.) thumbwheel (T.W.) switch controls the G.N. resistors. The G.N. circuit subtracts 10k from the switch setting and relays short out the unwanted resistors. The total resistance to the FET switch is the G.N. resistance plus the 10kΩ equivalent resistance. (The 10kΩ equivalent resistance prevents zero resistance to be switched in.) This total resistance is indicated by the G.N. T.W. switch as shown below.

Gain Normalization T.W. Switch



Example: If you have 010 XS on the G.N. TW switch the resistance to the integrator will be 100k.

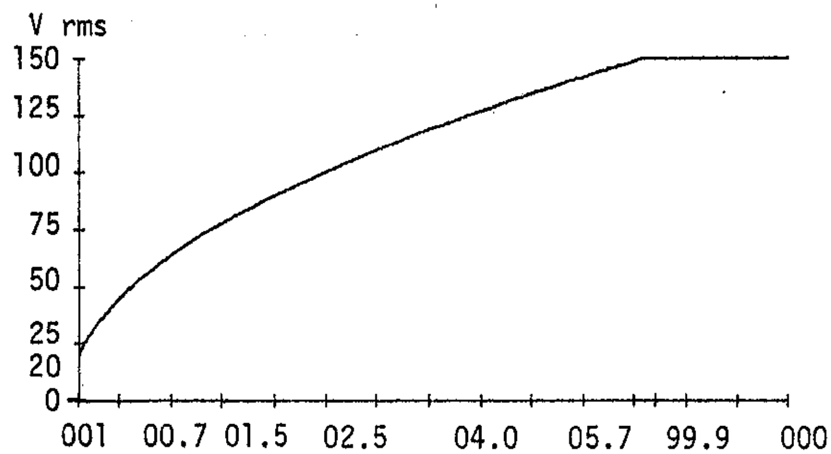
A 000 XS on the TW switch = 10Mohm to the integrator.

Input impedance will range from approximately 9kohm to 100kohm depending on G.N. settings.

MAXIMUM ALLOWABLE INPUT VOLTAGE VS G.N. SETTINGS:

Voltages from 0 to 150V rms can be applied to the input depending on the gain normalization switch settings. 0 to 20V rms can be applied, using any G.N. setting. Voltages greater than 20 V rms up to 150 V rms can be applied with a certain minimum G.N. setting or greater.

The following graph shows input voltage vs. minimum G.N. T.W. switch setting:



EXAMPLE: If 125 volts rms is applied to the input, the minimum G.N. setting will be 04.0. However, settings greater than this can be used. The G.N. switch multiplier has no effect on the input resistors.

The following formula can be used to find the minimum G.N. setting for a specific voltage greater than 20 volts rms.

G.N. TW switch setting = $\frac{V^2}{4000}$ V = input voltage in volts rms.

EXAMPLE: For an input voltage of 150 V rms, the minimum G.N. switch setting will be:

Minimum G.N. setting = $\frac{(150)^2}{4000}$ = 5.625

G.N. setting = 5.7 (rounding up to one decimal place)
Then G.N. setting should be set to 05.7 ms.

Voltages greater than 150 V rms will permanently damage the 100 kohm shunt resistor. The integrator input resistors should never be allowed to dissipate more than 40 milliwatts.

IMPORTANT: To change the gain normalization T.W. switch settings with an input voltage greater than 20 V rms, turn the trigger switch to the manual position and wait until unit stops integrating. Then change the settings and return trigger switch to position you were using. The next conversion will be with the old T.W. settings. The 2nd conversion will be with the new settings.

MODEL 720 FRONT PANEL DESCRIPTION

1. ON SWITCH - Turns on line power to the Model 720.

2. POWER INDICATOR - Indicates line power on.

3. DATA - Lamps indicate status of data output register lines. At low values of Integration Period, lamps may appear dimly lighted due to data shifting into output register.

4. STATUS:

   Flag - Indicates valid data available on Data Lamps and output lines. Reset by Flag Reset or new data shifting into output register. Appears to be always on unless Flag Reset is used.

   Busy - Indicates that the Model 720 is integrating, converting or resetting the integrator. Busy off indicates that 720 will accept a trigger. With TRIGGER in AUTO, lamp appears always on.

   Integrator Overload - Indicates that integrator has overloaded on the previous integration and therefore output data may not be invalid. The integrator has twice the dynamic span of A/D and therefore a ± full scale converter output is easily possible without overloading the integrator. Integrator Overload appears in the data stream with the DATA.

5. TRIGGER:

   Auto - This position sets the Model 720 for continuous operation with an internal trigger generated at the end of each integrator reset period.

   Manual - This position activates the front panel TRIGGER push-button. When depressed the button triggers the Model 720 (if BUSY STATUS lamp is not on).

   External - This position activates the external trigger on rear panel DATA connector. EXT TRIGGER is enabled when BUSY line is at LOGIC "0".

6. INTEGRATION PERIOD- Sets the Integration Period from 1.00 ms to 9.999 seconds. It is possible to set values less than 1.0 ms, but some specifications may degrade. Multiplier has 4 positions: X1, X10, X100, EXT. EXT activates the EXTERNAL INTEGRATE line on the DATA connector.

7. GAIN NORMALIZATION- Sets the normalization from 1.0 ms to 9.99 seconds. Multiplier has 3 positions: X1, X10, X100.

MODEL 720 REAR PANEL DESCRIPTION

1. Analog Input - Triaxial connector with:
   *Center - High
   *Inner Shield - Analog Lo
   *Shell - Chassis GND
   Triaxial connectors and cable must be used for safety if analog Lo is not at chassis ground.

2. Banana Jack: *Analog Lo (Black) - connects to inner shield of analog input
   Binding Posts: *Digital Lo (Blue) - connects to output logic common (on Output Connectors)
   *Chassis Ground - Connects to chassis & power line ground

3. Output (see output information)
   Data - 37 pin connector
   Control - 50 pin connector

4. Power Line Voltage Selection Switches with four positions:

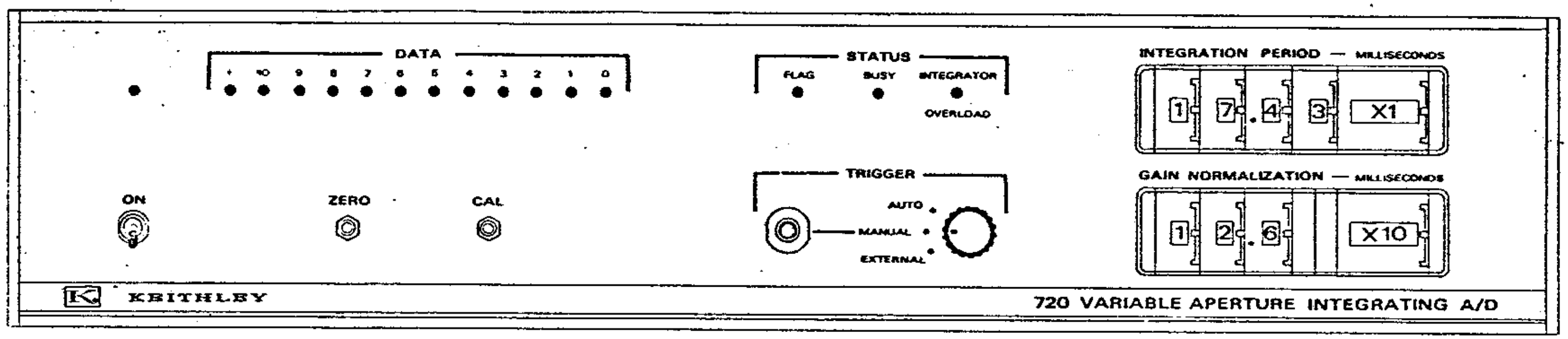
   90 to 110 volts
   105 to 125 volts
   195 to 235 volts
   210 to 250 volts

   CAUTION: Select proper power line voltage before connecting line cord.

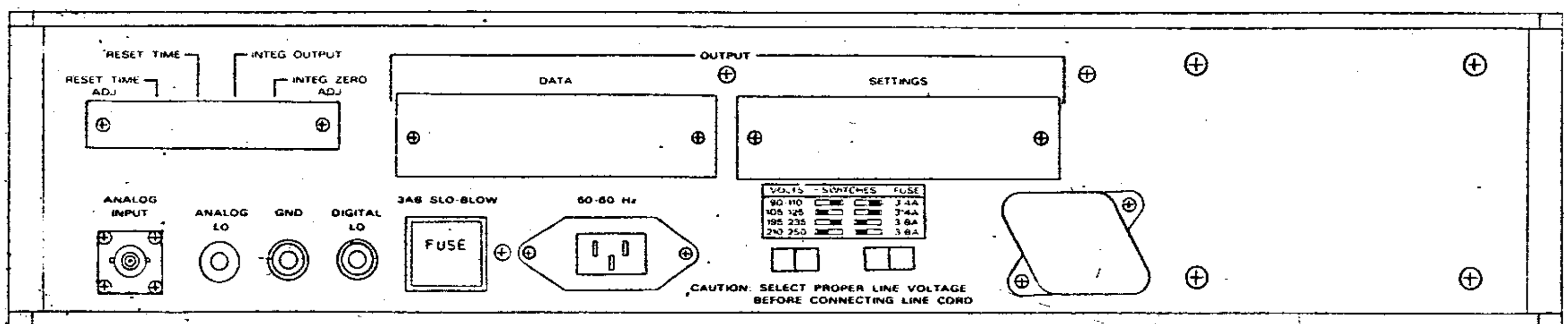
5. Line Cord Connector

6. Fuse - 100 volts & 115 volts - 3AB Slo Blo Fuse 3/4A 230 volts and 215 volts - 3AB Slo Blo Fuse 3/8A

7. Insulating Cover Over Power Supply Regulator transistor.



FRONT PANEL



REAR PANEL

CONTROL SETTING CONNECTOR

STROBES (Input)

A logic zero on a strobe line enables the appropriate output bits. All lines have to be strobed except BUSY. All strobed output lines are at logic 1 when respective strobes are not activated.

INTEGRATION PERIOD

The output information corresponding to the Integration Period Thumb-Wheel settings is composed of four (4) BCD digits plus a multiplier code given by:

Integration Period Multiplier Codes

	'A'	'B'
X1	0	0
X10	1	0
X100	0	1
EXT	1	1

The code can be thought of as the 2 least significant of a BCD exponent, i.e., Integration Period x 10^{xxBA}.

INTEGRATION PERIOD MULTIPLIER

See Integration Period.

GAIN NORMALIZATION

The output information corresponding to the Gain Normalization T.W. settings is composed of 3 BCD digits plus a multiplier code given by:

Gain Normalization Multiplier

	'A'	'B'
X1	0	0
X10	1	0
X100	0	1

The code can be thought of as the 2 least significant bits of a BCD exponent, i.e., Gain Normalization x 10^{BA}.

GAIN NORMALIZATION MULTIPLIER

See Gain Normalization

DIGITAL LO

Digital Lo is the output Logic common. Numerous pins are provided for interfacing ease and to reduce ground resistance. Digital Lo is also provided as a binding post on the rear panel.

DATA & POLARITY

The output code is positive true offset binary, for example:

	Polarity Bit
+F.S.	111-----1
0	100-----0
-1	011-----1
-F.S.	000-----0

DATA is guaranteed valid when FLAG is logic 1.

POLARITY

See DATA.

FLAG ($\overline{\text{FLAG}}$)

FLAG in logic state 1 indicates when the DATA, POLARITY, or INTEGRATOR OVERLOAD lines are valid. FLAG and the above lines become valid concurrently. FLAG may be (prematurely) reset externally or (OR) will be reset internally when the above lines are not valid. Reset pulse should be typically 200 nanoseconds minimum.

STROBES

See Strobes on Control Setting Connector.

+5 VOLTS

The output logic supply is provided for ease of interfacing. The unit has a 150Ω resistor in series with the supply. The user may jumper this resistor. The user may typically draw 200mA from these terminals.

INTEGRATING

This line is in a logic 1 state during the integration portion of the cycle.

INTEGRATOR OVERLOAD

Integrator overload appears with the DATA and POLARITY. When this line is valid and in a logical 1 state, it indicates that the integrator has overloaded during the previous integration.

BUSY

The BUSY line is at a logical 1 when the 720 is integrating, converting, or resetting. When the BUSY line is at logic zero and 720 is prepared to accept a trigger, either (EXTERNAL MANUAL or AUTO as selected by the front panel switch). NOTE: In AUTO mode the BUSY line will assume logical zero for 0.5 to 1.5 microseconds between the start of the next integration and the end of the previous reset portion of the 720 cycle.

FLAG RESET

Logic level zero resets FLAG to logical zero. The reset state is held until the first end of the conversion state after release. The FLAG RESET is used to prevent multiple collection of the previous conversion results.

EXTERNAL INTEGRATION PERIOD (ON INTEGRATION PERIOD MULTIPLIER SWITCH)

Logic level zero initiates integration. Logic level one terminates integration. The state of this input will not be recognized again until the end of the reset portion of the 720 cycle. This line should be in the logic 1 state for typically 200 nanoseconds minimum.

EXTERNAL TRIGGER

A transition from a logic 1 to a logic 0 after the falling edge of the BUSY line initiates one 720 cycle of integration, conversion and reset within 1 microsecond. Typically trigger must remain in logic level zero for 200 nanoseconds minimum. The line must also be in logic level one for 200 nanoseconds minimum typically before the logic 1 to "0" transition. The line may otherwise remain in either state indefinitely.

TRIGGER SETTING

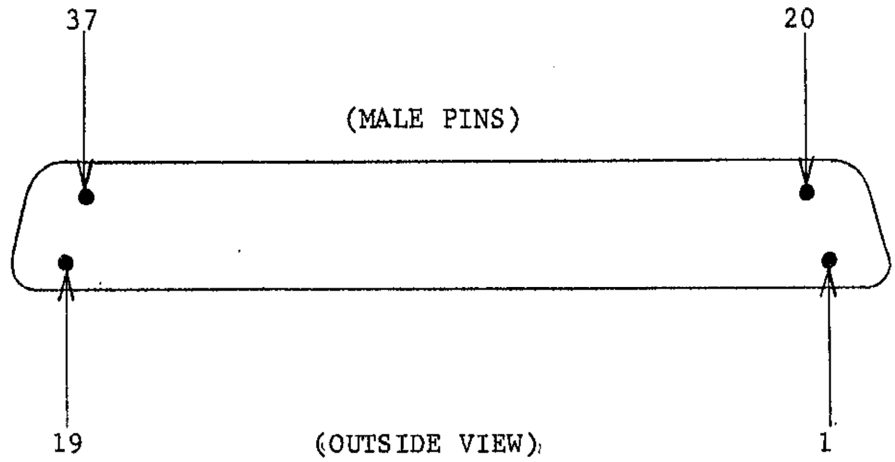
The position of the front panel trigger switch is indicated by the following code:

	'A'	'B'
AUTO	0	0
MANUAL	1	0
EXTERNAL	0	1

DIGITAL LO

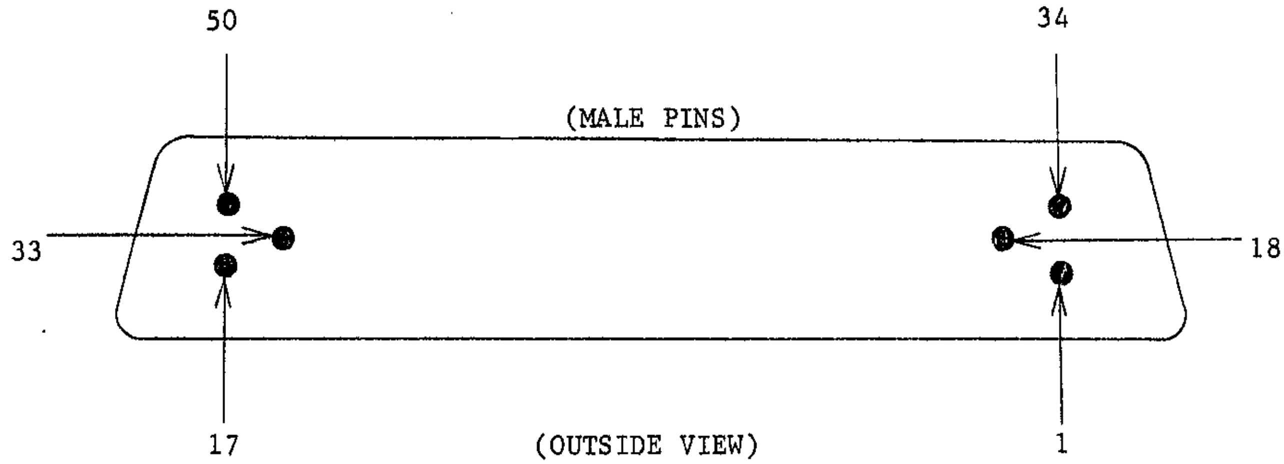
See DIGITAL LO on Control Setting Connector.

MODEL 720
REAR PANEL
DATA CONNECTOR



PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	DATA 0 (A)	20	+5 VOLTS
2	DATA 1 (A)	21	+5 VOLTS
3	DATA 2 (A)	22	+5 VOLTS
4	DATA 3 (A)	23	+5 VOLTS
5	DATA 4 (B)	24	+5 VOLTS
6	DATA 5 (B)	25	INTEGRATING (D)
7	DATA 6 (B)	26	INT. OVERLOAD (D)
8	DATA 7 (B)	27	BUSY
9	DATA 8 (C)	28	FLAG RESET
10	DATA 9 (C)	29	EXT. INT. PERIOD
11	DATA 10 (C)	30	EXT. TRIGGER
12	POLARITY (+=1) (C)	31	TRIGGER SETTING 'A' (E)
13	FLAG (D)	32	TRIGGER SETTING 'B' (E)
14	$\overline{\text{FLAG}}$ (D)	33	DIGITAL LO
15	STROBE (A)	34	DIGITAL LO
16	STROBE (B)	35	DIGITAL LO
17	STROBE (C)	36	DIGITAL LO
18	STROBE (D)	37	DIGITAL LO
19	STROBE (E)		

KEITHLEY INSTRUMENTS, INC.
MODEL 720
REAR PANEL
CONTROL SETTING CONNECTOR



PIN NO.	SIGNAL NAME		PIN NO.	SIGNAL NAME	
1	STROBE F		26	INT. PERIOD MULT. 'A'	F
2	INT. PERIOD $1X10^{-2}$	G	27	INT. PERIOD MULT. 'B'	F
3	INT. PERIOD $2X10^{-2}$	G	28	GAIN. NORM. $1X10^{-1}$	L
4	INT. PERIOD $4X10^{-2}$	G	29	GAIN. NORM. $2X10^{-1}$	L
5	INT. PERIOD $8X10^{-2}$	G	30	GAIN. NORM. $4X10^{-1}$	L
6	INT. PERIOD $1X10^{-1}$	H	31	GAIN. NORM. $8X10^{-1}$	L
7	INT. PERIOD $2X10^{-1}$	H	32	GAIN. NORM. MULT. 'A'	P
8	INT. PERIOD $4X10^{-1}$	H	33	GAIN. NORM. MULT. 'B'	P
9	INT. PERIOD $8X10^{-1}$	H	34	DIGITAL LO	
10	INT. PERIOD $1X10^{0}$	J	35	DIGITAL LO	
11	INT. PERIOD $2X10^{0}$	J	36	DIGITAL LO	
12	INT. PERIOD $4X10^{0}$	J	37	DIGITAL LO	
13	INT. PERIOD $8X10^{0}$	J	38	DIGITAL LO	
14	INT. PERIOD $1X10^{1}$	K	39	DIGITAL LO	
15	INT. PERIOD $2X10^{1}$	K	40	DIGITAL LO	
16	INT. PERIOD $4X10^{1}$	K	41	DIGITAL LO	
17	INT. PERIOD $8X10^{1}$	K	42	DIGITAL LO	
18	STROBE G		43	GAIN. NORM. $1X10^{0}$	M
19	STROBE H		44	GAIN. NORM. $2X10^{0}$	M
20	STROBE J		45	GAIN. NORM. $4X10^{0}$	M
21	STROBE K		46	GAIN. NORM. $8X10^{0}$	M
22	STROBE L		47	GAIN. NORM. $1X10^{1}$	N
23	STROBE M		48	GAIN. NORM. $2X10^{1}$	N
24	STROBE N		49	GAIN. NORM. $4X10^{1}$	N
25	STROBE P		50	GAIN. NORM. $8X10^{1}$	N

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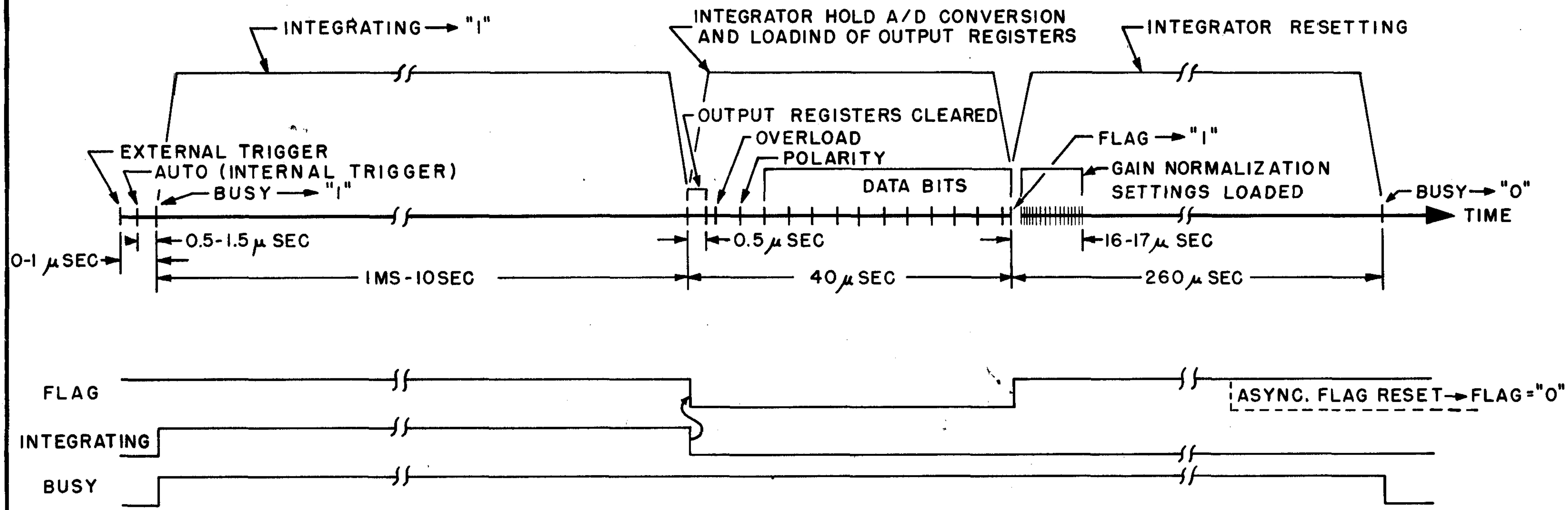


MODEL	NEXT ASSEMBLY	QTY.
USED ON		

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 1-17-76	SCALE NONE	TITLE MODEL 720 TIMING DIAGRAM
KEITHLEY INSTRUMENTS CLEVELAND, OHIO	XX = ± .015 ANG = ± 1	DRN D. J. K.	ENG APPR DJA	
	XXX = ± .005 FRAC = ± 1/64	MATERIAL		NO 28200 B
	SURFACE MAX 63	FINISH		

INTERFACE EXAMPLE

INTRODUCTION

This example interface is presented to demonstrate a technique of using the Model 720 with a 16-bit minicomputer. One 16-bit general purpose I/O register was allocated to the 720. The entire interface is a cable - - no logic packages or components were used. The operating system of the example PDP-11 is BASIC with an assembly language patch (external function). Many of the routines of BASIC (similar to standard routines available in a floating point package) were utilized to simplify the coding. Only the actual 720 subroutine is discussed, not the linkage to BASIC.

SOFTWARE

The higher level language instruction that was used was CALL (14, A, B, V). The first number in the parenthesis, 14, is the label for this particular subroutine. As the routine is entered, the output register is cleared and then the rest of the CALL statement is evaluated. The statement is continued to be scanned until a comma is found. The string "A" or the variable "A" is evaluated by an existing subroutine. After it is evaluated, it is tested to verify it is within allowable limits and then stored.

The scan continues to the next comma and similarly the delay between readings, "B", is evaluated, tested and stored. Finally the starting address of the array or variable to be filled is found and stored.

The BUSY bit is tested. If it is LO a word is outputed to zero the appropriate bit to trigger a conversion. The first strobe for the Data Word is activated in anticipation.

While the Model 720 is integrating the flag bit is tested until it goes Hi, at which time the Data Word is inputed. Next a program is tested to check which characters had been put in a buffer from an interrupt.

The number of readings is decremented and tested. If the required number of readings has not been met the program jumps to a delay subroutine which in this case was a real time clock.

Upon completion of the loop the thumbwheels are inputed. The appropriate strobes are activated, the BCD digits are inputed, these are made into ASCII characters and put into a string. When the string is complete the existing ASCII to floating point converter routine is called.

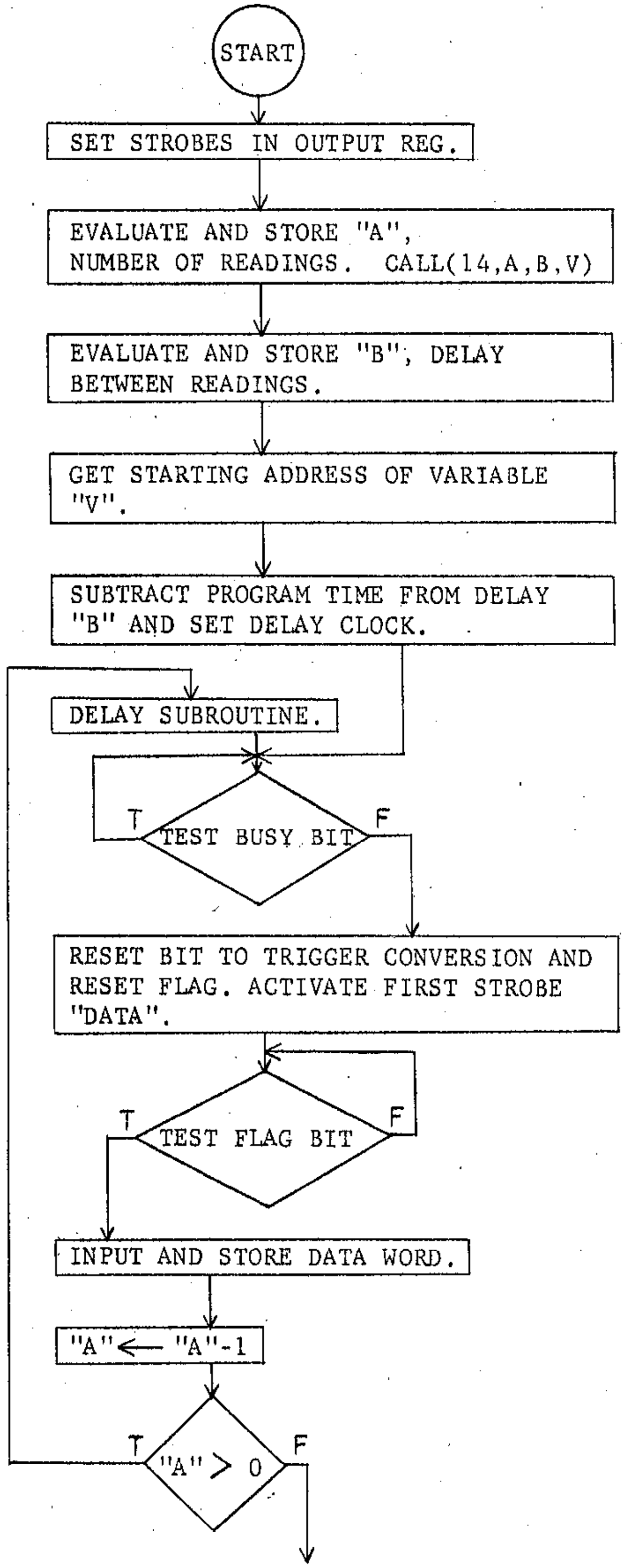
Now all the information has been inputed and there is time available to process the Data Words. The appropriate bits are tested for, stripped of and/or set to form a binary integer. The existing binary integer to floating point routine is called. The pointers are updated and tested for completion of the Data Word conversion, where the subroutine is now finished.

HARDWARE

The Model 720 was connected to a DEC DR-11A general purpose I/O interface consisting of one 16-bit input port, one 16-bit output register and 2 request lines which can be tested by the program.

The inputs are TTL. The outputs are open collector. The appropriate strobe and output lines from the Model 720 were wired "OR"ed in the connectors mating to the Model 720. The cable consisted of 40 feet of 50 conductor ribbon cable with alternate lines grounded. Depending on the programming, the alternate grounds may not be necessary. The only pull-up resistors used were the internal 10kΩ pull-up resistors internal to the Model 720. No hardware other than the cable was used for the interface.

DATA COLLECTION



NEXT PAGE

ACTIVATE SECOND STROBE, "INT. PERIOD".

↓

INPUT THE SECOND MOST SIG. DIGIT OF, "INT. PERIOD".

↓

MAKE ASCII CHARACTERS AND PUT INTO STRING.

↓

ACTIVATE THIRD STROBE, "INT. PERIOD".

↓

INPUT THIRD DIGIT.

↓

MAKE INTO ASCII. PUT DECIMAL PT., THIRD DIGIT, INTO STRING.

↓

ACTIVATE FOURTH STROBE.

↓

INPUT LEAST SIG. DIGIT OF, "INT. PERIOD".

↓

MAKE INTO ASCII. PUT FOURTH DIGIT AND "E" FOR EXPONENT INTO STRING.

↓

ACTIVATE FIFTH STROBE, "MULTIPLIER".

↓

INPUT MULTIPLIER CODE.

↓

MAKE INTO ASCII AND PUT INTO STRING.

↓

SET UP POINTERS AND CALL ASCII TO FLOATING POINT SUBROUTINE.

↓

ACTIVATE SIXTH STROBE, GAIN. NORM. MOST SIG. DIGITS.

↓

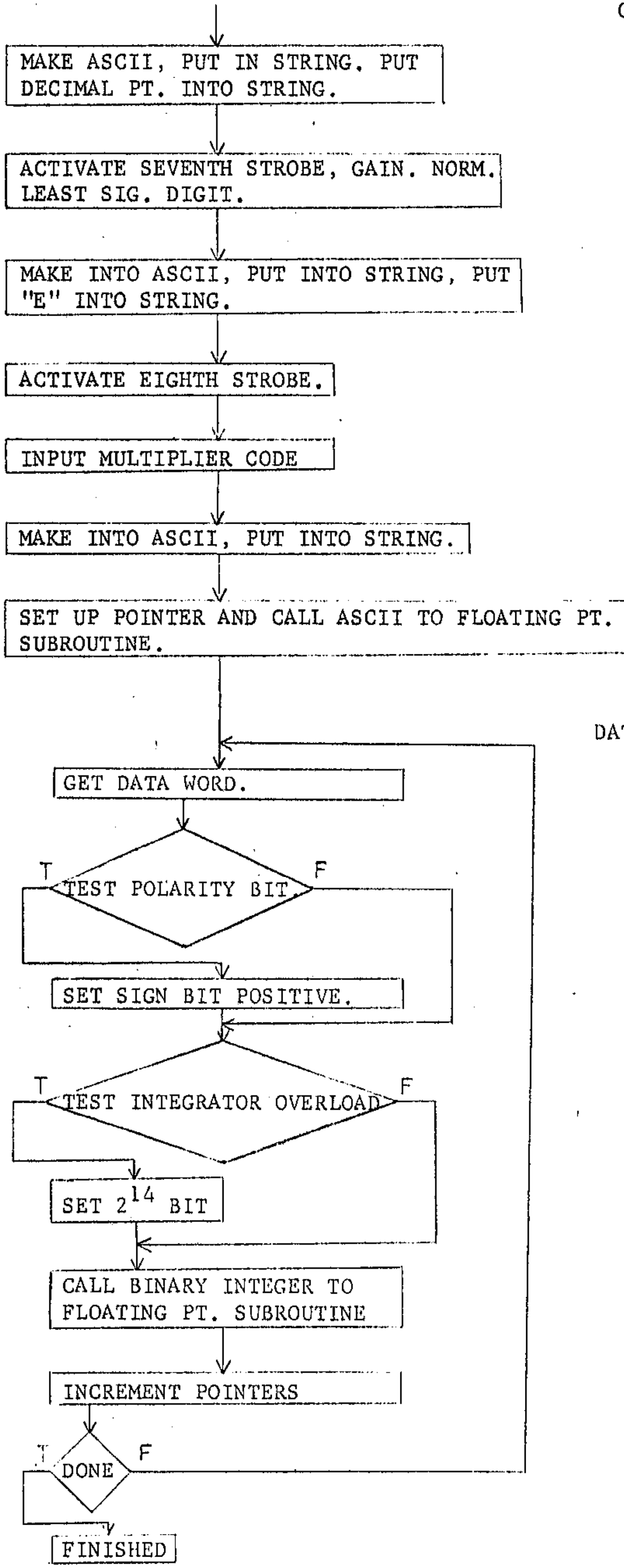
INPUT MOST SIG. DIGITS.

↓

NEXT PAGE

CONTROL SETTINGS

DATA WORD CONVERSION



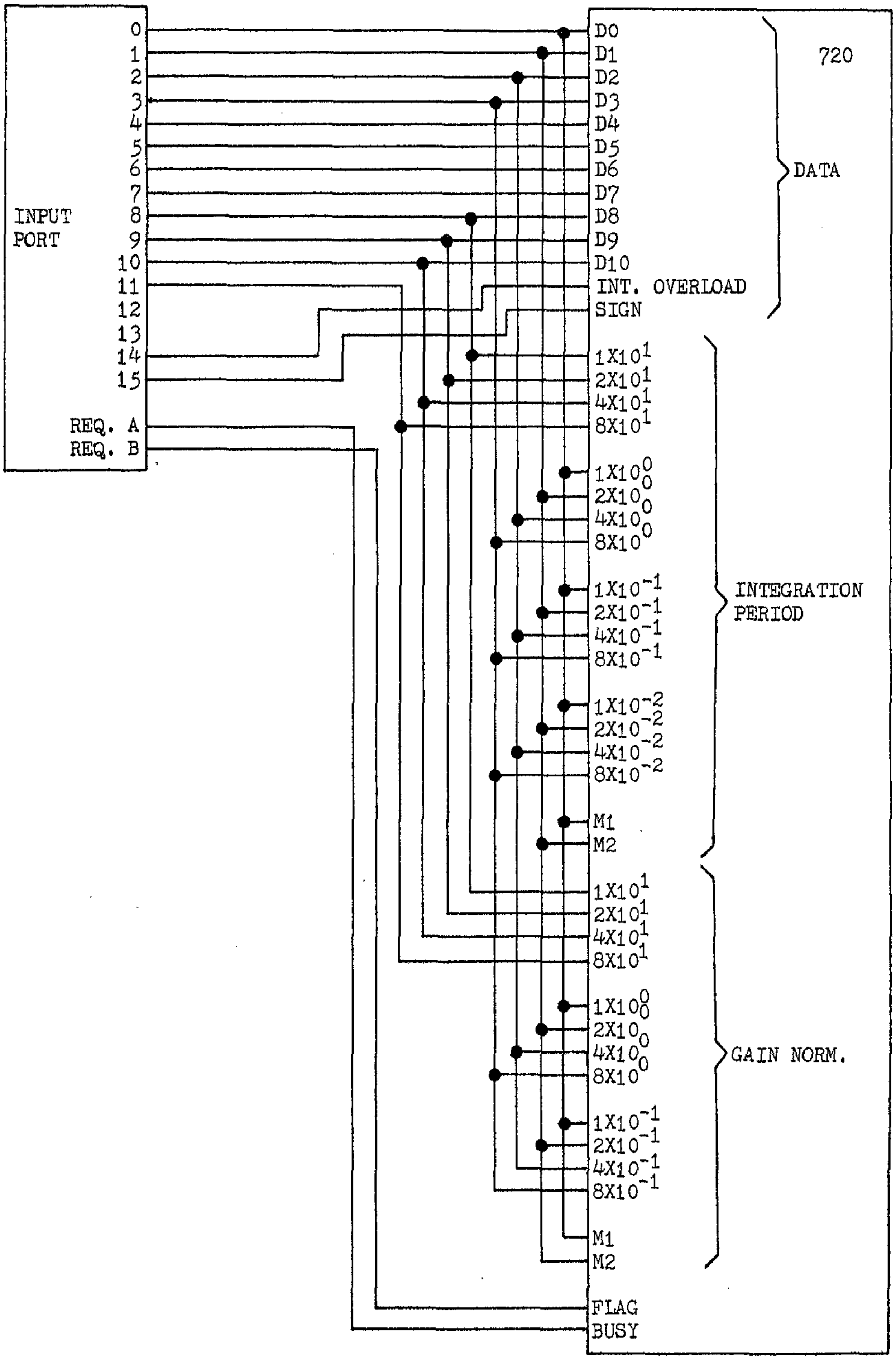
MULTIPLEXING FORMAT

OUTPUT REGISTER (DR 11 A) TO 720

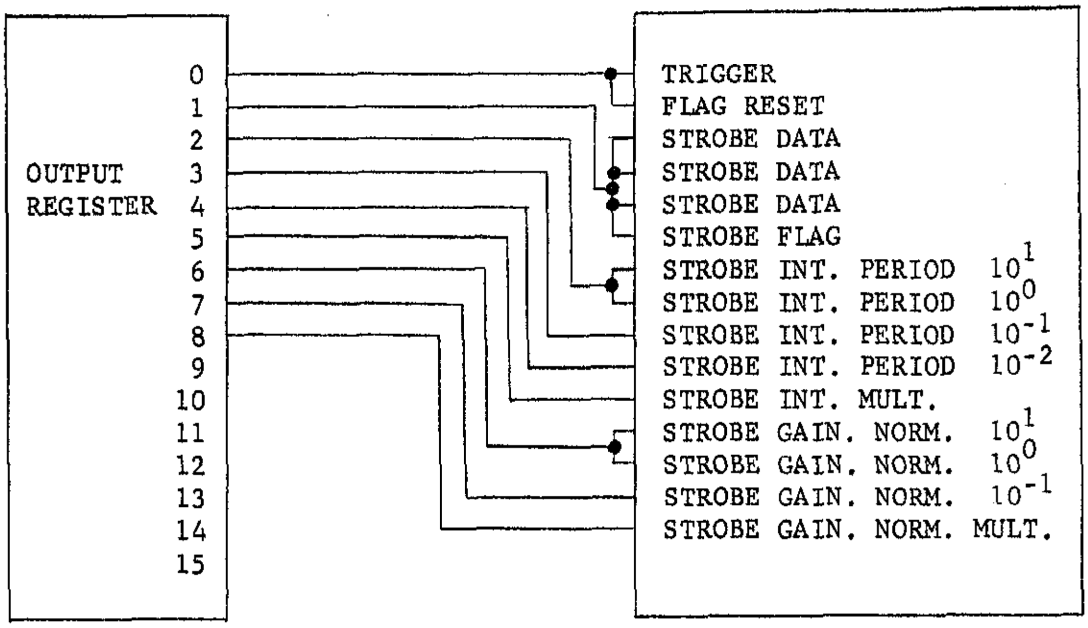
OUTPUT BITS	SET STROBES	#1	#2	#3	#4	#5	#6	#7	#8	TRIG. AND FLAG RESET
0	1	1	1	1	1	1	1	1	1	0
1	1	0	1	1	1	1	1	1	1	1
2	1	1	0	1	1	1	1	1	1	1
3	1	1	1	0	1	1	1	1	1	1
4	1	1	1	1	0	1	1	1	1	1
5	1	1	1	1	1	0	1	1	1	1
6	1	1	1	1	1	1	0	1	1	1
7	1	1	1	1	1	1	1	0	1	1
8	1	1	1	1	1	1	1	1	0	1
9	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	0
OCTAL	777	775	773	767	757	737	677	577	377	776

INPUT PORT (DR 11A)

BIT #	DATA WORD	INT. PERIOD	INT. PERIOD	INT. PERIOD	INT. MULT.	GAIN. NORM.	GAIN. NORM.	GAIN. NORM.	MULT.
0	D0	$1X10^0$	$1X10^{-1}$	$1X10^{-2}$	"A"	$1X10^0$	$1X10^{-1}$	MULT.	"A"
1	D1	$2X10^0$	$2X10^{-1}$	$2X10^{-2}$	"B"	$2X10^0$	$2X10^{-1}$	MULT.	"B"
2	D2	$4X10^0$	$4X10^{-1}$	$4X10^{-2}$		$4X10^0$	$4X10^{-1}$		
3	D3	$8X10^0$	$8X10^{-1}$	$8X10^{-2}$		$8X10^0$	$8X10^{-1}$		
4	D4								
5	D5								
6	D6								
7	D7								
8	D8	$1X10^1$				$1X10^1$			
9	D9	$2X10^1$				$2X10^1$			
10	D10	$4X10^1$				$4X10^1$			
11		$8X10^1$				$8X10^1$			
12									
13									
14	INT. OL.								
15	POLARITY								
REQ A	BUSY								
REQ B	FLAG								
STROBE	#1	#2	#3	#4	#5	#6	#7	#8	
LINES	4	2	1	1	1	2	1	1	


INPUT PORT
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
REQ. A
REQ. B
720
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
INT. OVERLOAD
SIGN
DATA
1X10^1
2X10^1
4X10^1
8X10^1
1X10^0
2X10^0
4X10^0
8X10^0
1X10^-1
2X10^-1
4X10^-1
8X10^-1
1X10^-2
2X10^-2
4X10^-2
8X10^-2
M1
M2
INTEGRATION PERIOD
1X10^1
2X10^1
4X10^1
8X10^1
1X10^0
2X10^0
4X10^0
8X10^0
1X10^-1
2X10^-1
4X10^-1
8X10^-1
M1
M2
GAIN NORM.
FLAG
BUSY

CABLING


OUTPUT
REGISTER
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
TRIGGER
FLAG RESET
STROBE DATA
STROBE DATA
STROBE DATA
STROBE FLAG
STROBE INT. PERIOD 10^1
STROBE INT. PERIOD 10^0
STROBE INT. PERIOD 10^-1
STROBE INT. PERIOD 10^-2
STROBE INT. MULT.
STROBE GAIN. NORM. 10^1
STROBE GAIN. NORM. 10^0
STROBE GAIN. NORM. 10^-1
STROBE GAIN. NORM. MULT.

CIRCUIT DESCRIPTION

1. GENERAL: The Model 720 is a variable aperture integrating analog-to-digital converter. The circuit is composed of five functional sections which are the Isolated A/D section; the Control and Counter Section; the Gain Normalization Section; the output Logic Section and the Power Supply. Refer to the 720 Timing diagram in the operating section and Figure 2, the overall block diagram.

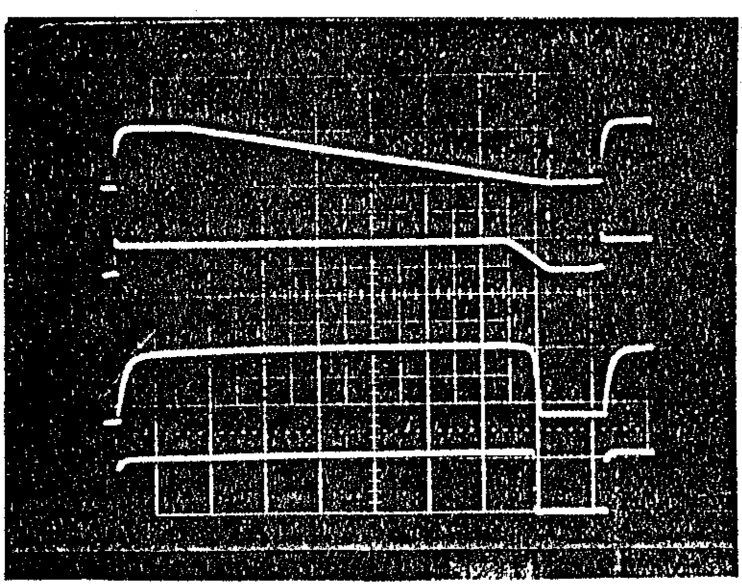
2. ISOLATED ANALOG/DIGITAL SECTION. (Refer to Schematic 3)
The isolated A/D section converts an analog input signal to a digital binary code by means of an integrator module, U-57, and an analog to digital converter, U-18. The integrator, integrates under command from the control section. The integrate signal is transmitted through an isolation pulse transformer, T_1, and a Schmitt trigger, U1. After the input signal has been integrated, it goes to the A/D module by way of a front panel calibration pot, R-211. Approximately 2 μs after the termination of the integrate signal the A/D converter starts its conversion which takes about 40 μs. During the 40 μs the A/D converter transmits its data with the overload bit in front of the bit stream to the output logic section by way of isolation pulse transformer, T2. Isolation transformer T3 is used to transmit a clock pulse train from the A/D module to the output logic section. Upon completion of the A/D conversion the integrator is switched to the reset mode until the next integrate command.

The following are scope photographs that show timing and signal levels of the isolated section:

$V_{in} \cong$ +5 V dc

Thumbwheel settings (T.W.) = $\frac{\text{0150X1}}{\text{015X1}}$

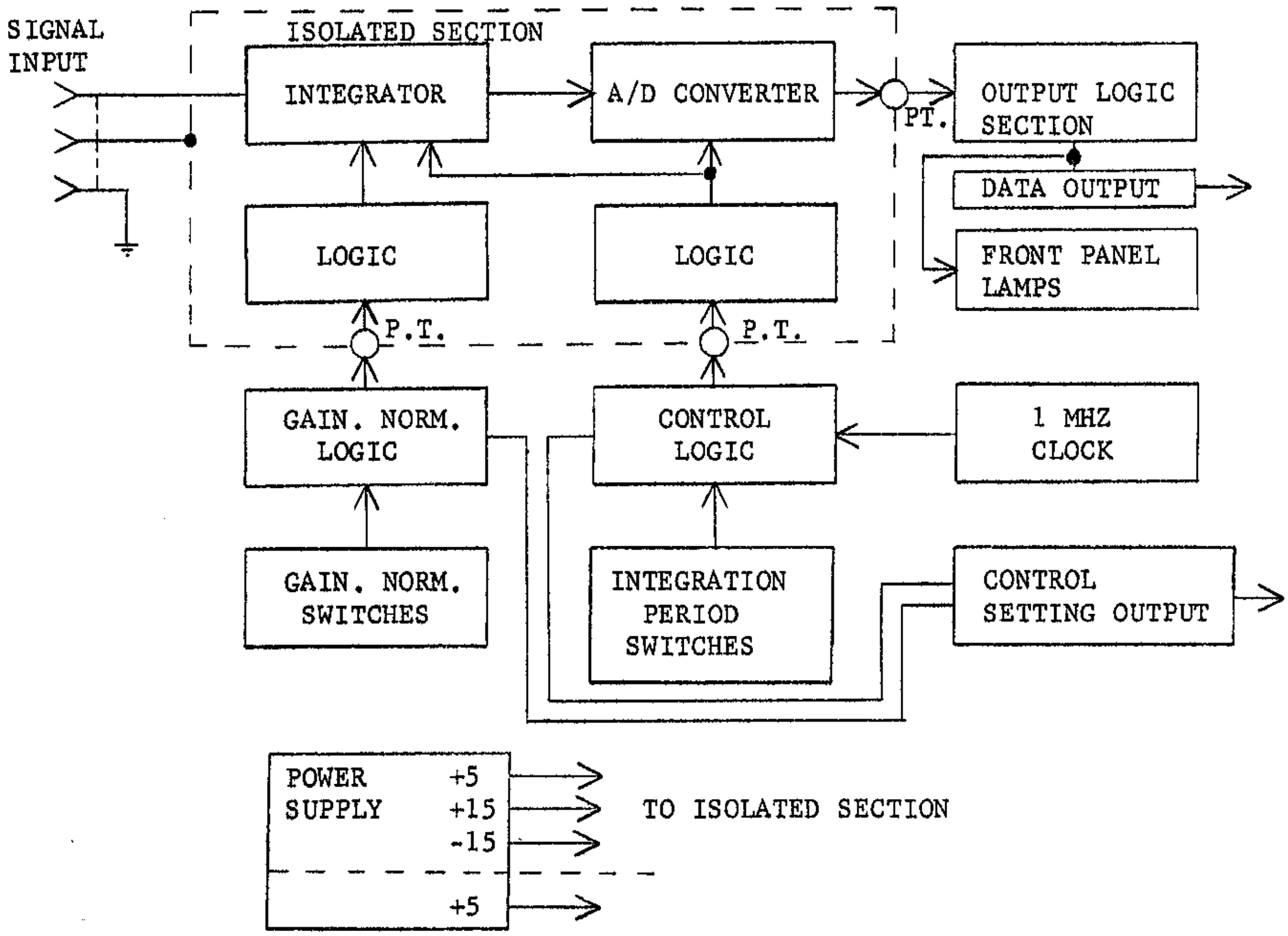
Scope Settings: Horiz: .2ms/div
Trig External: integrate U64/5
Slope = +



	X10 Probes Vert.Volts/Div.	Scope Input to:
GND	1 V	A U57/14
GND	.2V	B U57/9
GND	1.0V	C U52/6
GND	.5V	D U39/5,8

Fig. 3

MODEL 720 BLOCK DIAGRAM



P.T.= PULSE TRANSFORMER

Figure 2.

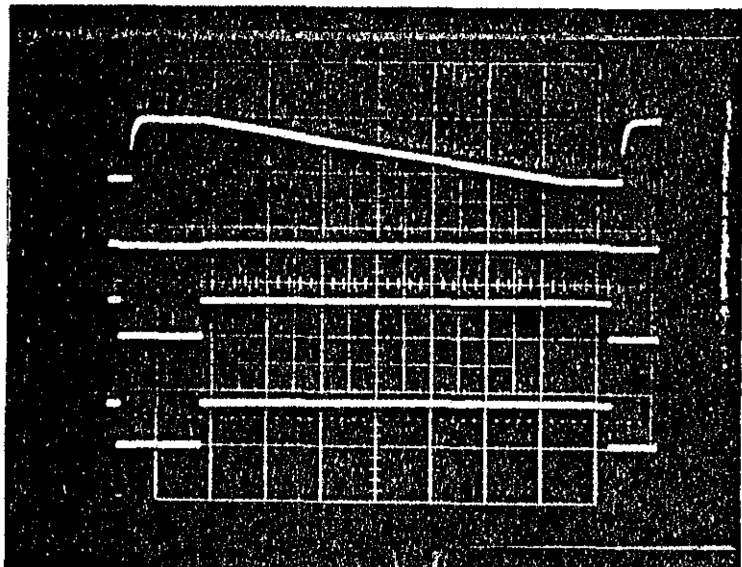
The photograph shows what happens when an overload occurs. With an overload voltage applied to the input of the 720 and the gain set at 1, Fig. 3, Trace "A" showns the output of the integrator which is going negative and saturating. Trace "B" shows the overload indicating signal. This is level amplified by U-52 and the output is seen in Trace "C". The negative going signal turns U-39/C on and the output voltage is seen in Trace "D". With a negative input overload voltage applied, the signals traces A, B and C will be positive. Trace D will be the same.

$V_{in} \cong +5$ V dc

$TW = \frac{0150X1}{015X1}$

Scope settings Horiz: .2 ms/div. delayed ∿ 1.5 ms

Trig: Ext. Integrate Slope +



X10 Probes

	Vert. volts/div.	Scope input to:
GND	1.0V	E U57/14
GND	.2V	F U1/1
GND	.5V	G U1/6
GND	.5V	H U1/8

View Shown

Expanded view shown in Fig. 5.

Expanded in Fig.6.

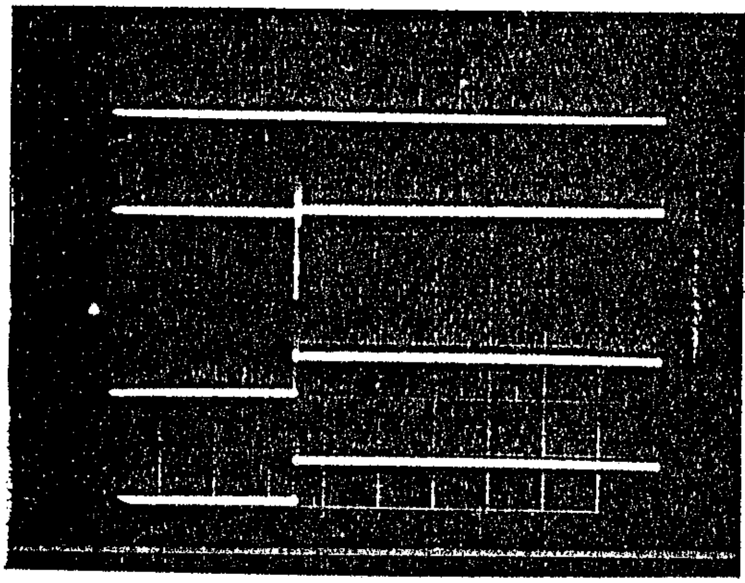
Figure 4.

In the above photo, the top trace "E" is the integrator output voltage. Trace F shows the output of pulse transformer T1, which shows the integrate command pulses from the control section. Fig. 5 Trace "J" and Fig. 6 Trace "N" show expanded views of the integrate pulse. Trace "G" shows the integrate signal at the output of Schmitt trigger U1/6. The integrate signal goes high, the integrator module starts to integrate the input signal. When the signal goes LO the integrator module stops integrating. Trace "H" shows the integrate signal at Pin 34 of A/D module. When the signal goes LO the A/D converter starts its conversion.

$V_{in} \cong +5V$ dc

$TW = \frac{0150X1}{015\ X1}$

Scope settings Horiz: 10 μs/div. delayed ∿ 1.5 ms.
Trigger Ext: $\overline{\text{Integrate}}$ Slope +



X10 Probes

	Vert Volts/Div.	Scope Input	
GND	1.0V	I	U57/14
GND	.1V	J	U1/1
GND	.5V	K	U1/6
GND	.5V	L	U1/8

Figure 5.

Figure 5 Trace "I" shows the output of the integrator. The integrator is turned on when the output of the Schmitt trigger goes high as seen in Trace "K". Trace "J" shows the pulse which causes the Schmitt trigger (U1A) output to go high. Trace "L" shows the output of Schmitt trigger (U1B).

$V_{in} \cong +5V$ dc

$TW = \frac{0150X1}{015\ X1}$

Scope Settings Horiz: 10 μs/div. delayed ∿1.5 ms.

Trigger Ext: $\overline{\text{Integrate}}$ Slope +

	X 10 Probes Vert.Volts/Div.	Scope inputs to:
— GND	1.0V	M U57/14
—GND	.1V	N U1/1
—GND	.5V	O U1/6
—GND	.5V	P U1/8

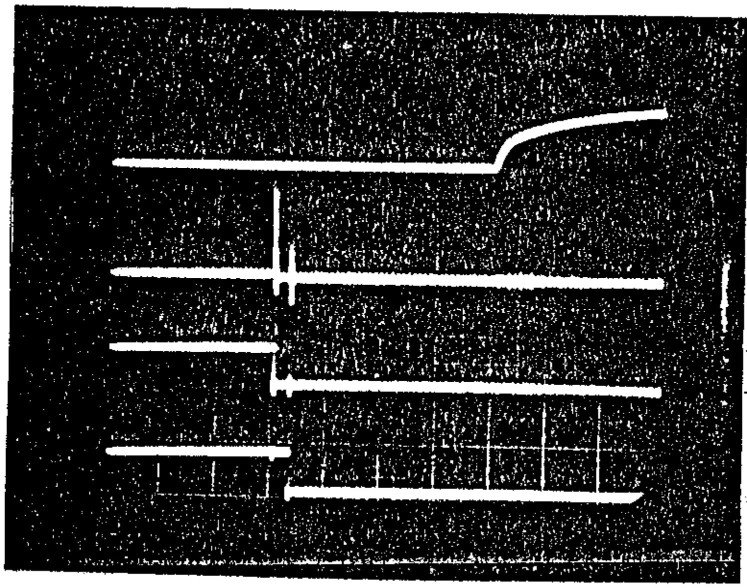


Figure 6.

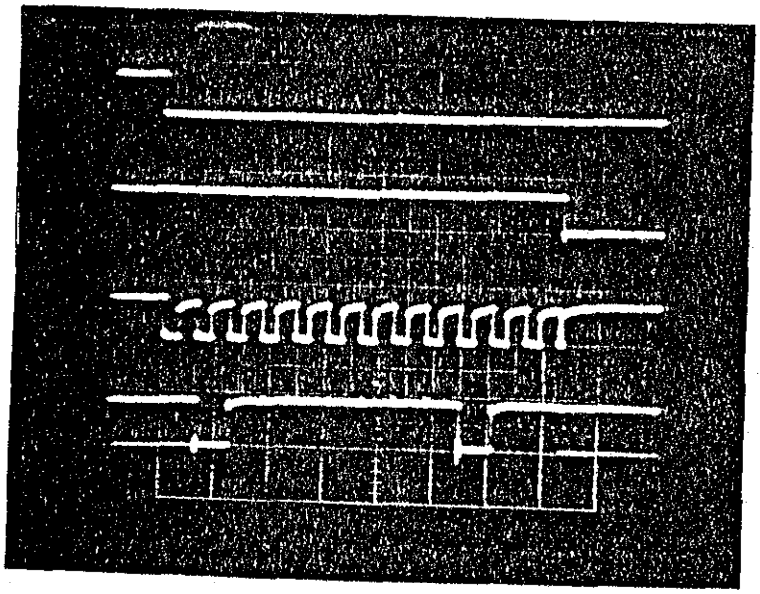
Figure 6 is an expanded view of Fig. 4 to show the end of integrate plus and the 2 μs delay of the integrate signal to U18/34. The start of conversion point, trace "M", shows the integrator output. With +5 volts applied to the 720, the integrator output has saturated at -10 volts. When the A/D conversion is finished converting its data, the integrator is reset and the signal goes to ground potential as shown in the top trace. Trace "N" shows the pulse at the end of the integrate signal from the control section. Trace "O" at U1 Pin 6 shows the integrate signal. The signal goes low when the end of integrate pulse goes high. Trace "P" shows the 2 μs delay between trace "P" and trace "O". When trace "P" goes low the A/D converter starts it's conversion.

Signals of the A/D Converter.

V_{in} = +8 mV

$TW = \frac{0150X1}{015\ X1}$

Scope Settings: Horiz: 5 μs/div. Delayed ∿ 1.5 ms.
Trigger Ext: $\overline{\text{Integrate}}$
Vert: 5V/div.



Trace	Scope Input to:
U	U18/34
V	U18/33
W	U18/35 & 36
X	U18/32

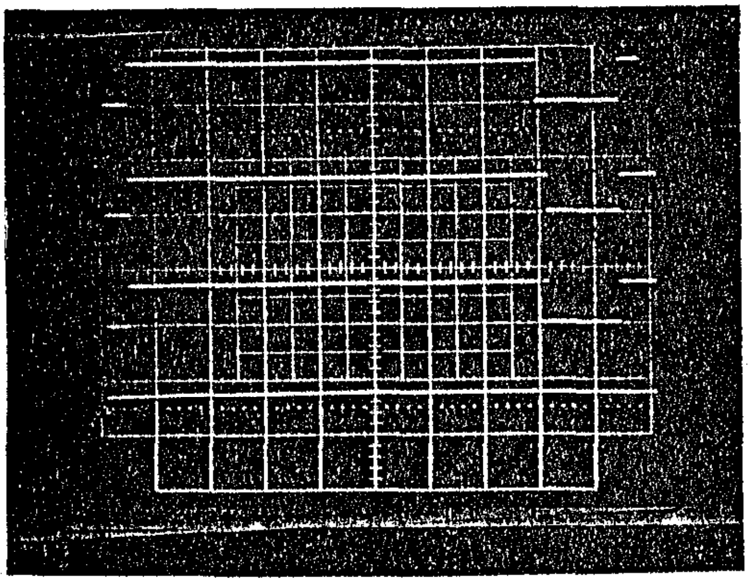
Figure 8.

The top trace "U" shows integrate signal going LO after 2 μs delay. This is the start of the A/D conversion. Trace "V" is the end of conversion signal. When the A/D converter is through converting the signal goes LO and resets the integrator U57. Trace "W" shows the clock output, while Trace "X" shows the serial data.

$V_{in} \cong 8mV$

$TW = \frac{0150X1}{015\ X1}$

Scope Setting: Horiz: .2ms/div.
Trig Ext: INTEGRATE
Vert: 5V/Div.



Trace	Scope Inputs To:
Q	U18/34
R	U18/33
S	U27/9
T	U27/6

Figure 7.

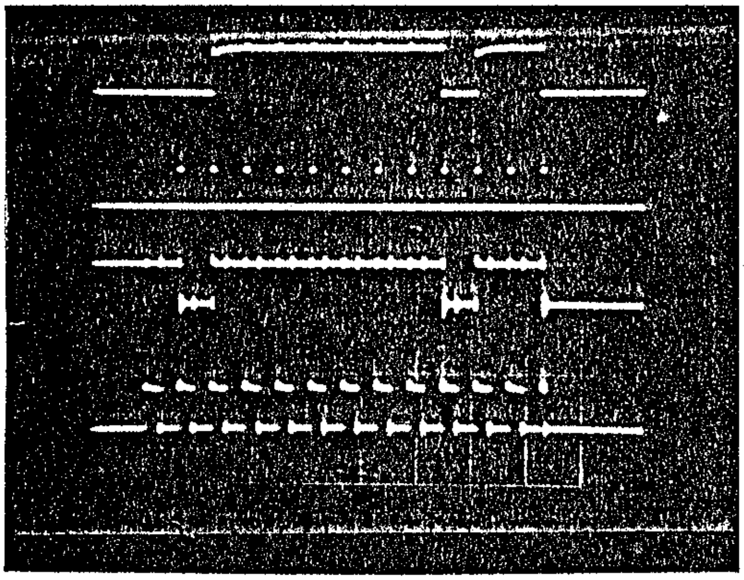
Figure 7 trace "Q" shows the signal at U18/34 which is the integrate signal plus a 2 microsecond delay. The period that the signal is LO is the reset time. This reset period is controlled by the control section and is set for 300 microseconds. When the signal in trace "Q" goes LO the A/D converter starts its conversion. In trace "R" the LO signifies the end of the conversion and resetting of the integrator. The difference between traces "Q" and "R" is 50 microseconds, which is the A/D conversion time. Trace "S" shows the data (after the falling edge of "Q"). Refer to Fig. 8 and 9 for expanded view. Trace "T" shows the output U27/6 which is normally HI. It will go LO briefly if the last "LSB" was a zero.

Model 720

V_{in} = 9 mV

TW = $\frac{0150X1}{015\ X1}$

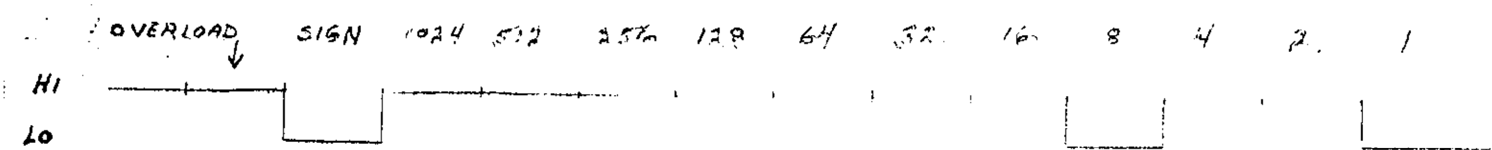
Scope Setting: Horiz: 5µs/div. delayed ~ 1.5 ms.
Trig Ext: $\overline{\text{INTEGRATE}}$
Vert: 5V/Div.



Trace	Scope Input To:
Y	U18/32
Z	U19/39
AA	U27/9
BB	U26/11

Figure 9.

Trace "Y" shows the serial data output of U18. Signals indicate +9 mV. Trace "Z" shows the 12 storbe pulses which are used to strobe valid data through U27B. Trace "AA" shows the data at U27/9. Trace "BB" shows the inverted clock signal.
Trace "AA":



The data is LO true. Therefore the above signals indicate a +9 mV because the sign bit is low and 8 and 1 are low.

3. OUTPUT LOGIC SECTION (Refer to Schematic 2).

The output logic section receives data from the isolated section, displays the data on the front panel LED's, and makes the data available at the output connector P15.

At the termination of the integrate signal a one shot (U64) is fired which clears the output shift registers (U54, U55) and presets flip-flop U48 to a "1". The data from the isolated A/D section is coupled through isolation pulse transformer T2. The preset "1" (U48) is shifted ahead of the bit stream as it is clocked in to the shift registers. The preset "1" is shifted to the last cell where it sets the flag F/F U48B and also sets an internal flag for the gain normalization registers indicating that the A/D conversion is complete. The clock pulses are also transmitted from the isolated A/D section through pulse transformer T3.

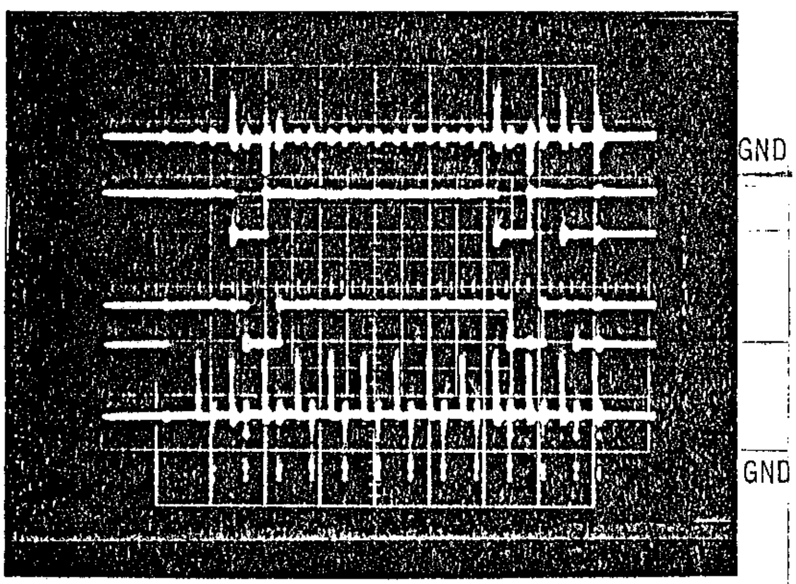


Figure 10.

X10 Probes Vert V/Div.	Trace	Scope Inputs To:
	A	U47/1
.2V		
.5V	B	U47/1
.5V	C	U/48/5
.2V	D	U47/9

Scope Settings

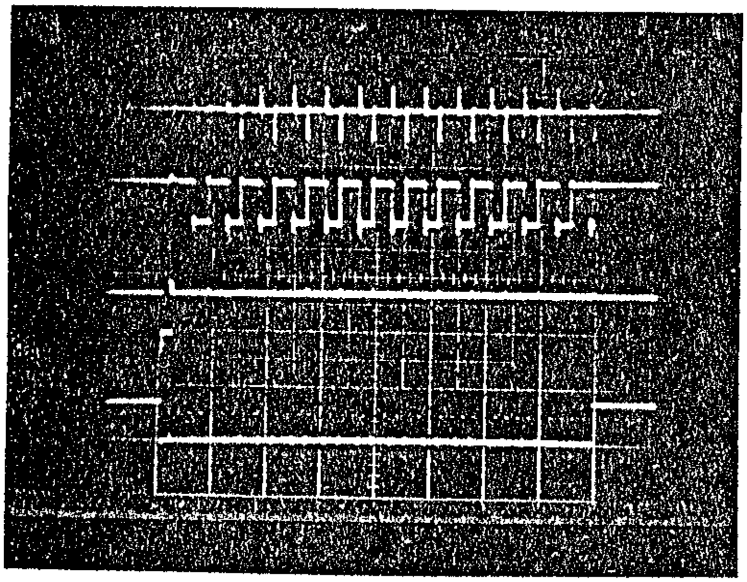
Horiz: 5μs/div delayed ∿1.5 ms.

Trig Ext: $\overline{\text{INTEGRATE}}$

V_{in} = 8mV or 9mV

$TW = \frac{\overline{0150X1}}{0150X1}$

Figure 10 trace "A" shows the data pulses coming from the isolated section through pulse transformer T2. Trace "B" shows the data at the output of Schmitt trigger U47A. Trace "C" shows the data at the input to shift register U54. Trace "D" shows the clock pulses at the output of T3, which after going through the Schmitt trigger U47B are used to clock the data into the shift registers.



Trace	Scope Inputs To:
E	U47/9
F	U47/8
G	U64/1
H	U48/11

Scope Settings: Horiz: 5μs/div. delayed ∿1.5ms
Vert: 5V/Div. X10 Probe
Trig Ext: $\overline{\text{Integrate}}$
Slope = +

$TM = \frac{0150X1}{015\ X1}$

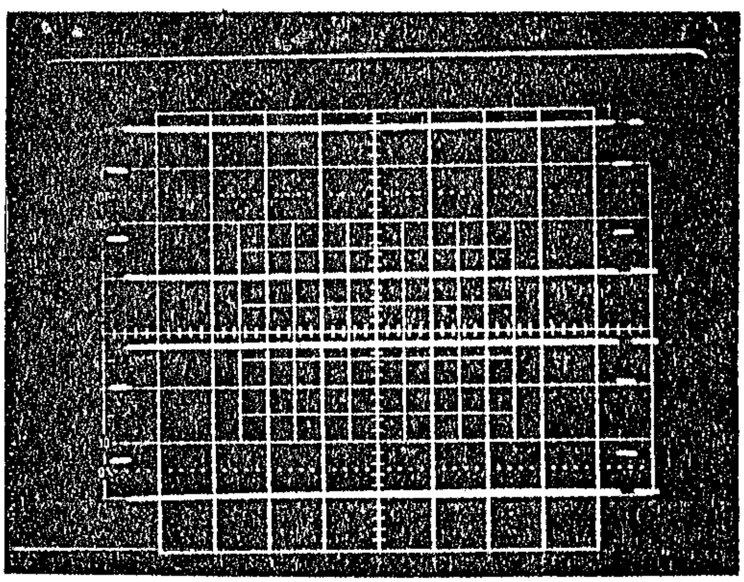
Figure 11.

Figure 11 trace "E" shows the clock pulses coming through isolation pulse transformer T3. Trace "F" shows the clock signal at the output of Schmitt trigger U47B. The clock pulses shift the data into shift registers U54 and U55. At the end of the integrate signal a one shot (U64) is fired which clears the output shift registers and presets U48A to a "1". This clear pulse is seen in trace "G". Trace "H" shows the output of U55/13, which goes to "0" when cleared. The signal will stay low until all the data is clocked in and the preset "1" causes Pin 13 to go high. This causes the flag to go high and signals U8/3 in the G.N. section (refer to Schematic 1) that the data transfer is complete.

CONTROL AND COUNTER SECTION (Refer to Schematics 1 & 2)

This section controls the integration and reset time of the system. The control section consists of a pair of flip-flops (U46A, B) to internally synchronize the trigger to the system. Triggering can occur from an external TTL-type signal, the front panel pushbutton switch (S3), or the internal clock. The trigger mode is set by front panel switch (S3). An external integration period signal can be applied to the system, however the trigger and internal reset signals will be disabled.

When the integrate F/F has been set the integrate signal is transmitted to the isolated section and the counters (U31, 32, 33, 34) are allowed to count down from the thumbwheel switch (S4) presettings. A "borrow" signal from U34 stops the integrate signal by resetting flip-flop U46B which fires a one shot (U17) to prevent retriggering for 300 microseconds.



Trace	Scope Inputs To:
A	U46/5
B	U46/8
C	U17/1
D	U17/5

$TW = \frac{0900X1}{090\ X1}$

Scope Set:
Horiz: 1ms/div
Vert: 5V/div.
X10 Probes

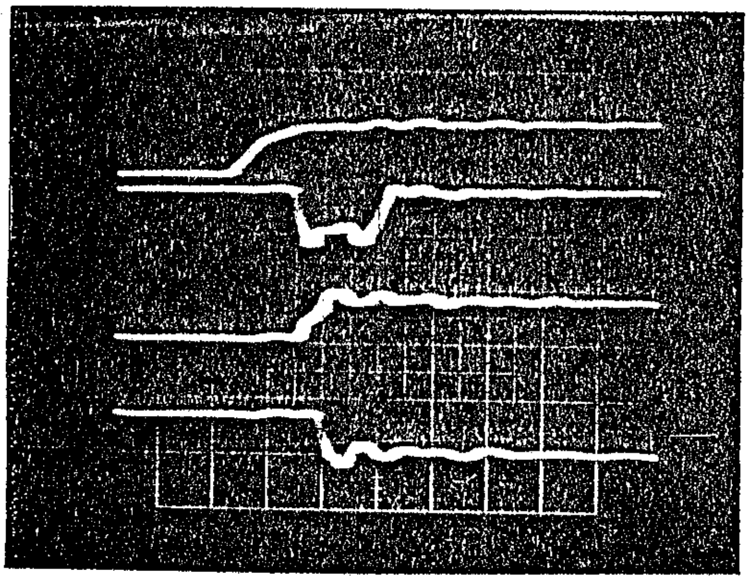
Trig: $\overline{\text{INTEGRATE}}$
Slope = +

Figure 12.

Fig. 12, Trace "A", shows the output of U46A. After the 300 microsecond reset time the signal will go Hi when triggered. This will cause the output of U46B (shown in Trace "B") to go low, which starts the counters to count down. The counters will produce a borrowed pulse which resets U46B, which then causes U17 to be fired. This resets U46A for 300 microseconds. Trace "C" shows the output of U17/1 while trace "D" shows the $\overline{\text{INTEGRATE}}$ signal.

TW = 0010X1
001 X1

Scope Settings: Horiz: .05 μs/div. Delayed ∿1.5ms.
Vert: .5V/div. X10 Probes
Trig: Ext $\overline{\text{INTEGRATE}}$ Slope +



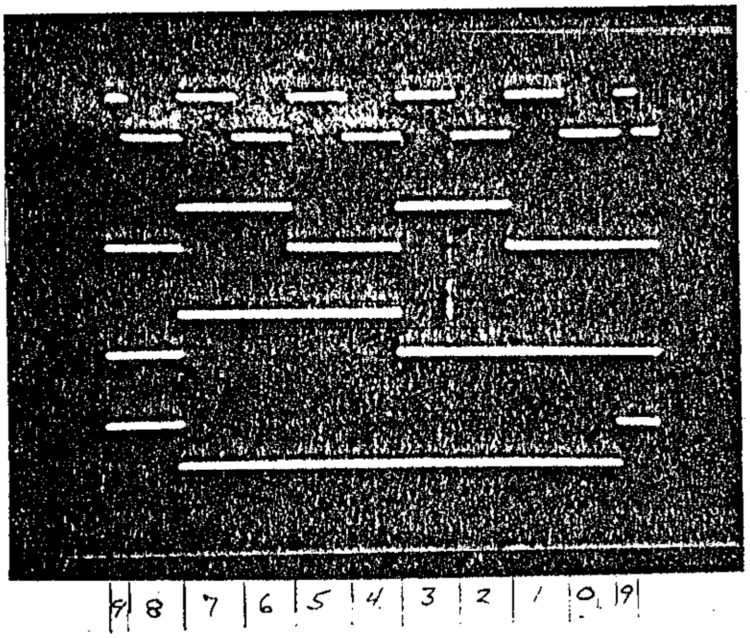
Trace	Scope Inputs To:
E	U19/1
F	U34/13
G	U46/8
H	U34/11

Figure 13.

Fig. 13 is an expanded view to show the borrow pulse from U34. The pulse is produced at the end of the integration period and it is shown in trace "F". Trace "E" shows the rising edge of the provided clock. Trace "G" shows the $\overline{\text{INTEGRATE}}$ line. The unit integrates until this signal goes high. Trace "H" shows the $\overline{\text{LOAD}}$ signal. When the signal goes lo, the settings on the integration T.W. switch (S4) is loaded into the counters.

TW = $\frac{0900X1}{090\ X1}$

Scope Settings: Horiz: 1ms/div
Vert: .5V/div. X10 Probes
Trig: $\overline{\text{INTEGRATE}}$ Slope = +



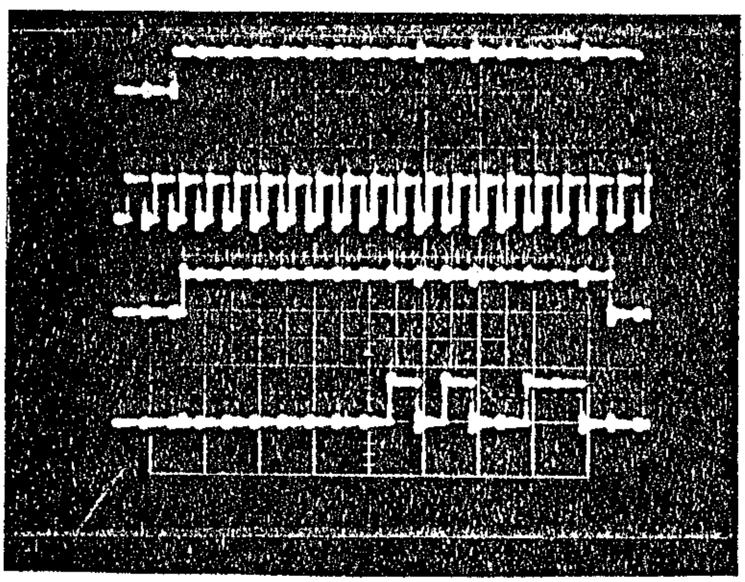
Trace	Scope Inputs To:
I	U33/3
J	U33/2
K	U33/6
L	U33/7

Figure 14.

Fig. 14 shows the Q outputs of U33. The signals show a 9 loaded into U33 and the countdown to zero and then to a 9 again. The counters will count down from their loaded number and a borrow pulse will be produced between 9, 0 to 9 count.

5. Gain Normalization Section. (Refer to Schematics 1 & 3)

The gain normalization section controls the input resistance and the integrator capacitors of the integrator module U57. In order to prevent zero resistance to be switched onto the integrator and to compensate for resistance of the FET switch, a 10k equivalent resistance is permanently wired to the input of the integrator. The actual value of resistance that should be switched in would be the desired resistance minus 10kΩ. The adders (U12, U13, U14) and the NOR gates (U3, U4, U5) subtract one from the front panel T.W. switch S5. This number is loaded into shift registers U6 and U7 along with the multiplier settings (capacitor) and upon completion of the A/D conversion, the T.W. switch settings are transferred thru pulse transformers T4 and T5 to shift registers in the isolated section. The transfer of data to shift registers U35 and U36 takes 16 μs. The data is not latched because the relays K4 to K15 and associated circuitry cannot respond to the bits passing by in this short time. Capacitors C32, 33 and 34 are used to slow down the turn on time of Q39A, E and D so that no two of the G.N. capacitors C51, C54 and C55 will be switched on to the integrator U57 simultaneously, preventing the relay contacts from welding.



Trace	Scope Inputs To:
A	U8/3
B	U8/11
C	U8/9
D	U7/9

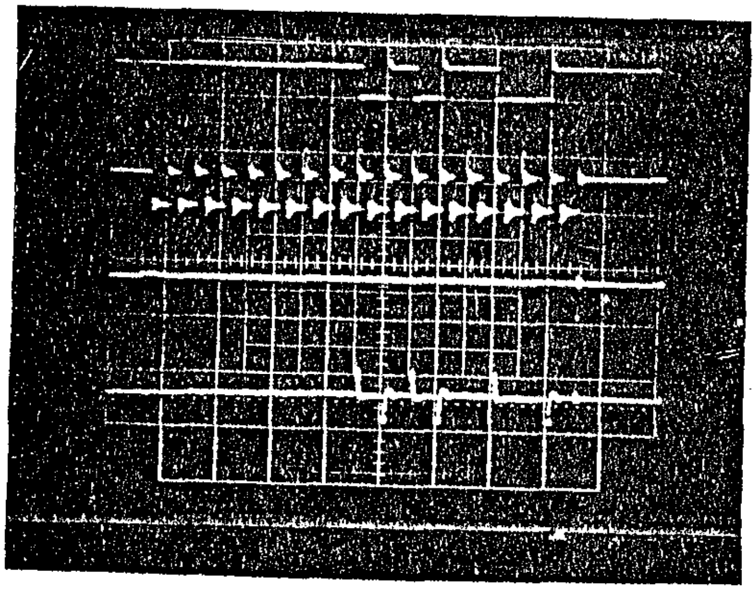
$TW = \frac{0150X1}{015\ X1}$

Scope Set:
Horiz: 2μs/div
Delayed ∿ 1.5 ms.
Vert: .5V/div
X10 Probes
Trig: Ext $\overline{\text{INTEGRATE}}$

Figure 15.

Fig. 15 Trace "A" shows the signal going from LO to HI when the output data has been shifted into registers U54 and U55. Trace "B" shows the 720 clock train. When the signal in trace A goes HI and on the rising edge of the clock pulse, U8/9 will go HI for 16 μs as shown in Trace "C". The G.N. settings in registers U6 and U7 can then be shifted out to U35 and U36.

Fig. 15 trace "D" shows the data being shifted out.



Trace	Scope Inputs To:
E	U24/3
F	U24/6
G	U16/12
H	U25/1

$TW = \frac{0150X1}{015\ X1}$

Scope Settings:
Same as Fig. 15.

Figure 16.

Trace "E" shows the inverted G.N. data going to pulse transformer T4. Trace "F" shows the $\overline{\text{CLOCK}}$ signal going to pulse transformer T5. Trace "G" shows the reset pulse from U16 going to U8A, B. The pulse is produced 16 μs (16 clocks) after the start of the gain normalization data transfer. Trace "H" shows the data pulses at the output of pulse transformer T4.

TW = $\frac{0150X1}{015\ X1}$

Scope Settings; Horiz: 2 μs/div. Delayed ∿ 1.5 ms.
Trig: Ext. INTEGRATE
X10 Probes

Vert: V/Div.	Trace	Scope Inputs To:
.5V	I	U25/6
.5V	J	U25/9
.5V	K	U37/8
.1V	L	U38/3

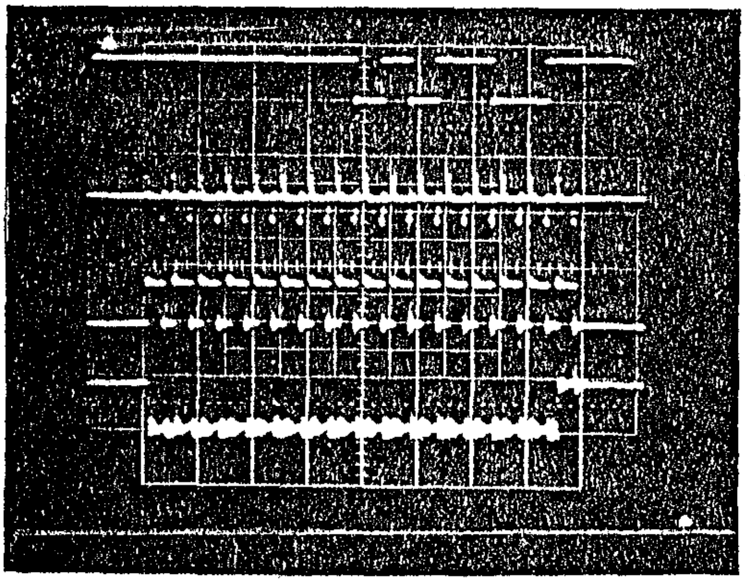
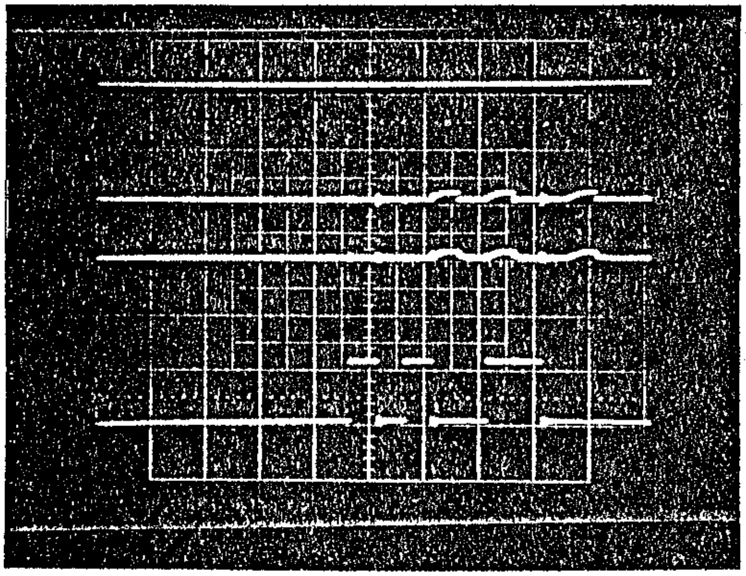


Figure 17.

Trace "I" shows the G.N. data as it is clocked into shift registers U35, U36. Clock pulses at the output of T5 are shown in Trace "J". Trace "K" shows the clock pulse after passing through Schmitt trigger U25A and inverter U37/8. Trace "L" shows the signal at U38/3. This point goes LO as the G.N. data is coming into the shift registers and the signal goes high at the last clock pulse which turns U39E on. This indicates the gain normalization X1 setting is being used.

T.W. = $\frac{0150X1}{015\ X1}$

Scope Settings: Horiz: 2 μs/div. Delayed ∿ 1.5 ms.
Trig: Ext: Not INTEGRATE
Vert: .5V/div. X10 probes



Trace	Scope Inputs To:
M	U39/14
N	U38/6
O	U39/1
P	U51/8

Figure 18.

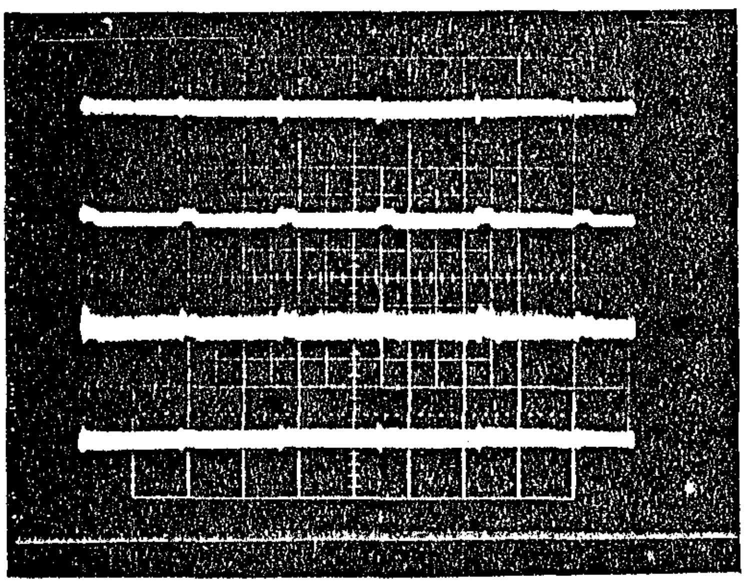
Fig. 18 trace "M" shows that in X1 position U39/14 is LO and relay I2 is turned on. Trace "N" shows the signal at U38/6 which is LO in the X1 position. This point will go high in the X10 setting. Trace "O" shows the collector of U39/1 as being high and relay T1 will be off. Trace "P", the signal at U51/8, when this point is lo the relay is turned on which shorts out the resistor. When the resistor is selected this point goes high.

6. Power Supply Section. (Refer to Schematic 3)

The power supply will operate with a line voltage from 90 to 125 V ac and 195 to 250 V ac by switching S6 to the proper positions and using the correct fuse, F1. The power supply consists of two sections. One section supplies +5 volts @ 3 A to the control and counter section, the output section and the gain normalization section. The other section of the power supply supplies +5 volts @ .75 A and ±15 volts @ 150 mA each. The ±15 volt supplies use the +5 volt supply as a reference. The +5 volt @ .75 amp supply supplies power to the A/D module and the supporting logic in the isolated section. The ±15 volt supplies supply power to the integrator module and the A/D module.

Scope photographs of ripple of the power supplies:

Scope: Vert. 5mV/div. X10 probes
Horiz. 1ms/div.



Supply

+5V @ 3A

+5V @ .75A

-15V @ 150mA

+15V @ 150mA

Figure 19.

CALIBRATION

1. General. This section contains information necessary to calibrate the Model 720 to the appropriate published specifications.

2. Required Test Equipment. Recommended test equipment for calibration is given in Table 1.

ITEM	DESCRIPTION	MFGR	MODEL
A	Voltage source .002% accuracy	Fluke	343A
B	Frequency/Period Counter .001%	Monsanto	120A
C	Ohmmeter > .1% accuracy (DMM)	Keithley	190
D	Oscilloscope BW = 10 MHz	Tektronix	
E	Picoammeter	Keithley	610C

3. Procedure. Calibrate at 25°C ±3°C, with unit warmed up. Set thumbwheel (T.W.) 0100X1/010X1 and trigger switch in auto position.

a. Clock.

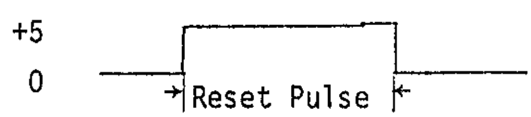
1. Connect Monsanto counter to 49 Pin 2 and digital LO (U9 Pin 7).

2. Adjust variable capacitor C2, and set the frequency to 1.000000 MHz.

b. Reset Time.

1. Connect oscilloscope to test point #2, through access panel on the back panel. Use digital LO for LO connection.

2. Adjust R-209 (reset Adj. pot) for a pulse width of 300 μs.



c. A/D converter (U18)

1. Remove P-11 and short test point 1 to analog LO.

2. Adjust offset pot R-36 for a binary reading of 011...111/100...000 flashing on the front panel LED's.

3. Remove short and apply +4.9976 volts to test point #1 and adjust gain pot R-35 for 000...000/000...001 flashing. (Use analog LO for LO connection).

4. Remove voltage source and replace P-11.

d. Integrator (U57)

1. Remove R87, 100kohm input shunt resistor.

2. Use Keithley 190 to check and adjust input resistance.

3. Set TW switches to $\frac{9999x100}{001 \times 1}$ and connect HI of 190 to input connector (J1) HI.

Connect LO of 190 to U57 Pin 7 (Σ junction).

4. With unit integrating adjust pot R-89 for a resistance of 10 kohm ±.1% or better.

5. To verify that the input resistors are in spec, set the gain normalization TW switch to the following settings and check that the resistance is within ±.1% (190 connected same as in step 2).

G.N. TW SETTING	RESISTANCE ±.1%
00.2	20k
00.3	30k
00.5	50k
00.9	90k
02.0	200k
03.0	300k
05.0	500k
09.0	900k
20.0	2M
30.0	3M
50.0	5M
90.0	9M
00.0	10M

6. Remove 190 and replace R-87, 100kohm input resistor.

7. Set TW switches to $\frac{0200x100}{020x100}$, short 720 input and adjust front panel zero pot to mid-range.

8. Adjust pot R208 through access panel for 011...111/100...000 flashing. you can adjust front panel zero pot for fine adjustment.

9. Remove short from input and apply +2047 mV from a dc calibrator to the input and adjust front panel cal pot for 111...110/111...111 flashing.

10. Remove +2047 mV and short 720 input, then set T.W. switches to $\frac{0200x10}{020x10}$ and rezero unit with front panel zero pot.

11. Remove short and apply +2047 mV to the input. The reading should be within ±2 bits from where unit was calibrated.

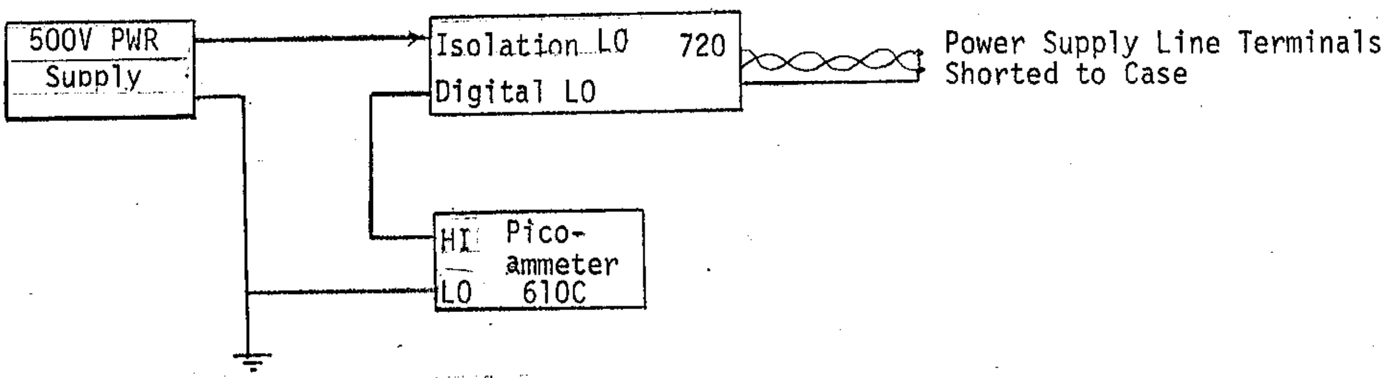
12. Repeat steps 10 and 11 using T.W. setting of $\frac{0200x1}{020x1}$

12. If readings are >±2 bits you can adjust the integrator trim capacitors for closer readings. When checking the ranges make sure the unit is properly zeroed first.

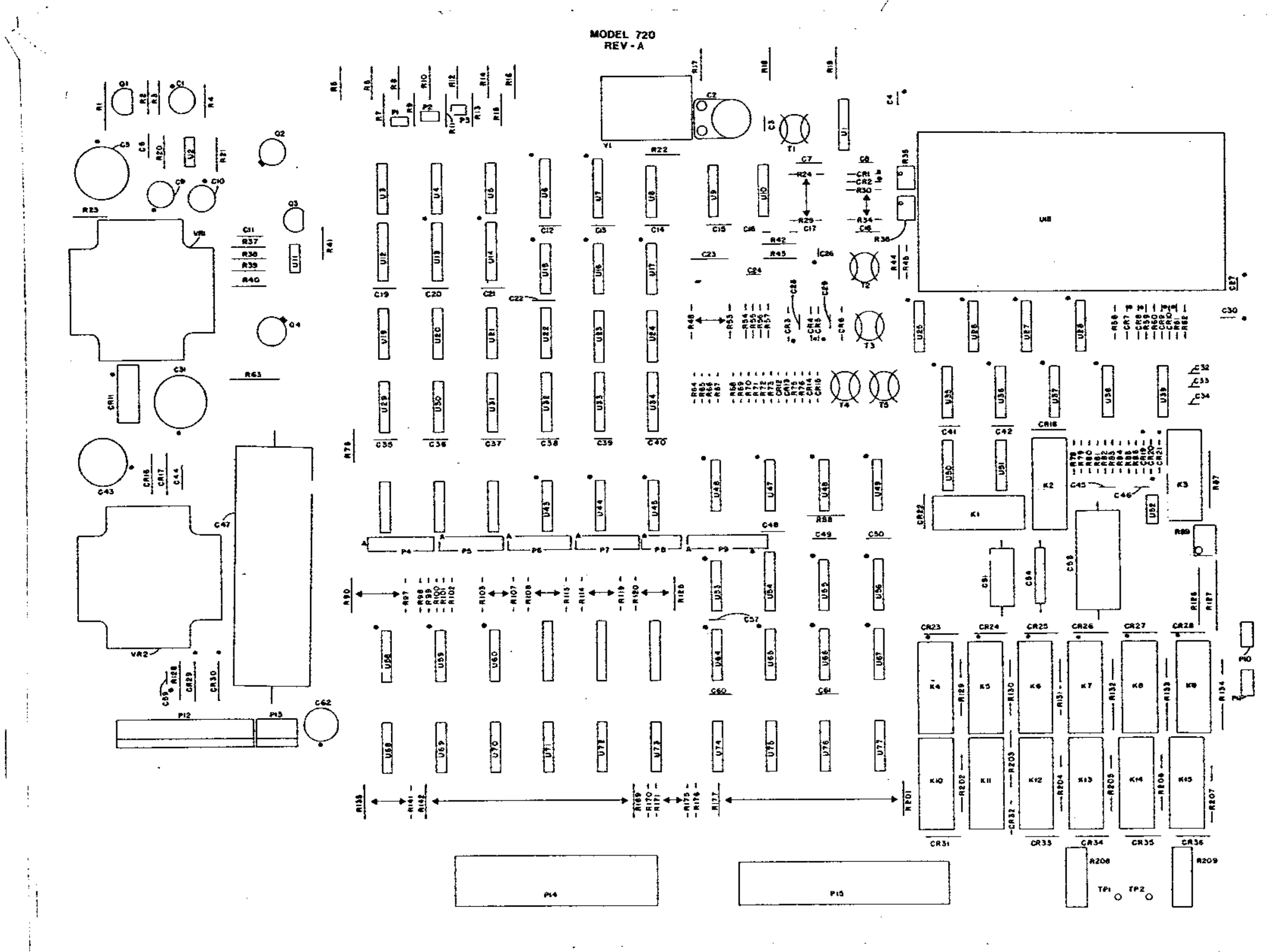
TRIM CAPACITORS	RANGE
C-56*	X100
C-52*	X10
C-53*	X1

*Use polystyrene

e. Isolation.



1. 720 should be warmed up. Pull line cord from outlet and short terminals to chassis gnd.
2. Apply 500 volts dc as shown above.
3. Check leakage current for typically 10^{-6} amperes (see specs).



COMPONENT LAYOUT

REPLACEABLE PARTS

REPLACEABLE PARTS LIST. The Replaceable Parts List describes the components of the Model 720 and its accessories. The List gives the circuit designation, the part description, a suggested manufacturer, manufacturer's part number and the Keithley Part Number.

HOW TO ORDER PARTS.

a. For parts orders, include the instrument's model and serial number, the Keithley Part Number, the circuit designation and a description of the part. All structural parts and those parts coded for Keithley manufacture (80164) must be ordered from Keithley Instruments or its representative. In ordering a part not listed in the Replaceable Parts List, completely describe the part, its function and its location.

b. Order parts through your nearest Keithley representative or the Sales Service Department, Keithley Instruments, Inc.

AMP	ampere	MtF	Metal Film
		Mil. No.	Military Type Number
CbVar	Carbon Variable	My	Mylar
CerD	Ceramic, Disc		
Comp	Composition	Ω	ohm
DCb	Deposited Carbon	Poly	Polystyrene
		P	pico (10^{-12})
EAl	Electrolytic, Aluminum		
EMC	Electrolytic, metal cased	μ	micro (10^{-6})
ETT	Electrolytic, tantalum		
		v	volt
f	farad	Var	Variable
k	kilo (10^3)	w	watt
		WW	Wirewound
M or meg	mega (10^6) or megohms	WWVar	Wirewound Variable
m	milli (10^{-3})		
Mfg.	Manufacturer		

Abbreviations and Symbols

CODE-TO-NAME LIST

CODE TO NAME List of Suggested Manufacturers.
Reference: Federal Supply Code for Manufacturers, Cataloging Handbook H4-2.

01121	Allen-Bradley Corp. Milwaukee, Wisc. 53204
01295	Texas Instruments, Inc. Semiconductor Div. Dallas, Texas 75231
02660	Amphenol Corp. Broadview, Ill. 60153
02735	RCA Solid State Div. Somerville, N.J. 08876
04713	Motorola Semicon. Prod. Phoenix, Ariz. 85008
06751	Components, Inc. Semcor Division Phoenix, Ariz. 85019
14655	CornellDubilier Elec.Div. Newark, N.J. 07105
56289	Sprague Electric Co. Visalia, Calif. 93278
14752	Electro Cube Inc. San Gabriel, Calif. 91776
18324	Signetics Corp. Sunnyvale, Calif. 94086
22526	Berg Electronics, Inc. New Cumberland, Pa. 17070
24655	General Radio Co. West Concord, Mass. 01781
29309	Richey Electronics Inc. Nashville, Tenn. 37213
58474	Superior Electric Co. Bristol, Conn. 06010
70903	Belden Mfg. Co. Chicago, Ill. 60644
71590	Centralab Div. of Globe-Union, Inc. Milwaukee, Wisc. 53201
72982	Erie Technological Prods. Erie, Pa. 16512
73445	Amperex Electronic Div., North American Philips Co. Hicksville, N.Y.
75042	IRC Div. of TRW, Inc. Philadelphia, Pa. 19108
80164	Keithley Instruments, Inc. Cleveland, Ohio 44139
80294	Bourns, Inc. Riverside, Calif. 92507
81073	Grayhill, Inc. La Grange, Ill. 60525
82389	Switchcraft, Inc. Chicago, Ill. 60630
96684	RCA Electronic Components Harrison, N.J. 07029
90201	Mallory Capacitor Indianapolis, Ind. 46206
91637	Dale Electronics, Inc. Columbus, Nebr. 68601
95712	Dage Electric Co., Inc. Franklin, Ind.

Parts shown on Schematic Number 27864E, Sheet 1, Counters and Time Constant Logic

CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG. DESIGNATION	KEITHLEY PART NO.
	CONNECTORS			
J4 - J7	Connector, 8 Pin Berg Housing	22526	65039-Style C	CS-310
J8	Connector, 5 pin Berg Housing	22526	65039-040 (Lettered)	CS-251
P14	HDP-20 Economy Connector	02660	205869-1	CS-307
	RESISTORS			
R22,R46,R47	1kΩ, 10%, 0.25W, Comp	01121	CB-102-10%	R-76-1k
R48-R51	470Ω, 10%, 0.25 W, Comp	01121	CB-471-10%	R-76-470
R76	4.7kΩ, 10%, 0.25W, Comp	01121	CB-472-10%	R-76-4.7k
R77	1kΩ, 10%, 0.25 W, Comp	01121	CB-102-10%	R-76-1k
R90-R98	22kΩ, 10%, 0.25W, Comp	01121	CB-223-10%	R-76-22k
R99, R100	15kΩ, 10%, 0.25 W, Comp	01121	CB-153-10%	R-76-15k
R101, R102	10kΩ, 10%, 0.25W, Comp	01121	CB-103-10%	R-76-10k
R103-R121	22kΩ, 10%, 0.25 W, Comp	01121	CB-223-10%	R-76-22k
R136-R175	10kΩ, 10%, 0.25 W, Comp	01121	CB-103-10%	R-76-10k
	SWITCHES			
S4	Switch, Thumbwheel	80164	-	SW-378
S5	Switch, Thumbwheel	80164	-	SW-379
	TRANSFORMERS			
T4, T5	Pulse, Transformer	80164	-	720-11A
	INTEGRATED CIRCUITS			
U3-U5	Positive NOR gates, 14 Pin DIP	01295	SN7402N	IC-32
U6,U7	8-Bit Shift Register, 16 Pin DIP	18324	N74165	IC-123
U8	Dual D Flip-Flop, 14 Pin DIP	01295	SN7474N	IC-31
U12-U14	4-Bit Binary Full Adder, 16 Pin DIP	01295	SN7483N	IC-120
U16	Synchronous 5-Bit Up/Down Counter, 16-Pin DIP	01295	SN74193N	IC-44
U19	Quad, 2 input Pos NAND, 14-Pin DIP	01295	SN7401	IC-47
U20-U22	Decade Counters, 14-Pin DIP	01295	SN7490N	IC-37
U24	Quad NAND, 14-Pin DIP	01295	SN7400N	IC-38
U29	HEx Inverter, 14-Pin DIP	01295	SN7404N	IC-33
U30	Positive NOR gates, 14-Pin DIP	01295	SN7402N	IC-32
U31-U34	UP/Down Counter, 16-Pin DIP	01295	SN7404N	IC-110
U43-U45,U58	Hex Inverter, 14-Pin DIP	01295	SN7404N	IC-33
U59,U60, U68-U73	Quad NAND Gate, 14-Pin DIP	04713	MC858P	IC-52

COMPONENT DESIGNATION LISTING

Parts shown on Schematic Number 27864E, Sheet 2, Control and Output Logic

CAPACITORS

CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG. DESIGNATION	KEITHLEY PART NO.
C2	Capacitor, Trimmer	72982	557-000,A,5.0-25 pF	C-265-5-25P
C3	Capacitor 20pF, 500V, Mica	14655	CD10ED200J03	C-236-20P*
	*Nominal value selected at factory			
C16,C17	Capacitor, 100pF, 500V, Mica	14655	CD10ED101J03	C-236-100P
C23	Capacitor, .068μF, 50V, Poly	14752	625B1A683-J	C-201-.068
C24	Capacitor, 4700pF, 1000V, Cer.D.	56289	10SS-D47	C-64-4700P
C26	Capacitor, 1.2μF, 20V, ETT	06751	TD1-20-125-20	C-179-1.2M
C28	Capacitor, 330pF, 1000V, Cer.D.	71590	DD-331	C-64-330P
C57	Capacitor 680pF, 1000V, Cer.D.	71590	DD-681	C-64-680P
C63	Capacitor, .01μF, 1000V, Cer.D.	56289	5GAS-S10	C-22-.01

RECTIFIERS

CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG. DESIGNATION	KEITHLEY PART NO.
CR3-CR6	Rectifiers, 75mA, 75V	01295	1N914	RF-28

PILOT LIGHTS

CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG. DESIGNATION	KEITHLEY PART NO.
DSI-DS16	Red-Light Emitting Diode	80164	-	PL-61

CONNECTORS

CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG. DESIGNATION	KEITHLEY PART NO.
J19	Bananna, Jack, Black	80164	-	BJ-9-0
J18	Binding Post, Green	58474	DF21	BP-11-5
J17	Binding Post, Blue	58474	DF21	BP-11-6
J9	Connector, 10-Pin Berg Housing	22526	65039-039 (Lettered)	CS-237
P15	HDP-20 Economy connector	02660	205859-1	CS-306

COMPONENT DESIGNATION LISTING

Parts shown on Schematic Number 27864E, Sheet 2, Control and Output Logic

CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG.DESIGNATION	KEITHLEY PART NO.
	RESISTORS			
R5-R19,R23	180Ω, 10%,0.25W Comp.	01121	CB-181-10%	R-76-180
R24	330Ω, 10%, 0.25W, Comp.	01121	CB-331-10%	R-76-330
R25	680Ω, 10%, 0.25W, Comp.	01121	CB-681-10%	R-76-680
R26	470Ω, 10%, 0.25W, Comp	01121	CB-471-10%	R-76-470
R27,R28	3.3kΩ, 10%, 0.25W, Comp	01121	CB-332-10%	R-76-3.3k
R29	68.1Ω, 1%, 0.125W, MTF	75042	CEA-TO-68-1Ω	R-88-68.1
R42	33kΩ, 10%, 0.25W, Comp	01121	CB-333-10%	R-76-33k
R52,R53	470Ω, 10%, 0.25W, Comp	01121	CB-471-10%	R-76-470
R54	464Ω, 1%, 0.125W, MTF	75042	CEA-TO-464Ω	R-88-464
R55	158Ω, 1%, 0.125W, MTF	75042	CEA-TO-158Ω	R-88-158
R56	464Ω, 1%, 0.125W, MTF	75042	CEA-TO-464Ω	R-88-464
R57	158Ω, 1%, 0.125W, MTF	75042	CEA-TO-158Ω	R-88-158
R64	1kΩ, 10%, 0.25W, COMP	01121	CB-102-10%	R-76-1k
R65	22kΩ, 10%, 0.25W, COMP	01121	CB-223-10%	R-76-22k
R66	4.7kΩ, 10%, 0.25W, COMP	01121	CB-472-10%	R-76-4.7k
R67,R68	6.8kΩ, 10%, 0.25W, COMP	01121	CB-682-10%	R-76-6.8k
R69	100Ω, 10%, 0.25W, COMP	01121	CB-101-10%	R-76-100
R88	1kΩ, 10%, 0.25W, COMP	01121	CB-102-10%	R-76-1k
R122-R125	22kΩ, 10%, 0.25W, COMP	01121	CB-223-10%	R-76-22k
R176	150Ω, 10%, 0.25W, COMP	01121	CB-151-10%	R-76-150
R177-R201	10kΩ, 10%, 0.25W, COMP	01121	CB-103-10%	R-76-10k
R209	20kΩ, .75W, COMP VAR.	80294	CB-151-10%	R-76-150
	SWITCHES			
S2	Switch, Pushbutton	81073	46-101B	SW-381
S3	Switch, Rotary	80164	-	SW-382
	TRANSFORMERS			
T1-T3	Pulse Transformer	80164	-	720-11A

COMPONENT DESIGNATION LISTING

Parts shown on Schematic Number 27864E, Sheet 2, Control and Output Logic

CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG.DESIGNATION	KEITHLEY PART NO.
	INTEGRATED CIRCUITS			
U9	Hex Inverter, 14-Pin DIP	01295	SN7404N	IC-33
U10	Transistor Array	86684	CA3086	IC-53
U15	Dual NAND Schmitt Trigger, 14-Pin DIP	18314	N7413A	IC-121
U17	Monostable Multivibrator, 14-Pin DIP	01295	SN74121N	IC-118
U23,U24	Quad NAND, 14-Pin DIP	01295	SN7400N	IC-38
U46	Dual D Flip-Flop, 14-Pin DIP	01295	SN7474N	IC-31
U47	Dual NAND Schmitt Trigger, 14-Pin DIP	18314	N7413A	IC-121
U48	Dual D Flip-FLop, 14-Pin DIP	01295	SN7474N	IC-31
U49	Hex Buffer/Driver, 14-Pin DIP	01295	SN7417N	IC-101
U53	Quad NAND Gates, 14-Pin DIP	04713	MC858P	IC-52
U54	5-Bit Shift Register, 16-Pin DIP	01295	SN7496N	IC-39
U55	8-Bit Parallel-Out Serial Shift Register, 14-Pin DIP	01295	SN74164J	IC-119
U64	Monostable Multivibrator, 14-Pin DIP	01295	SN74121N	IC-118
U65	Quad NAND Gates, 14-Pin DIP	04713	MC858P	IC-52
U66	Positive NOR Gates, 14-Pin DIP	01295	SN7402N	IC-32
U67	Hex Buffer/Driver, 14-Pin DIP	01295	SN7417N	IC-101
U74	Hex Inverter, 14-Pin DIP	01295	SN7404N	IC-33
U75-U77	Quad NAND Gates, 14-Pin DIP	04713	MC858P	IC-52
	CRYSTAL			
Y1	Crystal, 1MHz	80164	-	CR6

Model 720

COMPONENT DESIGNATION LISTING

Parts shown on Schematic Number 27864E, Sheet 3, Power Supply and Isolated A/D Section.

CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG. DESIGNATION	KEITHLEY PART NO.
	CAPACITORS			
C1	100μF, 15V, EAL	29309	JC6100158P	C-210-100
C4	56μF, 20V, ETT	06751	TD5-020-566-20	C-179-56
C5	2000μF, 25V, EAL	29309	JC-P-2000-25-8P	C-225-2000
C6	0.1μF, 250V, MTF	73445	C280AE	C-178-1
C7	0.1μF, 16V, CER.D.	71590	Uk16-104	C-238-.1
C8	330pF, 1000V, CER.D.	71590	DD-331	C-64-330P
C9,C10	100μF, 15V, EAL	29309	JC6100158P	C-210-100
C11	0.1μF, 250V, MTF	73445	C280AE	C-178-.1
C12-C15	0.1μF, 16V, CER.D.	71590	UK16-104	C-238-.1
C18	4700pF, 1000V, CER.D.	56289	10SS-D47	C-64-4700P
C19-C22	0.1μF, 16V, CER.D.	71590	UK16-104	C-238-.1
C27	22μF, 20V, ETT	06751	TD1-20-226-20	C-179-22
C29	330pF, 1000V, CER.D.	71590	DD-331	C-64-330P
C30	22μF, 20V, ETT	06751	TD1-20-226-20	C-179-22
C31	2000μF, 25V, EAL	29309	JC-P-2000-25-8P	C-225-2000
C35-C42	0.1μF, 16V, CER.D.	71590	UK16-104	C-238-.1
C43	2000μF, 25V, EAL	29309	JC-P-2000-25-8P	C-225-2000
044	0.1μF, 250V, MTF	73445	C280AE	C-178-.1
C45	6800pF, 500V, CER.D.	72982	851-Z5U0-682M	C-22-6800P
C46	0.01μF, 600V, CER.D.	72982	871-Z540-103M	C-22-.01
C47	10,000μF, 15V	90201	TCG103U015N3C3P	C-266-10,000
C48-C50	0.1μF, 16V, CER.D.	71590	UK16-104	C-238.1
C51	.039μF, 50V, POLY	80164	-	C-267-.039
C52	* , 500V, POLY	71590	-	C-138-*
C53	* , 500V, POLY	71590	-	C-138-*
C54	.0039μF, 50V, POLY	80164	-	C-267-.0039
C55	.39μF, 50V, POLY	80164	-	C-267-.39
C56	* , 500V, POLY	71590	-	C-138-*
C59	.47μF, 20V, ETT	06751	TD1-20-474-20	C-179-.47
C60, C61	0.1μF, 16V, CER.D.	71590	UK16-104	C-238-.1
C62	100μF, 15V, EAL	29309	JC6100158P	C-210-100

*Nominal value selected at factory.

COMPONENT DESIGNATION LISTING

CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG. DESIGNATION	KEITHLEY PART NO.
	RECTIFIERS			
CR1,CR2,CR7-CR10	Rectifier, 74mA, 75V	01295	1N914	RF-28
CR11	Rectifier, 2A, 100V	80164	-	RF-36
CR12-CR15	Rectifier, 72mA, 75V	01295	1N914	RF-28
CR16-CR17	Rectifier, 1A, 800V	04713	1N4006	RF-38
CR18-CR28	Rectifier, 75mA, 75V	01295	1N914	RF-28
CR-29, CR30	Rectifier, 3A, 50V	80174	-	RF-34
CR31-CR36	Rectifier, 75mA, 75V	01295	1N914	RF-28
	CONNECTORS			
J20	Connector, Triaxial	95712	33050-2-NT-34	CS-181
J1-J3	Connector, 2-Pin Berg Housing	22526	65039-034(Lettered)	CS-266
J10,J11	Connector, 3-Pin Berg Housing	22526	65039-034(Lettered)	CS-270
J12	11-Pin Molex, Female	80164	-	CS-287-11
J13	3-Pin Molex, Female	80164	-	CS-287-3
P12	11-Pin Molex, Male	80164	-	CS-288-11
P13	3-Pin Molex, Male	80164	-	CS-288-3
	RELAYS			
K1-K15	Relay	80164	-	RL-40
	TRANSISTORS			
Q1	Transistor	04713	2N3905	TG-53
Q2	Transistor	02735	40319	TG-50
Q3	Transistor	04713	2N3903	TG-49
Q4	Transistor	02735	40317	TG-43
Q5	Transistor	04713	2N5875	TG-114
	RESISTORS			
R1	3Ω, 5%, 0.5W, Comp	75042		R-19-3
R2	32.4kΩ, 1%, 0.125W, MTF	75042	CEA-TO-32.4k	R-88-32.4K
R3	64.9kΩ, 1%, 0.125W, MTF	75042	CEA-TO-64.9k	R-88-64.9k
R4	180Ω, 10%,0.25W, COMP	01121	CB-181-10%	R-76-180
R20	22kΩ, 10%, 0.25W, COMP	01121	CB-223-10%	R-76-22k
R21	1kΩ, 10%, 0.25W, COMP	01121	CB-102-10%	R-76-1k
R30	158Ω, 1%, 0.125W, MTF	75042	CEA-TO-158Ω	R-88-158
R31	464Ω, 1%, 0.125W, MTF	75042	CEA-TO-464Ω	R-88-464
R32,R33	470Ω, 10%, 0.25W, COMP	01121	CB-471-10%	R-76-470
R34	2.2kΩ, 10%, 0.25W, COMP	01121	CB-222-10%	R-76-2.2k
R35,R36	Potentiometer, .3W	80294	3279W	RP-94-20k

COMPONENT DESIGNATION LISTING

CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG. DESIGNATION	KEITHLEY PART NO.
	RESISTORS - Cont'd			
R37	97.6kΩ, 1%, 0.125W, MTF	75042	CEA-TO-97.6k	R-88-97.6k
R38	32.4kΩ, 1%, 0.125W, MTF	75042	CEA-TO-32.4k	R-88-32.4k
R39	22kΩ, 10%, 0.25W, COMP	01121	CB-223-10%	R-76-22k
R40	180Ω, 10%, 0.25W, COMP	01121	CB-181-10%	R-76-180
R41	1kΩ, 10%, 0.25W, COMP	01121	CB-102-10%	R-76-1k
R44	1.5MΩ, 10%, 0.25W, COMP	01121	CB-155-10%	R-76-1.5M
R45	150kΩ, 10%, 0.25W, COMP	01121	CB-154-10%	R-76-150k
R58-R61	4.7kΩ, 10%, 0.25W, COMP	01121	CB-472-10%	R-67-4.7k
R62	1kΩ, 10%,o.25W, COMP	01121	CB-102-10%	R-76-1k
R63	3Ω, 5%, 0.5W, COMP	75042	-	R-19-3
R70, R71	470Ω, 10%, 0.25W, COMP	01121	CB-471-10%	R-76-470
R72	464Ω, 1%, 0.125W, MTF	75042	CEA-TO-464Ω	R-88-464
R73	158Ω, 1%, 0.125W, MTF	75042	CEA-TO-158Ω	R-88-158
R74	464Ω, 1%, 0.125W, MTF	75042	CEA-TO-464Ω	R-88-464
R75	158Ω, 1%, 0.125W, MTF	75042	CEA-TO-158Ω	R-88-158
R78	1kΩ, 10%, 0.25W, COMP	01121	CB-102-10%	R-76-1k
R79	33kΩ, 10%, 0.25W, COMP	01121	CB-333-10%	R-76-33k
R80	1kΩ, 10T, 0.25W, COMP	01121	CB-102-10%	R-76-1k
R81	33kΩ, 10%, 0.25W, COMP	01121	CB-333-10%	R-76-33k
R82	1kΩ, 10%, 0.25W, COMP	01121	CB-102-10%	R-76-1k
R83, R84	33kΩ, 10%, 0.25W, COMP	01121	CB-333-10%	R-76-33k
R85	1.8kΩ, 10%, 0.25W, COMP	01121	CB-182-10%	R-76-1.8k
R86	4.7kΩ, 10%, 0.25W, COMP	01121	CB-472-10%	R-76-4.7k
R87	100kΩ, 10%, 0.25W, COMP	01121	CB-104-10%	R-76-100k
R89	Potentiometer, .5W	80294	3299W-1-101	RP-104-100
R126	1.15MΩ, 1%, .5W, MTE	75042	CEC-TO-1.15MΩ	R-94-1.15M
R127	10kΩ, .1%, 0.5W, MTF	91637	MFF-½-10kΩ	R-169-10k
R128	33Ω, 10%, 0.25W, COMP	01121	CB-330-10%	R-76-33
R129	400kΩ, .1%, 0.5W, MTF	91637	MFF-½-400kΩ	R-169-400k
R130	800kΩ, .1%, 0.5W, MTF	91637	MFF-½-800kΩ	R-169-800k
R131	1MΩ, .1%, 0.5W, MTF	91637	MFF-½-1MΩ	R-169-1M
R132	2MΩ, .1%, 0.5W,	91637	HMF-½-2MΩ	R-174-2M
R133	4MΩ, .1%, 0.5W	91637	HMF-½-4MΩ	R-174-4M
R134	8MΩ, .1%, 0.5W	91637	HMF-½-8MΩ	R-174-8M
R202	200kΩ, .1%, 0.5W, MTF	91637	MFF-½-200kΩ	R-169-200k

COMPONENT DESIGNATION LISTING

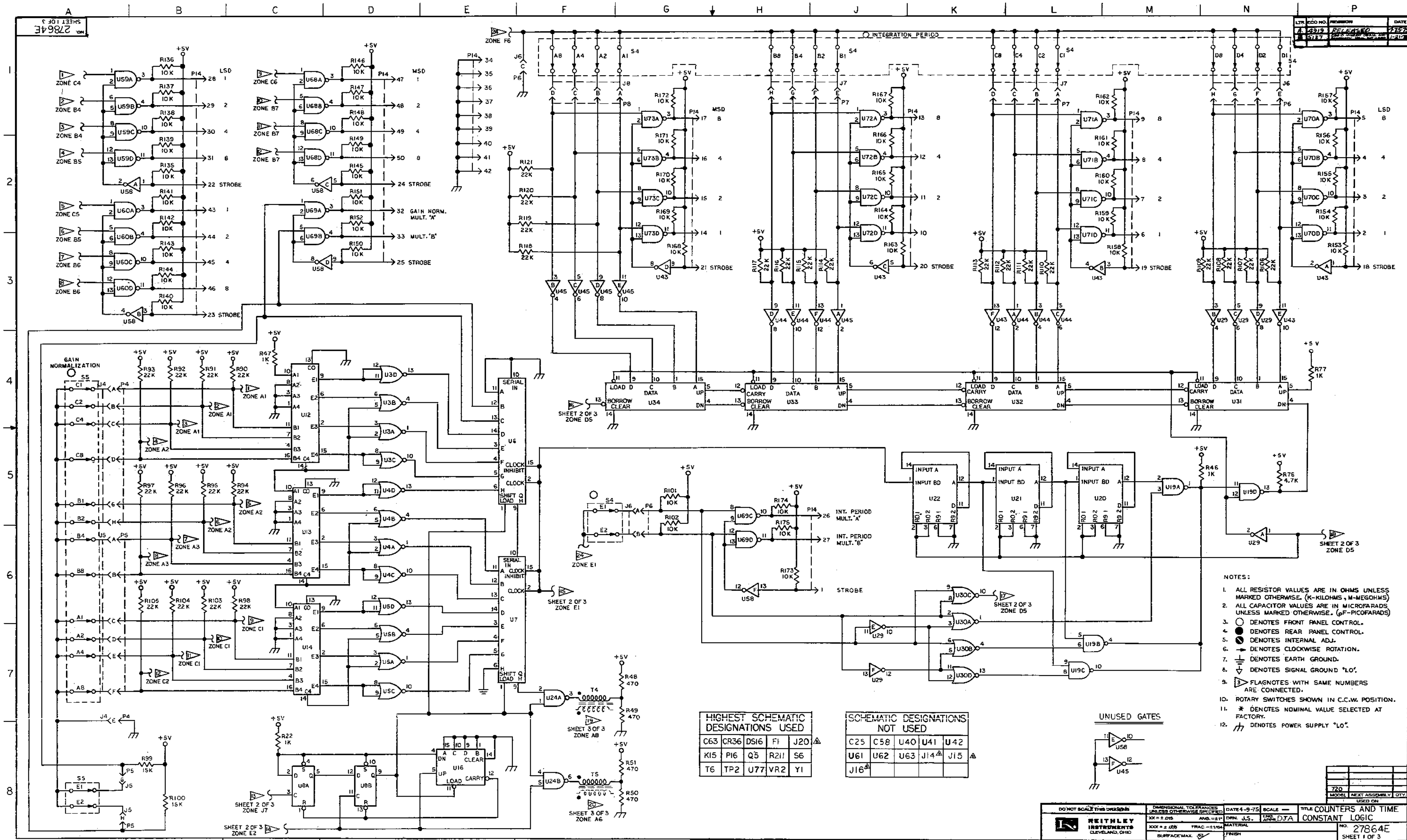
CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG. DESIGNATION	KEITHLEY PART NO.
	RESISTORS - Cont'd			
R203	100kΩ, .1%, 0.5W, MTF	91637	MFF-½-100kΩ	R-169-100k
R204	80kΩ, .1%, 0.5W, MTF	91637	MFF-½-80k Ω	R-169-80k
R205	40kΩ, .1%, 0.5W, MTF	91637	MFF-½-40kΩ	R-169-40k
R206	20kΩ, .1%, 0.5W, MTF	91637	MFF-½-20kΩ	R-169-20k
R207	10kΩ, .1%, 0.5W, MTF	91637	MFF-½-10kΩ	R-169-10k
R208	Potentiometer	80294	3006P	RP-89-1k
R210,R211	Potentiometer, 2W	80294	3540S-566-102	RP-113-1k
	TRANSFORMERS			
T1-T3	See Component Designation listing for Sheet 2			
T4, T5	See Component Designation listing for Sheet 1			
T6	Transformer, Power	80164	-	TR-161
	INTEGRATED CIRCUITS			
U1	Dual NAND Schmitt Trigger 14-Pin DIP	18324	N7413A	IC-121
U2, U11	Operational Amplifier	18324	N741V	IC-42
U18	Module, A/D Converter	80164	-	MO-2
U25	Dual NAND Schmitt Trigger 14-Pin DIP	18324	N7413A	IC-121
U26	Quad NAND, 14-Pin DIP	01295	SN7400N	IC-38
U27	Dual D Flip-Flop, 14-Pin DIP	01295	SN7474N	IC-31
U28	Quad, 2 Input Pos NAND,14-Pin DIP	01295	SN7401	IC-47
U35,U36	8-Bit Shift Register	01295	SN74164J	IC-119
U37	Hex Inverter, 14-Pin DIP	01295	SN7404N	IC-33
U38	Quad, Open Collector & Gates	01295	SN7409N	IC-122
U39	Transistor Array	02735	CA3086	IC-53
U50,U51	Hex Inverter, 14-Pin DIP	01295	SN7404N	IC-33
U52	Operational Amplifier	18324	N741V	IC-42
U57	Three Mode Integrator	80164	-	MO-1

COMPONENT DESIGNATION LISTING

CIRCUIT DESIGNATION	DESCRIPTION	MFG CODE	MFG. DESIGNATION	KEITHLEY PART NO.
	MISCELLANEOUS			
F1	Fuse, 3/4 A Slo-Blo, 250V for 115 volt operation	80164	-	FU-19
	Fuse, 3/8A Slo-Blo, 250V for 230 volt operation	80164	-	FU-18
P6	AC Receptacle	82389	EAC-301	CS-254
-	Cord Set	70903	-	CO-7
S1	Switch, Toggle	80164	-	SW-236
S6	Switch, Slide	80164	-	SW-388
-	Heat Sink for TG-43, TG-50	80164	-	HS-9
-	Heat Sink for IC-34	80164	-	HS-11
-	Socket for CR-6	80164	-	SO-62
-	Socket for MO-1	80164	-	SO-74
-	Berg Pins	80164	-	24249A
-	Contact (Molex)	80164	-	CS-276
-	Pins, Wire-Wrap	22526	75401-009	CS-312
-	Shorting Link	24655	938-L	BP-6

The 720 pc board has room for three 16-pin sockets, three 14-pin sockets and wire-wrap pins for the customer's own use. The following is a list of parts required:

DESCRIPTION	MFG CODE	MFG. DESIGNATION	KEITHLEY PART NO.
Pins, wire-wrap	22526	75401-009	CS-312
Socket, 16-Pin	80164	-	SO-65
Socket, 14-Pin	80164	-	SO-70



NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS UNLESS MARKED OTHERWISE. (K-KILOHMS, M-MEGOHMS)
2. ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS MARKED OTHERWISE. (pF-PICOFARADS)
3. ○ DENOTES FRONT PANEL CONTROL.
4. ● DENOTES REAR PANEL CONTROL.
5. DENOTES INTERNAL ADJ.
6. DENOTES CLOCKWISE ROTATION.
7. DENOTES EARTH GROUND.
8. DENOTES SIGNAL GROUND "LO".
9. FLAGNOTES WITH SAME NUMBERS ARE CONNECTED.
10. ROTARY SWITCHES SHOWN IN C.C.W. POSITION.
11. * DENOTES NOMINAL VALUE SELECTED AT FACTORY.
12. DENOTES POWER SUPPLY "LO".

UNUSED GATES

HIGHEST SCHEMATIC DESIGNATIONS USED				
C63	CR36	DS16	F1	J20
K15	P16	Q5	R211	S6
T6	TP2	U77	VR2	Y1

SCHEMATIC DESIGNATIONS NOT USED				
C25	C58	U40	U41	U42
U61	U62	U63	J14	J15
J16				

MODEL	NEXT ASSEMBLY	QTY.
720		

USED ON

DO NOT SCALE THIS DRAWING

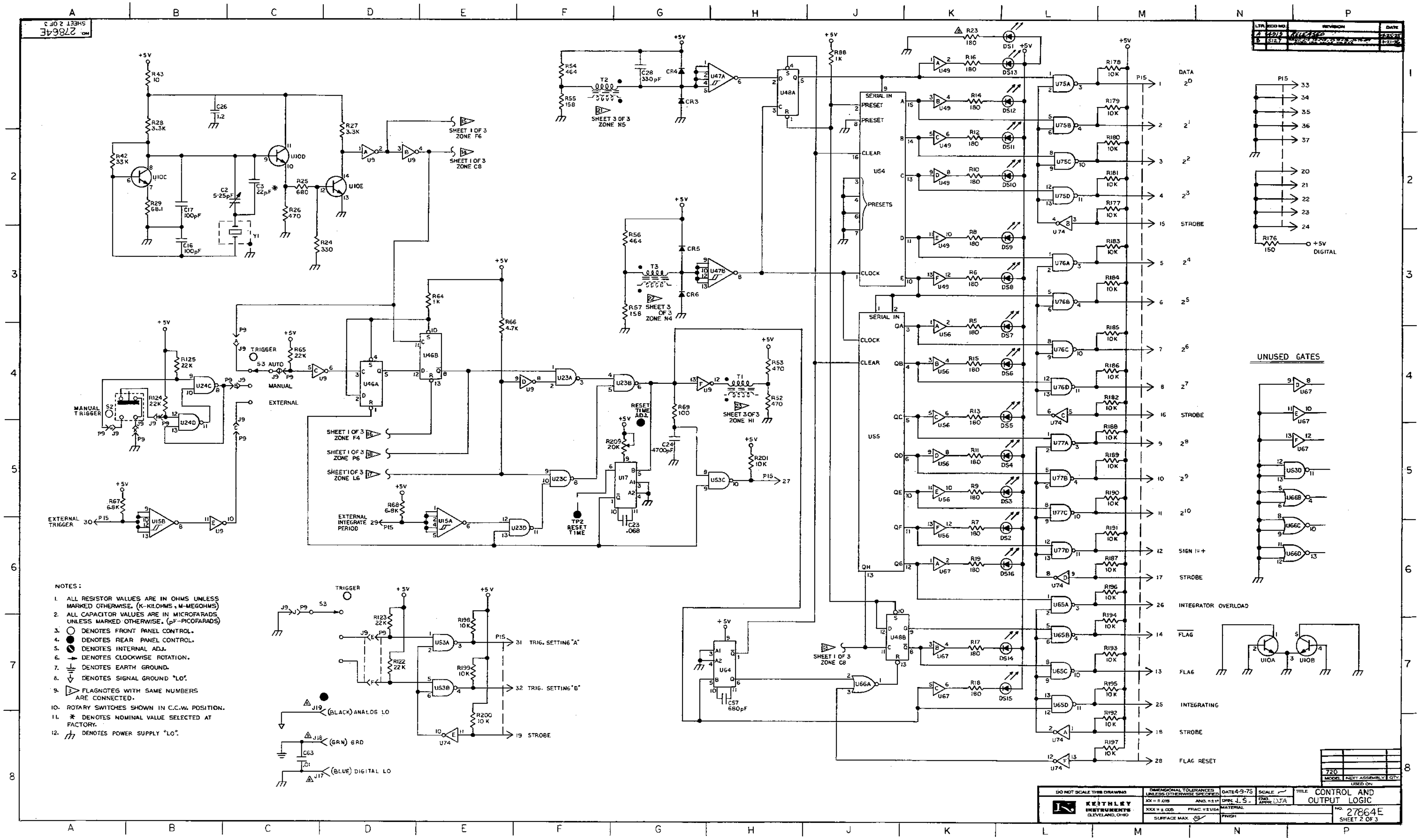
KEITHLEY INSTRUMENTS CLEVELAND, OHIO

DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED
XX = ± .015 ANG. = ±1°
XXX = ± .005 FRAC. = ±1/64
SURFACE MAX. 63

DATE 4-9-75 SCALE —
DRN. J.S. ENG. APPR. DJA
MATERIAL
FINISH

TITLE COUNTERS AND TIME CONSTANT LOGIC

NO. 27864E
SHEET 1 OF 3



NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS UNLESS MARKED OTHERWISE. (K-KILOHMS, M-MEGOHMS)
2. ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS MARKED OTHERWISE. (pF-PICOFARADS)
3. ○ DENOTES FRONT PANEL CONTROL.
4. ● DENOTES REAR PANEL CONTROL.
5. DENOTES INTERNAL ADJ.
6. DENOTES CLOCKWISE ROTATION.
7. DENOTES EARTH GROUND.
8. DENOTES SIGNAL GROUND "LO".
9. FLAGNOTES WITH SAME NUMBERS ARE CONNECTED.
10. ROTARY SWITCHES SHOWN IN C.C.W. POSITION.
11. * DENOTES NOMINAL VALUE SELECTED AT FACTORY.
12. DENOTES POWER SUPPLY "LO".

720		
MODEL	NEXT ASSEMBLY	QTY
USED ON		

DO NOT SCALE THIS DRAWING

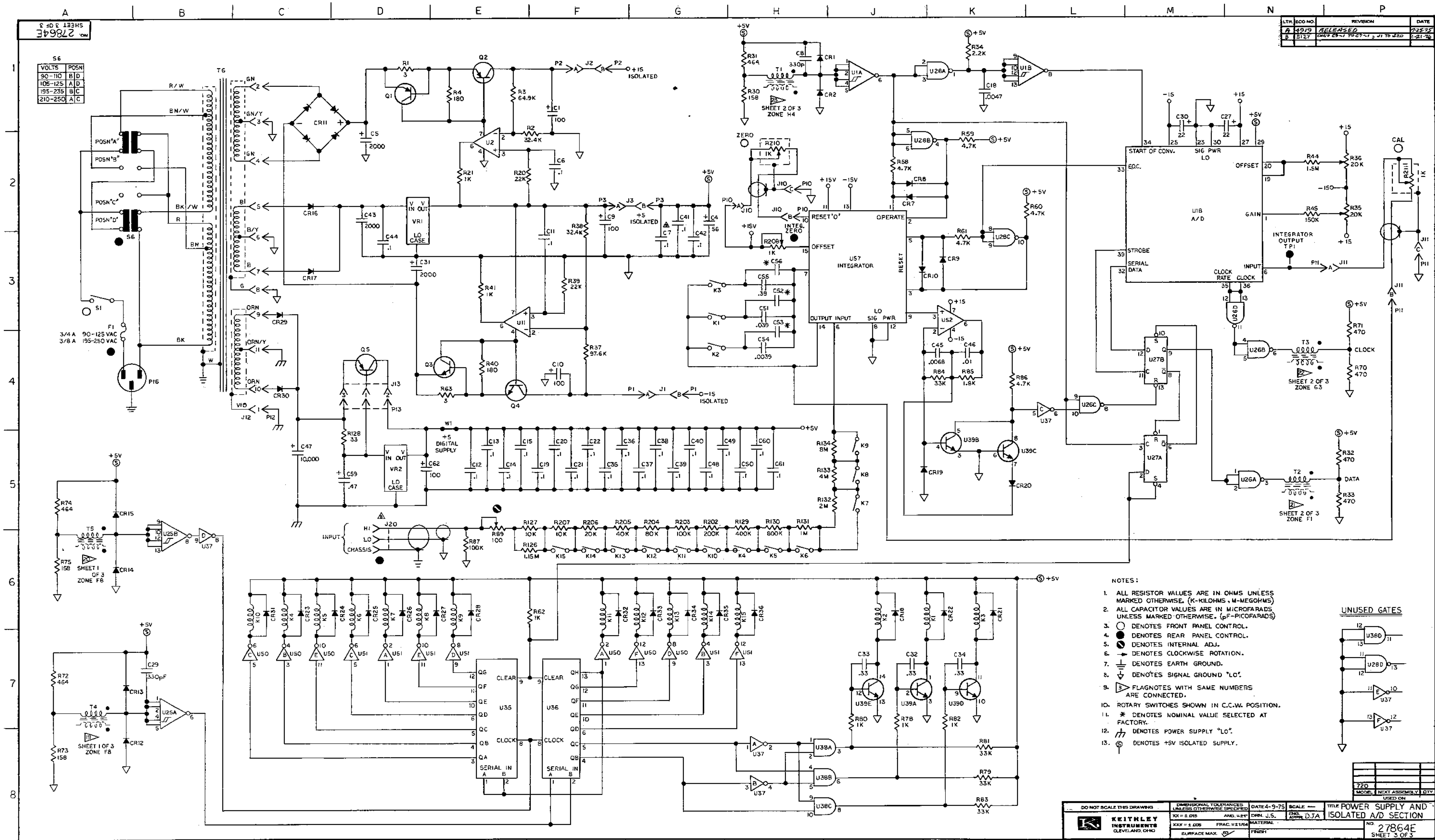
DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED
XX = ±.015 ANG. ±1°
XXX = ±.005 FRAC. ±1/64
SURFACE MAX.

KEITHLEY INSTRUMENTS CLEVELAND, OHIO

DATE 4-9-75 SCALE —
DRN. J.S.
ENG. APPR. DJA
MATERIAL
FINISH

TITLE CONTROL AND OUTPUT LOGIC

NO. 27864E
SHEET 2 OF 3



NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS UNLESS MARKED OTHERWISE. (K-KILOHMS, M-MEGOHMS)
2. ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS MARKED OTHERWISE. (pF-PICOFARADS)
3. ◯ DENOTES FRONT PANEL CONTROL.
4. ● DENOTES REAR PANEL CONTROL.
5. DENOTES INTERNAL ADJ.
6. DENOTES CLOCKWISE ROTATION.
7. DENOTES EARTH GROUND.
8. DENOTES SIGNAL GROUND "LO".
9. FLAGNOTES WITH SAME NUMBERS ARE CONNECTED.
10. ROTARY SWITCHES SHOWN IN C.C.W. POSITION.
11. * DENOTES NOMINAL VALUE SELECTED AT FACTORY.
12. DENOTES POWER SUPPLY "LO".
13. DENOTES +5V ISOLATED SUPPLY.

UNUSED GATES

LTR	ECO NO.	REVISION	DATE
A	4919	RELEASED	7-25-75
B	5127	CHGD C9-1 TO C9-1 ; J1 TO J20	1-21-76

DO NOT SCALE THIS DRAWING

KEITHLEY INSTRUMENTS CLEVELAND, OHIO

DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED: XX = ±.015, XXX = ±.005, ANG. ±2°, FRAC. ±1/64

DATE 4-9-75 · SCALE — · DRN. J.S. · ENG. APPR. DJA

TITLE: POWER SUPPLY AND ISOLATED A/D SECTION

MODEL 720

NO. 27864E SHEET 3 OF 3