INSTRUCTION MANUAL

Control Unit

Model 780

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CONTENTS

ILLUSTRATIONS

SPECIFICATIONS

GENERAL: Holds up to three System 1 Instrument Interface or special-purpose cards. Supplies power to cards. Captive cable plugs directly into the System 1 Programmable Calculating Unit.

DISPLAY: 18 LED lamps indicate the last Output 8-bit word transferred, the next 8-bit word to be Input, and whether the last word transferred was Data or Control.

CONTROLS: Front panel power switch. Internal switch sets Control Unit address.

702/702X INTERFACE:

GENERAL: Built-in interface connects directly to one Model 702/702X 10-channel Scanner, or with 7819-MSC, to as many as eight 10-channel Scanners for random access to single channels. For parallel-channel or matrix operation, one channel on each Scanner may be selected.

OUTPUT INSTRUCTION:

Control Transfer: Deactivates all or selectively activates one of up to 80 channels.

Power up/Reset: All scanner channels Off.

Nominal Instruction Time: 70 milliseconds.

ISOLATION (PCU GROUND TO ANALOG LO): Provided by Model 702X plug-in cards.

ENVIRONMENT:

OPERATING: 0°C to 40°C up to 80% relative humidity.

STORAGE: -25°C to 80°C

POWER: 90-110, 105-125, 210-250 volts (switch selected), 50-60 Hz, 50 watts.

DIMENSIONS,WEIGHT: 3-1/2 in. full rack, overall bench size 4 in. high x 17-1/4 in. wide x 15-1/2 in. deep (105 x 440 x 395 mm); 5 ft. (1-1/2m) captive cable to PCU. Net weight, 13 pounds (5,8 kg).

ACCESSORIES FURNISHED: Hardware for standard 3-1/2 in. x 19 in. rack mounting. 15-1/2 in. (395 mm) depth behind front panel.

SECTION 1. GENERAL INFORMATION

1-1. INTRODUCTION. The Model 780 Control Unit provides the link between the Programmable Calculating Unit (PCU) and all other instrumentation in the System 1. The Control Unit may be used with up to three Instrument Interfaces or other devices and eight Scanners. (A PCU and appropriate I/O Handler Software is needed to communicate with the Control Unit.)

Instrument Interfaces may be installed in any of three rear panel plug-in compartments or "slots". The locations of the Instrument Interfaces are labeled as Interface Number 1, 2, and 3.

Scanner interface circuitry is built into each Control Unit. The rear panel "SCANNER" connector mates with a System Interconnect Cable (Model 7021-2) furnished with the Keithley Model 702 Scanner.

When a Multi-Scanner Coupler is connected to the Control Unit, up to eight Scanners (80 channels total) may be used. Each Scanner connects to the MSC via individual System Interconnect Cables.

The Control Unit has 18 indicators on the front panel which display pertinent information as to the status of System 1 operations.

- INPUT Indicators: These indicators represent an 8-bit word to be transferred from the Control Unit to the PCU.
- OUTPUT Indicators: These indicators represent an 8-bit word which has been transferred from the PCU.
- DATA Indicator: This indicator identifies the last 8-bit word transferred as DATA.
- CONTROL Indicator: This indicator identifies the last 8-bit word transferred as a CONTROL byte.

In a System 1/782-XY, two Control Units are used. In this configuration an internal switch on each Control Unit is used to identify Control Unit #1 (CU1) and Control Unit #2 (CU2) in the System. This identification enables the user to communicate to either Control Unit via I/O Handler Software. A Dual Control-Unit Coupler must be installed on either Control Unit CU1 or CU2 to facilitate connection of a second Control Unit. The Control Units may be rack mounted using hardware furnished. The captive cable on the Control Unit is five feet long and mates with a 37-pin connector on the PCU or 2nd Control Unit. Cabling to instrument or other devices is furnished with individual Instrument Interfaces.

1-2. WARRANTY INFORMATION. See *GUIDE TO USING THE SYSTEM 1* for detailed information.

1-3. CHANGES. Improvements or changes to the Control Unit which are not incorporated into the *INSTRUCTION MANUAL* can be found in the System 1 *Instruction Manual Addenda*.

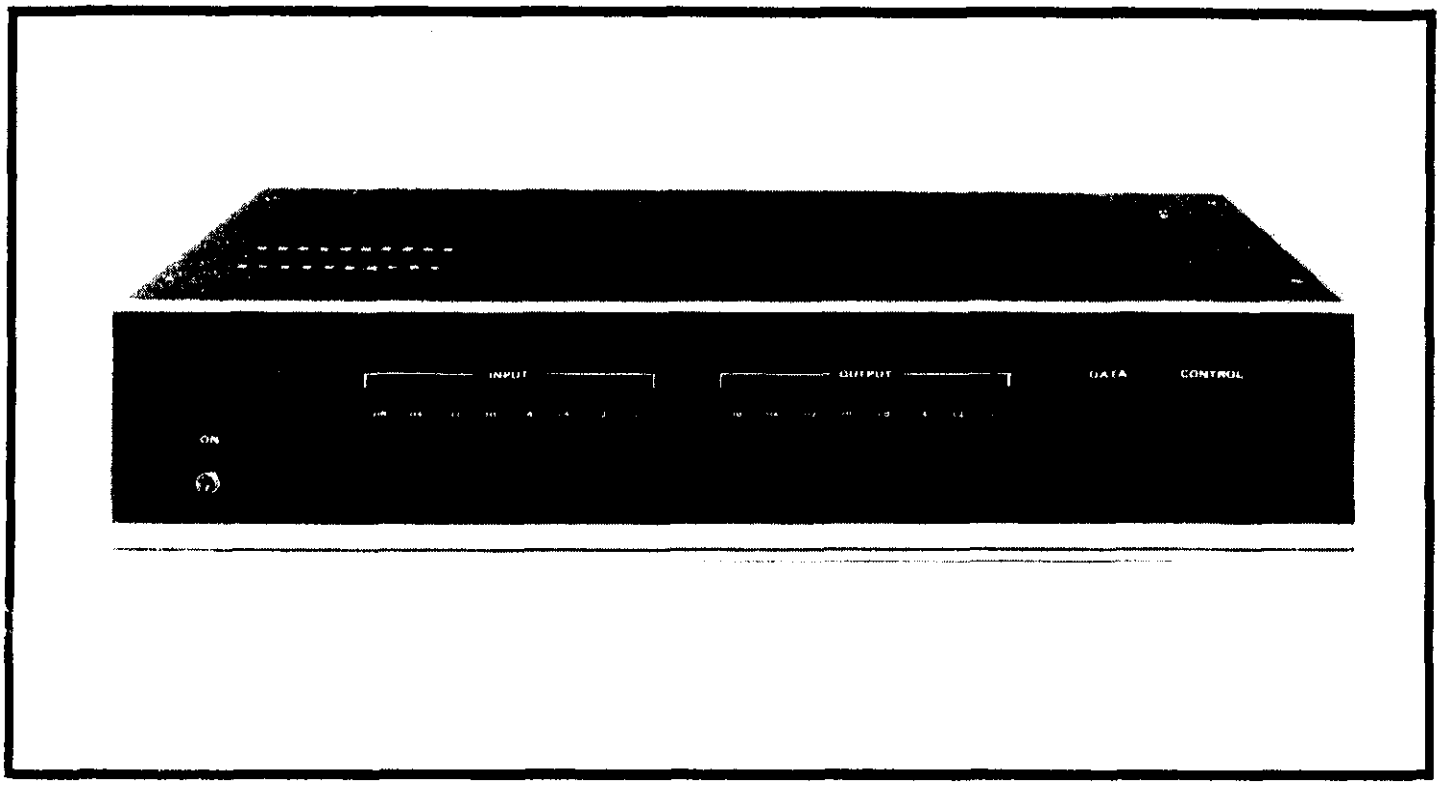


FIGURE 1. Front Panel.

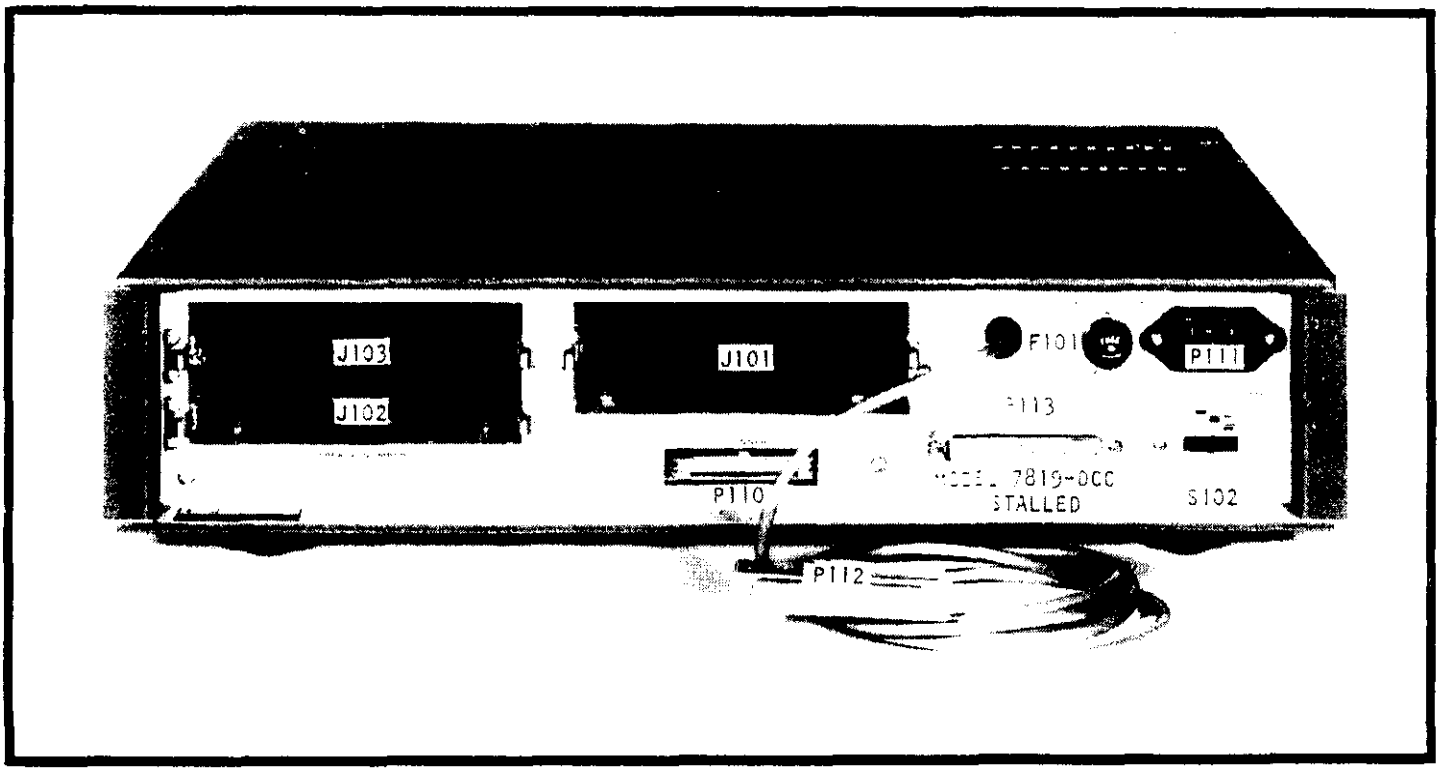


FIGURE 2. Rear Panel.

SECTION 2. INITIAL PREPARATION

2-1. GENERAL. This section provides information needed for incoming inspection and preparation for use.

2-2. INSPECTION. The equipment furnished was carefully inspected both mechanically and electrically before shipment. Upon receiving the equipment, check for obvious damage which may have occured during transit. Report any damage to the shipping agent and your Keithley representative.

2-3. SYSTEM CONSIDERATIONS. The Control Unit is used in all configurations of the System 1 Calculator-Based Instrumentation System. It is recommended that the user determine the configuration to be used prior to placing the Control Unit in the System. The following factors should be considered:

a. Use of more than one Control Unit. The Control Unit has an internal switch (S103) which is set at the factory in CU1 position, to designate the Control Unit as "Control Unit 1". If two Control Units are to be used in the System 1, the Dual Control-Unit Coupler must be incorporated and the second Control Unit must be designated as CU2. If only one Control Unit is used, no modification of the Control Unit is needed. See Figure 5 for location of internal switch S103.

TABLE 2-1.

Control Unit Useage in System 1

Model No.	Number of Control Units Needed	Dual Control-Unit Coupler	S103 Setting
System 1/781	1	Not Required.	CU1
System 1/782	2	Required. See Table 2-4.	First unit-CU1 Second unit-CU2

b. Use of two or more Scanners. If two or more Scanners are to be used in the System 1, the Multi-Scanner Coupler must be used with the Control Unit. (See page 6-2.)

c. Use of more than one Instrument Interface. If more than one Instrument Interface is installed in a Control Unit at the same time, Model 7820-GPA I/O Handler Software must be used. See *GUIDE TO USING THE SYSTEM 1* for system hardware and software requirements.

2-4. HOW TO INSTALL INTERFACES. (SERIES 7801, 7802, 7813)

a. Locations. The rear panel of the Control Unit has three plug-in compartments, identified as Interface Numbers 1, 2, and 3. These compartments can accept any Keithley Instrument Interface or Accessory listed in Table 2-2.

TABLE 2-2.

Instrument Interfaces and Accessories Useable in the System 1

Model No.	Name
Model 7801-160B/1602B	Instrument Interface
Model 7801-171/1712	Instrument Interface
Model 7801-180/1802	Instrument Interface
Model 7801-445	Instrument Interface
Model 7801-616/6162	Instrument Interface
Model 7802-110	8-Bit Isolated I/O Interface
Model 7813	Interval Timer/Clock
Model 7802-CIK	Custom Interface Card
Model 7819-IEC	Interface Extender Card

b. Installation. Any Keithley System 1 Interface will mate with any of the three plug-in compartments. Slide the Plug-in Card into the compartment with "component side" facing up. Make certain the card edges are aligned with the grooves in the compartment. When the card is fully inserted, the "locking tabs" on the card should be snapped into locking position as shown in Figure 3. On some Instrument Interfaces a switch setting must be made on the pc card prior to installing in the Control Unit. (See *INSTRUCTION MANUAL, Instrument Interface.*)

c. Removal. Unfasten "locking tabs" by pulling both tabs outward. Grasp the end of the card and pull out of chassis.

2-5. HOW TO RACK MOUNT THE CONTROL UNIT. The Control Unit is designed for 19 inch full rack mounting when used with the Model 1007 Rack Mounting Kit. The position of the Control Unit in a rack should be determined relative to the instruments or devices used in the System 1. For example, Series 7801 Instrument Interfaces have a 6 foot (2m) length cable which mates with a digital measuring instrument. Therefore considerations should be made for cable routing behind the rear panel. See page 6-1 for rack mounting information.

2-6. HOW TO APPLY POWER TO THE CONTROL UNIT.

a. How to set the Line Switch. The Control Unit has a single Line Switch which permits the user to select line voltage in three ranges. See Table 2-3.

CAUTION

Remove line cord before changing switch positions.

TABLE 2-3.

Line Voltage Selection

Position	Line Voltage	Fuse (Keithley Part No.)
	90-110V rms	1/2A (FU-4)
	105-125V rms	1/2A (FU-4)
	210-250V rms	1/4A (FU-17)

b. Line Power. The Control Unit line power receptacle mates with Keithley line cord CO-7 (furnished). The line cord is designed for use with three-prong receptacles having a grounded connection.

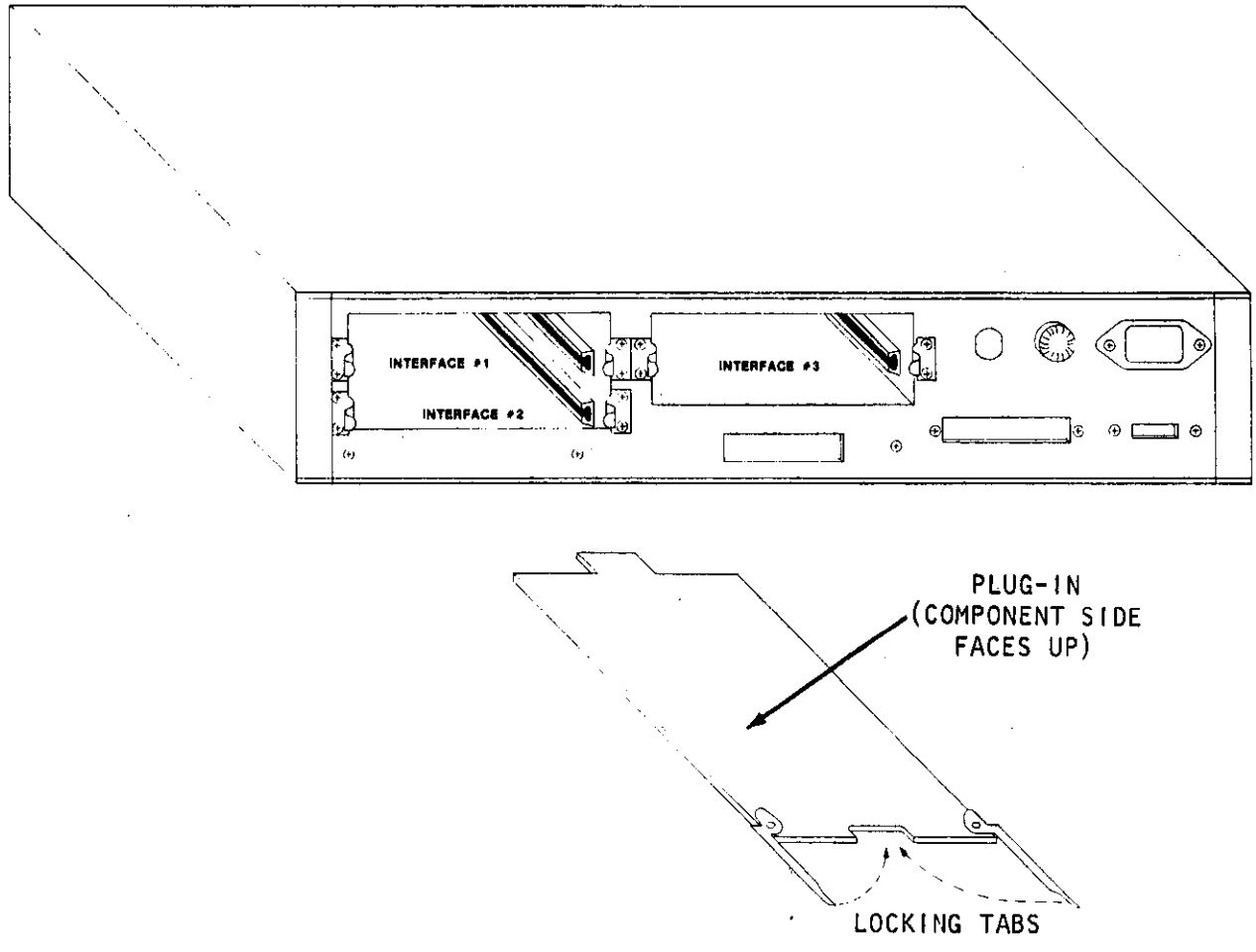


FIGURE 3. Installation of Series 7801, 7802, 7819-IEC and 7813 Cards.

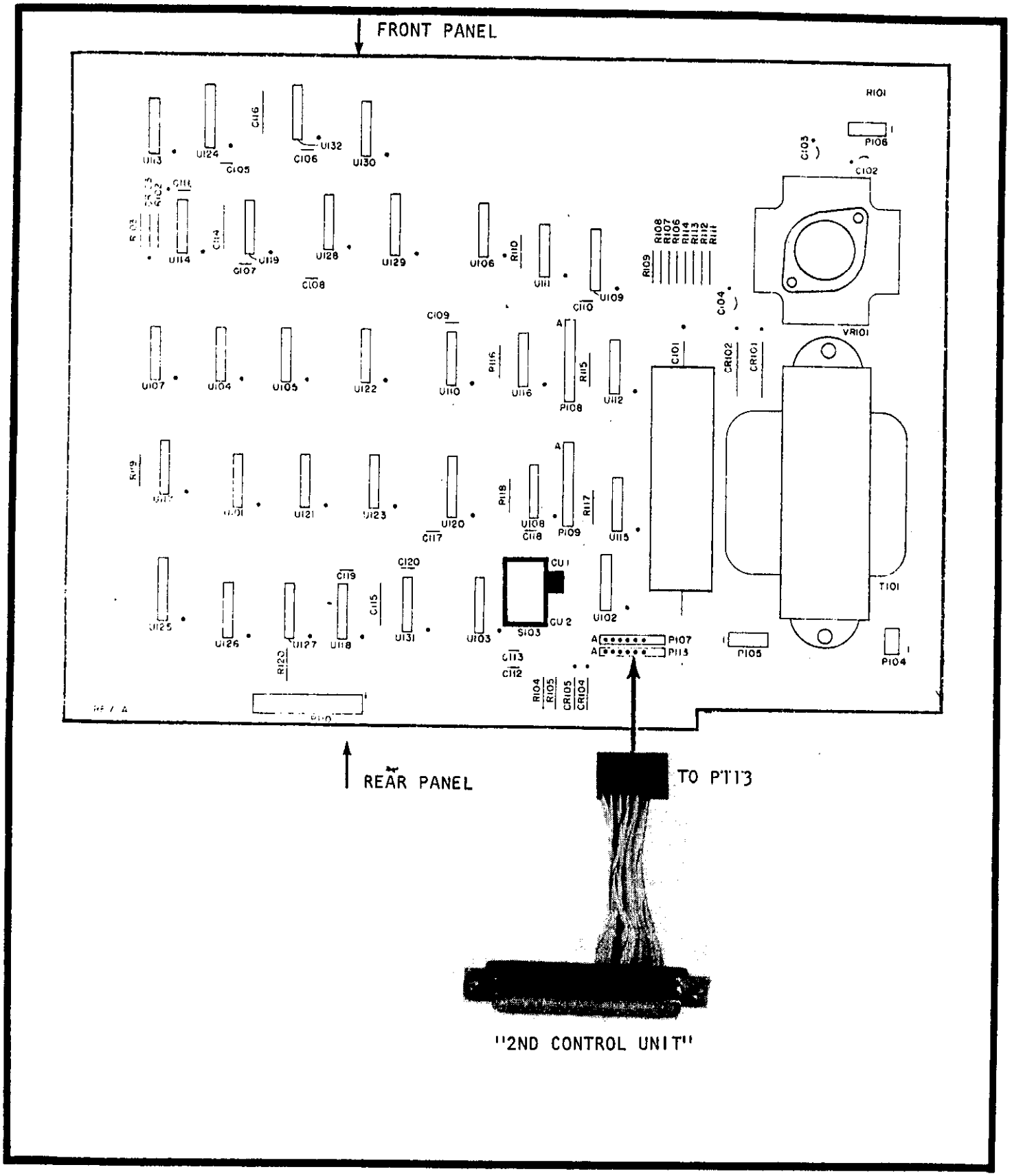


FIGURE 4. Installation of Dual Control Unit Coupler (Model 7819-DCC).

c. Power-Up Reset. When power is applied to the Control Unit a "Power-Up" reset is generated which causes all installed interfaces to go to their specific "power up" condition. The "power up" condition is listed in *INSTRUCTION MANUAL, Instrument Interface,* Series 7801, 7802 or 7813.

2-7. HOW TO USE REAR PANEL CONNECTORS (See Figure 2).

a. SCANNER Connector (P110). This connector is a 26-pin 3M Electro Products Division Part No. 3429. Pin 4 has been removed to admit a "polarizing key" on the mating System Interconnect Cable (Model 7021-2 or 7021-10).

b. TO PCU Cable (P112). This five foot long cable is a 37-conductor integrally mounted cable terminated by an ITT Cannon Part No. DC-37P male connector. The cable mates with a receptacle on Keithley PCU, Peripheral Coupler, or second Control Unit.

c. 2ND CONTROL UNIT (Spare opening). This opening is used when modifying a Control Unit for use in a System 1/782. When shipped from the factory the Control Unit has a cover plate (part no. 26864) over the opening. When a Dual Control-Unit Coupler is installed on the Control Unit the cover plate must be removed and replaced with a 37-pin receptacle. See Table 2-4 and Figure 4.

d. INTERFACE NUMBER 1 (J103). This connector is a 50-pin card-edge type which mates with Series 7801 and 7802 Instrument Interfaces and Model 7813.

e. INTERFACE NUMBER 2 (J102). This connector is a 50-pin card-edge type which mates with Series 7801 and 7802 Instrument Interfaces and Model 7813.

f. INTERFACE NUMBER 3 (J101). This connector is a 50-pin card-edge type which mates with Series 7801 and 7802 Instrument Interfaces and Model 7813.

TABLE 2-4.

How to Install the Dual Control-Unit Coupler

1. Disconnect power cord.
2. Remove cover plate over 2nd CONTROL UNIT opening.
3. Remove the Control Unit top cover.
4. Install 37-pin receptacle using original screws used with cover plate.
5. Install Berg housing (8-pin) as shown in Figure 4.
6. Replace top cover.

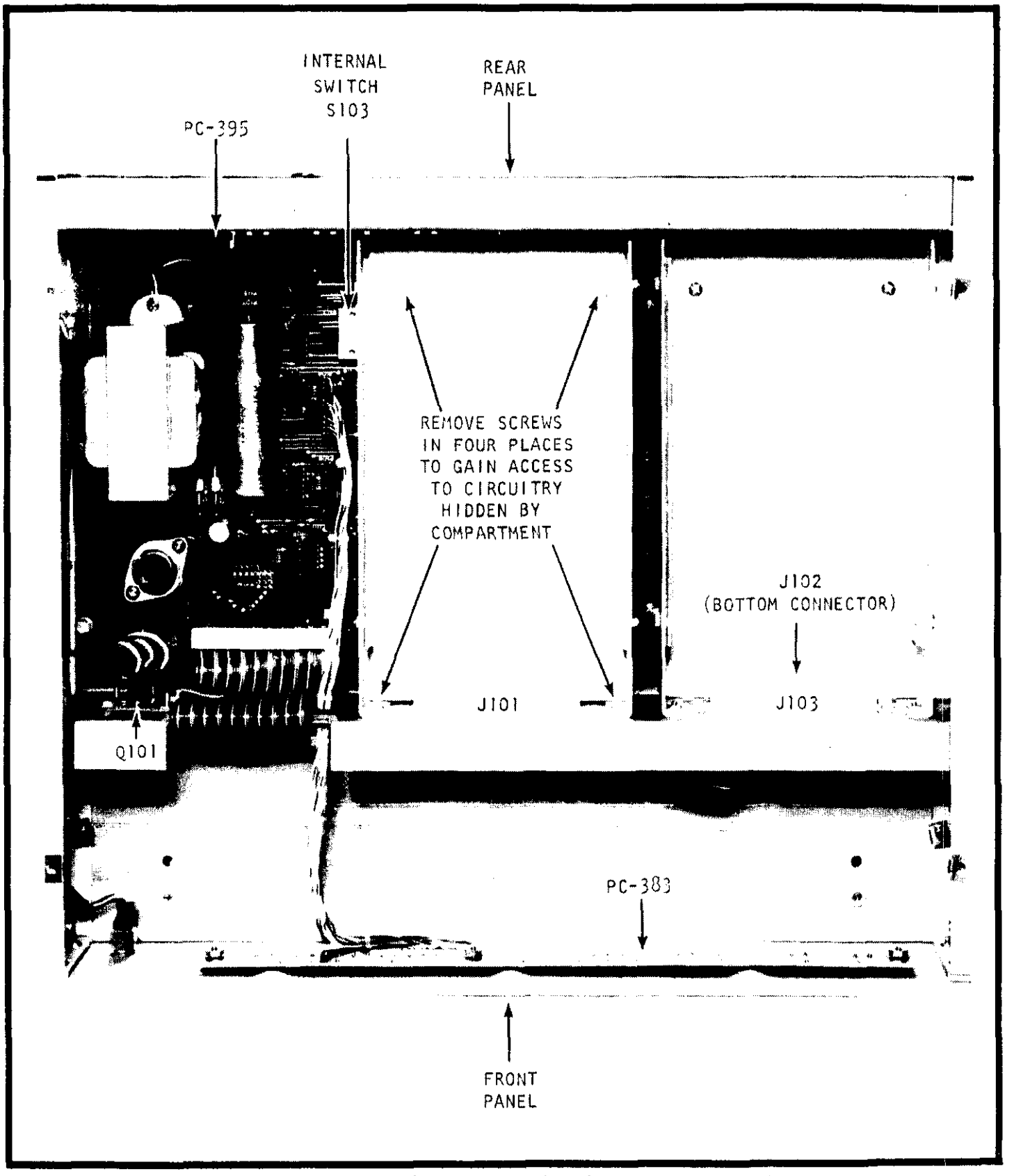


FIGURE 5. Top View of Control Unit With Cover Removed.

SECTION 3. INTERFACE CONSIDERATIONS

3-1. GENERAL. This section provides basic operating information concerning the interface bus and Scanner interface.

3-2. INTERFACE BUS CONFIGURATION. The Control Unit has three 50-pin card-edge connectors J101, J102, and J103 corresponding to Interface Numbers 3, 2, and 1. Except for Slot Address lines, all signals are wired in parallel on the three connectors. See Figure 6.

TABLE 3-1.

Summary of Signals on Interface Bus

Name	Remarks
Slot Address (SA)	All three Slot address lines are wired to connectors J101, J102, and J103. Refer to Figure 6 for wiring.
9VAC	This voltage is an auxiliary ac voltage used for certain Instrument Interfaces.
$\overline{\text{PWR UP RESET}}$	This signal is generated when power is applied to the Control Unit.
C0, C1, C2	These signals are Control commands.
CP (Control Pulse)	This signal is generated after a Control Byte has been received.
DP (Data Pulse)	This signal is generated after a Data Byte has been transferred.
RESET	This signal is generated for either of the following conditions: RESET code is received from the PCU PWR UP RESET is generated
VCC	This is a +5V logic supply for Interface logic.
GND	This is a logic supply "LO".
DIH8, DIH4, DIH2, DIH1 DIL8, DIL4, DIL2, DIL1	These lines are the eight input data lines. Data which is to be sent to the PCU is applied to these lines.
BC7, BC6, BC5, BC4, BC3, BC2, BC1, BC0	These lines are outputs of the Byte Counter circuit.
$\overline{\text{CP}}$ ($\overline{\text{Control Pulse}}$)	See CP above.
$\overline{\text{DP}}$ ($\overline{\text{Data Pulse}}$)	See DP above.
$\overline{\text{RESET}}$	See RESET above.
$\overline{\text{DOH8}}$, $\overline{\text{DOH4}}$, $\overline{\text{DOH2}}$, $\overline{\text{DOH1}}$ $\overline{\text{DOL8}}$, $\overline{\text{DOL4}}$, $\overline{\text{DOL2}}$, $\overline{\text{DOL1}}$	These lines are the eight data output lines. These lines represent data at the Output Register, except that the data has been inverted.

INTERFACE NUMBER	CORRESPONDING CONNECTOR	SIGNAL ON PINS* 1	2	3
1	J103	SA-1	SA-2	SA-3
2	J102	SA-2	SA-3	SA-1
3	J101	SA-3	SA-2	SA-1

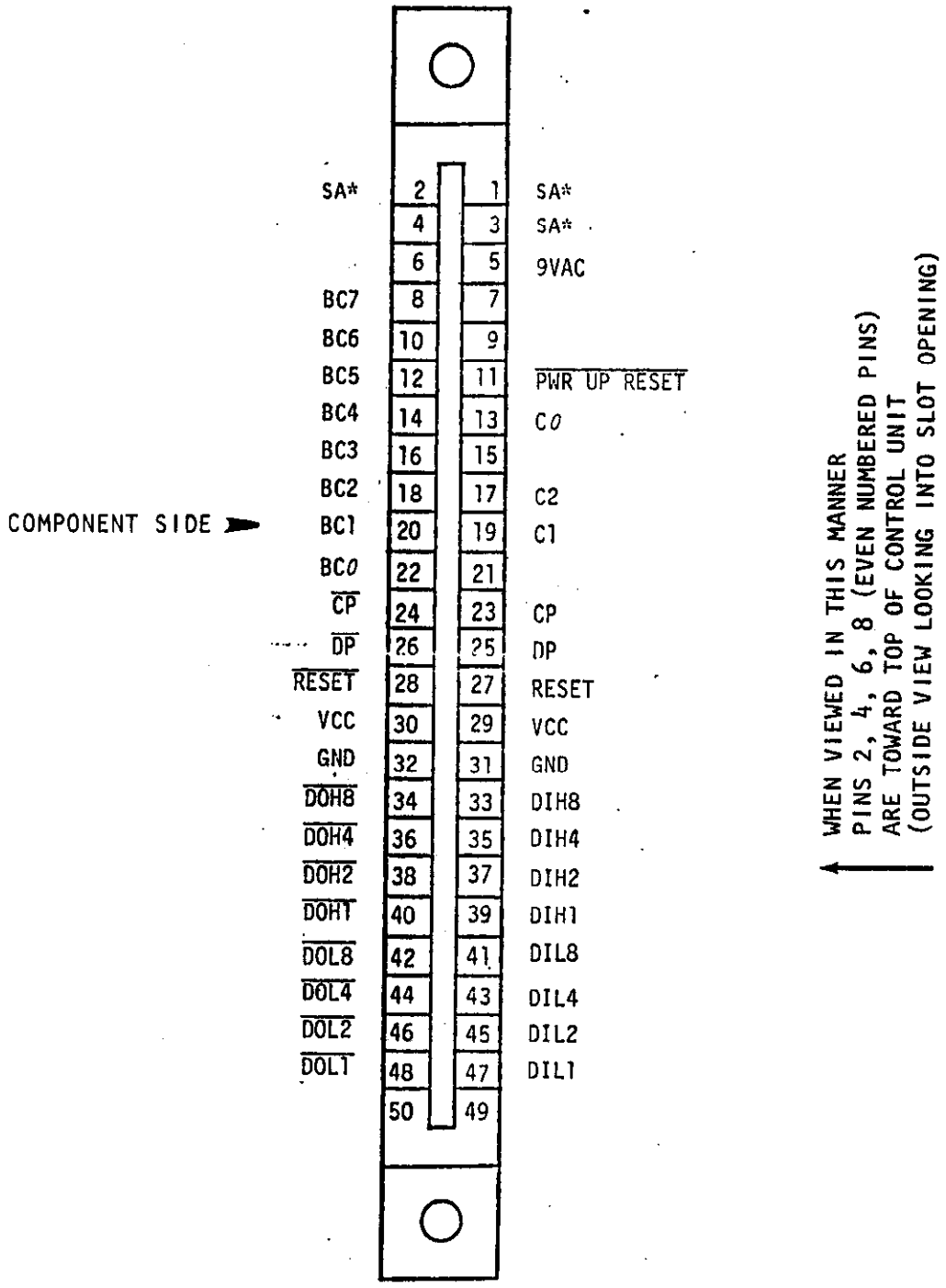


FIGURE 6. Card-edge Connector (J101, J102, or J103).

3-3. SCANNER INTERFACE. The Scanner interface provides capability to control up to 8 Keithley Model 702/702X Scanners. The "SCANNER" connector is a 26-pin connector that mates with a Series 7021 System Interconnect Cable. When used with a single Scanner, only one System Interconnect Cable is needed. If two or more Scanners are to be connected to a single Control Unit, a Multi-Scanner Coupler must be connected to the Control Unit. See Section 6, ACCESSORIES for detailed information on the use of the Multi-Scanner Coupler (Model 7819-MSC).

TABLE 3-2.

Connector (P110) Pin Identification on the Control Unit

Pin No.	Name	Remarks
1	CHAD 1	CHannel ADdress Input
2	CHAD 4	CHannel ADdress Input
3	Not Used	No Connection
4	Polarizing Pin	No Connection
5	LOCHAD 6	LOad CHannel ADdress-Scanner #6
6	LOCHAD 7	LOad CHannel ADdress-Scanner #7
7	LOCHAD 8	LOad CHannel ADdress-Scanner #8
8	RELAY READY	
9	REMOTE ALL OFF	
10	Not Used	No Connection
11	Not Used	No Connection
12	LOCHAD 2	LOad CHannel ADdress-Scanner #2
13	LOCHAD 4	LOad CHannel ADdress-Scanner #4
14	CHAD 2	CHannel ADdress Input
15	CHAD 8	CHannel ADdress Input
16	LOCHAD 1	LOad CHannel ADdress-Scanner #1
17	Not Used	No Connection
18	COMMON	Digital Common
19	COMMON	Digital Common
20	COMMON	Digital Common
21	COMMON	Digital Common
22	COMMON	Digital Common
23	Not Used	No Connection
24	Not Used	No Connection
25	LOCHAD 3	LOad CHannel ADdress-Scanner #3
26	LOCHAD 5	LOad CHannel ADdress-Scanner #5

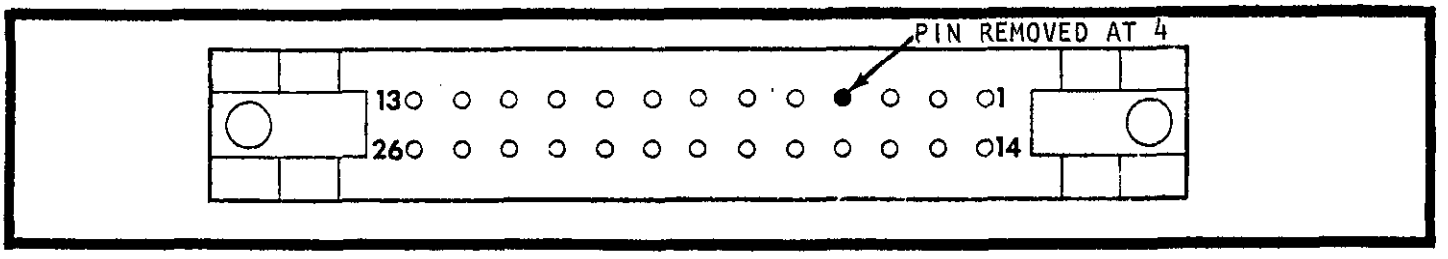


FIGURE 7. Scanner Connector (P110) on Rear Panel.

TABLE 3-3.

Typical Logic Definitions Based on Manufacturers' Data

Input Lines		Output Lines	
LOGIC "1" (Minimum)	LOGIC "0" (Maximum)	LOGIC "1" (Minimum)	LOGIC "0" (Maximum)
+2.0V	+0.8V	+2.4V	+0.4V

NOTE

Absolute maximum input voltage = +5.25V

Absolute minimum input voltage = -0.5V

TABLE 3-4.

Standard Terminology Used For Logic Lines

Symbol Name	Definition	Comments
ABC	High True	True = Logic "1"
$\overline{ABC}$	Low True	True = Logic "0"

SECTION 4. THEORY OF OPERATION

4-1. GENERAL. The Control Unit contains circuitry which links the Programmable Calculating Unit (PCU) and all other System 1 instrumentation. This circuitry handles data transfers between the PCU and accessory interfaces or the built-in scanner interface.

4-2. CIRCUIT DESCRIPTION.

a. The circuitry can be divided into ten functional circuits.

1. Control/Data Byte Detector Circuit.
2. Output Control/Data Register Circuit.
3. Input Data Register Circuit.
4. Indicator Circuit.
5. Control Byte Decoder Circuit.
6. Reset Circuit.
7. Control Byte One-Shot Multivibrator Circuit.
8. Data Byte One-Shot Multivibrator Circuit.
9. Byte Counter Circuit.
10. Scanner Interface Circuit.

b. Control/Data Byte Detector Circuit.

1. General Circuit Description. This circuit indicates whether a Control Operation (OPCB) or Data Operation (OPDB, IPDB) is being executed. Input signals are $\overline{\text{OTCT}}$ and $\overline{\text{DTEN}}$.

2. Detailed Circuit Description. When neither Control or Data operations are executed, $\overline{\text{OTCT}}$ and $\overline{\text{DTEN}}$ are a logic "0" during T8 to T15 of a machine cycle. When an OPCB instruction is executed, $\overline{\text{OTCT}}$ is at logic "1" during the entire machine cycle. When either an OPDB or IPDB instruction is executed, $\overline{\text{DTEN}}$ will remain a logic "1" for the entire machine cycle (i.e. $\overline{\text{DTEN}}$ will not have a transition from logic "1" to logic "0").

c. Output Control/Data Register Circuit.

1. General Circuit Description. This circuit is a serial in/parallel out Shift Register. Output control/data from the PCU is loaded into this register (U110) and clocked by $\phi 2$. BYOT is the serial input. BYOT is the inversion of signal $\overline{\text{BYOT}}$.

2. Detailed Circuit Description. When an output instruction (OPCB or OPDB) is executed, the contents of the Index Register is shifted into the Output Register. Output lines DOL1 through DOH8 are buffered and applied to the bus. If an OPCB instruction is executed the Control Byte Decoder is activated.

d. Input Data Register Circuit.

1. General Circuit Description. This circuit is a parallel in/serial out Shift Register. Input data from the Control Unit is transferred to the PCU via this register. A byte (8 bits) of data is serially transmitted to the PCU via BYIN, and clocked by $\phi 2$.

2. Detailed Circuit Description. Data input lines on the bus (DIL1 through DIH8) are shifted into the PCU Index Register and replace previous contents.

e. Indicator Circuit.

1. General Circuit Description. A total of 18 LED indicators are used on the Control Unit front panel to display data or status of control operations. The indicators are grouped as follows:

a) INPUT indicators (L1 through H8). These indicators represent data to be transferred from the Control Unit to the PCU.

b) OUTPUT indicators (L1 through H8). These indicators represent data which has been transferred from the PCU.

c) INSTRUCTION indicators. These indicators show whether the last I/O instruction executed was a control operation (OPCB) or a data operation (OPDB or IPDB).

2. Detailed Circuit Description. All indicators are driven by two-input NAND gates.

a) INPUT indicators (L1 through H8). Input data to be shifted into the PCU Index Register is displayed on indicators L1 through H8.

b) OUTPUT indicators. The data on the Output Control/Data Register is displayed on indicators L1 through H8.

c) INSTRUCTION indicators. The NAND gates are connected to form an RS Flip-Flop. The R and S inputs to the Flip-Flop are the two outputs of the Control/Data Byte Detector.

f. Control Byte Decoder Circuit.

1. General Circuit Description. This circuit accepts control information and decodes it into individual control signals. These signals are then used for controlling or transferring data to accessory instruments (when appropriate accessory Instrument Interface is installed).

2. Detailed Circuit Description.

a) PCU peripherals and the Control Unit are addressed using IH of an OPCB. Since IH is four bits wide, there are sixteen possible addresses, 0 through 15. System 1 uses two of sixteen possible addresses. Addresses 8 (binary 1000) and 9 (binary 1001) are used to address CU1 and CU2 respectively. The address to which a Control Unit will respond is determined by the setting of S103, located on the Control Unit printed circuit board.

b) As mentioned above, the contents of the Output Control/Data Register is a copy of the Index Register after an output instruction has been executed. Of these outputs, DOH1 through DOH8 represent the contents of IH. Execution of an OPCB instruction enables these bits to be applied to an address decoder. This decoder determines whether IH contains an eight or a nine depending on the position of the S103. The decoder's output will go high if IH contains a "one of us" code.

c) The low-order four bits of a Control Byte represent an operation code. If the address contained in IH is "one of us", that is an eight or nine, the DOL1 through DOL8 data are latched into U120. The contents of IL are then decoded into Slot Addresses and Control signals. It is these signals which control the action of the instrument interface cards.

d) In addition to enabling the IL latch, the address decoder also sets an RS flip-flop when IH contains a "one of us" code. The output of this flip-flop is used to enable BYIN so that data can be transferred to the PCU. When the address part of a Control Byte is not "one of us", the flip-flop is reset. This prevents our interface from interferring with other peripherals which might be connected to the PCU.

g. Reset Circuit.

1. General Circuit Description. A RESET signal is generated under the following conditions:

a) Control Unit Power Up. When power is first applied to the Control Unit via the Power Switch, or disconnecting and reconnecting line power to the Control Unit with Power Switch set to ON.

b) PCU Reset. When a RESET command is generated at the PCU.

2. Detailed Circuit Description.

a) Control Unit Power Up. The RESET signal is applied to the bus and causes the following actions:

1) Clears Output Data Register.

2) Sets all accessory Instrument Interface circuitry to "Power-Up" condition. (See individual Instrument Interface Instruction Manual for detailed information.)

3) Clears control signals C0, C1, and C2.

4) Disables BYIN (resets Flip-Flop).

5) Initiates a $\overline{\text{PWR UP RESET}}$.

b) PCU Reset. When a RESET command (OPCB and IL = 13_{10}) occurs, the following actions result:

1) Output Data Register = 13_{10}.

2) Sets all accessory Instrument Interface circuitry to "Power-Up" condition. (See individual *INSTRUCTION MANUAL* for detailed information.)

3) Clears control signals C0, C1, and C2.

4) Disables BYIN (resets Flip-Flop).

h. Control Byte One-Shot Multivibrator Circuits.

1. General Circuit Description. These circuits are used to synchronize transfer of control information within the Control Unit.

2. Detailed Circuit Description.

a) U131. This One-Shot is fired at a logic "1" to logic "0" transition of the Control Byte Detector signal. This occurs at T15 of an OPCB instruction. The One-Shot output enables the Address Decoder and Reset Command Detector.

b) U132. This One-Shot is fired at a logic "1" to logic "0" transition of the above one-shot and causes a Control Pulse (CP) on the bus.

i. Data Byte One-Shot Multivibrator Circuit.

1. General Circuit Description. The output of this circuit is called Data Pulse (DP). This signal is similar to CP.

2. Detailed Circuit Description (U119). This One-Shot is fired at a logic "1" to logic "0" transition of the Data Byte Detector signal, i.e. when either IPDB or OPDB operations are executed.

j. Byte Counter Circuit.

1. General Circuit Description. This circuit generates eight control signals, BC0 through BC7, and are used as Strobe and Latch Enable functions.

2. Detailed Circuit Description. This circuit consists of a Decade Counter (U128) and a "One-out-of-Ten" Decoder (U129). When a Control Byte is detected, the Counter is reset to zero. The counter is incremented by DP. The Counter is wired so that when the counter is incremented beyond 7, the output is set to 9. The Byte Counter outputs are available on the bus, and permits data byte transfer without the need for a Control Byte Command (i.e. after an IPDB or OPDB instruction is executed, the Byte Counter is incremented, enabling the next data byte).

k. Scanner Interface Circuit.

1. General Circuit Description. This circuit contains logic to control one Scanner (or up to 8 Scanners, when the Multi-Scanner Coupler is used). The logic is divided into three functional circuits.

a) REMOTE ALL OFF Logic. When a REMOTE ALL OFF command is initiated by the PCU, the Scanner interface logic generates a logic "0" on pin 9 of SCANNER connector.

b) LOCHAD Logic. The LOCHAD logic latches a LOCHAD code coming from the PCU. A logic "0" is generated on the appropriate LOCHAD line.

c) CHAD Buffer Logic. These buffer stages provide fan-out drive capability.

2. Detailed Circuit Description.

a) REMOTE ALL OFF Logic. Three logic gates (U121C, U118A, U123D) are used to generate a REMOTE ALL OFF command. The specific logic requirements for activating REMOTE ALL OF are given in Table 4-1.

TABLE 4-1.

Logic for REMOTE ALL OFF

INPUT						OUTPUT
SCAN ADDR	C1	U121-8	$\overline{CP}$	U118-1	RESET	REMOTE ALL OFF (Pin 9)
1	1	0	0	1	0	0 (REMOTE ALL OFF activated)
1	1	0	1	0	0	1 (REMOTE ALL OFF not activated)
X	X	X	X	X	1	0 (REMOTE ALL OFF activated)

X = Don't care

b) LOCHAD Logic. Five Logic gates are used with the Latch and Decoder. These gates control the operation of the latch and enable the LOCHAD buffers. Eight OR gates are used for buffering the LOCHAD outputs. When enabled, these gates apply the output of the decoder to the Scanners connected to the Control Unit.

c) CHAD Buffer Logic. The CHAD Buffer circuits (U113A, D, E, F) provide fan-out capability.

TABLE 4-2.

LOCHAD Lines Used on Scanner Connector

Scanner Number	Pin Number
1	16
2	12
3	25
4	13
5	26
6	5
7	6
8	7

TABLE 4-3.

Logic for LOCHAD Lines

INPUT										OUTPUT
SCAN ADDR C0		U121-11	$\overline{DP}$	U104-4	BC0	BC1	U121-6	U108-10	$\overline{RESET}$	
1	1	0	0	1	1	0	0	1	1	Latch enable is logic "1"
1	1	0	1	0	1	0	1	0	1	Latch enable is logic "0"
X	X	X	X	X	X	X	X	X	0	Latch enable is logic "1"
1	1	0	0	1	0	1	1	0	1	Lochad enable is logic "1"
1	1	0	1	0	0	1	1	0	1	Lochad enable is logic "0"

X = Don't care

TABLE 4-4.

Illustration of Logic for CHAD Lines (Four of Ten Useable Combinations Shown)

INPUT				OUTPUT			
$\overline{DOL8}$	$\overline{DOL4}$	$\overline{DOL2}$	$\overline{DOL1}$	CHAD 8	CHAD 4	CHAD 2	CHAD 1
1	1	1	0	0	0	0	1
1	1	0	1	0	0	1	0
1	0	1	1	0	1	0	0
0	1	1	1	1	0	0	0

TABLE 4-5.

RELAY READY Logic

INPUT			OUTPUT
SCAN ADDR	C0	U121-11	U101-12
1	1	0	1 (RELAY READY enabled)
0	1	1	0
1	0	1	0
0	0	1	0

4-3. HOW TO INTERPRET THE FRONT PANEL INDICATORS. The Control Unit has 18 indicators as shown in Figure 8.

INPUT. These indicators represent data to be sent to the PCU from Interface Number 1, 2, or 3 or Scanner interface.

OUTPUT. These indicators represent data which has been received from the PCU.

The data represented by the indicators is sometimes in the form of two 8-4-2-1 BCD digits. Data from the PCU is represented in program memory as a three digit octal number from 000 to 377.

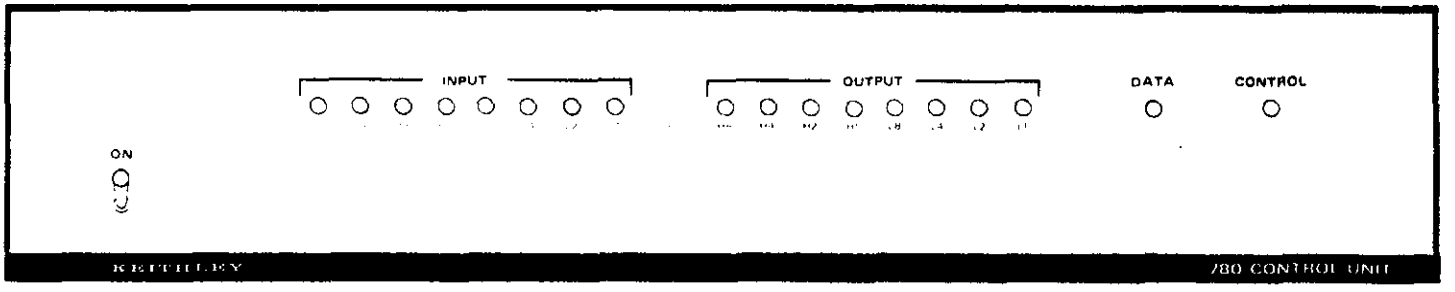


FIGURE 8. Front Panel Indicators.

SECTION 5. MAINTENANCE

5-1. GENERAL. This section contains procedures for Performance Verification.

5-2. REQUIRED TEST EQUIPMENT. Recommended test equipment is given in Table 5-1. Test equipment other than recommended may be substituted if specifications equal or exceed the stated characteristics.

5-3. PERFORMANCE VERIFICATION. Use the following procedures to verify basic operation of the instrument (apart from any other component of the Keithley System 1 except the PCU). If the instrument is out of specification at any point, perform the troubleshooting check as in Section 5-4. In addition to test equipment a series 7810 I/O Handler Software program will be needed.

TABLE 5-1.

Recommended Test Equipment Accessories Needed For Performance Verification

Item	Name	Specification	Mfr.	Model
A	Oscilloscope	DC coupled, 4 channels, 2V & 5V/div. Sweep rate 50ms/div to 5µs/div External Triggering Capability	Tektronix	560
B	Programmable Calculating Unit	-11 Memory installed (minimum size)	KI	PCU
C	I/O Handler Software (magnetic card)	Series 7810	KI	Series 7810

a. Initial Set-Up

1. Connect the PCU to line power, set Power ON, and set RUN/STEP/LOAD switch to RUN.

2. Set the Control Unit as described in Section 2-6 of this manual.

3. Plug the 37-pin connector from the Control Unit to the rear panel of the PCU.

4. Apply power to the Oscilloscope for measurements to follow. Specific settings will be given for each test.

NOTE

Wherever a test point on the circuit board is specified, the circuit designation of the circuit module (such as U103) is given followed by the pin number on that module or integrated circuit (example U103-12).

b. Test #1. This test procedure checks the Control/Data Byte Detector under the condition that the PCU is executing no I/O instructions. No program is needed for this test.

1. Ensure that the PCU is set to ON and that the IDLE light is on.
2. Set the oscilloscope as follows:
   a) Vertical Sensitivity - 5 volts/div.
   b) Horizontal Sweep - 50 µs/div.
   c) Trigger Source - Channel 1, positive slope.
3. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 Input to U103-12 (OTCT).
   b) Connect Channel 2 Input to U103-11 (DTEN).
   c) Connect Channel 3 Input to U103-8 (Control Detector output).
   d) Connect Channel 4 Input to U103-9 (Data Detector output).
4. Verify that OTCT and DTEN are present as shown in Figure 9.
5. Verify that Control Detector output and Data Detector output are at signal LO as shown in Figure 9.

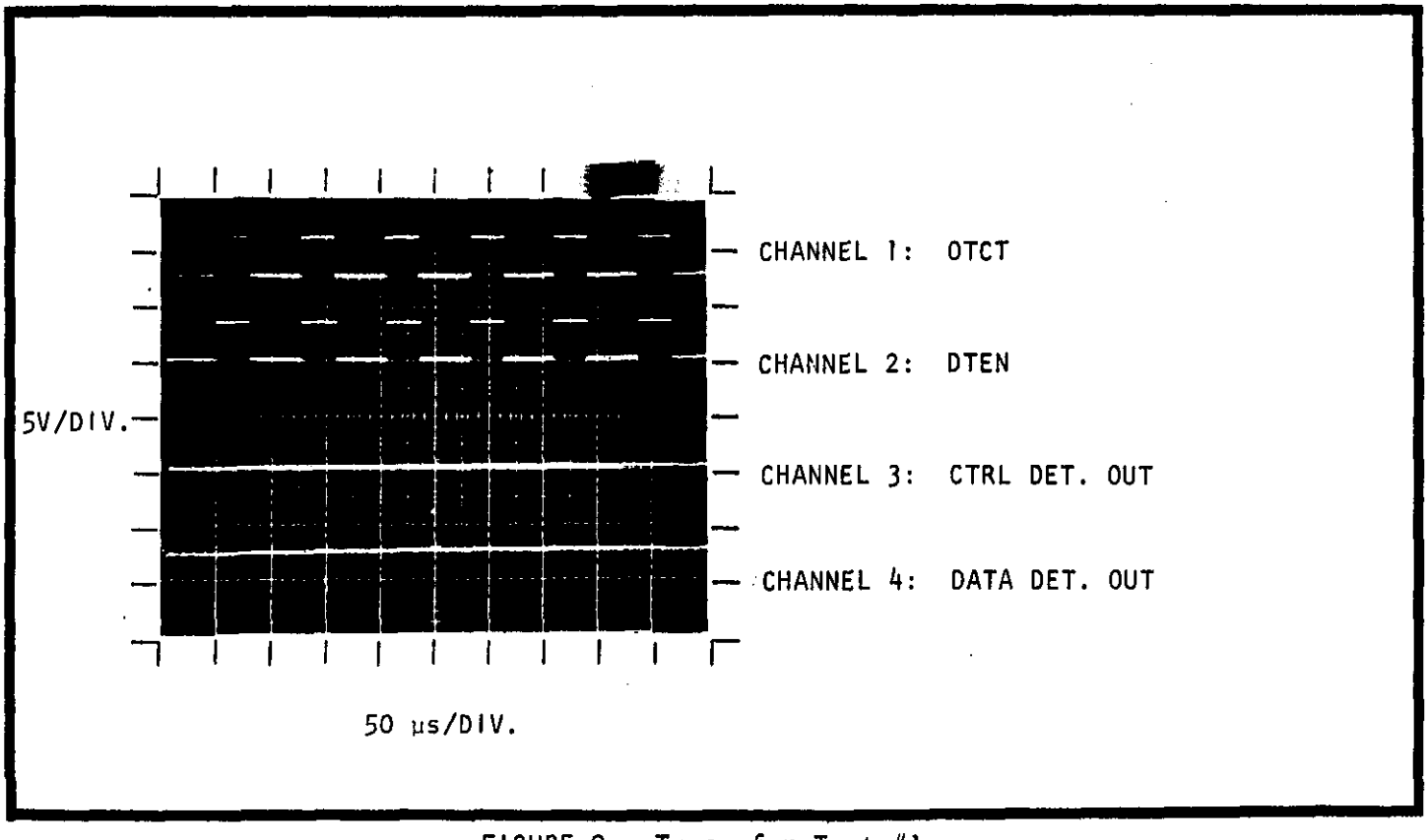


FIGURE 9. Trace for Test #1.

c. Test #2. This test procedure checks the Control/Data Byte Detector outputs under the OPCB condition. A program is needed to obtain the OPCB condition.

1. Enter the program listed in Table 5-2. (See page 5-9.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the Oscilloscope as follows:
   a) Vertical Sensitivity - 5 volts/div.
   b) Horizontal Sweep - 50 µs/div.
   c) Trigger Source - Channel 1, positive slope.
4. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 Input to U103-12 (OTCT).
   b) Connect Channel 2 Input to U103-11 (DTEN).
   c) Connect Channel 3 Input to U103-8 (Control Detector output).
   d) Connect Channel 4 Input to U103-9 (Data Detector output).
5. Run the program beginning at branch point 0 0.
6. Verify that OTCT is present except during each execution of an OPCB instruction (three consecutive OPCB instructions as in this example), as shown in Figure 10.
7. Verify that DTEN is present regardless of an OPCB instructions.
8. Verify that the Control Detector output goes to Logic "1" during each execution of an OPCB instruction.

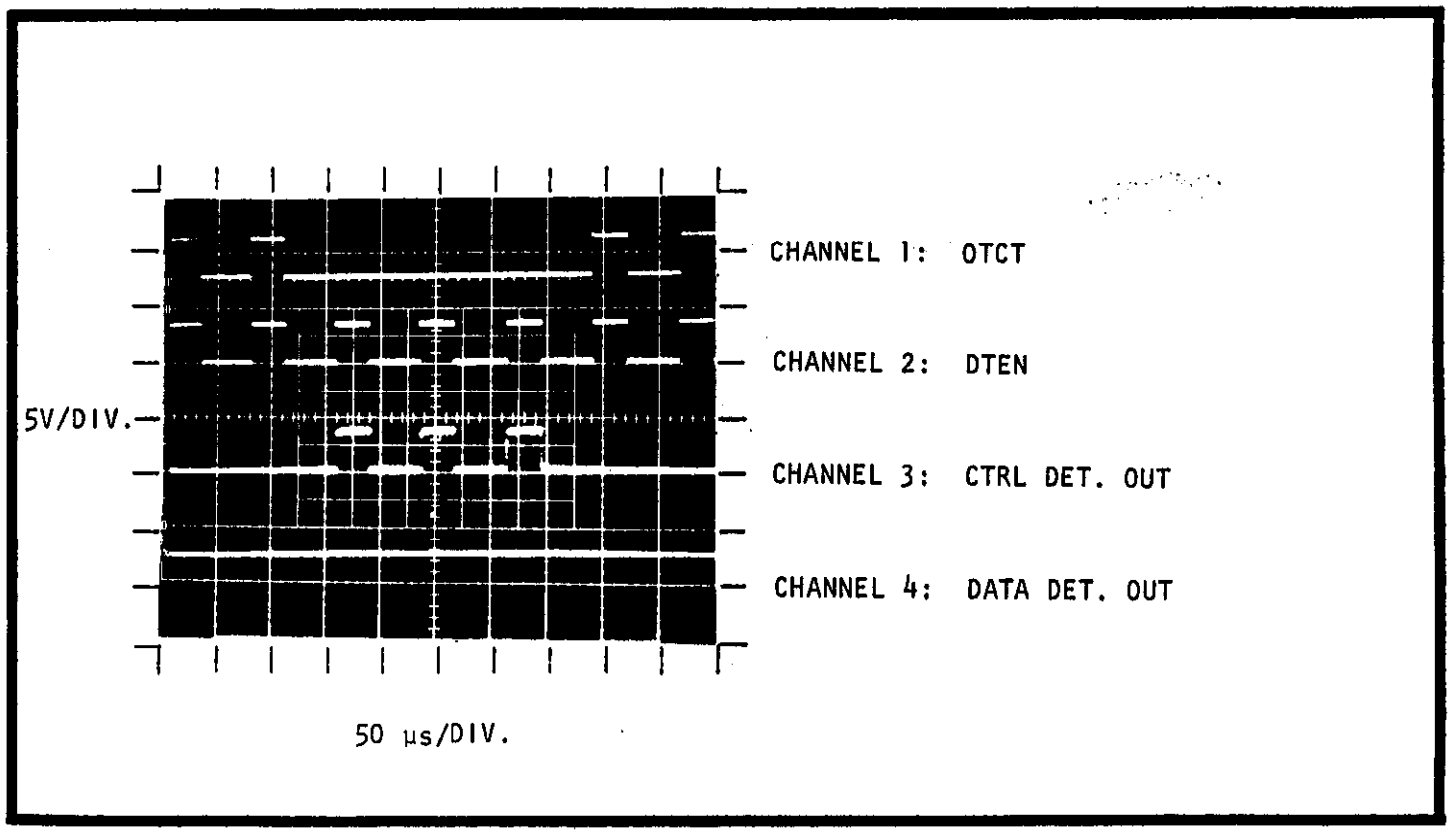


FIGURE 10. Trace For Test #2.

d. Test #3. This test procedure checks the Control/Data Byte Detector outputs under the OPDB condition. A program is needed to obtain the OPCB condition.

1. Enter the program listed in Table 5-3. (See page 5-9.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the Oscilloscope as follows:
   a) Vertical Sensitivity - 5 volts/div.
   b) Horizontal Sweep - 50μs/div.
   c) Trigger Source - Channel 2, positive slope.
4. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 Input to U103-12 (OTCT).
   b) Connect Channel 2 Input to U103-11 (DTEN).
   c) Connect Channel 3 Input to U103-8 (Control Detector output).
   d) Connect Channel 4 Input to U103-9 (Data Detector output).
5. Run the program beginning at branch point 0 0.
6. Verify that DTEN is present except during each execution of a OPDB instruction (three consecutive OPDB instructions as in this example), as shown in Figure 11.
7. Verify that OTCT is present regardless of a OPDB instruction.
8. Verify that the Data Detector output goes to Logic "1" during each execution of a OPDB instruction.

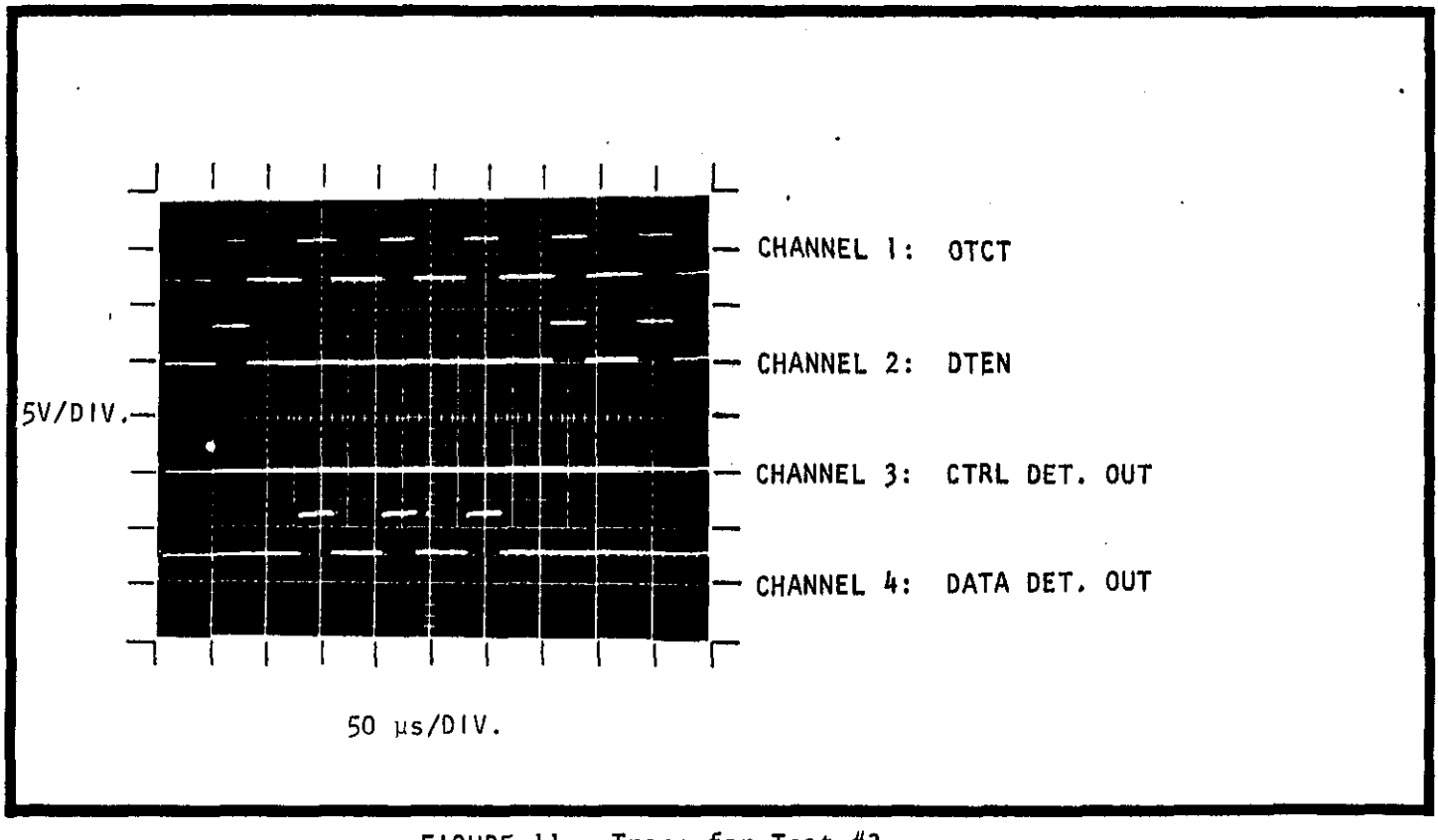


FIGURE 11. Trace for Test #3.

e. Test #4. This test procedure checks the Control/Data Byte Detector outputs under the IPDB condition. A program is needed to obtain the IPDB condition.

1. Enter the program listed in Table 5-4. (See page 5-9.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the oscilloscope as follows:
   a) Vertical Sensitivity - 5 volts/div.
   b) Horizontal Sweep - 50µs/div.
   c) Trigger Source - Channel 2, positive slope.
4. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 Input to U103-12 (OTCT).
   b) Connect Channel 2 Input to U103-11 (DTEN).
   c) Connect Channel 3 Input to U103-8 (Control Detector output)
   d) Connect Channel 4 Input to U103-9 (Data Detector output)
5. Run the program beginning at branch point 0 0.
6. Verify that DTEN is present except during each execution of a IPDB instruction (three consecutive IPDB instructions as in this example), as shown in Figure 12.
7. Verify that OTCT is present regardless of a IPDB instruction.
8. Verify that the Data Detector output goes to Logic "1" during each execution of a IPDB instruction.

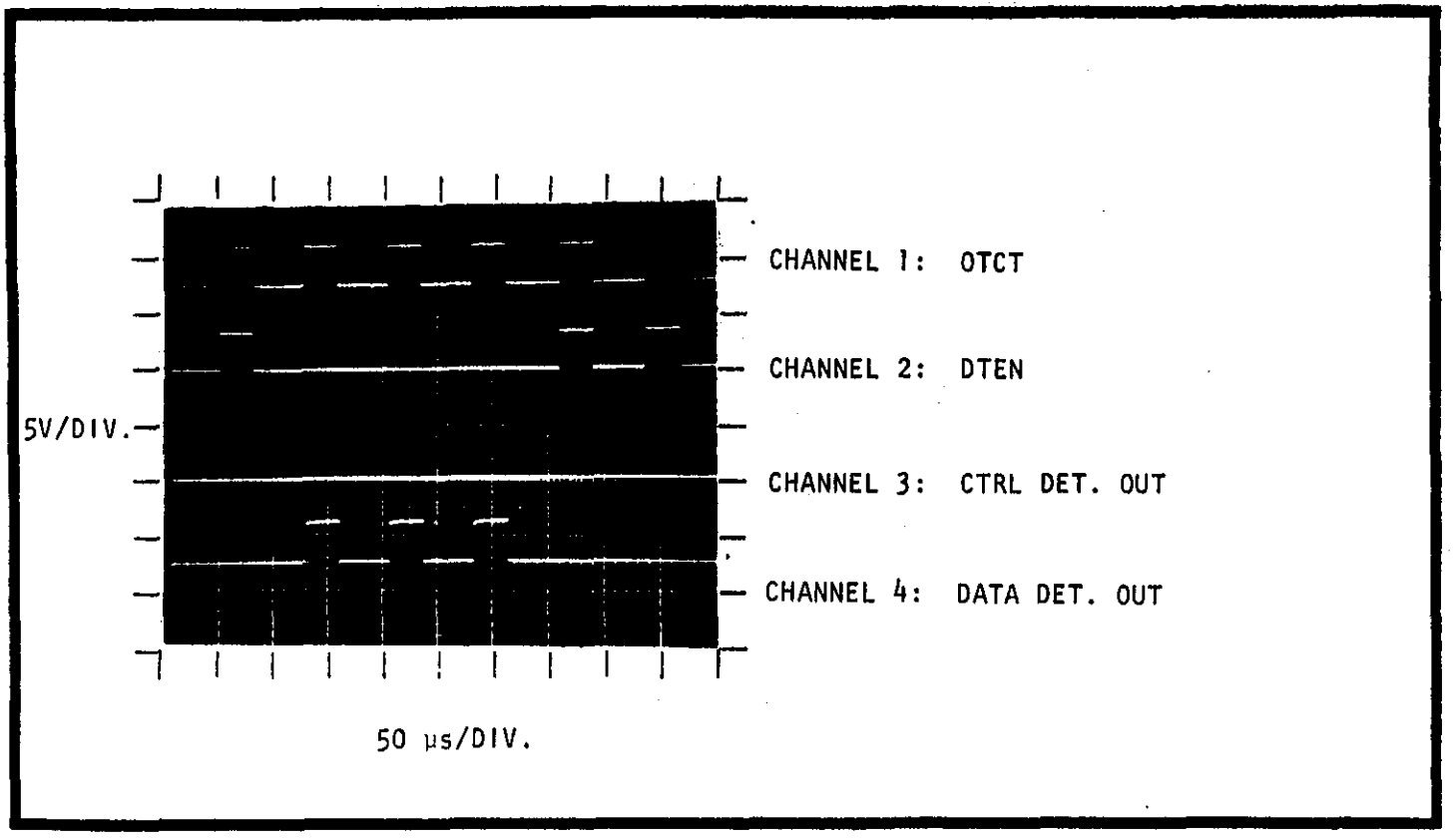


FIGURE 12. Trace for Test #4.

f. Test #5. This test procedure checks the $\phi 2$ Enable Line. The $\phi 2$ Enable line, PCU clock line, and PCU BYOT line are used to control the operation of the Output Control/ Data Register. A program must be loaded into the PCU to obtain an OPCB condition.

1. Enter the program as listed in Table 5-5. (See page 5-9.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the Oscilloscope as follows:
   a) Vertical Sensitivity - 5 volts/div.
   b) Horizontal Sweep - 5μs/div.
   c) Trigger Source - Channel 1, positive slope.
4. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 Input to U107-10 ($\phi 2$ Enable).
   b) Connect Channel 2 Input to U107-9 ($\phi 2$).
   c) Connect Channel 3 Input to U110-1 (BYOT, Data Out)
5. Run the program beginning at branch point 0 0.
6. Verify the traces shown in Figure 13.

NOTES.

Data is clocked into the Output Control/Data Register on the falling edge of $\phi 2$. Data is clocked with L1 being sent first. L1 to H8 is 10010101 binary.

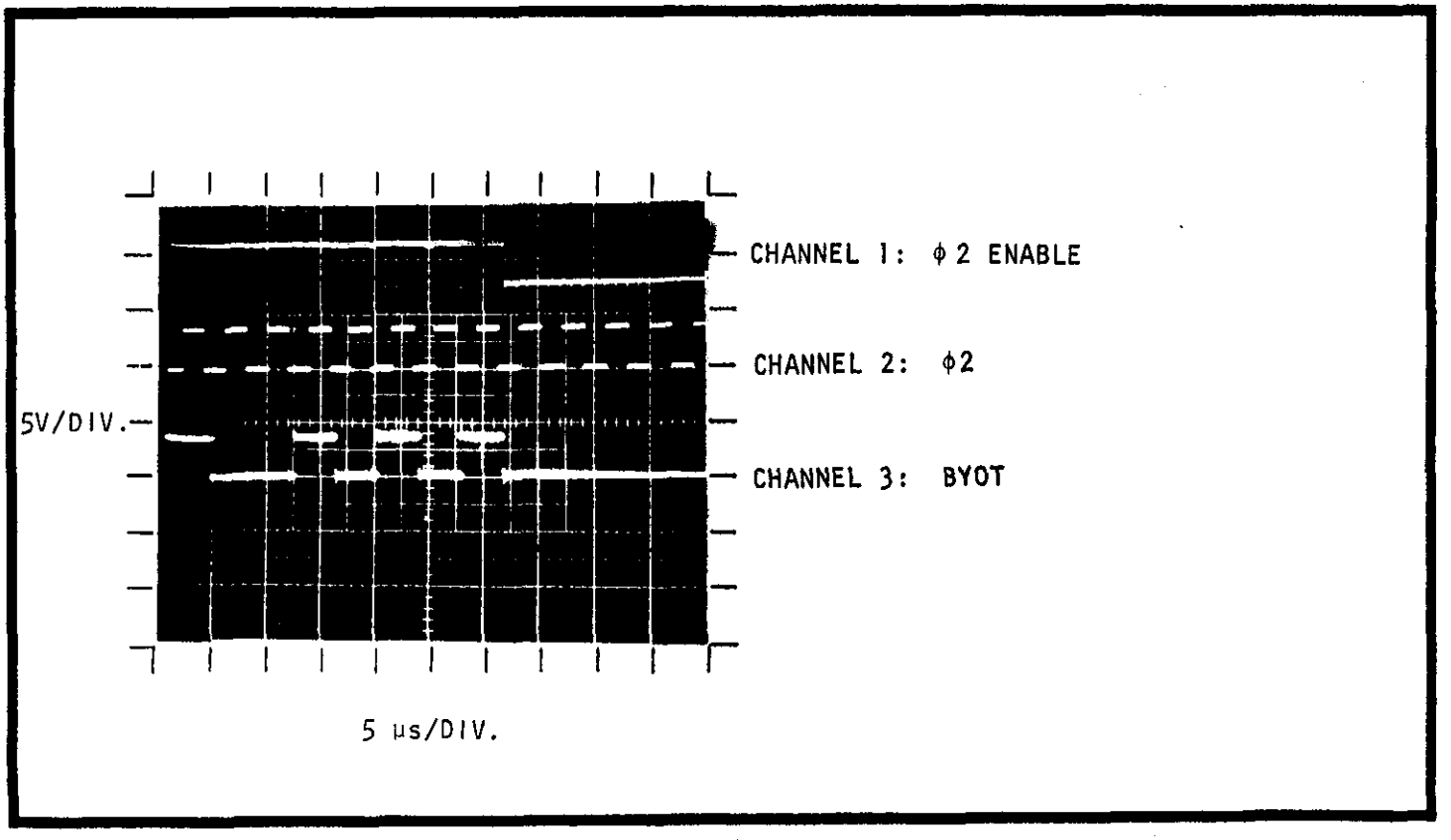


FIGURE 13. Trace for Test #5.

g. Test #6. This test procedure checks the relationship between: Control Byte Detector Output and the two one shots associated with Control Bytes under the OPCB condition. A program must be loaded into the PCU to obtain the OPCB condition.

1. Enter the program listed in Table 5-6. (See page 5-9.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the Oscilloscope as follows:
   a) Vertical Sensitivity - 5 volts/div.
   b) Horizontal Sweep - 10μs/div.
   c) Trigger Source - Channel 1, positive slope.
4. Make connections to the Control Unit circuitry as follows:
   a) Connect channel 1 Input to U103-8 (Control Byte Detector output).
   b) Connect Channel 2 Input to U131-6 (Q output of 1st one-shot).
   c) Connect Channel 3 Input to U132-6 (Control Pulse CP)
5. Run the program beginning at branch point 0 0.
6. Verify the traces shown in Figure 14.
   a) Q output of first one-shot should coincide with Logic "1" to Logic "0" transition of the Control Byte Detector output. (Synchronizes signals for the Control Unit.)
   b) Q output of second one-shot should coincide with Logic "1" to Logic "0" transition of Q output of first one-shot. (Synchronizes control signals for Instrument Interfaces.)

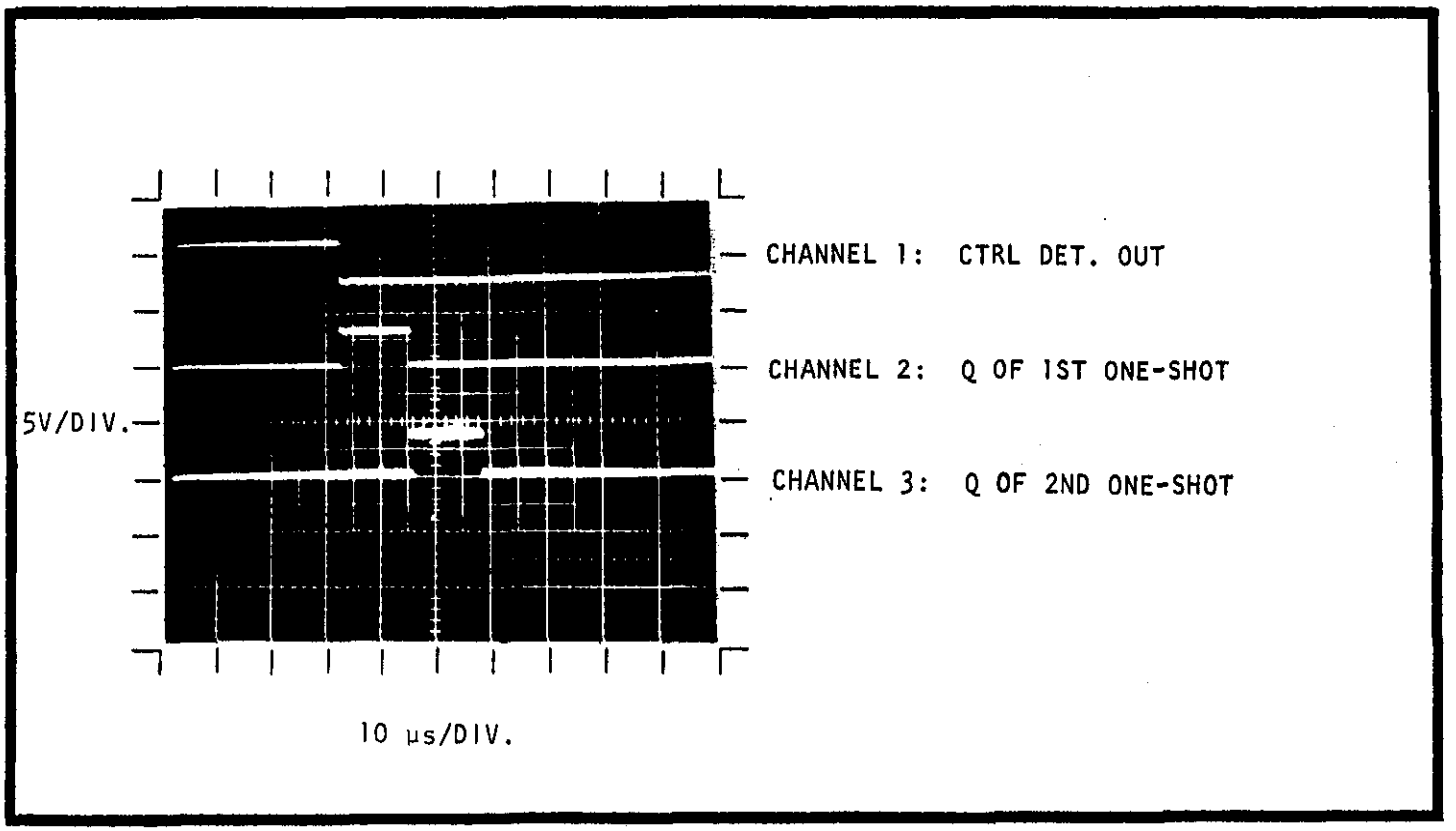


FIGURE 14. Trace For Test #6.

h. Test #7. This test procedure checks the relationship between: Data Byte Detector Output and the Data Pulse (DP) one-shot under the OPDB condition. A program must be loaded into the PCU to obtain the OPDB condition.

1. Enter the program listed in Table 5-7. (See page 5-9.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the Oscilloscope as follows:
   a) Vertical Sensitivity - 5 volts/div.
   b) Horizontal Sweep - 10μs/div.
   c) Trigger Source - Channel 1, positive slope.
4. Make connections to the Model 780 circuitry as follows:
   a) Connect Channel 1 Input to U103-9 (Data Byte Detector output).
   b) Connect Channel 2 Input to U128-14 (Data Pulse DP).
   c) Connect Channel 3 Input to U132-6 (Control Pulse CP).
5. Run the program beginning at branch point 0 0.
6. Verify the traces shown in Figure 15.
   a) Data Pulse should coincide with the Logic "1" to Logic "0" transition of the Byte Detector Output.
   b) Control Pulse does not appear (remains at Logic "0").

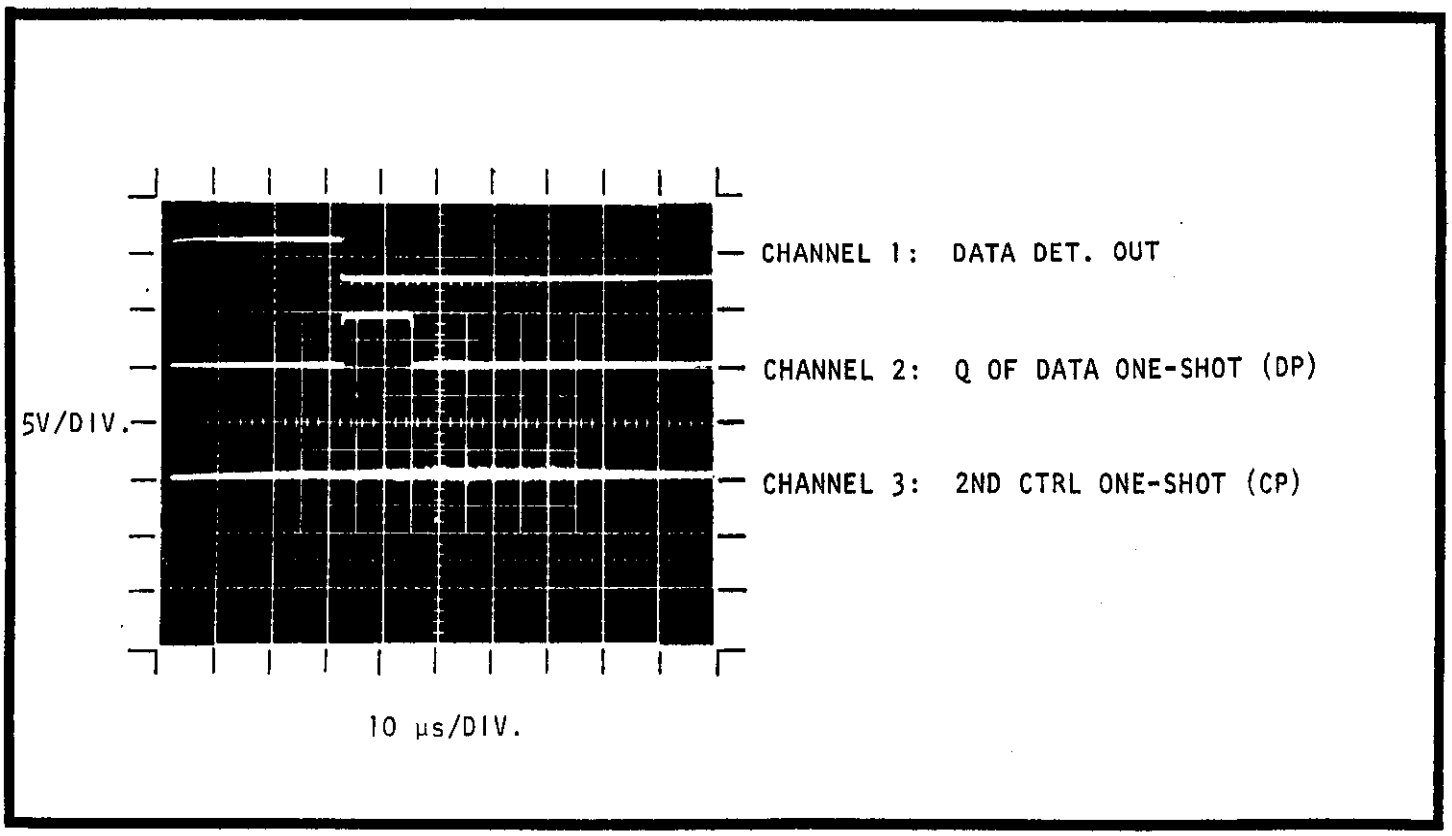


FIGURE 15. Trace For Test #7.

Table 5-2
Program Needed to Perform Test #2

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	3 1 4	OPCB
1	3 1 4	OPCB
2	3 1 4	OPCB
3	2 2 0	JU00, 000
4	0 0 0	

Table 5-3
Program Needed to Perform Test #3

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	3 1 5	OPDB
1	3 1 5	OPDB
2	3 1 5	OPDB
3	2 2 0	JU00, 000
4	0 0 0	

Table 5-4
Program Needed to Perform Test #4

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	3 0 5	IPDB
1	3 0 5	IPDB
2	3 0 5	IPDB
3	2 2 0	JU00, 000
4	0 0 0	

TABLE 5-5.
Program Needed To Perform Test #5

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 251
1	2 5 1	
2	3 1 4	OPCB
3	2 2 0	JU00, 000
4	0 0 0	

TABLE 5-6.
Program Needed To Perform Test #6

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 251
1	2 5 1	
2	3 1 4	OPCB
3	2 2 0	JU00, 000
4	0 0 0	

TABLE 5-7.
Program Needed to Perform Test #7

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 015
1	0 1 5	
2	3 1 5	OPDB
3	2 2 0	JU00, 002
4	0 0 2	

i. Test #8. This test procedure checks the Data Output Register and the Data Output lamp drivers. A series 7810 I/O Handler program (magnetic card) is needed to perform the test, as well as a specific keyboard entered program.

1. Enter a series 7810 I/O Handler program via the magnetic card reader at branch point 0 0.

2. Enter the program listed in Table 5-8. (See page 5-13.)

3. Place the PCU in Program Mode.

4. Run the program beginning at branch point 0 0.

5. Verify that the Data Output indicators (representing DOL1, DOL2, DOL4, DOL8, DOH1, DOH2, DOH4, DOH8) are lighted corresponding to a "walking one" moving towards the left. The Data Output lines $\overline{\text{DOL1}}$ through $\overline{\text{DOL8}}$ may also be observed. Since the data lines are inverted, a "walking zero" should be observed.

6. Enter the program listed in Table 5-9.

7. Place the PCU in Program Mode.

8. Run the program beginning at branch point 0 0.

9. Verify that the Data Output indicators (representing DOL1, DOL2, DOL4, DOL8, DOH1, DOH2, DOH4, DOH8) are lighted corresponding to a "walking zero" moving towards the left. The Data Output lines, $\overline{\text{DOL1}}$ through $\overline{\text{DOH8}}$ may also be observed. Since the data lines are inverted, a "walking one" should be observed.

j. Test #9. This test procedure checks the Byte Counter circuitry using a static test. A program must be loaded into the PCU to obtain OPCB and OPDB conditions.

1. Enter the program listed in Table 5-10. (See page 5-13.)

2. Place the PCU in Program mode.

3. Set the oscilloscope as follows:

   a) Vertical Sensitivity - 2 volts/div.

   b) Horizontal Sweep - 50 ms/div.

   c) Trigger Source - AUTO Trigger.

4. Make connections to the following Byte Count (BC) lines at Interface Number 1: BC0, BC1, BC2, BC3, BC4, BC5, BC6, BC7.

5. Run the program beginning at branch point 0 0.

6. Verify that the BC0 line is at Logic "1" when the PCU "IDLE" indicator is lighted.

7. Depress RESUME.

8. Verify that BC1 line is at Logic "1" when the PCU "IDLE" indicator is lighted.

9. Depress RESUME.

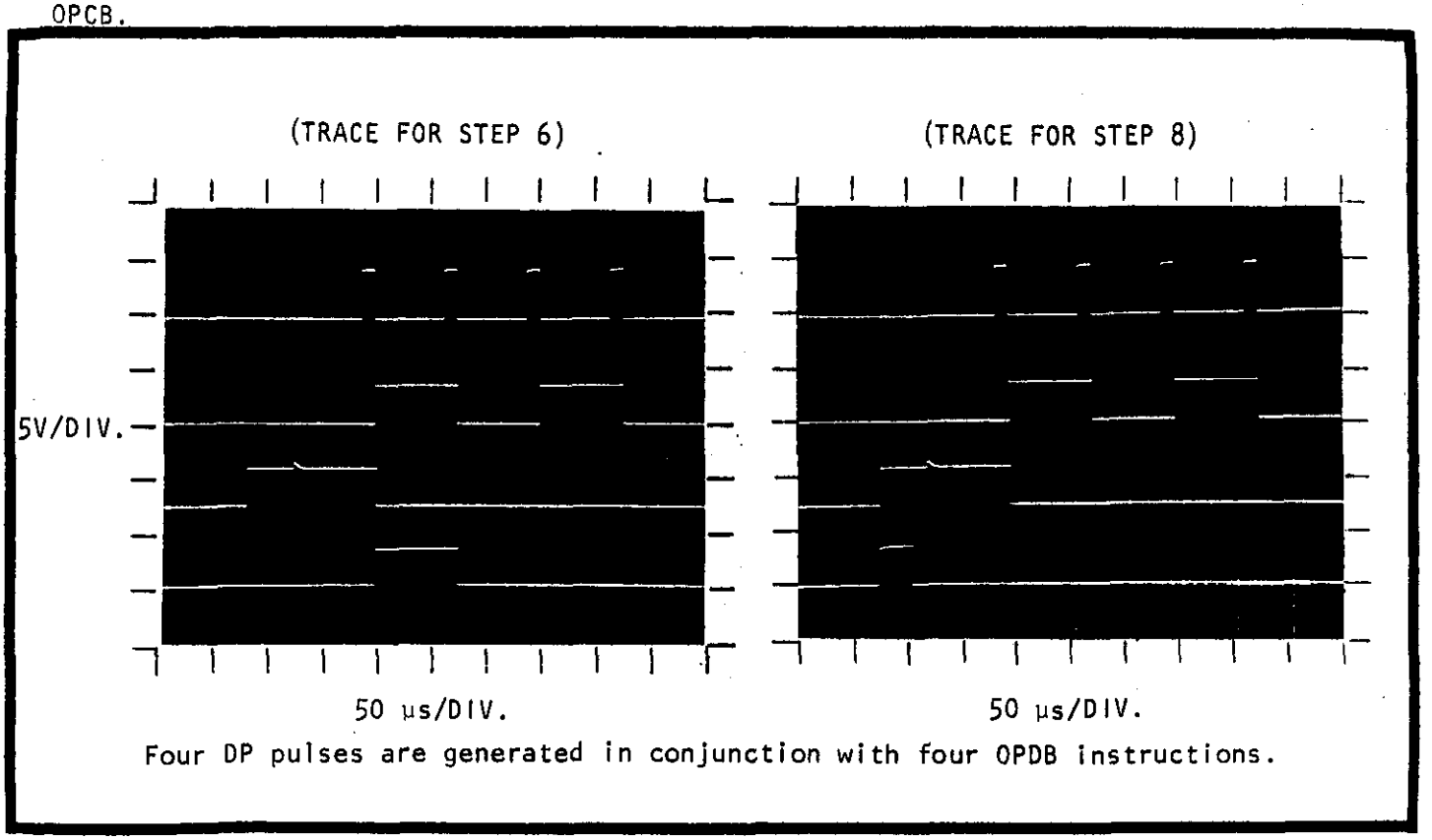
10. Verify that BC2 line is at Logic "1" when the PCU "IDLE" indicator is lighted.

NOTE

Continue the test in a similar fashion until BC7 has been tested. Each time RESUME is depressed the program will cause the next BC line to go to Logic "1". After BC7 has been tested, all succeeding RESUME key strokes will have no effect on the BC lines (that is, all BC lines will remain at Logic "0"). The program may be run again by jumping to branch point 0 0.

k. Test #10. This procedure checks the Byte Counter circuitry using a dynamic test. A program must be loaded into the PCU to obtain OPCB and OPDB conditions.

1. Enter the program listed in Table 5-11. (See page 5-13.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the oscilloscope as follows:
   a) Vertical Sensitivity - 5 volts/div.
   b) Horizontal Sweep - DELAYED 50µs/div.
   c) Trigger Source - Channel 1, positive slope.
4. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 7 input to U128-14 (Data Pulse DP).
   b) Connect Channel 2 input to U128-1 (QA on Data Byte Counter).
   c) Connect Channel 3 input to U105-2 (BC0).
   d) Connect Channel 4 input to U105-4 (BC1).
5. Run the program beginning at branch point 0 0.
6. Verify that QA is toggled by the Logic "1" to Logic "0" transition of the Data Pulse (DP), thus incrementing the Byte Counter from BC0 to BC1.
7. Change the oscilloscope connection on the Channel 4 Input from U105-4 to U103-8 (Control Byte Detector output).
8. Verify that BC0 is set to Logic "1" by the Logic "0" to Logic "1" transition of OPCB.



Four DP pulses are generated in conjunction with four OPDB instructions.

FIGURE 16. Trace For Test #10.

1. Test #11. This procedure checks the "one of us" decoder. This circuit is activated by a Control Byte with IH = 8 or 9 depending on the position of Switch S103. A program must be loaded in the PCU to obtain an OPCB condition.

1. Set the Control Unit internal switch S103 to CU1 position.
2. Enter the program listed in Table 5-12. (See page 5-13.)
3. Set the RUN/STEP/LOAD switch on the PCU to RUN.
4. Set the oscilloscope as follows:
   a) Vertical sensitivity - 5 volts/div.
   b) Horizontal Sweep - 20μs/div.
   c) Trigger Source - Channel 1 (negative slope).
5. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 to U131-1 ($\overline{Q}$ of first CTRL one-shot).
   b) Connect Channel 2 to U107-11 ($\overline{\text{one of us}}$).
   c) Connect Channel 3 to U118-13 (Latch Enable).
   d) Connect Channel 4 to U118-10 (BYIN Enable).
6. Run the program beginning at branch point 0 0.
7. Verify the traces shown in Figure 17.

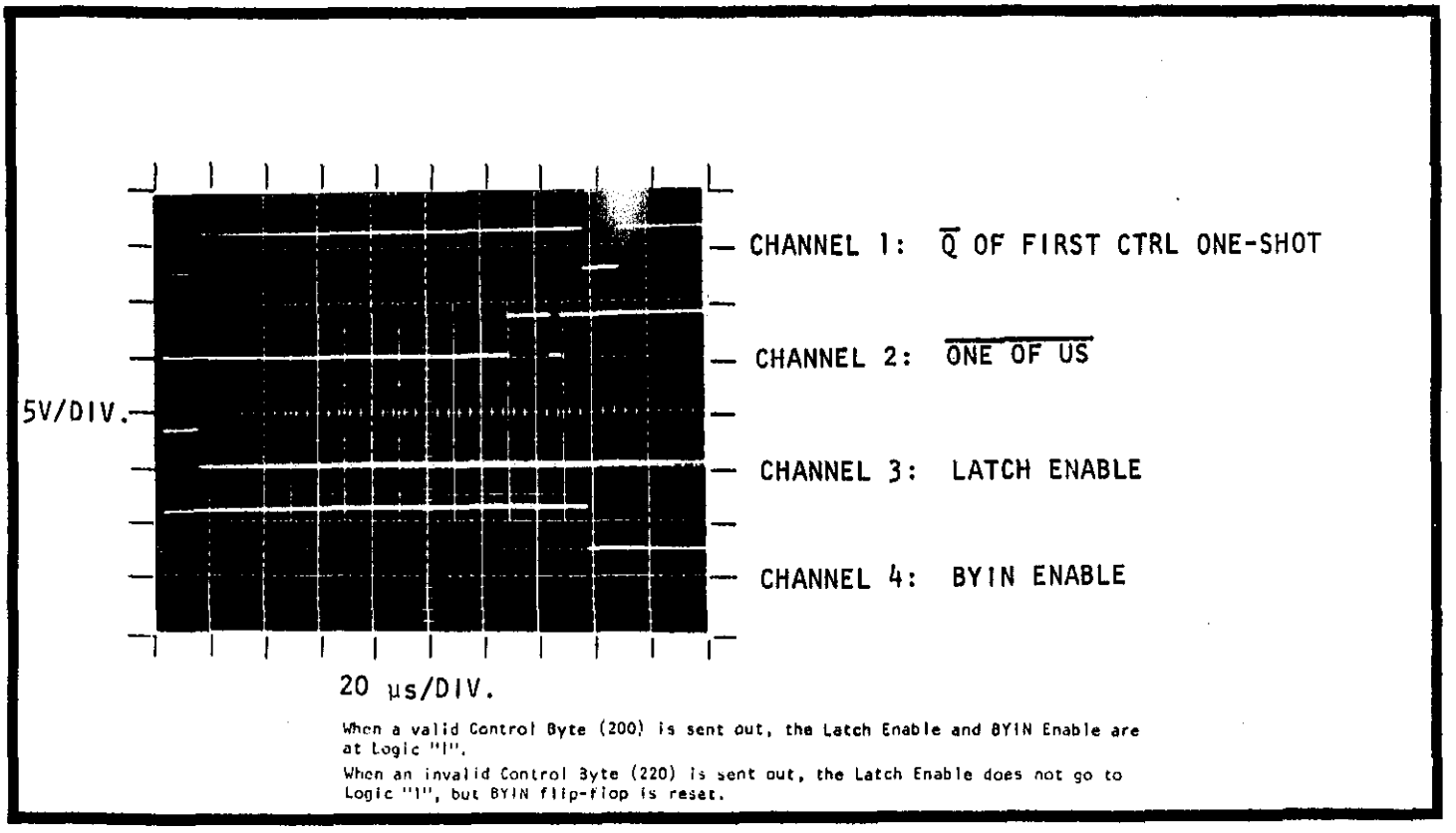


FIGURE 17. Trace For Test #11.

TABLE 5-8.

Program Needed to Perform Test #8 (Part 1)

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 001
1	0 0 1	
2	3 1 5	OPDB
3	3 4 7	SLCI
4	1 6 0	STI0
5	0 0 1	"1"
6	1 0 7	WAIT
7	1 6 1	RCI0
8	2 2 0	JU00, 002
9	0 0 2	

TABLE 5-9.

Program Needed To Perform Test #8 (Part 2)

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 376
1	3 7 6	
2	3 1 5	OPDB
3	3 4 7	SLCI
4	1 6 0	STI0
5	0 0 1	"1"
6	1 0 7	WAIT
7	1 6 1	RCI0
8	2 2 0	JU00, 002
9	0 0 2	

TABLE 5-10.

Program Needed to Perform Test #9

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	3 1 4	OPCB
1	0 5 6	HALT
2	3 1 5	OPDB
3	0 5 6	HALT
4	2 2 0	JU00, 002
5	0 0 2	

TABLE 5-11.

Program Needed to Perform Test #10

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 200
1	2 0 0	
2	3 1 4	OPCB
3	3 1 5	OPDB
4	3 1 5	OPDB
5	3 1 5	OPDB
6	3 1 5	OPDB
7	2 2 0	JU00, 000
8	0 0 0	

TABLE 5-12.

Program Needed to Perform Test #11

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 200
1	2 0 0	
2	3 1 4	OPCB
3	3 4 1	ICIH
4	3 1 4	OPCB
5	2 2 0	JU00, 000
6	0 0 0	

TABLE 5-13.

Program Needed to Perform Test #12

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 200
1	2 0 0	
2	3 1 4	OPCB
3	3 4 0	ICIL
4	0 5 6	HALT
5	2 2 0	JU00, 002
6	0 0 2	

m. Test #12. This procedure checks the Control Byte Operation Decoder. The Control Byte operation Decoder decodes the IL portion of a Control Byte. A program must be loaded into the PCU to obtain an OPCB condition.

1. Enter the program listed in Table 5-13. (See page 5-13.)

2. Set the RUN/STEP/LOAD switch on the PCU to RUN.

3. Set the oscilloscope as follows:

   a) Vertical Sensitivity - 2 volts/div.

   b) Horizontal Sweep - 50 ms/div.

   c) Trigger Source - AUTO Trigger.

4. Run the program beginning at branch point 0 0.

5. Make a connection between Channel 1 Input and the following pins on Interface Number 1: 1 (SA1), 2 (SA2), 3 (SA3), 13 (C0), 19 (C1), 17 (C2) and U121-10 (SCAN ADDR) on the Model 780 pc board.

6. Verify that the signals in Table 5-14 are at Logic "1" depending on the contents of IL. Each time RESUME is depressed another Control Byte will be sent out of the PCU and the contents of IL will be incremented by one. After IL = 15, the program loops to IL = 0.

NOTE

The operation codes above a decimal 10 are not presently used by the Control Unit, except 13 (RESET) which is IH independent.

TABLE 5-14.

Summary of Signal Condition

ACTION	(BASE 10) IL CONTENTS	STATUS OF SIGNAL LINES						
		SA1	SA2	SA3	C0	C1	C2	SCAN ADDR
Run Program	0	1	x	x	1	x	x	x
Depress Resume	1	x	1	x	1	x	x	x
Depress Resume	2	x	x	1	1	x	x	x
Depress Resume	3	x	x	x	1	x	x	1
Depress Resume	4	1	x	x	x	1	x	x
Depress Resume	5	x	1	x	x	1	x	x
Depress Resume	6	x	x	1	x	1	x	x
Depress Resume	7	x	x	x	x	1	x	1
Depress Resume	8	1	x	x	x	x	1	x
Depress Resume	9	x	1	x	x	x	1	x
Depress Resume	10	x	x	1	x	x	1	x
Depress Resume	11	x	x	x	x	x	1	1
Depress Resume	12	1	x	x	x	x	x	x
Depress Resume	13	x	1	x	x	x	x	x
Depress Resume	14	x	x	1	x	x	x	x
Depress Resume	15	x	x	x	x	x	x	1
Depress Resume	0	1	x	x	1	x	x	x

x = Don't Care

n. Test #13. This test procedure checks the BYIN Enable Flip-Flop. A program must be loaded into the PCU to obtain an OPCB condition.

1. Enter the program listed in Table 5-15. (See page 5-19.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the oscilloscope as follows:
   a) Vertical Sensitivity 2 volts/div.
   b) Horizontal Sweep - 100µs/div. (MAIN TIME BASE)
      50µs/div. (DELAYED SWEEP)
   c) Trigger Source - Channel 1 (Negative slope).
4. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 Input to U118-10 (BYIN Enables F/F Q output).
   b) Connect Channel 2 Input to U107-1 ($\overline{\text{RESET}}$).
5. Run the program beginning at branch point 0 0.
6. Verify that output of BYIN F/F is:
   a) Set by a valid "one of us" code.
   b) Reset by a $\overline{\text{RESET}}$ signal.

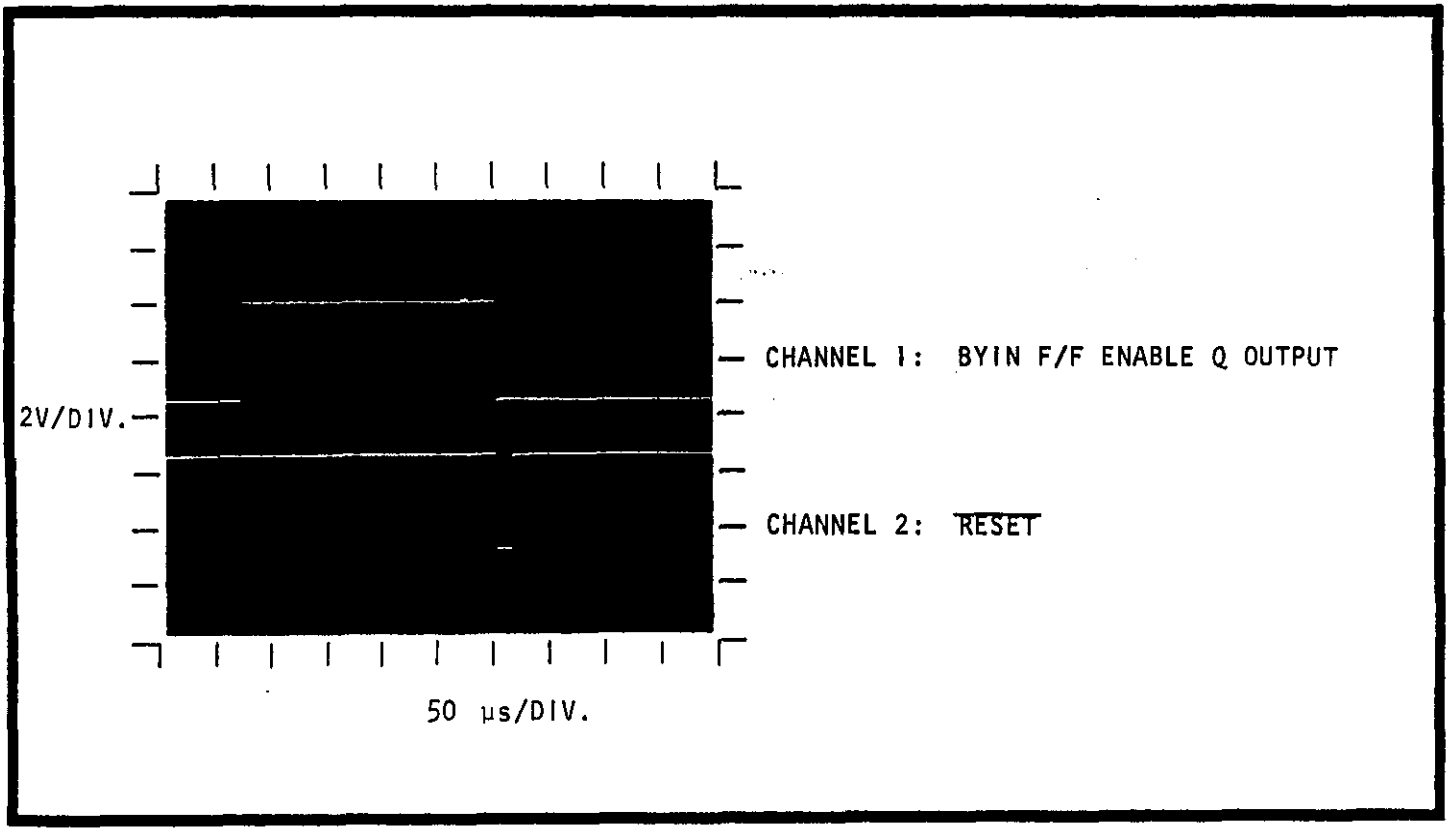


FIGURE 18. Trace For Test #13.

o. Test #14. This test procedure checks the IH Independent RESET Code Detector. This circuit detects Control Bytes with IH = don't care" and IL = 15 octal, such as RESET Control Byte. A program must be loaded into the PCU to obtain an OPCB condition.

1. Enter the program listed in Table 5-16. (See page 5-19.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the oscilloscope as follows:
   a) Vertical Sensitivity - 5 volts/div.
   b) Horizontal Sweep - 100µs/div. (MAIN TIME BASE)
      50µs/div. (DELAYED SWEEP)
   c) Trigger Source - Channel 1 (Negative Slope).
4. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 Input to U114-6 (Reset Code Detector output).
   b) Connect Channel 2 Input to U104-2 (First CTRL one-shot $\overline{Q}$).
   c) Connect Channel 3 Input to U104-1 (Reset Signal to OR Gate).
5. Run the program beginning at branch point 0 0.
6. Verify traces shown in Figure 19.

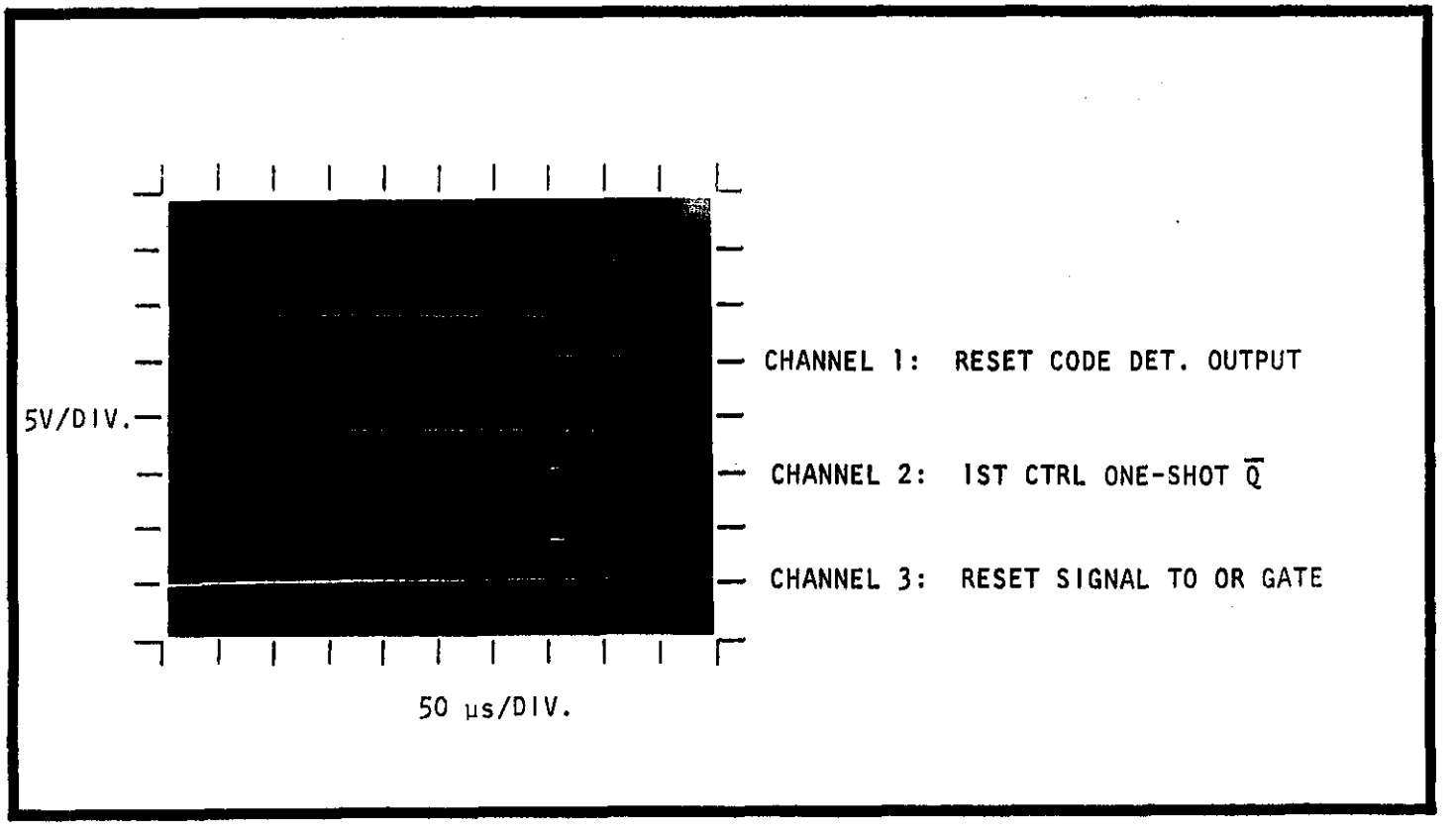


FIGURE 19. Trace For Test #14.

p. Test #15. This test procedure checks the Power Up Reset circuitry. This circuitry operates when power is first applied to the Control Unit. Both a RESET and a POWER UP RESET pulse is generated. No program is needed for this test. (No PCU connection is needed).

1. Set the oscilloscope as follows:

   a) Vertical Sensitivity - Channel 1: 2 volts/div.
   Channel 2: 1 volt/div.

   b) Horizontal Sweep - 50 ms/div.

   c) Trigger Source - See below for suggested settings using an oscilloscope with storage capability.

2. Make connections to the Control Unit circuitry as follows:

   a) Connect Channel 1 Input to U114-8 (Power Up Reset output).

   b) Connect Channel 2 Input to U114-9 (Input from RC circuit).

3. Set the oscilloscope to SINGLE SWEEP mode.

4. Manually start the sweep with the LEVEL control.

5. Turn on the Control Unit Power Switch when the sweep reaches the approximate center of the screen.

6. Verify a Power-Up Reset signal on Channel 1 as shown in Figure 20.

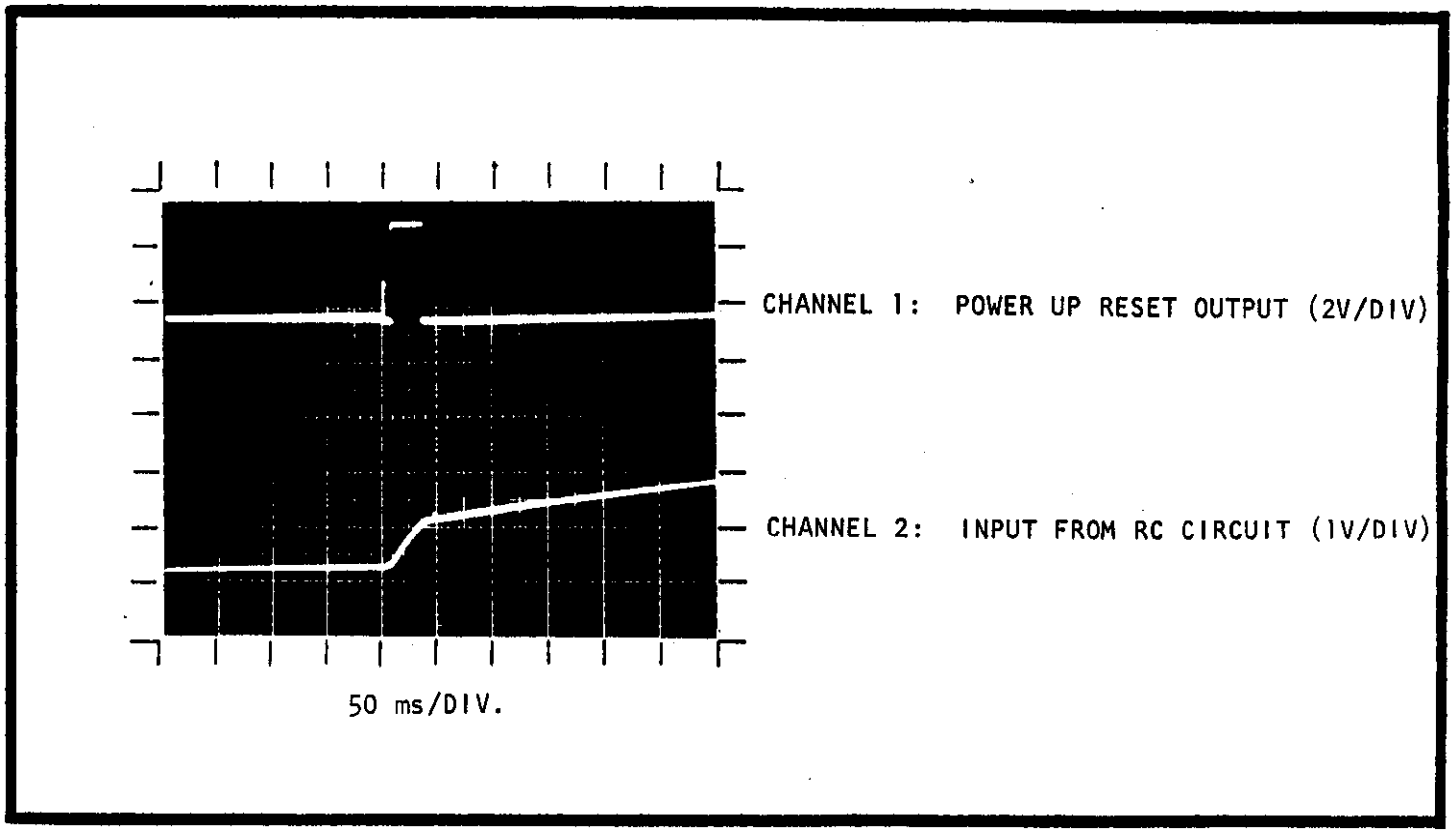


FIGURE 20. Trace For Test #15.

q. Test #16. This test procedure checks the RESET and $\overline{\text{RESET}}$ lines. A program must be loaded into the PCU to obtain an OPCB condition.

1. Enter the program listed in Table 5-17. (See page 5-19.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the oscilloscope as follows:
   a) Vertical Sensitivity - 5 volts/div.
   b) Horizontal Sweep - 50µs/div. (MAIN TIME BASE)
      10µs/div. (DELAYED SWEEP)
   c) Trigger Source - Channel 1, positive slope.
4. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 Input to U101-8 (RESET).
   b) Connect Channel 2 Input to U104-13 ($\overline{\text{RESET}}$).
   c) Connect Channel 3 Input to U104-2 (First CTRL One-Shot $\overline{Q}$).
5. Run the program beginning at branch point 0 0.

NOTE

The program will run continuously. Depress RESET to stop the program.

6. Verify that the FIRST CTRL one-shot $\overline{Q}$ goes to Logic "0" when RESET goes to Logic "1", as shown in Figure 21.

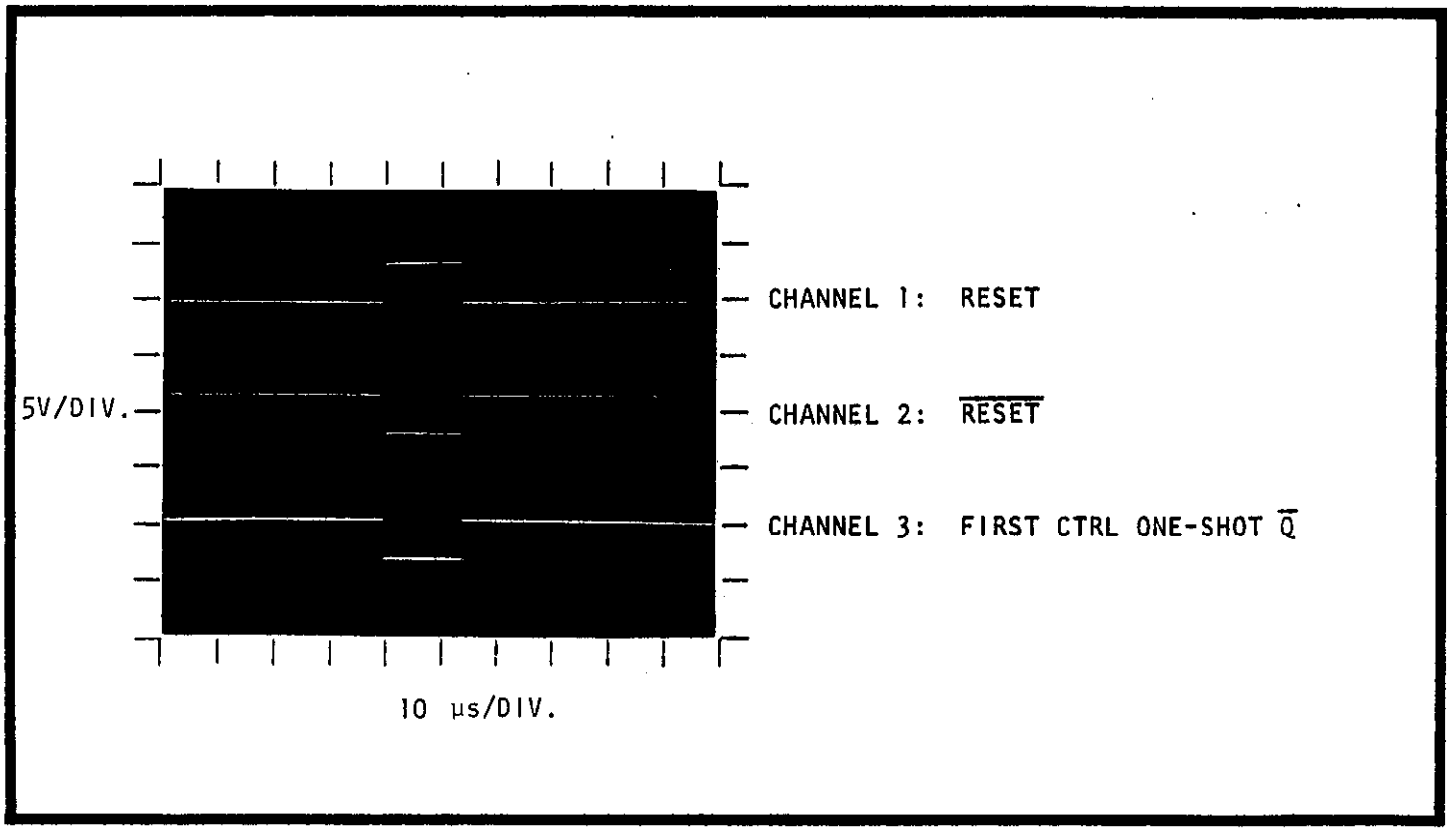


FIGURE 21. Trace For Test #16.

TABLE 5-15.

Program Needed to Perform Test #13

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 200
1	2 0 0	
2	3 1 4	OPCB
3	2 6 6	LDIX, 015
4	0 1 5	
5	3 1 4	OPCB
6	2 2 0	JU00, 000
7	0 0 0	

TABLE 5-16.

Program Needed to Perform Test #14

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 200
1	2 0 0	
2	3 1 4	OPCB
3	2 6 6	LDIX, 015
4	0 1 5	
5	3 1 4	OPCB
6	2 2 0	JU00, 000
7	0 0 0	

TABLE 5-17.

Program Needed to Perform Test #16

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 015
1	0 1 5	
2	3 1 4	OPCB
3	2 2 0	JU00, 000
4	0 0 0	

TABLE 5-18.

Program Needed to Perform Test #17

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 200
1	2 0 0	
2	3 1 4	OPCB
3	2 0 0	BR00, 015
4	0 1 5	
5	2 6 6	LDIX, 204
6	2 0 4	
7	3 1 4	OPCB
8	2 0 0	BR00, 015
9	0 1 5	
1 0	2 6 6	LDIX, 210
1 1	2 1 0	
1 2	3 1 4	OPCB
1 3	0 5 6	HALT
1 4	2 6 6	LDIX, 015
1 5	0 1 5	
1 6	3 1 4	OPCB
1 7	0 5 6	HALT
1 8	3 7 1	RCLP
1 9	3 7 1	RCLP

TABLE 5-19.

Program Needed to Perform Test #18

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 000
1	0 0 0	
2	3 1 5	OPDB
3	3 4 0	ICIL
4	0 5 6	HALT
5	2 2 0	JU00, 002
6	0 0 2	

r. Test #17. This test procedure checks the C0, C1 and C2 lines.* A program must be loaded into the PCU to obtain an OPCB condition.

1. Enter the program listed in Table 5-18.
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Run the program beginning at branch point 0 0.
4. Verify that SA1 and C0 are set to Logic "1".
5. Depress RESUME. A RESET will be sent out.
6. Verify that C0 is set to Logic "0".
7. Depress RESUME.
8. Verify that SA1 and C1 are set.
9. Depress RESUME.
10. Verify that RESET is sent out and C1 is reset.
11. Depress RESUME.
12. Verify that SA1 and C2 are set.
13. Depress RESUME.
14. Verify that RESET is sent out and C2 is reset.
15. To run the program again, jump to branch point 0 0 and RESUME.

*NOTE

These lines can be examined on connector J101, J102, or J103 as shown in Figure 6, page 3-2.

s. Test #18. This test procedure tests the Scanner interface circuitry (CHAD lines). A program must be loaded into the PCU.

1. Enter the program listed in Table 5-19. (See page 5-19.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the Oscilloscope as follows:
   a) Vertical Sensitivity - 2 volts/div.
   b) Horizontal Sweep - 2 ms/div.
   c) Trigger Source - Channel 1
4. Connect Channel 1 to the "TO SCANNER" connector at the various CHAD lines indicated in Table 5-20.
5. Run the program beginning at branch point 0 0.

NOTE

The program steps through the 16 possible combinations of addresses in binary sequence (mod 16). Verify that front panel indicators and CHAD lines are as given in Table 5-20.

TABLE 5-20.

Summary of CHAD Testing

Program Action	OUTPUT Indicators				"SCANNER" Lines (P110) (Pin 15) (Pin 2) (Pin 14) (Pin 1)				Remarks
	L8	L4	L2	L1	CHAD 8	CHAD 4	CHAD 2	CHAD 1	
Start Program	0	0	0	0	0	0	0	0	Channel 0 selected
RESUME	0	0	0	1	0	0	0	1	Channel 1 selected
RESUME	0	0	1	0	0	0	1	0	Channel 2 selected
RESUME	0	0	1	1	0	0	1	1	Channel 3 selected
RESUME	0	1	0	0	0	1	0	0	Channel 4 selected
RESUME	0	1	0	1	0	1	0	1	Channel 5 selected
RESUME	0	1	1	0	0	1	1	0	Channel 6 selected
RESUME	0	1	1	1	0	1	1	1	Channel 7 selected
RESUME	1	0	0	0	1	0	0	0	Channel 8 selected
RESUME	1	0	0	1	1	0	0	1	Channel 9 selected
RESUME	1	0	1	0	1	0	1	0	No Channel
RESUME	1	0	1	1	1	0	1	1	No Channel
RESUME	1	1	0	0	1	1	0	0	No Channel
RESUME	1	1	0	1	1	1	0	1	No Channel
RESUME	1	1	1	0	1	1	1	0	No Channel
RESUME	1	1	1	1	1	1	1	1	No Channel

t. Test #19. This test procedure tests the Scanner interface circuitry (LOCHAD lines), except for gates U126 and U127. A program must be loaded into the PCU. (No Scanner needs to be connected.)

1. Enter the program listed in Table 5-21. (See page 5-22.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the Oscilloscope as follows:
   a) Vertical Sensitivity - 2 volts/div.
   b) Horizontal Sweep - 2 ms/div.
   c) Trigger Source - AUTO trigger
4. Connect Channel 1 to the "SCANNER" connector at the various LOCHAD lines indicated in Table 5-22.
5. Run the program beginning at branch point 0 0.

NOTE

The program can be used to step through all eight LOCHAD commands. Verify that the logic on the appropriate LOCHAD line is as given in Table 5-22. Also verify that the correct indicators are lighted.

NOTE

Part 2 of Test #19 is continued on page 5-23.

TABLE 5-21.

Program Needed to Perform Test #19 (Part 1)

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 010
1	0 1 0	
2	1 6 3	STI1
3	2 6 6	LDIX, 001
4	0 0 1	
5	1 6 0	STI0
6	2 6 6	LDIX, 203
7	2 0 3	
8	3 1 4	OPCB
9	1 6 1	RCI0 .
1 0	3 1 5	OPDB
1 1	3 4 0	ICIL
1 2	1 6 0	STI0
1 3	1 6 4	RCI1
1 4	3 4 0	ICIL
1 5	1 6 3	STI1
1 6	2 6 0	JLNZ, 025
1 7	0 2 5	
1 8	0 5 6	HALT
1 9	2 2 0	JU00, 000
2 0	0 0 0	
2 1	0 5 6	HALT
2 2	2 2 0	JU00, 006
2 3	0 0 6	

TABLE 5-22.

Summary of Test Points Used in Test #19.

Scanner LOCHAD Line	U125 Logic Levels								"SCANNER" Connector P110	OUTPUT Indicators			
	2	3	4	5	6	7	9	10	Pin No.	L8	L4	L2	L1
1	0	1	1	1	1	1	1	1	16	0	0	0	0
2	1	0	1	1	1	1	1	1	12	0	0	1	0
3	1	1	0	1	1	1	1	1	25	0	0	1	1
4	1	1	1	0	1	1	1	1	13	0	1	0	0
5	1	1	1	1	0	1	1	1	26	0	1	0	1
6	1	1	1	1	1	0	1	1	5	0	1	1	0
7	1	1	1	1	1	1	0	1	6	0	1	1	1
8	1	1	1	1	1	1	1	0	7	1	0	0	0

Part 2 of Test #19

6. Enter the program listed in Table 5-23.
7. Set the RUN/STEP/LOAD switch on the PCU to RUN.
8. Set the Oscilloscope as follows:
   a) Vertical Sensitivity - 2 volts/div.
   b) Horizontal Sweep - 10µs/div.
   c) Trigger Source - Channel 1, positive slope.
9. Connect Channel 1 to the "SCANNER" connector at the various LOCHAD lines indicated in Table 5-22.
10. Run the program beginning at branch point 0 0.
11. Verify the waveform shown in Figure 22. (See page 5-24.)

NOTE

The program runs continuously. To halt the program, depress RESET. The program has been written specifically for LOCHAD 1 only. To test the remaining 7 LOCHAD lines the program must be altered. For example, to test LOCHAD 2, change location 0004 to code 002 instead of code 001.

TABLE 5-23.

Program Needed to Perform Test #19 (Part 2)

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 203
1	2 0 3	
2	3 1 4	OPCB
3	2 6 6	LDIX, 001
4	0 0 1	
5	3 1 5	OPDB
6	3 1 5	OPDB
7	2 2 0	JU00, 000
8	0 0 0	

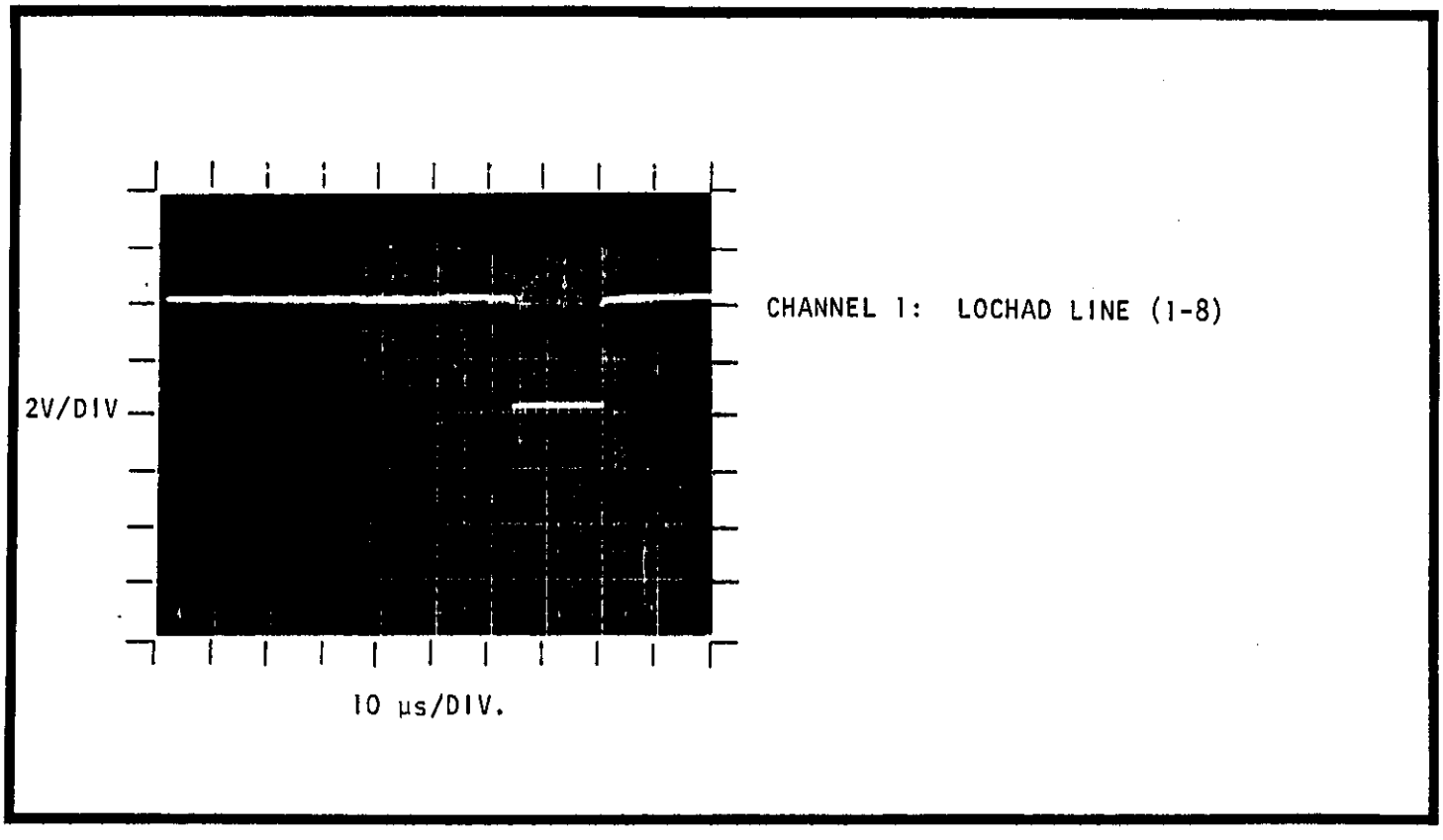


FIGURE 22. Trace For Test #19 (Part 2).

u. Test #20. This test procedure checks the Scanner interface circuitry (Latch Enable). *A program must be loaded into the PCU to obtain OPCB and OPDB conditions.*

1. Enter the program listed in Table 5-24. (See page 5-28.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the Oscilloscope as follows:
   a) Vertical Sensitivity - 5 volts/div.
   b) Horizontal Sweep - 200µs/div. (MAIN TIME BASE)
      50µs/div. (DELAYED SWEEP)
   c) Trigger Source - Channel 1, positive slope.
4. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 Input to U104-6 ($\overline{DP}$).
   b) Connect Channel 2 Input to U117-2 (CO • SCAN ADDR).
   c) Connect Channel 3 Input to U121-5 (BCO).
   d) Connect Channel 4 Input to U108-10 (Latch Enable).
5. Run the program beginning at branch point 0 0.
6. Verify that Latch Enable is at Logic "1" under the following conditions:
   a) CO • SCAN ADDR is at Logic "1".
   b) BCO is at Logic "1".
   c) $\overline{DP}$ is at Logic "0".

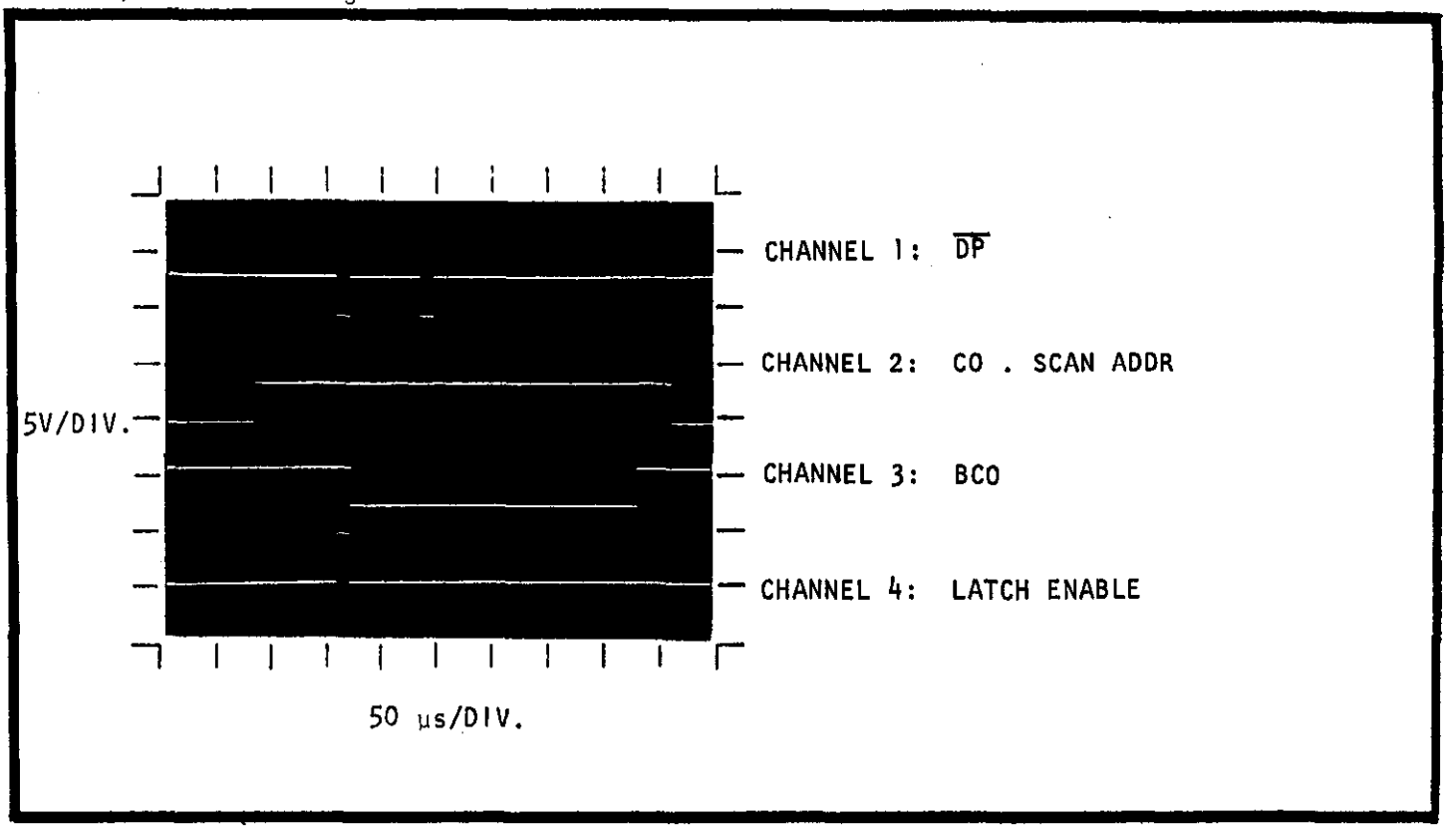


FIGURE 23. Trace For Test #20.

v. Test #21. This test procedure checks the Scanner interface circuitry (LOCHAD Enable). A program must be loaded into the PCU to obtain OPCB and OPDB conditions.

1. Enter the program listed in Table 5-24 (same program used in Test No. 20).
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the Oscilloscope as in Test No. 20.
4. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 Input to U104-6 ($\overline{DP}$).
   b) Connect Channel 2 Input to U117-2 (CO • SCAN ADDR).
   c) Connect Channel 3 Input to U121-1 (BC1).
   d) Connect Channel 4 Input to U121-3 (LOCHAD Gate Enable).
5. Run the program beginning at branch point 0 0.
6. Verify that LOCHAD Gate Enable is at Logic "0" under the following conditions:
   a) CO • SCAN ADDR is at Logic "1".
   b) BC1 is at Logic "1".
   c) $\overline{DP}$ is at Logic "0".

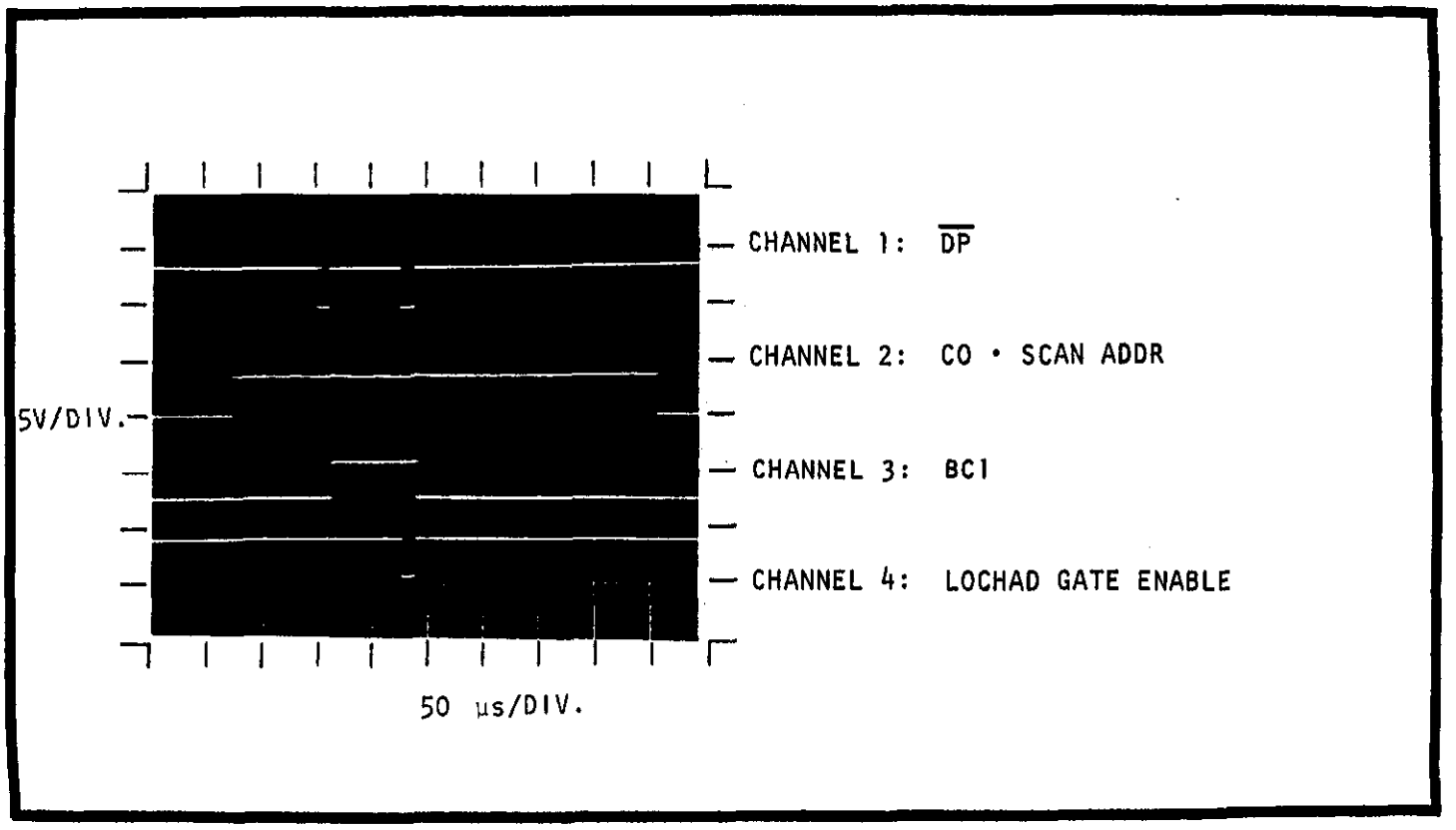


FIGURE 24. Trace For Test #21.

w. Test #22. This test procedure is used to check the Input Data Register. A program must be loaded into the PCU to obtain OPCB and IPDB conditions.

1. Enter the program listed in Table 5-25 (See page 5-28.)
2. Set the RUN/STEP/LOAD switch on the PCU to RUN.
3. Set the Oscilloscope as follows:
   a) Vertical Sensitivity - Channel 1, 2: 5 volts/div.
      Channel 3: 2 volts/div.
   b) Horizontal Sweep - 50µs/div. (MAIN TIME BASE)
      5µs/div. (DELAYED SWEEP)
   c) Trigger Source - Channel 1, positive slope.
4. Make connections to the Control Unit circuitry as follows:
   a) Connect Channel 1 Input to U109-1 (Data Byte Detector Output).
   b) Connect Channel 2 Input to U109-2 (PCU Clock Signal).
   c) Connect Channel 3 Input to U108-11 (PCU Byte Input Line).
5. Run program beginning at branch point 0 0.
6. Verify traces shown in Figure 25.

NOTE

The OPCB instruction sends out a Control Byte with 200 code. This is a "one-of-us" code and sets the BYIN Flip-Flop to enable the BYIN line. The data being applied to the INPUT REGISTER is (L1 to H8) 01001011 binary.

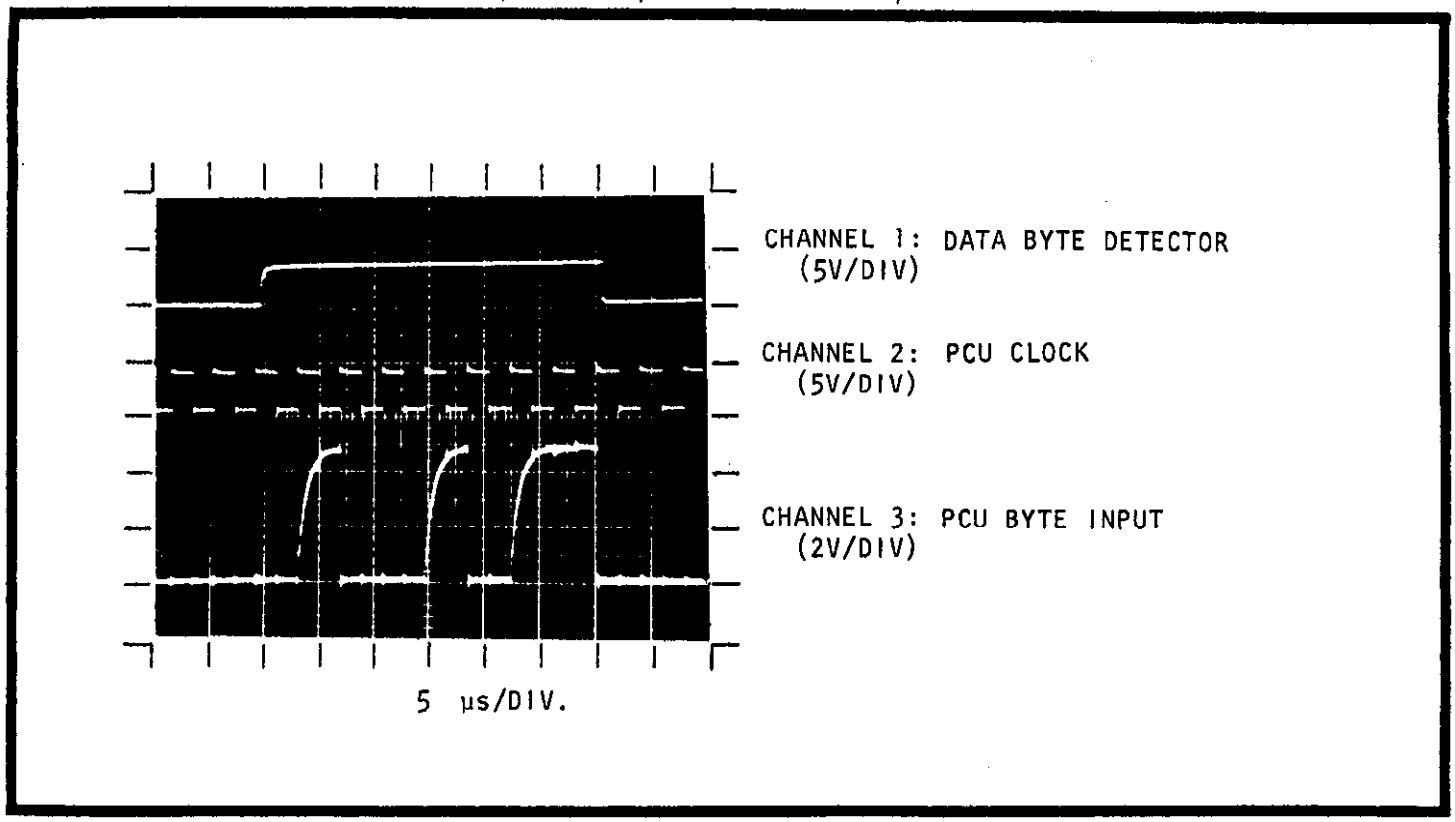


FIGURE 25. Trace For Test #22.

TABLE 5-24.

Program Needed to Perform Test #20

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 203
1	2 0 3	
2	3 1 4	OPCB
3	3 1 5	OPDB
4	3 1 5	OPDB
5	2 6 6	LDIX, 200
6	2 0 0	
7	3 1 4	OPCB
8	2 2 0	JU00, 000
9	0 0 0	

TABLE 5-25.

Program Needed to Perform Test #22

DECIMAL STEP	INSTRUCTION CODE	INSTRUCTION MNEMONIC
0 0 0 0	2 6 6	LDIX, 200
1	2 0 0	
2	3 1 4	OPCB
3	3 0 5	IPDB
4	3 0 5	IPDB
5	2 2 0	JU00, 003
6	0 0 3	

SECTION 6. ACCESSORIES

6-1. RACK MOUNTING KIT. (Similar to hardware supplied with Model 1007 Rack Mounting Kit)

a. General. The rack mounting hardware furnished with the instrument permits standard 3-1/2 in. x 19 in. rack mounting, 15-1/2 in. (395 mm) depth behind the front panel. The hardware included consists of two angle brackets and extra mounting screws.

b. Installation Instructions.

1. Remove the "side dress" panels on both sides of the instrument as follows:

a) Remove two screws (#6-32 x 1/4) on each side of the instrument.

b) Slide the "side dress" panels toward the rear of the instrument to remove.

2. Install an "angle bracket" (Item 21) on each side using longer screws (Items 22 and 28) in place of original screws (a total of three screws is needed per side).

TABLE 6-1.

Parts List For Rack Mounting Kit

Item No.	Description	Qty Req'd	Keithley Part No.
21	Angle Bracket	2	27410B
22	Screw, #6-32 x 5/8, Phillips	4	--
28	Screw, #6-32 x 1/2, Phillips	2	--

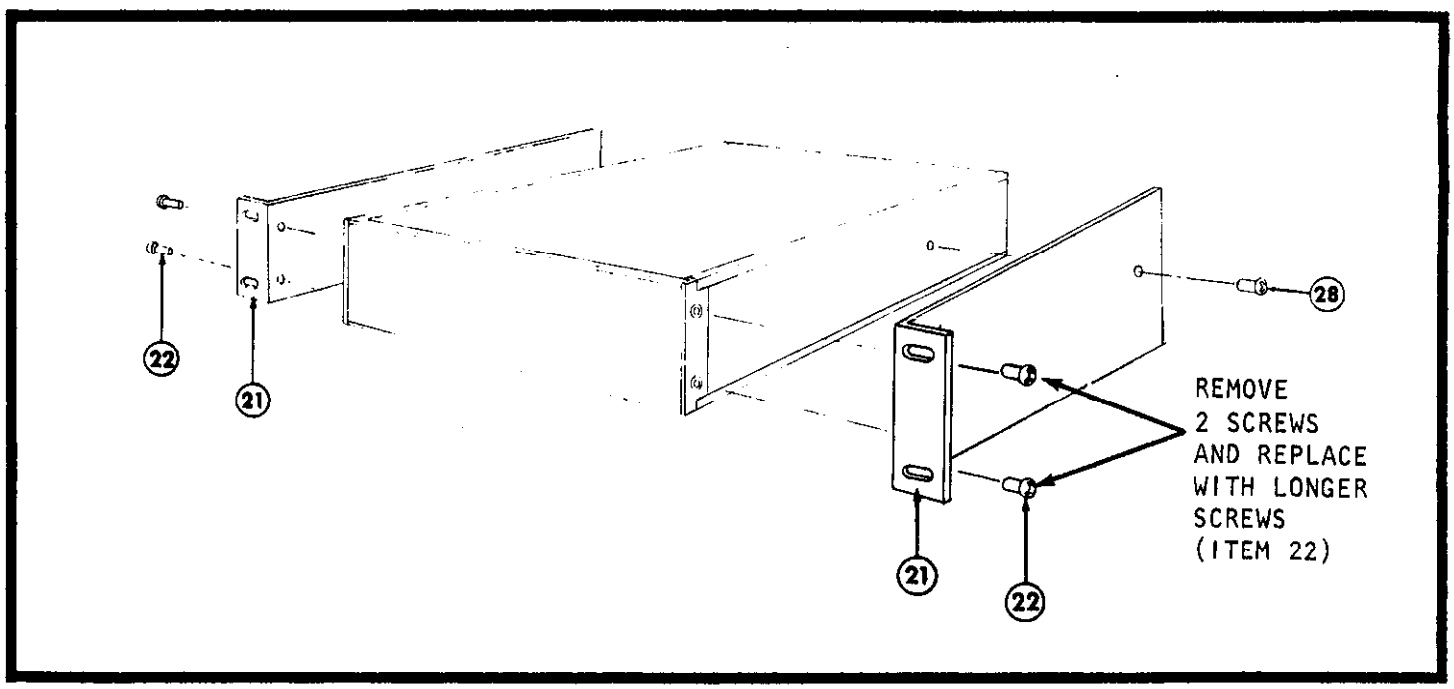


FIGURE 26. Rack Mounting of the Control Unit.

6-2. MULTI-SCANNER COUPLER (Model 7819-MSC).

a. General. The Multi-Scanner Coupler provides additional connections for up to 8 Scanners. I/O Handler Software, furnished with any Series 7801 Instrument Interface, Series 7802, or Model 7813, may be used to control multiple Scanners connected to the MSC.

1. A single Model 7021-10 System Interconnect Cable is furnished with the MSC to couple to the Control Unit.

2. In addition, the MSC provides eight connectors which mate with any System Interconnect Cable (furnished with each Scanner).

3. A set of slide switches enable the user to modify the Scanner interconnections if necessary. When set to NORMAL, only one active Scanner at a time is permitted.

NOTE

Each switch connects the Scanner VCH line (pin 24) to a "VCH bus", when set to NORMAL (ON). If it is desired to use the System 1 for parallel-channel or matrix operation refer to *PCV PROGRAMMING TECHNIQUES*. The I/O Handler program must be altered to permit parallel-channel selections since the software routine sends out a REMOTE ALL OFF signal prior to executing a new channel address. See also schematic 27357D in Section 7 of this manual.

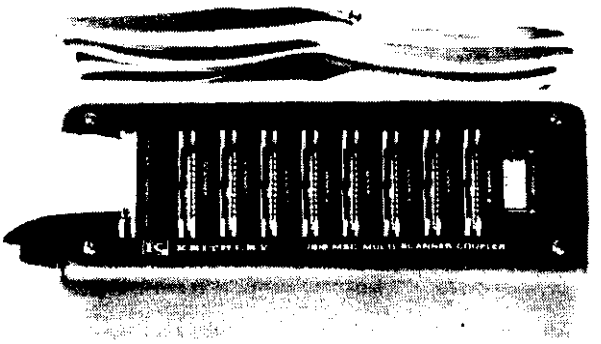


FIGURE 27. Multi-Scanner Coupler (Model 7819-MSC).

SPECIFICATIONS

GENERAL: Couples single scanner output connector of Model 780 to eight connectors for controlling up to eight Model 702 Scanners. Total length (sum) of all scanner interconnection cables must not exceed 40 feet.
MULTIPLE-CHANNEL SELECT: Scanner interconnections prevent inadvertent selection of multiple channels. This protection feature can be defeated by switches on Model 7819-MSC, permitting one channel on each scanner to be selected for parallel-channel or matrix operation.
SIZE, WEIGHT: 2 in. high x 9 in. wide x 3-1/2 in. deep (50 x 230 x 90 mm). Net weight, 1-1/4 pounds (0.6 kg).
ACCESSORIES FURNISHED: Model 7021-10 cable, 10 ft. (3m) long.

b. How to Install the MSC.

1. Connect a System Interconnect Cable (Model 7021-2 or Model 7021-10) between SCANNER on the Control Unit and TO 780 CONTROL UNIT on the MSC.

2. Connect Scanner 1 DIGITAL INPUT and SCANNER 1 input on the MSC, Scanner 2 DIGITAL INPUT and SCANNER 2 input on the MSC, etc.

NOTE

Total length (sum) of all scanner interconnection cables must not exceed 40 feet.

3. Set all slide switches on the MSC to NORMAL.

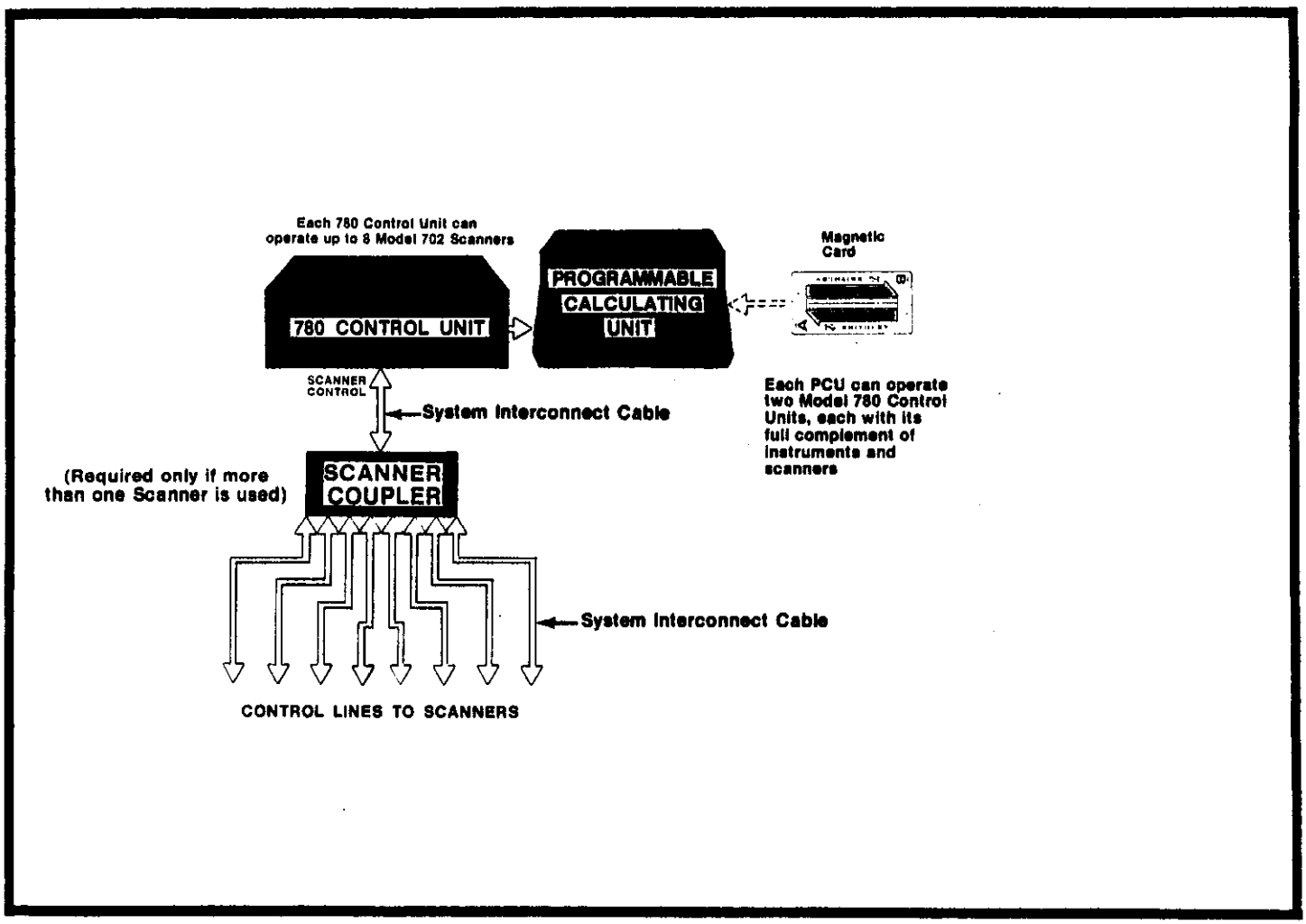


FIGURE 28. Typical System 1 Multi-Scanner Connection.

6-3. INTERFACE EXTENDER CARD (Model 7819-IEC). This Interface Card is a System 1 compatible plug-in board that mates with a card-edge connector at Interface Number 1, 2, or 3 on a Control Unit. It permits operation of an Interface (Series 7801) or special-purpose card (Series 7802 and 7813) external to the Model 780 for troubleshooting and repair.

6-4. CUSTOM INTERFACE (Model 7802-CIK).

a. The Custom Interface Card is a System 1 compatible plug-in board for constructing custom interfaces. Provision is made for accessibility to input, output, and control signals (TTL) on the Control Unit.

b. The printed circuit board accepts up to 20 sixteen-pin wire-wrapped DIP sockets. All internal and external connections are terminated in pads for wire-wrappable post insertion.

c. Power is available from the Control Unit to supply logic power. Circuit tapes are provided for power and ground distribution.

d. Due to the card structure the CIK can be installed at Interface Number 3 or Interface Number 1 (if Interface Number 2 is empty). Clearance for wire-wrappable pins prohibits installation of a CIK in Interface Number 2.

e. Typical mating components which may be used with the Model 7819-CIK include the following.

1. Wire-wrappable 14-pin DIP socket, Amphenol part no. 82120013-144 (not furnished).
2. Wire-wrappable 16-pin DIP sockets, Amphenol part no. 82120013-164 (not furnished).
3. PC-mountable 50-pin ribbon-cable header, Keithley part no. CS-311 (not furnished).
4. Wire-wrappable terminals, Vector T44-1 (not furnished).

NOTE

No active electronic components are furnished with the CIK.

SPECIFICATIONS, MODEL 7802-CIK

GENERAL: PC board for convenient construction of custom interfaces. Provides access to System 1 input, output, and control signals (TTL).
COMPONENT MOUNTING: PC board accepts up to 20 sixteen-pin wire-wrappable DIP sockets. All internal and external connections terminated in pads for wire-wrappable post insertion.
CONNECTORS:
INTERNAL: 50-pin gold-plated card edge mates with connector in Model 780 Control Unit.
EXTERNAL: Provision for PC mounting of 50 conductor ribbon-cable header (3M® Model 3426-0000), or metal mounting plate may be machined to accept a connector.
POWER AVAILABLE: Logic power; +5 volts referenced to PCU ground, 0.5 amperes maximum. Power and ground are distributed on board.
SIZE, WEIGHT: 4-1/2 in. x 9 in. (115 x 230 mm) printed circuit card. Depth with wire-wrappable posts installed limits mounting to slot 3 in Model 780, and slot 1 if slot 2 is not used. Net weight, 3 ounces (85 g).
ACCESSORIES FURNISHED: Card latch/pull assembly and external connector mounting plate are attached.

f. Limitations on Signal Lines.

1. Output Lines. In general, each Output line can drive a maximum of three TTL loads. The Slot Address (SA) lines can drive up to eight TTL loads. If more drive capability is needed, a buffer can be used, consisting of two 7404 Series inverters connected in series.

2. Input Lines. The data input lines must be driven with open collector gates. Use 7401 Series Quad 2-Input NAND gates for DIL2 through DIH8. Use a power gate such as an MC858 to drive DIL1. The data input line drivers must be disabled when they are not actively driving the lines.

NOTE

Pull-up resistors are furnished on the pc board in the Control Unit for DIL1-DIH8 lines.

g. Limitations on +5V Power Supply. The Model 7802-CIK may draw a maximum of 0.5 ampere.

h. Custom Interface Design. Since an interface used with the System 1 involves both I/O Handler Software and interface circuitry (hardware), the designer should be thoroughly familiar with contents of the following manuals.

1. *INSTRUCTION MANUAL, Control Unit, Model 780*
2. *PCU PROGRAMMING TECHNIQUES*
3. *PCU ADVANCED PROGRAMMING*

NOTE

An interface design such as any series 7801 Interface may be used as an example when designing a custom interface.

6-5. DUAL CONTROL UNIT COUPLER (Model 7819-DCC). The DCC is a field-installable accessory that may be used to expand any System 1 for use with two Control Units. The DCC provides a 37-pin connector into which a second Control Unit may be plugged. (See pages 2-4 and 2-5 for detailed installation instructions.)

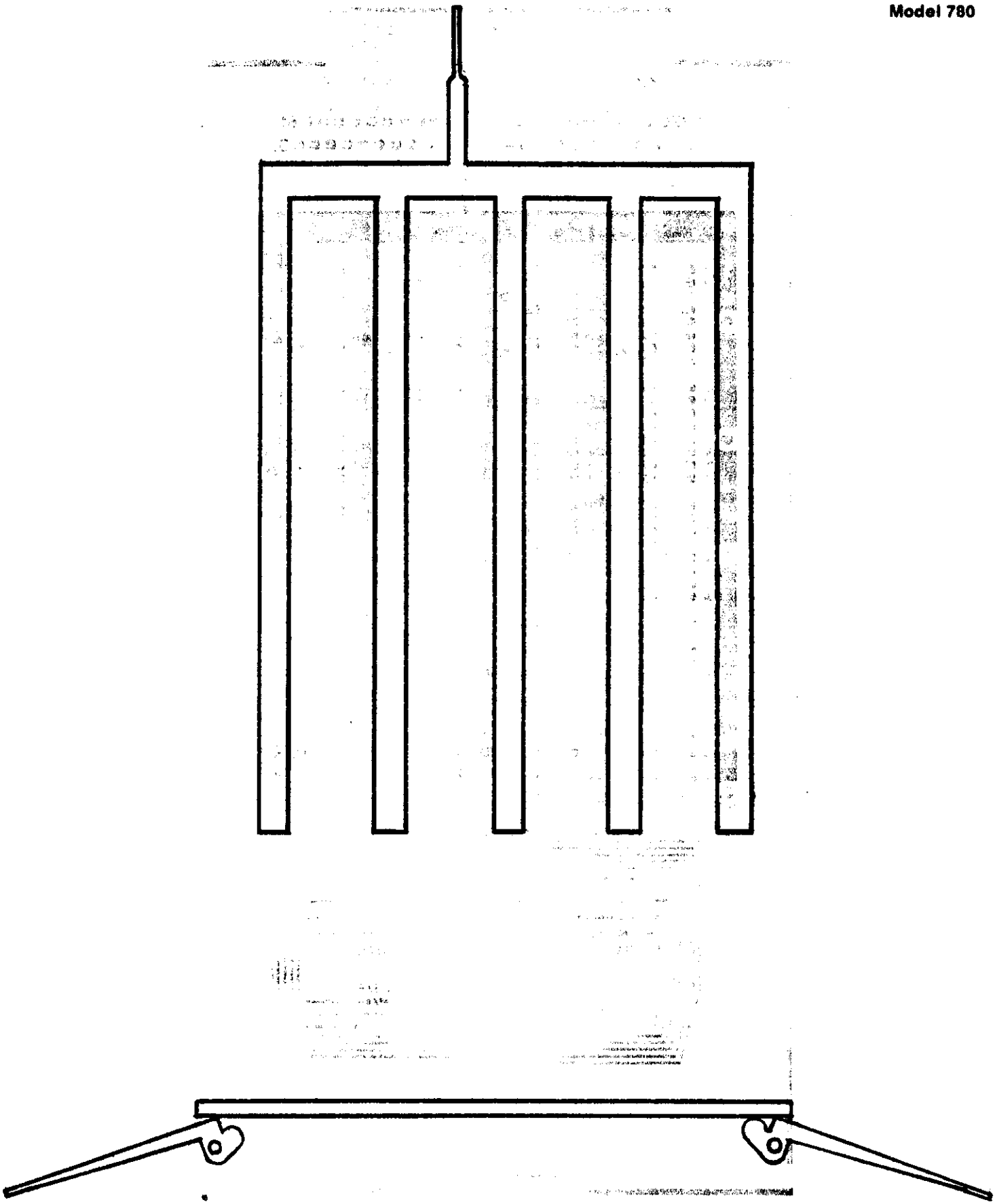


FIGURE 29. Custom Interface (Model 7802-CIK)

SECTION 7. REPLACEABLE PARTS

7-1. GENERAL. This section contains information for ordering replacement parts. The parts list is arranged in alphabetical order of their Circuit Designations.

7-2. ORDERING INFORMATION. To place an order or to obtain information concerning replacement parts, contact your Keithley representative or the factory. See the inside front cover of the catalog for addresses. When ordering, include the following information.

a. Instrument Model Number

b. Instrument Serial Number

c. Part Description

d. Circuit Designation (if applicable)

e. Keithley Part Number.

7-3. SCHEMATICS.

a. Control Unit, PC-383, PC-395. Schematic Number 27007E describes all Control Unit circuitry including the Scanner interface.

b. Instrument Interfaces. Schematics for all accessory interfaces are found in the individual *INSTRUCTION MANUAL* for Series 7801, 7802, and 7813 interfaces.

c. Multi-Scanner Coupler (Model 7819-MSC). Schematic 27357D

TABLE 7-1.

PC Board Designation Series

Series	Description	Designation	Page No.
100	Control Unit, Logic	PC-395	7-5
600	Display Board	PC-383	7-5

TABLE 7-2.

Mechanical Parts List

Item No.	Description	Qty. Per Assembly	Keithley Part No.	Figure No.
-	Chassis Assembly	-	--	30
-	Front Panel Assembly	-	--	
1	Front Panel	1	26860C	
2	Screw, Slotted, 6-32 x 3/8	4	--	
3	Front Panel Overlay	1	26865C	
4	Rear Panel	1	26892C	
5	Side Extrusion Left	1	24378B	
6	Side Extrusion Right	1	24378B	
7	Corner Bracket	2	24745B	
8	Screw, Socket, 6-32 x 1/4	4	--	
9	Screw, Phillips, 6-32 x 1/4	4	--	
10	Clip for Side Dress	2	FA-101	
11	Side Dress Panel	2	24360B	
-	Top Cover Assembly	-	--	30
12	Top Cover	1	26875C	
13	Screw, Socket, 6-32 x 5/16	4	--	
-	Bottom Cover Assembly	-	27264B	30
14	Bottom Cover	1	27263C	
15	Screw, Socket, 6-32 x 5/16	4	--	
-	Feet Assembly	-	--	
16	Molded Foot	4	24322B	
17	Rubber Foot	4	FE-6	
18	Tilt Bail	1	14704B	
19	Screw, Phillips, 6-32	4	--	
20	Kep Nut, 6-32	4	--	

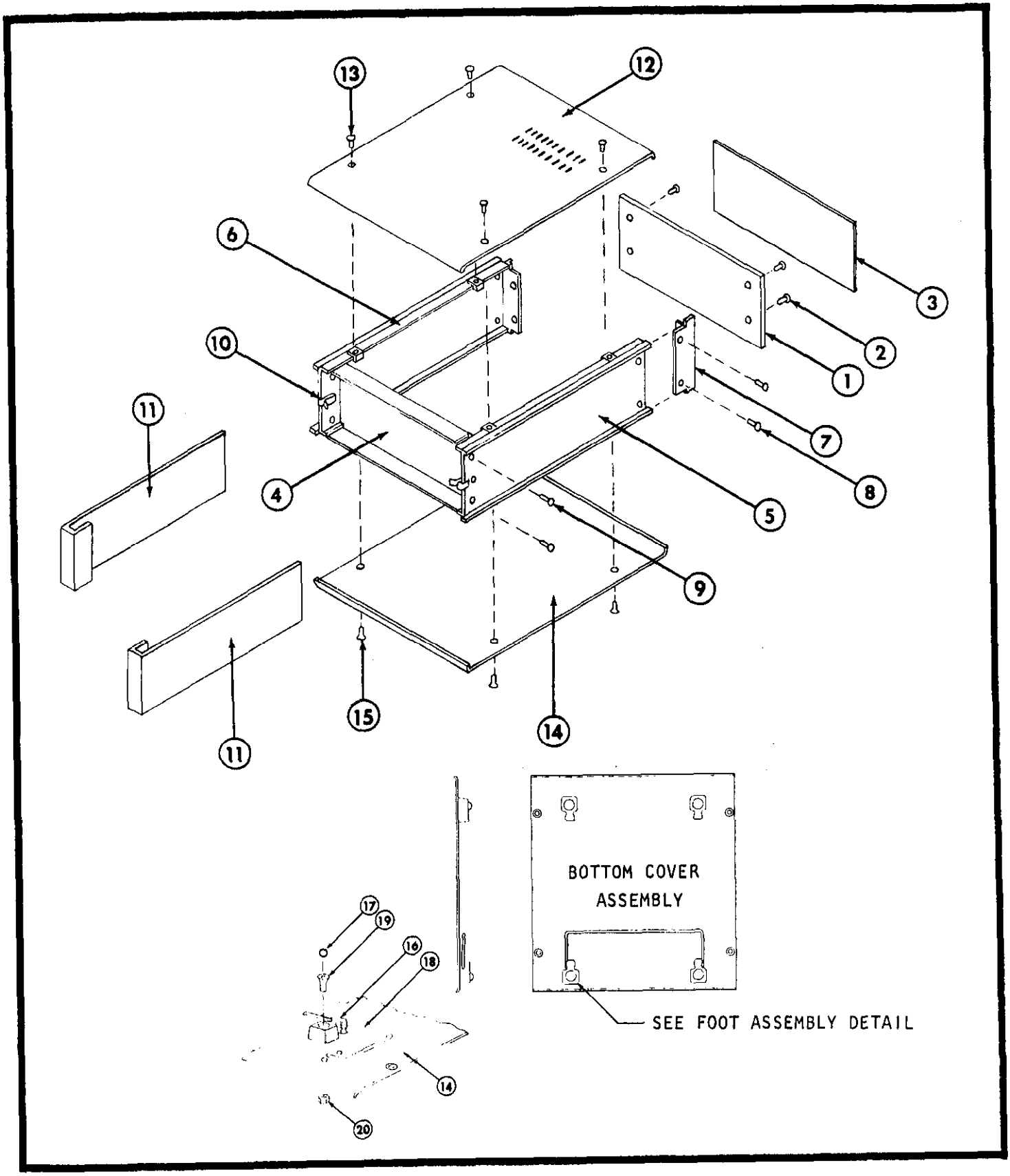


FIGURE 30. Chassis Assembly

TABLE 7-3.

Cross-Reference of Manufacturers

ABREV.	NAME AND ADDRESS	ABREV.	NAME AND ADDRESS
A-B	Allen-Bradley Corp. Milwaukee, WI 53204	KI	Keithley Instruments, Inc. Cleveland, OH 44139
ALCO	Alco Electronic Products, Inc. North Andover, MA 01845	MALL	Mallory Capacitor Indianapolis, IN 46206
BERG	Berg Electronics, Inc. New Cumberland, PA 17070	MOLEX	Molex Downers Grove, IL 60515
BUSS	Bussmann Mfg. Div. St. Louis, MO 63107	MOT	Motorola Semiconductor Products Phoenix, AZ 85008
C-W	Continental-Wirt Electronics Corp. Warminster, PA 18974	NAT	National Semiconductor Corp. Santa Clara, CA 95051
CAN	ITT Cannon Electric Santa Ana, CA 92702	REI	Richey Electronics, Inc. Nashville, TN 37213
CENLB	Centralab Division Milwaukee, WI 53201	S-C	Switchcraft, Inc. Chicago, IL 60630
COMPI	Components, Inc. Beddeford, ME 04005	SIG	Signetics Corp. Sunnyvale, CA 94086
ECI	Electrocube Inc. San Gabriel, CA 91776	SOL	Solitron Devices, Inc. Tappan, NY 10983
ERIE	Erie Technological Products, Inc. Erie, PA 16512	TEXAS	Texas Instruments, Inc. Dallas, TX 75231
H-P	Hewlett-Packard Palo Alto, CA 94304	3M	3M Company Headquarters St. Paul, MN 55101

CAPACITORS

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
C101	10000 µF, 15V	MALL	TCG103U015N3C3P	C-266-10000M	1
C102	0.47 µF, 20V, ET	COMPI	TD1-20-474-20	C-179-0.47M	2
C103	0.47 µF, 20V, ET	COMPI	TD1-20-474-20	C-179-0.47M	-
C104	100 µF, 15V, EAL	REI	JC6100158P	C-210-100M	1
C105	0.01 µF, 16V, CerD	CENLB	UK16-104	C-238-0.01M	10
C106	0.01 µF, 16V, CerD	CENLB	UK16-104	C-238-0.01M	-
C107	0.01 µF, 16V, CerD	CENLB	UK16-104	C-238-0.01M	-
C108	0.01 µF, 16V, CerD	CENLB	UK16-104	C-238-0.01M	-
C109	0.01 µF, 16V, CerD	CENLB	UK16-104	C-238-0.01M	-
C110	0.01 µF, 16V, CerD	CENLB	UK16-104	C-238-0.01M	-
C111	22 µF, 20V, ET	COMPI	TD1-20-226-20	C-179-22M	1
C112	0.0022 µF, 500V, CerD	ERIE	831-Z5U0-222M	C-22-0.0022M	2
C113	0.0022 µF, 500V, CerD	ERIE	831-Z5U0-222M	C-22-0.0022M	-
C114	0.01 µF, 50V, Metal Poly Carbonate	ECI	625B1A	C-201-0.01M	3
C115	0.01 µF, 50V, Metal Poly Carbonate	ECI	625B1A	C-201-0.01M	-
C116	0.01 µF, 50V, Metal Poly Carbonate	ECI	625B1A	C-201-0.01M	-
C117	0.01 µF, 16V, CerD	CENLB	UK16-104	C-238-0.01M	-
C118	0.01 µF, 16V, CerD	CENLB	UK16-104	C-238-0.01M	-
C119	0.01 µF, 16V, CerD	CENLB	UK16-104	C-238-0.01M	-
C120	0.01 µF, 16V, CerD	CENLB	UK16-104	C-238-0.01M	-
C121	680 pF, 1000V, CerD	CENLB	DD-681	C-64-680P	1

DIODES

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
CR101	Rectifier, 3A, 50V (1N4139)	SOL	3A50	RF-34	2
CR102	Rectifier, 3A, 50V (1N4139)	SOL	3A50	RF-34	-
CR103	Rectifier, 75 mA, 75V	TEXAS	1N914	RF-28	3
CR104	Rectifier, 75 mA, 75V	TEXAS	1N914	RF-28	-
CR105	Rectifier, 75 mA, 75V	TEXAS	1N914	RF-28	-

DIGITAL DISPLAY

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
DS601	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	18
DS602	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS603	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS604	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS605	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-

DIGITAL DISPLAY (Cont'd)

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
DS606	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS607	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS608	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS609	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS610	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS611	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS612	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS613	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS614	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS615	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS616	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS617	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-
DS618	Pilot Light, Light Emitting Diode	H-P	HP5082-4494	PL-63	-

FUSE

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
F101	(117V) Fuse, 1/2A, 250V, Slo-Blo 3AG	BUSS	MDL-1/2A	FU-4	1
	(250V) Fuse, 1/4A, 250V, Slo Blo 3AG	LITFU	313-250	FU-17	1

CONNECTORS

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
J101	Card Edge	3M	3415-0000	CS-294-2	3
J102	Card Edge	3M	3415-0000	CS-294-2	-
J103	Card Edge	3M	3415-0000	CS-294-2	-
J104	Connector, 2-pin, Female.	MOLEX	2139-2	CS-275	1
J105	Receptacle, 3-pin, Female	MOLEX	2139-3	CS-287-3	2
J106	Receptacle, 3-pin, Female	MOLEX	2139-3	CS-287-3	-
J107	Housing, Mini PV, 10-pin.	BERG	65039-C	CS-310	1
J601	Receptacle, 10-pin.	BERG	20052	CS-237	2
J602	Receptacle, 10-pin.	BERG	20052	CS-237	-
P101	Not Used.	..	..	..	-
P102	Not Used.	..	..	..	-
P103	Not Used.	..	..	..	-
P104	Receptacle, 2-pin	MOLEX	A-2391-2A	CS-288-2	1
P105	Receptacle, 3-pin	MOLEX	A-2391-3A	CS-288-3	1
P106	Receptacle, 4-pin	MOLEX	A-2391-4A	CS-288-4	1
P107	Male Pin.	KI	..	24249A	-
P108	Male Pin.	KI	..	24249A	-

CONNECTORS (Cont'd)

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
P109	Male Pin.	KI	..	24249A	-
P110	Receptacle, 26-pin, "SCANNER" . . .	KI	Modified CS-295-1	26744A	-
P111	Receptacle, 3-pin, "LINE POWER" . .	S-C	EAC 301	CS-254	1
P112	Connector, 37-pin, Female	CAN	DC-37P	CS-302	1
P113	Male Pin.	KI	..	24249A	-

TRANSISTORS

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
Q101	PNP Transistor, TO-3 Case	MOT	2N5875	TG-114	1

RESISTORS

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
R101	33 Ω, 10%, 1/4W, Comp	A-B	CB-330-10%	R-76-33	3
R102	47 KΩ, 10%, 1/4W, Comp	A-B	CB-473-10%	R-76-47K	1
R103	10 KΩ, 10%, 1/4W, Comp	A-B	CB-103-10%	R-76-10K	9
R104	33 Ω, 10%, 1/4W, Comp	A-B	CB-330-10%	R-76-33	-
R105	33 Ω, 10%, 1/4W, Comp	A-B	CB-330-10%	R-76-33	-
R106	470 Ω, 10%, 1/4W, Comp	A-B	CB-471-10%	R-76-470	7
R107	470 Ω, 10%, 1/4W, Comp	A-B	CB-471-10%	R-76-470	-
R108	470 Ω, 10%, 1/4W, Comp	A-B	CB-471-10%	R-76-470	-
R109	470 Ω, 10%, 1/4W, Comp	A-B	CB-471-10%	R-76-470	-
R110	10 KΩ, 10%, 1/4W, Comp	A-B	CB-103-10%	R-76-10K	-
R111	470 Ω, 10%, 1/4W, Comp	A-B	CB-471-10%	R-76-470	-
R112	470 Ω, 10%, 1/4W, Comp	A-B	CB-471-10%	R-76-470	-
R113	470 Ω, 10%, 1/4W, Comp	A-B	CB-471-10%	R-76-470	-
R114	270 Ω, 10%, 1/4W, Comp	A-B	CB-271-10%	R-76-270	1
R115	10 KΩ, 10%, 1/4W, Comp	A-B	CB-103-10%	R-76-10K	-
R116	10 KΩ, 10%, 1/4W, Comp	A-B	CB-103-10%	R-76-10K	-
R117	10 KΩ, 10%, 1/4W, Comp	A-B	CB-103-10%	R-76-10K	-
R118	10 KΩ, 10%, 1/4W, Comp	A-B	CB-103-10%	R-76-10K	-
R119	10 KΩ, 10%, 1/4W, Comp	A-B	CB-103-10%	R-76-10K	-
R120	10 KΩ, 10%, 1/4W, Comp	A-B	CB-103-10%	R-76-10K	-
R121	10 KΩ, 10%, 1/4W, Comp	A-B	CB-103-10%	R-76-10K	-
R601	180 Ω, 10%, 1/4W, Comp	A-B	CB-181-10%	R-76-180	18
R602	180 Ω, 10%, 1/4W, Comp	A-B	CB-181-10%	R-76-180	-

RESISTORS (Cont'd)

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
R603	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R604	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R605	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R606	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R607	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R608	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R609	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R610	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R611	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R612	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R613	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R614	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R615	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R616	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R617	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-
R618	180 Ω, 10%, 1/4W, Comp.	A-B	CB-181-10%	R-76-180	-

SWITCHES

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
S101	Toggle Switch, "POWER"	ALCO	MSTZ05N	SW-271	1
S102	Slide Switch, "LINE SETTING". . . .	S-C	11D-1139	SW-273	1
S103	Slide Switch DPDT, "CU1/CU2". . . .	C-W	GG-350-PC-DPDT	SW-385	1

TRANSFORMER

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
T101	Power Transformer, Center-Tapped Secondary	KI	...	TR-162	1

INTEGRATED CIRCUITS

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
U101	Hex Inverters TTL, 14-Pin DIP . . .	TEXAS	SN7404N	IC-33	6
U102	Hex Inverters TTL, 14-Pin DIP . . .	TEXAS	SN7404N	IC-33	-
U103	Positive NOR Gates, 14-Pin DIP. . .	TEXAS	SN7402N	IC-32	5
U104	Positive NOR Gates, 14-Pin DIP. . .	TEXAS	SN7402N	IC-32	-
U105	Hex Inverters TTL, 14-Pin DIP . . .	TEXAS	SN7404N	IC-33	-

INTEGRATED CIRCUITS (Cont'd)

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
U106	Hex Inverters TTL, 14-Pin DIP . . .	TEXAS	SN7404N	IC-33	-
U107	Positive NAND Gates, Quad 2-Input, 14-Pin DIP.	TEXAS	SN7400N	IC-38	2
U108	Quad NAND Gate, 14-Pin DIP.	MOT	MC858P	IC-52	6
U109	Parallel-Load 8-Bit Shift Register, 16-Pin DIP.	SIG	N74165	IC-123	1
U110	8-Bit Parallel Out, Serial Shift Registers, 14-Pin DIP	TEXAS	SN74164J	IC-119	1
U111	Quad NAND Gate, 14-Pin DIP.	MOT	MC858P	IC-52	-
U112	Quad NAND Gate, 14-Pin DIP.	MOT	MC858P	IC-52	-
U113	Hex Inverters TTL, 14-Pin DIP . . .	TEXAS	SN7404N	IC-33	-
U114	Dual NAND Schmitt Trigger, 14-Pin DIP	SIG	N7413A	IC-121	1
U115	Quad NAND Gate, 14-Pin DIP.	MOT	MC858P	IC-52	-
U116	Quad NAND Gate, 14-Pin DIP.	MOT	MC858P	IC-52	-
U117	Quad NAND Gate, 14-Pin DIP.	MOT	MC858P	IC-52	-
U118	Positive NOR Gates, 14-Pin DIP. . .	TEXAS	SN7402N	IC-32	-
U119	Monostable Multivibrator, 14-Pin DIP	TEXAS	SN74121N	IC-118	3
U120	Bistable Latches, 16-Pin DIP. . . .	TEXAS	SN7475N	IC-36	2
U121	Positive NAND Gates, Quad 2-Input, 14-Pin DIP.	TEXAS	SN7400N	IC-38	-
U122	Positive NOR Gates, 14-Pin DIP. . .	TEXAS	SN7402N	IC-32	-
U123	Positive NOR Gates, 14-Pin DIP. . .	TEXAS	SN7402N	IC-32	-
U124	Bistable Latches, 16-Pin DIP. . . .	TEXAS	SN7475N	IC-36	-
U125	BCD/Decimal decoder, 16-Pin DIP . .	TEXAS	SN7442	IC-51	2
U126	Quad, 2-Input OR, 14-Pin DIP. . . .	SIG	N7432A	IC-115	2
U127	Quad, 2-Input OR, 14-Pin DIP. . . .	SIG	N7432A	IC-115	-
U128	Decode Counters, 14-Pin DIP	TEXAS	SN7490N	IC-37	1
U129	BCD/Decimal decoder, 16-Pin DIP . .	TEXAS	SN7442	IC-51	-
U130	Hex Inverters TTL, 14-Pin DIP . . .	TEXAS	SN7404N	IC-33	-
U131	Monostable Multivibrator, 14-Pin DIP	TEXAS	SN74121N	IC-118	-
U132	Monostable Multivibrator, 14-Pin DIP	TEXAS	SN74121N	IC-118	-

VOLTAGE REGULATOR

Circuit Desig.	Description	Mfr. Code	Mfr. Desig.	Keithley Part No.	Qty.
VR101	5 volt Regulator, TO-3 Case	NAT	LM309K	IC-98	1

End of Section 7

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COMPONENTS LOCATED ON PC-395

Circuit Desig.	Location Code
C101	H-4
C102	K-2
C103	J-1
C104	K-3
C105	C-2
C106	C-2
C107	C-3
C108	C-3
C109	E-4
C110	G-3
C111	B-2
C112	F-8
C113	F-8
C114	B-3
C115	D-7
C116	C-1
C117	E-6
C118	F-6
C119	D-7
C120	E-7
C121	G-3
CR101	J-4
CR102	J-4
CR103	A-2
CR104	G-8
CR105	G-8
P104	L-8
P105	K-8
P106	K-1
P107	H-8
P108	G-5
P109	G-6
P110	D-8
P111	*
P112	*
P113	H-8
R101	K-1
R102	B-2
R103	A-3
R104	F-8
R105	F-8
R106	H-3
R107	H-3
R108	H-3
R109	H-3
R110	F-3
R111	H-3
R112	H-3
R113	H-3
R114	H-3
R115	G-4
R116	F-4
R117	G-6
R118	F-6
R119	A-6
R120	C-8
S103	F-8
T101	L-7
U101	B-6
U102	G-7
U103	F-8
U104	B-5
U105	C-5
U106	F-3
U107	B-5
U108	F-6
U109	G-3
U110	E-5
U111	F-3
U112	G-5
U113	B-2
U114	B-3
U115	G-6
U116	F-5
U117	B-6
U118	D-8
U119	C-3
U120	E-6
U121	C-6
U122	D-5
U123	D-6
U124	B-2
U125	B-8
U126	B-8
U127	C-8
U128	D-3
U129	D-3
U130	D-2
U131	E-8
U132	D-2
VR101	K-4

*Part is located elsewhere on the chassis

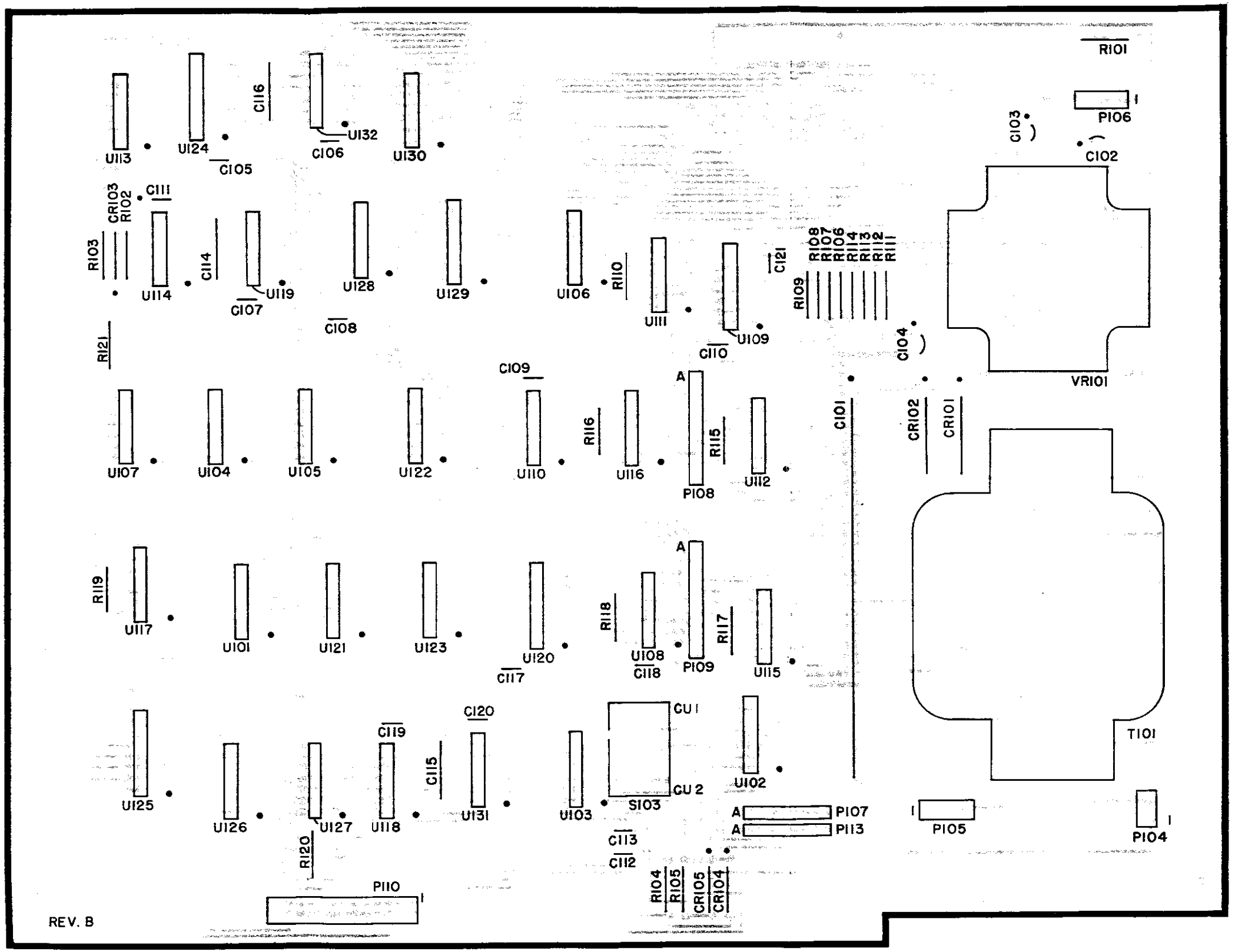

FIGURE 31. Component Layout For PC-395.

27007E

NOTES:
1. ALL RESISTOR VALUES ARE IN OHMS UNLESS MARKED OTHERWISE. (K-KILOHMS, M-MEGOHMS)
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. ○ DENOTES FRONT PANEL CONTROL.
4. ● DENOTES REAR PANEL CONTROL.
5. ◑ DENOTES INTERNAL CONTROL.
6. ⏚ DENOTES EARTH GROUND.
7. ⏦ DENOTES POWER SUPPLY "LO".

LTR	ECO NO.	REVISION	DATE
A	4478	RELEASED	9-17-74
B	4995	ADDED JUMPER TO TRANS.	9-23-75
C	5039	ADDED C121 & R121	10-31-75

HIGHEST SCHEMATIC DESIGNATIONS USED		
△C121	P113	U132
CR105	Q101	VR101
DS618	△R121	
J107	R618	
J602	S103	

SCHEMATIC DESIGNATIONS NOT USED
P101
P102
P103

MODEL 7819-DCC (OPTIONAL)

PC-383

INPUT

OUTPUT

SLOT 3 ADR.

SLOT 2 ADR.

SLOT 1 ADR.

SCAN ADR.

780		
MODEL	NEXT ASSEMBLY	QTY.
USED ON		

DO NOT SCALE THIS DRAWING

KEITHLEY INSTRUMENTS CLEVELAND, OHIO

DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED: XX = ± .015, ANG. = ±1°, XXX = ± .005, FRAC. = ±1/64, SURFACE MAX. 63

DATE 10-15-74 DRN R.S. MATERIAL FINISH

SCALE

TITLE SCHEMATIC, 780 CONTROL UNIT (PC-383 & PC-395)

NO. 27007E

KEITHLEY

Keithley Instruments Division / Keithley Instruments, Inc.
28775 Aurora Road / Cleveland, Ohio 44139 / U.S.A. / (216) 248-0400 / Telex: 98-5469 / Telefax: 248-6168

WEST GERMANY: Keithley Instruments GmbH / Heiglhofstr. 5 / München 70 / 089-71002-0 / Telex: 52-12160 / Telefax: 089-7100259
GREAT BRITAIN: Keithley Instruments, Ltd. / 1 Boulton Road / Reading, Berkshire RG 2 ONL / 0734-861287 / Telex: 847 047 / Telefax: 0734-863665
FRANCE: Keithley Instruments SARL / 3 Allée des Garays / B.P. 60 / 91124 Palaiseau/Z.I. / 1-6-0115 155 / Telex: 600 933 / Telefax: 1-6-0117726
NETHERLANDS: Keithley Instruments BV / Avelingen West 49/4202 MS Gorinchem/P.O. Box 559/4200 AN Gorinchem/01830-35333/Telex: 24 684 / Telefax: 01830-30821
SWITZERLAND: Keithley Instruments SA / Kriesbachstr. 4 / 8600 Dübendorf / 01-821-9444 / Telex: 828 472 / Telefax: 0222-315366
AUSTRIA: Keithley Instruments GesmbH / Rosenhügelstrasse 12 / A-1120 Vienna / (0222) 84 65 48 / Telex: 131677 / Telefax: (0222) 84 35 97
ITALY: Keithley Instruments SRL / Viale S. Gimignano 4/A / 20146 Milano / 02-4120360 or 02-4156540 / Telefax: 02-4121249