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New Challenges In WLR Testing

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Industry Cycles in Reliability Testing

Activities to solve semiconductor reliability problems follow a somewhat predictable cycle, just as Moore's law drives the geometric shrink. As an example, with the adaptation of the VLSI generation of technology, aluminum interconnects were introduced to keep the speed of the circuit on track. Reliability problems such as electromigration were quickly identified. Once the problems were identified, the degradation mechanism had to be modeled through experimental efforts. With the models in place, process engineering efforts took place to optimize the reliability of the new technology. As the technology matured, the focus shifted to defect reduction. With the introduction of ULSI technology, the cycle was again repeated with new materials, such as strained silicon; copper, and low-κ interconnect dielectrics.

As the number of material compounds being introduced continues to increase, reliability related challenges continue to accelerate. These new challenges mean that reliability testing is being taxed beyond current measurement hardware capabilities. Engineers and researchers involved with reliability and quality assurance are encountering a widening capability gap between the existing instruments and unmet testing needs.

This situation calls for increased collaboration between test instrument vendors and their leading edge reliability customers.

Reliability Test Trends

Today we are seeing the introduction of new gate dielectrics to address the increasing leakages associated with ultra thin gates. With the introduction of unconventional dielectric materials, such as Hafnium oxides, the degradation mechanism known as Bias Temperature Instability (BTI) has become every more problematic. The new materials generally reduce gate leakage, which leads to lower quiescent operating currents, however it also results in threshold and baseband voltage instability.

In addition to BTI, the new generation of gate stacks (high-k-metal gates specifically) display time dependent dielectric breakdown (TDDB) characteristics that are distinctly different from conventional SiO2. Earlier models for hard and soft breakdown were well understood, but the new materials display "progressive breakdown". There is currently a major effort underway to understand the fine details of the physics behind this failure mechanism, and a growing sense of urgency as the materials move into the engineering phase where process compatibility is being optimized. These subtleties require a new class of instrumentation that not only possesses better measurement capabilities, but also substantial processing power to accommodate innovative test sequences.

Many degradation mechanisms are the

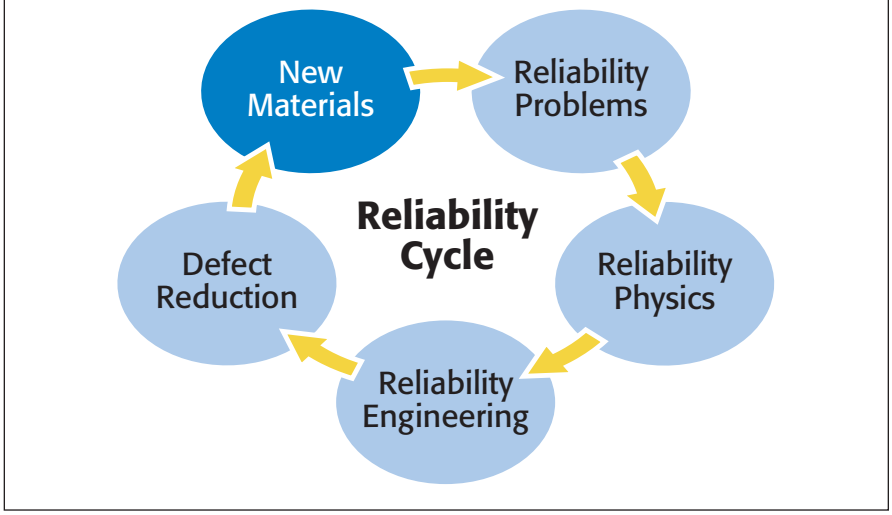

Figure 1. Semiconductor defect-reduction / reliability-improvement cycle.

result of trapped charge. Consequently, the magnitude of parameter degradation needs to be measured relative to trapping and de-trapping rates of the device. Measurements must be made very quickly after the electrical stress condition is removed, AND the stress condition needs to be restored as quickly as possible after the measurement. Much of the older test equipment falls short of these needs.

Additionally, it is clear that various transistor performance enhancement technologies result in complex interaction with respect to device and circuit reliability. For instance, strain silicon processes that enhance channel mobility have been shown to exacerbate BTI. Furthermore, instability in threshold voltage results in elevated off-currents and subsequent higher junction temperatures. High junction temperatures accelerate dielectric leakage and breakdown. These high order interactions are difficult to model and make failures more random. Developing reliable models requires test instruments that can capture a statistically significant number of samples with fast test sequences.

Large data sets are particularly important in modeling the interaction between transistors within a circuit, which is even more complex than the mechanisms that operate within individual transistors. For example, P-MOS and N-MOS transistors do not degrade the same way. N-MOS devices are more prone to BTI. As a consequence, a circuit with complementary transistors transporting a clock signal may cause a change in duty cycle or signal skewing. Additionally, complex interactions can occur between different degradation mechanisms. For example, soft dielectric breakdown usually results in increased leakage. Although this does not render the transistor useless, it can possibly accelerate BTI. Because of these issues, capturing statistically significant sample sizes may mean collecting data points of 40,000 or more.

Implications for Older Test Equipment Generations

These new challenges mean that reliability testing is being taxed beyond current measurement hardware capabilities. Mechanisms such as BTI and progressive breakdown need to be measured quickly and accurately. The old method of multiplexing between structures generally is not fast enough. To achieve statistically meaningful sample sizes, and meet critical timing requirements, it is often necessary to dedicate source and measurement hardware to each structure.

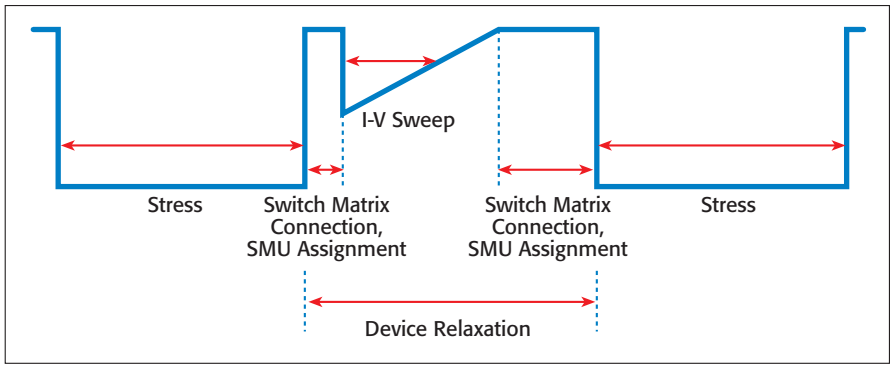

Figure 2. Multiplexed SMUs may not properly control device relaxation time.

Using typical traditional measurement systems for reliability testing raises the following issues:

Low-cost per channel systems generally rely on switching to reduce the number of SMUs needed; this means stress-measure transitions are slow. Multiplexing also makes it impossible to continuously monitor each test structure. This also means that truly parallel testing is impossible.

Poor timing and latencies often make it impossible to capture important transient events, and also results in poorly controlled relaxation times.

The instruments' on-board processors have limited programmability or decision making capacity. This also means that potentially valuable processes, such as data thinning, are impossible.

Many traditional systems have a buffer size of about 5000; this is too small for most reliability testing needs, such as capturing an entire high-K-metal gate failure.

The software architecture of a traditional test system is illustrated in ***Figure 3***. Typically, the central controller is a PC running the SMU control libraries. These libraries contain test routines for all SMU-related activity, including decision making.

One major short coming of this architecture is that the central controller has to take care of each step in the test routine. As an example, consider the standard isothermal electromigration test, where current is dynamically adjusted to keep a constant temperature across the test structure. The SMU sources a current and measures resistance. Then it

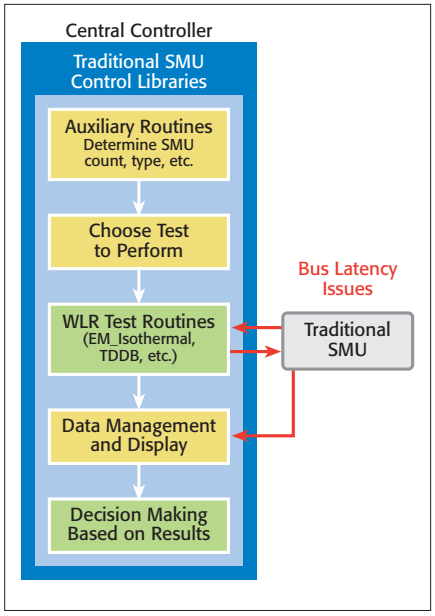

Figure 3. Software Architecture of a Traditional Test System

reports the resistance value over the GPIB bus to the central controller. The controller calculates the temperature, and then decides which current to source next. The next instruction with a new current source value is sent to the SMU, again over the GPIB bus. This process is repeated – perhaps for hundreds or thousands of data points. This situation applies for all routines in general, and for many the bus latency is a serious issue.

New Generation Test Equipment

Today there is a new test system architecture based on "Smart" SMUs that provide higher throughput, better measurement integrity, greater flexibility, and overall significantly more information processing and decision making capacity. This is made possible by embedding a full 32-bit Test Script Processor (TSP™) that runs a full-featured programming language on the instrument.

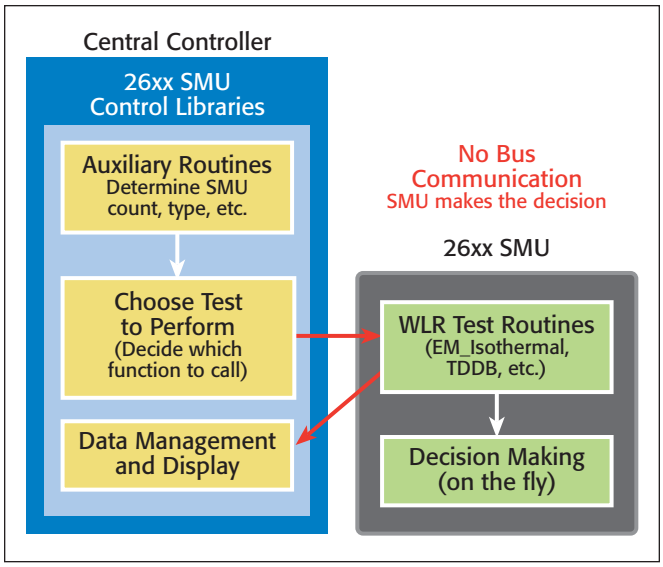

Figure 4. New Software architecture based on the "Smart SMU" concept.

This new class of Smart SMUs are embodied in the Keithley 2600 Series of SourceMeter® Instruments.

Because of the PC-like computing capabilities, 2600 Series SourceMeters bring about a software architecture shift in test systems (***Figure 4***). Note that the responsibility of controlling test routines along with all decision making is now shifted to the instrument while the central controller (PC) retains the responsibility of making function calls to the embedded scripts and data management.

Custom test routines with complex decision can resides inside the instrument. The SMU no longer needs to communicate data back to a PC controller program (over the GPIB), and then wait for the decision and next instruction. In short, bus latency is no longer an issue – tests can be executed much faster in a more autonomous manner.

The instrument's TSP scripting language is based on a well known open source language engine, which incidentally has a significant following among video game developers. This scripting language is designed with the expressed goals of simplicity, efficiency, portability and low embedding cost. To the credit of the designers of this language, the result is a fast language engine with small footprint, making it ideal in embedded systems. It comes will all the necessary case constructs for complex decision making, along with other rich features – details of which are beyond the scope of this discussion.

Although test scripts can be written using any word processor, the 2600 Series SourceMeters come with a convenient script building tool – Test Script Builder. Once written, scripts can be stored inside the non-volatile buffers of the 2600. From a software migration standpoint, much of the user's test sequence will be implemented in the instrument. In most cases, one function call to the embedded test scripts, with a single GPIB write command, will start the entire test sequence.

Typically, the software configuration for a 2600-based system consists of two main parts (***Figure 5***):

1. A GUI residing on the PC for taking user inputs and displaying data.
2. Test Scripts residing on the master 2600 to sequence all test routines and decision making.

Note that, the primary responsibility any GUI based program on the PC is now limited to making appropriate function calls based on test parameters and test selection, plus data display and management.

To accommodate the increased processing capabilities, the 2600 Series also have significantly increased data storage capacity. This includes multiple non-volatile buffers that can store approximately fifty thousand measurement and timestamp data pairs for each SMU. Additionally, there can be multiple volatile buffers for each SMU. In fact, the user can create and specify the desired buffer size for volatile buffers. The buffer timestamps have one microsecond resolution, and timing accuracy of 50 parts per million.

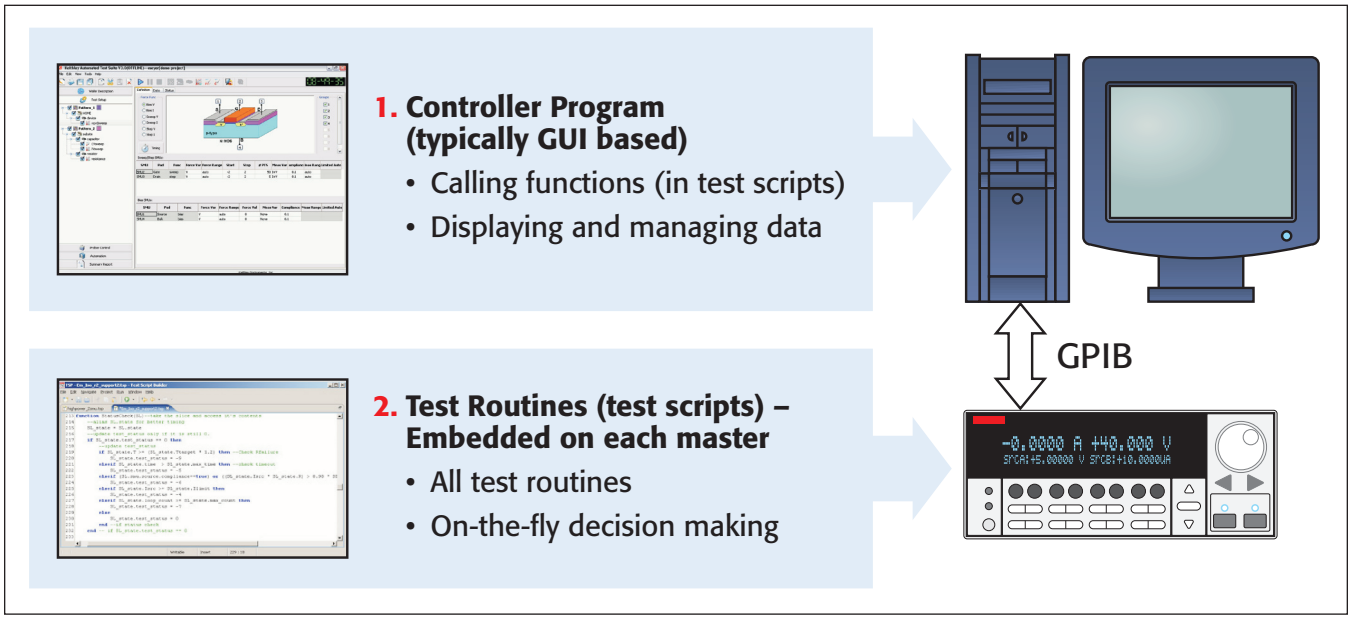

Figure 5. Two Part Software-Architecture with 2600 Series SourceMeters.

System Architecture and Parallel Testing

In order to take further advantage of increased processing capabilities, another unique feature introduced with the 2600 Series is the 'mainframe-less' expansion capability. This novel feature allows multiple SourceMeters to be tied together in a master-slave configuration using an inter-unit communication bus, TSP-Link™, by using standard Ethernet cable. By using this virtual configuration, all SMUs behave as if they are in one large mainframe system. The master occupies a GPIB address, and it can control up to 128 SMUs through the TSP-Link bus. The master unit runs the user written embedded scripts and acts as the decision maker for all the SMUs it controls.

This capability ushers in unprecedented flexibility in system architecture to fit specific testing needs. Depending on how intensive the test is, or how much parallel testing needs to be done, systems can be designed with the appropriate number of masters. ***Figure 6a*** shows a system with one master controlling 16 SMUs (two SMUs in each unit) and ***Figure 6b*** shows four masters each controlling four SMUs. One master controlling a group of SMUs is known as a "channel group".

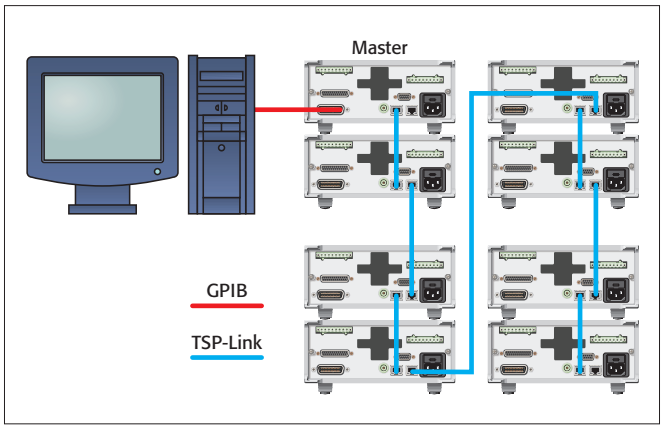

Figure 6a. Multi-channel test system with one master controlling 16 SMUs (2 SMUs per instrument).

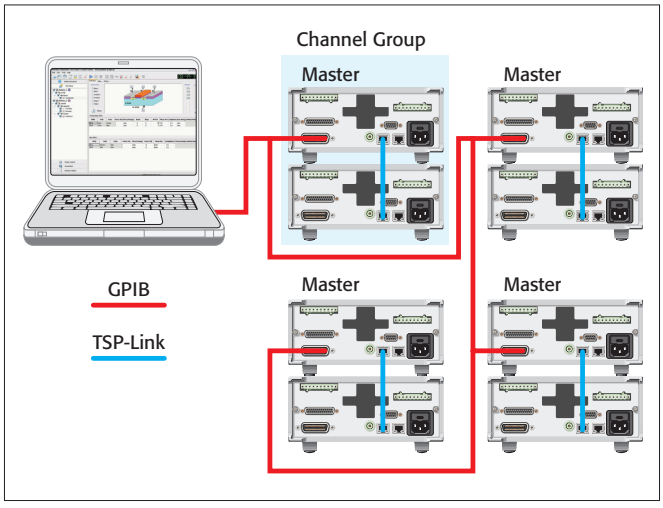

Figure 6b. Multi-channel test system with one master controlling 4 SMUs in a channel Group, and a total of 4 Channel Groups

Note that the only requirement for a 2600 to act as a master is to have it occupy a GPIB address.

The configuration in ***Figure 6b*** is ideal for testing a 4-terminal device where each terminal needs a SMU. Since each channel group has a master that controls all SMUs in the channel group, this is a convenient configuration for parallel testing. Typically, a library of test scripts are pre-loaded to all the masters and then the test can be run by making a single function call to the scripts with user entered parameters. All the GUI software needs to do is send the function call with user entered parameters by using a GPIB write. If more synchronization for parallel testing is desired, the PC can send a GPIB group trigger to all the masters, which intern can start running the test routines on SMUs within the group. For this arrangement to work, the only key feature needed in the GUI program is to have basic GPIB functions – GPIB Read, GPIB Write etc.

The arrangement in ***Figure 6b*** is also similar to a modern computer network in which processing power is distributed throughout the network. A single central processor with many "passive" terminals is a thing of the past. This is also the case with the 2600 Series base test systems, where responsibility for running the test functions and decision making are distributed to all masters.

Hardware Performance to Match New Processing Capabilities

The source-measure hardware engine of the Keithley Series 2600 is unequaled in its versatility. Its high speed allows the capture of transient behavior, and it can collect up to 10,000 readings per second, or up to 5,500 source-measure points per second.

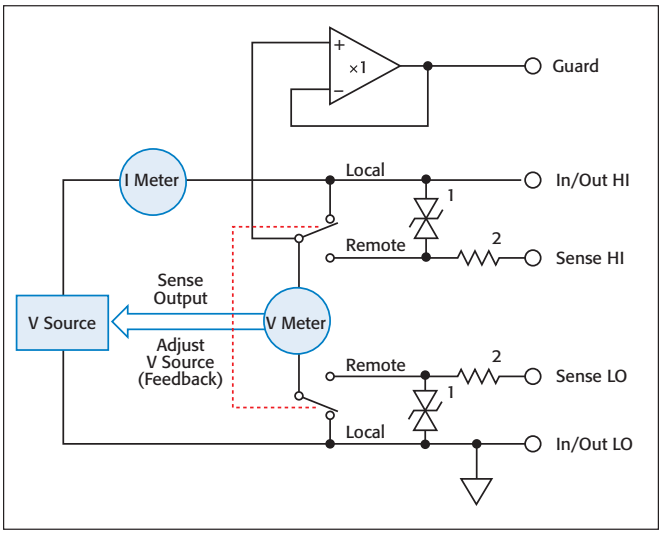

Figure 7. Force-Sense circuitry of the 2600 Series (source voltage configuration shown).

The force and sense circuitry (***Figure 7***) has Force (In/Out) Hi/Lo and Sense Hi/Lo terminals, which allow the use of Force Lo or Sense Lo for return current. Traditional SMUs usually need a separate Ground Unit for return current. Each Force Lo and Sense Lo of the 2600 Series is electrically isolated from chassis ground, so a single SMU can perform full 4-wire Kelvin measurements. This is a significant advantage in many test protocols, such as electromigration, because only one SMU is needed per sample structure. Since a common ground is unnecessary, testing multiple devices is no issue for 2600-based platforms.

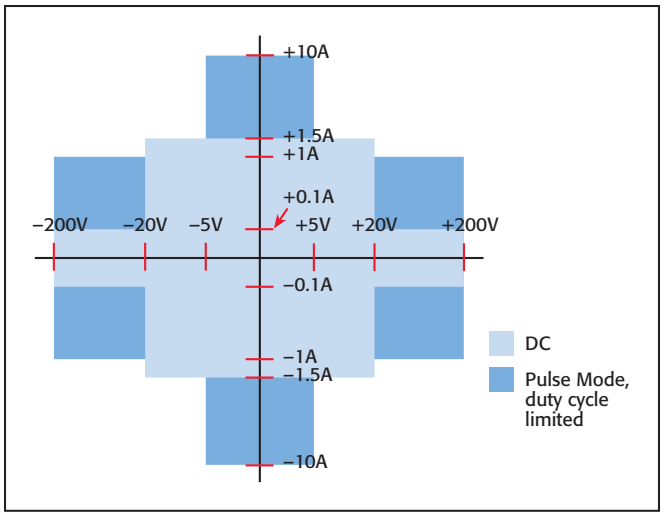

Figure 8. Four-quadrant operating parameters of Keithley Models 2611 and 2612.

All of the Series 2600 SMUs feature full 4-quadrant operation (***Figure 8***), making them suitable for a wide variety of applications where they can function as either a source or sink (load). Furthermore, each SMU has two A/D converters for simultaneous current and voltage measurements. This cuts down on latencies and increases test throughput. System size can be easily scaled, as shown in ***Figure 9.***

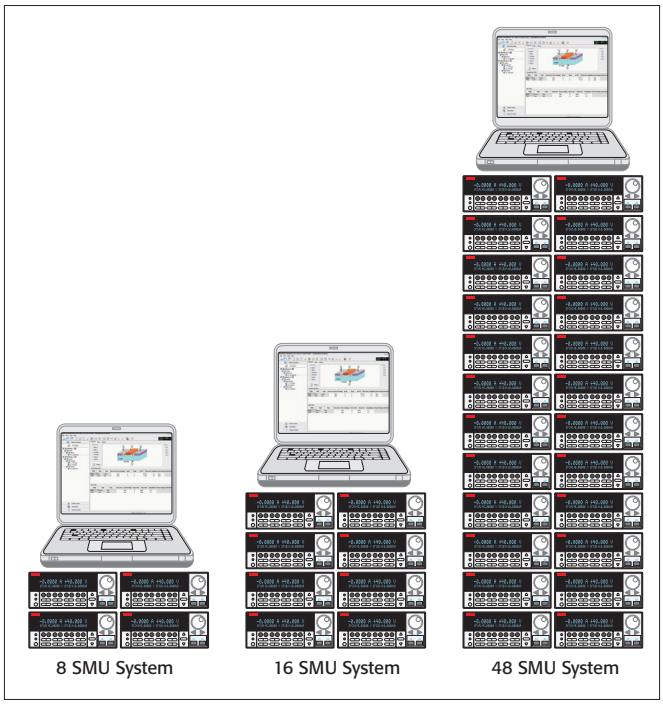

Figure 9. Creating scalable systems is easy, and up to 896 SMU channels are possible.

Taking Advantage of SMU Test Sequencing

In switching from individual source-measure instruments to SMUs, the most dramatic gain in throughput comes from a change in system programming. Instead of using PC-based control, the SMU's test sequencer and program memory are allowed to control the testing. This takes advantage of a wide range of SMU features and functions, such as four-quadrant operation, voltage and current sweeping, built-in waveform generation, deep program memory, picoamp sensitivity, 5½-digit resolution, measurement comparator for fast pass/fail testing, and digital I/O for control of other equipment.

All this functionality is taken to a new heights in the Keithley 2600 Series SMUs. Their embedded script programming increases flexibility, and the ability to perform tests autonomously has become extremely powerful. Users can do more with one instrument, and hardware/software integration tasks are greatly simplified. You can easily create cost-effective, scalable, high throughput solutions for precision DC, pulse, and low frequency AC source-measure testing.

Series 2600 instruments provide two to four times the test speed of competitive solutions in I-V reliability testing applications. They also offer higher source-measure channel density and a significantly lower cost of ownership. Analog-to-digital converters provide simultaneous I and V measurements in less than 100µs, and source-measure sweep speeds of less than 230µs per point. This high speed source-measure capability, plus embedded test scripts, allows throughput gains of up to 10X over equivalent PC-based programs operating via GPIB.

Conclusions

Semiconductor reliability testing is again at a point where emerging test needs are far beyond what older traditional test systems can offer. A paradigm shift in test system architecture is needed to successfully meet the new requirements. The Keithley 2600 Series represents the new generation of smart SMUs, with the architecture and features to provide high throughput, data integrity, and flexibility for easy expansion and repurposing, as required in semiconductor reliability test programs. KEITHLEY

About the Author

Joey Tun is Sr. Applications Engineer at Keithley Instruments in Cleveland, Ohio where he is responsible for SourceMeter® products. He has BSEE from Purdue University and has been involved in the test and measurement industry for over six years.

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