KEITHLEY

*Application Note Series*

Number 2535

# Monitoring Channel Hot Carrier (CHC) Degradation of MOSFET Devices using Keithley Model 4200-SCS

## Introduction

Channel Hot Carrier (CHC) induced degradation is an important reliability concern in modern ULSI circuits. Charge carriers gain kinetic energy as they are accelerated by the large electric field across the channel of a MOSFET. While most carriers reach the drain, hot carriers (those with very high kinetic energy) can generate electron-hole pairs near the drain due to impact ionization from atomic-level collisions. Others can be injected into the gate channel interface, breaking Si-H bonds and increasing interface trap density. The effect of CHC is time dependant degradation of device parameters, such as $V_T$, $I_{DLIN}$, and $I_{DSAT}$.

This channel hot carrier induced degradation (also called HCI or hot carrier injection) can be seen on both NMOS and PMOS devices and will affect device parameters in all regions, such as $V_T$, sub-threshold slope, Id-on, Id-off, Ig, etc. The rate of degradation of each parameter over stress time depends on the device layout and process used.

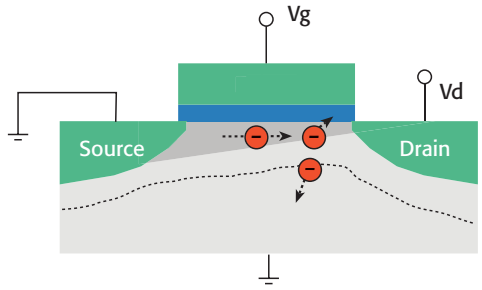



**Figure 1. Channel Hot Carrier degradation**

## Procedures for CHC Degradation Test

A typical Channel Hot Carrier test procedure consists of a pre-stress characterization of the device under test (DUT), followed by a stress and measurement loop [1] (***Figure 2***). In this loop, devices are stressed at voltages higher than normal operating voltages. Device parameters, including $I_{DLIN}$, $I_{DSAT}$, $V_T$, Gm, etc, are monitored between stresses and the degradation of those parameters is plotted as a function of accumulated stress time. Prior to conducting this stress and measurement loop, the same set of device parameters is measured to serve as baseline values.

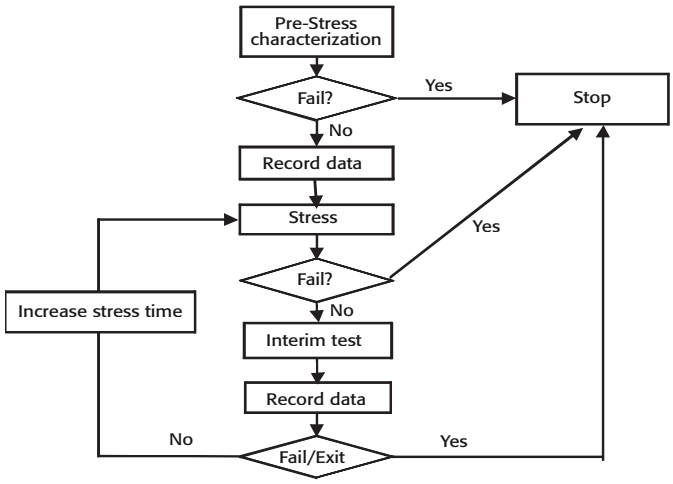



**Figure 2. Typical CHC test procedure**

Stress bias conditions are based on worst-case degradation bias conditions, which are different for NMOS and PMOS FETs. Typically, for drain voltage stress, it should be less than 90% of the source drain breakdown voltage. Then, at the drain stress voltage, the gate stress voltage is different depending on the type of transistor and gate length. ***Table 1*** shows worst-case degradation bias conditions for NMOS and PMOS FETs created using different technologies [2].

| Technology | L >= 0.35um | L < 0.25um |
|---|---|---|
| N-MOSFET | Vg (max Isub) | Vg (max Isub) or Vg = Vd |
| P-MOSFET | Vg (max Ig) | Vg = Vd |

**Table 1. Worst-case stress bias conditions for NMOS and PMOS FETs**

The worst-case stress bias conditions can be easily determined using interactive test modules (ITMs) on the Model 4200-SCS Semiconductor Characterization System.

## Device connections

It's easy to perform a CHC test on a single transistor. However, each CHC test typically takes a long time to complete, so it's desirable to have many DUTs stressed in parallel, then characterized sequentially between stresses to save time. To accomplish this, a switch matrix is needed to handle the parallel stresses and sequential measurements between stresses. ***Figure 3*** shows an example of a hardware configuration for a typical CHC test for multiple DUTs. The Model 4200-SCS provides the stress voltages and measurement capability, while the switch matrix enables parallel stress and sequential measurements of multiple devices.

Depending on the number of devices under test, it's possible to use either the Model 708A mainframe, which accommodates one switch matrix card (12 device pins), or a Model 707A mainframe, with up to six matrix cards (72 pins maximum). The total number of different gate and drain stress biases is limited by the number of SMUs in the system. ***Figure 4*** illustrates a connection diagram using eight SMUs (for total of eight different drain and gate stress biases) plus a ground unit (for ground terminal) to stress 20 transistors in parallel.

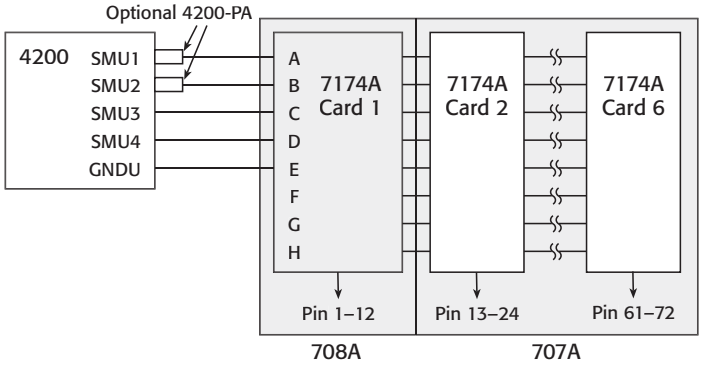



**Figure 3. Hardware configuration example**

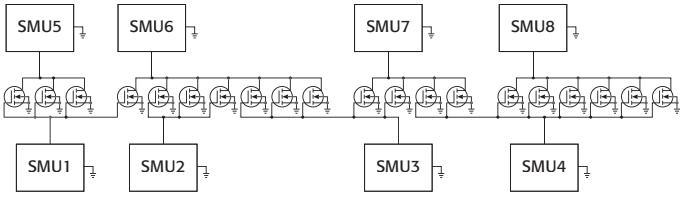



**Figure 4. Example of using eight SMUs to stress 20 devices in parallel. A separate ground unit (GNDU) is used for common terminals.**

## Determining device parameters

Hot carrier parameters monitored include $V_{TH}$, GM, $I_{DLIN}$ and $I_{DSAT}$. These parameters are initially measured before stress and re-measured at each cumulative stress time. The $I_{DLIN}$ is the measured drain current with the device biased in the linear region, while $I_{DSAT}$ is the measured drain current with the device biased in the saturation region. $V_{TH}$ and GM can be determined using either constant current or extrapolation methods. In the extrapolation method, the $V_{TH}$ is determined from the maximum slope of the $I_{DS}$ vs. $V_{GS}$ curve.

The Model 4200-SCS's Formulator Tool greatly simplifies extracting these parameters. Built-in functions include *Differentiate* to obtain GM, a *MAX* function to obtain the maximum GM (Gmext), and a least squares line-fit function to extract $V_{TH}$ (Vtext). The formulas to calculate these parameters can be found in the HCI projects supplied with the Model 4200-SCS, and corresponding tests in test libraries. Some examples of these formulas include:

GM = DIFF(DRAINI,GATEV)

GMEXT = MAX(GM)

VTEXT = TANFITXINT(GATEV, DRAINI, MAXPOS(GM))

The last equation (VTEXT) is the x intercept of tangent fit of the $I_D$-$V_G$ curve at the maximum GM point. ***Figure 5*** illustrates the Formulator Tool interface.

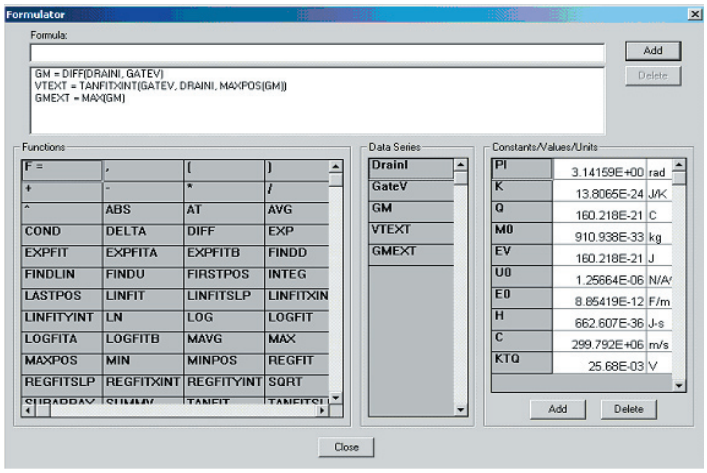



**Figure 5. Model 4200-SCS's Formulator Tool interface**

Once those parameters are calculated from individual tests, they can be exported by checking the check box in "Output Value" option for monitoring the degradation over stress time. For each test, an exit on compliance option can be selected, allowing the system either to skip the device or stop the overall CHC test in case of a device failure. For more details on these options, refer to the complete 4200-SCS Reference Manual.

## Setting up stress conditions

One of the operating features enhanced in version 5.0 of the Keithley Test Environment Interactive (KTEI) software for the Model 4200-SCS software is a stress cycle within the project tree structure with both voltage and current stress capabilities. Users can take advantage of the stress cycle to set up DC stresses on DUTs for preset durations. The duration of the stress for each cycle can be set up in either a linear or a logarithmic way (see ***Figure 6***). This feature is used in CHC/HCI, NBTI, EM (electromigration) and charge trapping applications to provide a constant DC stress (voltage or current). In stress/measure mode, the user can set up stress conditions for each terminal of the device under test (***Figure 7***). After each stress cycle, the Model 4200-SCS goes through a measurement sequence, which can include any number and type of user-defined tests and parameter extractions. The degradation of those parameters over time is plotted in the stress graph. The Model 4200-SCS's "toolkit" architecture offers users tremendous flexibility in creating test sequences and stress-measure projects.

For critical parameters, a target degradation value can be set (see ***Figure 7***). Once the degradation of that parameter exceeds the target, that specific test will stop. This saves significant time by eliminating unnecessary stress and measure cycles on failed devices.

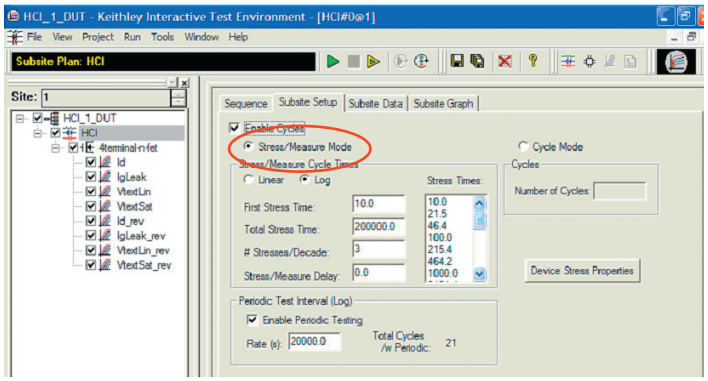



**Figure 6. Stress cycle set-up page.**

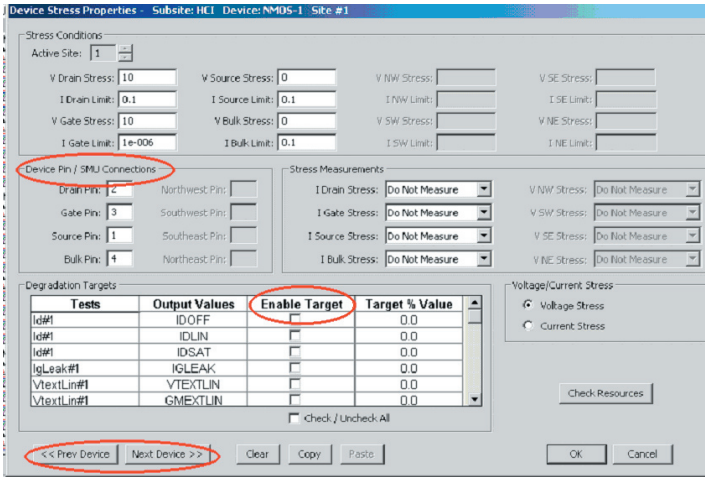
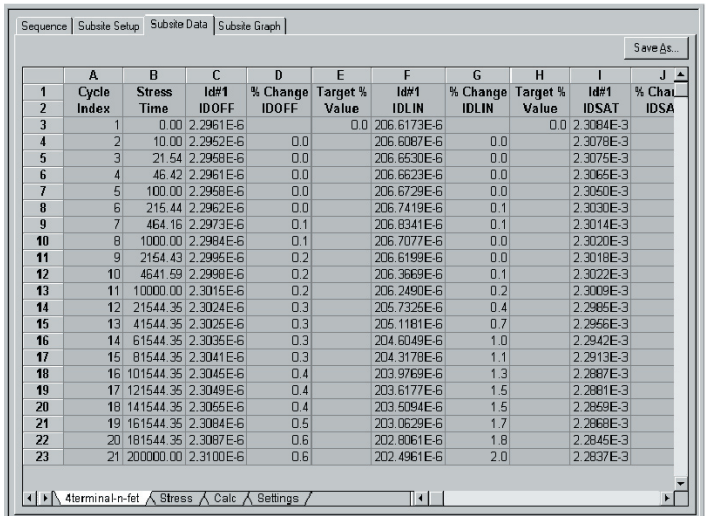



**Figure 7. Device stress/pin connection/degradation target value set-up window.**

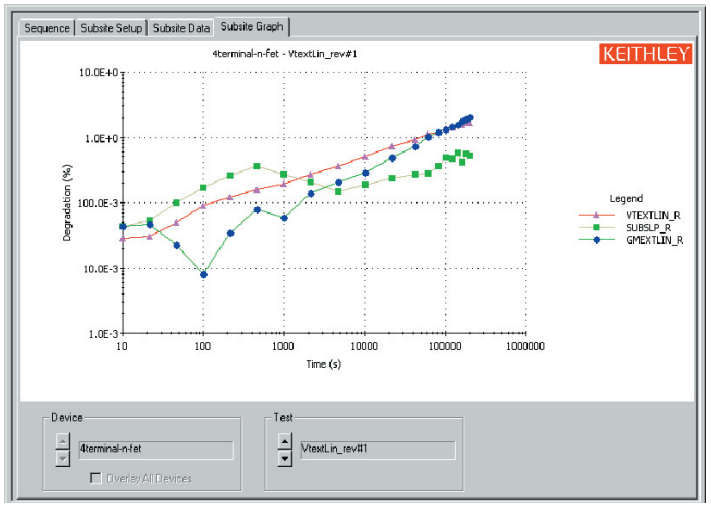
If multiple DUTs are defined in the project, it's possible to toggle between devices using the "previous device" and "next device" buttons in the device stress set-up window (***Figure 7***). The "copy" and "paste" buttons can be used to copy stress settings from one device to the other without the need to re-enter all the information in all the input fields. With multiple devices stressed in parallel in different stress configurations, it can be difficult to correlate the number of different stress biases required and the number of SMUs available to apply them. Pressing the "check resource" button makes it easy to determine if there are enough SMUs for all the stress biases involved, and see how the SMUs are assigned to each of the different stress biases. A ground unit is used by default if the switch matrix is attached to the system and if the stress bias on the terminal is 0V.

A separate data sheet (***Figure 8a***) is incorporated within the stress set-up window to save information about cycle index, stress time, and monitored parameters extracted from the measurement between stresses, such as $I_D$ and $V_T$. The data is saved automatically in Excel file format (.xls) in the project directory. It's possible to export the data to other locations as text or Excel files. If the system is in stress/measure mode, the degradation of the monitored parameters relative to pre-stress measurements is calculated automatically and can be plotted on the graph page (***Figure 8b***). For more information on the stress-measure capabilities provided in KTEI 5.0 software, consult the complete 4200-SCS Reference Manual.




| | A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Cycle | Stress | Id#1 | % Change | Target % | Id#1 | % Change | Target % | Id#1 | % Chai |
| 2 | Index | Time | IDOFF | IDOFF | Value | IDLIN | IDLIN | Value | IDSAT | IDSA |
| 3 | 1 | 0.00 | 2.2961E-6 | | 0.0 | 206.6173E-6 | | 0.0 | 2.3084E-3 | |
| 4 | 2 | 10.00 | 2.2952E-6 | 0.0 | | 206.6087E-6 | 0.0 | | 2.3078E-3 | |
| 5 | 3 | 21.54 | 2.2958E-6 | 0.0 | | 206.6530E-6 | 0.0 | | 2.3075E-3 | |
| 6 | 4 | 46.42 | 2.2961E-6 | 0.0 | | 206.6623E-6 | 0.0 | | 2.3065E-3 | |
| 7 | 5 | 100.00 | 2.2958E-6 | 0.0 | | 206.6729E-6 | 0.0 | | 2.3050E-3 | |
| 8 | 6 | 215.44 | 2.2962E-6 | 0.0 | | 206.7419E-6 | 0.1 | | 2.3030E-3 | |
| 9 | 7 | 464.16 | 2.2973E-6 | 0.1 | | 206.8341E-6 | 0.1 | | 2.3014E-3 | |
| 10 | 8 | 1000.00 | 2.2984E-6 | 0.1 | | 206.7077E-6 | 0.0 | | 2.3020E-3 | |
| 11 | 9 | 2154.43 | 2.2995E-6 | 0.2 | | 206.6199E-6 | 0.0 | | 2.3018E-3 | |
| 12 | 10 | 4641.59 | 2.2998E-6 | 0.2 | | 206.3669E-6 | 0.1 | | 2.3022E-3 | |
| 13 | 11 | 10000.00 | 2.3015E-6 | 0.2 | | 206.2490E-6 | 0.2 | | 2.3009E-3 | |
| 14 | 12 | 21544.35 | 2.3024E-6 | 0.3 | | 205.7325E-6 | 0.4 | | 2.2985E-3 | |
| 15 | 13 | 41544.35 | 2.3025E-6 | 0.3 | | 205.1181E-6 | 0.7 | | 2.2966E-3 | |
| 16 | 14 | 61544.35 | 2.3035E-6 | 0.3 | | 204.6049E-6 | 1.0 | | 2.2942E-3 | |
| 17 | 15 | 81544.35 | 2.3041E-6 | 0.3 | | 204.3178E-6 | 1.1 | | 2.2913E-3 | |
| 18 | 16 | 101544.35 | 2.3045E-6 | 0.4 | | 203.9769E-6 | 1.3 | | 2.2887E-3 | |
| 19 | 17 | 121544.35 | 2.3049E-6 | 0.4 | | 203.6177E-6 | 1.5 | | 2.2881E-3 | |
| 20 | 18 | 141544.35 | 2.3055E-6 | 0.4 | | 203.5094E-6 | 1.5 | | 2.2869E-3 | |
| 21 | 19 | 161544.35 | 2.3084E-6 | 0.5 | | 203.0629E-6 | 1.7 | | 2.2868E-3 | |
| 22 | 20 | 181544.35 | 2.3087E-6 | 0.6 | | 202.8061E-6 | 1.8 | | 2.2845E-3 | |
| 23 | 21 | 200000.00 | 2.3100E-6 | 0.6 | | 202.4961E-6 | 2.0 | | 2.2837E-3 | |

**a)**




**b)**

**Figure 8. a) Stress data sheet stores all stress information, including measurement results during stresses, and selected parameters measured between stresses. b) Plot of percentage degradation data as a function of stress time**

## Building a CHC project

The following steps outline a typical process for building a CHC project. For details on each step, consult the complete 4200-SCS Reference Manual.

1. Create the project structure
   a. Determine if switch matrix is available
   b. Determine if enough SMUs are available
   c. Build project structure
2. Build individual tests between stresses
   a. Make switch connection if switch matrix is used
   b. Build new test using interactive test modules (ITMs)

c. Calculate device parameters using the Formulator tool

d. Set up exit on compliance conditions

e. Export parameter values for degradation monitoring

f. Repeat steps b through e for monitoring more parameters

3. Repeat step 2 if there are multiple DUTs

4. Set up stress conditions in sub-site level

a. Set up stress time

b. Set up device stress conditions

i. Stress voltage

ii. Pin connections

iii. Target degradation values

iv. Go to next device

5. Run project and examine degradation data

Parameter degradation data and raw measurement data are saved automatically in Excel file format during the run time of the project. Therefore, even if the project is stopped before completion, the measured data has already been captured. The raw I-V curves between stresses can be overlaid on stress cycles, so it's easy to visualize how the I-V degrades as a function of stress time. ***Figure 9*** shows Vgs-Id curves from overlaying 21 stress cycles.

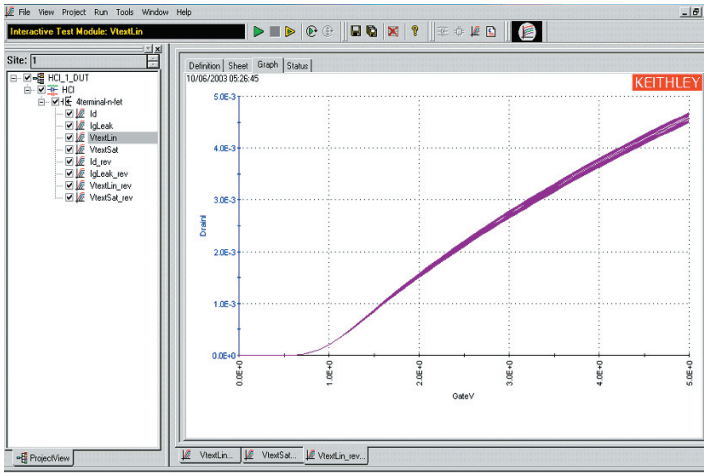



**Figure 9. Plot of overlaid data from multiple stresses.**

***Figure 10*** is an example of a CHC project that tests five sites on a wafer. The Model 4200-SCS controls prober movement from site to site through built-in drivers that are compatible with most common semi-automatic probe stations on the market.

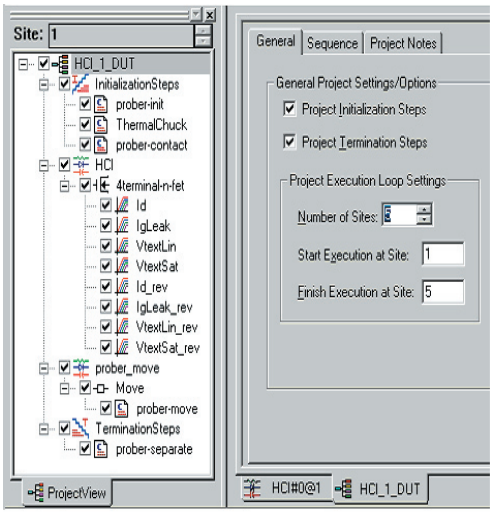



**Figure 10. Example of a wafer level CHC test.**

## Conclusion

The enhanced stress-measure loop in KTEI5.0 software allows setting up a CHC test without the need for any programming. Together with the interactive test interface, Formulator Tool, and powerful graphing capabilities, KTEI 5.0 software makes the Model 4200-SCS an ideal tool for evaluating device reliability parameters such as CHC induced degradation of MOSFETs, as well as its better-known role in device characterization.

## References

[1] JEDEC Standard 28-A, "Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress," 2001.

[2] Vijay Reddy, "An introduction to CMOS semiconductor Reliability," IRPS Tutorial, 2004.



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