

**Technology and Economics Drive Testing Needs**

# Short Pulse Testing Mandatory for Semiconductor Reliability

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*Developing ICs that work is one thing; developing them to last is another. The latter is getting more difficult as new technologies present new reliability problems. Pulse testing on the wafer, before packaging, can help.*

**Test Methods Must Change**

In advanced IC technologies, traditional DC testing may not uncover reliability problems caused or exacerbated by new materials and failure mechanisms. Shrinking geometries, new materials, and more complex designs are having a tremendous impact on device lifetimes due to increased fragility, higher power density, and new failure mechanisms. This is especially true for nanoscale gate dielectrics using new high- $\kappa$  materials. Processes that once produced devices with 100-year lifetimes may now yield only 10-year lifetimes – uncomfortably close to expected system lifetimes. Therefore, reliability must be designed in from the start, tested thoroughly, and constantly monitored in production.

In many cases, the way HCI (hot carrier injection), NBTI (negative bias temperature instability), and TDDDB (time dependent dielectric breakdown) tests are performed in stress-measure cycling needs to expand be-

yond current implementations. The practice of repetitive DC cycling with instruments that use a switch matrix can allow charge trapping relaxation that may not represent actual use conditions, and may mask high speed effects that would be typical in actual use conditions. Today, ultra-short pulse testing is needed to reveal these subtle interfacial charge trapping problems that won't show up in DC testing.

Accelerated testing such as HCI and NBTI can quickly generate curves that are extrapolated to predict operating lifetime and thereby provide insight into device design and manufacturing processes. The most efficient method is to over-stress the device, measure degradation trends of key operating parameters, and extrapolate the data to the full lifetime (*Figure 1*).

However, it doesn't help if the extrapolation isn't representative of the way a device is going to be used. For example, NBTI degradation can relax when gate voltage stress is turned off. Then drain current and threshold voltage may recover and change back toward their original values – a scenario that may not match real-life usage. If stress is resumed after recovery, degradation will follow the previous degradation curve. With such relaxation in a stress-measure cycle, test results can overestimate transistor life when it is used in a constantly on state. On the other hand, properly controlled relaxation might be the right kind of testing for a transistor that is turned on and off frequently. In this case, a traditional DC stress and degradation technique that doesn't allow for recovery effects may underestimate transistor life. Failing good devices is almost as costly as passing bad devices.

Similarly, devices subject to self-heating (such as SOI or power devices) may also be incorrectly characterized by DC testing. When a device is intended for fast-switching

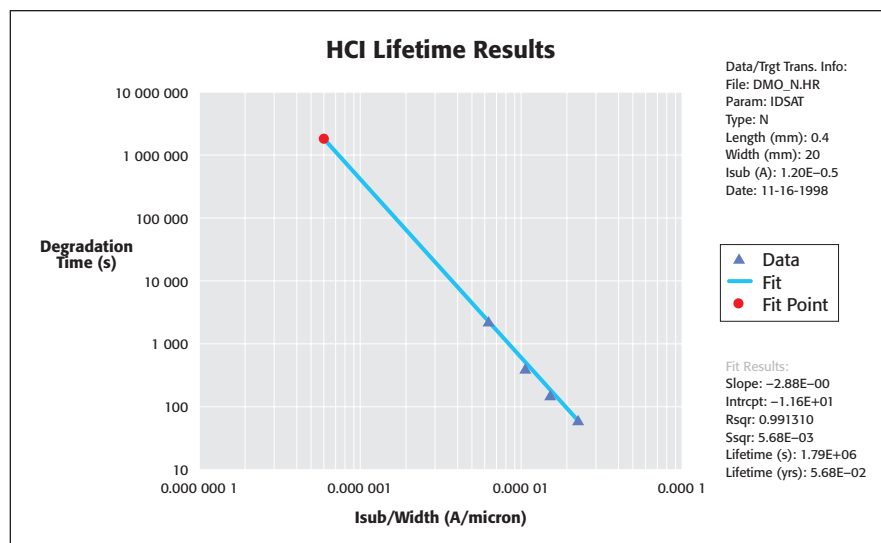


Figure 1. Example of lifetime reliability extrapolation from HCI testing.

but is tested with a DC method, thermal stresses unrelated to actual use can be introduced. Then extrapolated lifetime and performance characteristics are bound to be incorrect and misleading.

A better way of handling the dynamics of this problem is to use pulse stress instead of DC stress. With pulsing, the transistor is stressed in a more realistic way. Degradation of threshold voltage can be measured as a function of pulse frequency and measured without the artifacts caused by DC stress. This provides important information about the nature of recovery in different applications and depicts intrinsic operation of the device (without charge trapping or isothermal effects). This information can be used in technology development and circuit design to better manage lifetime and reliability issues.

### Development of High- $\kappa$ Gate Films

Use of the pulse technique is particularly important in qualifying high- $\kappa$  gate materials and production processes for MOSFET devices, which are still evolving. Many of these new technologies still have leakage currents higher than mature technologies, and there are a large number of interface states as well as traps in the materials. To characterize them fully, multiple measure-

ment techniques are typically required. Usually, these include DC I-V, Pulse I-V, C-V, and charge-pumping measurements.

A new technique, Single Pulse Charge Trapping (SPCT), uses a pulse generator to do fast I-V curves to either avoid charge trapping or measure charge trapping as a function of a device's switching frequency. With some modeling work, SPCT can distinguish the initial charge-trapping centers from those created later in the film by voltage stresses. Another advantage of SPCT is its simple and direct nature – test results can be compared to a DC measurement without resetting the system hardware or moving the wafer to another station.

The key to success in SPCT is to control switching time and relaxation of trapped charges between force and measurement. Therefore, it requires short pulses with fast (nanoseconds) rise and fall times, instead of using DC testing as commonly found in older test systems. With these ultra-short pulses, you can control the amount of injected charge, see if there is any interface damage due to stress, and determine how the damage affects charge trapping behavior.

To characterize transistors with different functionalities, including high frequency operation, the best modeling comes from instrumentation that avoids artifacts associ-

ated with DC or slower pulse measurements. Modeling engineers can use ultra-short pulse data to better depict real device performance and optimize designs for actual operating conditions. Process engineers also need these data to characterize and track improvements in film quality and device degradation. In both cases, the results are better lifetime predictions and reliability.

The core instrumentation requirement for SPCT is a semiconductor characterization system with multiple source-measure units (SMUs) and pre-amps that provide sub-femtoamp resolution for gate leakage current measurements. It also requires an ultra-short pulse generator, and measurement bandwidth high enough to capture device responses down to tens of nanoseconds. Commercial test systems of this type are now available. For instance, the Keithley Model 4200-SCS Semiconductor Characterization System now has a Pulse I-V (PIV) option in a completely integrated bench-top package with simplified PIV software that quickly delivers accurate charge trapping data, or operational data without self heating. These capabilities are essential in shortening the time-to-market for leading edge researchers working beyond the 90nm node with high- $\kappa$  materials, thermally sensitive devices, and advanced memory designs. KEITHLEY

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