Pulsed Characterization of Charge-trapping Behavior in High-κ Gate Dielectrics

Yuegang Zhao, Keithley Instruments, Inc.

Chadwin D Young, Rino Choi, and Byoung Hun Lee, SEMATECH High-κ Material Research

This article discusses the nature of the charge trapping and the limitation of DC characterization techniques in quantifying trapped charge. Then, it describes an ultra-fast pulse I-V technique for characterizing the intrinsic ("trap free") performance of high-κ gate transistors that exhibit the fast transient charging effect (FTCE).

Development of High-κ Gates for Advances CMOS Devices

High dielectric constant (high-κ) materials, such as hafnium oxide (HfO_2), zirconium oxide (ZrO_2), alumina (Al_2O_3), and their silicates, have drawn a great deal of attention in recent years for potential use as gate dielectrics in advanced CMOS processes [1]. With high dielectric constants, gate dieletrics can be made thicker than SiO_2 while achieving the same capacitance. The result is leakage current that can be lower by as much as several orders of magnitude. However, there are still technical challenges to overcome, such as V_t instability [2-4], carrier channel mobility degradation [5-9], and long-term device reliability [10-13].

One of the important issues preventing implementation of high-κ gates is the trapping of charges in the pre-existing traps inside these dielectrics [14-15]. When the transistor is turned on, some of the channel carriers will be accumulated in the gate dielectric due to the vertical electrical field, resulting in a shift of threshold voltage and a reduction in drain current. Fully understanding charge-trapping and these related mechanisms is the key to understanding channel mobility degradation and device reliability problems. However, traditional DC testing techniques may not accurately characterize these mechanisms.

Limitation of DC Characterization Techniques

As charges are trapped in the gate dielectric, the threshold voltage of the transistor increases due to the built-in voltage in the gate capacitor; therefore, the drain current decreases. It appears that charge trapping and de-trapping times strongly depend on the composition of the gate stacks, i.e., physical thickness of the interfacial SiO_2 layer and high-κ film, as well as process techniques [16-18]. The time scale varies from several microseconds to tens of milliseconds [19]. The de-trapping of the charges is also strongly gate voltage and polarity dependent.

The wide dynamic range of charge trapping, and the voltage dependent trapping and de-trapping, make it very difficult to use one type of characterization technique (especially a DC technique) to get a complete picture of what is going on inside the stacked gate dielectric. For example, commonly used methods employ a double sweep in either DC V_{gs}-I_d or high frequency C-V measurements. These techniques involve ramping gate voltage back and forth while drain current or gate capacitance is measured. If hysteresis is seen on the resulting I-V or C-V curves, it is a clear indication of charge trapping inside the gate stacks.

The issue with this technique is that the hysteresis is strongly dependent on measurement time. The hysteresis measured in the DC I-V test could be different from that in a C-V test, because the time taken for each measurement may be dramatically different. This is illustrated by dual sweep C-V measurements taken at different speeds (***Figure 1***). Test speed is strongly dependent on instrumentation and not easily controlled. Even if it were, there is no model to quantify how much charge is really trapped in the gate during the test; i.e., hysteresis cannot quantify the amount of charge trapped, since a significant portion of the fast transient trapping could be lost in the DC measurement.

Another method involves DC stress voltage to inject charges intentionally into the gate, then the use of C-V or I-V method to

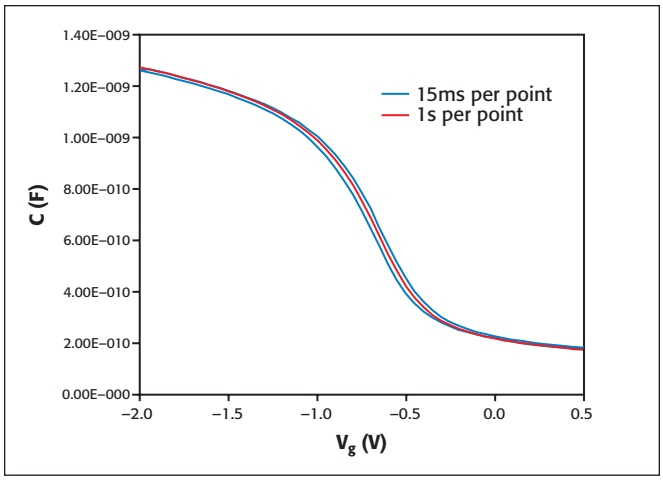

Figure 1. Time-dependent hysteresis of C-V: Slower measurements produce less hysteresis, indicating an equilibrium condition has been reached. Moreover, hysteresis cannot quantify fast transient trapping, since a significant portion of the fast transient trapping could be lost in the DC measurement.

measure the flat band voltage or threshold voltage shift [20]. The amount of charge trapped can be calculated based on this formula:

$$Q_{trap} = C_{gate} \cdot \Delta V_{fb}, \text{ or } Q_{trap} = C_{gate} \cdot \Delta V_{I}.$$

The issue with this technique is the transition period between DC stress and I-V or C-V measurement, when typically there is no applied voltage, or voltage is very low compared to the stress condition. When stress voltage is off, the charges trapped in the gate can de-trap in as little as tens of microseconds. So, only a fraction of the total trapped charges are measured due to the relaxation effect, resulting in an overly "optimistic" view of the film's quality.

Ultra-short Pulse Characterization Techniques

Better methods have been developed over the past few years [3, 4, 19, 21] for capturing the fast transient behavior of charge trapping. ***Figure 2*** shows two different test configurations for a Single Pulse Charge Trapping (SPCT) measurement. In both setups a pulse is applied to the gate of the transistor while its drain is biased at a certain voltage. The change in drain current, resulting from the gate pulse, appears on the digital oscilloscope.

The difference between these two configurations is that the one in ***Figure 2b*** has much higher bandwidth than the one in ***Figure 2a***; therefore, it can capture much faster pulse responses (down to tens of nanoseconds). At such high speed, the bulk traps in a high-κ layer are unlikely to respond; therefore, an "intrinsic" transistor response with negligible charge-trapping effect can be measured.

The key to using SPCT is to look at charge trapping and de-trapping within a single, well-configured gate pulse (***Figure 3***). The pulse usually starts in a position that discharges the gate capacitor before the voltage ramp begins. This is to clean up any residual charges trapped in the gate. Then, during the rise time of the voltage ramp, the corresponding drain current response is captured, allowing a V_{gs}-I_d curve to be formed.

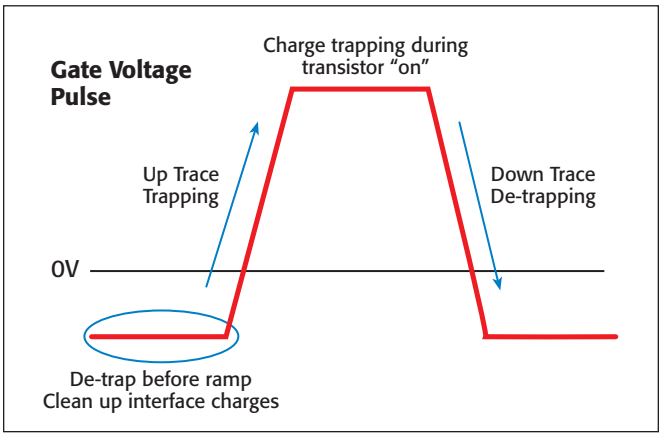

Figure 3. Trapping and de-trapping in single gate voltage pulse.

If the pulse rise time is fast enough that there is no charge trapping, then the V_{gs}-I_d curve represents the transistor's intrinsic behavior, free from error due to spurious charge-trapping effects [16]. During the plateau of the pulse, the transistor is turned on, and some of the channel carriers might be trapped in the gate, which changes the threshold voltage and causes the drain current to drop. During the fall time of the pulse, another V_{gs}-I_d curve is formed, but with the charge-trapping effect that should be measured.

Figure 4a shows an example of a pulse I-V measurement with different pulse speeds using setups from ***Figures 2a*** and ***2b*** respectively. A DC I-V curve is overlaid for comparison. There is hysteresis with

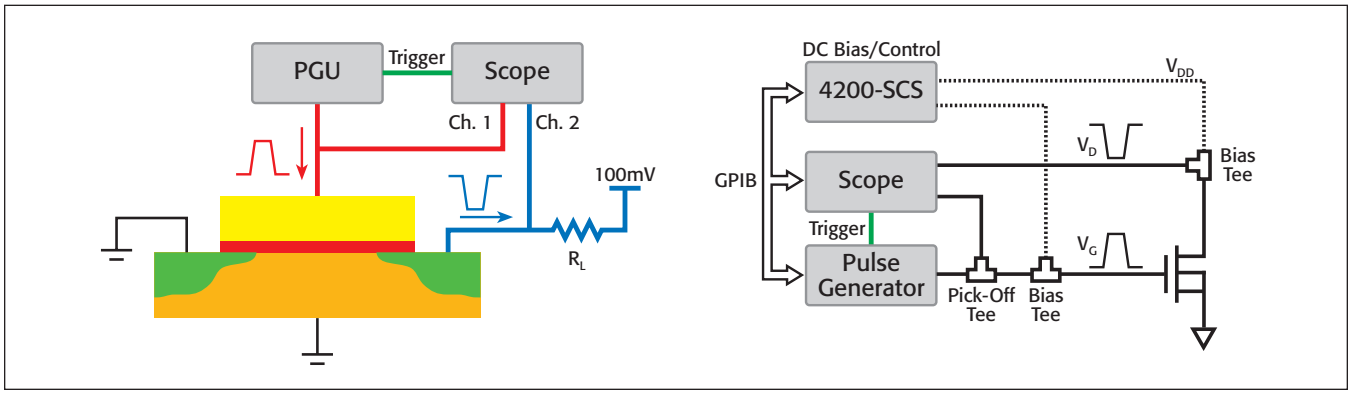

Figure 2. Two different pulse I-V test setups to study transient charge trapping: (a) pulse generator unit (PGU) and scope; (b) integrated test system with hardware and software designed specifically for fast transient trapping measurements.

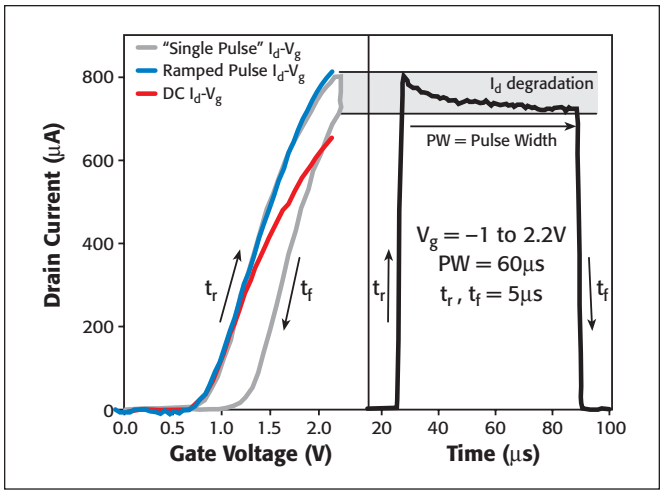

Figure 4. Single Pulse Charge Trapping measurements: (a) the ultra-short ramped pulse I_d-V_g and slow "single pulse" pulse with hysteresis (DC result is shown as a reference), and (b) corresponding slow pulse versus time illustrating an alternative approach to determine the degradation of I_d.

the slower pulse due to charge trapping. By using the faster pulse, hysteresis is eliminated because there's insufficient response time for charges to be trapped.

Slower pulse measurements should only be used for high-κ devices with relatively low charge-trapping effects. Although the hysteresis of a slower pulse I-V curve can quantify charge trapping better than a DC method, results must be interpreted with caution, since de-trapping effects are influenced by the specific structure of the gate stack and the pulse fall time. Also, when two traces in the tr and tf portions are not parallel, it is difficult to define the point at which hysteresis is measured.

An alternative approach is to plot pulse I_d versus time (***Figure 4b***). An evaluation of the pulse width portion of I_d (where I_d degrades) can be used to quantify trapped charge [15, 16]. Still, to ensure negligible charge trapping during the entire pulse, one can use a fast pulse with short rise and fall times. This can be achieved easily with the ultra-short-pulse test system in ***Figure 2b***. It produces I_d-V_g values by using a single pulse per point of less than 100ns.

Benefits of Short Pulse Characterization

Since there is much less charge-trapping effect with very short pulse widths, the drain current measured is higher than under DC conditions (red curve, ***Figure 4a***). This results in a higher predicted channel carrier mobility when pulse I-V data are used to generate a model, which is more representative of transistors that are switching very fast (i.e., those that will not experience full charge-trapping effects). Another advantage of the ultra-short pulse system is that the pulse I-V measurements, with pulse widths on the order of nanoseconds, can be performed very easily and results can be compared to a DC measurement without resetting the system hardware or moving the wafer to another station. Such a comparison is shown in ***Figure 5***.

Drive current measured using the pulse I-V technique can be significantly higher than DC due to the lack of charge-trapping effects. This illustrates the close-to-intrinsic performance of transistors with high-κ gate dielectrics, and ultimately demonstrates the advantage of the ultra-short pulse I-V technique.

Because of complications associated with trying to characterize charge-trapping effects for transistors with different functionalities, including high frequency operation, the best solution for modeling engineers is to use instrumentation and a test configuration that avoids artifacts associated with DC or slower pulse measurements. The ultra-short pulse measurement technique provides a better depiction of real device performance [22], so the resulting models help optimize designs for actual operating conditions.

Process engineers also need these pulse measurement techniques to characterize and track improvements in their continuing efforts to improve film quality and remove charge-trapping degradation. Finally, an understanding of the intrinsic behavior of high-κ gate dielectric devices is key to understanding the physics of charge trapping

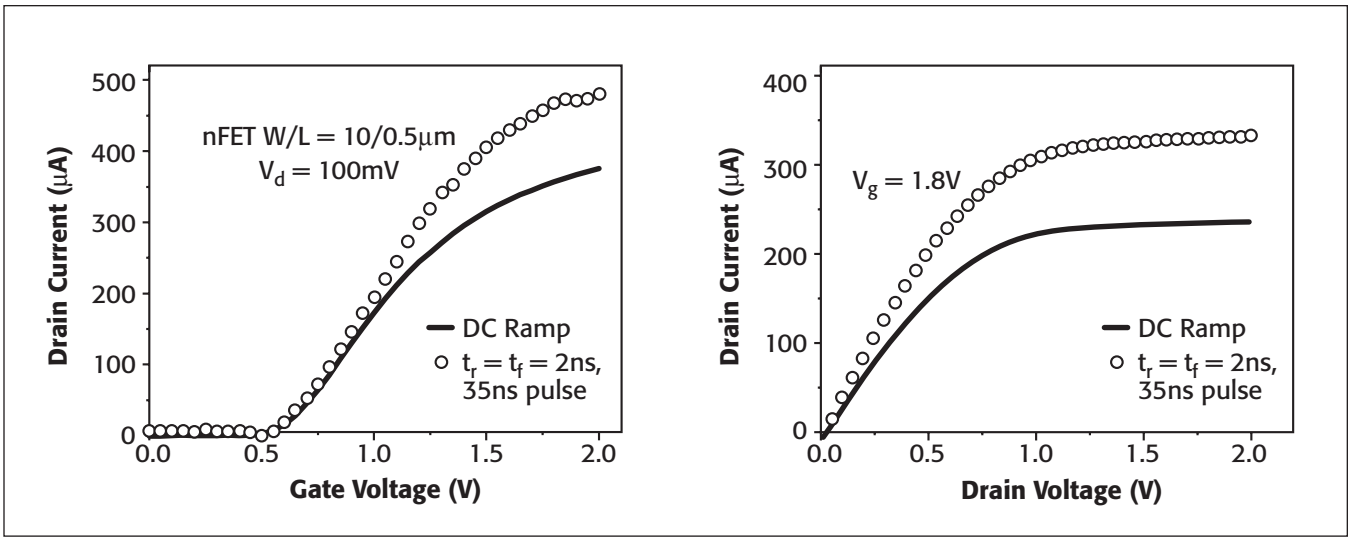

Figure 5. Overlay of ramped pulse I-V and DC I-V measurements on NMOSFET with high-κ (HfO2) gate dielectric: (a) DC and pulsed Id-Vg measurement at linear region, (b) DC and pulsed Id-Vd measurement. Short pulse parameters allowed close-to-intrinsic drive current to be measured and compared to the DC measurement.

and de-trapping. This physical-based understanding leads to the correct extrapolation of device lifetime.

Sources of Error

Although ultra-short pulse measurements are a powerful technique, recognize that speed characteristics are in the radio frequency (RF) domain. Therefore, it is easy to introduce measurement errors if the test system is not optimized for high bandwidth. There are three main sources of errors: signal losses due to cables and connectors, losses due to device parasitics, and contact resistance.

Signal losses due to cables and connectors, as well as contact resistance effects, can be calibrated out using a transistor with a SiO_2 gate, where there is no charge-trapping effect. The pulse I-V curve should overlay the DC I-V curve precisely once the calibration is complete.

However, device parasitics, usually parasitic capacitance between pad contacts, cannot be easily removed. This will reduce the pulse current from the drain terminal. This problem can be designed out by using RF-compatible transistor structures (Ground-Signal-Ground), and by increasing pad pitch so that capacitance between the pads is small enough not to affect pulse current measurements.

Conclusion

DC characterization techniques are inadequate for capturing the dynamic nature of charge trapping in high-κ gate stack structures. Pulse I-V is a powerful technique that allows characterizing transistors with high-κ gate stacks in a trap-free environment that permits assessing their intrinsic qualities. When current is measured in a shorter time than that associated with the charge-trapping time scale, improved intrinsic transistor characteristics can be achieved, including a drive current that is significantly higher than that measured with traditional DC I-V techniques. KEITHLEY

New Test System Solutions

The Keithley Model 4200-SCS Semiconductor Characterization System offers new solutions for characterizing advanced materials and devices. These include a pulse generation and measurement option, and stress-measure reliability testing software.

The new Pulse I-V (PIV) package for the Model 4200-SCS comes in a completely integrated and compact form factor to satisfy the growing need for pulsed testing in leading edge semiconductor development. This is the first commercial benchtop system capable of doing PIV with less than 100ns pulse widths, in addition to DC measurements. It is supplied with patent pending PIV software and simplified interconnects so users do not have to grapple with racks of equipment, complicated wiring connections, internally developed software, and questionable test data. The result is superior measurements and faster time-to-market for leading edge researchers working beyond the 90nm node with high-κ materials, thermally sensitive devices, and advanced memory. The PIV package can be ordered for new units, or applied to existing Model 4200-SCS systems in the field.

The KTEI 6.0 software and wafer level reliability test enhancements allow engineers to easily put different measurement techniques together for timely data collection. The hardware is configurable from two to eight SMUs. An optional preamp has 0.1fA resolution. The Model 4200-SCS can also control other instruments, such as a switch matrix, C-V meter, and pulse generator without user programming. This can be done using GPIB, Ethernet, or RS-232. The interactive software has a test plan manager with an enhanced wafer level stress-measure loop, interactive test setup interface, Excel-like data sheet, easy graphing capability, and more. The Model 4200-SCS also has the flexibility to be used in an interactive manual mode (for single test operation during development), or in more automated production use cases.

References

[1] E. Gusev, E. Cartier, D. Buchanan, M. Gribelyuk, M. Copel, H. Okorn-Schmidt, and C. D'Emic, in Proc. of Conference on Insulating Films on Semiconductors, 2001.

[2] A. Kerber, E. Cartier, L. Pantisano, R. Degraeve, T. Kauerauf, Y. Kim, A. Hou, G. Groeseneken, H. E. Maes, and U. Schwalke, "Origin of the threshold voltage instability in SiO2/HfO2 dual layer gate dielectrics," IEEE Electron Device Lett., vol. 24, pp. 87, 2003.

[3] A. Kerber, E. Cartier, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke, "Characterization of the VT instability in SiO2/HfO2 gate dielectrics," in Proc. 41st Annual IEEE Intl. Reliability Physics Symp., p. 41-45, 2003.

[4] C. D. Young, R. Choi, J. H. Sim, B. H. Lee, P. Zeitzoff, Y. Zhao, κ. Matthews, G. A. Brown, and G. Bersuker, "Interfacial Layer Dependence of HfSixOy Gate Stacks on Vt Instability and Charge Trapping Using Ultra-short Pulse I-V Characterization," in Proc. 43rd Annual IEEE Intl. Reliability Physics Symp., p. 75-79, 2005.

[5] M. Fischetti, E. Cartier and D. Neumayer, J. Appl. Phys., 90, p. 4587, 2001.

[6] A. Kerber, et al., VLSI, p. 159 (2003).

[7] W. Zhu, J.-P. Han, and T. P. Ma, "Mobility Measurements and Degradation Mechanisms of MOSFETs Made With Ultrathin High-κ Dielectrics," IEEE Transactions on Electron Devices, vol. 51, p. 98-105, 2004.

[8] C.D. Young, IEEE Electron Device Letters, vol. 26, no. 8, p. 586, 2005.

[9] D. V. Singh, P. Solomon, E. P. Gusev, G. Singco, and Z. Ren, "Ultra-fast Measurements of the Inversion Charge in MOSFETs and Impact on Measured Mobility in High-κ MOSFETs," in IEEE Intl. Electron Devices Meeting Tech. Digest, p. 863-866, 2004.

[10] E.Gusev, et al., Appl. Phys. Lett., vol. 83, p.5223, 2003.

[11] B.H. Lee, R. Choi, J.H. Sim, S.A. Krishnan, J.J. Peterson, G.A. Brown, and G. Bersuker, "Validity of Constant Voltage Stress Based Reliability Assessment of High-κ Devices," IEEE Transactions on Device and Materials Reliability, vol. 5, no. 1, p. 20-25, 2005.

[12] S. Zafar, A. Kumar, E. Gusev, and E. Cartier, "Threshold Voltage Instabilities in High-κ Gate Dielectric Stacks," IEEE Transactions on Device and Materials Reliability, vol. 5, no. 1, p. 45-64, 2005.

[13] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, G. Ghibaudo, "Review on High-κ Dielectrics Reliability Issues," IEEE Transactions on Device and Materials Reliability, vol. 5, no. 1, p. 5-19, 2005.

[14] G. Bersuker, et al., Materials Today, 7, p.26., 2004.

[15] G. Bersuker, J. H. Sim, C. D. Young, R. Choi, B. H. Lee, P. Lysaght, G. A. Brown, P. Zeitzoff, M. Gardner, R. W. Murto, and H. R. Huff, "Effects of Structural Properties of Hf-Based Gate Stack on Transistor Performance," presented at 2004 Spring Meeting of the Material Research Society, p. 31-35, 2004.

[16] C. D. Young, R. Choi, J. H. Sim, B. H. Lee, P. Zeitzoff, Y. Zhao, k. Matthews, G. A. Brown, and G. Bersuker, "Interfacial Layer Dependence of HfSixOy Gate Stacks on Vt Instability and Charge Trapping Using Ultra-short Pulse I-V Characterization," presented at the

43rd Annual IEEE Intl. Reliability Physics Symp. Proc, p. 75-79, 2005.

[17] R. Choi, S.J. Rhee, J.C. Lee, B.H. Lee, and G. Bersuker, "Charge Trapping and Detrapping Characteristics in Hafnium Silicate Gate Stack Under Static and Dynamic Stress," IEEE Electron Device Lett., vol. 26, no. 3, p. 197-199, 2005.

[18] J.H. Sim, R. Choi, B.H. Lee, C.D. Young, P. Zeitzoff, D.-L. Kwong, and G. Bersuker, "Trapping/De-trapping Gate Bias Dependence of Hf-Silicate Dielectrics with Poly and TiN Gate Electrode," Jpn. J. of Appl. Phys., vol. 44, no. 4B, p. 2420-2423, 2005.

[19] C. Leroux, J. Mitard, G. Ghibaudo, X. Garros, G. Reimbold, B. Guillaumor, F. Martin, in IEEE Intl Electron Devices Meeting Tech Digest. p.737-740, 2004.

[20] S. Zafar, S. Callegari, V. Narayanan,, and S. Guha, "Impact of Moisture on Charge Trapping and Flatband Voltage in Al2O3 Gate Dielectric Films," Applied Physics Letters, vol. 81, p. 2608, 2002.

[21] C.D. Young, Y. Zhao, M. Pendley, B.H. Lee, κ. Matthews, J.H. Sim, R. Choi, G.A. Brown, R.W. Murto and G. Bersuker, "Ultra-Short Pulse Current-Voltage Characterization of the Intrinsic Characteristics of High-κ Devices", Jpn. J. of Appl. Phys., vol. 44, no. 4B, 2437, 2005.

[22] C. Y. Kang, R. Choi, J. H. Sim, C. Young, B. H. Lee, G. Bersuker, Jack C. Lee, "Charge trapping effects in HfSiON dielectrics on the ring oscillator circuit and the single stage inverter operation," in IEEE Intl Electron Devices Meeting Tech Digest, p. 485-488, 2004.

About the Authors

Yuegang Zhao received his MBA from Case Western Reserve University (2005), M.S. in Semiconductor Physics from the University of Wisconsin, Madison (2000), and his B.S. in Physics from Peking University, Beijing, China (1997). He joined the Semiconductor Business Group of Keithley Instruments Inc. in 2001 and is a lead applications engineer. He has worked on various device characterization and reliability test techniques including RF CV measurement on ultra-thin gate oxide, multi-site parallel NBTI testing with minimized relaxation, and pulse I-V characterization of high-κ gate and SOI devices. He has authored and co-authored more than 15 publications in the last two years in technical journals, magazines and conferences. He has two patents pending on pulse I-V test techniques.

Chadwin D. Young received his B.S. degree in Electrical Engineering from the University of Texas at Austin in 1996. He received M.S. and Ph.D. degrees from the North Carolina State University in 1998 and 2004, respectively. He held several internships until 2001 when he joined SEMATECH. Here, he completed his dissertation research on high-κ gate stacks. He now continues this research at SEMATECH as a project engineer specializing in pulse-based characterization methodologies for the evaluation of charge trapping properties in high-κ gate stacks. He has authored or co-authored more than 65 research publications and presentations.

Rino Choi received his Bachelor of Science and Master of Science degree in the Department of Inorganic Materials Engineering of the Seoul National University in 1992 and 1994, respectively. He received the Ph.D. in Materials Science and Engineering Program in 2002 from the University of Texas at Austin. From 1994 to 1999 he worked for Daewoo Motors Company as a development and test engineer. Since 1999, he has studied various high-κ dielectrics and published more than 50 journal and conference papers. Since his graduation he has been continuing the research on the electrical characterization and reliability of advanced gate stacks at SEMATECH.

Byoung Hun Lee received a B.S. (1989) and a M.S. (1992) in Physics from Korea Advanced Institute of Science and Technology and Ph.D. (2000) in electrical and computer engineering from the University of Texas at Austin. He worked at Samsung semiconductor (1992-1997) and has been with IBM since 2001. He has authored and co-authored more than 190 journal and conference papers in various semiconductor research areas, including gate oxide reliability, SOI devices and processes, strained silicon devices, and high-κ and metal gate processes and devices. He is currently on assignment to SEMATECH as a manager in the advanced gate stack program, managing advanced clean, dielectric, electrode, baseline, and electrical characterization projects.

KEITHLEY INSTRUMENTS, INC. ■ 28775 AURORA ROAD ■ CLEVELAND, OHIO 44139-1891 ■ 440-248-0400 ■ Fax: 440-248-6168 ■ 1-888-KEITHLEY ■ www.keithley.com

BELGIUM
Sint-Pieters-Leeuw
Ph: 32-2363-0040
Fax: 32-2363-0064
www.keithley.nl

CHINA
Beijing
Ph: 8610-82255010
Fax: 8610-82255018
www.keithley.com.cn

FINLAND
Espoo
Ph: 358 9 88171661
Fax: 358 9 88171662
www.keithley.com

FRANCE
Saint-Aubin
Ph: 33-1-6453-2020
Fax: 33-1-60-1-77-26
www.keithley.fr

GERMANY
Germering
Ph: 49-89-84-93-070
Fax: 49-89-84-93-0734
www.keithley.de

UNITED KINGDOM
Theale
Ph: 44-118-929-7500
Fax: 44-118-929-7519
www.keithley.co.uk

INDIA
Bangalore
Ph: 91-80-2212-8027
Fax: 91-80-2212-8005
www.keithley.com

ITALY
Milano
Ph: 39-02-55 38 421
Fax: 39-02-55 38 42 28
www.keithley.it

JAPAN
Tokyo
Ph: 81-3-5733-7555
Fax: 81-3-5733-7556
www.keithley.jp

KOREA
Seoul
Ph: 82-2-574-7778
Fax: 82-2-574-7838
www.keithley.co.kr

MALAYSIA
Kuala Lumpur
Ph: 60-3-4041-0899
Fax: 60-3-4042-0899
www.keithley.com

NETHERLANDS
Gorinchem
Ph: 31-1-836-35333
Fax: 31-1-836-30821
www.keithley.nl

SINGAPORE
Singapore
Ph: 65-6747-9077
Fax: 65-6747-2991
www.keithley.com.sg

SWEDEN
Solna
Ph: 46-8-509-04-600
Fax: 46-8-655-26-10
www.keithley.com

TAIWAN
Hsinchu
Ph: 886-3-572-9077
Fax: 886-3-572-9031
www.keithley.com.tw

Printed in the U.S.A. No. 2767 0506