Parallel Parametric Measurements Reduce Test Costs

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As the dimensions of modern integrated circuits continue to shrink, device fabrication and parametric testing have become more challenging. Every device shrink, process innovation, and new material makes the volume and repeatability of parametric test data more critical in process development and the control of modern fabs. Today's fabs must understand how to produce and characterize advanced materials such as high-κ gate dielectrics and low-κ insulators used in conductive layers – quickly and cost-effectively. Tomorrow's IC producers may need to manufacture and test transistors formed from carbon nanotubes or other technologies that researchers have just begun to explore.

Parallel Test Practices

By way of definition, wafer-level parallel parametric testing involves concurrent execution of multiple tests on multiple scribe line test structures. It offers enormous potential for increasing the throughput of existing test hardware.

Increasing market pressures are driving fabs to minimize test times and explore the benefits of parallel testing. This methodology offers a relatively inexpensive way to increase test throughput with existing parametric test systems, thereby lowering significantly the cost of ownership and total cost of testing. Just as important, parallel testing can address the growing need to perform more tests on the same structures in less time as device scaling increases the randomness of failures. By extracting more data from every probe touchdown, parallel test offers fabs the flexibility to choose whether they want to increase their wafer test throughput dramatically, or use the available time to acquire significantly more data and thereby gain greater insight into production processes.

At the present time, structures being tested in parallel are typically located within a single Test Element Group (TEG). Few IC manufacturers test structures in different TEGs simultaneously. To implement this strategy the parametric tester's controller is used to inter-leave execution of multiple tests in a way that maximizes available processing time and test instrumentation capacity, which might otherwise have idle periods. With proper test structure design, this "multi-threaded" sequencing reduces execution time for multiple tests on multiple structures to little more than the time needed to execute the longest test in a sequence.

Comparison of parallel and sequential test modes – In traditional parametric testing, each measurement in a test sequence must be completed before the next one begins. I.e., tests run consecutively, synchronized so that the start of the next test sequence begins upon conclusion of the prior sequence. Total test time for an individual TEG is approximately the sum of test times for individual devices, plus the significant delays that can occur due to switching latencies.

In parallel testing, the sequences are coordinated, but tests in a given sequence run more or less at the same time. In an ideal sequence, all parallel tests would start simultaneously and chain together with no delays in each thread. In reality, there are slight delays between the start times of each test sequence due to prober, controller, and parametric tester latencies. See ***Figure 1***.

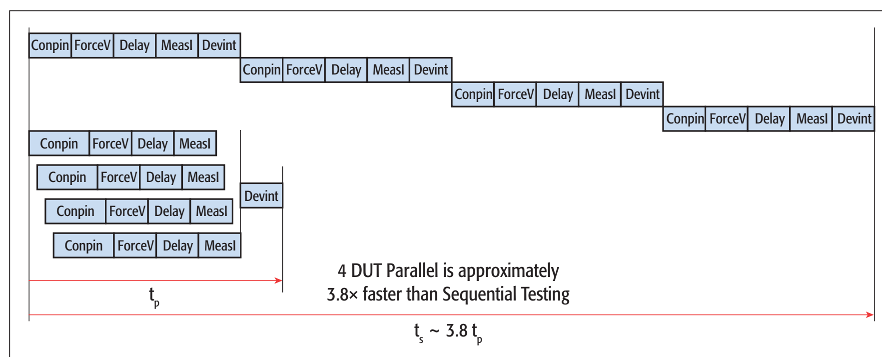


Figure 1. Comparison of elapsed times between sequential and parallel testing of four DUTs. The sequential test time (t_s) is approximately 3.8 times longer than the parallel test time (t_p).

Modern parametric testers can be fitted with as many as eight source-measure units (SMUs), though most systems have less. For the sake of argument, if a tester configured with eight SMUs was operated sequentially for simple tests such as measuring resistance (which requires only one SMU for the two measurement nodes), then seven SMUs would sit idle. Parallel testing increases utilization of all test cell resources (prober, parametric tester, and other instruments) by measuring multiple devices simultaneously and thereby dramatically increases throughput.

This is true whether test structures are the same type (homogenous) or different (heterogeneous). A heterogeneous example is shown in ***Figure 2***. It consists of two transistors, one resistor, and one diode, which could be measured independently and asynchronously by performing different connect-force-measure sequences on all devices simultaneously.

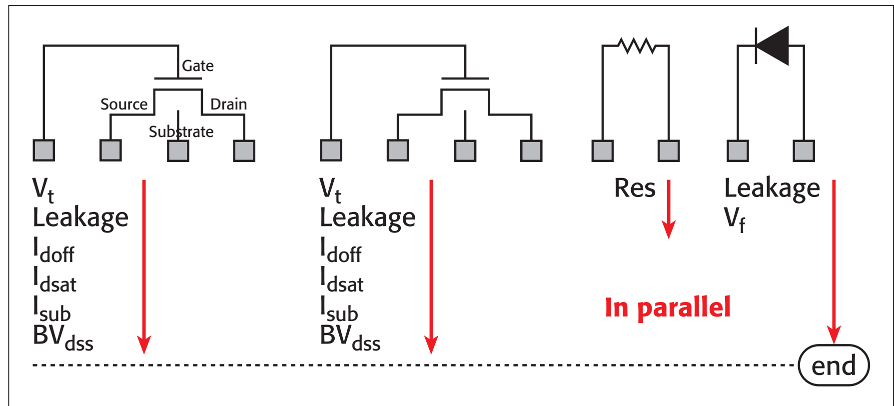


Figure 2. Example of parallel testing on four heterogeneous devices within a single TEG.

Wafer-level parallel parametric test vs. parallel functional test – Although the concept of parallel testing has been discussed extensively in the semiconductor industry over the last few years, many of those discussions focus on parallel functional testing of packaged components, rather than on wafer-level parallel parametric test. As you may imagine, instrumentation for these two types of parallel testing tend to be quite different. For example, Keithley's Model 4500-MTS Multi-Channel I-V Test System and its Series 2600 System SourceMeter® Multi-Channel I-V Test Solutions can be applied to parallel functional test applications. Keithley's S680 Automatic Parametric Test Systems fall into the wafer-level parallel parametric test category.

Both types of parallel testing use multiple SMUs operating asynchronously to reduce total test time, but there are obvious differences. First, the size and cost of test hardware is drastically different. Second, functional tests on packaged devices are largely immune to the parasitic capacitances between devices under test that interfere with parametric test accuracy, regardless of whether tests are performed sequentially or in parallel. In addition, parallel functional testing typically supports the use of channel groups for testing multiple devices and adaptive testing that eliminates further tests on failed devices. However, parallel parametric testing can also be combined with adaptive testing to further improve wafer test throughput.

Parallel parametric test vs. adaptive test – Adaptive testing also has the potential for increasing test throughput. This can be used with or without parallel test. In results-based adaptive testing, a parametric tester software module allows programming that increases or decreases the number of wafer sites tested and the number of tests performed, based on the results of previous measurements. See the associated sidebar for more details.

A Continuum of Parallel Test Strategies

It's important to remember that the approach to parallel testing may not be the same for all fabs (or even all test cells within the same fab). Rather than a single strategy, it's more productive to think of parallel test implementation as a continuum. The point on the continuum that's most appropriate for a particular fab or test cell will depend on a number of factors, including manufacturing technology, the maturity of production processes and TEGs, and the anticipated product lifespan (i.e., how long the fab will continue to manufacture the product). The following sections describe the end points and midpoint of this implementation continuum.

Pick the "low hanging fruit" – For many fabs or test cells with mature processes, this approach to parallel test will be the most attractive because it involves changing only the test sequencing on existing TEGs. Typically, this requires analysis of the TEG and test sequence, with the aim of reordering or regrouping existing tests on heterogeneous structures to minimize the time in switching between test pads. This approach is usually the fastest, surest way to achieve significant throughput improvements with a relatively limited investment in analysis, new software, and test sequence modifications.

Doing the heavy lifting – This point in the continuum demands much more extensive analysis of both the test sequence and the TEG and requires significant changes in both. Usually, a number of new reticles must be designed, manufactured, and validated to allow parallel testing of more test structures within the TEG. This point in the parallel test continuum may also require changes to the probe card design, as well as the installation of additional SMUs. While it's important for prospective users to understand the expense and time required at this point in the continuum, for many fabs the throughput gains and additional data collection that parallel testing allows may justify the effort.

Plowing the "green field" – When developing the technology for new products, it's relatively inexpensive to design TEGs that maximize the number of structures that can be tested in parallel. Since reticles and test sequences are also being developed at this time, the disruption of a testing process is not an issue. While this point in the continuum offers the greatest potential payback in the form of higher throughput, it's better to not try parallel test for the first time on a new product. There are too many other pressing issues to be resolved when ramping up production. As described earlier, it's better to first implement parallel test on mature processes and later apply the knowledge gained from that experience to implement it on new products. In any case, take advantage of parametric test vendors who can

supply valuable assistance by reviewing test structures and algorithms and may make it possible to ramp up parallel test technology significantly faster.

Weighing the Advantages of Parallel Test

Parallel parametric testing offers a variety of advantages over sequential testing:

Cost of ownership advantages – Clearly, a major advantage of parallel test is a reduction in cost of ownership (COO) of the parametric test system on which it is implemented. The main reason is that COO for a process or metrology tool is most sensitive to system throughput. By increasing throughput, parallel test decreases the system's cost of ownership. Depending on a variety of factors, users have experienced throughput increases from parallel testing that range from five percent up to a 75 percent. For a particular fab or test cell, the factors having the greatest impact on throughput improvement are the following, which relate to test design:

The existing test structure and pad layout – When designing scribe line test structures, saving space has long been an important objective for many TEG designers. In order to minimize the amount of costly wafer real estate devoted to TEGs, designers have typically designed structures with shared gate pads, which can make it impossible to test certain structures in parallel.

The types of test structures within the TEG – Suppose a test structure is comprised of a transistor array, and all transistors share a single gate pad. It would be impossible to use parallel testing to fully characterize the transistors in such a structure. On the other hand, a resistor network would probably allow parallel testing of all the resistors, because such a structure could have a test pad at every node in the network. This allows the tester to source current across the entire network, and then measure the voltage drop at each node.

Most TEGs, however, fall somewhere in between these two extremes. A typical scenario is a TEG that includes one or more capacitors, resistors, diodes, and transistors. Although some of these test structures may in fact share pads, some degree of parallel testing is still possible. For example, it might be possible to measure the forward voltage drop of a diode and the resistance of a resistor in parallel, even if they are connected in series, as long as there is a pad at the node where the two structures connect. Similarly, it's likely that one can measure the resistance of a polysilicon line, the leakage of a capacitor, and the reverse leakage of a diode in parallel. Typically, however, C-V measurements are performed in sequence, because few testers have more than one C-V meter. There also is the potential for C-V measurements to form parasitic coupling with nearby structures or probe tips when C-V is conducted in parallel with other measurements.

Increased test cell capacity –For fabs that have limited make-up test capacity and floor space, parallel test can be an economical option that doesn't require a lot of resources. By allowing fabs to use existing test hardware and floor space more efficiently, parallel test may eliminate the need for additional test cells. This may also reduce the number of test cells needed in a new fab.

Other factors that help reduce the overall cost of test – Parallel test users report a variety of situations that have helped reduce their overall cost of parametric testing:

- **Avoiding the cost of new test cells:** Suppose a fab has three test cells and anticipates the need for increased test capacity due to a new product addition

Parallel Test vs. Adaptive Test

When weighing alternatives for improving parametric test throughput, fab managers often consider an adaptive testing strategy rather than parallel testing. While both represent valid approaches for reducing cost of ownership, they are very different in nature. A brief overview of adaptive testing may be helpful in understanding these differences.

Results-based adaptive testing allows programming the tester to increase or decrease the number of sites tested and the number of tests performed on a wafer based on the results of previous measurements. If the results from previous sites are acceptable, the number of sites and/or tests can be reduced, thereby increasing throughput when testing good wafers. When previous test results don't meet the pre-set criteria, adaptive test supports several different scenarios. If the test is used for process control, the tester can make extensive additional tests at the bad sites automatically (more tests, same TEG), so that a more complete set of parametrics is available for analysis by the process engineer if the lot is placed on hold. When used for lot dispositioning, the tester can perform the same tests at all die on the wafer automatically (same tests, more die), to determine known good die for final test. In either case, adaptive test can largely reduce or eliminate the time, expense, and errors involved in re-probing.

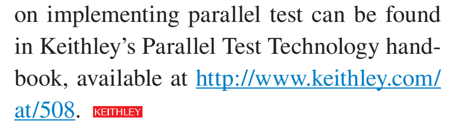
Most parallel parametric test experts would advise test managers against attempting to ramp up both parallel testing and adaptive testing at the same time because these techniques are based on differing strategies, even though both are designed to increase test throughput. Adaptive test requires setting thresholds that define what constitutes an acceptable or unacceptable wafer. Unacceptable wafers can trigger 100% testing of the remainder of the lot in order to gather additional data, which the process engineer can use in tracking down the source of the problem. In contrast, parallel testing, by clustering tests and structures for improved efficiency, already provides a larger data sample in less time, without relying on adaptive testing's reduced sampling strategy. Implementing either strategy can be a relatively complex and time-consuming process that may require a good amount of a test manager's attention for several months. Generally, it's preferable to implement parallel test first, to ensure that the test content is stable.

Serial sequential testing of multiple structures within a TEG results in the highest quality parametric measurements. Parasitic coupling can degrade some parallel measurements to some degree. Given that the process is not optimized to control parasitic coupling behaviors, the variability of the parasitic coupling results in a broader statistical distribution of parametric measurement results. This broader distribution could trigger adaptive testing to increase sampling. The adaptive test parameters may need to be adjusted to compensate for the broader statistical distributions.

or higher demand for an existing product. By increasing the throughput of each test cell by 30%, for example, parallel testing can preclude the need for another cell.

- **Reducing the cost of make-up capacity:** Fabs with relatively steady product demand may still need make-up test capacity to allow for production interruptions, such as maintenance, yield crashes, etc. Parallel testing can handle such disruptions without having to add more test cells.
- **Lower operator costs:** Fewer test cells require fewer operators—it's as simple as that. This also reduces operator training costs.
- **Gaining more insight into production processes:** Because parallel test increases throughput and provides more test capacity, this gives fabs the flexibility to add more tests to a test sequence without increasing costs. Gathering more information can help fabs gain a better understanding of production processes.
- **Lower cost of consumables:** Fewer test cells mean fewer consumable items, such as probe cards.

Readers may be interested in evaluating the impact of parallel testing on the overall Cost of Test for their specific semiconductor test floor operation. For that purpose, Keithley recommends Wright, Williams, and Kelly's TWO COOL® for Wafer Sort & Final Test software. More information on implementing parallel test can be found in Keithley's Parallel Test Technology handbook, available at http://www.keithley.com/at/508.



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